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A 2GHz GaN Class-J Power Amplifier for Base Station Applications

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1. INTRODUCTION

Need for reduction of base station power consumption while increasing QoS

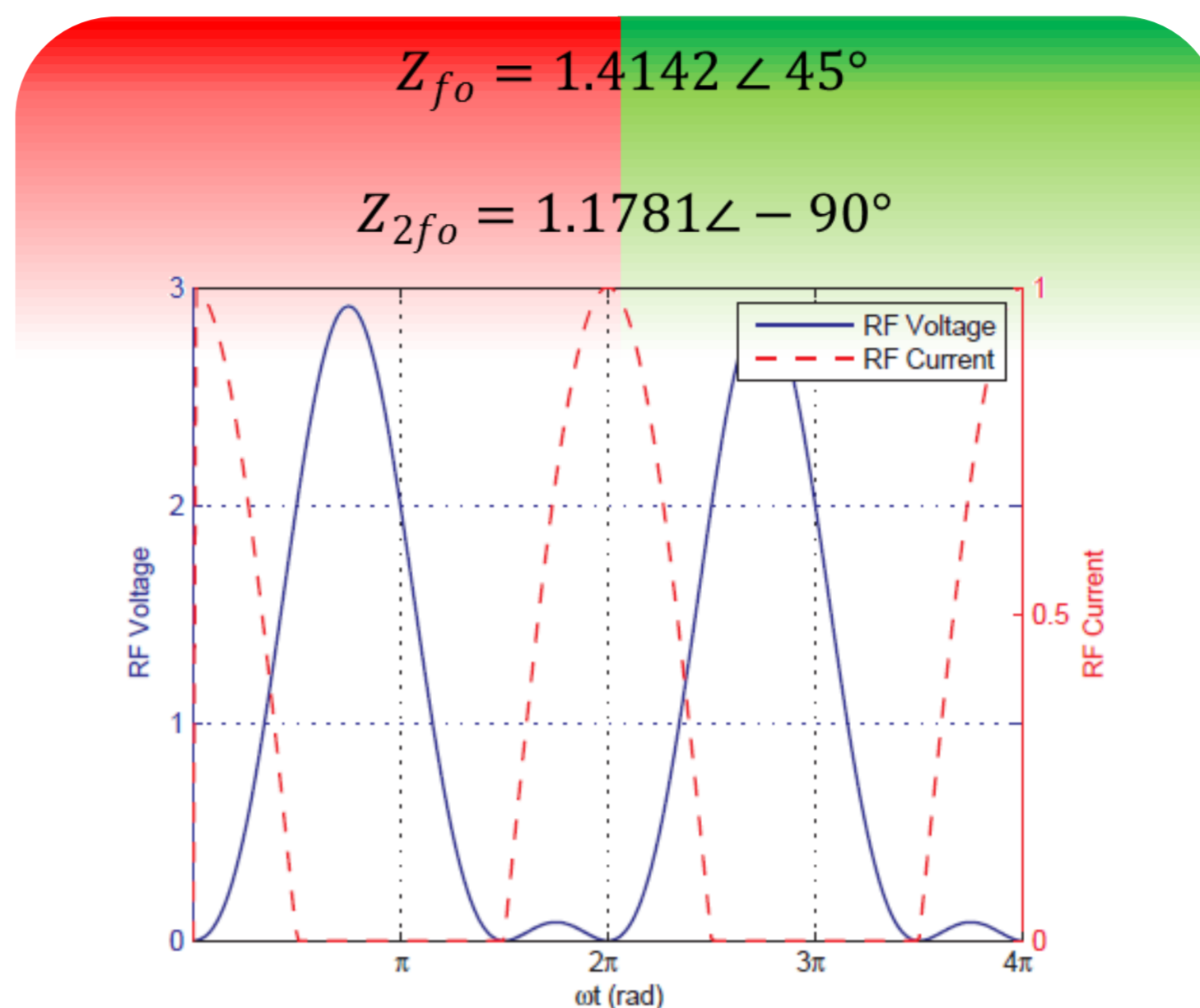
- Power Amplifier is a major power consumer
- High order constellations are necessary
- Channel bandwidths keep increasing

- **Efficient**
- **Linear**
- **Wideband**

Class-J

- Recently introduced (2006)
- **Complex fundamental impedance**
- **Reactive 2nd harmonic**
- **Continuous “design space”**
- Multiple impedance pairs (Z_{f_0} , Z_{2f_0})
- Class-B-like output power and efficiency
- Class-B / J / J* are specific sub-cases

2. CLASS-J THEORY



$$Z_{f_0} = \frac{\pi\sqrt{1+d^2}(1-\cos\frac{\alpha}{2})}{a-\sin\alpha} \angle \text{atan}\left(-\frac{1}{d}\right) + \varphi$$

$$\varphi = \begin{cases} \frac{\pi}{2}, & d \geq 0 \\ -\frac{\pi}{2}, & d < 0 \end{cases}$$

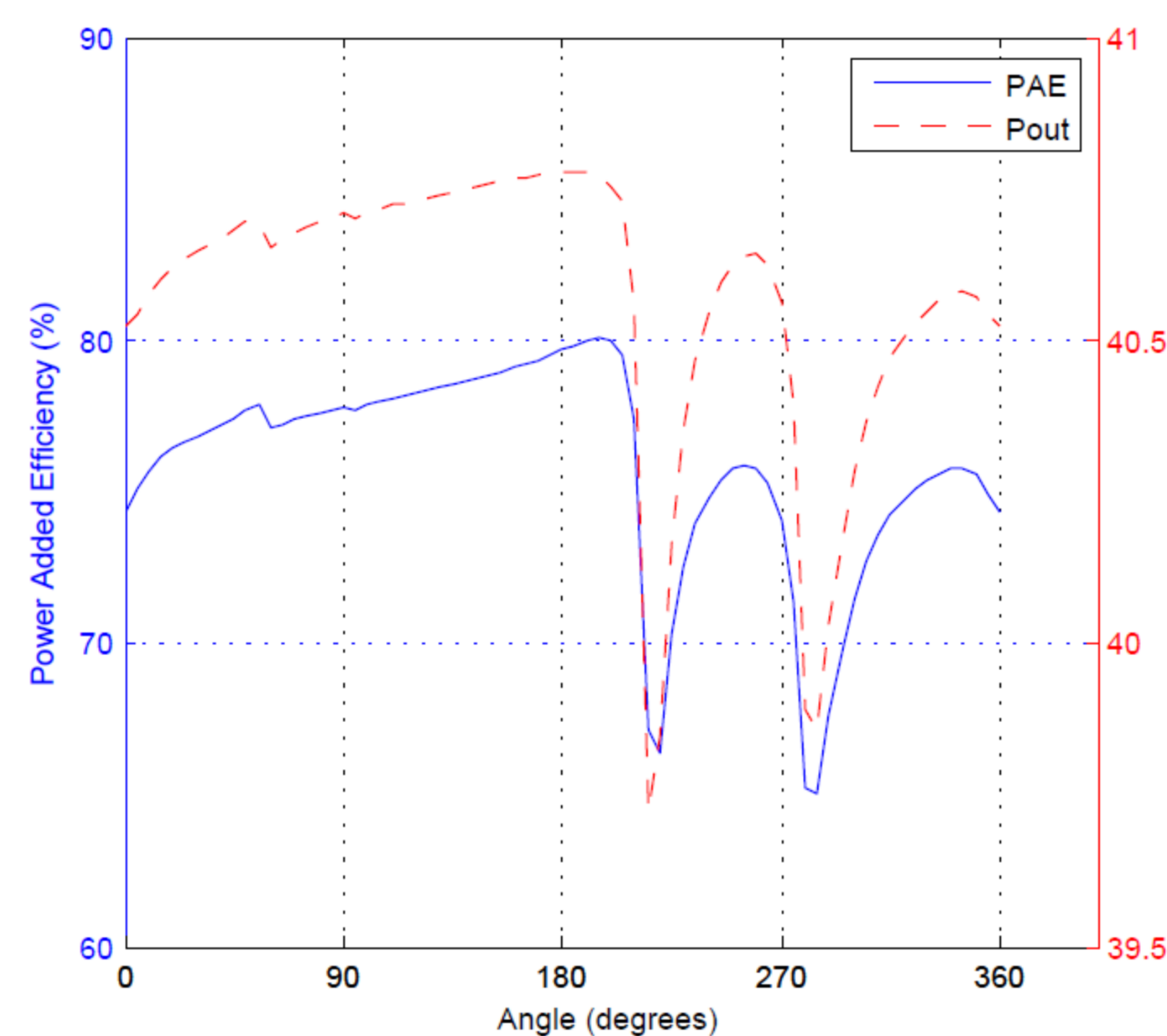
$$Z_{2f_0} = \frac{d}{2} \frac{\pi(1-\cos\frac{\alpha}{2})}{\sin\frac{\alpha}{2} - \frac{1}{3}\sin\frac{3\alpha}{2}} \angle -\frac{\pi}{2}$$

3. METHODOLOGY – REALIZATION OF THE POWER AMPLIFIER

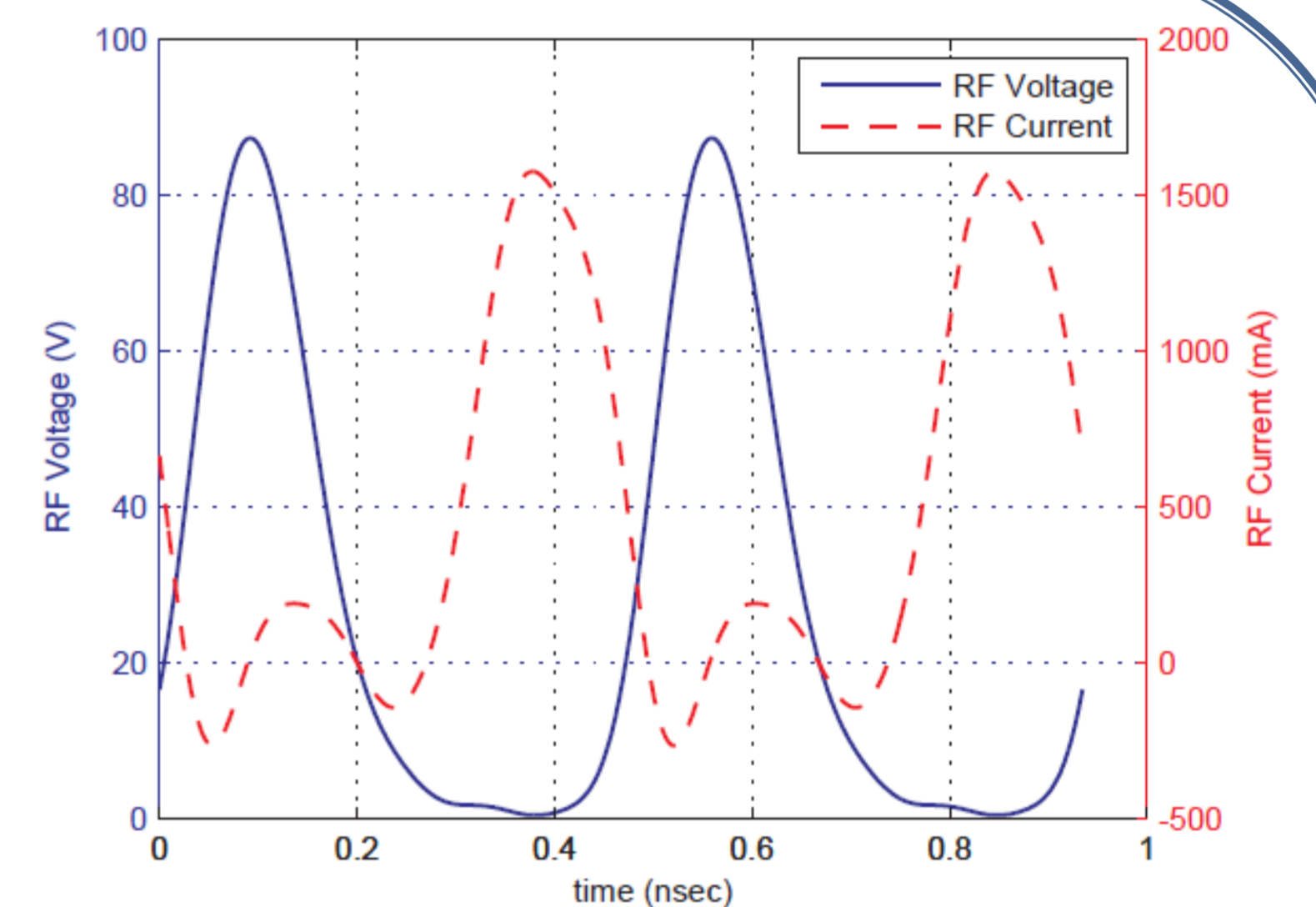
- Large signal transistor model
- Extrinsic parasitics and package model
- Intrinsic drain impedances given from theory
- **No active harmonic load-pull**
- **No RF waveform probing**

1. Deep Class - AB biasing
2. Determine appropriate load-line
3. Intrinsic drain impedances based on theory
4. **3rd output harmonic impedance**
5. **Source-pull for efficiency/gain**
6. **Observe intrinsic drain waveforms**
7. **Design matching networks**

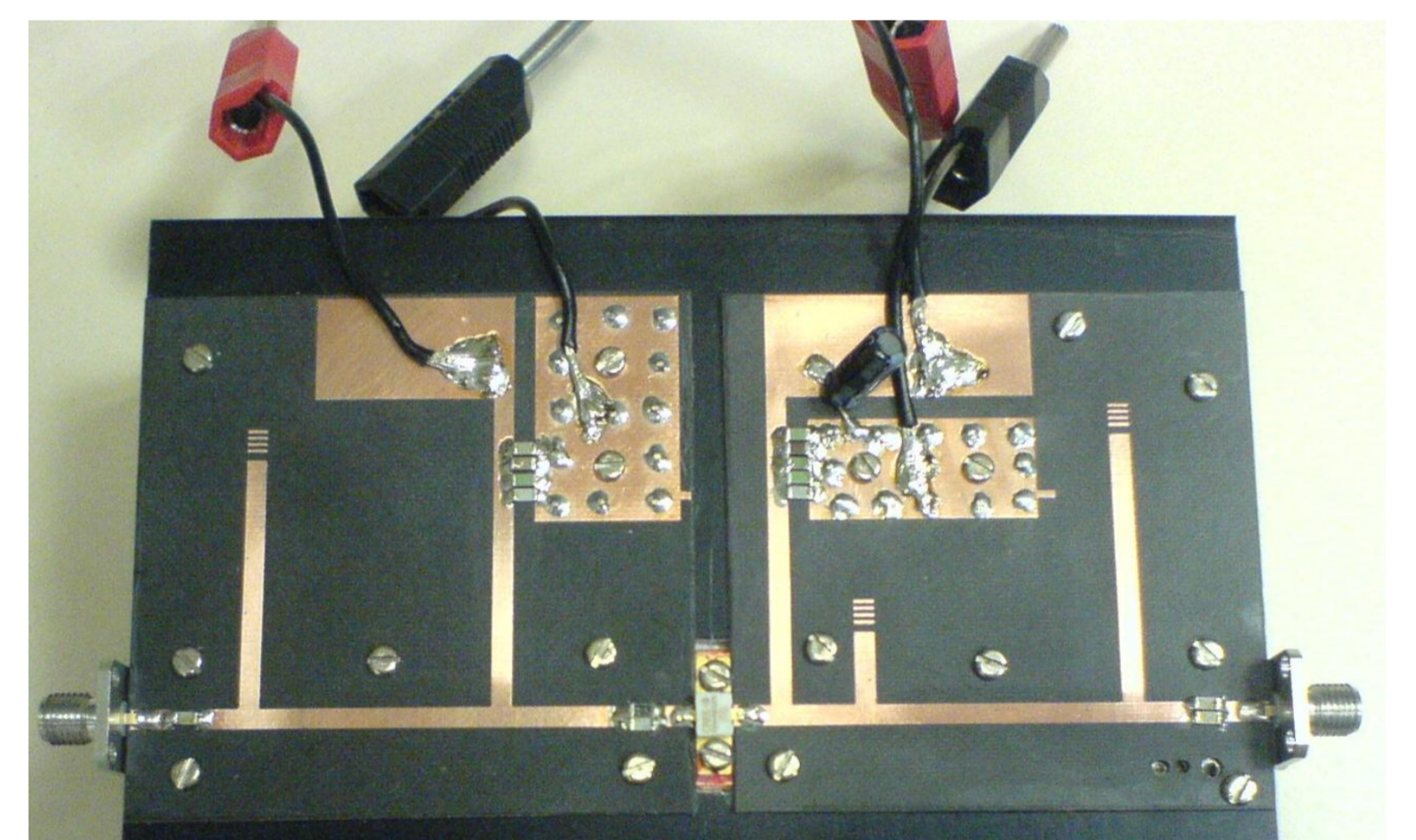
- 3rd harmonic not defined by theory
- 3rd harmonic reflection coefficient angle swept
- Affects efficiency / output power
- Chose an insensitive/efficient case



- Intrinsic drain waveforms
- De-embedded in simulations to prove Class of operation
- No “zero” voltage crossing
- Similar to expected waveforms
- Some 3rd harmonic present
- Current “hump”

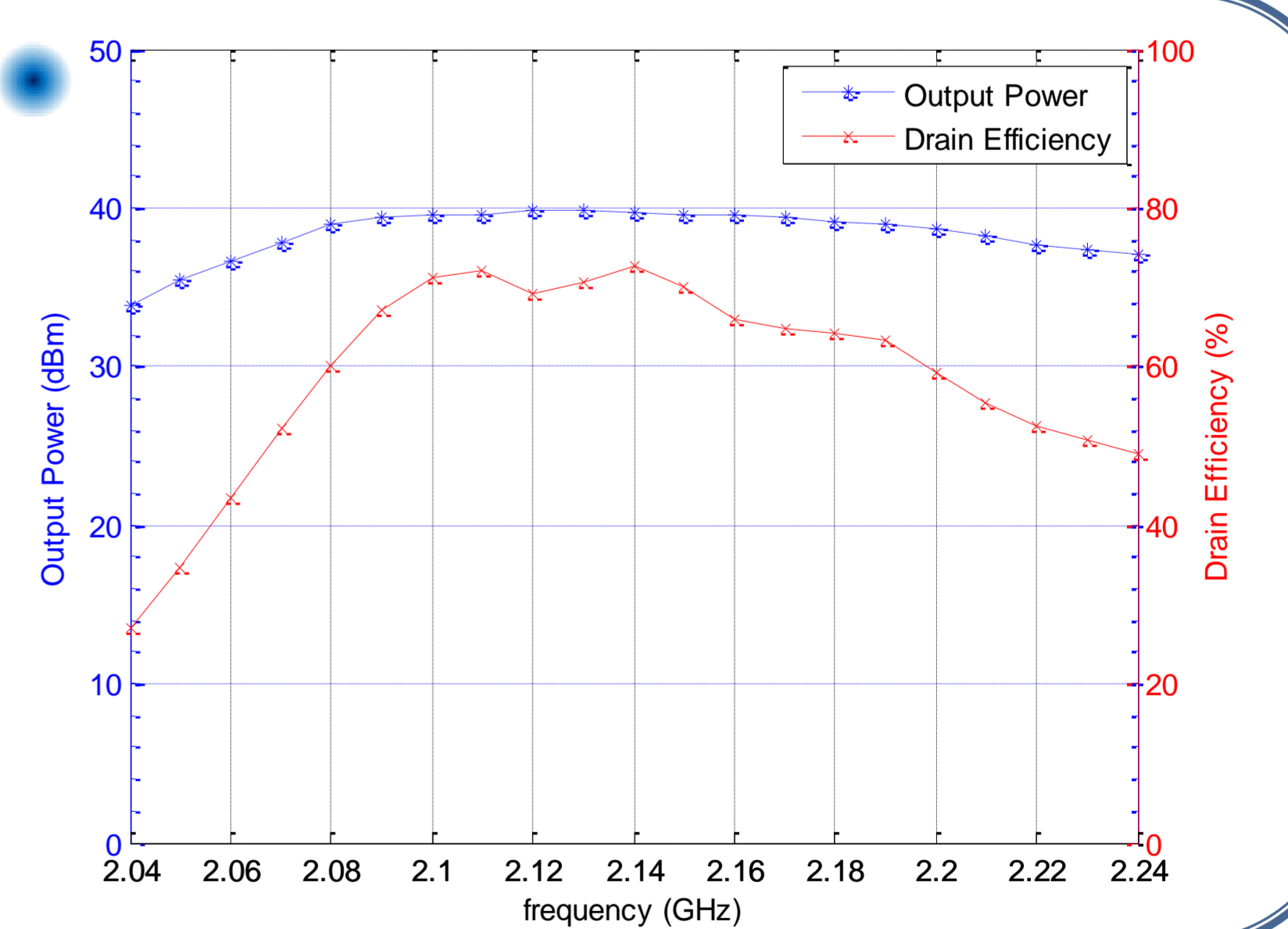
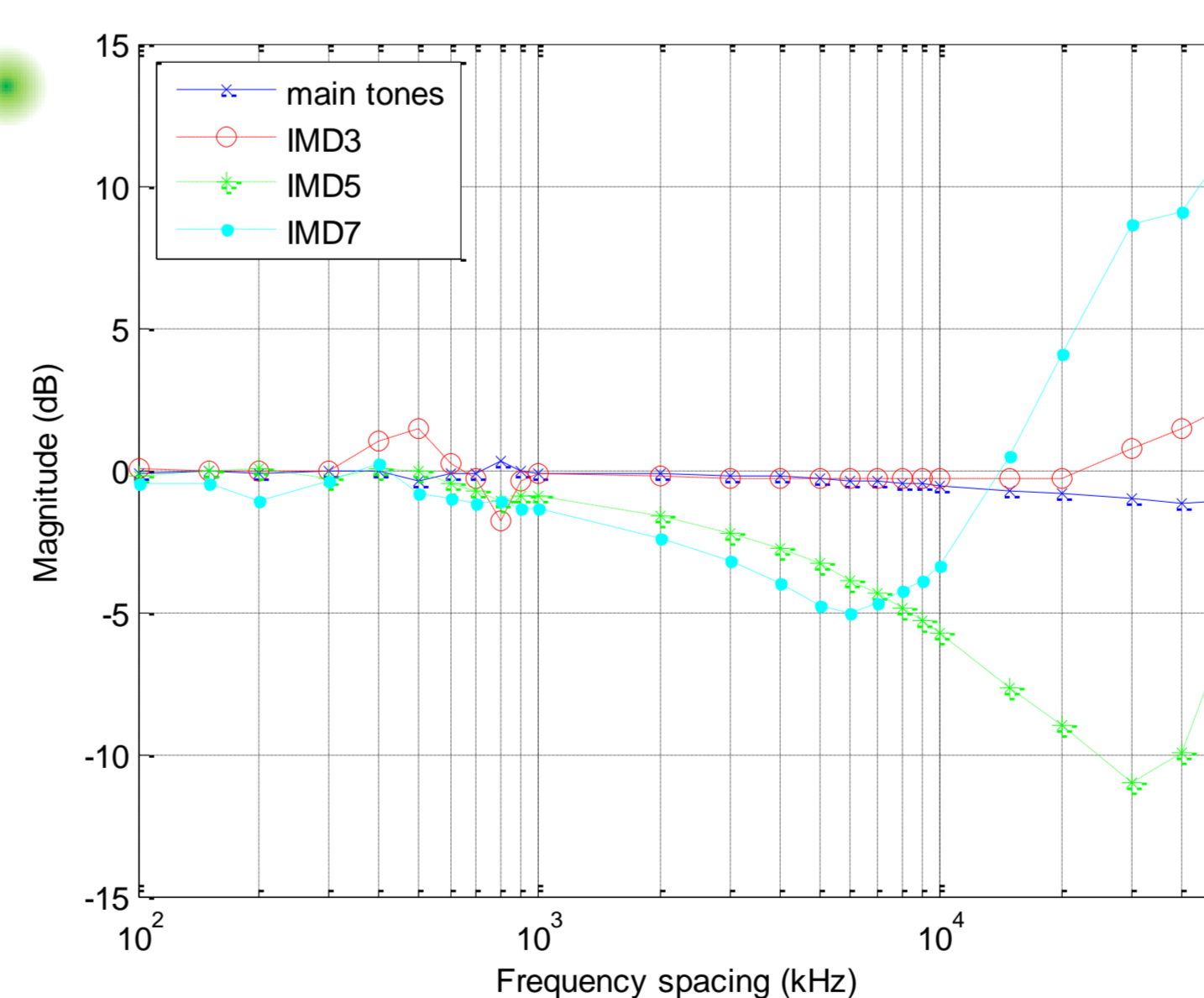
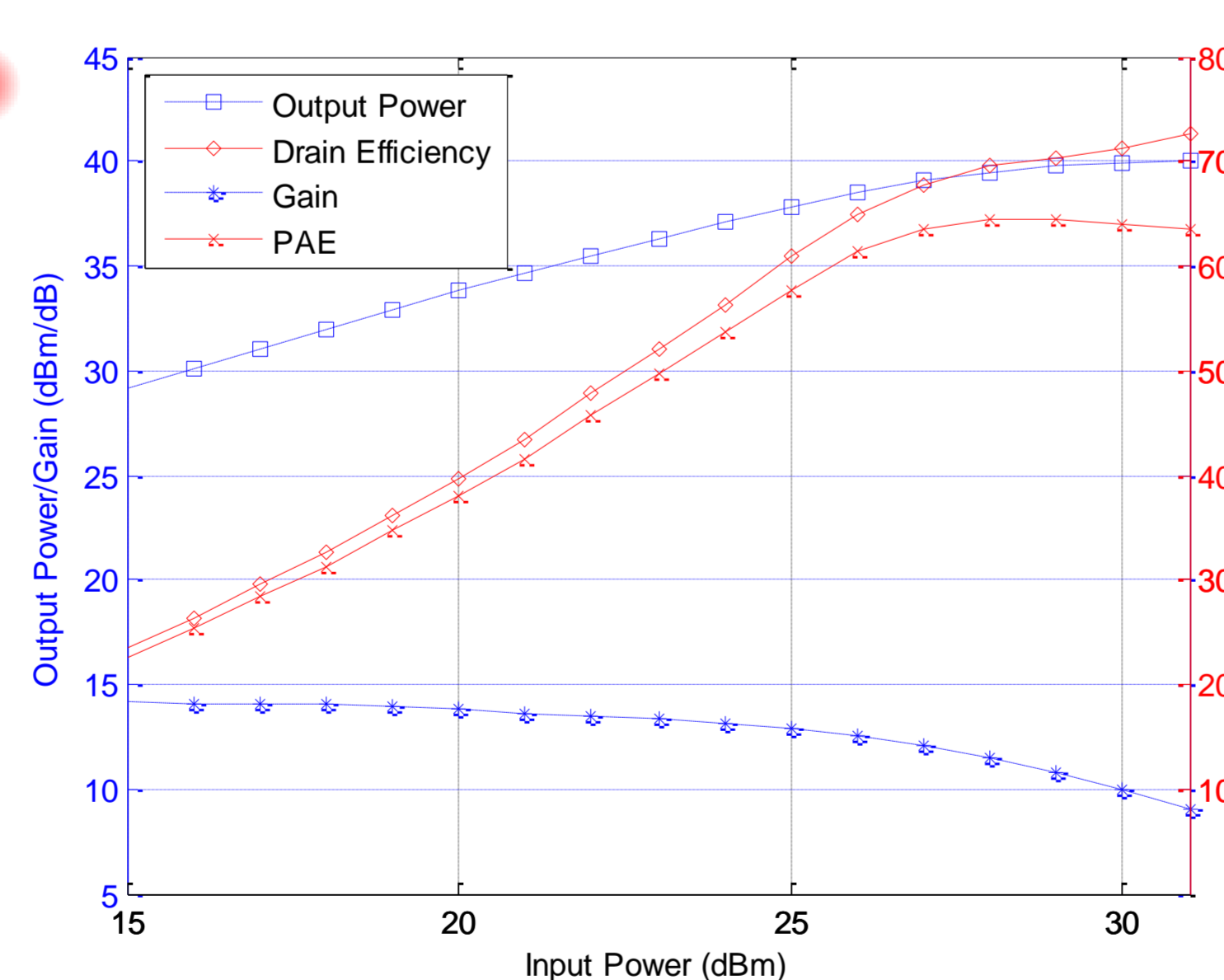


- Distributed matching networks
- 2 harmonics controlled at the input, 3 at the output
- RT/Duroid 8550 substrate
- $E_r = 2.2$, $T = 787\text{mm}$
- Size : 13.5 x 6.5 cm
- Higher E_r will reduce size



4. PERFORMANCE

- 65% maximum PAE
- 40dBm output power
- Good back-off performance
- Low asymmetry up to 20MHz
- Low memory effects
- Facilitates linearization
- 60%+ efficiency over 140MHz
- 39-40dBm output power over band
- LTE and LTE-Advanced



5. CONCLUSIONS

- **More freedom in PA design / No need for specific impedances**
- **Theory and extrinsic parasitic model is sufficient**
- **3rd output harmonic impedance is important**
- **65% PAE, over 70% drain efficiency, 40dBm output power**
- **Low memory effects**
- **Promising under ET/EER implementations**