



Tariq, M. F., Baltaci, T., Horseman, T. R., Butler, M. R. G., & Nix, A. R. (2002). Development of an OFDM based high speed wireless LAN platform using the TI C6x DSP. In IEEE International Conference on Communications, 2002 (ICC 2002), New York. (Vol. 1, pp. 522 - 526). Institute of Electrical and Electronics Engineers (IEEE). 10.1109/ICC.2002.996908

Link to published version (if available):
[10.1109/ICC.2002.996908](https://doi.org/10.1109/ICC.2002.996908)

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Development of an OFDM based High Speed Wireless LAN Platform using the TI C6x DSP

M. Fahim Tariq[†], Yusuf Baltaci[†], Tony Horseman, Mike Butler, Andrew Nix

Centre for Communications Research, University of Bristol,
Merchant Venturers Building, Woodland Road,
Bristol BS8 1UB, United Kingdom

Abstract-Coded Orthogonal Frequency Division Multiplexing (COFDM) is currently specified in all three of the world's 5 GHz wireless LAN standards (Hiperlan/2, IEEE 802.11a and MMAC HiSWANa). This technology was chosen due to its robustness at high data rates in a frequency selective multipath channel. Each standard operates using adaptive sub-band Quadrature Amplitude Modulation (QAM) and offers a maximum data rate of 54 Mbits/s over a 20 MHz channel. This paper describes a real-time DSP implementation of an asynchronous OFDM based high speed WLAN system. The software reconfigurable OFDM based platform is developed around the Texas Instruments fixed point TMS320C6201 DSP. The physical layer DSP performance is evaluated and compared for an indoor channel against floating point C++ based simulations. Data throughput and complexity estimates are generated from the resulting hardware platform. Finally, a video based communications application is developed to operate over the demonstrator. Results indicate that the fixed point DSP solution can operate within 0.5 dB of the floating point simulation in an AWGN channel. For the indoor fading channel, an implementation loss of around 2.5 dB was observed.

I. INTRODUCTION

At present there is considerable world-wide interest in the development of short-range high-speed wireless modems based around the use of Coded Orthogonal Frequency Division Multiplexing (COFDM). The majority of this interest is focused towards the 5 GHz frequency band, with systems conforming to either the ETSI Hiperlan/2 [1], IEEE 802.11a [2] or MMAC HISWANa [3] standard. Together, these three standards provide near worldwide wireless LAN (WLAN) coverage. Collaboration between ETSI and IEEE has ensured a high degree of commonality between the Physical Layer (PHY) specifications of their respective systems. Similar collaboration with the Japanese standards body is expected to ensure physical layer compatibility within the MMAC standard.

Each of the above standards is based around a 48 data carrier COFDM PHY layer. A range of channel adaptive modulation and coding modes are supported, based on the state of the radio channel and the required quality of service.

This paper describes a real-time DSP implementation of an asynchronous OFDM QPSK-based physical layer platform using the Texas Instruments fixed-point TMS320C6201 DSP [4]. The performance of the system is evaluated in AWGN and ETSI BRAN channel 'A' conditions with an RMS delay spread of 50ns. Performance results are obtained using baseband transmission over cables in I & Q format. The

results are compared with floating-point software simulations to calculate the fixed point DSP implementation loss. Finally, real-time compressed and uncompressed video applications are developed to run over the experimental platform.

II. KEY SYSTEM PARAMETERS

A flexible DSP based platform can reduce the development cost of modems that conform to all three of the current 5 GHz wireless LAN standards. More importantly, the DSP system can be used to test experimental components and algorithms. In particular, RF designs and power amplifier solutions may be rigorously tested via repeated packet transmission and analysis. In addition, once RF transmission has been achieved, the system can be used to explore data transmission and support the development of more advanced services such as the transport of error resilient or transcoded video streams.

Recent improvements in DSP power consumption and processing speed have increased the viability of DSP based solutions, particularly when assisted by strategic acceleration. Given the degree of physical layer commonality between the three 5GHz WLAN standards, a flexible multi-format software-based DSP and FPGA solution is a future possibility.

The key system parameters for our baseband prototype modem are listed in Table 1.

Parameters	Value
RF Channel bandwidth	20 MHz
Modulation scheme	OFDM QPSK
Data payload rate	24 Mbits/s
Number of data subcarriers	48
Number of pilot subcarriers	4
Subcarrier frequency spacing	0.3125 MHz
Sampling rate	20 MSPS
IFFT/FFT points	64
IFFT/FFT period	3.2 μ s
Guard interval	0.8 μ s
OFDM symbol interval	4 μ s
Preamble duration	8 μ s
OFDM symbols per packet	23
Coding scheme	None

Table 1: Summary of the major system parameters

[†] Now with ProVision Communication Technologies Limited, University Gate, Park Row, Bristol BS8 5UB, United Kingdom

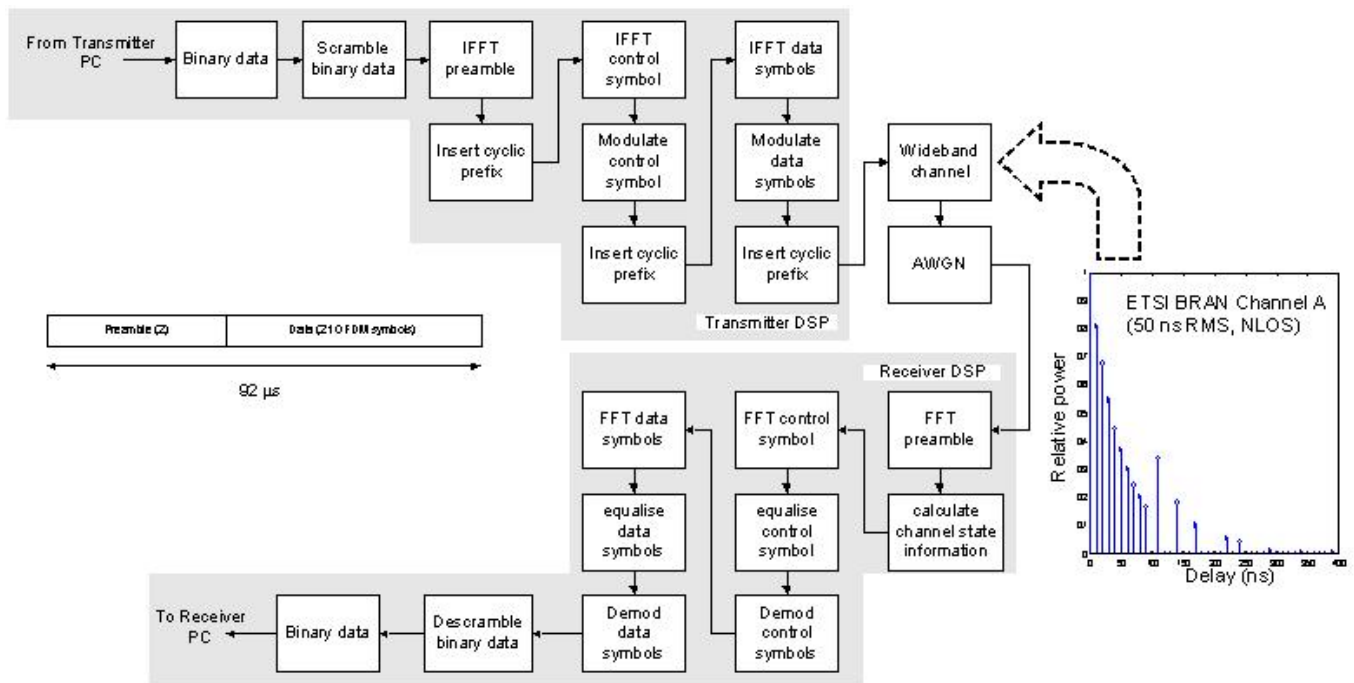


Fig. 1: Block diagram of the system

III. SYSTEM DESCRIPTION

Fig. 1 shows the basic functions used to develop the hardware prototype and the software simulation. The incoming binary bits are partitioned into blocks to produce a packet comprising 23 OFDM symbols. The binary block (corresponding to bits from OFDM symbols 3 to 23) is scrambled to whiten the data sequence. The first two OFDM symbols are used to transmit a preamble. This is used in the receiver for timing recovery, frequency offset correction and Channel State Information (CSI) estimation. The preamble is similar to that used in all three 5GHz WLAN standards. The remaining 21 OFDM symbols are used to carry the payload data.

An OFDM symbol consists of a useful part and a cyclic prefix. Here, the useful part is generated from 48 data symbols, 12 frequency nulls and 4 pilot carriers. A 64 point IFFT converts the frequency domain symbol into a sequence of complex time domain samples. The last 16 of these samples are added to the start of the symbol to form a cyclic prefix. The resulting 80 sample structure is referred to as an extended symbol. A comprehensive description of OFDM symbol generation can be found in the standards [1,2].

To evaluate system performance, a simulated frequency selective baseband channel is included in the DSP. As part of the standardisation process, ETSI BRAN specified a set of five channel models that were intended to represent a wide range of environments in which the HIPERLAN/2 system was intended to operate. These channels were designated the letters A, B, C, D and E [5]. The performance of the system reported in this paper has been evaluated under ETSI BRAN

channel 'A'. This channel represents an office environment with Non Line of Sight (NLOS) propagation and an RMS delay spread of 50ns. The average power delay profile of channel 'A' is given in Fig. 1.

Channel 'A' is modelled by applying Rayleigh fading statistics to each of the channel taps shown in Fig. 1. After convolving the OFDM packet with the channel impulse response, AWGN is added to the system.

At the receiver, the preamble is separated from the received OFDM packet. An average Channel State Information (CSI) vector is then calculated for each of the 64 carriers by performing an FFT on both preamble symbols. The CSI vector is used to compensate channel distortion on the data OFDM symbols, thus effectively achieving coherent detection. The demodulated bits are descrambled to recover the original binary data stream.

IV. PROTOTYPE DEVELOPMENT

A block diagram of the hardware prototype is given in Fig. 2. It consists of four main parts:

1. Transmitter Personal Computer (TxPC).
2. Transmitter DSP (TxDSP).
3. Receiver DSP (RxDSP).
4. Receiver Personal Computer (RxPC).

The TxPC hosts the TxDSP while the RxPC hosts the RxDSP. The PCs perform a wide range of functions and these include:

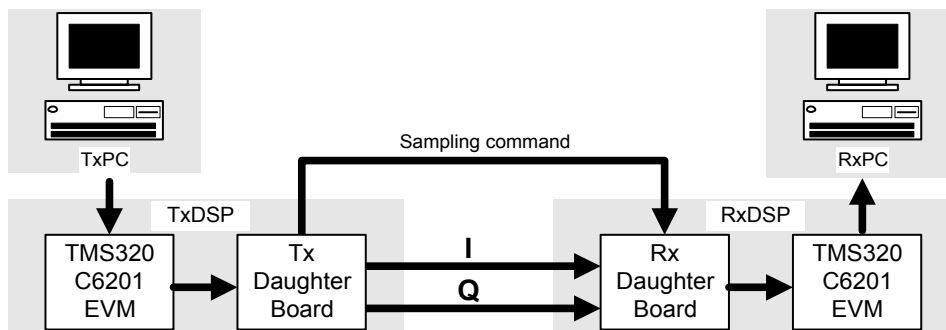


Fig. 2: Hardware prototype

1. Access DSP memory via the PCI bus.
2. Control DSP operation.
3. Provide binary data to TxDSP and read received binary data from RxDSP.
4. Provide the Graphical User Interface (GUI) to transmit video and display diagnostic waveforms.
5. Host design software (functions include video compression and decompression).

The TxDSP and RxDSP each consist of two parts:

1. Texas Instruments TMS320C6201 EVM (called EVM hereafter).
2. Custom transceiver daughterboard shown in Fig. 3.

The EVMs are used in PCI expansion slots inside the TxPC and RxPC. The EVMs perform the following functions:

1. Exchange data with the PC.
2. Packetise, modulate and IFFT data, add preamble and channel (TxDSP), calculate CSI, equalise and demodulate data (RxDSP).
3. Send data to transmit (Tx) daughterboard buffers, retrieve data from receive (Rx) daughterboard buffers.

The transmit and receive daughterboards are connected by cables to send complex (I and Q) data in a simplex form. A special synchronisation signal is sent to initiate the sampling and storage process in the receiver. The daughterboards were designed and manufactured at the University of Bristol and integrate both transmit and receive functions onto a single PCB. This enables future extension to half-duplex operation.

The nucleus of the daughterboard is a 4096 word FIFO memory. To support transmit and receive functions, the FIFO takes input data from either the DSP (via the EMIF) or a dual 20MSPS 10bit ADC. The data outputs of the FIFO are directed to the DSP in receive mode, or to a dual DAC when transmitting. The DAC includes a two times interpolating filter that generates a 40MSPS output from a 20MSPS input. This feature greatly simplifies the design of the terminal. Both the data converters (from Analog Devices) have interleaved data buses for I and Q samples. This results in a board with narrow buses (for small size) and a sample rate low enough to make the board realisable.

The EVM to transceiver interface was able to support, in bursts, the 40MSPS data transfer rate required, so with

careful use the transceiver can reliably sample many more than the 4096 words the FIFO can hold. As mentioned previously, the transmit and receive functions were synchronised by use of a special cable. Using this configuration it is possible to generate received data that is time aligned to within a few samples. Assuming a 16 sample timing uncertainty window, the DSP uses each packet's preamble to accurately time align the data.

The necessary analogue circuitry was also included on the PCB, comprising of reconstruction and anti-alias low pass filters with 1dB bandwidths of 11 and 8MHz respectively. Additionally, wideband op-amps were required to perform a differential to single ended conversion, and power supplies to isolate the analogue and digital circuitry as much as possible. The board outputs are capable of driving 50Ω loads at 1V peak to peak, while the inputs have a similar range. The results obtained during this work were gained by connecting the terminals with coax cables at baseband. However, these cables can be replaced by any radio with I and Q inputs/outputs that support the required bandwidth.

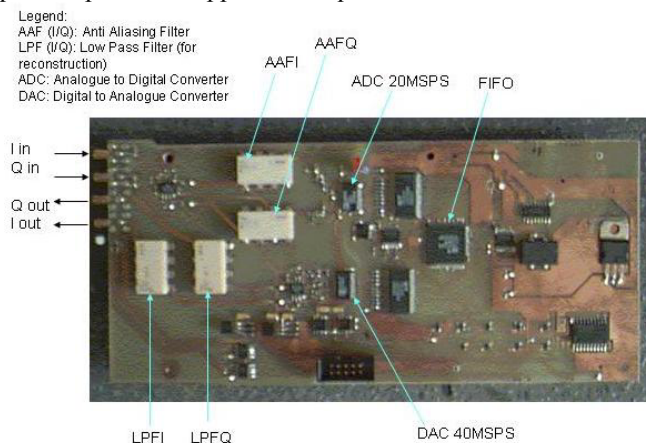


Fig. 3: Daughterboard photograph

To make the operating conditions significantly more realistic, a radio channel was modelled in the transmitter software. It was later realised that this impacted seriously on the transmitted SNR as the analogue output had deep spectral nulls. With nulls approaching -40dB, the SNR at the receiver was unreasonably low, and would certainly not allow use of the higher level modulation schemes employed in

HIPERLAN/2 and IEEE802.11a. This situation could be eased significantly by using either a real radio channel, which would generate spectral nulls without impacting as significantly on SNR except when the received power is very low, or a hardware simulated radio channel to allow more controlled measurements to be made.

V. SOFTWARE SIMULATION

Along with the hardware development, a floating-point software simulation was written in Visual C++ to provide a benchmark for calculating the implementation loss of the hardware simulator. All the basic functions highlighted in section III have been implemented in the software simulation.

VI. VIDEO TRANSMISSION

The hardware system was now extended to support real time video transmission using either uncompressed (at 1.7 Mb/s) or compressed (H263+ at 100 kb/s) video streams. A snapshot of the demonstrator running with a H.263+ video stream is shown in Fig 4.

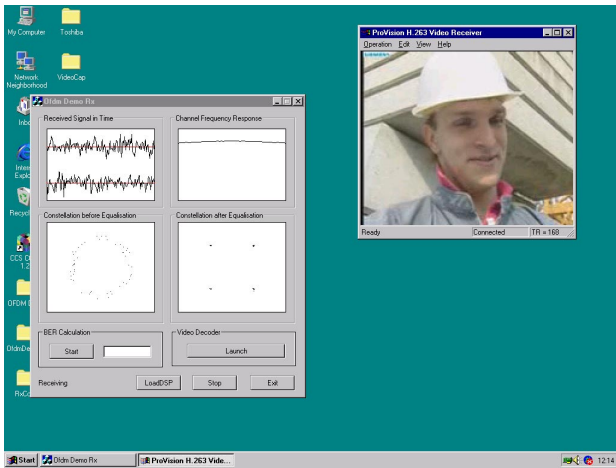


Fig. 4: Screenshot of the System with H263 Video Decoder

For uncompressed video, a video frame (see Fig. 5) was developed that comprises 160 OFDM packets. The transmission of video packets requires a packet number to be sent along with the payload. A third OFDM symbol was reserved within the OFDM packet described in Fig. 1 to transmit this information. The resulting OFDM packets had a data payload of 20 OFDM symbols.



Fig. 5: Uncompressed video frame

VII. SUSTAINED DATA RATE, DUTY CYCLE AND MIPS

The hardware prototype transmits 24 Mbit/s bursts of data. However, the duty cycle is much less than 100% due to delays at various stages in the system. The calculations of sustained data rate, time per OFDM packet and duty cycle are given below:

Bits per OFDM packet = $20 \times 48 \times 2 = 1920$
 Packets per video frame = 160
 Bits per video frame = 307200

Time per video frame:

DMA initialisation interval = $15 \mu s$
 Sampling interval = $135 \mu s$
 Mod/Demod interval = $500 \mu s \times 160$
 Data transfer interval = 10 ms
 Samples store interval = $10 \mu s$
 Total Video Frame Time = 181.6 ms

Time per OFDM packet = $181.6ms / 160 = 1.13 \text{ ms}$

Sustained data rate = $307200 \text{ bits} / 181.6 \text{ ms} = 1.7 \text{ Mbit/s}$
 Duty cycle = $1.7 / 24 = 7 \%$

A summary of the cycle counts required to implement the various sections of the transceiver is shown in Table 2. Standard compliant frame, frequency and timing synchronisation were not implemented in the demonstrator. Assuming on average that the C6xxx DSP executes 3 instructions per cycle, the required MIPS to achieve 100% duty cycle is 1626.

Process	Cycle Count
IFFT, FFT	1036
Equaliser Coefficients	5800
Equalise	256
Modulation, Demodulation	727
Scramble, De-Scramble	128
Guard Interval Insertion	22
Frame Synchronisation	N/A
Frequency Synchronisation	N/A
Frequency Correction	128
Time Synchronisation	N/A

Table 2: Achieved Cycle Counts for TI C6201 DSP

VIII. RESULTS AND DISCUSSION

The performance of the system has been evaluated in AWGN and ETSI BRAN channel 'A' with 50ns of RMS delay spread.

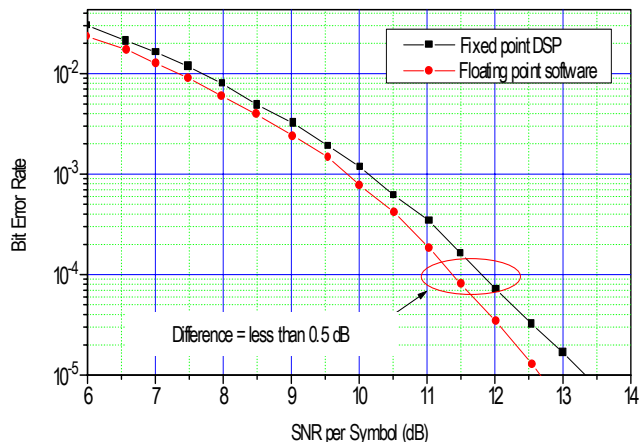


Fig. 6: Performance in AWGN channel

Fig. 6 compares results obtained from the hardware prototype with those from the floating point software simulation for uncoded QPSK modulation over an AWGN channel. Although the simulation software performs slightly better than the DSP implementation, the results are very similar. The poorer hardware performance is a result of the limited (16-bit) DSP word length compared to the floating-point capability of the software. In addition, for higher values of Signal to Noise Ratio (SNR), insufficient errors are detected to give accurate results. At a Bit Error Rate (BER) of 10^{-4} , the implementation loss is found to be less than 0.5 dB.

Fig. 7 compares the hardware and software results over ETSI channel 'A'. As can be seen, an error floor begins to form in the hardware results at around 30 dB. This is the result of the noise introduced to the signal by the daughterboard data converters. Measurements have shown that the two least significant received bits (of the ten bit samples) are noise, giving an rms noise voltage of 1.4. The system configuration gives an average signal amplitude of approximately 128 (the remainder of the data converter range is required to handle to peak excursions of the OFDM signal). From this, the maximum achievable SNR can be computed as follows:

$$SNR_{max} = 10 \log_{10}(128^2/1.4^2) = 39.1 \text{ dB}$$

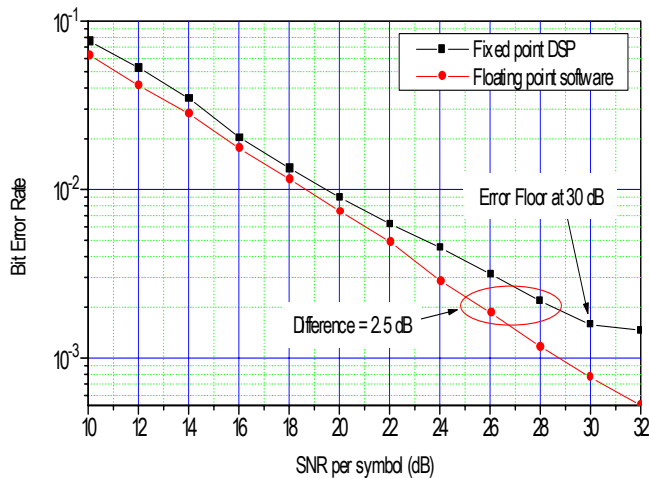


Fig. 7: Performance in ETSI BRAN channel 'A'.

Thus the higher SNRs in Fig. 8 approach the limits of the hardware, resulting in the beginnings of an error floor. It can be seen that the difference between the hardware and software results is around 2.5 dB for a BER of 2 in 1000. The hardware degradation is a result of the erroneous calculation of the CSI vector within a limited dynamic range. The degradation in BER and the appearance of an error floor can be limited by increasing the number of bits in the data converters or by the application of FEC (as specified in the standards). It should be noted that the error floor will be more severe for higher level modulation schemes, such as 16 and 64 QAM.

VIII. CONCLUSIONS

A real-time baseband implementation of an OFDM QPSK based WLAN system has been developed using the Texas Instruments fixed point TMS320C6201 DSP. A custom daughterboard was designed to accommodate buffer memory and high speed data converters. Uncompressed (at 1.7 Mb/s) and compressed (H263+ at 100 kb/s) video streams were successfully sent over the resulting system.

An instantaneous data rate of 24 Mb/s was achieved during burst transmission. However, at the application layer a sustained uncoded user data rate of 1.7 Mb/s was achieved. To achieve full data throughput some form of strategic hardware acceleration is required to support the DSP. Using a software only implementation, a duty cycle of 7% was achieved for the uncoded data. To achieve 100% throughput using this DSP, it was estimated that 1626 MIPS would be required. In practice, significant processing would be required to implement additional synchronisation and data encoding/decoding functions.

In AWGN, the system performed to within 0.5 dB of the floating point simulation results. In ETSI channel 'A' (50ns RMS delay spread), an error floor appeared at 30 dB SNR per symbol due to the dynamic range limitations of the hardware. The error floor can be reduced by i) increasing the number of bits in the data converters, ii) applying FEC coding or iii) improving the implementation of the channel model to increase the transmit SNR. However, even given these limitations, for a BER of 2 in 1000 the DSP platform performed to within 2.5 dB of the floating point simulation over ETSI BRAN channel 'A'.

ACKNOWLEDGEMENTS

The authors would like to thank Rob Heaton and Paul Ratliff from Mitsubishi Electric ITE-VIL United Kingdom for their valuable input and support of this work.

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