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Analog MIMO Detector: The Concept and Initial Results

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Abstract— In this contribution we propose an analogue receiver that can perform turbo detection in MIMO systems. The receiver is built from discrete non-linear analogue devices that perform detection in a "free-flow" network (no notion of iterations). This contribution can be viewed as an extension of analogue turbo decoder concepts to include MIMO detection. These first analogue implementations report reductions of few orders of magnitude in the number of required transistors, consumed energy and the same order of improvement in processing speed. Our implementation of MIMO decoder brings about the same advantages, when compared to traditional (DSP/FPGA) implementations.

I. INTRODUCTION

Turbo codes and more general turbo principles (turbo equalisation, turbo multi-user detection etc) are bound to have a substantial impact on the next generation wireless systems. The turbo principle requires exchange of so-called soft information, which is a probabilistic measure. In current implementations (e.g. turbo coding) this information is sampled then quantised (digitised) and handled by digital signal processors. The amount of digital information to be processed by DSPs and FPGAs is enormous and represent a "bottleneck" for high speed digital systems. However, the soft information, as analogue in nature is best represented in analogue domain (e.g. electric currents or voltages). More interestingly, it can be processed in this form by analogue networks as well. The analogue decoding paradigm formulated in [1][2] takes this stand.

First analogue implementations of binary decoders were reported in the literature in [3] [4] [5]. Those implementations reported reductions of 1-3 orders of magnitude in number of required transistors, consumed energy and the same order of improvement in processing speed. More ambitious CMOS only implementation of analogue decoders were recently reported in [6][7].

In truth, it was the neural networks community that first used analogue VLSI circuits to build simple artificial neural networks [8]. Both neural networks and communications engineering are by and large examples of computation, and as a result the fundamental building blocks are the same in both cases. Some fundamentals of analogue computations stem directly from the universal Turing machine paradigm worked out by Alan Turing nearly 70 years ago. Subsequently, they

were used in many versions of analogue and mixed mode (micro)processors built over the last few decades.

In this contribution we extend the concept of analogue detection and we attempt to layout MIMO (Multiple input - Multiple output) analogue decoder. As aforementioned, the state-of-the-art implementations of analogue computation networks realize binary codes. Equalisation in analogue networks was envisaged in [9]. All are examples of probability propagation principle that can be achieved using simple sum-product algorithm. In this contribution we will also be exchanging probabilities, which can be viewed as a form of sum-product algorithm.

The proposed analogue MIMO decoder calculates sets of marginal posterior probabilities (MPP). The major idea may be conveyed in figure 1. The mesh represents support for the joint posterior distribution. The thick dots on the lines along the axis represent the MPPs of interest. The only way to calculate the exact MPPs in MIMO system is to enumerate over the joint posterior probability, and then marginalise out. Marginalisation over discrete sets amounts to repeated summations. By Kirchhoff's current law, analogue summation can easily be achieved, and the speed improvement is due to fully parallel manner in which calculations of the joint posterior probability and marginalisation occurs.

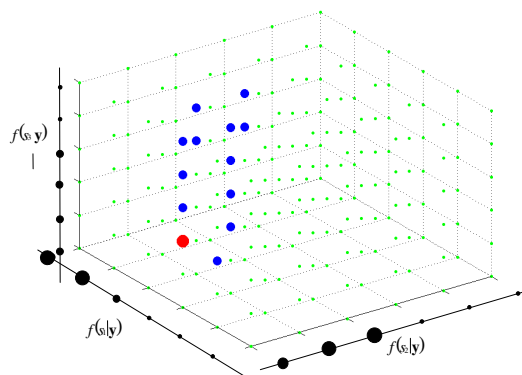


Fig. 1. Joint posterior and marginal posterior probabilities in a MIMO system.

II. SYSTEM DESCRIPTION AND DETECTION AIMS

The object of our study is a MIMO system. The system communicates N bits $b_n : b_n \in \{0, 1\}$. The stream of bits

is first encoded to $K > N$ coded bits: $c_k : c_k \in \{0, 1\}$, interleaved (a random permutation) $\pi: c_{\pi(k)} = \pi(c_k)$. We assume that modulation and encoding onto N_T transmit antennas takes place in one operation: space-time modulation encoding, where $D = N_T \log_2(M)$ portion of coded bits $c_{\pi(k)}$. This is arguably the simplest form of space-time signalling, known as: V-BLAST, Spatial-Multiplexing, Bit interleaved coded modulation etc. The resulting $N_T \times 1$ dimensional vector $\mathbf{x} = (x_1, \dots, x_{N_T})^T$ is transmitted from all N_T antennas at a time instant t . We will assume that the signal is transmitted over a narrowband channel \mathbf{H} of size $N_R \times N_T$; where each entry $h_{i,j}$ defines a channel connecting j^{th} transmit with i^{th} receive antenna. The system is conventionally modelled as:

$$\mathbf{y} = \mathbf{H}\mathbf{x} + \mathbf{n} \quad (1)$$

where \mathbf{y} - is the receive $N_R \times 1$ vector and \mathbf{n} - is the ubiquitous white Gaussian noise i.e. $\mathbf{n} \sim \mathcal{CN}(\mathbf{0}, \sigma_n^2 \mathbf{I})$. Typically, it is assumed that $h_{i,j}$ are i.i.d. random variables $h_{i,j} \sim \mathcal{CN}(\mathbf{0}, 1)$, however this is not required here, other than $h_{i,j}$ to be known to the receiver. The ultimate goal is to detect the transmitted information bits given the received signal and the channel. To be more specific we are looking for a set of point estimates that maximise the set of marginal posterior distributions: $\{f(b_1 | \mathbf{y}_{1:T}, \mathbf{H}), \dots, f(b_N | \mathbf{y}_{1:T}, \mathbf{H})\}$ - (i.e. MAP - maximum a posteriori estimates). In general, this task is computationally not tractable, and instead it is conventional to use a sub-optimal procedure: so-called turbo-detection. The resulting system with such detector is known as: Turbo-Blast, Turbo Spatial multiplexing, Turbo-BICM etc. Essentially, the turbo detection is an iterative process where, so-called soft MIMO detector computes for each time instant t $\{f(x_1 | \mathbf{y}_t, \mathbf{H}), \dots, f(x_{N_T} | \mathbf{y}_t, \mathbf{H})\}$, and the soft binary channel decoder computes $\{f(b_1 | c_{1:K}), \dots, f(b_N | c_{1:K})\}$.

It is the main aim of this contribution to discuss how those tasks can be carried out in the analogue circuits. Since the detection of binary codes using analogue VLSI has been extensively described in an excellent monograph [3], we will concentrate on the MIMO detection block. The MPPs of interest are calculated as follows:

$$f(x_i | \mathbf{y}) = \sum_{-i} f(x_{1:N_T} | \mathbf{y}) \propto \sum_{-i} f(\mathbf{y} | x_{1:N_T}) f(x_{1:N_T}) \quad (2)$$

Where $-i$ stands for "all except i ". The observations are independent given the symbols and it is reasonable to assume that the extrinsic information (which becomes the prior for the decoder) is also separable i.e.

$$f(x_i | \mathbf{y}) \propto \sum_{-i} \prod_{i=1}^{N_R} f(y_i | x_{1:N_T}) \prod_{j=1}^{N_T} f(x_j) \quad (3)$$

In general any further simplifications (i.e. factorisations) are not possible. If one wants to calculate any marginal, the only way is to calculate the joint posterior distribution and marginalise out the variables as prescribes by (3) (i.e. no message passing tricks would help). Given our assumption about the noise, the likelihood is Gaussian

$$f(y_i | x_{1:N_T}) \propto \exp\left(-\frac{1}{\sigma_n^2} |y_i - \mathbf{h}_{i,:}^T \mathbf{x}|^2\right) \quad (4)$$

All operations in (4) can be carried out explicitly in the analogue domain. In this paper we opt for an alternative approach that also computes the exact values of the marginals of interests. Arguably this will lead to a simpler implementation of at least the analogue part of the MIMO decoder. First we assume that the digital part of the receiver calculates the QR decomposition of the channel matrix i.e. $\mathbf{H} = \mathbf{Q}\mathbf{R}$, where \mathbf{R} is upper triangular and $\mathbf{Q}^H \mathbf{Q} = \mathbf{I}$. Left multiplication of the received signal by \mathbf{Q} produces a signal model:

$$\tilde{\mathbf{y}} = \mathbf{R}\mathbf{x} + \tilde{\mathbf{n}} \quad (5)$$

(note that the noise statistics do not change). However the analogue layout of the decoder is different since our model is now causal (\mathbf{R} is triangular). (The QR decomposition has been used in the past with various MIMO detectors). The decomposition now looks as:

$$f(x_i | \mathbf{y}) \propto \sum_{-i} \prod_{i=1}^{N_R} f(y_i | x_{1:i}) \prod_{j=1}^{N_T} f(x_j) \quad (6)$$

E.g. in the case of a 3×3 MIMO system the likelihood factors as:

$$f(y_1, y_2, y_3 | x_1, x_2, x_3) = f(y_3 | x_3) f(y_2 | x_2, x_3) f(y_1 | x_1, x_2, x_3) \quad (7)$$

Notice that when implemented in digital domain there is no real difference between the two approaches as both boil down to enumerating entire state-space of the joint distribution and marginalisation in the second step.

III. ANALOGUE IMPLEMENTATION DETAILS

As indicated in eq. (4), the fundamental operations required to be implemented are: multiplication, summation and negative exponential function i.e. $\exp(-x)$. In this section we discuss how those basic blocks can be implemented in analogue circuits.

A. Multiplier

The most important function that has to be implemented with analogue circuits is multiplication of two input voltages, both of which can be positive or negative. A four-quadrant multiplier circuit is therefore needed to achieve this. This basic block is used most often in the analogue MIMO detector. The Gilbert multiplier circuit [8] performs multiplication using the output from a differential pair as the input for another two differential pairs - figure 2. The circuit is arranged in such way that the output current is given by the combination of all four upper currents is:

$$I_{out} = (I_{13} + I_{24}) - (I_{14} + I_{23}) = I_b \tanh \frac{k(V_1 - V_2)}{2} \tanh \frac{k(V_3 - V_4)}{2}$$

The output current and voltage of the Gilbert multiplier follow a $\tanh(x)$ rule, which for small input voltage differences can be approximated by $\tanh(x) \approx x$. Additionally this basic circuit has a limitation on the inputs: $\max(V_3, V_4) > \min(V_1, V_2)$

Multiplication is typically performed on random voltages. Hence, it is difficult to make any assumptions about the range

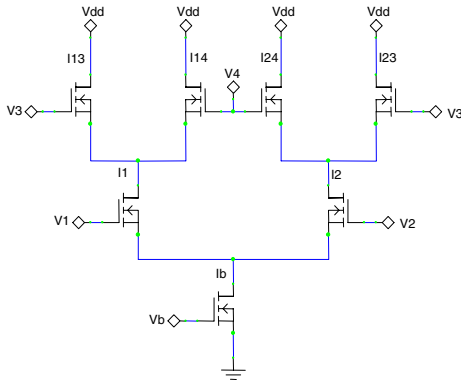


Fig. 2. Gilbert multiplier basic cell.

of the input signals. A wide-range multiplier [8] is required in order to ensure that the circuit works properly for both high and low input voltage levels. One possible choice is the wide-range Gilbert multiplier circuit, shown in figure 3. The wide

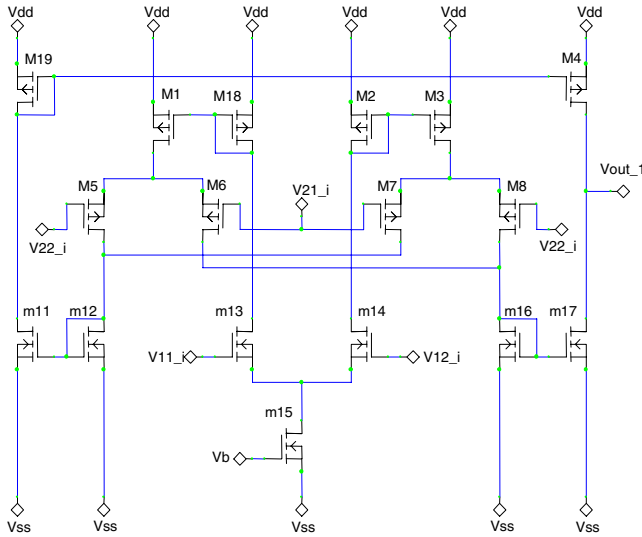


Fig. 3. Wide Range Gilbert Multiplier.

range multiplier isolates the bottom differential pair from the upper differential pairs using current mirrors. This allows the range of V_3 and V_4 to be independent of V_1 and V_2 allowing the circuit to work properly for input voltages close to the supply voltage. The SPICE simulated output of the wide-range Gilbert multiplier is shown in figure 4. The observed voltage is closely approximated by $\Delta V_{out} = \frac{V_1 V_2}{V_{ref}}$ (with $V_{ref} = 10mV$). For high input values the $\tanh(x)$ behaviour starts being noticed, degrading the output characteristic of the circuit. For moderate input values, up to 30-60 mV, the linearity is high enough to multiply the two inputs with great accuracy.

B. Summation

The summation operation is most conveniently performed in the current domain. By Kirchoff's current law, it is enough just to connect the wires in a node - figure 5. Indeed, such summers are used in the MIMO decoder in the "marginaliser" block. A voltage summation is also required to avoid excessive

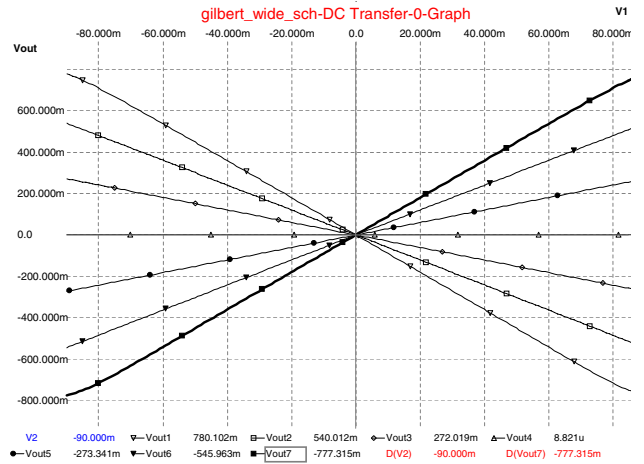


Fig. 4. Output characteristics of the Wide-range Gilbert Multiplier. The plots correspond to the second input set at $\pm 90mV$, $\pm 60mV$, $\pm 30mV$ and $0V$

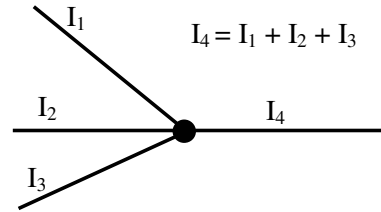


Fig. 5. Kirchoff's current law summer.

number of voltage-current-voltage transformations. A circuit [10] capable of performing voltage summation is shown in figure 6. By simple analysis of the circuit, the output voltage can be obtained as a function of the gate-source voltages of the transistors [10]:

$$\begin{aligned}
 V_{os} &= \sqrt{\frac{(W/L)_1}{(W/L)_2}} ((V_{GS1} - V_{GS2}) + (V_{GS3} - V_{GS4})) \\
 &= \sqrt{\frac{(W/L)_1}{(W/L)_2}} (V_1 + V_2)
 \end{aligned}$$

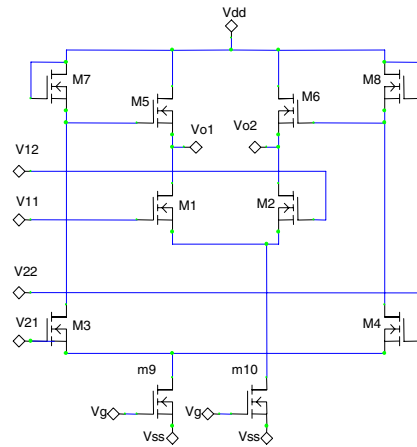


Fig. 6. Voltage differential adder circuit.

Figure 7 shows the simulated response for $(W/L)_1 = (W/L)_2$.

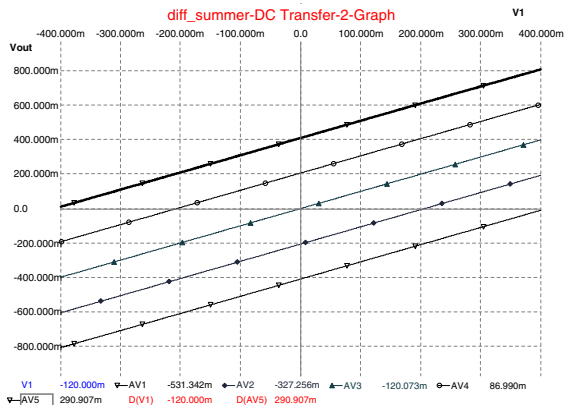


Fig. 7. Output characteristics of the differential adder circuit. The plots correspond to the second input set at $\pm 400mV$, $\pm 200mV$ and $0V$

C. Negative exponential

A function of the type $f(x) = A - \frac{\sqrt{Bx}}{C}$ can be used to approximate the negative exponential i.e. $\exp(-x)$. It is important to restrict the output voltage of the circuit to positive values. This can be achieved by a simple filtering of the output current using a current mirror and then converting again to a voltage. Alternatively, in the case of our MIMO detector, where the negative exponential is always followed by a multiplication, the problem can be overcome by using a one-quadrant multiplier that would ignore negative inputs. In MIMO analogue decoder, the negative exponential function is multiplied by a factor K :

$$\Delta V_{out} = KV_{ref} \exp\left(\frac{-V_{in}}{V_{ref}}\right) \quad (8)$$

A block diagram of the circuit and the results obtained from SPICE simulation are shown in figures 8 and 9 respectively. The ideal response shown corresponds with equation (8) with $K=1.8$ and $V_{ref}=10mV$. The negative values of the output voltage have been forced to zero using a current mirror at the output, with the proper Voltage-to-Current and Current-To-Voltage conversion of the signal. This is not shown in the block diagram, since the best solution would be the use of a one-quadrant multiplier after every exponential circuit. The one remaining operation $|x|^2$ is simply achieved by a four quadrant multiplier realizing $x \cdot x$.

IV. ANALOGUE MIMO DECODER EXAMPLE

We have simulated in SPICE software an analogue MIMO decoder with 3 transmit and 3 receive antennas. A BPSK modulation was assumed. Six bits of data are encoded to 15 (coded) bits by a LDPC code. The schematic of analogue LDPC decoder is depicted in figure 10. The layout corresponds to an unfolded bipartite graph. The implementation of the LDPC decoder is based on the concept developed in [3]. The MIMO decoder consists of 5 identical modules, each providing MPPs for 3 coded bits. The outputs of the MIMO decoder are wired directly to the analogue LDPC decoder. One of the modules is presented in figure 11. The layout of the module corresponds to a factor graphs that describes eq. 6 for the

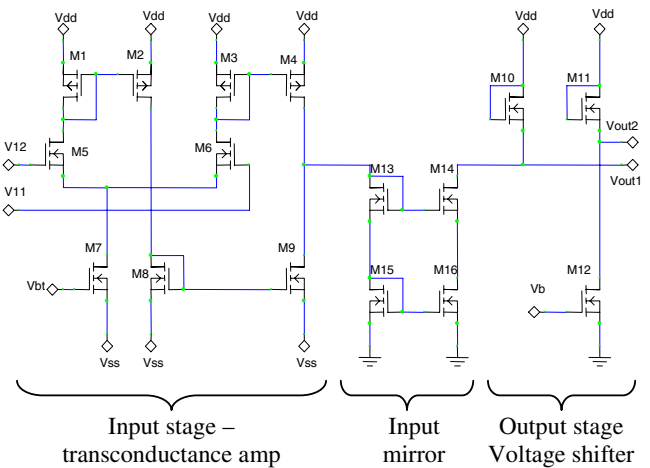


Fig. 8. Block Diagram of the negative exponential MOS circuit.

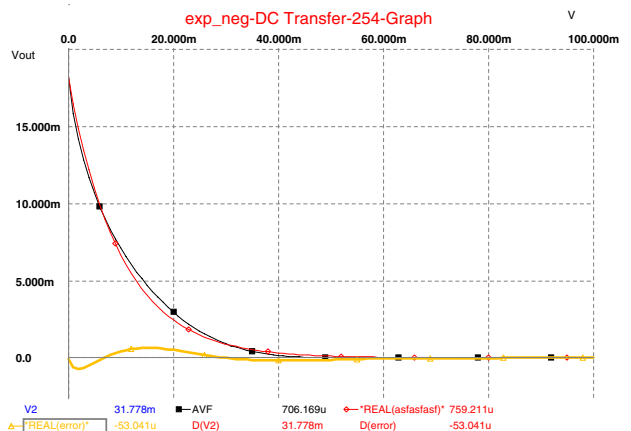


Fig. 9. Output characteristic obtained from SPICE and the ideal response.

case of $N_T = 3$ i.e. equation 7. The outputs of the modules are fed to the marginaliser block figure 12. The marginaliser consists of triple output cascode current mirrors (not depicted) and current summers of the type of figure 5. Table I depicts results of a comparison between the analogue LDPC decoder and a standard sum-product detection (software simulation of a digital decoder). A great accuracy of the analogue decoder can be observed. Table II depicts comparison results between analogue MIMO decoder and simulated exact APP MIMO decoder. A good accuracy of analogue MIMO decoder can be observed, albeit inferior to that of LDPC decoder. The inaccuracies are introduced mainly by the approximation in the exponential function and variations in the currents due to the non ideal behaviour of the transistors.

V. CONCLUSIONS

In this contribution we have proposed an analogue detector for a MIMO system. It is expected that such decoder will offer similar advantages as are reported by analogue binary decoders' i.e. significant improvements in: processing speed, reduction in transistor count, power efficiency and heat dissipation. On the downside, since the decoder mimics the full complexity APP decoder (albeit very efficiently), the transistor

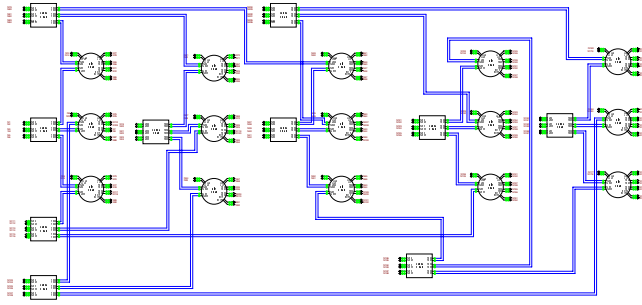


Fig. 10. Layout of the analogue LDPC code decoder.

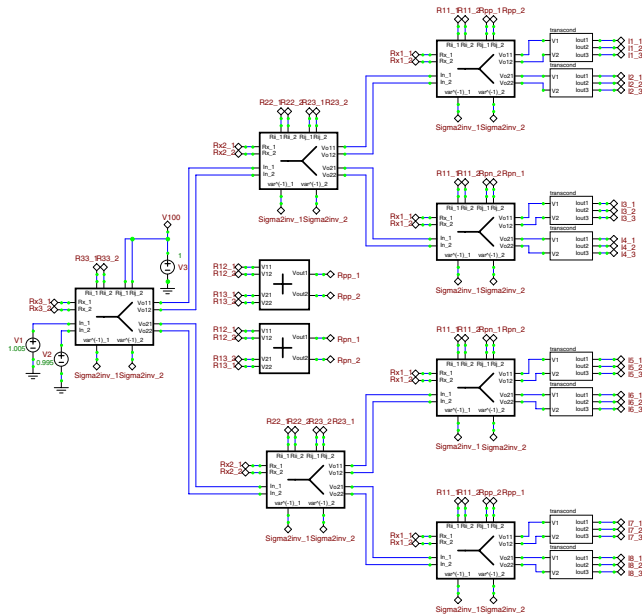


Fig. 11. Layout of the basic module of the analogue APP MIMO decoder.

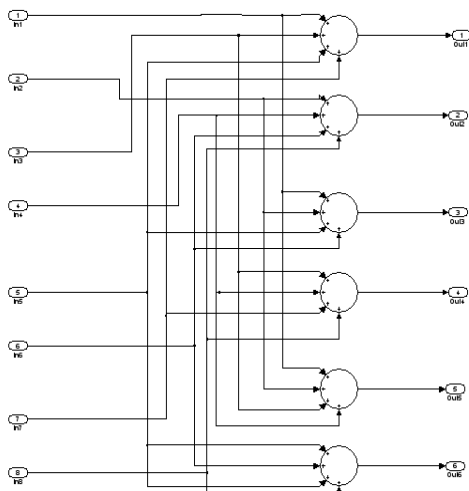


Fig. 12. Marginaliser.

TABLE I
ANALOGUE LDPC DECODER COMPARISON RESULTS.

Eb/No (dB)	mean(abs(error))	var(error)	Eq. iterations
0	2.90e-03	5.92e-05	41
1	5.00e-03	1.86e-04	100
2	4.90e-04	1.24e-05	41
3	1.08e-08	2.36e-15	20
5	2.91e-09	1.62e-16	12
7	4.37e-10	1.07e-17	4

TABLE II
ANALOGUE MIMO DECODER COMPARISON RESULTS.

Eb/No (dB)	mean(abs(error))	var(error)
0	0.02060	0.00086
1	0.02650	0.00150
2	0.02090	0.00110
3	0.01820	0.00095
5	0.01420	0.00073
7	0.01270	0.00093
9	0.01300	0.00130

count (not the processing speed!) increases exponentially. Such MIMO decoder may still be feasible for a MIMO system with small number of transmit antennas and simple modulation formats. However, one of the major challenges seems to be the design of reduced complexity high performance algorithms that could be executed in analogue VLSI networks.

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