Baltaci, Y., Kaya, I., & Nix, A. R. (2000). Implementation of a HIPERLAN/1 compatible CMF-DFE equaliser. In Vehicular Technology Conference 2000 (VTC 2000-Spring). (Vol. 3, pp. 1884 - 1888). Institute of Electrical and Electronics Engineers (IEEE). 10.1109/VETECS.2000.851599

Implementation of a HIPERLAN/1Compatible CMF-DFE Equaliser

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Abstract

The Channel Matched Filter Decision Feedback Equaliser (CMF-DFE) is a high performance equalisation method with reduced computational complexity; which is essential for high-speed communication systems with severe intersymbol interference. The method exploits the fact that matched filtering of a wideband channel results in a symmetrical channel profile centred on a real-valued peak while exploiting multipath diversity. This paper describes the implementation of a HIPERLAN/1 compatible equaliser using the CMF-DFE method. The performance of the implemented algorithm and the implementation benchmarks are given for the Hiperlan/1 standard. Results are also given for a number of different modulation schemes.

I. Introduction

Current demand for fast equalisation arises since it offers a successful countermeasure to the harmful intersymbol interference effects introduced by the indoor wireless channel. Equalisation enables the combining of multipath energy and ensures the viability of high data-rate communication. Given the development of wideband communication standards such as wideband-CDMA (W-CDMA) [1] and TDMA methods such as GSM, IS54, HIPERLAN [2,3,4], the development of equalisation algorithms and the implementation of filter technologies have become an important area for communication device manufacturers. This is particularly true for time-varying mobile radio channels, where adaptive filter design becomes a challenge because of the need for high-speed convergence and low power consumption.

The Channel Matched Filter Decision Feedback Equalizer (CMF-DFE) is a high performance equalization method recently developed at the University of Bristol [5,6]. The method exploits the fact that matched filtering of a wideband multipath channel results in a symmetrical channel profile around a real-valued peak. This guaranteed profile shape could be used to provide robust DFE symbol synchronisation. The CMF fully exploits the multipath activity in the channel and represents an optimum filter in the presence of noise. This results in a 3 dB improvement in the noise performance compared with conventional equaliser designs. Figure 1 shows the block diagram for the CMF-DFE concept.

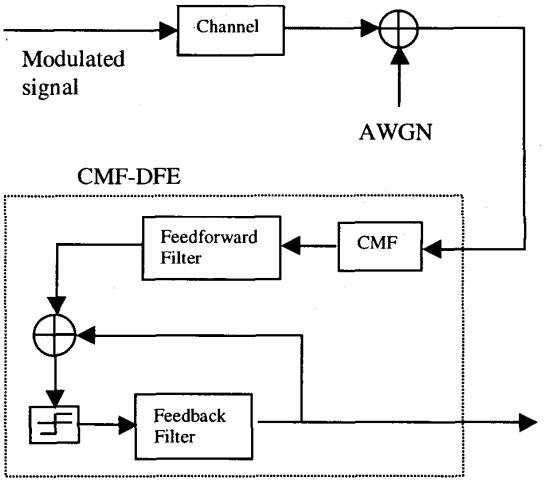

Figure 1 – CMF-DFE Equaliser.

II. Hiperlan/1 Standard and the Required Training Time

The Hiperlan/1 standard transmits data at 23.5 Mb/s and requires channel equalisation to overcome the harmful effects of intersymbol interference (ISI). The chosen modulation is Gaussian Minimum Shift Keying (GMSK) with a bandwidth factor (BT) of 0.3. The transmitted signal is precoded and toggled before modulation in order to receive the I and Q data in a manner similar to offset QPSK [7].

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The main structure of the Hiperlan/1 data packet consists of a 450 symbol long training packet and at least one 496 symbol long information packet. The training packet lasts for 18.2 μs and consists of five 31-bit long m-sequences repeated 3 times each. The last m-sequence is truncated to complete the training section using 450 symbols. Figure 2 shows the main structure of the Hiperlan/1 data packet.

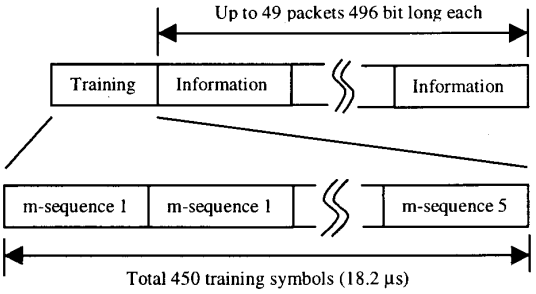

Figure 2 – Hiperlan/1 data packet structure.

Considering the high-speed data-communications present in Hiperlan/1, a simple and effective equalisation technique is required to provide an economic implementation. The CMF-DFE method has been proposed as an effective, high performance solution for Hiperlan/1 [6].

III. Principle Stages of the CMF-DFE

The CMF-DFE equalisation code for Hiperlan/1 has been ported to the Texas Instruments C62xx DSP platform and shown to meet the required training time. The CMF-DFE method requires the completion of 4 main steps during training.

- Channel estimation.
- Matched channel coefficient calculation.
- Feedforward filter coefficient calculation.
- Feedback filter coefficient calculation.

The performance of the CMF-DFE very much depends on the correct estimation of the channel profile. The channel estimation algorithm makes use of the first 31-bit PN sequence in the Hiperlan/1 training packet as illustrated in figure 2. In order to fully exploit the multipath activity and optimise the overall performance, a windowing algorithm is used to search over the resulting correlation output to find the channel profile that has the largest signal power within a 5 symbol period. At the same time, the position of the detected window provides frame synchronisation for the equalised data. The block diagram for the channel estimation algorithm is given in figure 3.

Since a considerable amount of time is required for the channel estimation process, the correlation is carried out assuming that the timing of the data is known within a 16 symbol accuracy. This course timing assumption should be considered as a worst case scenario since in practice the receiver will have a good knowledge of the high bit rate timing based on the reception of the previous low bit rate unequalised header. As a result, 16 x 31 complex multiply and accumulate operations are required for channel estimation assuming QPSK modulation. This value is doubled for GMSK modulation since only half of the PN sequence is sent using either the In-phase or Quadrature channels. It is therefore necessary to extend the correlation over 62 symbols for the Hiperlan/1 application.

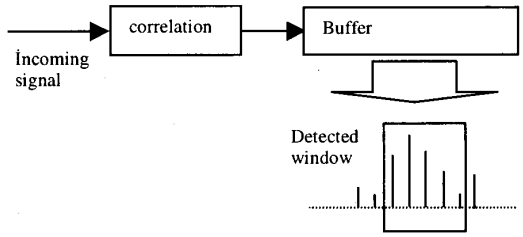

Figure 3 – Channel estimation.

Channel matched filtering represents a process that uses a filter with coefficients that are the complex conjugate of the mirror image of the estimated channel profile. If an ISI corrupted signal is passed through the matched filter, the resulting transfer function of the channel becomes symmetrical around a real-valued central peak. Moreover, channel matched filtering provides optimum symbol synchronisation for the equaliser filter [7]. The method results in a fixed timing point that does not fluctuate from channel to channel as shown in figure 4.

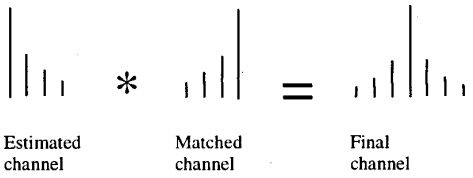

Figure 4 – Channel matched filtering.

The feedforward filter coefficient calculation involves solving a set of equations built from the convolution of the channel with the channel matched filter [6]. The solutions are obtained by

inverting a 5 x 5 Teoplitz matrix using the Gauss elimination method.

When the feedforward filter coefficients are obtained, the feedback coefficients can be calculated in a straightforward manner directly from the convolution of the feedforward filter with the matched channel coefficients [6].

IV. CMF-DFE Demonstrator using the C62xx EVM Board

The CMF-DFE equaliser algorithm has been ported to C62xx DSP taking into account the implementation issues described previously. The following cycle counts have been obtained.

	QPSK	GMSK
Training (entire)	**1967**	**3055**
Equalisation (per symbol)	**38**	**40**

Table 1 – Cycle counts for CMF-DFE.

As a result, the training takes approximately 9.8 μs for QPSK and 15 μs for GMSK modulation using a 200 MHz C62xx DSP. The higher training cycle count for GMSK is due to the longer channel estimation as described in section III. The results confirm that real-time Hiperlan/1 training and synchronisation can easily be achieved in DSP using the CMF-DFE method. It should be noted that the cycle counts during training are quoted for the entire training process, whereas for equalisation they are quoted as cycles per symbol.

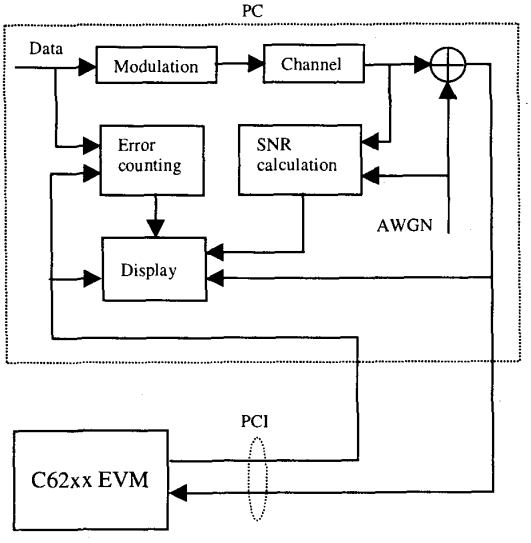

Figure 5 – CMF-DFE demonstration application

A demonstration program has been developed at the University of Bristol in order to test the implemented CMF-DFE DSP code running on the C62xx for different modulation schemes. The channel model and the transmission process have been implemented on the PC and sent to the EVM board through the PCI bus. The generated data is limited to 10-bit resolution in order to take into account the influence of 10-bit ADCs used in the Hiperlan/1 baseband CMF-DFE demonstrator board. The block diagram of the CMF-DFE demonstrator and an example screenshot of the program is shown in figures 5 and 6.

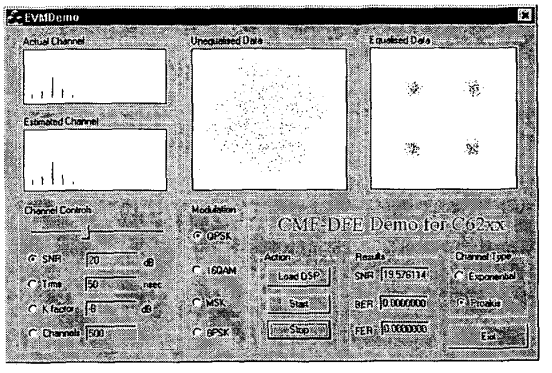

Figure 6 – CMF-DFE demonstration screen shot.

A baseband hardware demonstrator has also been constructed based on the same DSPs. The baseband transmitter consists of a GMSK modulator and DSP board. A daughter board has been developed for the C62xx EVM to digitize the incoming analogue baseband signal at twice the Hiperlan/1 bit rate. The digitized data has been separated into two different buffers, one containing even numbered samples and the other odd numbered samples. The buffer containing the higher energy is then chosen as the sampled input to the equaliser. The transmitter and the receiver are connected to each other via coaxial cables to test the CMF-DFE as shown in figure 7.

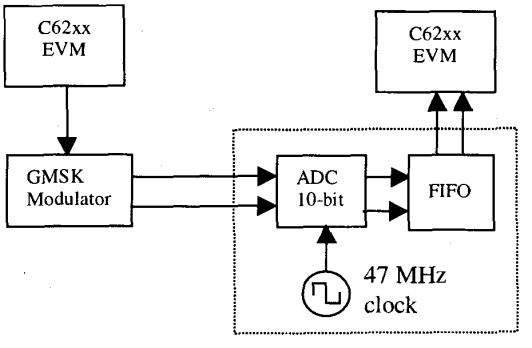

Figure 7 – Baseband CMF-DFE demonstrator

V. Performance Results

Performance results have been obtained for a number of different modulation schemes. For a 50 ns rms delay spread channel based on an exponential delay profile, 1500 uncorrelated wideband Rayleigh channels were generated on the PC and sent to the DSP card for equalisation. Figure 8 shows the performance comparison for MSK, QPSK, and 8-PSK modulations versus signal-to-noise ratio. The channel was simulated using a T-spaced model assuming optimum sampling at the receiver. In the DSP, 16-bit fixed-point arithmetic has used for all modulation schemes.

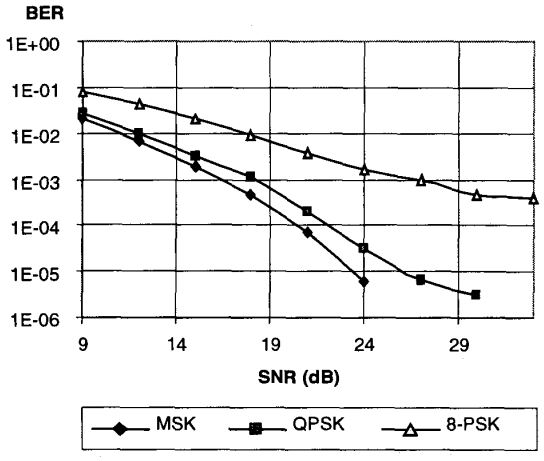

Figure 8 – Performance of 16-bit CMF-DFE.

Moreover, in order to compare the performance of the DSP code with a floating point "C" implementation, identical channel conditions were recreated and the resultant signal equalised using the floating point "C" and 16-bit DSP versions of the CMF-DFE code. Figure 9 shows that the 16-bit implementation is slightly inferior when compared to the floating-point solution. This is to be expected since the floating point approach has a much wider dynamic range.

A realistic Hiperlan/1 simulation has been also implemented and the simulated baseband signal sent to the DSP. In Hiperlan/1, the specified modulation scheme is GMSK with a bandwidth factor of 0.3 (BT = 0.3). In order to receive the I and Q signals at receiver directly in the phase domain, the data is precoded prior to the modulation as described in the standard.

Since it is impossible to perfectly know the optimum sampling point at the receiver, the simulated signal is sampled in a random manner, assuming 8 samples per symbol, for each channel and sent to the DSP accordingly. Also ETSI recommended a T/2 spaced channel model. This model was used with a 50 ns rms delay spread obtained using an exponential delay profile

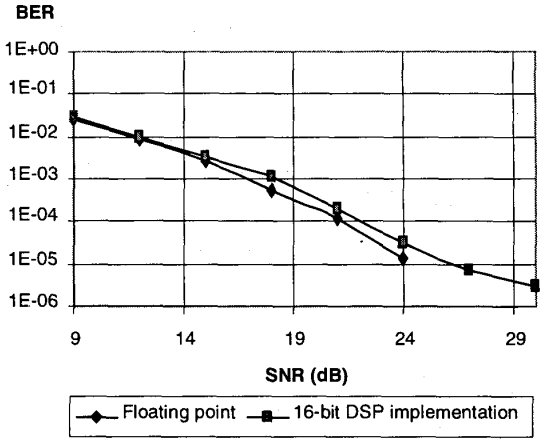

Figure 9 – Performance comparisons for floating point and 16-bit QPSK implementations.

Figure 10 shows that the 16-bit DSP implementation of the CMF-DFE for Hiperlan/1 is considerably better than the result obtained using the well-known LMS method. The LMS has also been considered for Hiperlan/1 due to its simplicity. Using current DSP technology, it is impossible to train an LMS based equaliser to the CMF-DFE performance level in real-time for Hiperlan/1. As a result, we conclude that the CMF-DFE is far easier to realize in current DSP technology and also has superior performance.

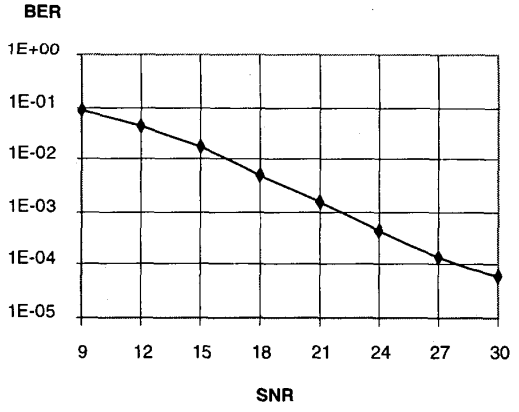

Figure 10 – Performance of 16-bit CMF-DFE in Hiperlan/1 (rms delay spread = 50 ns). GMSK modulation BT = 0.3. ETSI recommended T/2 channel model.

VI. Equaliser Filter Considerations

From table 1, it can be seen that it is possible to train the CMF-DFE equaliser filter in real time for

Hiperlan/1. However, the maximum achievable data-rate using the DSP for equaliser filter implementation is approximately 5 Mb/s. This is far from the required 23.5 Mb/s data-rate of Hiperlan/1.

In order to investigate the feasibility of using an ASIC circuit for the equaliser filter, different coefficient resolutions have been used for the same channel conditions. It was found that the equaliser filter coefficient resolution could be decreased to 6-bit resolution without any considerable performance degradation so long as the training is implemented in a 16-bit resolution DSP. The simulations have shown that the degradation is only about 0.1 dB if the calculated equaliser filter coefficients are truncated to 8-bits. This implies that it would be straightforward to implement and equaliser filter accelerator ASIC using a relatively small FPGA device.

The block diagram for a real-time Hiperlan/1 CMF-DFE equaliser based on the C62xx training engine is given in figure 11.

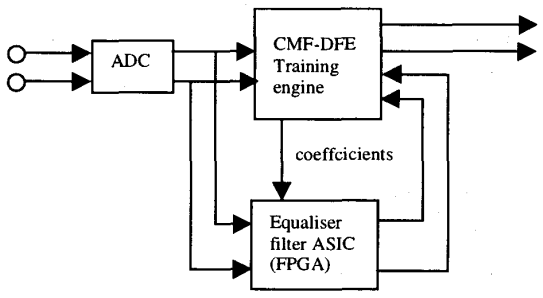

Figure 11 – Block diagram of the real time Hiperlan/1 CMF-DFE equaliser.

VII. Conclusions

The implementation of the CMF-DFE method has been described in this paper using the Texas Instrument C62xx. It has been shown that real time implementation of CMF-DFE equaliser is possible for Hiperlan/1 using existing DSP technology.

It was found that the performance degradation of the CMF-DFE method is negligible if the trained equaliser coefficients are truncated to smaller resolutions when loaded into the equaliser filter. The importance of this finding is that for custom hardware or DSP acceleration, the CMF-DFE method can offer a low power and high performance equalisation solution for Hiperlan/1.

VIII. Acknowledgements

The authors would like to thank Texas Instruments for the donation of DSP hardware and the provision of funding to perform these studies. In particular we would like to thank Greg Peak and David Thomas of Texas Instruments.

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