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A Flexible Test-Bed For Developing Hybrid Linear Transmitter Architectures.

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Abstract

The focus of this paper is a digital test-bed that accommodates flexibility in the designing of hybrid architectures. It comprises a high-speed analog-to-digital and digital-to-analog interface, an FPGA and a C6x DSP evaluation board for signal-processing. The remainder of the test-bed comprises a RF transmitter. The modular nature of the test-bed allows it to support either quadrature baseband or digital IF sampling. The use of a FPGA and DSP for digital processing allows high throughput whilst allowing complex linearisation algorithms. The test bed performance is demonstrated using the Cartesian loop transmitter architecture. The Cartesian loop was chosen as it is a well known linear transmitter architecture. Further work will be to include two or more architectures to raise the efficiency and performance (greater linearity or bandwidth). The candidate schemes for hybrid architectures with Cartesian loop are pre-distortion, envelope elimination and restoration and dynamic biasing.

1 Introduction

Linearisation of power amplifiers to meet spectral emission standards has been extensively researched and many techniques have been found, e.g. predistortion, Cartesian Loop, Envelope elimination and restoration, Polar Loop, LINC and CALLUM. The various techniques have allowed very high degrees of linearity over a narrow bandwidth or moderate amounts of linearity over a wider bandwidth.

The different techniques have various efficiency trade-offs. In order to meet the linearity specification of current standards employing linear-modulation (i.e. those with varying RF envelope), linearisation methods in common use today generally have low efficiencies. Most schemes trade efficiency for linearity in that the linearisation scheme can only apply a certain amount of distortion suppression after which the power amplifier (PA) must provide the remaining distortion reduction. Thus, if high linearity is required, the PA must be more linear at the expense of power efficiency. In this context the extra linearity is obtained by backing-off the PA so that its output power is well below its peak power rating. Typically the adjacent channel power ratio (ACPR) improves 2 dB for every dB of power back-off.

Table 1 shows a comparison of three standards that can benefit from PA linearisation. TETRA[1] was designed as a replacement to analog PMR networks and imposes one of the toughest transmitter linearity requirements facing RF designers today. EDGE[2] is less stringent and as such could be met by backing off a class-AB power amplifier, albeit at the expense of efficiency. EDGE is an evolution of the GSM network to allow operators to get the full benefit of there GSM networks whilst rolling out full 3rd generation UMTS networks[3]. The UMTS[4] transmitter solution is quite different (due to its wide-bandwidth) to that of TETRA and EDGE and will not be considered in this paper.

Specification	EDGE	UMTS	TETRA
RF bandwidth	225 kHz (99%)	5 MHz (99%)	18 kHz (-3dB)
Channel spacing	200 kHz	5 MHz	25 kHz
Modulation	π/8-QPSK	W-CDMA (QPSK)	π/4-DQPSK
Symbol rate	271 kb/s	3.84 Mchip/s	18 kb/s
Power spectral mask	200 kHz offset = -30 dBc[1] 250 kHz offset = -33 dBc[1] 400 kHz offset = -60 dBc[1]	2.5 MHz offset = -35 dBc[1] 3.5 MHz offset = -45 dBc[1] 7.5 MHz offset = -54 dBc[2]	25 kHz offset = -60 dBc[3] 50 kHz offset = -70 dBc[3] 75 kHz offset = -70 dBc[3]
1 Measurement bandwidth is 30 kHz bandwidth 2 Measurement bandwidth is 30 kHz bandwidth, (Specification is actually –39 dBc in 1 MHz Bandwidth) 3 Measured in 18 kHz band centred about offset.			

Table 1. Comparison of EDGE, UMTS and TETRA transmission mask specifications.

The market drivers for lightweight handheld terminals and long talk-time are heavily related to the technical metric of transmitter power efficiency. Techniques that make the radio more efficient allow smaller (lower capacity) batteries or a longer useable time between

battery charge-cycles[5]. The transmitter places a heavy demand on the battery, and therefore, utilising more efficient transmitters can increase talk-time or reduce the battery size. Advances in technology are unlikely to significantly improve the efficiency of the current linearisation methods operating on linear power-amplifiers such as class AB. This is due to the poor efficiency of these PA's[6]. Additionally non-linear amplifiers such as class C are difficult to linearise significantly using any one method.

A need exists for exploring and comparing schemes and in particular, for coupling together two or more schemes into hybrid architectures to improve the bandwidth, linearity and efficiency above that available from any one scheme. The hybrid method employs complementary techniques that overcome the weakness (or constraints) that any one method has on its own. By removing constraints the hybrid architecture is more flexible and can cover more standards thus making it suitable for a software defined radio.

2. The digital test-bed

The focus of this paper is a digital test-bed (as shown in figure 1 that accommodates flexibility in the design of hybrid architectures. It comprises a high-speed analog-to-digital and digital-to-analog interface, a digital signal-processing unit, and interchangeable transmitter line-up. The modular nature of the test-bed allows it to support either quadrature baseband or digital IF sampling. By using quadrature demodulators to translate the RF signals to baseband, the converters can operate as conventional sampling ADC's, or they can sample an IF frequency, either by subsampling or Nyquist-rate sampling. The choice between IF sampling and baseband sampling depends on the bandwidth and final RF frequency required. Sampling the IF directly reduces the component count by one ADC. The use of an IF stage can introduce image products which must be removed by filtering, this can be difficult unless a high IF frequency is chosen. Most handportables are required to operate over many channels, so the IF filter must track the changing image. Tracking filters with sufficient attenuation are difficult to implement and are not desirable. Finally, the use of miscellaneous ADC's and DAC's can be used for additional control of the analog transmitter line-up, e.g. envelope control of the PA bias.

The processing is carried out via a FPGA and DSP to facilitate highly complex algorithms and fast throughput rates. The FPGA primarily provides high speed I/O operations, e.g. as needed in a Cartesian loop where the time delay introduced by the use of FIFO's would render it unstable[7]. The DSP is better suited to complex algorithms that are not required to operate in real time e.g. as in calibration settings, or training algorithms.

The hardware implementation used in the digital test-bed uses two Analog Device AD9201's for input signal ADCs, and two AD9750's for the output signal DACs. The input signals can be sampled at 20 MSPS, giving a maximum baseband-bandwidth of 10 MHz. The FPGA is a Xilinx Virtex XCV200, this device has a large gate capacity as well as onboard RAM for look-up-tables (LUT's), thus most algorithms and systems are easily catered for. The FPGA board has provision to interface to a Texas instruments C6x EVM board.

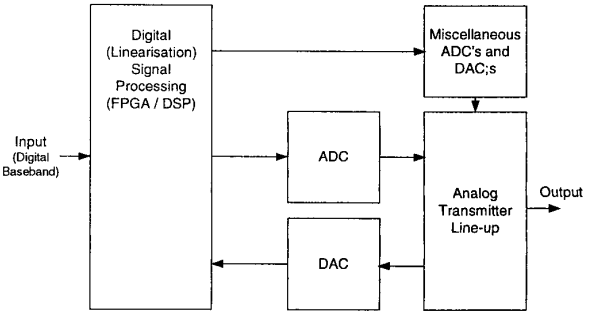

Figure 1. Test bed block diagram.

3. Cartesian Loop Implementation

Linearisation of power amplifiers using Cartesian loop[8] is a technique which achieves high degrees of linearity over a narrow bandwidth. As the bandwidth is increased the degree of distortion suppression must be reduced to maintain stability.

A conventional Cartesian loop is shown in figure 2. A directional coupler samples the output of the transmitter where it is quadrature-demodulated to Cartesian co-ordinate signals, and subtracted from the input to form a complimentary distorted error signal. After the loop filter, the distorted error signal is complimentary to the PA distortion signal at its output. Thus, at the output of the PA the distortion is cancelled[9]. The amount of distortion reduction is equal to the open loop gain of the loop, thus inside the loop-filter pass-band this gain is high and good levels of cancellation are achieved, outside this bandwidth the gain drops, as does the level of cancellation. The stability of the loop is dependent on the open-loop-gain, time-delay in the RF circuitry and the loop-filter bandwidth. Thus, bandwidth and linearity are traded off against each other for a given stability margin. The phase shifter is needed to counter for RF delays which cause rotation of the signal constellation [7,10]. The modulation can be coherently demodulated by phase shifting the local oscillator (LO) to either the quadrature modulator or demodulator. The amount of phase shift is unique for every channel, and generally requires a training sequence to determine the optimum setting.

correction achieved in the 1st, 2nd and 3rd adjacent channel is, 20.9 dB, 11.7 dB and 5 dB respectively. Figure 5, shows the correction in the intermodulation distortion versus the offset from the channel centre frequency.

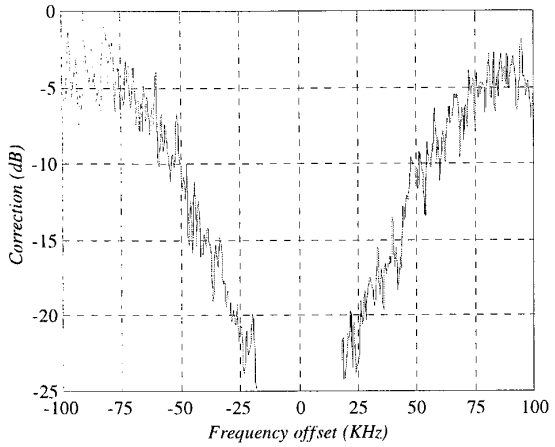

Figure 5. Amount of correction achieved as an offset from channel centre frequency

The TETRA specification requires the 1st, 2nd and 3rd ACPR to be –60 dBc, -70 dBc and -70 dBc respectively. Thus at least another 10 dB of correction is necessary to meet this specification. The limit on the correction is due to the loop stability, increasing the open loop gain increases the correction yet decreases the stability margin. The implementation uses a single-pole loop-filter. More complex filters are possible that increase the stability margin, and thus allow more correction[12].

4. Envelope Elimination & Restoration (EER)

Figure 6 shows a conventional EER transmitter. The RF signal s(t) is separated into its envelope and phase components (i.e. polar co-ordinates). The PA amplifies the constant-envelope phase signal, and the envelope signal modulates the voltage supply to the PA. The PA is usually a high efficiency class e.g. C, D or E. As the PA operates on a constant envelope signal, it's output is more linear. The amplitude modulator operates on the envelope signal and is commonly class S and is also highly efficient.

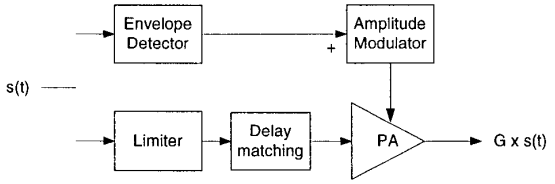

Figure 6. Envelope Elimination & Restoration (EER)

The EER transmitter whilst simple, achieves only modest amounts of correction and requires delay lines to compensate for differences between the envelope and phase path delays[13]. The addition of envelope feedback is popular and some implementations of this have achieved intermodulation distortion (IMD) of –30 to -50 dBc (for 1W to 20W) and efficiencies of up to 50% [14,15].

For modern applications, the limiter and envelope detector are replaced with digital processes that generate the envelope and phase signals directly from the baseband signals. Figure 7 shows the Cartesian loop in a hybrid with an envelope modulated PA. The use of Cartesian feedback can replace or help envelope feedback, as well as reducing phase distortion effects due to high envelope modulation depths, and time delay mismatches. Additionally as the envelope and phase generation processes are now inside the Cartesian loop, their specifications may be relaxed just as they were for the DAC's in the DCL.

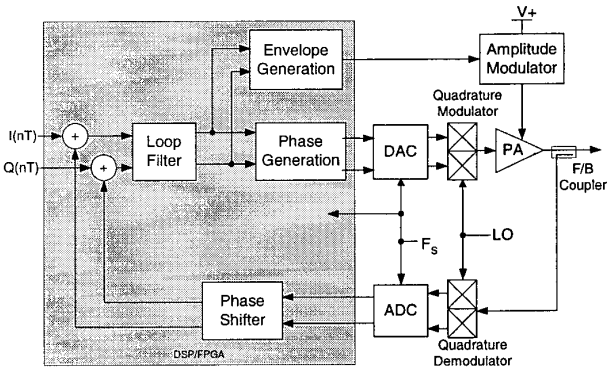

Figure 7. Hybrid Cartesian Loop and Envelope Restoration Linearisation.

5. Dynamic biasing.

The architecture shown in figure 7 can be easily modified to allow the PA gate to be dynamically biased[16]. The gate bias or drive of the PA is altered according to the instantaneous envelope amplitude. The PA bias point can then be optimised for maximum efficiency or linearity as needed. As the envelope information is already generated, all that is needed is a mapping of the envelope to gate/bias or drive level. As the power required to alter the gate bias is small, linear techniques can be used without compromising efficiency.

6. Predistortion & Cartesian Loop

Figure 8 shows a predistortion and Cartesian loop hybrid first reported by Mansell[17] as an analog Cartesian Loop. Note, that without the feedback & input summation stages, figure 8 would only implement predistortion. Predistortion is a method of linearisation that distorts the input modulation so that the combined gain characteristic of the amplifier and predistorter is linear. This requires

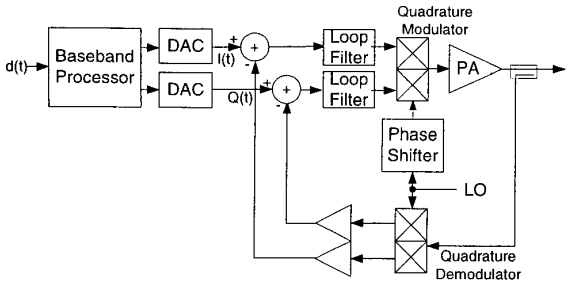

Figure 2. Analog Cartesian loop transmitter.

The test-bed performance is demonstrated using the Cartesian loop linear transmitter architecture as it is a well known, additionally the use of digital techniques simplifies the implementation of this architecture. The test-bed is used to replace the linearisation-baseband-section of a Cartesian loop, i.e. feedback summation amplifier, loop filter, and phase shifter, (see figure 3). This configuration of Cartesian loop shell be referred to as Digital-Cartesian-Loop (DCL). The FPGA performs the real-time loop functions of the DCL, and the DSP is left to do the non-real-time calibration and configuration functions. Replacing the baseband processing with digital circuitry gives many advantages, namely,

1. The phase shifter can be precisely implemented at baseband (with no noise or distortion introduced), in either the feedback path or forward path as a matrix rotation, e.g.

$$\begin{bmatrix} \hat{I}(nT) \\ \hat{Q}(nT) \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} I(nT) \\ Q(nT) \end{bmatrix}$$

   where θ is the desired phase shift angle.
2. The signals needed for calibration are already digital. Thus, the extra ADC's and DAC's required for calibration purposes are eliminated, reducing component count and easing circuit layout.
3. The DAC's at the input in figure 2 are now moved inside the loop, thus their specifications can be relaxed[11]. The noise and distortion inside the loop-filter-bandwidth will be reduced in a manner similar to the PA. However outside the loop bandwidth the noise and distortion will not be reduced and the specifications of the DAC must be able to meet these.
4. Factors affecting performance such as loop filter bandwidth and gain are now reconfigurable, allowing multiple standards to be used by a single hardware platform.

These advantages are slightly offset by the addition of the two ADC's in the feedback path which are required to have the same linearity and noise performance as needed at the transmitter output. Assuming that the digital processing was integrated in with the baseband processor (for little extra area cost) the overall saving is the removal of the phase shifter, some baseband amplifiers, and some DAC's & ADC's used for calibration

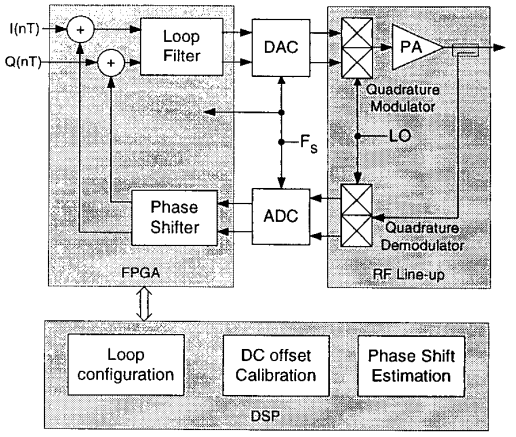

Figure 3. Digital baseband version of Cartesian loop transmitter

To implement the Cartesian loop the sampling frequency used was 11 MHz. The digital latency was five samples, three from the ADC, and two from the FPGA. The PA was a class AB module. Tests were made at 400 MHz. Figure 4, shows the PA output for TETRA modulation i.e. π/4-DQPSK, 18 kbaud, and root raised cosine filter with roll off factor, $\alpha = 0.35$. The DCL was configured to give 20 dB of correction at a power level of +31 dBm (1.26 W).

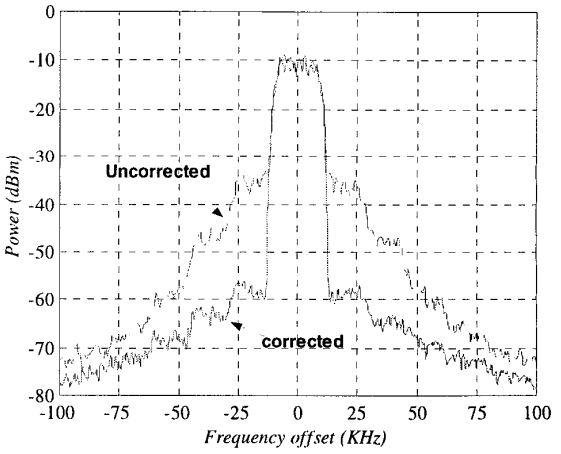

Figure 4. Performance of the digital Cartesian loop for TETRA modulation.

The channel spacing for TETRA is 25 kHz, and channel bandwidth is 18 kHz. The ratio of power in adjacent channels to the signal power is called the adjacent channel power ratio, (ACPR). The 1st, 2nd and 3rd ACPR is –48.5 dBc, -56 dBc, and -62.3 dBc respectively. The

knowledge of the PA non-linearity, which changes with temperature, VSWR, frequency, output power and other environmental effects. Thus adaptive predistortion is a method of continually updating the predistorter with a characteristic that is complimentary to the PA[18,19].

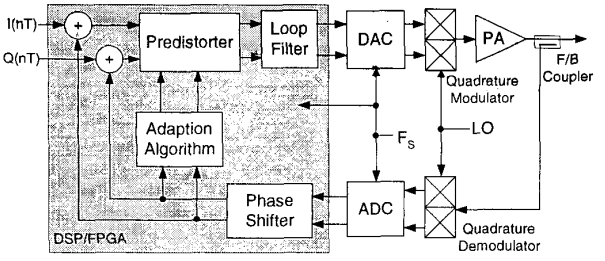

Figure 8. Predistortion and Cartesian Loop.

The error signal of the Cartesian loop is predistorted. Thus the predistorter partially linearises the PA, and the Cartesian loop further linearises the predistorted system. It is possible to predistort the feedback signal or the input signal, but to do so requires the predistorter to have a more stringent spurious frequency specification. The combined techniques of predistortion and Cartesian loop provide greater linearisation correction than either individually, this extra correction can be used to increase PA efficiency as well as increase the Cartesian loop's stability or bandwidth. The hybrid of digital Cartesian loop and predistortion is favoured over the analog implementation because;

1. The addition of predistortion adds no extra components to the hardware. It increases the size of the digital section, which is minor compared to the addition of DAC's, ADC's and summing amplifiers as needed in the analog case.
2. The phase shifter can be set precisely, removing this variable from the adaption algorithm.

7. Conclusion

A digital test-bed has been demonstrated that can perform Cartesian loop linearisation. The Cartesian loop was able to obtain 20dB correction for TETRA.

The successful digital implementation enables the testing of hybrids of Cartesian loop and other linearisation methods such as EER, Dynamic biasing, & Predistortion. The synergy of two linearisation schemes together will potentially give significant efficiency boosts over any single scheme alone.

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