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TRUST Approach to Software Defined Radio: RF Considerations

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Abstract: *The design of the RF component of a Software Defined Radio (SDR) is a challenging task. This paper sets out to examine the important issues concerning the design of both the transmitter and the receiver. Techniques of achieving wideband linearity in the transmitter are reviewed. The importance of being able to design a low phase noise oscillator to operate over a wide range of frequencies is discussed. Receiver architecture is also reviewed. The major problems associated with the design of the receiver component of an SDR (linearity and image signals) are reviewed. The relationship of blocker specifications to receiver linearity is described. The paper concludes with a discussion of some problems unique to SDRs, and in particular those that need to be transparently reconfigured.*

1. Introduction

A large amount of research work has gone into the various aspects of software radio design. The TRUST project sets out to consolidate this work as far as the user's terminal is concerned. The need for reconfigurable terminals from various perspectives (in particular the end-user) and the associated mapping to technology innovation within TRUST is described in [1]. TRUST will look at user needs, power management, scalable video coding, transceiver algorithms, spectrum sharing techniques, system identification in Composite Radio environments, Multimode monitoring and intelligent mode switching, Radio resource allocation for software download, and network support for burst by burst adaptive algorithms at physical layer. In addition, TRUST will look at Baseband architecture and Radio Frequency architecture. It is the latter 2 considerations on which the whole edifice of Software radio will rise or fall. Producing an elegant design for the radio side of the software radio is a big challenge, and this paper sets out to examine some of the issues. Baseband issues are canvassed in a companion paper [2].

2. Transmitter design

2.1 Introduction – Transmitter design

The wideband linear transmitter is one of the critical components in the flexible mobile terminal. This transmitter will be required to operate at frequencies extending from 900MHz to 5.5GHz covering the GSM, DECT, UTRA, Bluetooth and HIPERLAN/2 bands. Some of the modulation formats to be transmitted impose strong technical requirements by themselves[3], but the difficulty gets really extreme when they require to be solved in a common design. High output power, linearity, efficiency and carrier frequency accuracy are some of the important parameters to be considered for this transmitter in all the frequency bands. As most of the transmitter designs previously reported are of a narrowband nature, an SDR transmitter will need to be a state-of-the art design.

2.2 Trust transmitter concept

A general block diagram for this transmitter is shown in Figure 1. It will have three main component parts: a two-stage up-converter, the local oscillators, and the power amplifier. Since the technical specifications differ from one block to another, it is feasible to initially

develop separate designs for each one. In this sense, we have conceived a two-stage solution: first, working simultaneously in the most suitable architectures for each case, and second, integrating them into a transmitter prototype.
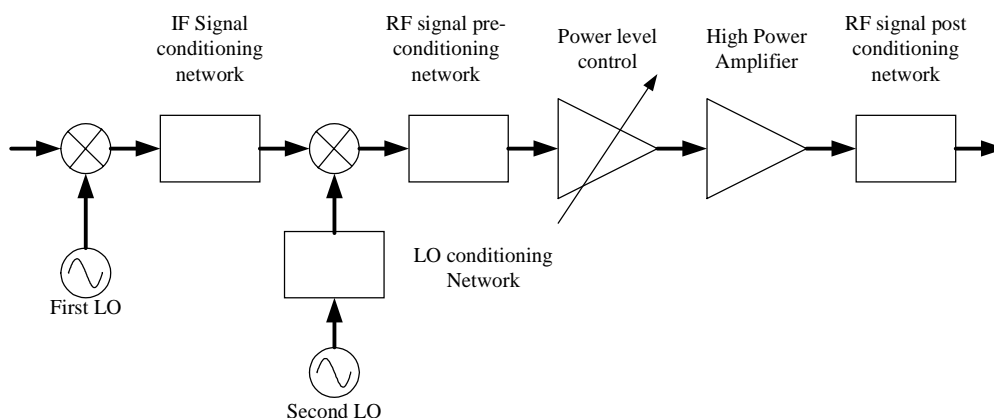

Figure 1 Transmitter general block diagram

2.2.1 Up-converter

A first up-conversion stage should translate the different modulation formats to a fixed intermediate frequency around 240MHz. Different commercial products can be found to implement the mixer and the fixed local oscillator without important problems.

The second up-conversion is then required to translate the signal from this fixed intermediate frequency to the different final output frequency bands. In order to assure a highly linear conversion, special care should be taken in conditioning the IF and local oscillator signals for the optimum second mixer performance. Thus, the IF power level, and specially the IF bandwidth, should be properly adjusted for each modulation format. One suitable solution for the bandwidth control relies on the use of a bank of filters, probably with lumped elements; but some other possibilities will be considered in order to obtain a flexible filter design with the possibility of arranging things so that the bandwidth is voltage controlled.

2.2.2 Second local oscillator

A wideband oscillator could be implemented with a wideband negative resistance element and a low Q resonator. As this second local oscillator should generate frequencies in different bands with good phase noise behaviour, this solution is not adequate[4].

Obtaining the desired phase noise performance seems to be only possible, if a wideband negative resistance element, with different high Q resonators (one for each band) is then employed, as shown in Figure 2.

The phase locked loops should thus have a main loop and different sub-loops for properly controlling each resonator. Each of these sub-loops will properly define the channel carrier frequency according to the associated format (channel spacing will vary from 200 kHz in GSM up to 20 MHz in HIPERLAN/2).
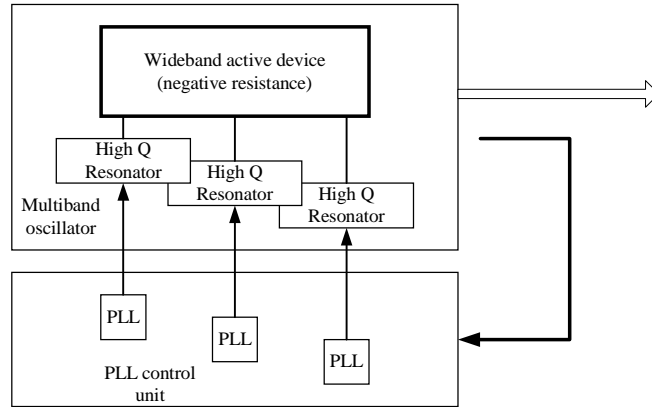
Figure 2 Second local oscillator.

2.2.3 Power Amplifier

A general diagram for the power amplifier is given in Fig. 3. This block is the one that imposes the strongest design challenges[5]. It should guarantee high power, efficiency and linearity in the different bands. Some studies have supported the possibility of employing a common power device, but special care should be put into the design of the input and output networks which are forced to provide multiband matching.

Multiband matching is preferred over the use of a bank of narrowband matching networks, due to the critical problems that may appear when switching from one network to another at high power levels.

A combination of predistortion and feedforward schemes[6] seems to be needed in order to get the low distortion requirements. These schemes could be made simpler if some effort is dedicated to improving the linearity of the selected device, with proper bias point and load control.
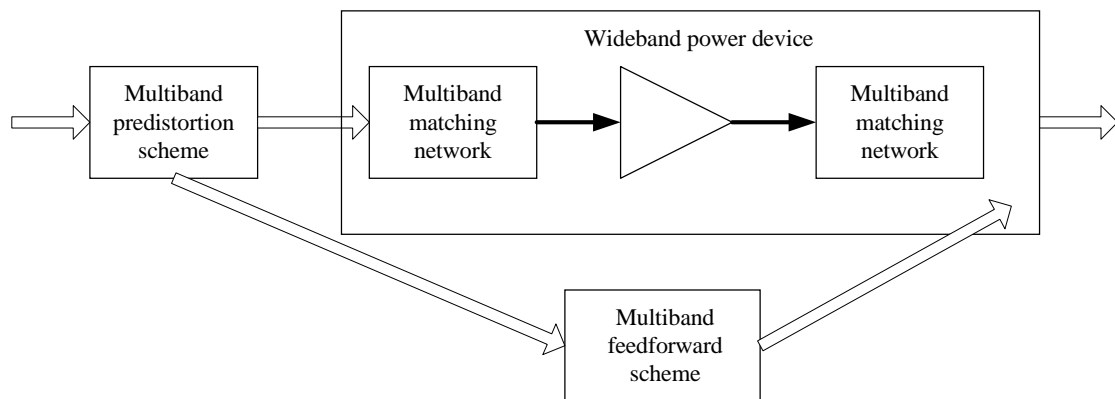

Figure 3 Power amplifier configuration

2.3 RF pre- and post- conditioning networks

These networks are mainly conceived to remove the spurious products that may appear after the second conversion or after the power amplifier. As the spurious frequencies differ from selecting one format to another, special care should be put in making these networks of reconfigurable nature.

The real problem arises when designing the network at the power amplifier output, due to the difficulties related to switching one in a set of networks in that point. Research should be done in the near future, to solve this particular question.

3. Receiver Design

3.1 Introduction – Receiver Design

Ideally a software radio should have the ADC placed as high up the receiver RF chain as possible.

A survey of ADCs available today[7] shows that the technology is not available to achieve the required simultaneous wide bandwidth, high sampling rate, high dynamic range, and low power consumption. Theoretical consideration[8] will also show that the power consumption of an ADC increases with increase in dynamic range and sampling rate.

We are thus left with traditional RF hardware, which has to somehow be made more flexible. A first approach would be to remove filters or make them wider bandwidth. Filters are placed in traditional radios to solve two problems. Firstly, they are there to prevent high power interfering signals from overloading the receiver, and secondly, they are there to deal with image signals. If they are removed, or their effectiveness is reduced, then other ways of dealing with the problems they solve, must be introduced.

Image signals result because, during the process of mixing down, both the high side product, and the low side product are mixed down to IF. The unwanted product is referred to as the image signal. The image signal is always separated from the wanted signal by twice the IF frequency.

3.2 Receiver Architecture

There are a number of approaches to the radio receiver architecture. Those of interest to the designer of an SDR can be classified as:
    (a) Zero or low IF architecture.
    (b) Multiple conversion with one or two final conversion possibly done in DSP.

3.2.1 Zero IF architecture

A typical Zero IF (or "Direct Conversion") receiver is shown in Figure 4. This architecture

has the advantage that if the 2 local oscillator signals are in phase quadrature, and exact

amplitude balance, then the image signal will be cancelled[1]. Additional advantages of this

configuration have to do with its simplicity, that is, one local oscillator and minimal filtering.

This advantage makes it attractive for integrated "one chip" radios.

For these advantages, a high price is paid. The principal disadvantages of direct down conversion are:
    (i.)   The local oscillator must produce two signals that are in precise phase quadrature, and precise amplitude balance, over the whole frequency range covered by the receiver. This is extremely difficult to achieve.

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[1] In this case the image signal is the wanted signal, folded backwards in frequency.

(ii.)   Most of the gain occurs in one amplifier. This results in the possibility of amplifier stability problems.

(iii.)   It is possible for local oscillator signal to radiate from the receive antenna.

(iv.)   It is possible for the local oscillator to reflect off the time varying impedance of the antenna. This can result in a slowly time varying signal being detected.

(v.)   1/f noise, and DC offset of the base band amplifier will cause problems[2].

(vi.)   Second order distortion products will appear in the baseband signal.

Despite these disadvantages, a zero IF stage is still possible (see for example ref.[9],[10]). A slight variation on the direct conversion concept is the "Low IF" architecture[11],[12]. A low IF architecture uses conversion to a very low frequency IF to overcome the problems of 1/f noise and DC offset associated with the full direct conversion. Because the image and the wanted signals are separated by only a small frequency, image reject mixing is still required. The difficulty of applying low IF, or zero IF technology to a flexible receiver design however is enormous, and these architectures are not seen as a short or medium term solution.
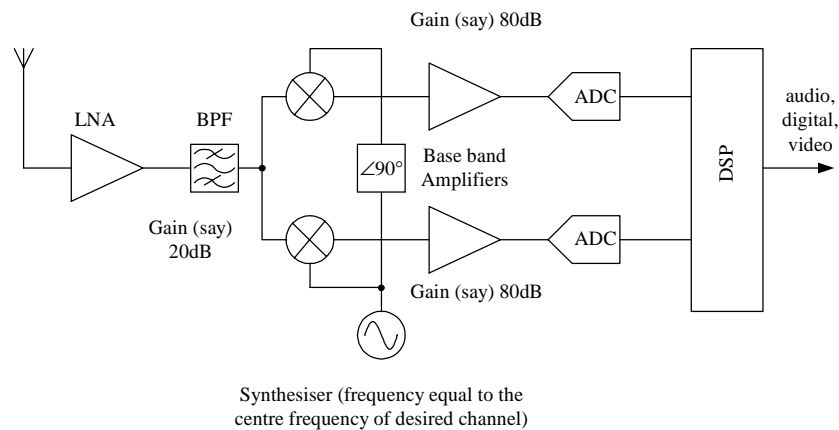

Figure 4 Zero IF (direct down conversion) receiver

3.2.2 Superhetrodyne architecture

The rejection of a direct conversion approach to receiver design leaves the conventional superhetrodyne structure to be investigated. With a superhetrodyne receiver, double, triple or higher order down conversions are possible. In order to avoid image signals "crowding in" on the wanted signal, high changes in signal frequency are to be avoided. It is for this reason that a triple IF structure has been chosen as a preferred receiver architecture. A dual conversion architecture would require big frequency changes, and a higher number of conversions would be needlessly complex.

3.2.3 Triple conversion architecture.

This type of architecture is illustrated in Figure 5. This architecture overcomes the limitations associated with direct conversion, and introduces a few of its own. The good news is that all of the RF gain need not be placed at one frequency, the 90° phase shifted oscillator has only to be set up at one frequency, the second order distortion products are out of band, the local oscillator frequencies are likely to be out of band, and the 1/f noise is not such a problem.

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[2] DC offsets are caused by self-mixing of the local oscillator signals as they leak through the mixer and are reflected from various parts of the RF circuit. They are a particular headache for "would be" direct conversion receiver designers.

The downside of this architecture is its complexity relative to a zero IF solution, and the fact that the image rejection problems, which the direct down conversion architecture more or less solves, now reappear.
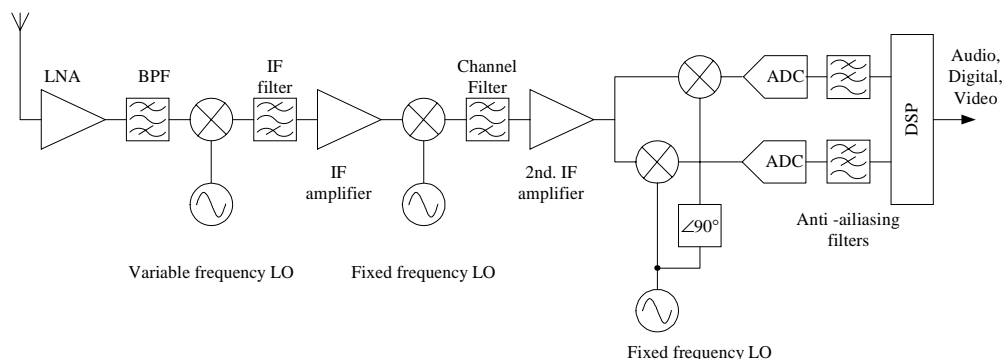

Figure 5 Triple conversion with final conversion done in hardware.

The separation of the image signal from the wanted signal is twice the IF frequency. To be able to remove the image signal via filtering, it is desirable that the image signal be separated from the wanted signal by as high a frequency as possible. This implies a high first IF frequency.

From the point of view of being able to reduce the distortion performance required of the amplifier/mixer chain that constitutes the receiver, it is important that channel filtering be done as high up in the receiver chain as possible. This could be done in the "channel filter" in Figure 5. For flexibility, this filter would need to be made switchable (say from 20MHz (HIPERLAN/2) to 5MHz (UMTS) to 200kHz (GSM)). The importance of this filter is that it "mops up" the distortion products. Final channel filtering would be required to take place in the DSP, where the mathematically defined pulse shapes of the root raised cosine, or Gaussian filters, can be more easily realised.
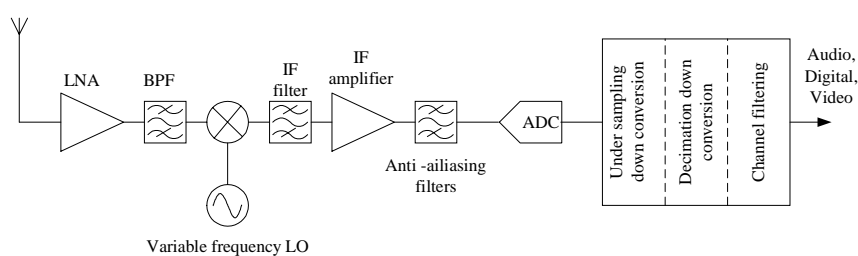

Figure 6 Triple conversion with the final 2 conversions done in DSP

It is possible do achieve some of the analog signal processing functions that are shown in Figure 5 using DSP. Figure 6 shows how this may be done. Whilst this circuit appears to only be a single conversion architecture, the "under sampling" and "decimation" processes are themselves down conversion processes. The decision on how far up the IF chain to take the DSP will involve the trade off of hardware complexity for higher speed ADC signal processing.

3.3 TRUST Approach

The major problems for the TRUST consortium to solve, given the receiver architecture chosen, are as follows:
  (a) Design a receiver of sufficient bandwidth to cover all the frequencies involved.
  (b) Design a receiver of sufficient linearity over a wide bandwidth, to handle blocking signals.
  (c) Cope with image signals either through flexible image filtering, or through improved image reject mixing

4. Design considerations with a software radio

Once the architecture has been chosen then the receiver has to be designed. This involves the bringing together of several important receiver parameters. Table 1 indicates the parameters that must be considered in the design process.

Receiver Specification	Influenced by:	Impact on receiver design
Input sensitivity	Air interface standard	Defines total gain of the receiver chain (amplifiers, filters, mixers duplexers)
Maximum input level	Air interface standard	Defines AGC range required for the receiver
Distortion performance	Blocker specifications	Defines TOI of the devices that make up the receiver
		Defines positioning and performance of filters within the receiver chain.
IF frequency	Preselect filter design	The higher the IF frequency the further apart are the wanted and image signals.
ADC resolution	Signal to noise ratio at the lowest signal level	Determines the resolution required of the ADC

Table 1 Design trade-offs in receiver design

4.1 Distortion performance

The blocker specifications will be an important factor in determining the allowed distortion performance of a receiver. The distortion performance is generally specified in terms of the Third Order Intercept (TOI). For example, a diagramatic representation the blocker specifications [13] of a GSM system is shown in Figure 7.
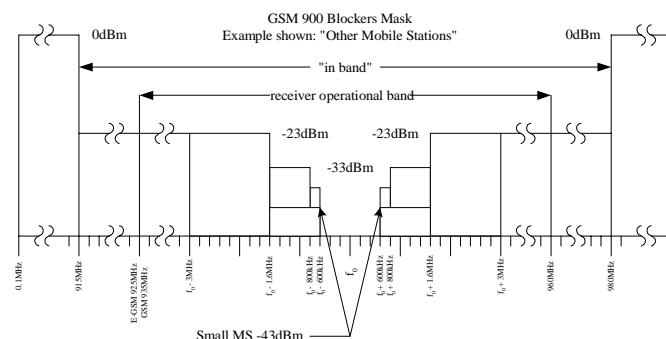

Figure 7 "Other Mobile Stations" blocker mask

If the receiver is left open to (say) the 5MHz channel of UMTS, then any blocker within ±2.5MHz of the centre frequency may introduce distortion products into the wanted GSM channel. It can be seen from Figure 7 that the blockers at these frequencies are allowed to be

up to –23dBm. GSM air interface standards specify a test signal of 3dB above the reference sensitivity level. This translates to –101dBm. The standards also specify a co-channel carrier to interference ratio of 9dB. This implies that the blockers should introduce a signal level of no greater than –110dBm into the wanted channel. The distortion product introduced by the –23dBm blockers is thus –110dBm, or 87dBm down on the blocker. Using a standard formula for calculating the required input TOI of the receiver, it can be shown that this is +20.5dBm. This is a huge input TOI. Some further comments on what this amounts to in terms of the receiver building blocks are given in reference [14].

5. Image signals

Image signals have been mentioned briefly in 3.1. Image signals are countered in conventional receiver via the use of fixed preselect filters. In a flexible receiver a fixed filter is not possible. Some electronic means of fine-tuning the preselect filter would provide flexibility, and lead to a more elegant solution to this design problem. This possibility will be investigated during the course of the TRUST project.

6. Additional considerations for the SDR application

6.1 Transparent Reconfigurability

The nature of the "Transparently Reconfigurable" objective of the TRUST project is that the radio is able to reconfigure without significant intervention of the user in that process. To support this, three communications processes are required to take place on a SDR. These are:
(a) Communication over the existing communication channel,
(b) Monitoring the environment to assess what services are available, and to see what software is available for down load,
(c) Facilitate software download preparatory, to switching to another standard.
These services may need to be set up on individual radio channels. Moreover, the user application may require simultaneous connections to different air interfaces. Whether this means separate transmitters and receivers will depend on how wideband and linear the TRUST receivers and transmitters can be made.

System aspects researched in TRUST, which will deliver these additional RF subsystem requirements, are discussed in [15]: consideration will be given to these requirements as they are developed.

6.2 Control of RF Parameters

Control of the RF subsystem is directed from the baseband controller. This system will reference a cache of RF system parameters. It is envisaged that the reconfiguration process will be managed by the baseband controller, specifying RF subsystem behaviour in terms of parameter values. A table of capabilities of the RF subsystem, indicating the valid ranges of parameters, is also likely to be required. These requirements are currently under development in TRUST, as discussed in companion papers [[2]and [15]]. It is expected that there will be some type of local RF controller to interface between the RF hardware and the baseband controller.

7. Conclusions

The design of a RF section for the physical layer of a SDR is a challenging task. Linearity over wide bandwidths is an issue with both the transmitter and receiver. Flexibility of filtering is a big issue with the receiver, and to a lesser extent with the transmitter. Operation of the

frequency synthesiser will be complex. An innovative approach using state of the art technology will be necessary, if an elegant RF system is to be designed.

8. Acknowledgement

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