Indonesian Journal of Electrical Engineering and Informatics (IJEEI)
Vol. 7, No. 3, Sep 2019, pp. 555~563
ISSN: 2089-3272, DOI: 10.11591/ijeei.v7i3.581

Analytical current Model for Dual Material Double Gate Junctionless Transistor

S.C.Wagaj [1], S.C.Patil [2]
[1,2] Dept. of Electronics & Telecommunication, JSPM's Rajarshi Shahu College of Engineering, Tathawade, Pune, Savitribai Phule Pune University, Pune, Maharashtra, India

Article Info

Article history:

Received Jul 13, 2018
Revised Sep 6, 2018
Accepted Apr 18, 2019

Keyword:

Dual Material Gate
Bulk Current
Junctionless
Silicon on Insulator
Semiconductor device modeling

ABSTRACT

A Transistor model with bulk current is proposed in this article for long channel dual material double gate junctionless transistor. The influence of different device parameters such as body thickness, channel length, oxide thickness, and the doping density on bulk current is investigated. The proposed model is validated and compared with simulated data using Cogenda TCAD. The model is designed by Poisson's equation and depletion approximation. Current driving capability of MOSFET is improved by dual material gate compare to single material gate.

Corresponding Author:

S.C. Wagaj,
Dept. of Electronics & Telecommunication, JSPM's Rajarshi Shahu College of Engineering,
Tathawade, Pune, Savitribai Phule Pune University, Pune, Maharashtra, India
Email: scwagaj@yahoo.com

1. INTRODUCTION

In 21st century, Silicon on Insulator was known as Integrated Circuit Technology. According to International Technological road map MOSFET channel length should reduce. Short channel effect has problems such as increase in subthreshold swing, decrease in Ion/Ioff ratio, drain induced barrier lowering, and transconductance etc. These short channel effect problems can be overcome by different types of transistors. At the time of formation of source and drain junction while using doping profile, thermal budget poses big challenge. However, junctionless transistor is best candidate for improving short channel effect problem because of very low thermal budget. This was reviewed in the literature [1] [2]. Junctionless transistor is more simple compared to inversion model MOSFET because of junctionless fabrication procedure. Double gate junctionless transistor is best candidate for CMOS technology. However, junctionless transistor suffers from less drain current and transconductance due to high doping concentration in the channel region [3]. The concept related to Dual material gate junctionless transistor is studied in literature [4] [5].

Dual material gate (DMG) junctionless transistor improves transconductance and carrier transport efficiency. Peak electric field at source side accelerates more electrons due to DMG structure due to which current driving capability increases. M.Jagdesh kumar and Anurag Chaudhari designed two dimensional analytical model for channel potential of DMG SOI Transistor in order to improve short channel effect problem [5][6]. Hougin Lou et. al demonstrated dual material gate junctionless nanowire transistor which showed significant improvement in transconductance, output conductance and cut off frequency in comparison with single material gate junctionless nanowire transistor [7]. Ratul K.Baruah designed analytical model for channel potential of dual material gate junctionless transistor by using high-k spacer. However, because of using high-k spacer cut-off frequency of this MOSFET reduced drastically [8]. Gnani et.al presented a design of analytical drain current model for junctionless ultra thin body silicon on insulator transistor and this model design was used under gradual channel approximations which neglected short channel effects [9]. In a work

of Duarte et.al, bulk current model was designed for long channel double gate junctionless transistor [10]. But, bulk current model for dual material double gate junctionless transistor was not found in literature. Vandana Kumari et.al demonstrated drain current model for dual material double gate junctionless transistor, but the model failed to mention the effect of channel thickness, gate oxide thickness, channel doping density and channel length on drain current [11]. In [12] current model of subthreshold region was not mentioned. Ekta Goel et.al demonstrated analytical model of threshold voltage for graded channel dual material double gate MOSFETs, but drain current model not found in this paper [12]. In junctionless transistor, current flows through bulk of channel region. Jaspreet Singh et.al demonstrates the surface potential model and drain current based on surface potential model [13]. However, channel thickness, oxide thickness and doping density affection on drain current is not found in this paper. Ashutosh Kumar et.al demonstrate surface potential model of a Dual material double gate junctionless FET, however, the drain current model is missing in this article [14]. Balraj Singh et.al demonstrate analytical drain current model in subthreshold region and affection of channel thickness, doping density, channel length on drain current of single material double gate junctionless transistor [15]. Objective of this paper is to demonstrate bulk current model and subthreshold current model of dual material double gate junctionless transistor that are not found in literature.

In this paper, a simple analytical expressions are used to describe bulk current for dual material double gate junctionless transistor in linear and subthreshold region. The model is validated by comparing simulation results of COGENDA TCAD using 2-D structure. Basic drift diffusion model, impact ionization model, Fermi Dirac statistic, band to band tunneling and low field mobility model are incorporated in this simulation software as shown in equation (1). μ_0 is low field mobility model.

$$\mu_0 = \mu_{\min} + \frac{\mu_{\max}\left(\frac{T}{300}\right)^{\nu} - \mu_{\min}}{1+\left(\frac{T}{300}\right)^{\xi}\left(\frac{N_{total}}{N_{ref}}\right)^{\alpha}} \quad (1)$$

Where, μ_{min} is 55.24 cm^2/v.s, μ_{max}=1429.23 cm^2/v.s, v=-2.3, ξ=-3.8, α=0.73, N_{ref}=1.072x10^{17} cm^{-3}. $N_{total} = N_A + N_D$ is total impurity concentration, T is lattice temperature.

Authors in [16] demonstrated Zener tunneling in semiconductor using this software. Only default parameter values of different models used for simulation. In the proposed model, the oxide thickness, channel length, doping density and channel thickness are varied to study addition effect of these on drain current.

2. BULK CURRENT MODEL

In Dual Material Double Gate Junctionless Transistor (DMDGJLT) MOSFET simulation, the following process/device parameters are used as in Table 1.

Table 1. Device parameters

Parameter	DMDGJLT
Channel length 1	0.05 µm
Channel length 2	0.05 µm
Oxide thickness (t_{ox})	5 nm
Channel Thickness (t_{si})	10 nm
Doping concentration (N_D)	1x10^{19} cm^{-3}
Channel width (W)	1 µm
Work function of Gate 1(N poly)	5.5eV
Work function of Gate 2 (P poly)	4.2eV
Supply voltage (V_D)	1V

An approximation method is used in the Model for dual material double gate junctionless transistor. Further to solve the Poisson's equation in the channel we followed accumulation mode transistor [17]. To determine the depletion width X_{dep} in the bulk current regime the following equations are given below.

$$X_{dep}\left(V_G, V(y)\right) = \left(\frac{\varepsilon_{si}}{C_{ox}}\right)\left[-1+\sqrt{1-\frac{2C_{ox}^2}{\varepsilon_{si}qN_{si}}\left(V_G - V_{FB1} - V(y)\right)}\right] \quad (2)$$

$$X_{dep}\left(V_G, V(y)\right) = \left(\frac{\varepsilon_{si}}{C_{ox}}\right)\left[-1+\sqrt{1-\frac{2C_{ox}^2}{\varepsilon_{si}qN_{si}}\left(V_G - V_{FB2} - V(y)\right)}\right] \quad (3)$$

ε_{si} is the permittivity of silicon, N_{si} is channel doping density. V_G is the gate voltage, V_{FB} is flat band voltage. $V(y)$ is channel potential at y in the channel. In expression $C_{ox}=\varepsilon_{ox}/t_{ox}$, ε_{ox} is oxide permittivity and

t_{ox} is gate oxide thickness. In Dual Material Double Gate Junctionless Transistor channel doping density is 10^{19} cm^{-3}. Therefore, DMDG JLT can be simplified by a Taylor series expansion for the threshold voltage point V_{TH} that can be found in (2) by setting $X_{dep} = t_{si}/2$ where t_{si} is channel thickness.

$$X_{dep}\left(V_G, V(y)\right) \cong -\frac{C_{eq}}{qN_{si}} \times \left(V_G - V_{FB1} - V(y)\right) + \left(\frac{t_{si}}{2}\right) \times \left(1 - \frac{\left(\frac{C_{OX}}{2} + C_{dep}\right)}{\left(C_{ox} + C_{dep}\right)}\right) \quad (4)$$

C_{dep} is half channel depletion capacitance, $C_{dep}=2\varepsilon_{si}/t_{si}$

$$X_{dep}\left(V_G, V(y)\right) \cong -\frac{C_{eq}}{qN_{si}} \times \left(V_G - V_{FB2} - V(y)\right) + \left(\frac{t_{si}}{2}\right) \times \left(1 - \frac{\left(\frac{C_{OX}}{2} + C_{dep}\right)}{\left(C_{ox} + C_{dep}\right)}\right) \quad (5)$$

C_{eq} is equivalent capacitance given by series connection C_{ox} and C_{dep}. In DMDG JLT channel thickness is very thin compared to oxide thickness. Therefore,

$$\frac{\left(\frac{C_{OX}}{2} + C_{dep}\right)}{\left(C_{ox} + C_{dep}\right)} \text{ tends to 1}$$

$C_{dep}= 2\ \varepsilon_{si}/t_{si}$, $C_{eq}= (C_{dep}\ C_{ox}) / (C_{dep} + C_{ox})$, $C_{ox}= \varepsilon_{ox}/t_{ox}$, finally X_{dep} is

$$X_{dep1}\left(V_G, V(y)\right) \cong -\left(\frac{C_{eq}}{qN_{si}}\right) \times \left(V_G - V_{FB1} - V(y)\right) \quad (6)$$

$$X_{dep2}\left(V_G, V(y)\right) \cong -\left(\frac{C_{eq}}{qN_{si}}\right) \times \left(V_G - V_{FB2} - V(y)\right) \quad (7)$$

The bulk current through the channel should satisfy ohm's law, dV=I.dR, where dR is differential channel resistance.

$$dR_1 = \frac{dy}{2W\mu_b qN_{si}\left(\frac{t_{si}}{2} - X_{dep1}\right)} \quad (8)$$

$$dR_2 = \frac{dy}{2W\mu_b qN_{si}\left(\frac{t_{si}}{2} - X_{dep2}\right)} \quad (9)$$

W is channel width, μ_b is bulk electron mobility, N_{si} is channel doping density, q is electron charge, t_{si} is channel thickness. Using graded channel approximation, ohm's law is integrated with dR_1 and dR_2 given by (6) and (7).

Bulk current under gate1:

$$I_{bulk1} = 2\mu_b qN_{si}\left(\frac{W}{L}\right) \times \left[\left(\frac{t_{si}}{2} + \frac{C_{eq}}{qN_{si}}\left(V_G - V_{FB1}\right)\right)V_{DS} - \frac{C_{eq}}{qN_{si}}\frac{V_{DS}^2}{2}\right] \quad (10)$$

Bulk current under gate2:

$$I_{bulk2} = 2\mu_b qN_{si}\left(\frac{W}{L}\right) \times \left[\left(\frac{t_{si}}{2} + \frac{C_{eq}}{qN_{si}}\left(V_G - V_{FB2}\right)\right)V_{DS} - \frac{C_{eq}}{qN_{si}}\frac{V_{DS}^2}{2}\right] \quad (11)$$

$$I_{bulk} = I_{bulk1} + I_{bulk2}$$

μ_b is electron mobility and W is width of channel and L is channel length, V_{FB1} and V_{FB2} is flat band voltage 1 and flat band voltage2, respectively. Threshold voltage equation is $V_{TH1}=V_G - V_{FB1}-(qN_{si}t_{si}/2C_{eq})$ and $V_{TH2}=V_G-V_{FB2}-(qN_{si}t_{si}/2C_{eq})$. Work function of silicon channel is W_{si}=4.05+(0.56-(0.026*log(N_d/N_i))).When V_{DS} is equal to $V_{GS}-V_{TH}$ then MOSFET is in saturation state. When more drain voltage is applied then pinch-off point move towards source side. In saturation region drain to source voltage square term is negligible. Flat band voltage is different for L_1 and L_2, hence workfunction is different under gate1 and gate2.

Channel potential distribution in the channel is solved using one dimensional Poisson equation [18].

$$\phi(x) = \frac{-qN_{si}}{\varepsilon_{si}}\frac{x^2}{2} + \frac{qN_{si}}{\varepsilon_{si}}\frac{t_{si}}{2}x + \phi_s \quad (12)$$

$\phi(x)$ is potential at silicon silicon interface, ϕ_s is surface potential, t_{si} is channel thickness, ε_{si} is dielectric constant of silicon. N_{si} is doping density of channel.
The area of electon concentration near the source is

$$N(0) = N_{si}\int_0^{ti} \exp\left(\frac{\phi(x)}{V_T}\right)dx \quad (13)$$

Electron concentration is an exponential function of $\phi(x)$, the electron concentration contributes mainly $N(0)$ at x_{min}. The position x_{min} at which a potential is minimum.

$$\left.\frac{d\phi(x)}{dx}\right|_{x=x_{\min}} = 0 \quad (14)$$

We find that $x_{min}=t_{si}/2$. Substituting $x_{min}=t_{si}/2$ into (11) results in:

$$\phi_{\min} = \frac{1}{8}\frac{qN_{si}}{\varepsilon_{si}}t_{si}^2 + \phi_s \quad (15)$$

$$\phi(x) = \frac{-qN_{si}}{2\varepsilon_{si}}\left(x - \frac{t_{si}}{2}\right)^2 + \frac{1}{8}\frac{qN_{si}}{\varepsilon_{si}}t_{si}^2 + \phi_s \quad (16)$$

Subtracting (5) into (6), we have

$$\phi(x) - \phi_{\min} = \frac{-qN_{si}}{2\varepsilon_{si}}\left(x - \frac{t_{si}}{2}\right)^2 \quad (17)$$

Assuming that the change in potential corresponding to conductive channel is

$$\phi_t = \phi(x) - \phi_{min}$$

$$(x - x_{min})^2 = \phi_t / a$$

$$a = -qN_{si}/2\varepsilon_{si}$$

in (13), developing exponential term in taylor series at ϕ_{min} and taking first order term

$$n_1 = \frac{4}{3}N_{si}\frac{t_{si}}{2}\exp\left(\frac{\phi_{\min}}{V_T}\right) \quad (18)$$

$$n_2 = \frac{4}{3}N_{si}\frac{t_{si}}{2}\exp\left(\frac{\phi_{\min}}{V_T}\right) \quad (19)$$

n_1 is electron concentration under gate1 and n_2 electron concentration under gate2. When the channel is fully depleted, ϕ_s can be obtained as

$$\phi_s = V_G - V_{FB1} + \frac{qN_{si}t_{si}}{2C_{ox}}$$

Thus the subthreshold current due to gate1

$$I_1 = qd_n\frac{W}{L_1}n_1\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \quad (20)$$

Subthreshold current due to gate2

$$I_2 = qd_n\frac{W}{L_2}n_2\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \quad (21)$$

d_n is diffusion coefficient $d_n=\mu_n$ x (KT/q), $(KT/q=0.026\text{V})$. $V_T=KT/q$ is thermal voltage. W is width of channel and its value is 1µm. Channel length of gate1 is L_1 and gate2 is L_2.

3. MODEL VERIFICATION AND DISCUSSION

COGENDA Visual 2-D TCAD simulation is used for verification of this model. Energy balance equation, Lombardi mobility model, drift diffusion model for lattice temperature model and impact ionization

model are incorporate in this COGENDA Visual 2-D TCAD simulation. Channel length of gate1 is 50nm and gate2 is 50nm. Dual material double gate junctionless is symmetric MOSFET. Work function of gate1 (N^+poly) is kept 5.5eV and gate2 (P^+poly) is 4.2eV. Channel uniform doping density is $1x10^{19}$ cm^{-3} and oxide thickness is 7nm, channel length 100nm, channel thickness 10nm, V_{DS}=0.05V. Source and drain 10nm was kept small in order to reduce parasitic effect.

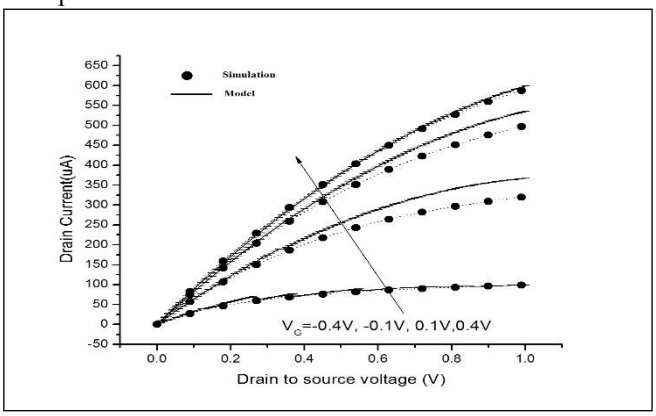

Figure 1. Drain current versus drain to source voltage for different gate voltage.

Figure 1 shows that drain current versus drain to source voltage changes from -0.4V, -0.1V, 0.1V and 0.4V and V_{DS} varies from 0 to 1V. Here, parameters are, channel length 0.1µm, t_{ox}=7nm, channel thickness 10nm and doping density $1x10^{19}$ per cm^{-3}. As shown in above graph, model calculation (line) match (agrees) with numerical simulation (symbols) for different gate voltages. As like conventional MOSFET, V_{DS} is equal or greater than V_{GS}-V_{TH} in such a case (then) MOSFET works as saturation region. In this diagram, it is observed that current saturates due to velocity saturation of shorter channel length. Because of dual material gate, current driving capability of MOSFET increases in comparison with single material gate MOSFET [7][19]. When gate voltage is 0.4V, and V_{DS}=1V then current is $5.9x10^{-4}$A. When current increases then transconductance of MOSFET increases and this benefit for analog circuit.

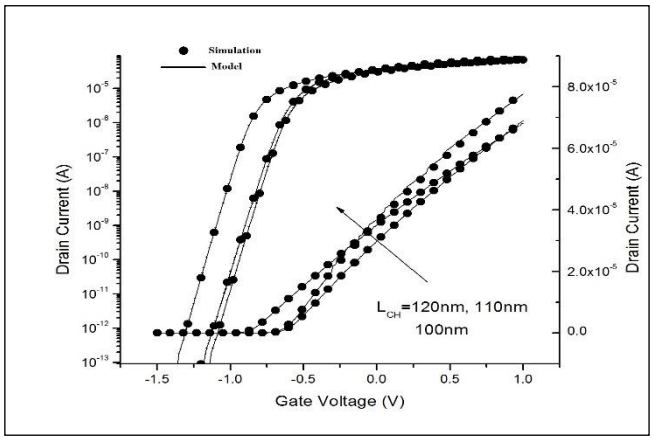

Figure 2. Drain current versus Gate voltage for different channel length for V_{DS}=0.05V

Figure 2 shows that drain current versus gate voltage for different channel length. When channel length increases threshold voltage of MOSFET decreases. It has been observed that off state current decreases when channel length increases. Off state current is 10^{-8}A, 10^{-11}A and 10^{-11}A at channel length 100nm, 110nm and 120nm respectively at V_{GS}=-1V. In junctionless transistor more barrier between source and channel at channel length increases, hence off current decreases. It has been observed that subthreshold slope (SS=dV_G/d(log(I_D)) remains constant for all channel length shown in Table 2. It means that short channel effect problem also improved due to dual material gate junctionless transistor. It is observed that there is a good correlation between simulation and model result.

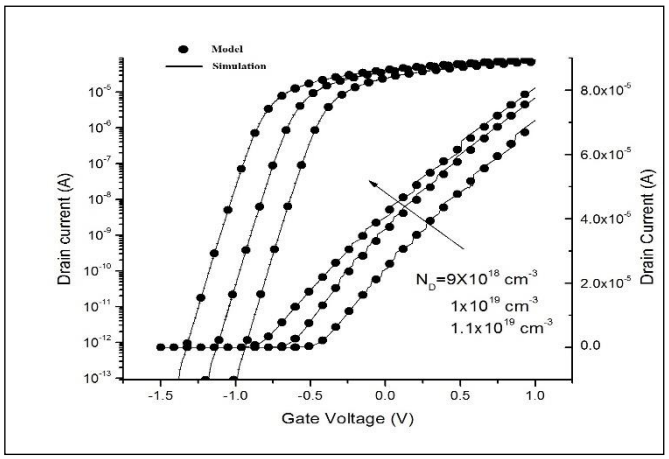

Figure 3. Drain current versus Gate voltage for different doping density of channel region at V_{DS}=0.05V .

Figure 3 shows that drain current versus gate voltage for different doping density. When doping density decreases then threshold voltage of MOSFET increases and current driving capability increases due to carrier mobilty increase as well as due to reduction of ionization scattering in the channel [20]. It is observed that less doping density is used then off current decreases. It has been observed that current driving capability increases when doping density increases which means less ionization scattering effect on mobility and already very less surface roughness mobility degradation in junctionless transistor because of current flowing through bulk. When channel is lightley doped, number of carriers availability for conduction is very less and hence channel is completely depleted and higher voltage required to diminish the depletion for current conduction. Finally it observed that there is a good corelation between model and simulation.

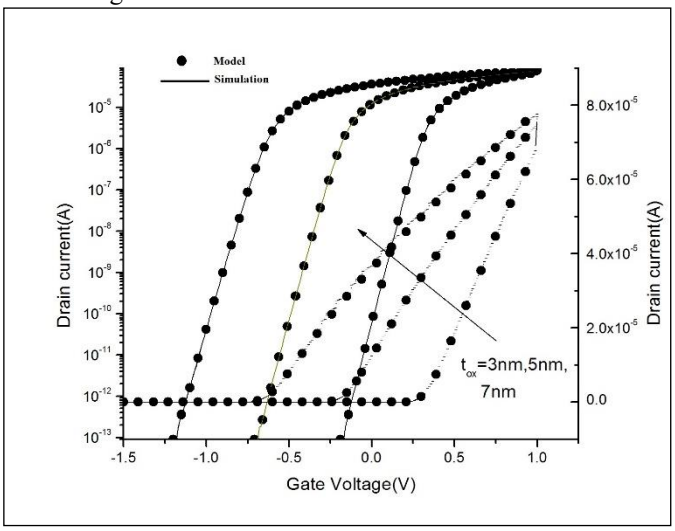

Figure 4. Drain current versus Gate voltage for different oxide thickness at V_{DS}=0.05V

Figure 4 shows that drain current versus gate volatge. Threshold voltage of MOSFET decreases when thickness of sio_2 layer increases. Dual material double gate junctionless transistor improves the performance when subthrehold slope decreases, DIBL value decreases and I_{ON}/I_{OFF} ratio increaes. Effect of oxide thickness variation on threshold voltage is maximum in comparison with channel thickness and doping density. When V_{GS} is 0V and when t_{ox}=3nm then MOSFET is easily in the off state when compared to 7 and 5nm oxide thickness MOSFET. It has been observed that when gate oxide thickness increases then it has less effect of gate voltage on depletion width of channel. Smaller oxide thickness means bigger gate capacitance that is more capable of depleting the channel and producing small OFF current.

Figure 5 shows that variation of drain current versus gate voltage for different channel thickness. When channel thickness increases then threshold voltage decreases. Subthreshold slope ($SS=dV_G/d(\log(I_D))$ is 90 mV/decade for channel thickness 6nm and 80 mV/decade when channel thickness is 8 and 10nm. In camparison silicon film thickness 6nm, the silicon film thickness 10nm will enhanced ON current by approximately 2 orders of magnitude. On the other hand decreases channel thickness increases the resistance,

which significantly lower the maximum current. Table 3 shows different SS value at different t_{si} when t_{ox}=3nm, N_D=9x10^{18} cm^{-3},L=100nm and SS value at different t_{ox} when t_{si}=10nm, N_D=9x10^{18} cm^{-3} and L=100nm.

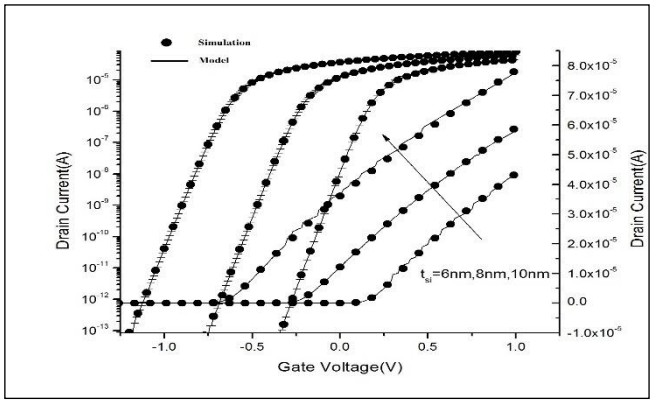

Figure 5. Drain current variation versus gate voltage for different channel thickness at V_{DS}=0.05V.

Table 2. DMG DG JLT different concentration parameters and subthreshold slope (S.S.)

N_D (cm^{-3})	S.S. (mV/decade)	Channel length (nm)	S.S. (mV/decade)
9x10^{18}	80	100	100
1x10^{19}	100	110	100
1.1x10^{19}	60	120	100

Table 3. DMG DG JLT different thickness parameters and subthreshold slope (S.S.)

t_{si} (nm)	S.S. (mV/decade)	t_{ox} (nm)	S.S. (mV/decade)
6	90	3	80
8	80	5	70
10	100	7	100

If Channel thickness and gate oxide of DMDGJLT decreases then subthreshold slope decreases which means that off current decreases. It has been observed that gate oxide thickness of junctionless transistor increases then control of gate on channel decreases. No full depletion in channel when maximum gate oxide thickness of junctionless transistor, which is off current increase. Table 2 shows that SS value at different doping density at t_{si}=10nm, t_{ox}=3nm, L=100nm and SS value at different channel length at t_{si}=10nm, t_{ox}=3nm and N_D=9x10^{18} cm^{-3}.

Moreover, DIBL value for gate oxide thickness 3nm and another parameter remains constant, while DIBL=V_{TH}(V_{DS}=0.05V) – V_{TH}(V_{DS}=1V) = 30mV/V. The threshold voltage is determined at this current (10^{-7} x (W/L)). Channel length of MOSFET increases then DIBL decreases. It has been observed that DIBL value is improve at gate oxide thickness is 3nm and SS value is 60 mV/decade at doping density 1.1x10^{19} cm^{-3}. Table 4 shows that DIBL value at different oxide thicknes at t_{si}=10nm, N_D=9x10^{18} cm^{-3}, L=100nm and DIBL value at different channel length at t_{si}=10nm, t_{ox}=3nm and N_D=9x10^{18} cm^{-3}.

Table 4. DMG DG JLT different parameters and drain induced barrier lowering (D.I.B.L)

Parametr (nm)	t_{ox}	D.I.B.L. (mV/V)	Parameter Channel length(nm)	D.I.B.L. (mV/V)
3		30	100	90
5		40	110	80
7		90	120	70

Table 5. Comparison proposed device values with different researchers.

Sr.No	Parameters	Values by different researchers	Proposed device value
1	On current(μA)	60 Juan p.Duarte et al [10]	600
2	Off current(μA)	0.01 Juan P.Duarte et.al[10]	0.000001
3	DIBL (mV)	33 Vandana kumari et.al [11]	30
4	Subthreshold slope (mV/decade)	62 Vandana Kumari et.al [11]	60

Table 5 shows that comparison of proposed device values with different researchers proposed MOSFETs at t_{ox}=7nm, t_{si}=10nm, N_D=1x10^{19} cm^{-3} and L=1000nm. It has been observed that on current of proposed device is maximum and off current is minimum (1pA at channel length 120nm) which means that I_{on}/I_{off} ratio improves compares to single material double gate junctionless transistor. Subthreshold slope of our device is minimum compare to [11] dual material double gate junctionless transistor. Threshold voltage of my proposed device and other researcher's device mentined in references is approximately same [21] [22].

4. CONCLUSION

In this paper, we have proposed, model of bulk current for long channel Dual Material Double gate junctionless MOSFET from Poisson equation in the channel using a depletion approximation and has been verified by simulation result of cogenda visual TCAD. Model is valid in all regions, sub-threshold, linear and saturation. In this paper we observe that MOSFET channel thickness, oxide thickness; channel doping and channel length affect on drain current and threshold voltage of MOSFET. It has been observed that current driving capability of MOSFET is improved due to Dual material gate. Therefore this device is a better candidate for operating in the three regions.

REFERENCES

[1]. C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, "Junctionless multigate field-effect transistor," *Applied Physics Letters*, vol. 94, no. 5, pp. 053511-1–053511-2, Feb. 2009.

[2]. C.W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, *et al.*, "Performance estimation of junctionless multigate transistors, *Solid State Electron.*, vol. 54, no. 2, pp. 97–103, Feb. 2010.

[3]. J.P.Colinge, Chi Woo Lee, Isabelle Ferain, and Yan R,"Reduced electric field in junctionless transistors", *Applied Physics Letters,*vol 96, pp. 073510, 2010.

[4]. Long, Hou, J.M. Kuo, and K. K. Chin, "Dual material gate (DMG) field effect transistor," *IEEE Transaction on Electron Devices*, vol. 46.No.5, pp. 865-870, 1999.

[5]. M. J. Kumar and A. Chaudhry, "Two-dimensional analytical modeling of fully depleted DMG SOI MOSFET and evidence for diminished SCEs," *IEEE Trans. Electron Devices*, vol. 51, no. 4, pp. 569–574, Apr. 2004.

[6]. J.P. Colinge, C.W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, *et al.*, "Nanowire transistors without junctions," *Nat. Nanotechnology.*, vol. 5, no. 3, pp. 225–229, Mar. 2010.

[7]. Haijun Lou, Lining Zhang,Yunxi Zhu,"A Junctionless Nanowire Transistor with a Dual Material Gate", *IEEE Transaction on Electron Devices* Vol 59,No 7,pp. 1829-1836, July 2012.

[8]. Ratul Baruah and R. P. Paily,"A Dual-Material Gate Junctionless Transistor with High-K Spacer for Enhanced Analog Performance",*IEEE Transaction on Electron Devices*,Vol 61, No 1 Jan-2014.

[9]. Elena Gnani, Antonlo Gnudi, Susanna Reggiani, "Theory of the Junctionless Nanowire FET", *IEEE Transactions on Electron Devices*, Vol. 58,No. 9, pp.2903-2910,Sep-2011.

[10]. J. P. Duarte, Sung-Jin Choi, Dong-II Moon,"Simple Analytical Bulk Current Model for Long-Channel Double-Gate Junctionless Transistors", *IEEE Electron Device Letters*, Vol.32,No 6, pp.704-706, June.2011.

[11]. Vandana Kumari, Neel Modi, Manoj Saxena,"Theoretical Investigation of Dual Material Junctionless Double Gate Transistor for Analog and Digital Performance,"*IEEE Transaction on Electron Devices*, Vol 62,No 7,pp.2098-2105, July.2015.

[12]. Ekta goel, Sanjay Kumar,"2-D Analytical modeling of Threshold voltage for Graded-channel Dual Material Double-Gate MOSFETs", *IEEE Transaction on Electron Devices,* vol.63, No.3, pp.966-973, March-2016.

[13]. Jaspreet Singh, Vijit Gadi, "Modeling a Dual-material-Gate Junctionless FET Under Full and Partial Depletion Conditions Using finite-Differentiation Method", *IEEE Transaction on Electron Device*, Vol.63, No.6, pp.2282-2287, June-2016.

[14]. A. Kumar Agarwal and P.N.V.R. Koutilya,"A Pseudo 2-D surface potential model of a dual material double gate junctionless field effect transistor", *Journal of Computational Electronics*, Vol.14, pp.686-693,Jun 2015.

[15]. Balraj singh and Deepti Gola," Analytical modeling of subthreshold characteristics of ion-implanted symmetric double gate junctionless field effect transistors", *Materials Science in Semiconductor Processing*, Vol.58, pp.82-88, 2017.

[16]. E.O. Kane, "Zener tunneling in semiconductors," *J. Phys. Chem. Solids*, vol 12, p. 181–188, 1959.

[17]. J.P.Colinge,"Conduction Mechanisms in Thin-Film Accumlation Mode SOI P-channel MOSFET's", *IEEE Transaction on Electron Devices*, Vol 37, No 3, pp.718-723, March. 1990.

[18]. Zhang Zhengfan, Li Zhaoji, Tan Kaizhou, "Investigation into Sub-threshold Performance of Double-Gate Accumlation Mode SOI MOSFET", in Proc.7th International Conference on ASICs, Guilin.pp.1150-1153,2007.

[19]. Ping Wang,Yigi Zhuang, Cong Li,"subthreshold behavior models for nanoscale junctionless double-gate MOSFETs with dual-material gate stack", *Japanese journal of Applied Physics,* vol 53, 084201, 2014.

[20]. Zhuojun Chen,Yongguang Xian,Minghua Tang," Surface potential-based Drain Current Model for long-channel Junctionless Double-Gate MOSFETs", *IEEE Transactions on Electron Devices*, Vol.59, No.12, pp.3292-3298, Dec-2012.

[21]. M. A. Riyadi, I. D. Sukawati, and Teguh Prakoso. "Influence of Gate Material and Process on Junctionless FET Subthreshold Performance." *International Journal of Electrical & Computer Engineering*, vol 6 no. 2, p. 895-900, 2016.
[22]. Jung, Hakkee. "Central Electric Field and Threshold Voltage in Accumulation Mode Junctionless Cylindrical Gate MOSFET." *International Journal of Electrical & Computer Engineering*, vol.8 no 2 ,p.673~679, 2018.

BIOGRAPHY OF AUTHORS

S.C. Wagaj received the B.E.and M.E. degrees in Electronics Engineering from Shivaji University Kolhapur, Maharashtra, India, in 1999 and 2006 respectively. He is currently pursuing the Ph.D. with Modeling and simulation of junction-less transistor for low power and high performance in the JSPM‟s RajarshiShahu college of Engineering Pune research center of SavitribaiPhule Pune University, Pune.
He is currently working as Assistant Professor at JSPM‟s RajarshiShahu college of Engineering Pune.His research interests includes Modeling and Simulation of novel device structures on SOI Junction-less MOSFETs. He is a life member of Indian Society for Technical Education New Delhi India. He published five papers in International Journal and four papers in International Conference. He published one Indian patent on shielded channel junctionless Transistor in Jan 2016

Dr. Shailaja Patil is professor at the Department of Electronics and Telecommunication of RSCOE, affiliated to Savitribai Phule Pune University, Pune. She received Ph.D. in Computer Engineering from SVNIT, SURAT. She has total 25 years of research and teaching experience in the field of Wireless Technologies, Internet of Things and Pervasive computing. She has authored many research articles in International conference and journal, Book chapters, Patent, and Book. She has worked as session chair/ reviewer/ for various national/ international conferences. She is a member of professional bodies such as ISTE, IEEE and ACM.