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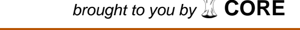
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Analysis of Solid State Relay Solutions Based on Different Semiconductor Technologies

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Acknowledgements

This work was partly funded by the Spanish Ministry of Economy Industry and Competitiveness (Research Contracts SMARTCELLS no. TEC2014-51903-R, Ramon y Cajal no. RYC-2010-07434 and PCIN-2014-057) and by AGAUR funds (2014-SGR 1596).

Keywords

«Industrial application», «Induction heating», «Power semiconductor device», «Device application», «Device characterisation».

Abstract

This paper provides an analysis on the design, implementation and operation of Bi-Directional Switches (BDS) based on power semiconductor devices intended to replace Electro Mechanical Relays (EMR) in home appliances. Static and dynamic characterizations of test vehicles developed using different power device semiconductor technologies (TRIAC, Super Junction (SJ) MOSFET, IGBT…) are presented. At this time, emerging Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) seem to be very suitable for the mentioned applications. Actually, GaN HEMTs based BDS has demonstrated to be the best solution to replace EMRs, with a high expectation to a significant cost reduction.

Introduction

EMRs are the cheapest solution for commutating power sub-circuit blocks and have been in use up to now for implementing BDS in industrial electronics applications [1]. However, they present a set of disadvantages (e.g., slow response, presence of moving parts, acoustic noise, high input power consumption, short life, presence of electric arcs during commutation, large size and weight) which intend to be removed by a semiconductor devices based design.

This work focuses on implementing a Single-Pole, Single-Throw (SPST) BDS, which can be operated in two states: blocking state, where its two terminals are disconnected one from each other (high impedance state), and conduction state, where they are both connected together (low impedance state). Furthermore, the BDS has to be capable of blocking voltage between its terminals in both directions while opened, and allowing a bidirectional current flow while closed (AC applications). The most commonly used Single-Pole, Double-Throw (SPDT) function can be considered as an extension of the SPST case and all the results derived from our study can be extended to the SPDT relay.

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The presented BDSs aim to be used in home appliances, such as induction cookers for inductors multiplexing [1], main power supply connection switches, etc. This framework implies rated voltages and current levels of 600-1200 V and 20-70 A for the power devices involved in the study. Fast switching capability is not a main requirement but the BDS must convey high frequency AC currents (tens of kHz), involving relatively high *dV/dt* and *dI/dt* values (in the range of 500 V/µs and 6700 A/ms respectively). The main characteristic demanded to the analyzed BDSs was as low as possible conduction losses.

There exist a wide range of possible implementations for the BDS function based on semiconductor devices, which are conditioned by their individual characteristics. The most relevant implementations are depicted in Table I. The TRIAC [2] solution is in fact the only single device capable of implementing a BDS by itself.

Another possibility consists in a solution based on two RB-IGBTs [4]-[7]. As the RB-IGBTs provide bidirectional voltage blocking and unidirectional current conduction capabilities, two of these devices are arranged in anti-parallel for implementing the BDS function [7] [8].

Furthermore, IGBT+Diode (in Co-Pack package) [9], normally-on Silicon Carbide (SiC) JFETs [10], SJ MOSFETs [11] and normally-off GaN HEMTs [10] [12] provide bidirectional current conduction and unidirectional voltage blocking capabilities, so an anti-series arrangement of two of these devices is required for implementing the BDS function [8] [13]-[15].

Table I: Implemented BDS Solutions Classification

Device	Device characteristics	BDS implementation symbol	BDS function
One power device			
TRIAC	Bidirectional voltage blocking and bidirectional current conduction		One device only
Multiple power devices			
RB-IGBTs	Bidirectional voltage blocking and unidirectional current conduction		Anti-parallel arrangement of two devices
IGBT+Diode SiC JFETs SJ MOSFETs GaN HEMTs	Unidirectional voltage blocking and bidirectional current conduction		Anti-series arrangement of two devices

This paper starts describing the implementations of the different analyzed BDS into test vehicles. These test vehicles have been implemented using the most performing power devices commercially available in the voltage and current ranges of interest, focusing on the 600 V – 40 A rated values. Then, their static and dynamic characterization results are depicted in the following sections. Finally, a discussion of those results is presented in the last section, together with the conclusions of this work.

BDS Implementation

The BDS solutions based on power semiconductor devices introduced in the previous section have been implemented in test vehicles. As it is depicted in the block diagram of Fig. 1, all these test vehicles have two main inputs: an external power supply (V_{AC}) and an input control signal (V_{IN} = 0 V / 5 V); while their outputs are the two power terminals. The implementation of these test vehicles is determined by the driving requirements of each power device: switching characteristics

 ISBN: 9789075815276 et CFP17850-ART
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(voltage/current control and levels, parasitic capacitances), operation modes (normally-on or normally-off), number of required power devices and the way they are arranged in the BDS, etc. Therefore, a specific driving circuitry is designed for each solution. One or more floating voltage power supplies are used for biasing an opto-coupled gate-driver (at levels V_{EE} and/or V_{CC}) which isolates the input signal V_{IN} from the power stage, resulting into a gate control signal (V_{CON}) for enabling (bidirectional current conduction, I_{BDS}) or disabling (bidirectional voltage blocking, V_{BDS}) the power stage devices. In addition, each test vehicle has been provided with overvoltage protection devices between gate-source and drain-source terminals. As the objective of the present work was to analyze all the possible solutions based on different semiconductor technologies, in a first step the study of the thermal dissipation issues was postponed for a second phase. For this reason, any heat-sink or dissipation system is observed in Fig. 2. This approach allowed the development and electrical characterization of up to 6 test vehicles, and the selection of the most promising solutions to be fully developed in future works.

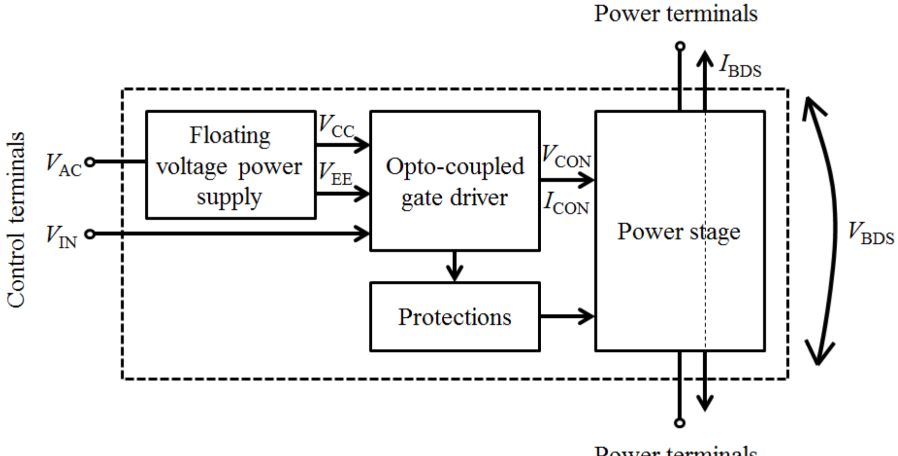

Fig. 1: Block diagram of the test vehicles.

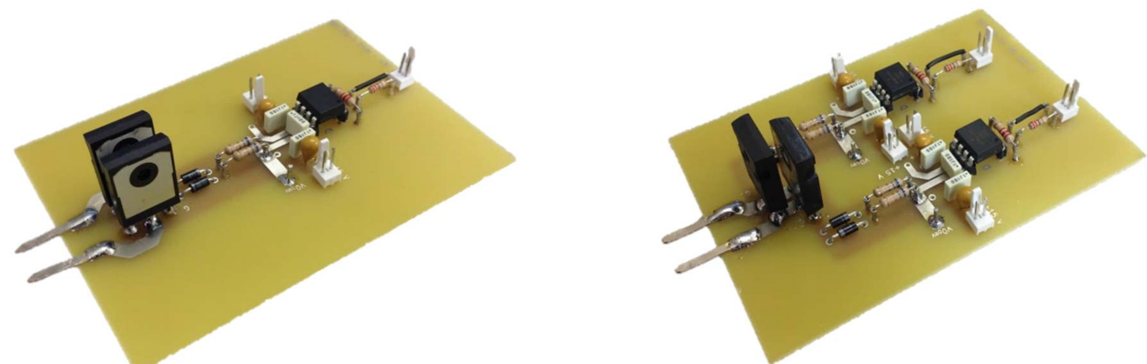

Fig. 2: Test vehicles for implementing a BDS from IGBT+Diode (co-pack) and RB-IGBTs.

The TRIAC based BDS requires just one single-chip device and one opto-DIAC gate driver, thereby presenting the best integration characteristics, the lowest control complexity and costs.

The implementations based on IGBTs, and MOSFETs present a good ease of control as their driving voltages make them compatible with standard IGBT/MOSFET gate drivers including an opto-coupler at the input. However, a common source configuration is not possible for the RB-IGBT BDS, and it requires two separate drivers and four power sources (as it can be derived from the picture in Fig. 2) for implementing the V_{CC} and V_{EE} voltages (see Fig. 1), with a consequently higher control complexity and costs. In addition, together with IGBT+Diode based BDS, they present lower integration characteristics as four individual chips are involved.

Regarding the GaN HEMTs and SiC JFETs based BDSs, due to the unavailability of reasonably priced commercial gate opto-drivers for their specific driving voltages, these solutions require separated

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opto-couplers for providing galvanic isolation, together with specific gate drivers for managing their individual driving voltages: V_{CON} = 7 V / -2 V for GaN HEMTs, V_{CON} = 2 V / -15 V for SiC JFETs, with an increased control complexity and costs. Furthermore, both implementations result in very robust solutions, as conduction in the third quadrant (SCRC or Self Commutated Reverse Capability) provides natural "freewheel paths" in case that both transistors do not commutate simultaneously. However, thanks to their lateral structure, GaN HEMTs provide additional integration capabilities since a monolithical integration of the BDS power stage is possible as it has already been presented in many publications [16]-[19]. In addition, GaN has an extra advantage compared with SiC as a result of the enhanced mobility of electrons, which translates into a device with a smaller size for a given R_{on} and breakdown voltage (BV). Despite the rest of the considered devices, the selected SiC JFETs are normally-on switches. Therefore, two different versions of the same BDS have been implemented for evaluating the BDS performance when using a non-inverted opto-coupler and the one for enabling a normally-off control of the BDS. In addition, together with SJ MOSFETs BDS, SiC JFETs BDS integration characteristics are in the grey area between GaN HEMTs BDS or TRIACs and IGBTs based BDS, as only two individual chips are required.

In order to study the electrical behavior of the different test vehicles, static and dynamic analysis have been performed.

Static Characterization

The static analysis includes the extraction of the static I-V curves of the analyzed BDS test vehicles in forward and blocking modes using a curve tracer. From these results, their on-state resistance (R_{on}), on-state voltage drop (V_{BDS}) and conduction losses are extracted.

Fig. 3 shows the static test results and highlights V_{BDS} @ I_{BDS} = 25 A (and at the corresponding gate driving I_{CON} or V_{CON} depending on the involved power devices). Blue curves are representative of BDSs voltage blocking capability (breakdown voltage ($V_{(BR)BDS}$)). Alternatively, black curves are representative of BDSs current conduction capability. Static analyses demonstrate that all the studied solutions are capable of implementing the BDS function. Those based on bipolar devices show an off-set voltage in their I-V curves which translates in slight distortions of the AC currents/voltages flowing through the BDS in the zero-crossing region, while SiC JFETs, SJ MOSFETs and GaN HEMTs BDS have no off-set voltage and experience symmetrical switching. However, this fact does not represent a serious problem in practical applications but increases the conduction power losses.

The best performance in terms of the conduction power losses is achieved by the implementations based on TRIACs and SJ MOSFETs. However, it is noted that as GaN HEMTs are an emerging technology, for the moment when the static tests were performed a brand new device with almost 3 times lower R_{on} was still not available. A BDS implementation based on these new devices would lower V_{BDS} @ I_{BDS} = 25 A close to TRIACs. It is worth to point out that in the framework of the studied applications, conduction losses are predominant as the BDSs are used at very low switching or commutation frequencies. Concerning the SiC JFETs it is also relevant to consider that the devices analyzed in this work are rated for 1200 V BV. Consequently, the availability of 600 V devices (not commercially accessible) could improve significantly their figures of merit for the BDS application.

All analyzed devices (except the TRIAC) show positive forward voltage drop coefficient with temperature for practical current levels, meaning that the current scalability of the BDS solutions is possible by parallel interconnection of devices. In this sense, an additional benefit of the unipolar devices is that as they do not show an off-set voltage, their paralleling allows a significant reduction of the conduction power losses.

Finally, it is worth to mention that as GaN HEMTs do not show avalanche capability, their BV process is destructive and higher security margin is required compared with the other devices. Accordingly, drain-source overvoltage protection is provided by placing a transient voltage suppressor (TVS) between the BDS power terminals.

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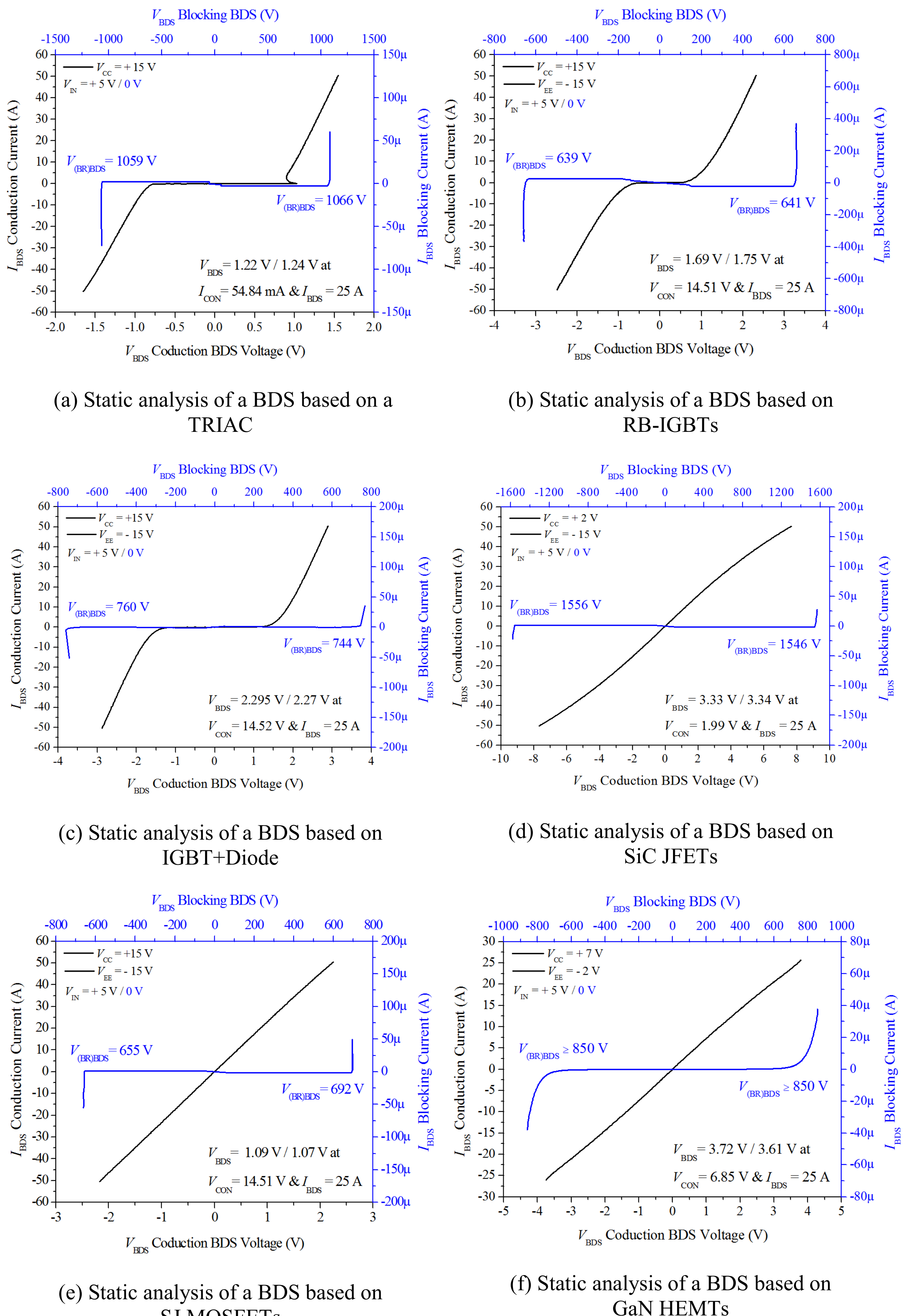

(a) Static analysis of a BDS based on a TRIAC

(b) Static analysis of a BDS based on RB-IGBTs

(c) Static analysis of a BDS based on IGBT+Diode

(d) Static analysis of a BDS based on SiC JFETs

(e) Static analysis of a BDS based on SJ MOSFETs

(f) Static analysis of a BDS based on GaN HEMTs

Fig. 3: Static I-V characteristics obtained for the six analyzed BDS solutions.

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Dynamic Characterization

A specific test platform, based on a full-bridge converter topology, was designed for performing the dynamic analysis. It applies for zero crossing current analysis of the proposed BDSs and aims to easily identify any malfunction on a wide range of *dV/dt* and/or *dI/dt* across the BDS under test. The following experimental results are collected using the aforementioned test vehicles.

In these tests, first a triangular AC current flows through the BDSs (15 A current peak, *dI/dt* = 6765 A/ms) and is then switched to blocking state (300 V, *dV/dt* = 520 V/µs). These *dV/dt* and *dI/dt* values are typically found in induction cooking applications. Green waveforms in Fig. 4 represent V_{CON}, black waveforms are the voltage drop between terminals of the BDS, V_{BDS}, and blue waveforms are the current through the switch, I_{BDS}.

In general, for a functional BDS we expect the following behavior: at the blocking instant, I_{BDS} stops flowing through the BDS after a few parasitic oscillations, while the BDS starts to withstand a bidirectional voltage. The mentioned oscillations are caused by the parasitic RLC elements of the circuit with a different contribution for each device, caused from the diverse variation of their non-linear parasitic capacitances. The amplitude of those oscillations is related to the devices output capacitance, while their frequency is conditioned by the devices BV.

Most solutions pass the dynamic tests with special mention to GaN HEMT and SiC JFET based BDSs. As it can be observed, the TRIAC is not capable of switching off because of highly exceeding its maximum rated *dI/dt* for the specified value in the studied application. Furthermore, the selected opto-DIAC gate driver introduces large delays at the beginning of the test (Fig. 4 (a)), which can be easily fixed by using a standard IGBT driver and correctly dimensioning the gate resistance of the TRIAC for voltage controlling the device.

SiC JFETs present good dynamic characteristics but high conduction power losses. However, extending this analysis to lower BV devices (< 1.2 kV), which are still not available for the moment, will improve the performance of this solution.

Perhaps one of the most relevant results of our study concerns the SJ MOSFET devices that showed very promising static characteristics. As it can be observed in Fig. 4, once the SJ MOSFET test vehicle is switched from conduction to blocking state, it experiences several problems: first, at a blocking voltage of 150 V it appears an abnormal voltage peak, close to the device nominal BV. In addition, once switched-off, a significant current peak flows through the devices. This issue seems to be related with the devices internal structure, but a complete explanation about this abnormal behaviour is not completely undertaken. From this analysis it is concluded that SJ technology shows controllability problems for the present application.

Finally, GaN HEMTs have been confirmed to be a promising solution to replace EMRs in a medium term from their excellent dynamic behavior.

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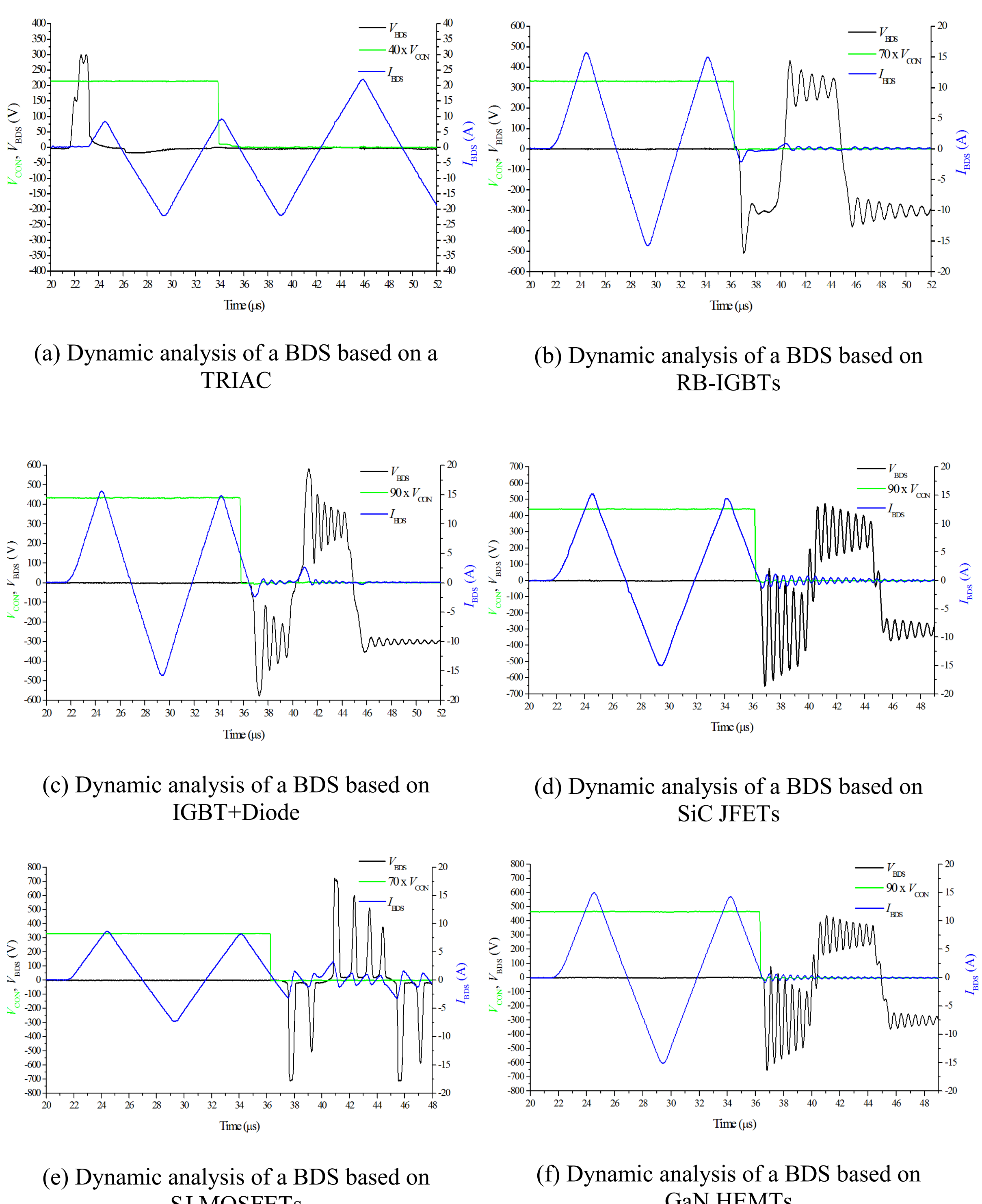

(a) Dynamic analysis of a BDS based on a TRIAC

(b) Dynamic analysis of a BDS based on RB-IGBTs

(c) Dynamic analysis of a BDS based on IGBT+Diode

(d) Dynamic analysis of a BDS based on SiC JFETs

(e) Dynamic analysis of a BDS based on SJ MOSFETs

(f) Dynamic analysis of a BDS based on GaN HEMTs

Fig. 4: Dynamic conduction to blocking state test results.

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Conclusion

This work reveals that alternatives to the EMR based on semiconductor devices are possible in home appliances applications, involving high frequency currents and voltages. The studied solutions provide the required I-V static characteristics for implementing the BDS function. However, a significant disparity exists between the best and the worst performance in terms of their control complexity, power losses, costs, etc. TRIAC and SJ MOSFETs appeared initially as very promising since they provided superior static characteristics, performing the lowest conduction voltage drops of all studied implementations. However, as a consequence of their anomalous behaviors (maximum rated *dI/dt* exceeded for the TRIAC and abnormal current peaks for the SJ MOSFET) both technologies have to be discarded for the studied application. Regarding the IGBT based solutions, IGBT+Diode BDS is robust and cost-effective, but together with RB-IGBTs present relatively high power losses due to the off-set voltage. SiC JFET based BDS presents excellent dynamic characteristics regardless the additional opto-driver implementation difficulties, but relatively high conduction power losses, in part due to the lack of commercial devices in the 600 V voltage range. Moreover, these SiC devices have a less expected costs drop in the short term than for GaN HEMTs. Finally, from their superior static and dynamic characteristics and the additional integration improvements from the possibility of implementing the BDS monolithically (lateral device), GaN HEMTs have been revealed as the best solution to replace EMRs in the mid-term. Only their thermal management seems to be critical and will be analyzed in future works.

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