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LDMOS versus GaN RF Power Amplifier Comparison Based on the Computing Complexity Needed to Linearize the Output

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Abstract: In order to maximize the efficiency of telecommunications equipment, it is necessary that the radio frequency (RF) power amplifier is situated as closely as possible to its compression point. This makes its response nonlinear, and therefore it is necessary to linearize it, in order to minimize the interference that nonlinearities cause outside the useful band (adjacent channel). The system used for this linearization occupies a high percentage of the hardware and software resources of the telecommunication equipment, so it is interesting to minimize its complexity in order to make it as simple as possible. This paper analyzes the differences between the laterally diffused MOSFET (LDMOS) and gallium nitride (GaN) power amplifiers, in terms of their nonlinearity graphs, and in terms of the greater or lesser difficulty of linearization. A correct choice of power amplifier will allow for minimization of the linearization system, greatly simplifying the complexity of the final design.

Keywords: linearization; power amplifier; predistortion; LDMOS; GaN

1. Introduction

In order to increase efficiency and to meet the telecommunications standards, many different techniques [1] have been proposed and employed to extend the linear range of the power amplifier (PA) response in radiofrequency (RF) communications: crest factor reduction (CFR), feedback linearization, feedforward linearization, predistortion techniques, envelope elimination and restoration (EER), linear amplification using nonlinear components (LINC), and combined Analog Locked Loop Universal Modulator (CALLUM).

The most commonly used linearization systems are those that use predistortion techniques to linearize the power amplifier (Figure 1).

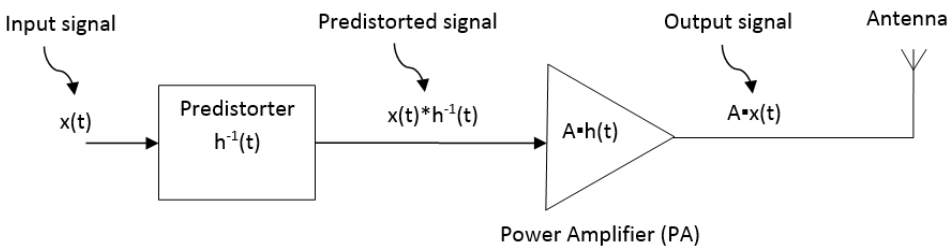

Figure 1. Basis of Predistortion Techniques.

The objective of the predistorter is to correct the nonlinearity that is introduced by the amplifier by distorting the input signal *x(t)* to be amplified, so that the PA output presents a behavior that is proportional to the input signal *x(t)* (Figure 1), minimizing the nonlinear distortion and hence improving the corresponding adjacent channel power (ACP). The ACP is the part of the frequency spectrum of the signal generated in our channel that interferes with the adjacent frequency channels [1]. The reduction of the ACP allows for transmissions at higher RF power levels using the same amplifier, therefore increasing its efficiency.

Many techniques have been developed to implement the predistorter: Volterra series [2], Memory Polynomials [3], Wiener and Hammerstein models [4], Lookup Tables (LUTs) [5], Neural Networks [6], Neural–Fuzzy systems [7], Genetic Algorithms [8], etc.

A lot of engineers face every day the problem of having to linearize a power amplifier, employing a limited number of computational resources, and discovering that not all of the amplifiers can be linearized using the same techniques. The aim of this work is to show how to simplify the design of the linearization system by means of the correct choice of power amplifier. It will be shown that the variation of the output power versus the input power must be deeply analyzed before the amplifier selection. This will decrease the number of computational resources required to linearize the system and to meet the telecommunication standards.

This paper is structured as follows. Section 2 presents the materials and methods that were used in the elaboration of this work. Section 3.1 describes how a predistorter works. Section 3.2 shows a comparison between laterally diffused MOSFET (LDMOS) and gallium nitride (GaN) power amplifiers. Section 3.3 presents a comparison of the required hardware and software resources to implement predistorters for LDMOS and GaN power amplifiers. Section 3.4 shows the obtained results of linearizing an LDMOS and a GaN amplifier using a Multilayer Perceptron Neural Network Digital Predistorter (DPD). Finally, Section 4 presents the conclusions of this work.

2. Materials and Methods

The following power amplifiers were considered in this paper:

- PD57006S-E: an LDMOS amplifier manufactured by ST Microelectronics, with the following characteristics:
  - Output power: 5 W
  - Power supply: 28 V
  - Gain: 14.8 dB
  - Efficiency: 50%
- NPTB00004A: a GaN amplifier manufactured by MACOM, with the following characteristics:
  - Output power: 6 W
  - Power supply: 28 V
  - Gain: 15 dB
  - Efficiency: 62%

The OMAP-L138, manufactured by Texas Instruments, was used to implement the predistortion techniques. It is a low-power DSP (Digital Signal Processor) + ARM (Advanced RISC Machine) processor capable of working at a clock frequency of 456 MHz.

The neural networks that we used in this paper were trained using the Matlab Neural Network Toolkit.

TETRA was selected as the telecommunication standard to modulate the input signal of the power amplifiers. TETRA is a 25 KHz bandwidth digital standard designed for professional radio communications.

3. Results

3.1. Predistortion Technique

Figure 2 shows the typical Gain (G) and Efficiency (η) curves for an LDMOS power amplifier (model PD57006S-E manufactured by ST Microelectronics).

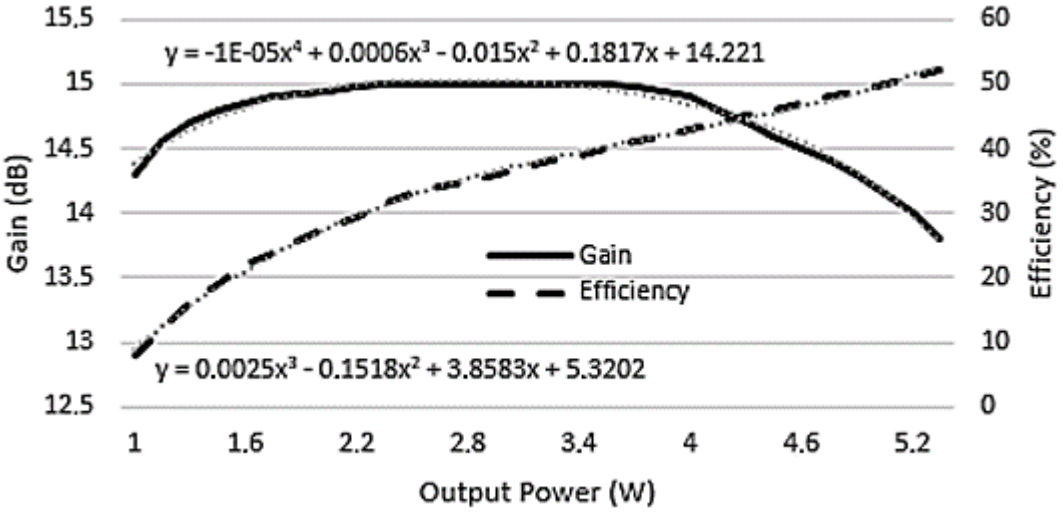

Figure 2. Measured characteristics of a LDMOS power amplifier (PA) (model PD57006S-E, ST Microelectronics) and the polynomial approximations.

As Figure 2 shows, as the output power increases, the efficiency of the amplifier also increases, up to a maximum value from which the gain begins to fall. The power output compression point (P1dB) is the output power that generates a gain compression of 1 dB in the amplifier. As the output power of the amplifier approaches the P1dB, the amplifier enters into the nonlinear operation region, distorting the output signal. Since the device must be as efficient as possible, the PA is configured to work near the P1dB of the amplifier, and therefore it will be necessary to apply a linearization technique in order to minimize the nonlinear distortion.

One of these linearization techniques is predistortion. As can be seen in Figure 1, the predistorter module modifies the input signal of the PA in order to pre-correct its nonlinearity. For this, the predistorter operation should be as similar as possible to the inverse function of the PA transfer function. There are different techniques to estimate the PA transfer function (Figure 3), and one of the most commonly used is the Memory Polynomial method.

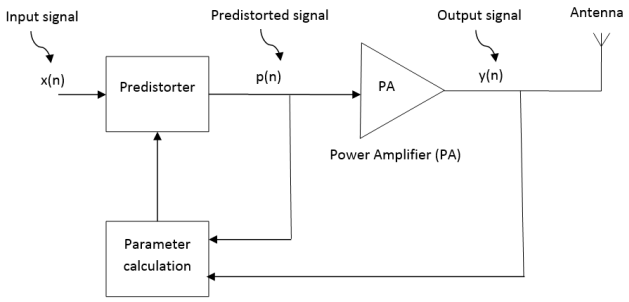

Figure 3. Generic predistortion scheme.

The Memory Polynomial model consists of:

$$y(n) = \sum_{k=0}^{K-1} \sum_{m=0}^{M-1} a_{km} p(n-m) \left| p(n-m) \right|^k \quad (1)$$

where K is the order of the polynomial model and M is the memory depth.

When the signal bandwidth is wide (hundreds of kHz), the memory effect of the PA becomes relevant, requiring it to be taken into account. Otherwise, when the signal bandwidth is narrow (<100 kHz), the memory effect is negligible (M = 1) and therefore (1) can be reduced to:

$$y(n) = \sum_{k=0}^{K-1} a_k p(n) \left| p(n) \right|^k. \quad (2)$$

Thus, the transfer function of the PA is modeled as a polynomial, and its inverse function is used as the transfer function of the predistorter module.

The feedback path in Figure 3 provides memory compensation (if necessary) and allows for a continuous compensation loop against changes in the PA transfer function due to temperature, frequency, or power supply variations.

This predistortion technique requires the transfer function to be recalculated periodically, adding complexity to the design, due to the required hardware and software resources. Therefore, reducing the degree of the polynomial model of the PA becomes mandatory to minimize the used resources to obtain the transfer function, for which correct selection of the PA will be pivotal, as will be seen in the next sections.

3.2. LDMOS versus GaN Power Amplifiers

Until the appearance of GaN amplifiers (around 2005), LDMOS amplifiers had dominated the market of high-power RF transmissions at frequencies below 2 GHz due to their low cost. The only competitors were the gallium arsenide (GaAs) amplifiers that allowed for higher frequencies, but at low power-transmission levels and with higher cost.

Currently, although the improvements in LDMOS amplifier characteristics allow for frequency ranges up to 22 GHz, GaN-based amplifiers [9] achieve frequencies up to 30 GHz at power densities up to five times higher, although at higher prices than LDMOS devices. Figure 4 shows the LDMOS and GaN transistor structures.

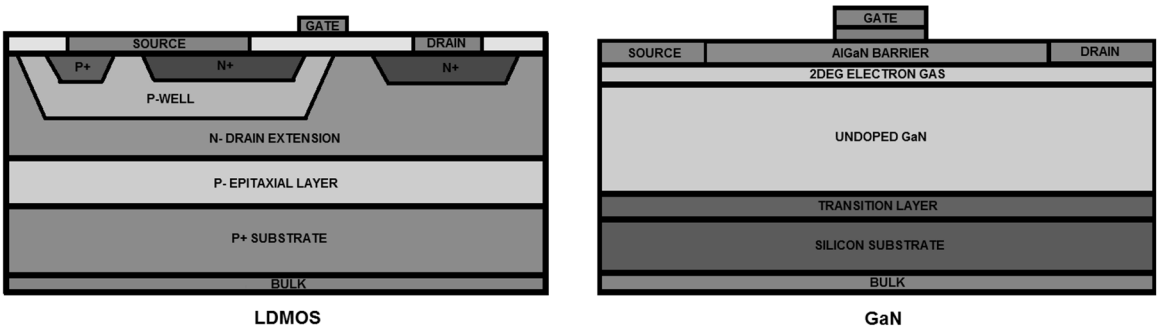

Figure 4. LDMOS and gallium nitride (GaN) transistor structures.

The main advantage of GaN is its higher power density. This is due to a band gap between the conduction and valence bands (Figure 5) that is higher than in LDMOS technologies, which provides both high breakdown voltages and power densities.

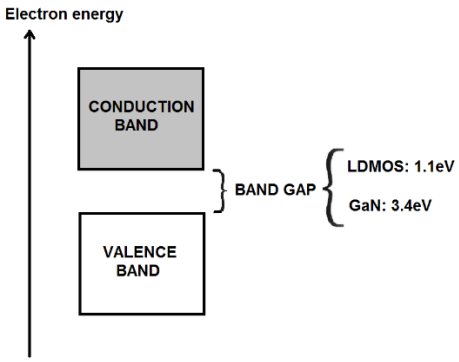

Figure 5. Band gap for LDMOS and GaN.

A comparison between LDMOS and GaN technologies is shown in Table 1.

Table 1. Comparison between LDMOS and GaN technologies.

	LDMOS	GaN
Maximum frequency	22 GHz	30 GHz
Power density	2 W/mm	10 W/mm
Efficiency at P1dB	60%	70%
Bandwidth	500 MHz	2500 MHz
Maximum temperature	Lower	Higher
Breakdown voltage	Lower	Higher
Maximum operating voltage	Lower	Higher
Cgs	Higher	Lower
Cds	Higher	Lower
Rin	Lower	Higher
Rout	Lower	Higher
Maximum RF power	1.5 kW	1 kW
Price	Lower	Higher
Robustness against impedance mismatches	Higher (65:1)	Lower (20:1)

Higher power density allows for GaN power amplifiers to operate at higher temperatures, therefore simplifying heat-sink and cooling requirements.

The lower input capacitance (gate-source capacitance, Cgs) of GaN power amplifiers results in lower amplitude modulation to phase modulation (AM-PM) distortion values [10] than LDMOS. This, together with a lower output capacitance (drain-source capacitance, Cds) and the higher input and output resistances (Rin and Rout), makes input and output impedances for the GaN power amplifiers higher, therefore allowing for simpler and lower loss circuits and wide bandwidth matching networks. Currently, this makes the GaN PAs more widely used than the LDMOS devices for broadband applications.

Nevertheless, LDMOS transistors are still more widely used than GaN PAs in some specific applications, such as wireless infrastructures, low-power battery-operated transceivers, small cells, and some microwave links, mainly because LDMOS devices can use plastic packaging—significantly reducing their cost. In addition, LDMOS transistors are more robust against impedance mismatching, which makes them preferable in the aforementioned application fields.

If we analyze the typical characteristics of a GaN PA, model NPTB00004A manufactured by MACOM (Figure 6), we observe that it has a smoother transition into the saturated region than a LDMOS PA (Figure 2).

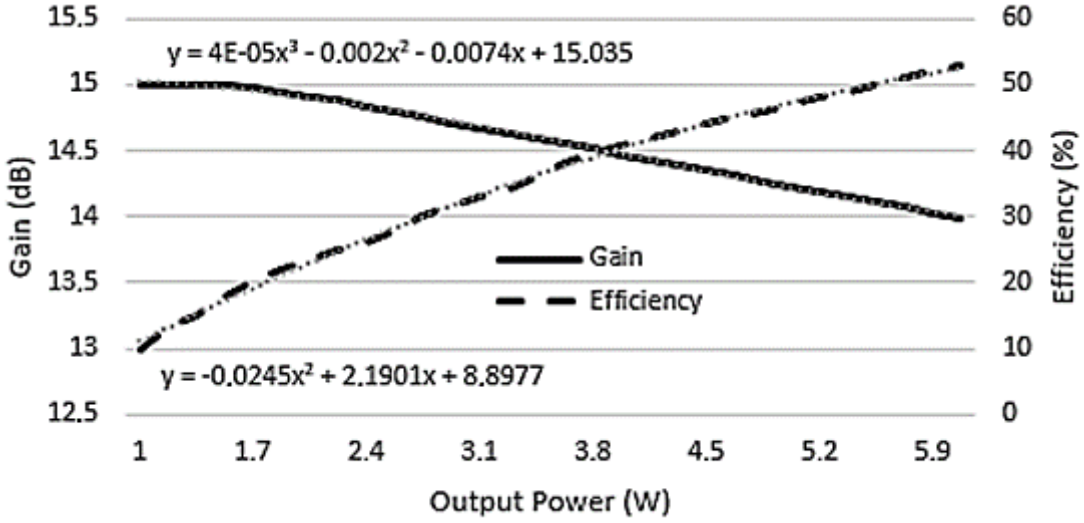

Figure 6. Measured characteristics of a GaN PA (model NPTB00004A, MACOM) and the polynomial approximations.

As will be seen in Section 3.3, this smoother transition can be critical in order to determine the linearization system complexity.

Since there are not generic equations for the Gain and for the Efficiency of LDMOS and GaN transistors, we can approximate these equations for the transistor models selected in this paper (Table 2).

Table 2. Approximated equations for the selected LDMOS and GaN transistors. Gain is expressed in dB, Efficiency is expressed in percentage, and Pout (Output Power) is expressed in Watts.

LDMOS (PD57006S-E)	GaN (NPTB00004A)
$Gain = -0.00001P_{out}^4 + 0.0006P_{out}^3 - 0.015P_{out}^2 + 0.1817P_{out} + 14.221$	$Gain = 0.00004P_{out}^3 - 0.002P_{out}^2 - 0.0074P_{out} + 15.035$
$Efficiency = 0.0025P_{out}^3 - 0.1518P_{out}^2 + 3.8583P_{out} + 5.3202$	$Efficiency = -0.0245P_{out}^2 + 2.1901P_{out} + 8.8977$

3.3. Complexity Analysis of the Linearization System (LDMOS vs. GaN)

In order to compare the linearization complexity of GaN and LDMOS power amplifiers [11], we can draw their output power versus input power. Figures 7 and 8 show the experimental input–output transfer functions and polynomial approximations for LDMOS and GaN, respectively, for different polynomial orders.

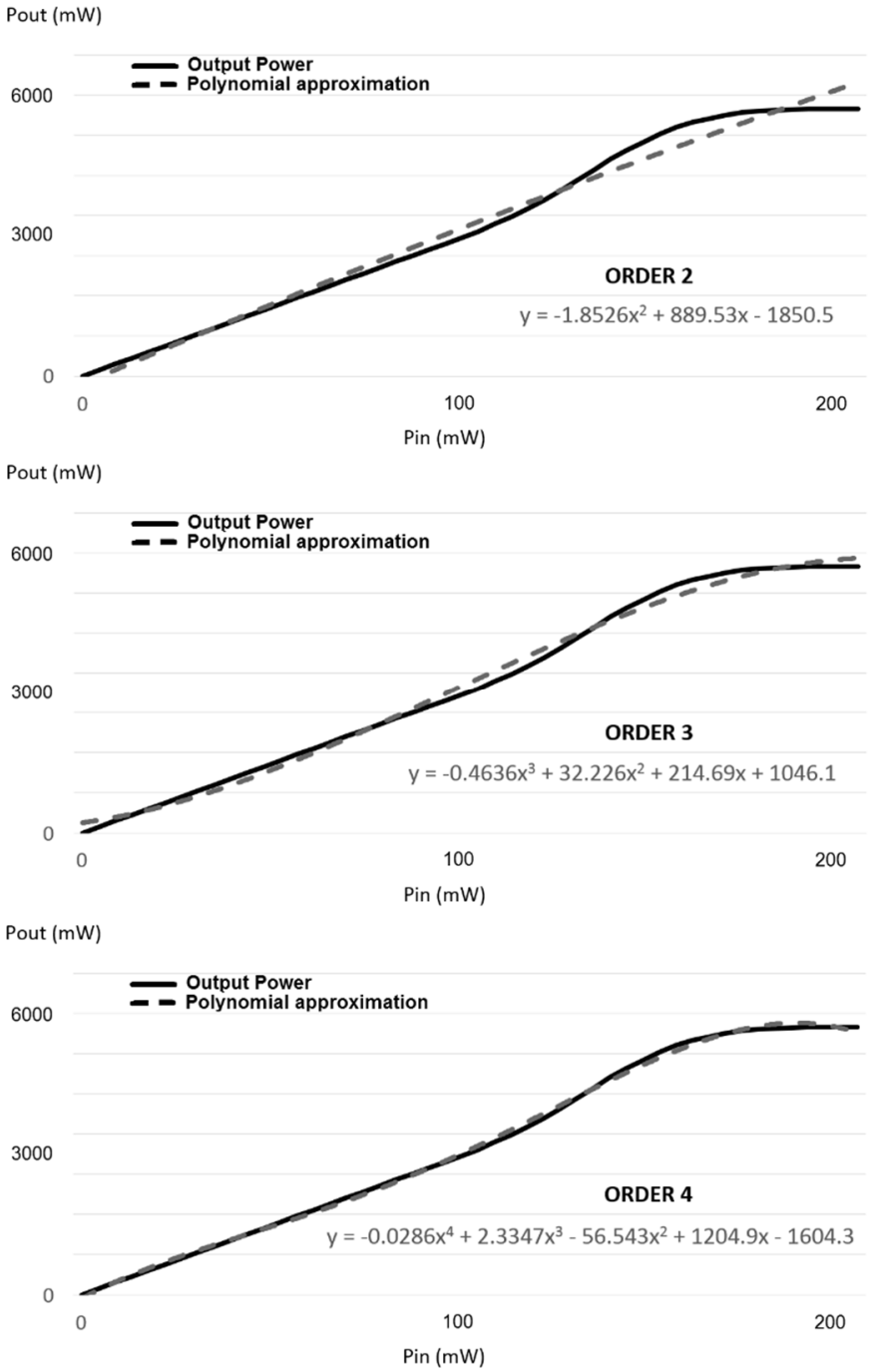

Figure 7. Output power versus input power for an LDMOS PD57006S-E amplifier (continuous line) and the polynomial approximation (dash line) when the polynomial order is changed (top: order 2, middle: order 3, bottom: order 4).

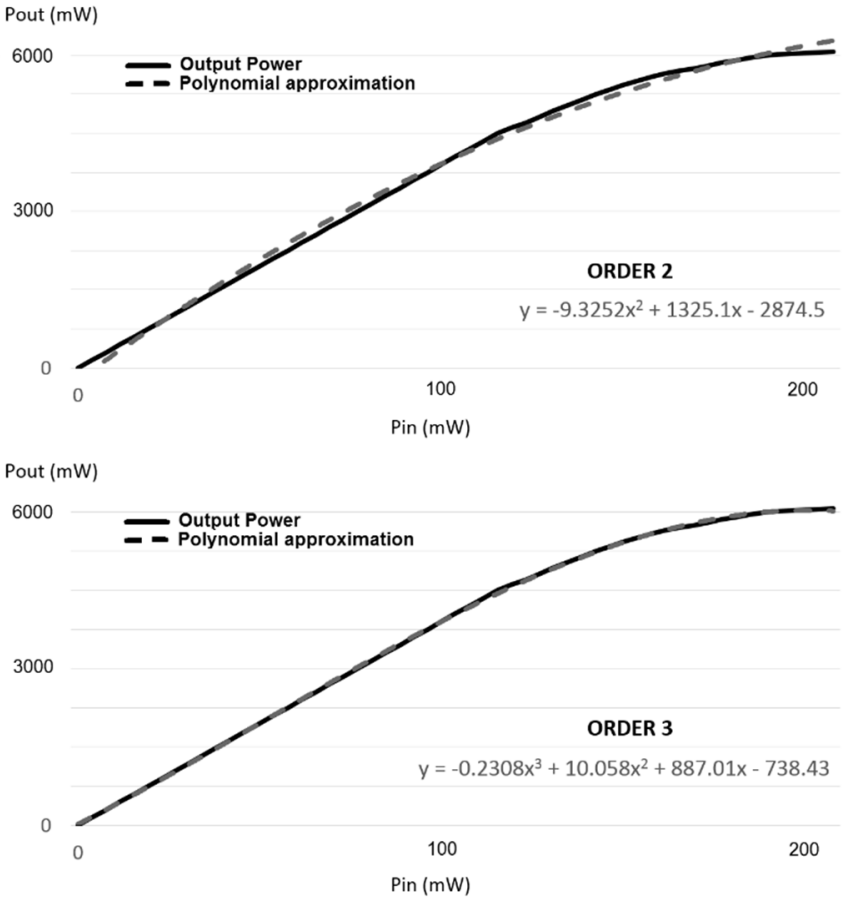

Figure 8. Output power versus input power for a GaN NPTB00004A amplifier (continuous line) and the polynomial approximation (dash line) when the polynomial order is changed (top: order 2, bottom: order 3).

As can be seen in Figure 8, a third-order polynomial is enough to model GaN PAs with an error level below 0.1%, while a fourth-order polynomial is required for LDMOS amplifiers (Figure 7), achieving an error of 0.6%. Therefore, it can be assumed that GaN amplifiers will require a lower number of coefficients and computing resources to implement a predistortion linearization technique than LDMOS devices will.

This higher complexity needed to linearize the LDMOS amplifiers is due mainly to the hump the LDMOS characteristically presents before the power output saturation (Figure 2), compared to the GaN PA's smoother shape. This difference can be also observed when comparing Figures 2 and 6.

Furthermore, the GaN PA's smoother behavior near the transition into saturation means that GaN amplifiers can operate closer to the saturated region, where efficiency is higher and distortion slowly increases as the device approaches saturation. This allows GaN amplifiers to operate nearer to the P1dB point.

3.4. Power Amplifier Complexity Comparison

A comparison of the complexity required in the linearization of the output power between LDMOS and GaN PAs was carried out by analyzing the resources necessary to meet the standard TETRA specifications [12]. For this, a multilayer perceptron (MLP) neural network DPD was selected as predistorter technique. This technique has previously shown its advantages compared to classical predistortion techniques [13]. The MLP DPD distorts the PA input signal, providing a correction to the amplifier output nonlinearities (Figure 9), thus improving the ACP of the output signal.

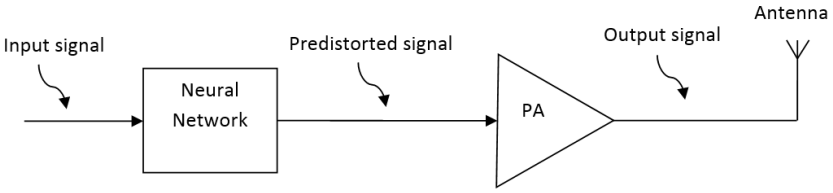

Figure 9. Digital predistorter (DPD) technique using a neural network.

The MLP consists of nonlinear output processors arranged in layers, whose interconnections are reinforced or weakened through a training process to attain a configuration that achieves the suitable nonlinearity compensation.

To perform the comparison, two PAs with similar features were selected for their linearization: a MACOM NPTB00004A (GaN technology) and an ST PD57006S-E (LDMOS technology).

An MLP consisting of one hidden layer with 20 processors using the hyperbolic tangent output function was trained to provide the predistortion values required to extend the linear range of the power amplifier output [13]. The single processors in input and output layers both provide linear transfer functions. Neural network training is performed using the Levenberg–Marquardt algorithm [14]. The neural network configuration can be seen in Figure 10. The results can be seen in Table 3, where a TETRA signal has been used as input signal, and the output power of both amplifiers has been obtained, increasing the input power to obtain at the output a power 1.5 dB less than the P1dB.

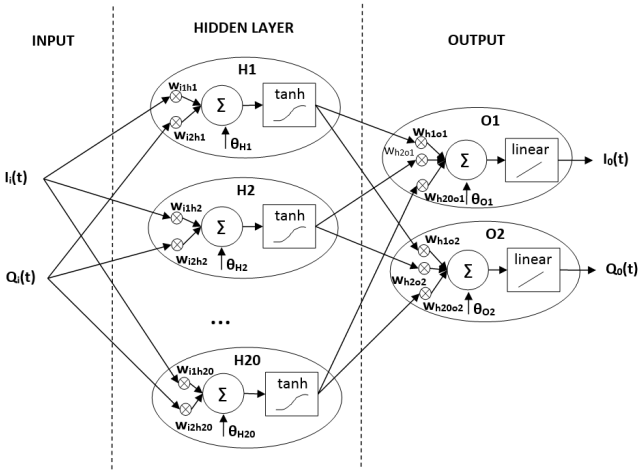

Figure 10. Neural network configuration.

Table 3. Adjacent channel power (ACP) improvement using a 20 neuron neural network.

	NTPB00004A	PD57006S-E
Output 1dB compression point (P1dB)	36.5 dBm	37.5 dBm
Output Power @ 925 MHz	35 dBm	36 dBm
Efficiency @ Output Power	50%	40%
ACP improvement	12 dB	10.5 dB

According to the results shown in Table 3, the proposed MLP architecture does not sufficiently improve the linear behavior of the LDMOS PA output power. So, the number of processors in the hidden layer should be increased to achieve the required ACP improvement, similar to that of the GaN amplifier. The corresponding results are shown in Table 4. As can be seen, a single hidden-layer neural network is not capable of achieving a suitable linearization for an LDMOS PA. Therefore, an additional hidden layer is defined in the MLP structure to obtain the expected ACP improvement. (Table 5).

Table 4. ACP improvement when varying the number of neurons of the neural network in the selected LDMOS amplifier.

Number of Neurons	ACP Improvement
20	10.5 dB
30	11 dB
40 or more	11.2 dB

Table 5. Neural network structures required to obtain the same ACP improvement for the selected LDMOS and GaN amplifiers.

	Neurons in 1st Hidden Layer	Neurons in 2nd Hidden Layer	ACP Improvement
NTPB00004A	20	-	12 dB
PD57006S-E	18	6	12 dB

The increment in the number of hidden layers and processors drastically increases the complexity of the solution, which can be compared to the increase in the order of the polynomial model previously shown in Section 3.3.

Predistorting the input signal using the MLP-based technique adds a time delay in the signal output. In the case of the selected GaN, the proposed architecture using 20 neurons in a single hidden layer running in an L138 OMAP (Open Multimedia Applications Platform) at a clock frequency of 456 MHz supposes a delay in the output signal of 15 ms (6500 clock cycles). In the case of the selected LDMOS, for the proposed architecture using 18 neurons in the first hidden layer and six neurons in the second hidden layer, the number of clock cycles required to calculate the neural network output under the same aforementioned conditions is 8500, corresponding to a time delay of 20 ms. Therefore, we could conclude that to achieve a similar timing delay, in the case of the LDMOS PA the DSP frequency should be increased to over 610 MHz. Table 6 shows these results.

Table 6. Required resources to linearize with a neural network.

	GaN	LDMOS
Number of cycles to linearize with the neural network	6500	8500
Necessary DSP frequency to linearize in 15 ms	456 MHz	608 MHz

4. Discussion

This paper shows the need to select the technology of the amplifier in order to correctly linearize its output through the available resources. We will have to evaluate whether the available resources are capable of linearizing the power amplifier, taking into account that a GaN amplifier is easier to linearize than an LDMOS amplifier, due basically to the smoother transition into saturation of the GaN amplifiers.

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