DC-Gain Measurement of the Frequency-to-Output Power Transfer Function based on sidebands for Domestic Induction Heating Applications

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Keywords

 \ll Induction heating \gg , \ll Resonant converter \gg , \ll Signal processing \gg , \ll Digital control \gg , Home appliances, Frequency-to-power transfer function, Power control.

Abstract

This paper analyzes different alternatives to obtain the dc gain of the frequency-to-output power transfer function of a series half-bridge resonant inverter for domestic induction heating. In this application, a full-wave rectified bus voltage usually feeds the inverter, and a constant switching frequency is applied during each half-period of the mains voltage. This dc gain is the derivative of the output power with respect to the frequency. A finite difference approximation to the derivative can be obtained measuring the output power during two consecutive half-periods of the mains voltage by injecting a small frequency increment in the second one. This paper compares five alternatives to estimate the gain in only one half-period of the mains, what would allow to increase the controller bandwidth. The alternatives are based on the computation of the DTFS of the sidebands. They are off-line implemented and experimentally verified. The proposed method can also be implemented in real time into a digital controller.

I. Introduction

Domestic induction heating applications require regulation in the cooking temperature by controlling the power transferred to the load. The considered topology in this work is the series-resonant half-bridge inverter (Fig. 1). The inductor-vessel is modeled as a series R - L circuit [1] where both are frequency-dependent. The bus voltage, v_{bus} , is a full-wave rectified mains waveform and the bus capacitor filter is designed to allow a big voltage ripple. Then, the inverter generates a medium-frequency (20 kHz - 100 kHz) current that flows through the induction coil. The produced alternating magnetic field generates heat in the bottom of the metal cooking pan due to induced Eddy current losses.

The power delivered to the load is usually controlled by varying the operating switching frequency, f_{sw} , and the duty cycle, D, in the middle-high output power range [2]. Due to the rectified mains voltage, the sampling time of the output power is equal to one half-period of the mains, T_b , so the closed-loop bandwidth must be below the mains frequency. Thus, in this range of frequencies, the frequency-to-output power transfer function, $G_{pf}(s)$, and the duty-to-output power transfer function, $G_{pd}(s)$, can be approximated by their dc-gains: $K_{pf0} = G_{pf}(0)$ and $K_{pd0} = G_{pd}(0)$ [3].

Previous works [4, 5] have shown the variability of these gains with the operating point and load impedance, and how the controller performance can be improved by computing their values. In [4],

the duty cycle is maintained constant to a value of D = 0.5, and the dc-gain K_{pf0} is computed off-line and stored in a table for different operating points. Then, after identifying the equivalent R - L load values, a gain-scheduling controller is designed. However, the bus voltage is assumed to be ideal (230 V_{rms}). In [5], K_{pf0} and K_{pd0} are computed by numerical differentiation between consecutive bus cycles by injecting small frequency and duty perturbations. Although this approach is quite simple and accurate, the sampling time is increased for the additional identification bus cycles. This article is focused on the computation of the dc-gain K_{pf0} in one bus cycle.

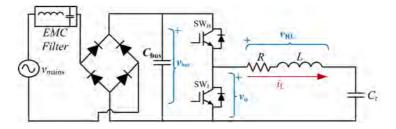


Fig. 1: Power electronics for a series half-bridge resonant inverter

The rest of the paper is organized as follows. The five approaches that compute the dc-gain in T_b and take into account the bus voltage amplitude modulation are detailed in section II. In sections III and IV, simulation and experimental results are reported respectively. Finally, conclusions and some remarks are drawn in section V.

II. Frequency-to-Output Power Transfer Gain

With a constant dc-bus voltage, the power delivered to the load can be expressed as:

$$P = \sum_{h=1}^{H} P_h = \sum_{h=1}^{H} \frac{R_h}{2} \frac{\hat{V}_h^2}{Z_h^2} = \sum_{h=1}^{H} \frac{G_h}{2} \hat{V}_h^2$$
(1)

where \hat{V}_h is the output voltage amplitude, R_h the resistance, Z_h the load impedance magnitude, and G_h the conductance (i.e. the real component of the admittance) at the corresponding *h*th-order harmonic of the switching angular frequency, $h\omega_{sw}$.

$$G_h = \operatorname{Re}\left(\frac{1}{Z_h}\right) = \frac{R_h}{R_h^2 + X_h^2} \tag{2}$$

 K_{pf0} can be obtained by using the harmonic balance method [6], which matches with the partial derivative of the output power, *P*, with respect to the input control variable f_{sw} :

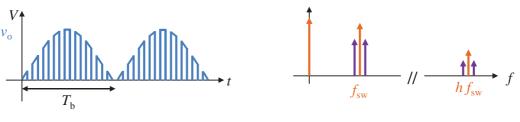
$$K_{\rm pf0} = \frac{\partial P}{\partial f}\Big|_{f_{\rm sw}} = -\sum_{h=1}^{H} \hat{V}_h^2 \frac{R_h}{f_{\rm sw}} \frac{(L_h h \omega_{\rm sw})^2 - 1/(C_{\rm r} h \omega_{\rm sw})^2}{Z_h^4}.$$
(3)

With a constant dc bus, the fundamental harmonic has the main contribution [6]. However, when considering the rectified bus voltage, the contribution of the fundamental harmonic is reduced [7]. Let us assume that the bus voltage is a rectified sine wave with period $T_b = 1/f_b$. Thus, the output voltage, v_o , can be seen as an amplitude modulated signal and it has harmonic components at frequencies $f_{h,n} = h \cdot f_{sw} + n \cdot f_b$ where $n \in \mathbb{Z}$ [7]. Under certain conditions of the quality factor Q of the load, that are fulfilled in the domestic induction heating field, the three dominant components of the output power are at f_{sw} , $f_{sw} + f_b$ and $f_{sw} - f_b$. v_o also includes sinusoidal components at the switching frequency and two sidebands, so it can be approximately expressed as:

$$v_{\rm o}(t) = \hat{V}_{0,0} + \hat{V}_{1,0}\sin(\omega_{\rm sw}t + \varphi_0) + \hat{V}_{1,1}\sin((\omega_{\rm sw}+\omega_{\rm b})t + \varphi_1)) + \hat{V}_{1,-1}\sin((\omega_{\rm sw}-\omega_{\rm b})t + \varphi_{-1})), \quad (4)$$

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where $\hat{V}_{1,0}$, $\hat{V}_{1,1}$ and $\hat{V}_{1,-1}$ represent the harmonics at the switching frequency, upper sideband and lower sideband, respectively.



(a) Waveform in the time domain

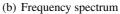


Fig. 2: Voltage at the half-bridge output v_0

The five methods presented in this work are based on different approximations of the output power taking into account the upper and lower sidebands. The first method only considers the component at the switching frequency. The output power is approximated as:

$$P \approx P_{\rm M1} = P_{1,0} = \frac{R_{1,0}}{2} \frac{\hat{V}_{1,0}^2}{Z_{1,0}^2}.$$
(5)

Thus, the first method, M1, estimates the dc gain as:

$$K_{\rm pf0,M1} = -\hat{V}_{1,0}^2 \frac{R_{1,0}}{f_{\rm sw}} \frac{(L_{1,0}\omega_{\rm sw})^2 - 1/(C_{\rm r}\omega_{\rm sw})^2}{Z_{1,0}^4}.$$
(6)

The signal power after applying the full-wave rectified bus voltage is spread out at the sidebands so the power at the switching frequency is reduced. The second method, M2, considers the first harmonic, the upper sideband and the lower sideband. The output power is approximated as:

$$P \approx P_{\rm M2} = P_{1,0} + P_{1,1} + P_{1,-1} = \frac{R_{1,0}}{2} \frac{\hat{V}_{1,0}^2}{Z_{1,0}^2} + \frac{R_{1,1}}{2} \frac{\hat{V}_{1,1}^2}{Z_{1,1}^2} + \frac{R_{1,-1}}{2} \frac{\hat{V}_{1,-1}^2}{Z_{1,-1}^2}.$$
(7)

Thus, the dc gain estimated by M2 is:

$$K_{\rm pf0,M2} = -\hat{V}_{1,0}^2 \frac{R_{1,0}}{f_{\rm sw}} \frac{(L_{1,0}\omega_{\rm sw})^2 - 1/(C_{\rm r}\omega_{\rm sw})^2}{Z_{1,0}^4} - \hat{V}_{1,1}^2 \frac{R_{1,1}}{f_{\rm sw} + f_{\rm b}} \frac{(L_{1,1}(\omega_{\rm sw} + \omega_{\rm b}))^2 - 1/(C_{\rm r}(\omega_{\rm sw} + \omega_{\rm b}))^2}{Z_{1,1}^4} - \hat{V}_{1,-1}^2 \frac{R_{1,-1}}{f_{\rm sw} - f_{\rm b}} \frac{(L_{1,-1}(\omega_{\rm sw} - \omega_{\rm b}))^2 - 1/(C_{\rm r}(\omega_{\rm sw} - \omega_{\rm b}))^2}{Z_{1,-1}^4}.$$
(8)

Since $\omega_{sw} >> \omega_b$, the third method, *M*3, assumes that $R_{1,0} = R_{1,1} = R_{1,-1}$ and $Z_{1,0} = Z_{1,1} = Z_{1,-1}$ and approximates the output power as:

$$P \approx P_{\rm M3} = \frac{\hat{V}_{1,0}^2 + \hat{V}_{1,1}^2 + \hat{V}_{1,-1}^2}{\hat{V}_{1,0}^2} P_{1,0}.$$
(9)

Thus, the dc gain estimated by M3 is:

$$K_{\rm pf0,M3} = \frac{\left(\hat{V}_{1,0}^2 + \hat{V}_{1,1}^2 + \hat{V}_{1,-1}^2\right)}{\hat{V}_{1,0}^2} K_{\rm pf0,M1}.$$
(10)

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From the point of view of digital signal processing, the full-wave rectified v_{bus} acts as the window functions used to decrease the spectral leakage in the discrete-time Fourier series (DTFS) [8]. When a window function $w(\tau)$ is applied to a signal, the overall signal power is reduced by the incoherent power gain (ICG) [9]:

$$ICG = \frac{1}{T_{\rm b}} \int_0^{T_{\rm b}} w^2(\tau) d\tau \tag{11}$$

and the amplitude for each signal frequency component is reduced by the coherent gain (CG):

$$CG = \frac{1}{T_{\rm b}} \int_0^{T_{\rm b}} w(\tau) d\tau.$$
⁽¹²⁾

The window function in this case is:

$$w(\tau) = \frac{v_{\text{bus}}(\tau)}{\max(v_{\text{bus}})}, \quad 0 \le \tau \le T_{\text{b}}.$$
(13)

Thus, the following relationship holds between the fundamental harmonic \hat{V}_1 with a constant dc bus voltage equal to the rms value of v_{bus} , and the harmonic $\hat{V}_{1,0}$ at the switching frequency with the rectified bus voltage, v_{bus} :

$$\hat{V}_1^2 = \frac{ICG}{CG^2} \hat{V}_{1,0}^2. \tag{14}$$

For an ideal full-wave rectified sine: ICG = 0.5, $CG = 2/\pi = 0.637$ and $ICG/CG^2 = \pi^2/8 = 1.2337$. The real value of ICG/CG^2 can be computed from the output voltage, v_0 , or from the bus voltage, v_{bus} , sampled at a lower rate:

$$\frac{ICG}{CG^2} = D\frac{v_{\text{o,rms}}^2}{v_{\text{o,avg}}^2} = \frac{v_{\text{bus,rms}}^2}{v_{\text{bus,avg}}^2}.$$
(15)

Once these gains are calculated, the fourth method, M4, approximates the output power as:

$$P \approx P_{\rm M4} = \frac{ICG}{CG^2} P_{1,0} = \frac{ICG}{CG^2} \frac{R_{1,0}}{2 \cdot Z_{1,0}^2} \hat{V}_{1,0}^2 \tag{16}$$

and estimates the dc gain as:

$$K_{\rm pf0,M4} = \frac{ICG}{CG^2} K_{\rm pf0,M1}.$$
(17)

The output power approximation used in (9) can also be expressed as:

$$P \approx P_{\rm M3} = P_{\rm M5} = \frac{R_{1,0}}{2} \frac{\hat{V}_{1,0}^2 + \hat{V}_{1,1}^2 + \hat{V}_{1,-1}^2}{Z_{1,0}^2} = \frac{G_{1,0}}{2} \left(\hat{V}_{1,0}^2 + \hat{V}_{1,1}^2 + \hat{V}_{1,-1}^2 \right), \tag{18}$$

this expression assumes the conductance at the first harmonic, $G_{1,0}$, and at the sidebands, $G_{1,1}$ and $G_{1,-1}$, are similar. The dc gain can be computed using the centered differencing formula as follows:

$$K_{\rm pf0} \approx \frac{P(f_{\rm sw} + f_{\rm b}) - P(f_{\rm sw} - f_{\rm b})}{2f_{\rm b}} = \frac{\hat{V}_{1,0}^2 + \hat{V}_{1,1}^2 + \hat{V}_{1,-1}^2}{2f_{\rm b}} \left(\frac{G_{1,1} - G_{1,-1}}{2}\right).$$
(19)

Thus, the fifth method *M*5 estimates the dc gain as:

$$K_{\rm pf0,M5} = \frac{\hat{V}_{1,0}^2 + \hat{V}_{1,1}^2 + \hat{V}_{1,-1}^2}{2f_{\rm b}} \left(\frac{P_{1,1}}{\hat{V}_{1,1}^2} - \frac{P_{1,-1}}{\hat{V}_{1,-1}^2}\right).$$
(20)

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To sum up, all the methods compute the dc gain from the DTFS [10] of the output voltage, v_o , and the inductor current, i_L , during T_b . The first method, M1, requires computing the DTFS at the switching frequency. Methods M2, M3 and M5 also need to calculate DTFS at the sidebands. The method M4 needs the same resources as M1, but it also requires computing the value of ICG/CG^2 . The computational complexity required for every method in terms of number of products and divisions is shown in Table I, where one DTFS implies 2N real multiplications (N complex multiplications) and N is the number of samples per bus cycle.

Table I: Computational complexity of every method

	Multiplications	Divisions
<i>M</i> 1	O(4N)	3
М2	O(12N)	5
М3	O(8N)	3
<i>M</i> 4	O(5N)	3
<i>M</i> 5	O(10N)	1

In Table I, it is assumed that the window gains in method M4 are computed at the original sampling rate and not at a lower one. In that case the number of multiplications would decrease considerably.

III. Simulation Results

The circuit parameters are $C_r = 1080$ nF, $L = 30 \,\mu$ H, and $R = 2.5 \,\Omega$. The bus voltage is an ideal full-wave rectified sinusoid with period $T_b = 10$ ms and amplitude 325 V. The average output power is computed between two zero crossings of the mains voltage from the output voltage and the inductor current sampled at 100 Msps.

Fig. 3(a) shows the percentage of the output power respect to the total power for the methods commented previously. The power delivered by the harmonic component at the switching frequency represents the 80 % of the total power. When the upper and lower sidebands or ICG/CG^2 are taken into account the percentage of delivered power is greater than 95 %. This shows that the first harmonic approximation to measure the output power that was discarded in [7] can be used if ICG and CG are taken into account.

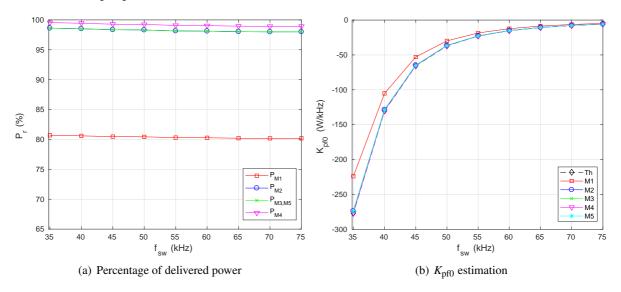


Fig. 3: Simulation results for different methods and frequencies

Fig. 3(b) shows the estimation of K_{pf0} using the methods introduced in the last section. The theoretical value is the approximation of the derivative of the power at f_{sw} and it has been obtained by numerical

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differentiation using the fourth order centered differencing formula with $\Delta f = 500$ Hz:

$$K_{\rm pf0,th}(f_{\rm sw}) = \frac{-P(f_{\rm sw} + 2\Delta f) + 8P(f_{\rm sw} + \Delta f) - 8P(f_{\rm sw} - \Delta f) + P(f_{\rm sw} - 2\Delta f)}{12\Delta f} + O((\Delta f)^4).$$
(21)

It can be seen that the first harmonic approximation under-estimates the absolute value of K_{pf0} and the other alternatives fit exactly to the theoretical one.

IV. Experimental Results

Fig. 4 shows the prototype used for the experimental verification of the proposed methods. A Chroma 61605 AC power source generates a sinusoidal voltage of 230 Vrms and 50 Hz. This voltage is rectified to get the bus voltage that feeds the inverter. The inductor-load system is composed of a circular coil with an external diameter of 21 cm and a commercial pot placed above the inductor.

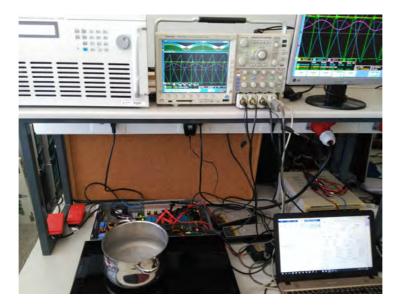


Fig. 4: Experimental setup

The switching frequency, f_{sw} , has been varied from 35 kHz to 75 kHz at steps of 5 kHz. For every frequency, the output voltage and inductor current during T_b have been measured and digitized with a Tektronix MSO 4104 oscilloscope at a sampling frequency of 100 Msps. Besides, for every frequency, f_{sw} , these measurements have also been taken at $f_{sw} \pm 500$ Hz and $f_{sw} \pm 1$ kHz so that (21) can be applied.

The obtained measurements have been processed off-line to obtain the output power and the frequencyto-output-power gain transfer function, K_{pf0} . Fig. 5(a) shows that the power delivered by the harmonic component at the switching frequency represents less than 80 % of the total power. As in simulation, when the upper and lower sidebands or the window gains are taken into account the percentage of delivered power is greater than 95 %.

Fig. 5(b) shows the estimation of K_{pf0} using the methods previously introduced. The theoretical value of K_{pf0} has been obtained applying (21). It can be seen that methods *M*1 to *M*4 give a close approximation to the theoretical gain. In fact, the methods that take into account the sidebands (*M*2 and *M*3) and the method that computes the window gains (*M*4) give a pretty similar result, which reinforces the idea that most of the information lies in the first harmonic and its sidebands. The method *M*5 is not as good as expected, its application results in positive values of K_{pf0} at some switching frequencies, what makes no sense since the output power is a monotonically decreasing function with the switching frequency.

Method M5 fails even using congruent frequencies because the load is nonlinear, and the values of R and L depend on the frequency [11] and the driven current [12], something that was not modelled in the simulation. Fig. 6 shows the measured conductance at the switching frequency and at its sidebands.

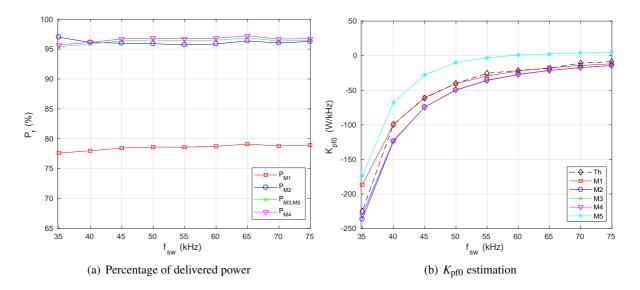


Fig. 5: Experimental results for different methods and frequencies

They are different because R and L are not constant, besides the difference between the conductances at the upper and lower sidebands is so small that there is not enough accuracy in the computation of (20).

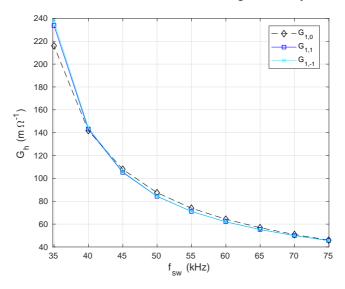


Fig. 6: Condutance measurements

V. Conclusion

When the bus is not a constant dc voltage, the power delivered by the harmonic component at the switching frequency represents only around the 80 % of the total power. This work presents three methods, *M*2 to *M*4, that solve this problem. Since the results are pretty similar for these three methods, the decision of which one is finally proposed will be based on the number of resources/calculations that are needed.

In global terms, the experimental results agree with the simulation ones for methods M1 to M4. They do not agree for method M5 because the simulated load model was linear and there are some differences in terms of accuracy and quantization.

As shown in Table I, method M4 only requires computing O(5N) multiplications and 3 divisions. If the window gains are calculated from v_{bus} at a lower sampling rate the number of multiplications would be even lower. This is the method finally proposed because it requires less resources than any of the methods that take into account the sidebands and can be easily implemented with digital techniques for on-line estimation.

References

- J. Acero, C. Carretero, I. Millán, O. Lucía, R. Alonso, and J. M. Burdío, "Analysis and modeling of planar concentric windings forming adaptable-diameter burners for induction heating appliances," IEEE Transactions on Power Electronics, vol. 26, no. 5, pp. 1546–1558, May 2011.
- [2] O. Lucía, J. M. Burdío, I. Millán, J. Acero, and D. Puyal, "Load-adaptive control algorithm of half-bridge series resonant inverter for domestic induction heating," IEEE Transactions on Industrial Electronics, vol. 56, no. 8, pp. 3106–3116, Aug 2009.
- [3] A. Domínguez, L. A. Barragán, J. I. Artigas, A. Otín, I. Urriza, and D. Navarro, "Reduced-order models of series resonant inverters in induction heating applications," IEEE Transactions on Power Electronics, vol. 32, no. 3, pp. 2300–2311, March 2017.
- [4] O. Jiménez, O. Lucía, I. Urriza, L. A. Barragán, P. Mattavelli, and D. Boroyevich, "An FPGA-based gainscheduled controller for resonant converters applied to induction cooktops," IEEE Transactions on Power Electronics, vol. 29, no. 4, pp. 2143–2152, April 2014.
- [5] A. Domínguez, L. A. Barragán, A. Otín, D. Navarro, and D. Puyal, "Inverse-based power control in domestic induction-heating applications," IEEE Transactions on Industrial Electronics, vol. 61, no. 5, pp. 2612–2621, May 2014.
- [6] A. Domínguez, A. Otn, L. A. Barragán, O. Lucía, and J. I. Artigas, "Modeling of resonant inverters with high harmonic content using the extended describing function method," in IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society, Oct 2012, pp. 5949–5954.
- [7] O. Jiménez, O. Luca, I. Urriza, L. A. Barragan, and D. Navarro, "Power measurement for resonant power converters applied to induction heating applications," IEEE Transactions on Power Electronics, vol. 29, no. 12, pp. 6779–6788, Dec 2014.
- [8] J. Proakis and D. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications. Prentice-Hall, 3rd edition, 1996.
- [9] F. J. Harris, "On the use of windows for harmonic analysis with the discrete fourier transform," Proceedings of the IEEE, vol. 66, no. 1, pp. 51–83, Jan 1978.
- [10] O. Jiménez, Luca, L. A. Barragán, D. Navarro, J. I. Artigas, and I. Urriza, "FPGA-based test-bench for resonant inverter load characterization," IEEE Transactions on Industrial Informatics, vol. 9, no. 3, pp. 1645–1654, Aug 2013.
- [11] N. Domingo, L. A. Barragán, J. M. M. Montiel, A. Domínguez, and J. I. Artigas, "Fast power-frequency function estimation for induction heating appliances," Electronics Letters, vol. 53, no. 7, pp. 498–500, 2017.
- [12] J. Serrano, J. Acero, I. Lope, C. Carretero, J. M. Burdío, and R. Alonso, "Modeling of domestic induction heating systems with non-linear saturable loads," in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), March 2017, pp. 3127–3133.