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Synchronous OEIC integrating receiver for ORGA applications

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Abstract

This work presents a monolithically integrated synchronous optical receiver fabricated in a standard 0.35 µm CMOS process. The receiver consists of a regenerative latch acting as a sense amplifier; two highly effective, low-capacitance *pin* photodiodes connected to its output nodes (one of them blocked to the light); and an adjustable reference current to compensate the dynamic offset created by the asymmetries between the parasitic capacitances of the photodiodes. For λ = 635 nm, a sensitivity of −25.8 dBm, −26.0 dBm, and −28.4dBm is obtained, respectively, for 400 Mbit/s, 350 Mbit/s, and 250 Mbit/s (BER = 10^{-9}). The power consumption is 670 µW, which translates to an energy efficiency of 1.7 pJ/bit at 400 Mbit/s.

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Keywords: Integrated optoelectronics; integrated *pin* photodiodes; integrating receivers.

1. Introduction

High-speed reconfigurable circuits have attracted great interest because their operation can be modified in order to avoid idle activity, allowing a re-use of the hardware components and thus optimizing performance. Although field programmable gate arrays (FPGAs) are the most commonly used reconfigurable system, their reconfiguration cycles of typically several milliseconds make them unsuitable for the speeds demanded in today's applications, which range up to several hundreds of megahertz [1], [2]. Higher reconfiguration speeds can be achieved by multi-context FPGAs, DAP/DNA or DRP circuits, but at a very low gate density [3].

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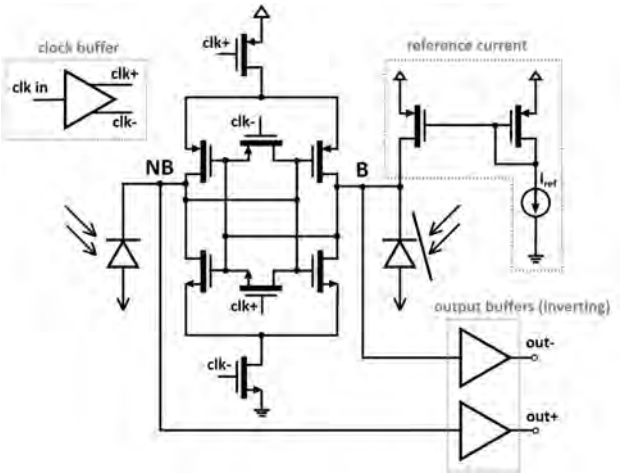

Fig. 1. Circuit diagram of the OEIC. One clock phase resets and the other one activates the latch. A DC current into the blocked PD node compensates asymmetries in the parasitic capacitances of the blocked and non-blocked PDs.

Another alternative are optically reconfigurable gate arrays (ORGAs) in combination with holographic memories, which can achieve near Gbit/s speeds without compromising gate density. To operate, ORGAs require optical receivers with high sensitivity, low power consumption and large integration density. Because of this, implementations based on conventional optical detectors with a transimpedance amplifier (TIA) are not possible because of their high power and large die area. For instance, in [4] a TIA with post amplifiers in 0.35 µm high-voltage CMOS needed 55 mW and a core area, excluding the PD, of 79 300 μm^2 to achieve a digital output.

As an alternative to TIA-based optical receivers, this paper proposes the use of the integrating optical receiver, whose digital operation achieves a drastic reduction of the power consumption while at the same time allows being downscaled to shorter technologies for faster operation. Recently reported implementations achieve Gbit/s with energy efficiencies of 0.9 pJ/bit [5], where a multi-quantum well (MQW) *pin* PD was flip-chip bonded to a CMOS chip, and 4.5 pJ/bit [6], which used an electro-absorption modulator at 1550 nm. The main disadvantage of integrating optical receivers is low sensitivity. For instance, [5] reports −16.5 dBm at 1 Gbit/s, and [6] −19.4 dBm at 1.2 Gbit/s. This happens because the voltage generated across the PD capacitance is inversely proportional to the capacitance itself; for this reason, the sensitivity of integrating optical receivers can be improved by their monolithic integration with the PD in an optoelectronic integrated circuit (OEIC). In this respect, current standard silicon CMOS and BiCMOS technologies allow small-area *pin* PDs with a capacitance under 100 fF, responsivity higher than 0.5 AW^{-1} and −3 dB cut-off frequency above 1 GHz [7].

In this work, a monolithic integrating optical receiver is implemented in a 0.35 µm CMOS process that allows the integration of a highly efficient 50 µm *pin* PD featuring 50 fF capacitance. The circuit is fed at only 2.5 V and it achieves 400 Mbit/s operation with a bit error ratio (BER) better than 10^{-9}. The regenerative latch achieves an energy efficiency of 1.7 pJ/bit and, along with the output buffer (excluding the PDs), occupies 50 µm × 30 µm.

2. Integrating optical receiver OEIC

The architecture of the OEIC is shown in Fig. 1. A regenerating latch driven by a synchronization clock operates in two phases: when the clock is high, i.e., clk+ is in a logic 1, the latch is reset to a metastable state characterized by $V_B = V_{NB} \approx V_{dd}/2$; in turn, when the clock is low, the operation as a latch is enabled. Two monolithically integrated *pin* PDs are connected to the outputs, one of them receiving the light input and the other one blocked by a metal layer. Ideally, if no external stimuli act after the reset, the metastable state is kept for the half clock period when the latch is enabled; however, in a practical implementation there are asymmetries breaking the metastable state that

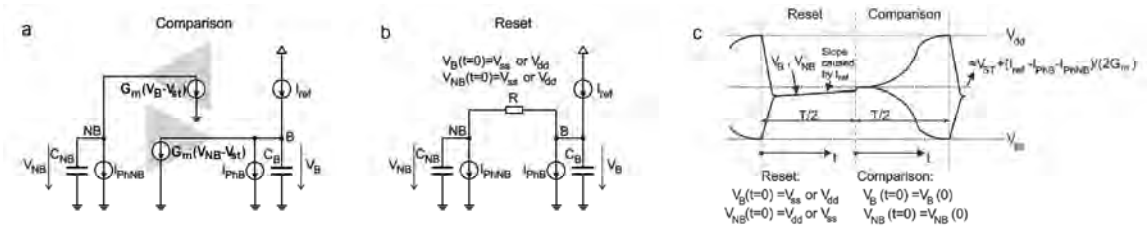

Fig. 2. Model for the latch (a) in the comparison phase and (b) during reset. (c) Main transients of the latch during reset and comparison.

need to be compensated for reliable operation. In particular, there is a significant increase of roughly 40 % in the parasitic capacitance of the blocked PD over the non-blocked PD caused by the metal layer above.

The asymmetry between the parasitic capacitance C_{NB} at node NB (non-blocked PD) and C_B at node B (blocked PD) causes a dynamic offset for the latch that has been analysed in [8]. Figs. 2a and 2b show, respectively, the circuits equivalent to Fig. 1 for comparison (clk+ = 1) and reset (clk+ = 0), where I_{PhNB}, I_{PhB} are the PD photo-currents compared during the comparison phase, G_m the transconductance and V_{st} the switching threshold of one of the two latch inverters, which are assumed equal for simplicity. I_{PhB} is usually very small due to light blocking and can be considered as dark current and current caused by stray light to the active area. A DC current $I_{ref} < 1$ µA is fed to node B to minimize dynamic offset. Fig. 2c shows a sketch of the transients in the latch.

The condition of a metastable state for equal PD currents ($I_{PhNB} = I_{PhB} = I_{Ph}$) in the comparison phase is that the exponential growing term of $V_B - V_{NB}$ is zero. Under the condition that $V_{st} > V_0$ in the comparison phase, the dynamic offset can be adjusted with a positive current I_{ref} into node B, taking care that for most process tolerances this condition is valid so that no negative I_{ref} is needed, which is controlled during the design of the latch. Another advantage is that the initial voltage V_0 of the comparison phase is controlled during the reset phase with I_{ref}.

3. Measured results

An edge-emitting laser source with λ = 635 nm and extinction ratio ER = 10 and a vertical cavity surface-emitting laser (VCSEL) with λ = 675 nm and ER = 5.5 have been used to generate the light input data stream, whose average power is controlled by an optical attenuator before reaching the OEIC through a multi-mode fibre with a core diameter of 62.5 µm. The output from the OEIC is sensed on-wafer by an active probe with 0.1 pF parallel 10 MΩ input impedance and 1:20 attenuation. The average power of the modulated light signal is obtained directly measuring the current through the OEIC substrate, which can be done because the anode of the integrated *pin* PD is formed by the p+ substrate and all transistors are isolated by deep n-wells or n-wells, taking into account the PD sensitivity, which is 0.51 AW^{-1} for 635 nm and 0.53 AW^{-1} for 675 nm.

Fig. 3 shows the eye diagrams at BER = 10^{-9} and Fig. 4 the sensitivity measurements carried out on the OEIC. The sensitivities at 400 Mbit/s, 350 Mbit/s, and 250 Mbit/s are, respectively, −25.8 dBm, −26.0 dBm and −28.4 dBm for 635 nm (Fig. 4a), and −25.8 dBm, −26.3 dBm and −27.4 dBm for 675 nm (Fig. 4b), all corrected for ER = ∞ and obtained for a 2^{31}-1 PRBS at BER = 10^{-9}. Finally, the power consumption of the OEIC is 4.75 mW, of which only 670 µW are consumed by the latch; at 400 Mbit/s, this translates to an energy efficiency of 1.7 pJ/bit.

4. Comparison and conclusion

This work presents a synchronous OEIC integrating receiver in an OPTO ASIC 0.35 µm CMOS technology with integrated *pin* PDs and dynamic offset compensation. The prototype shows a sensitivity of −25.8 dBm, −26.0 dBm and −28.4 dBm at 400 Mbit/s, 350 Mbit/s and 250 Mbit/s (BER = 10^{-9}), and a power consumption of only 670 µW.

Although the digital nature of integrating receivers makes the maximum speed dependent on technology, the OEIC shows a clear improvement in terms of sensitivity, which is 6.6 dB better than in [6], which operated at 1 Gbit/s in 250 nm CMOS, and 9.5 dB better than in [5], which operates at 1.2 Gbit/s in 90 nm CMOS. [9] used 0.7

Fig. 3. Eye diagram of the output signal of the OEIC at (a) 400 Mbit/s, average optical power −25.8 dBm, (b) 350 Mbit/s, average optical power −26.0 dBm, and (c) 250 Mbit/s, average optical power −28.4 dBm. 2^{31}-1 PRBS, BER = 10^{-9}, λ = 635 nm, ER = 10.

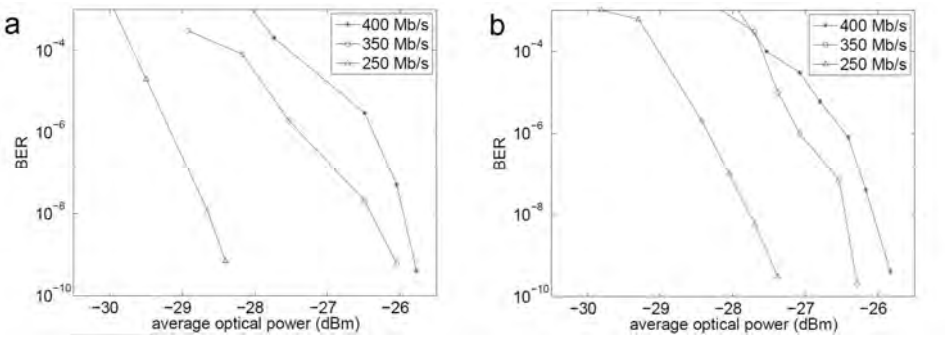

Fig. 4. Measured sensitivity of the OEIC at 400 Mbit/s, 350 Mbit/s and 250 Mbit/s for (a) λ = 635 nm, ER = 10 and (b) λ = 675 nm, ER = 5.5. 2^{31}-1 PRBS. The shown BER curves are corrected to ER = ∞.

µm CMOS and reported 14 dB worse sensitivity at 180 Mbit/s. Finally, [10] achieves a remarkable −29.0 dBm sensitivity in 0.35 µm CMOS, but at only 5 Mbit/s whereas our OEIC remains only 0.6 dB below in sensitivity but for a bit rate 50 times larger at 250 Mbit/s. This good sensitivity is achieved without compromising the low power and small area features of integrating optical receivers. In this sense, its energy efficiency is 1.7 pJ/bit and its area is 50 µm × 30 µm, in contrast to the hundreds of µm per side of TIA-based receivers, making it appropriate for applications featuring massively parallel receivers such as ORGAs.

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