Analog Integr Circ Sig Process
DOI 10.1007/s10470-013-0098-7

A rail-to-rail differential quasi-digital converter for low-power applications

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Received: 29 June 2012 / Revised: 30 April 2013 / Accepted: 5 June 2013

Abstract This paper presents an ultra low power differential voltage-to-frequency converter (dVFC) suitable to be used as a part of a multisensory interface in portable applications. The proposed dVFC has been designed in 1.2-V 0.18-μm CMOS technology, and it works properly over the whole differential input range (0.6 ± 0.6 V) providing an output frequency range of 0.0–0.9 MHz. The system has been tested for temperature variations from −40 to +120 °C and supply voltage variations of up to 30 %, being the maximum linearity error in the worse case of 0.017 %. Simulations against common mode voltage variations show a deviation in the output frequency of 0.4 %. This dVFC has power consumption below 60 μW, and it includes an enable terminal that sets the system in a sleep mode (180 nW) while no conversion is request. The dVFC occupies an active area of 250 μm × 150 μm.

Keywords CMOS mixed integrated circuits · Low-voltage low-power · Sensor interface · Voltage-to-frequency converter

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1 Introduction

At present, the use of wireless sensor networks (WSN) is continuously growing. Therefore, the development of smart sensors has increased due to the need for the sensor signal to be compatible with digital signal processors. A smart sensor includes, besides the sensing device, the interface so that the output is a digital signal related to the measured magnitude. Thus, due to the large amount of sensors involved in these networks, the use of low-cost analog sensors along with a programmable interface is the preferred choice if cost reduction becomes a priority. The interface has to be capable of adapting every sensor output to the input digital port requirements of the microcontroller (μC) embedded in each sensing node.

The simplest interface consists of an analog-to-digital converter (ADC) preceded by a programmable voltage adapter that adjusts the sensor output range to the ADC input range by means of gain and offset controls. However, in embedded microcontroller measurement systems, such as WSN, the use of voltage-to-frequency converters (VFC), also known as quasi-digital converters, have risen as a highly suitable alternative to the standard analog-to-digital conversion due to its advantages: the quasi-digital frequency signal offers high noise immunity and can straight interface the microcontroller, which next performs the final digitalization using its internal timers [1].

There are several types of VFCs, being the charge balance and the multivibrator the most common approaches. Although the charge balance VFC is more accurate than its multivibrator based counterpart, the former is also more complex and it demands more power than the latter [2], which provides sufficient accuracy to be used with low cost sensors used in WSNs. Therefore, recently reported low-voltage low-power CMOS VFCs are mainly based on an input voltage-to-

Journal : Large 10470 | Dispatch : 13-6-2013 | Pages : 9
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MS Code : ALOG-D-12-02599 | ☑ CP | ☑ DISK

current converter (VIC) followed by a multivibrator based current-to-frequency converter (IFC) and they operate in single-input mode [3, 4]. However, for certain sensor conditioning applications, such as the widely used Wheatstone bridge, or for noise rejection, differential signal processing would be desirable. Previous approaches to design CMOS differential VCFs also employ a VIC followed by an IFC approach, being the input differential VIC based on a differential amplifier with voltage controlled gain [5], an instrumentation amplifier [6] or a second generation current conveyor [7]. However, they present serious limitations in terms of input operating range, power consumption or important temperature dependence. Preliminary designs of the structure that is going to be introduced in this paper have been presented by the authors at two recent conferences [8, 9]. In addition, the proposed dVFC is a simplified and revisited version of the VFC presented at another conference [10], advancing towards ultra low-power consumption. Thus, in this final design, the biasing circuit has been improved to show a temperature independent behavior and a global enable has been included to set the system into an extremely low-power state while no measure is done. Further, to reduce power, OTAs are the simplest ones and the power management made in the control circuit has been corrected.

Therefore, the goal of this paper is the design and complete verification of a novel CMOS differential VFC fulfilling the following major requirements to fit WSN applications: low-voltage, compatible with the single-cell batteries used in the WSN market; low-power, in order to optimize battery life; rail-to-rail operation, since taking advantage of the full V_{DD} range results in enhanced resolution in the subsequent digitalization; the output levels have to be compatible with the µC logic levels and the output range must fit typical low-power µC clock frequencies (4 MHz). Finally, it is desirable that the VFC has temperature compensation and supply regulation to maintain constant sensitivity. Section 2 explains the proposed rail-to-rail temperature and supply independent differential VFC. Section 3 reports the main results obtained for a 1.2-V 0.18-µm CMOS implementation and conclusions are drawn in Sect. 4.

2 Differential voltage-to-frequency converter

2.1 Operation principle

The proposed differential voltage-to-frequency converter (Fig. 1) consists of a differential voltage-to-current converter (dVIC) followed by a bidirectional current integrator driven by a voltage window comparator (VWC) control circuit.

The input dVIC [Fig. 2(a)], as it will be explained thoroughly in Sect. 2.2, transforms the input signals $V_{in+} = V_{CM} + V_d/2$ and $V_{in-} = V_{CM} - V_d/2$ into signals $V_A = V_{CM} + V_d/4$ and $V_B = V_{CM} - V_d/4$ at nodes A and B, respectively. Note that the differential input voltages $V_{in+} - V_{in-} = V_d$ must be positive. Therefore a sign circuit (explained in Sect. 2.6) can be required. Voltages V_A and V_B generate across resistor R_S the current signal $I_d = V_d/2R_S$, which is next directly replicated through transistors T_3 and T_4 with a scaling factor given by K:1.

The scaled current I_d/K alternately charges and discharges a grounded capacitor C between the stable limits V_L and V_H of a VWC. The comparison results V_{CL}, V_{CH} are driven to a simple NAND-based RS flip-flop, which grants a stable output signal and provides the switching signals S_{DW} and S_{UP} that drive the gates of cascode transistors T_{3C} and T_{4C}, thus determining the direction of the current in the bidirectional current integrator. In this way, a repeated loop is built with a frequency of oscillation given by:

$$f_0 = \frac{I_d/K}{2C(V_H - V_L)} = \frac{1}{2C(V_H - V_L)}\frac{V_d}{2KR_S} \quad (1)$$

2.2 Differential voltage-to-current converter

The rail-to-rail dVIC is shown in Fig. 2(a). OTA_{VF1} and OTA_{VF2} are feedback voltage attenuation OTAs [11], which do not act as voltage followers but attenuate the input signal to keep transistors $T_1 - T_{1C}$ and $T_2 - T_{2C}$ in saturation region over the complete input range, so that the output current mirroring does not restrict the V–I operating range. To achieve this, let us focus on OTA_{VF1}, whose complete scheme is shown in Fig. 2(b). Between the main OTA1 non-inverting input –at a voltage V_{in+} due to negative feedback– and node A, an attenuator is introduced, implemented using a non-inverting amplifier stage formed by $OTA_{aux1} - T_{A1}$, an input resistor R_1 biased at V_1 and feedback resistor R_2. By means of a straightforward analysis, the voltage at node A is

$$V_A = \frac{R_2V_1 + R_1V_{in+}}{R_1 + R_2} \quad (2)$$

The voltage level V_1 is fixed to V_{CM} and resistors are set to $R_1 = R_2$, so that $V_A = V_{CM} + (V_d/4)$. Similarly, for OTA_{VF2}, again selecting the auxiliary voltage level $V_2 = V_{CM}$ and input and feedback resistors $R_3 = R_4$, the voltage at node B is

$$V_B = \frac{R_4V_2 + R_3V_{in-}}{R_3 + R_4} \quad (3)$$

This results in a fully symmetric structure, which maintains at nodes A and B the common mode voltage V_{CM} while the differential voltage V_d is halved. Therefore, the voltage across resistor R_S is $(V_A - V_B) = (V_d/2)$, and thus, a current $I_d = V_d/2R_S$ is generated.

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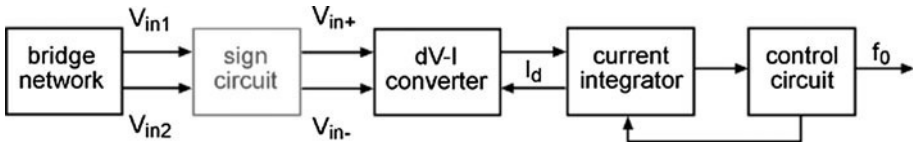
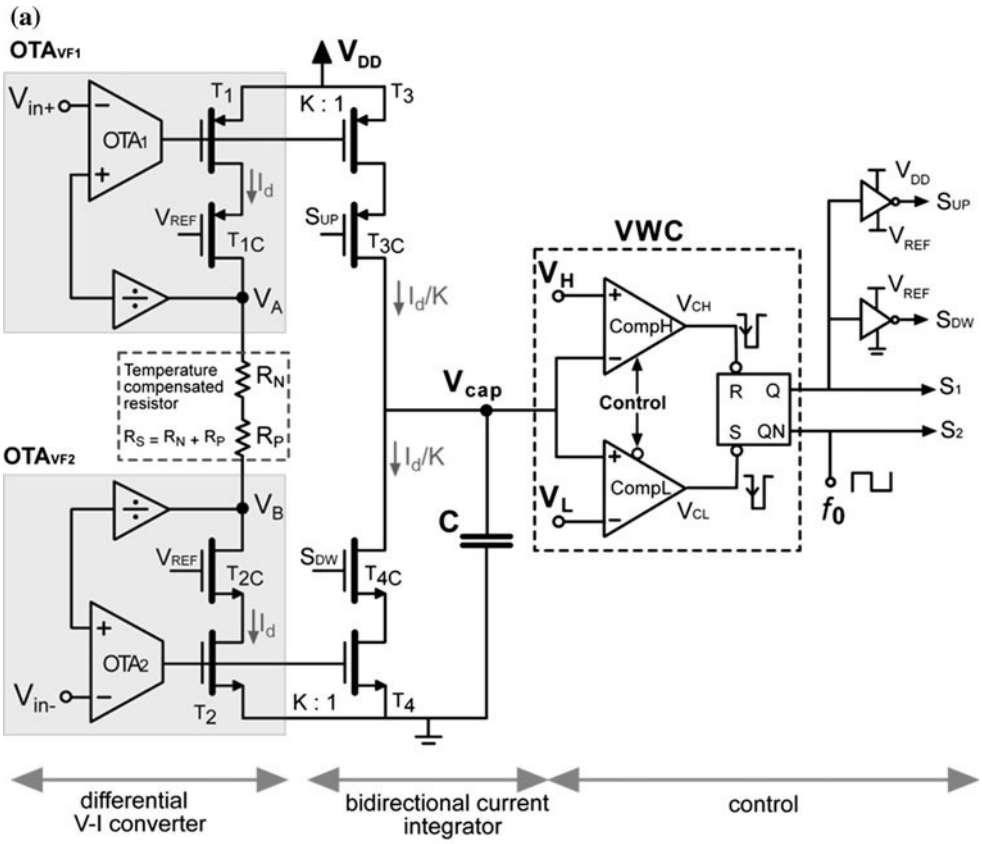


Fig. 1 Block diagram of the proposed differential VFC



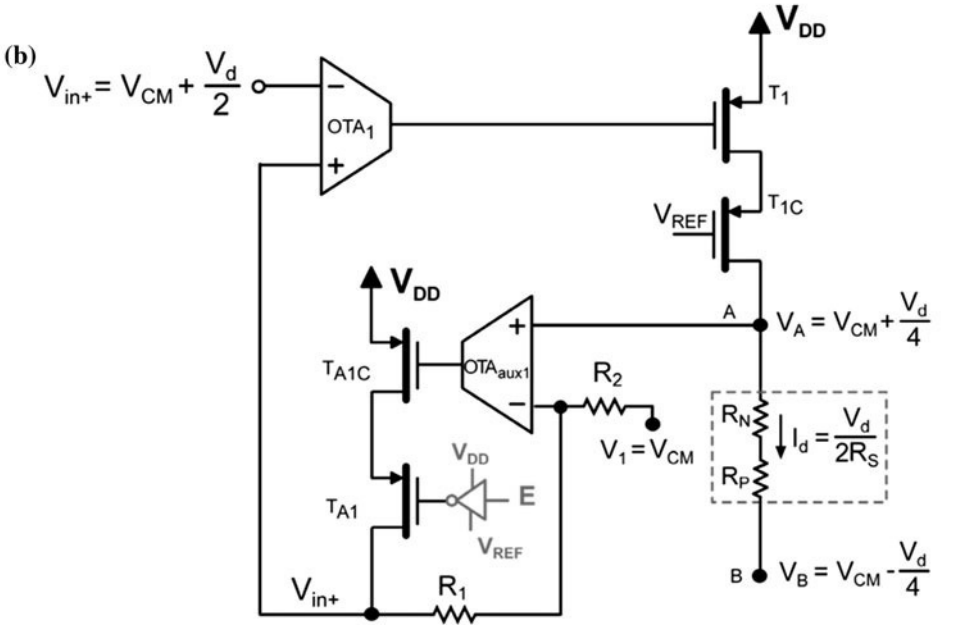


Fig. 2 Schematics of **a** proposed dVFC and **b** OTA_{VF1}

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As the input of both OTAs in OTA_{VF1} swing between V_{CM} and V_{DD}, they are made up using the simple NMOS input stage OTA shown in Fig. 3, to reduce both, the area and the power consumption. In the same way, as the input of both OTAs in OTA_{VF2} swing between *GND* and V_{CM}, they are made up of a simple PMOS input stage OTA, formed by the counterpart of the structure shown in Fig. 3. The resistor that makes the voltage-to-current conversion, R_S, is set to $R_S = 40$ kΩ and $R_1 = R_2 = R_3 = R_4 = 25$ kΩ, as a trade-off between power and area consumptions.

All OTAs work in the subthreshold region over all the input range to reduce power consumption, and they have a compensation network (a conventional $R_C - C_C$ network, not shown) to guarantee the system stability, while avoiding peaks in the closed-loop frequency response and underdamped oscillations [12].

2.3 Current integrator and control circuit

The generated current I_d is driven through transistors T_1 and T_2, and replicated through transistors T_3 and T_4 with a scaling factor K:1, being $K = 20/3$, in order to optimize the power consumption, while obtaining a suitable sensitivity in the dVFC. Cascode transistors are used to improve the current copy, but also because they work as the switching elements controlling the direction of the current: let us assume that the outputs of the VWC are $S_1 =$ '1′ and $S_2 =$ '0′, so that the switching signals that drive the gate of the cascode transistors T_{3C} and T_{4C} are $S_{UP} = V_{REF}$ and $S_{DW} = GND$ respectively. Thus, transistor T_{3C} is ON and T_{4C} is OFF, so that the current charges the capacitor C until the voltage V_{cap} reaches the comparison limit V_H. At that moment, the output of the upper comparator changes to '0′, what makes the VWC output signals change, being $S_1 =$ '0' and $S_2 =$ '1', and the switching signals $S_{UP} = V_{DD}$ and $S_{DW} = V_{REF}$, setting transistor T_{3C} in OFF and transistor T_{4C} in ON. Thus, the current discharges the capacitor until it reaches the lower limit V_L, starting again the charging phase. For both the NMOS and PMOS cascode transistors the gate voltage is set to $V_{REF} = 0.4$ V for simplicity. The integrating capacitor is set to $C = 3.125$ pF.

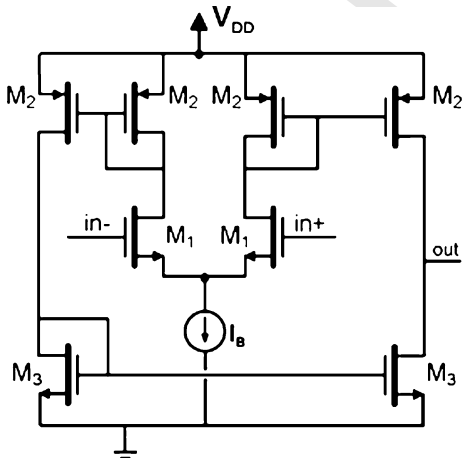

Fig. 3 Schematics of the NMOS OTA

The VWC is made up of two high-speed continuous-time simple differential pairs followed by inverters, shown in Fig. 4, and a NAND-based RS flip-flop. Transistors of the VWC employ minimal length to optimize speed. Comparison limits are set to $V_L = 0.4$ V and $V_H = 0.8$ V to keep transistors T_3 and T_4 working in the saturation region.

Therefore, taking into account the chosen values, the output frequency in Eq. (1) is now given by

$$f_0(MHz) = 0.75V_d(V) \tag{4}$$

2.4 V_{DD} and temperature dependence

Insensitivity to power supply variations is always desired, but it is even more important in battery operated systems, where the supply voltage continuously decreases. Thus, a simple solution to generate the bias current that reduces the power supply sensitivity is a conventional beta-multiplier referenced self-biasing circuit, shown in Fig. 5, that is used to set $I_B = 0.5$ μA [13]. Taking into account that all transistors work in subthreshold region, the current I_B is given by

$$I_B = \frac{nV_T}{R}\ln\alpha \tag{5}$$

where n is the emission coefficient, V_T is the thermal voltage (26 mV at room temperature) and $\alpha = 6$ is the scaling factor between M_4 and M_5.

Note that (5) is, in first order, power supply independent. With respect to temperature, I_B presents a positive variation due to the thermal coefficients of V_T and n. This variation can be compensated if the resistor $R = 115.6$ kΩ is implemented featuring the same positive variation. The temperature variation of a resistor is given by

$$R(T) = R_0\left(1 + TC_1(T-25) + TC_2(T-25)^2\right) \tag{6}$$

where R_0 is the resistor value at room temperature and TC_1 and TC_2 the first and second order temperature coefficients, respectively. Thus, R is made up with the serial connection of two resistors A and B with different thermal coefficients, being the composite resistor thermal coefficients given by

$$TC_i = TC_{i,A}(\beta/(1+\beta)) + TC_{i,B}(1/(1+\beta)) \tag{6}$$

where $\beta = R_{0,A}/R_{0,B}$ is the ratio of resistances at room temperature [14], being $i = 1, 2$ the order of the temperature coefficient. The composite resistor is made up with a NWELL ($TC_1 = 2.504 \times 10^{-3}$ °C^{-1},

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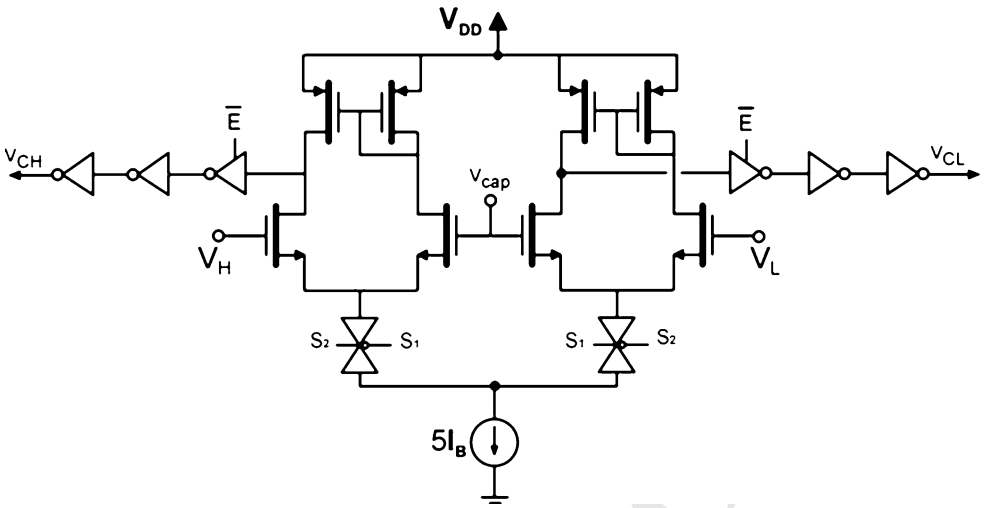

Fig. 4 Schematics of the comparators forming the VWC

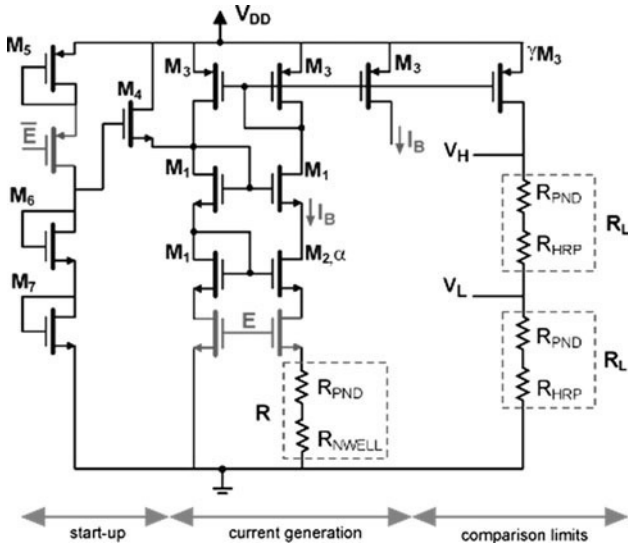

Fig. 5 Schematics of the β-multiplier reference circuit

$TC_2 = 8.566 \times 10^{-6}$ °C^{-2}) and a P$^+$ nonsalicide diffusion (PND) ($TC_1 = 1.184 \times 10^{-3}$ °C^{-1}, $TC_2 = 7.310 \times 10^{-7}$ °C^{-2}) resistors, being their ratio $\beta = 20/17$, and $TC_1 = 1.791 \times 10^{-3}$ °C^{-1}, $TC_2 = 4.355 \times 10^{-6}$ °C^{-2} the composite thermal coefficients, that compensate the temperature variation of V_T and n.

The VWC comparison limits, V_H and V_L, can be obtained from the generated I_B as shown in Fig. 5, being $V_L = 8I_BR_L$ and $V_H = 8I_B2R_L$. Therefore, to achieve V_{DD} and T independent comparison limits, the resistors R_L are implemented with the serial connection of two resistors, R_P and R_N with opposite temperature coefficients [9]. This is achieved by implementing R_N with a high resistive polysilicon (HRP) layer ($TC_1 = -8.34 \times 10^{-4}$ °C^{-1}, $TC_2 = 1.30 \times 10^{-6}$ °C^{-2}) and R_P with PND, being their ratio that immunizes the resistor against temperature variations $\beta = 1.5$, and the final thermal coefficients $TC_1 = -2.68 \times 10^{-5}$ °C^{-1}, $TC_2 = 9.08 \times 10^{-7}$ °C^{-2}. To generate $V_H = 0.8$ V and $V_L = 0.4$ V, the resistor $R = 100$ kΩ as a compromise between area and power consumption, and it is implemented with $R_P = 60$ kΩ and $R_N = 40$ kΩ.

With V_H and V_L supply and temperature independent, the remaining temperature dependence of the circuit is mainly due to resistor R_S. Therefore, it is implemented in the same way as R_L ($R_{PND} = 16$ kΩ, $R_{HRP} = 24$ kΩ).

This temperature compensation seems to be highly process dependent. However, the value of ten composite resistors ($R_{PND} + R_{HRP}$) have been measured by using a 4-wires technique, obtaining a 0.13 % dispersion between measured resistors with a maximum deviation of 4.1 % with respect to its nominal value, which shows that there is a need of a gain calibration in a fabricated dVFC. The composite resistors were next tested against temperature variations, varying less than 1.6 % over all the temperature range (−40, +120 °C), which proves that the adopted temperature compensation technique is correct. If this technique is desired to be migrated to a different process/technology, the ratio β among two resistors with different temperature coefficients should be recalculated to obtain a composite resistor that exhibits final first and second order temperature coefficients that minimize the temperature dependence.

Note that R_1, R_2, R_3 and R_4 do not need to be temperature compensated neither have accurate specified values because as long as they are well matched their ratio will remain constant. Therefore they are implemented using a HRP layer to optimize area.

2.5 Power consumption considerations

Power consumption is a key parameter in battery operated systems. Therefore, a power reduction technique based on the alternate operation of the comparators is introduced by

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adding transmission gates (as shown in Fig. 4): in the charging phase, the only comparator working is the high comparator whereas in the discharging phase, the only one that works is the low comparator.

In addition, an enable terminal has been included to set the VFC into a low-power mode with 180 nW power dissipation most of the time, waking up just to perform the calibration, frequency measurements and digital conversions, then returning to the sleep mode. The enable acts mainly in the β-multiplier reference circuit to no generate the biasing current and the comparison limits, but it also acts in the first inverter of each of the comparators conforming the VWC, fixing the digital state of each of the remaining inverters.

2.6 Sign circuit

In order to assure the proper operation of the circuit, a sign circuit can be required. It is implemented by means of a rail-to-rail comparator and transistors acting as switches, as shown in Fig. 6. The comparator is made up with an open-loop OTA equal to the one in Fig. 3 but with two complementary differential input amplifier stages in parallel to achieve rail-to-rail performance, followed by inverters. When $V_{in1} > V_{in2}$, $V_C = V_{DD} \equiv$ '1' and $V_{CN} = GND \equiv$ '0', so that T_5 and T_7 are ON and T_6 and T_8 are OFF; therefore, $V_{in+} = V_{in1}$, $V_{in-} = V_{in2}$. Conversely, when $V_{in1} < V_{in2}$, $V_{in+} = V_{in2}$ and $V_{in-} = V_{in1}$.

3 Post-layout results

Figure 7 shows the layout of the proposed dVFC, designed in a low-cost 0.18 μm CMOS technology from UMC with a single supply of 1.2 V. Power consumption is below 60 μW (180 nW in power down) and the active area is 250 μm × 150 μm, dominated by the β-multiplier circuit and the capacitors.

Figure 8(a) shows the variation of the normalized I_B and $V_H - V_L$ over the (−40, +120 °C) temperature range: I_B varies 52.5 pA/ °C while $V_H - V_L$ varies 29.4 μV/ °C. Figure 8(b) shows the variation of the normalized I_B and $V_H - V_L$ over a 1.0−1.4 V supply voltage range. In this case I_B varies 4.5 nA/V and $V_H - V_L$ 11.3 mV/V.

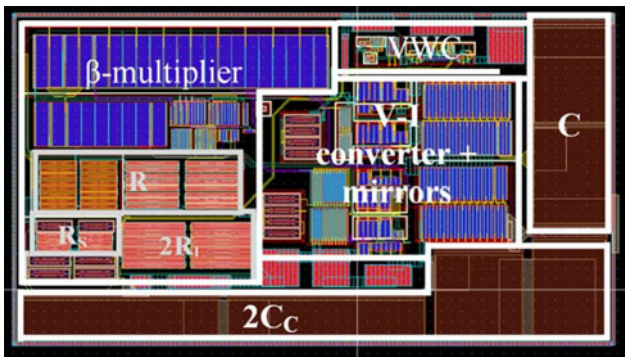

Fig. 7 Layout of the proposed dVFC

There are some errors that define the dVFC linearity: the *gain* or *sensitivity error* is the deviation in slope of the actual dVFC from the ideal one; the *offset error*, which is a constant frequency added to the output frequency, computed as $(f_{0,sim}(V_{in,min}) - f_{0,the}(V_{in,min}))$, expressed in Hz where $f_{0,sim}$ is the simulated value and the theoretical value $f_{0,the}$ is given from Eq. (4); the *relative error*, without offset and gain calibration, computed as $(f_{0,sim} - f_{0,the})/f_{0,the}$; and the main parameter, since it will define the maximum achievable number of bits in the frequency-to-code conversion, is the linearity error, which is calculated as the deviation of a straight line passing through the experimental VFC points. As with most precision circuitry, through adequate calibration processes gain and offset errors can be trimmed by the user in the microcontroller. However, this does not happen with the linearity error, which is inherent to each VFC topology. The linearity error can be thus considered a fundamental parameter, and the smaller the linearity error, the better the VFC. The offset errors are mainly due to mismatching in the OTAs differential pairs as well as to a non-ideal current copy across $T_1 - T_3$, $T_2 - T_4$. Gain errors are mainly due to deviations in the charging capacitor C, in the resistors R_S that converts the differential input voltage into a current and in the resistors R_L that provides the comparison limits V_H and V_L of the VWC, and it is also due to mismatching in the differential pairs of the comparators forming the VWC. Therefore, a calibration with two points can be made in the microcontroller to obtain the experimental gain and offset of the dVFC, thus being able to establish the $V_{in} - f_0$ relationship accurately.

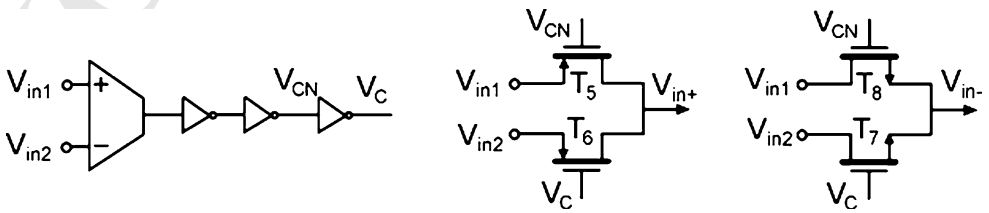

Fig. 6 Schematics of the sign circuit

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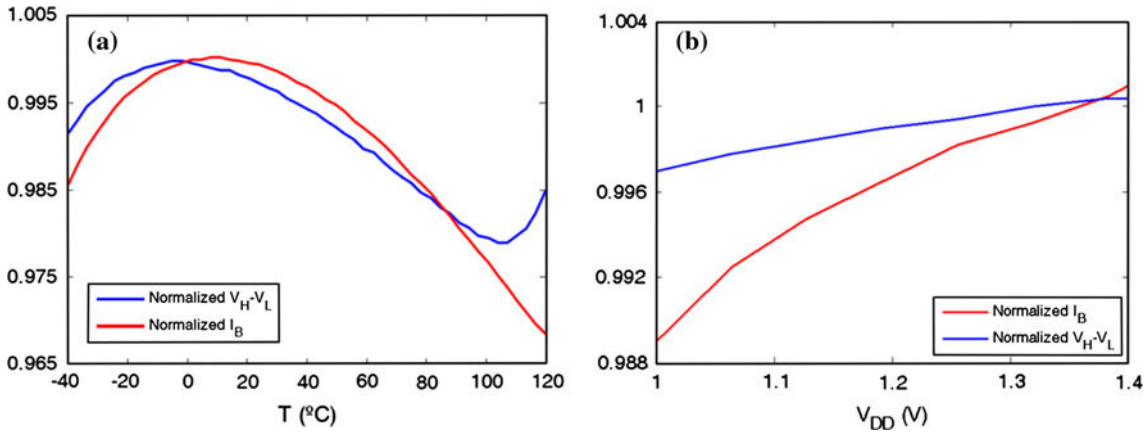

Fig. 8 Normalized I_B and $V_H - V_L$ over **a** (−40, +120 °C) temperature range and **b** (1.0, 1.4 V) supply range

At room temperature, with the nominal supply of 1.2 V and a common mode voltage of $V_{CM} = V_{DD}/2 = 0.6$ V the output frequency varies linearly between 0.0 and 0.9 MHz with a gain error of 2.9 %, an offset error of 2.8 kHz, a maximum relative error of 4.1 %, and a linearity error of 0.002 % for an input range of (0.6 ± 0.6 V).

Figure 9(a) shows the output frequency f_0 over the input range at different temperatures, from −40 to +120 °C, and Fig. 9(b) shows f_0 over the input range for different supply voltages, being $V_{CM} = V_{DD}/2$.

Over all the (−40, +120 °C) temperature range, the maximum gain error is 4.5 %, the maximum offset error is 3.1 kHz, the maximum relative error is 8.7 %, and the linearity error remains below 0.014 %. When the system is simulated for 30 % supply voltage variations (1.2 ± 0.2 V), the input range varies accordingly; however, the errors remain bounded: the maximum gain error is 6.1 %, the maximum offset error is 3.8 kHz, the maximum relative error is 8.9 %, and the linearity error remains below 0.005 %. In the worst case ($V_{DD} = 1$ V, $T = -40$ °C) the linearity error remains below 0.017 %.

The system has also been tested against $V_{CM} = 0.6 \pm 0.3$ V variations at the nominal $V_{DD} = 1.2$ V supply voltage. The frequency remains nearly constant with a maximum variation of 0.4 % with respect to the frequency at $V_{CM} = 0.6$ V.

A Monte Carlo analysis has been carried out varying in 3σ the process and mismatch foundry models in order to see the effect of mismatching. For 20 iterations, and over different single and differential input voltages, the variation on the output frequency is on average 3 %, mainly due to variations on the generated current across R_S.

The main performances of the proposed dVFC are compared in Table 1 with the few dVFCs encountered in the literature [5, 6]: exhibit a rather limited input range, larger errors, higher power consumption and they operate at higher supply voltages. The proposed dVFC is based on a preliminary design previously reported by the authors [10], however the newer and depurated version of dVFC exhibits a lower power consumption as well as a reduced area because: (i) it uses OTAs with single differential pairs instead of rail-to-rail OTAs, (ii) due to the common mode voltage at nodes V_1 and V_2, the current across feedback

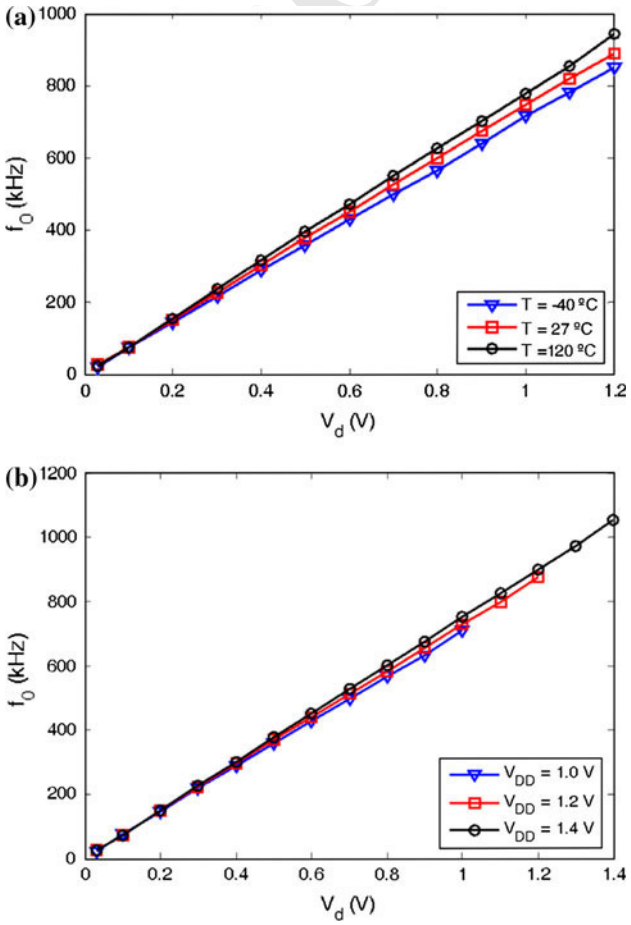

Fig. 9 Output frequency vs. differential input voltage for **a** (−40, +120 °C) temperature range and **b** (1.0, 1.4 V) supply range

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Table 1 Comparison of dVFCs

Parameter	[7], 2010	[6], 2011	This study
Technology	Commercial devices	0.18 µm CMOS	0.18 µm CMOS
Supply voltage (V)	±5	1.8	1.2
Sensitivity (kHz/V)	75	861	750
Input range	0.2 V diff (0.0 ± 0.1 V)	1.2 V diff (1.2 ± 0.6 V)	Full range (0.6 ± 0.6 V)
Relative error (%)	<5[1]	–	10.4[2]
Linearity error (%)	–	0.4[1]	0.014[2]
Power consumption (µW)	–	375	60

[1] Nominal

[2] For 30 % V_{DD} variation and (−40, +120 °C) temperature range

resistors R_1, R_2, R_3 and R_4 is halved, (iii) the charging and discharging currents are obtained directly from the V–I converter without using current mirrors. In addition, this dVFC keeps the common mode voltage V_{CM}, therefore maintaining the same operating conditions for the OTAs. As a conclusion, the proposed dVFC offers high performance characteristics with a compact design.

4 Conclusions

A simple compact 1.2-V 0.18-µm CMOS differential voltage-to-frequency converter has been presented showing improved characteristics over the state-of-the-art converters for low-power sensor interface electronics. This rail-to-rail dVFC exhibits low temperature and supply sensitivity, featuring competitive performances with other low-voltage low-power counterparts. The sensitivity and start frequency can be easily tuned.

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Journal : Large 10470 | Dispatch : 13-6-2013 | Pages : 9
Article No. : 98 | ☐ LE | ☐ TYPESET
MS Code : ALOG-D-12-02599 | ☑ CP | ☑ DISK

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