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Trabajo Fin de Grado

Diseño de ondulador de 1kW para alimentación de maniobra de ascensor desde baterías de 48V

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TRABAJOS DE FIN DE GRADO / FIN DE MÁSTER

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Escuela de Ingeniería y Arquitectura Universidad Zaragoza

Diseño de ondulador de 1kW para alimentación de maniobra de ascensor desde baterías de 48V

Summary

The inverter currently used by the enterprise Epicpower, spin-off from the University of Zaragoza is directly purchased in the market. The focus of the enterprise till these days has been the development of the energy recovery and single-phase systems for elevators but now, the reduction of the cost of the different elements in the system is a matter of higher importance. A conclusion about the cost and viability of a valid self-designed manufactured inverter must be obtained from this report.

The aim of this TFG is then to design a 230Vac/ 800W (the power needed due to recent test would be smaller) inverter fed by a module of 4 batteries of 12V each

This inverter would be included as an additional product or integrated in the current equipment, therefore it must meet the applicable normative as well as getting a reduce size and price. The design will be complete and references of the components, thermal dissipation modeling, etc… will be included as well.

The task for this inverter will be the feeding of the lift-controller, door-operator, lights… getting the energy stored in the batteries upstream. In the following sections further information about the whole equipment operation will be included in order to understand all the additional processes.

Plecs is the software that has been used to run the simulations, it is included in Matlab/Simulink which has been used as well. From their usage, the measures and waveforms shown in this report as well as comparisons and designs have been obtained.

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1. Introduction

Nowadays, one of the systems developed by the company Epic Power, spin-off from the University of Zaragoza, is carrying with the function of completely feeding an elevator from a single-phase mains instead of the traditional three-phase one.

To have a little overview of the system and clarify the place and importance of the device studied, the P2S is introduced.

P2S (Plug to Single-phase) is a system whose main aim is to avoid the three-phase mains installation in case of placing an elevator in a new building or reducing the hired power in case of an already existing one.

This equipment developed by the company just needs to get connected to the DC bus into any VVVF (Variable Voltage Variable Frequency drive) in the market to be able to feed the drive that feeds the motor. As it can be seen in Fig. 1, the equipment have several input power sources and one output. The inputs are the standard single-phase mains that can be found in any building with standard electrical installation and the solar panels in case of addition.

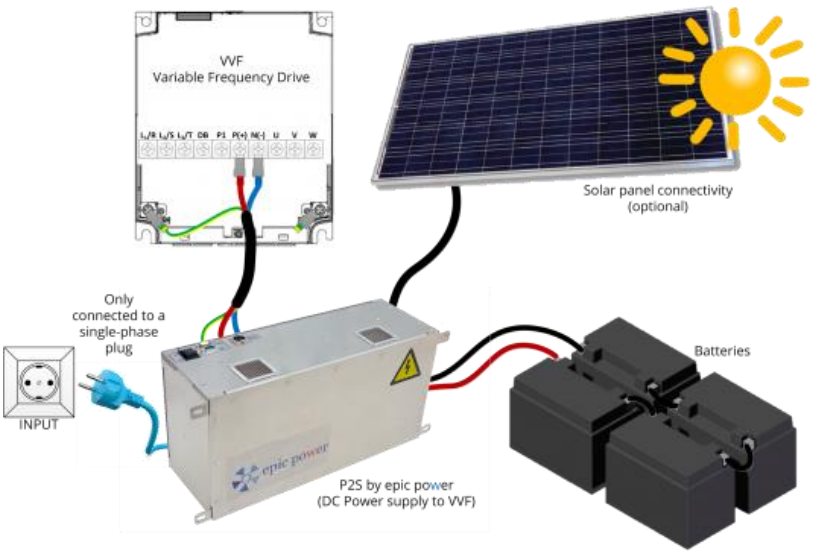

Fig. 1 System P2S by EPIC POWER

The batteries act as energy buffer receiving energy from a battery charger (500 W) connected to a standard socket. This charger keeps charging while the batteries are not full and there is not enough sun irradiation to charge the batteries only from the solar panels. Also, batteries can receive energy from the motor during regeneration trips (an elevator going down with people or going up empty).

When there is an energy demand the energy sent to the drive, after a boosting operation made in the DC/DC converter, is provided from the batteries.

The energy from the batteries is quite enough to, depending on the elevator characteristics, feed the motor and the maneuver for 100 trips in case of blackout. Then, apart from using the energy buffer as a UPS saving system, it feeds the maneuver of the elevator getting an autonomous system with only a single-phase mains.

This maneuver comprise the door operation, lights and panels feeding, buttons, alarms… All these subsystems have to be fed from a single-phase 230 Vrms voltage so this amplitude must be obtained somehow. As the system is thought to be able to supply the energy also in case of blackout, these subsystems cannot be connected directly to the single-phase mains but to the battery energy buffer through a DC/AC converter.

There is where the power inverter of the study enters. A DC/AC high efficiency low-cost power inverter from the 48VDC (approximately) voltage of the batteries to the 230 Vrms voltage output is needed.

Along the report, several designs will be considered. In the state of the art section four possible designs will be presented and evaluated. Only two of them will be selected for a deeper study that contains the sizing of the components, simulation, selection of components losses calculation and overall cost. Finally, methods of control, measuring and a final summary in Spanish are presented.

1.1. Objectives

The main objective of this project is to obtain an inverter for AC module applications by studying different possibilities already developed. The target is to get a new and cost-effective solution for injection of electrical power, obtained by the P2S system and saved in modules of batteries, into the lift maneuver operation.

The inverter has to be designed with low-cost and high reliability in terms of applicable normatives and requirements. Also, certain degree of integration should be obtained in the resulting device in order to include it in a limited space.

1.2. Requirements

The inverter built will have to accomplish certain requirements in order to work properly with the other devices connected. Therefore normative conditions will be taken into account in terms of harmonics and high-frequency response.

The output obtained from the inverter has to show a sinusoidal wave-form of 230 Vrms, 325 Vpeak, approximately. Also, the power the inverter has to supply is 800 W at maximum although at the beginning it was expected to be 1kW (changed to 800 W due to recent tests). The standard power of the inverter at steady state shouldn't be over 400W so the design of the circuits could be even more restricted.

As the voltage in the batteries will have a value of approximately 48-50V, the boost needed to get the 325 Vpeak at the output of the topology will be around 6.7 times the input value. Since the voltage difference is quite important it has been decided that a transformer would be used.

Owing to the variable load the inverter has to feed, reactive energy must be allowed inside the circuit. Besides, the overall efficiency of the inverter was decided to be over 90 %, so the amount of switching, conduction, iron and cooper losses should be quite small.

1.3. Normative

The normatives that set the bases of market and commercial requirements that has also been used for the design are shown below:

- UNE-EN_55016-1-1: "*Especificación para los métodos y aparatos de medida de las perturbaciones radioeléctricas y de la inmunidad a las perturbaciones radioeléctricas. Parte 1-1: Aparatos de medida de las perturbaciones radioeléctricas y de la inmunidad a las perturbaciones radioeléctricas*".This normative introduces methods and measuring tools for radio electric perturbations and radio electric perturbation immunity. The implementation from this normative is the bandwidth used for the fft spectrum in high-frequency.

- UNE-EN_50160: "*Características de la tensión suministrada por las redes generales de distribución*". Low-Voltage feeding characteristics, generalities, continuous happenings and voltage events.

- UNE-EN_61000-3-2=2006: "*Compatibilidad electromagnética (CEM), Parte 3-2: Límites para las emisiones de corriente armónica (equipos con corriente de entrada ≤ 16 A por fase)*". Current harmonic limits for class A systems with incoming current less than 16A per phase.

- UNE-EN_55014-1=2008: "*Compatibilidad electromagnética. Requisitos para aparatos electrodomésticos, herramientas eléctricas y aparatos análogos. Parte 1: Emisión*". Perturbation limits and application methods for bandwidths from 150 kHz to 30 MHz.

2. State of the art

To introduce the device that will be studied along this report the following definition is provided. A power inverter, or inverter, is a device that changes the direct current (DC) to alternate current (AC).

This change from DC to AC is obtained basically by switching some transistors in a specific way and timing. After that a filter is included in order to get the specific waveform and frequencies desired at the output.

Nowadays, inverters are widely used in photovoltaic applications. Photovoltaic cells are able to generate DC electric current when sunlight irradiates them. The solar market has increased exponentially in the last few years and then also the inverter development. Being the solar energy treatment the most extended application for the inverters nowadays, they can be used in other applications like uninterruptible power supplies (from batteries), electric motor speed-control and even Tasers.

A typical inverter requires a relatively stable DC power source capable of supplying enough current to fit the power demands of the system, then the first requirement for the source of the device has been set. This input source has to provide enough current but also a specific voltage. Depending on the application it is possible to find inverters of 12 VDC for smaller consumer inverters, 24 and 48 VDC for home energy systems, 200 to 400 VDC for input power of photovoltaic solar panels and 300 to 450 VDC when power is from electric vehicle batteries.

Now that a little overview of the device and its applications has been introduced, a first approach of the different possible inverter designs will be presented.

2.1. The DC/AC/AC design

The conversion from DC to AC at the low-voltage side is performed mostly in applications where high level of boosting is required since an AC boosting (via a transformer) is much more efficient than a DC one.

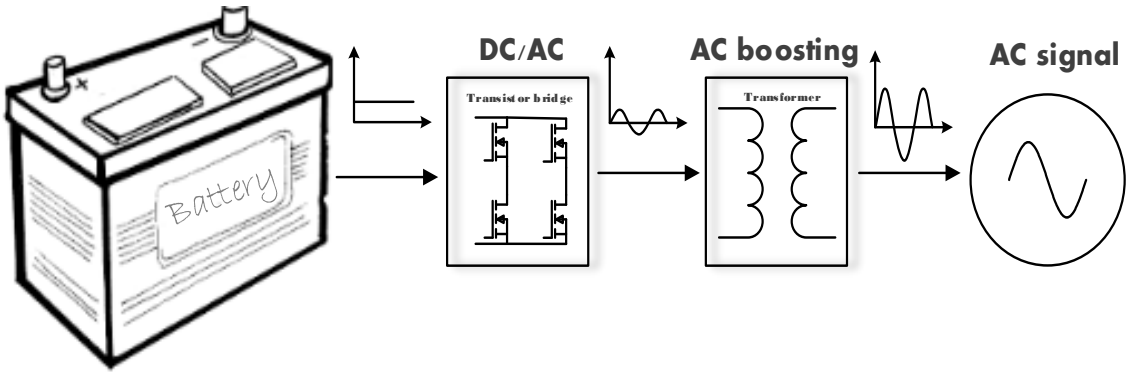

Fig. 2: DC/AC/AC design

Depending on the control performed to the transistor bridge, different waveforms at the output can be obtained.

Fig. 3: DC/AC/AC inverter, shown below depicts the function of the different parts of the circuit. The DC voltage from the batteries is switched at the DC/AC stage, then filtered and finally boosted via a transformer. It is quite a simple topology but the desired response depends very much on the switching process.

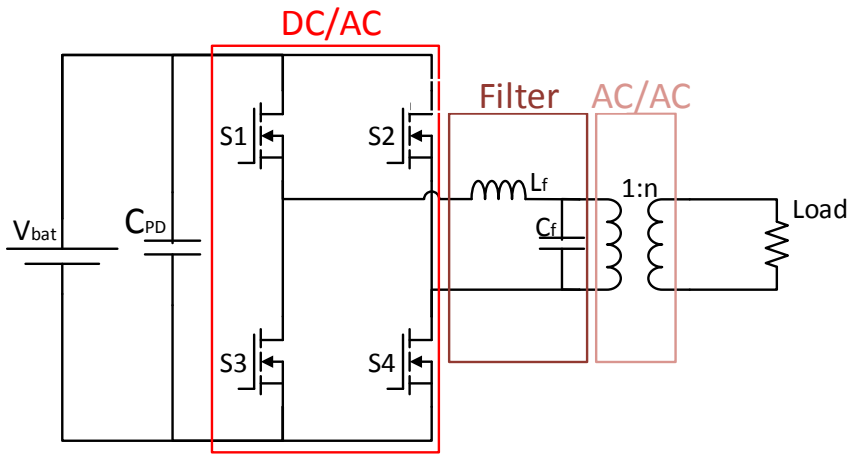

Fig. 3: DC/AC/AC inverter

As mentioned before, this kind of topologies tolerate several switching controls. The ones explained below and considered will be the multi-level and the PWM control.

2.1.1. Multi-level control

This control is performed at the line frequency. The simplest way of switching the devices would be to turn on and off both S1 & S4 (and S2 & S3 turn off and on) to obtain a square voltage wave at the output of the bridge.

S1	S2	S3	S4	V_{ab}
1	0	0	1	V
0	1	1	0	-V

Table 1: Square wave control

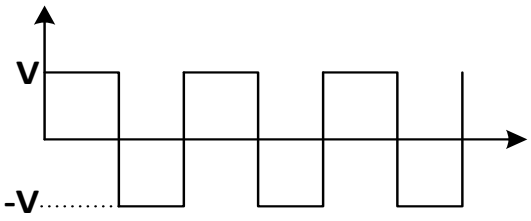

Fig. 4: Square wave voltaje

Nevertheless, the filter needed in this case would be quite big since it has to filter to a 50 Hz sinusoidal form of just two voltage levels V and -V.

Taking care of the control of each one of the switching devices, it is possible with four transistor to obtain a three-level output. The three levels will be the extreme levels V and –V and zero as it is shown in Fig. 5 . This control requires just a bit more of simply programing/control and offers a much better response of the desired output.

The more devices included in the bridge, the more variables to control, the more levels obtained. This way it can be obtained, a multi-level AC voltage that approaches quite a lot to a sinusoidal wave (very small THD). However, the control implementation in the DC/AC/AC topology has been the three-level configuration because of the use of just 4 transistors and the closer approach to a sine than the square one.

S1	S2	S3	S4	V_{ab}
1	0	0	1	-V
1	1	0	0	0
0	1	1	0	V
0	0	1	1	0
0	0	1	1	0

Table 2: Three-level switching control

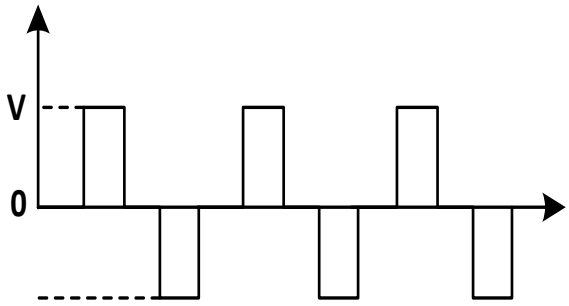

Fig. 5: Three-level AC

Then with this control the waves that can be seen in the DC/AC/AC design are depicted in Fig. 6.

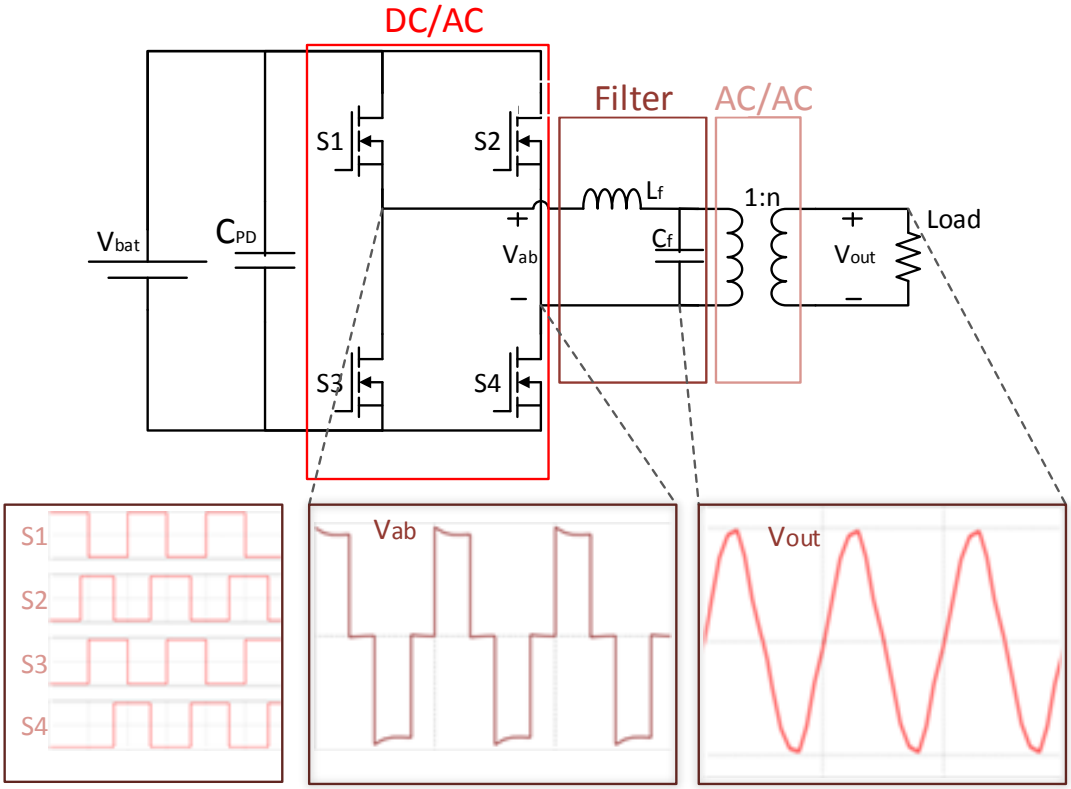

Fig. 6: Three-level waves, DC/AC/AC converter

2.1.2. PWM control

With the PWM control, the switching of the transistor is done at high frequency. Depending on the modulation factor selected, for this application, the switching frequency can be over 350 times the line frequency. That makes the accuracy of the voltage output wave obtained pretty close to a sine wave.

The standard PWM (bipolar) and unipolar PWM have been tested. Simulations have been performed with the unipolar one because of the fact that it improves the emission response. In the unipolar PWM, the odd harmonics (n1, n3, n5…) of the triangular wave (at the switching frequency) turn out annulled.

This control requires one more reference signal to compare the triangular wave and obtain the switching timings for the transistors but it worth when the achievement of normative is an important matter in the design.

Below, in figure Fig. 7, several waves in the circuit with the unipolar PWM control are depicted:

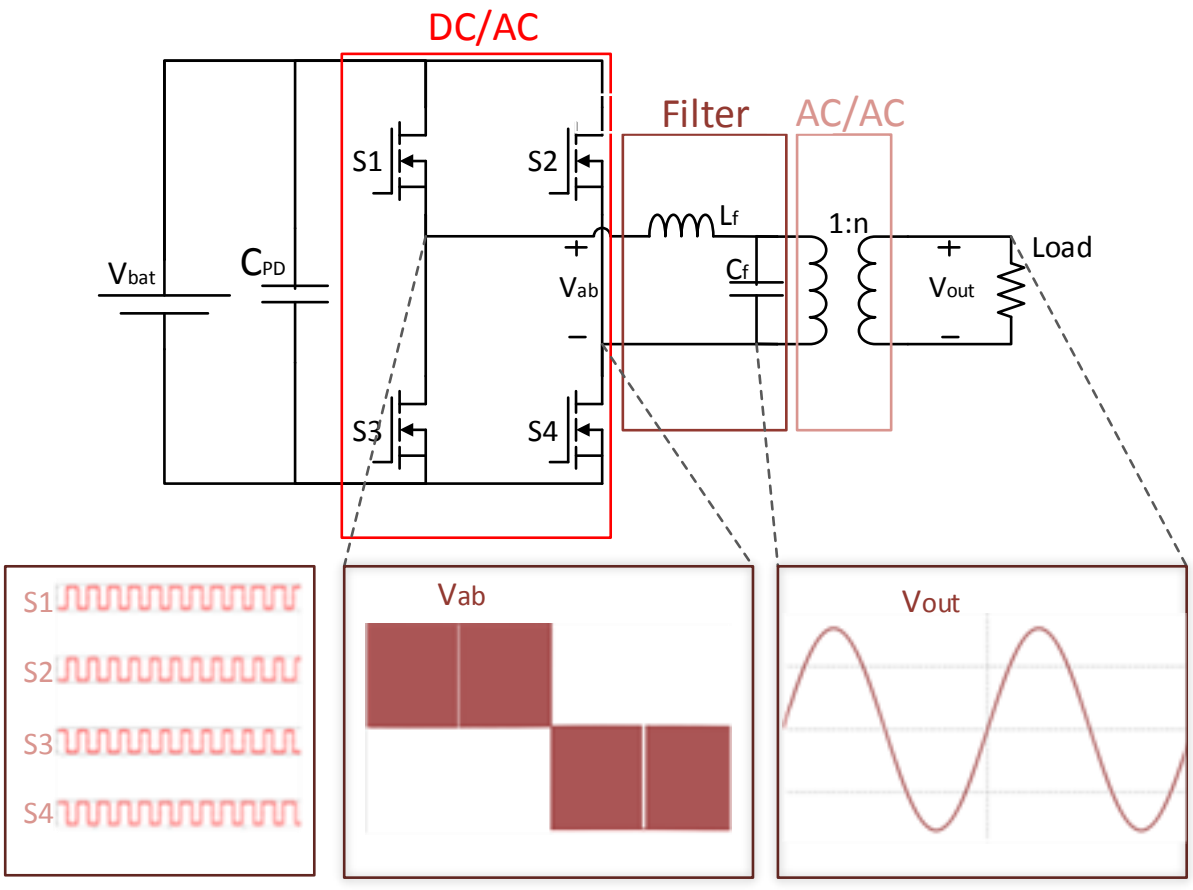

Fig. 7: Unipolar PWM waves, DC/AC/AC converter

2.2. The extended fly-back (differential DC/AC)

A similar basis to the DC/AC inverter explained in the previous section 2.1, is the one depicted in Fig. 8:

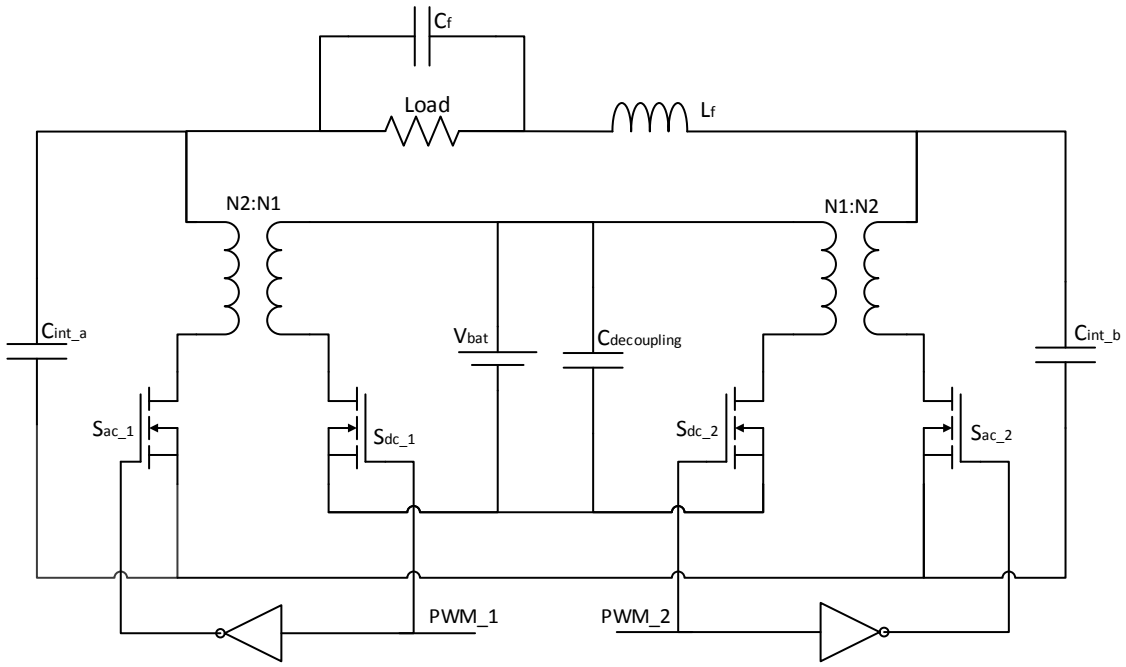

Fig. 8: Extended fly-back inverter (DC/AC design)

As the DC/AC design of section 2.1, the extended fly-back inverter is a design with a single stage. The transistor at the DC source side (primary of the transformer) turns on and off according to the PWM signal that feeds the control. The one at the secondary of the transformer does the opposite.

The inverter operates in Continuous Conduction Mode (which means that the current going through the magnetizing inductance in the transformers never arrives to zero).

The operation of this topology works as follows: The inverter generates an AC voltage across its output terminals by modulating two sinusoidal voltages across the intermediate capacitors (C_{int_a} & C_{int_b}) with a 180º displacement with respect to each other.

$$v_{C\_inta} = V_o + \frac{\hat{V}_{Load}}{2} \cdot \sin(\omega \cdot t) \qquad (1)$$

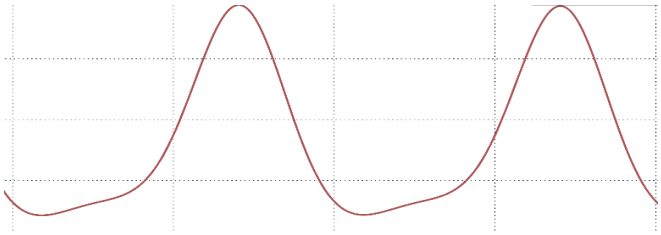

Fig. 9: Voltage, v(t) of intermediate capacitor a

$$v_{C\_intb} = V_o - \frac{\hat{V}_{Load}}{2} \cdot \sin(\omega \cdot t) \qquad (2)$$

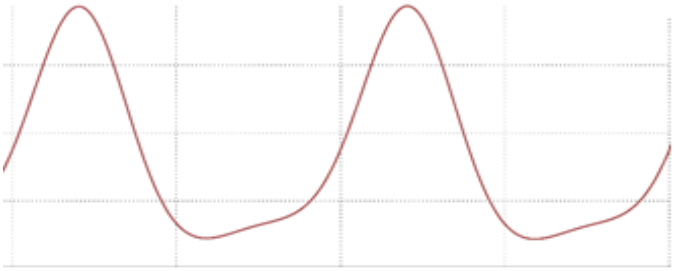

Fig. 10: Voltage, v(t) of intermediate capacitor b

$$v_{Load} = v_{C_{inta}} - v_{C_{intb}} = \hat{V}_{Load} \cdot \sin(\omega \cdot t) \qquad (3)$$

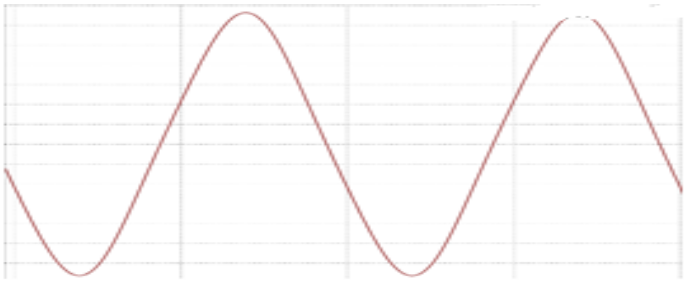

Fig. 11: Output voltage, Vint_a-Vint_b

The good point of this design is that the turn relationship for each one of the transformer would drop to half because of the differential mode of operation between the capacitor voltages. The operation would be at high frequency.

Since each one of the intermediate capacitors must have big capacitance in order to obtain a decent sine voltage waveform, the current demanded would be quite elevated and provided by the batteries.

For these reasons, the losses in the switching devices would be high and the efficiency would drop to low levels (one of the requirements was to obtain an inverter with over 90 % of efficiency).

2.3. The DC/DC/AC design

As an alternative option to the DC/AC design, the DC/DC/AC design is presented. There is also another option explained in section 2.3.2 that can be consider as a DC/DC/AC design but it does not contain a continuous DC bus inside the circuit.

2.3.1. DC boosted bus

The DC bus design is an alternative to the DC/AC low voltage conversion. It consist on a DC/DC converter that boost the voltage from the source to the desired level, in this case it would be a bus of around 350 V.

The operation of the design and an overview of its stages is depicted in Fig. 12.

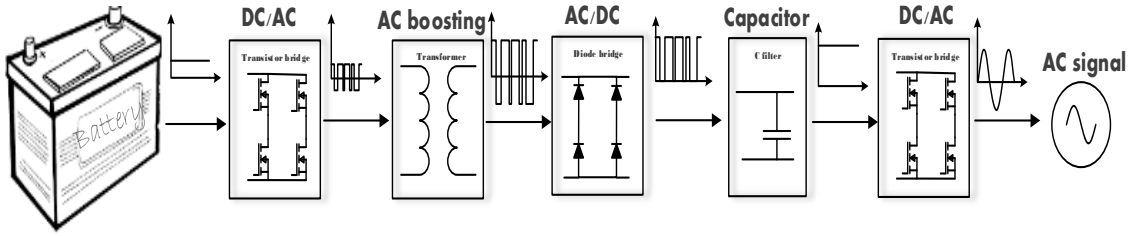

Fig. 12: DC/DC/AC bus design

This design has not been further studied because of its multi-stage condition which increases the cost and because of the efficiency it can be obtained with IGBT from an inversion at high voltage and frequency. That could be solved including silicon carbide transistors which introduce small $R_{DS_{ON}}$ and make possible the switching under this environment but the cost would be tremendous. Nevertheless, the bus hold by the capacitor could operate very much with an inductive load, so reactive energy would not be a problem anymore.

2.3.2. DC/AC/DC/AC design

This topology bet for the maintenance of a DC full-wave voltage signal inside the circuit. It makes necessary the inclusion several stages that will be performed by efficient devices. Due to its multi-stage condition, this circuit requires more number of elements.

A first approximation to the waves of the topology and its operation is depicted in Fig. 13:

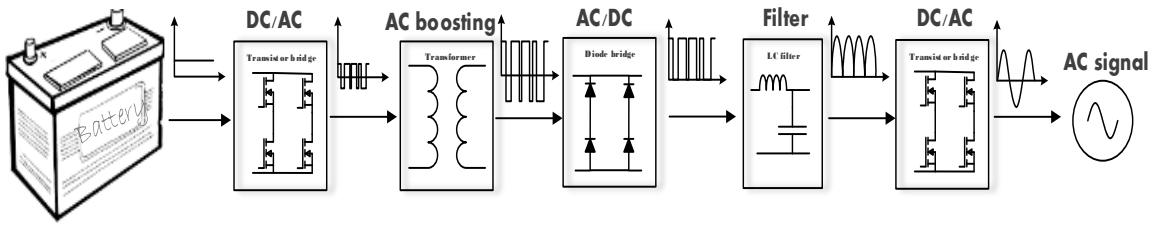

Fig. 13: DC/AC/DC/AC design

As the AC boosting is performed by a transformer, it would be interesting to make the transformer operate at high-frequencies to increase the efficiency. Then, the control for the first bridge of transistors must be one in which the output obtained assures that the medium voltage along the switching time is zero.

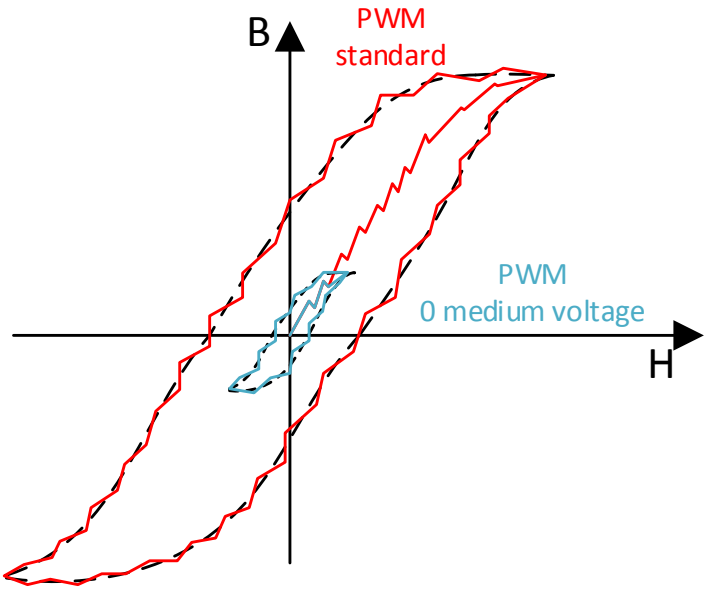

Fig. 14: Transformer magnetic field

If the magnetic field inside the transformer is small, the slope of the line obtained from the magnetizing relation B/H approaches to the axis and make possible the increase of the operating frequency in the transformer. As it can be seen in Fig. 14, the PWM built with a zero medium voltage (in blue color) is able to reach this condition. Nevertheless a standard PWM (either bipolar or unipolar), in red, increases the field since not a medium voltage along the switching frequency is supplied.

Then a variable-phase (further explained in section **¡Error! No se encuentra el origen de la referencia.**) PWM is used for this application to obtain a control modulation of 0 medium voltage along the switching time.

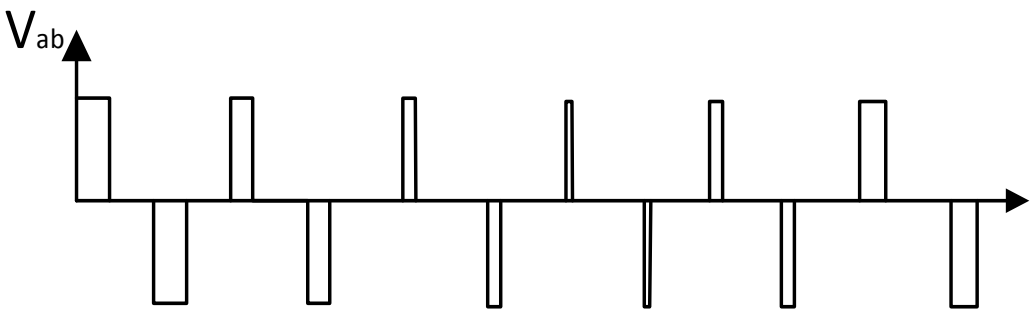

Fig. 15: Variable-phase PWM

The Fig. 16 shown below, depicts the function of the different parts in the circuit. Basically, the DC voltage is converted to AC, boosted by the transformer and converted again to DC. This second conversion leaves the voltage in a full-waveform in order to need just a rectification made by the second transistor bridge.

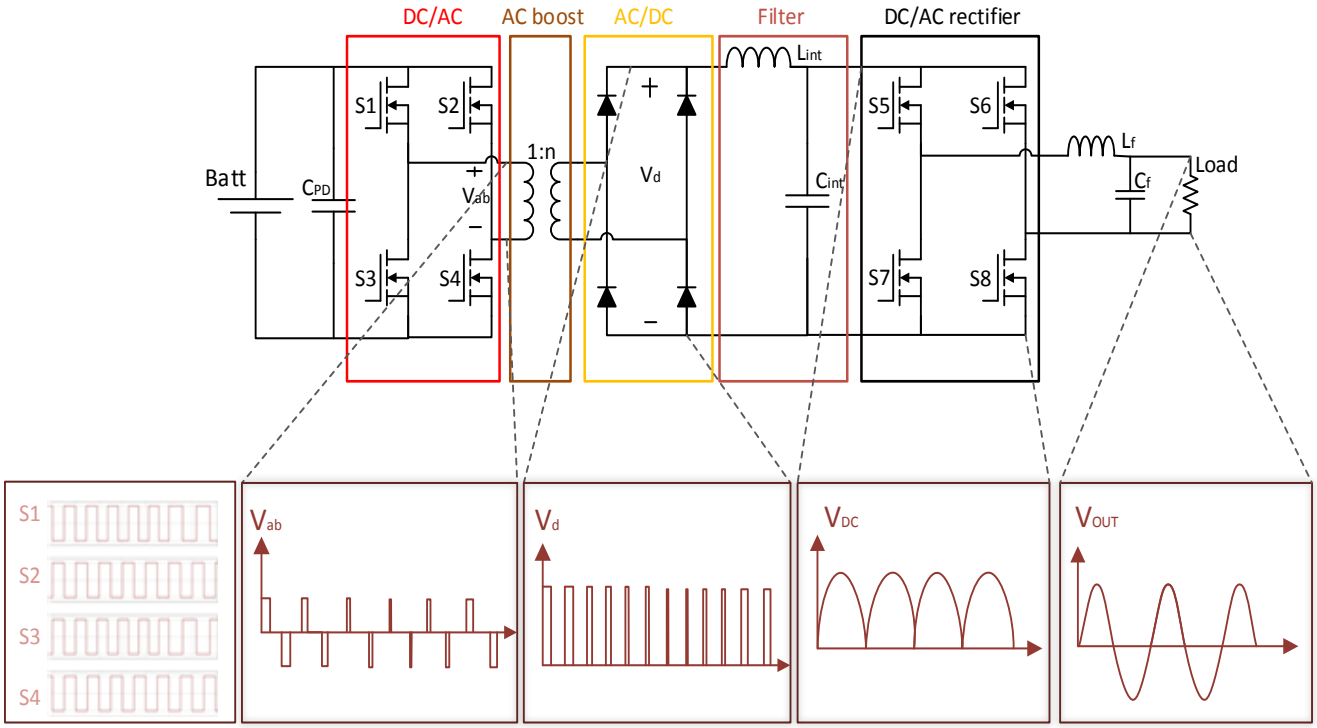

Fig. 16: DC/AC/DC/AC inverter

Then, the first DC/AC commutates at high-frequency (in this application should be enough with 20 kHz). The transformer also changes its polarity every switching cycle so the efficiency will be higher than in a laminated one of low switching frequency operation. Then it is converted to DC again through the diode bridge and filtered to obtain a full wave via the intermediate filter. The last operation is the rectification of the full wave in order to get the desired sine voltage wave.

The good point of this topology is that the filter used can be designed smaller than in the DC/AC design. So the viability of this multi-stage topology will be studied later in the report.

2.4. Conclusions

In the state of the art section, a summary of the different available and most common designs for inverter has been made. Those designs are mostly used in photovoltaic applications, where the power inverter market grows. A small overview of four different DC/AC designs operation has been presented in order to select the most suitable for the application.

Control, waves and operation of each design has been introduced in order to obtain a conclusion of each design about the necessity of a further study or not.

The DC/AC/AC design introduces an inverter that allows several controls for the switching devices to conform the wave. Either a multi-level or PWM control can be implemented. The PWM controls offers a better chance to approximate the most to a sine form without a big filter. Besides, reactive energy is allowed inside the circuit so a high reliability is assured. The drawback would be the line frequency transformer that would reduce the efficiency and increase the cost.

In the DC/AC extended flyback alternative, the turns relation of the transformer can get reduced to half because of its differential voltage obtaining. The control, PWM, is delayed 180 at each branch to build the differential wave. The drawback of this topology is the current demanded by the intermediate capacitors from the batteries because of their size. That causes a drop of the overall efficiency of the topology.

The alternative design with an intermediate DC bus, shows the most intuitive inverter. It is basically a DC/DC converter followed by a high voltage inverter. The good point of this design is the reliability, in terms of reactive energy. However, the inversion at high voltage and frequency with standard technology (IGBT) is not very efficient and other more expensive devices must be used to obtain a good performance.

The DC/AC/DC/AC design share the circuit with the previous design but with an intermediate inductor included. That makes appear a full voltage wave inside the circuit that is easy to rectify. This topology offers a high efficiency performance and relatively low cost. However, the reactive energy allowed is limited because the intermediate capacitor (voltage changing) is the one holding the energy.

Having all that in mind, the selected topologies for a deeper study have been the DC/AC/AC and the multi-stage design. Both topologies offer at first sight high efficiency and good quality performance.

3. Selected topologies design

Taking into account the conclusions obtained in the previous section, two topologies are going to be designed, the DC/AC and the multi-stage inverter. For each one of the topologies, the turn relationship for the transformer, the LC filter, the output obtained as well as the comparison with normative limits are going to be carried out in order. Then, the selection of the components and the efficiency of the topology will be discussed to finally obtain an overall cost of the design.

The switching frequency will be 18 kHz for the DC/AC, 20 kHz for the multi-stage design and the battery voltage 48 V for both. The load is the one specified by the power and voltage requirements at the output.

$$\text{Load} = V_{rms}{}^2/P_{max} = 230^2/800 = 66{,}125\ \Omega \qquad (4)$$

3.1. DC/AC (PWM control) inverter

This is one of the basis and more reliable designs for an inverter. It has not many elements so the cost would be relatively low.

Because the load may not be always pure resistive, the circuit had to allow and have any measure to treat reactive energy. That is reached with this topology since it could be returned to the source.

This design is depicted in Fig. 17.

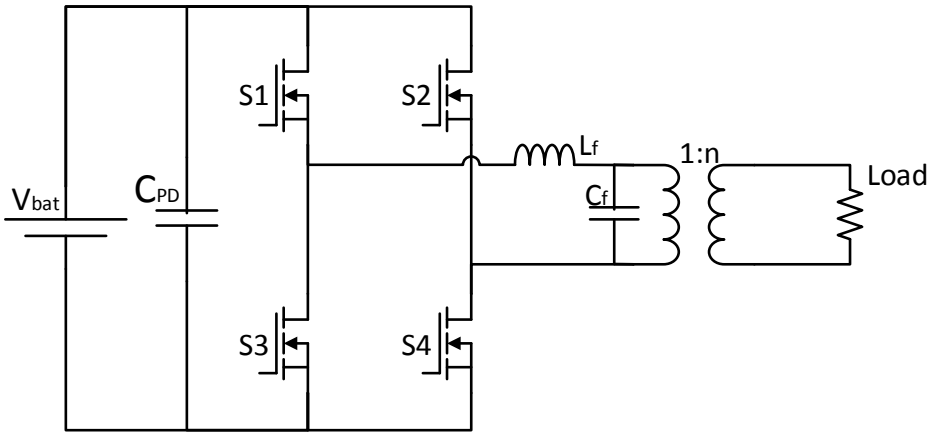

Fig. 17: DC/AC (PWM control) inverter

According to the specific RMS voltage of 230 Vac desired at the output and its sine shape form, the peak voltage value should be close to 325 V, then the turn relationship for the transformer should be:

$$Tr = \hat{V}_{Load}/V_{Bat} = 325/48 = 6{,}77 \approx 6{,}8 \qquad (5)$$

This is an approximate value and it should be checked with the real elements of the topology. This simple equation above is made without taking into account the voltage drop across the transistors which depending on the selection could be high.

3.1.1. LC filter calculation

The LC filter is designed to treat the boosted PWM voltage wave to get a 50 Hz one. Then, the smallest values for these elements should be obtained in order to reduce the cost. As the PWM works at 18 kHz, which is 360 times the line frequency, the voltage wave obtained after the conversion to AC easily filtered with a relatively small LC structure.

The cut frequency for the filter should be down to, at least, half the switching frequency, 18 kHz.

$$f_c = \frac{1}{2 \cdot \pi \cdot \sqrt{L_f \cdot C_f}} \qquad (6)$$

So, considering $f_c = 9kHz$, the LC product should be:

$$L_f \cdot C_f = \left(\frac{1}{2 \cdot \pi \cdot f_c}\right)^2 = \left(\frac{1}{2 \cdot \pi \cdot 9\ kHz}\right)^2 \geq 3{,}12 \cdot 10^{-10} \qquad (7)$$

In this case the provisional values that has been taken due to output results and normative comparison are:

- L=30 µH
- C=33 µF

$$L \cdot C = 9.9 \cdot 10^{-10} \longrightarrow f_c = 5\ kHz$$

A more accurate approximation could be made making a deeper study of the limits of high frequency emissions.

3.1.2. Simulation

In this section, the response of the design needed to confirm whether the requirements are reached or not is performed. If all the elements are well dimensioned, the waveform at the output should be a sine with a small ripple. Additionally high and low frequency limits should be as well over the output specter measures at both ranges of frequencies.

3.1.2.1 Output

Using values, from the previous calculation sections in software PLECS simulation, it is simple to model an approximate the behavior of the topology.

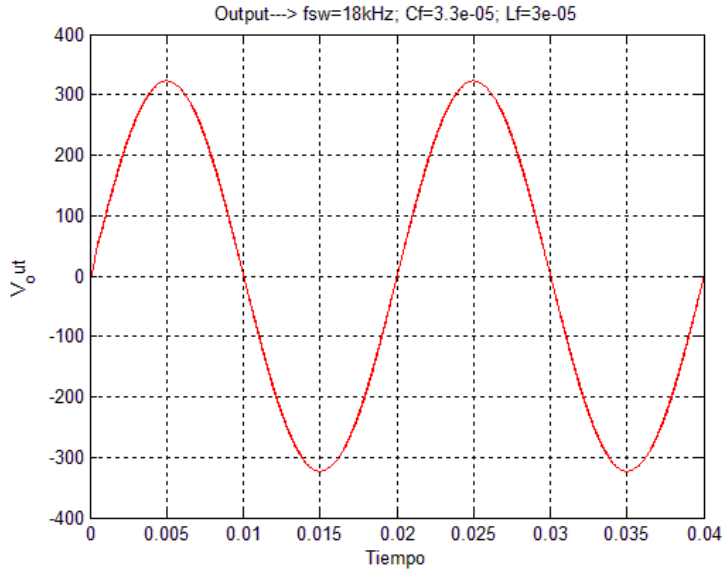

Fig. 18: DC/AC inverter output

The period time of the output wave rests at the desired period, 0.02. Also, the Vpeak is very close to 325 V, the desired voltage level. It has an observable ripple that is manifested at high frequencies.

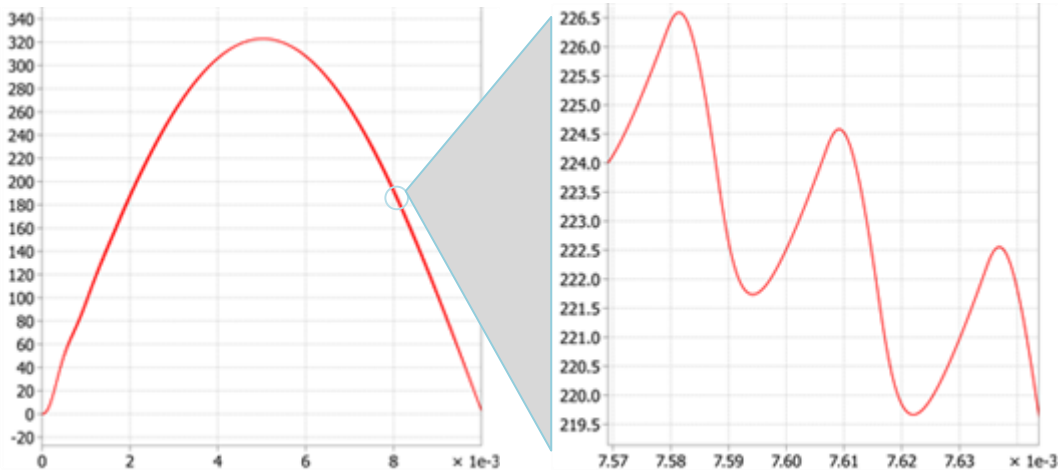

Fig. 19: Output ripple zoomed

What is seen at the zoomed part of Fig. 19 is a maximum ripple of 5 V. This ripple has to be checked with the normative to assure that is included inside the allowable range of high frequency operation.

This ripple appears at 36 kHz which is double the frequency of switching. Because of the unipolar PWM control at 18 kHz that is applied to the bridge, the harmonics that appears at the output will be the even ones. The unipolar PWM feature makes that the odd (and around) multiple harmonics of the saw-tooth signal (switching frequency, fsw) get annulled, then only the even ones appear (36 kHz, 72 kHz, 108 kHz…).

Although the existence of this high frequency ripple, the expectance for low-frequency response is valid. It will be shown in Fig. 20 where a representation of harmonics up to 2 kHz is performed.

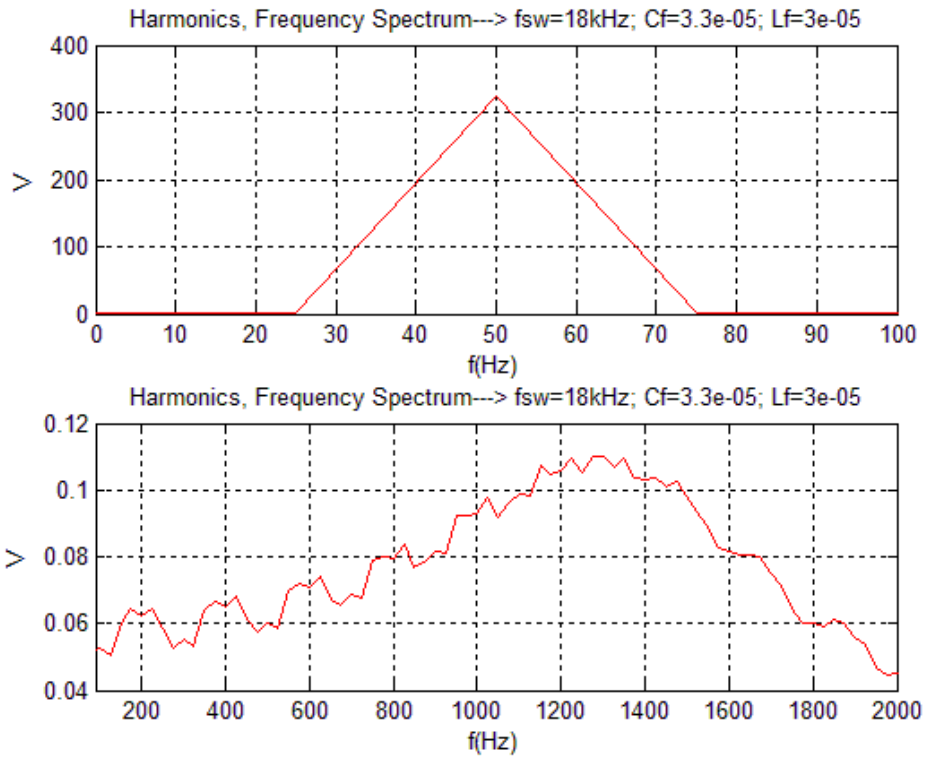

Fig. 20: DC/AC Harmonic response

At the line frequency, 50 Hz, there is a peak voltage of 322V, very close to 325 V, the desired peak voltage. All the other frequencies up to 2 kHz have an amplitude down to 0.5 V. Then, the output low frequency performance should achieve the low frequency normative.

3.1.2.2 Comparison with normative

The normative for low frequency (UNE-EN_61000-3-2), specify the limits of receiving harmonics by the elements that hold downstream the power inverter which is being designed, then these are the maximum amplitude values considered as valid.

Below in Fig. 21, the limit in volts for each one of the line frequency harmonics is painted in blue facing the current frequency specter response.

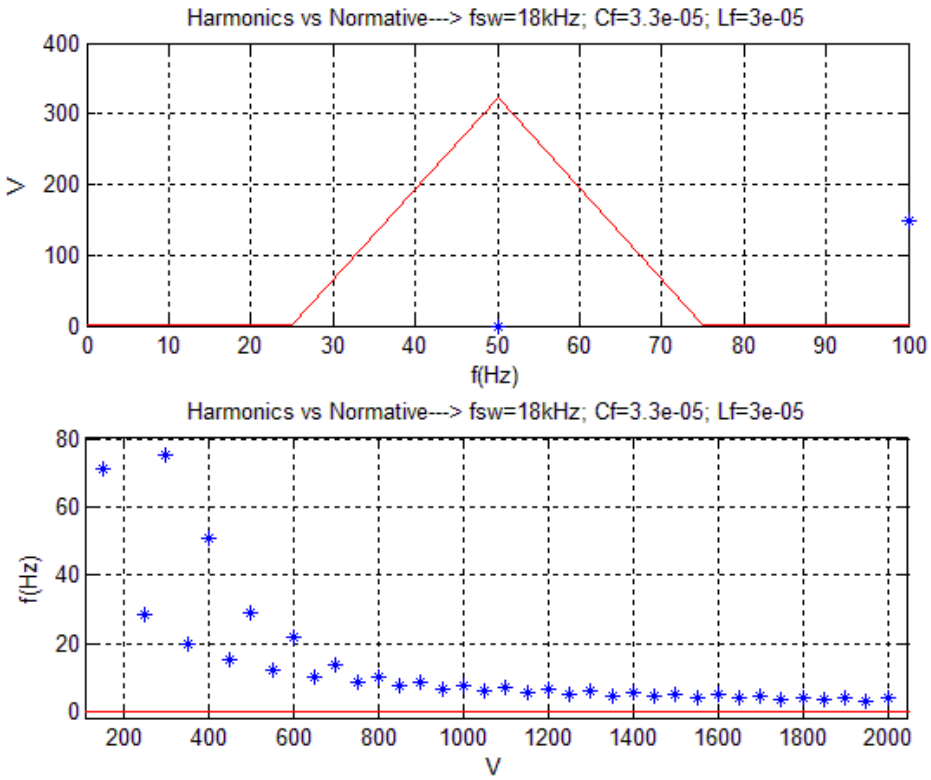

Fig. 21: DC/AC Harmonic vs Normative response

It's important to notice that using unipolar PWM control at 18 kHz make this result very much likely than in case a three-level switching control is used. That is because of the number of switching per period time, 360, that builds a very accurate sine. The real challenge then, is to achieve the response normative requirements for high frequencies since increasing the switching frequency generates harmonics at higher frequencies.

In terms of high-frequency harmonics / emissions, a LISN (Line Impedance Standard Network) circuit has been placed to make the measure. It has been place along the whole simulation stage but at low frequencies it is innocuous to the response. At high-frequency the LISN circuit makes possible a more accurate measurement. Further information about LISN can be found in section **¡Error! No se encuentra el origen de la referencia.**.

To be able to compare the high-frequency specter with the high-frequency normative limits what has been done is an adjustment for the bandwidth from 50 Hz to 9 kHz as the norm UNE-EN_55016-1-1 appoints.

This adjustment make the specter not to show the output peaks at each frequency but a mean of them as it is explained in section **¡Error! No se encuentra el origen de la referencia.¡Error! No se encuentra el origen de la referencia.**. Besides that, the output at each frequency after the adjustment needs to be under the normative limit (outputs with +3dB over the normative limit could get passed as suitable depending on the case due to the inexact measurement of EMIs).

If at this point of the simulation, the response of the topology is not reaching the normative requirements, there should be a re-adjustment either of the calculated filter or the control. Also another filter for EMIs can be added just before the load in order to smooth even more the high frequency possible harmonic peaks.

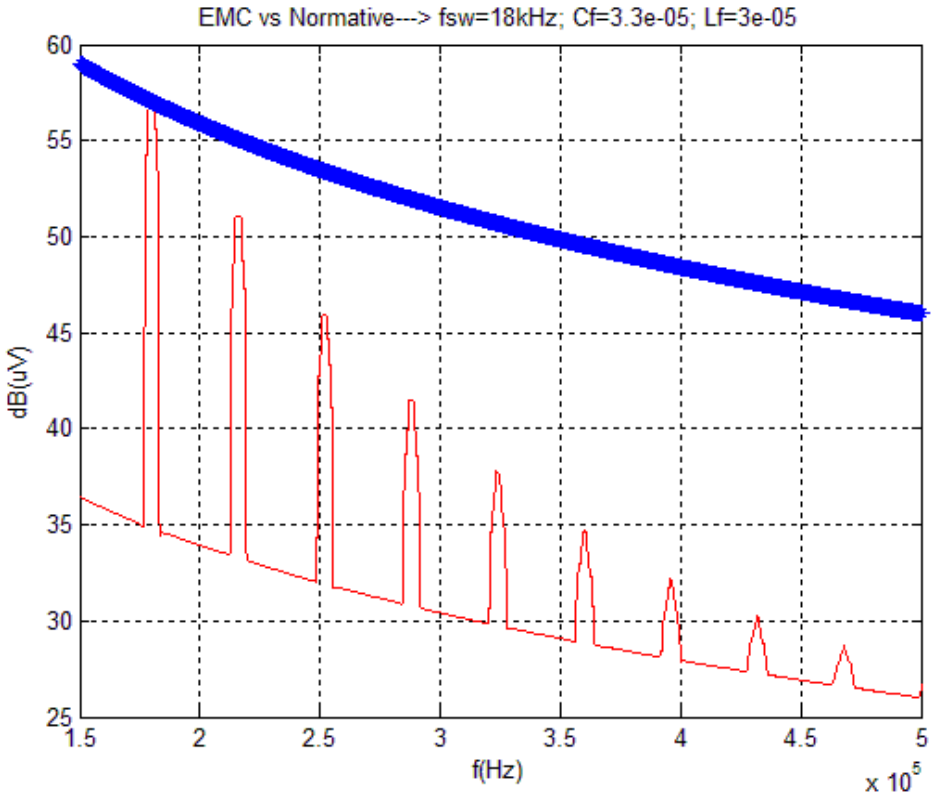

Fig. 22: DC/AC EMIs vs Limits

The previous figure (Fig. 22), represents the emission limits for class "A" systems (in blue) and the spectrum at high frequencies (in red) of the topology.

Peaks (in red) seen in Fig. 22, follows a specific pattern of repetition. At each 36 kHz one peak of emission appears, the first one seen is at 180 kHz, then 216, 252, 288… kHz. This was explained before and basically it appears at twice the switching frequency because of the features of the unipolar PWM control previously explained.

3.1.3. Selection of components

3.1.3.1 Transformer

The transformer included in this topology has a turn relationship of 6.8, which means that the output voltage at the secondary winding will be 6.8 times the primary voltage. The operating frequency in the transformer is the line frequency, 50 Hz. With this frequency the core of the transformer must be laminated with several grain-oriented sheets.

The transformer designed must be able to supply the power demanded by the elements downstream without saturating, then it is the first condition for this design. The below RMS values have been extracted from the simulations.

$$V_{PRIM/RMS} = 33.5\,V; \quad I_{PRIM/RMS} = 23.8\,A\,;$$

$$V_{SEC/RMS} = 227.7\,V\,; \quad I_{SEC/RMS} = 3.5\,A$$

$$P = V_{PRIM/RMS} \cdot I_{PRIM/RMS} = V_{SEC/RMS} \cdot I_{SEC/RMS} = 797\,VA \approx 800\,W \qquad (8)$$

For this power, the iron coefficient for grain-oriented magnetic sheets is between 1 and 1.1 according to Table 3.

Values of iron coefficient (k) for good quality magnetic sheets (grain-oriented)	
Transformer power	*Coefficient (k)*
from 25 to 100 VA	*0,7 - 0,85*
from 100 to 500 VA	*0,85 - 1*
from 500 to 1000 VA	*1 - 1,1*
from 1000 to 3000 VA	*1,1 - 1,2*

Table 3: Grain-Oriented magnetic sheet coefficient

With the power and the k coefficient, the core net section can be obtained.

$$S_n = k \cdot \sqrt{P(VA)} = 1 \cdot \sqrt{800} = 28.28\ cm^2 \qquad (9)$$

Taking into account the stacking factor as $F_{stacking} = 0.95$, the real core section is obtained.

$$S_r = \frac{S_n}{F_{stacking}} = \frac{28.28}{0.95} = 29.77 \approx 30\ cm^2 \qquad (10)$$

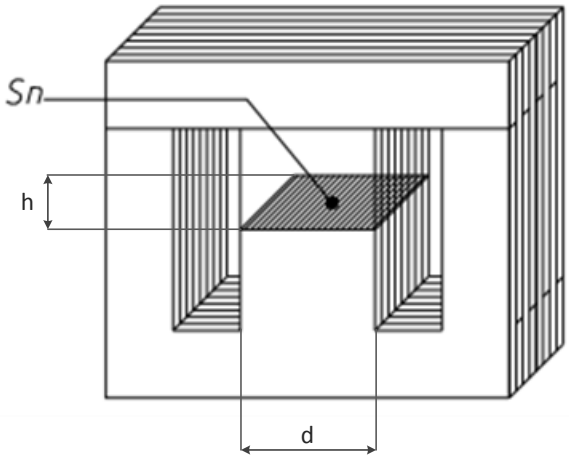

Fig. 23: Laminated magnetic core

The d factor depicted in Fig. 23 must be decided from a standard core size table. The selected core from DIN E41-302 is the EI 195 that has a d core width of 5.5 cm.

So the h dimension is determined by the following equation:

$$h = \frac{S_r}{d} = 5.45\ cm \qquad (11)$$

The number of sheets will depend on the width of them and the h value taken. Then, for a standard width of 0.35 mm, 147 sheets will be needed for a stacking factor of 95 %.

Once the core is selected, the number of turns for each winding must be decided. Having in mind the RMS voltage values of the primary and secondary winding, the ideal number of turns can be obtained via the following equations:

$$N_{PRIM} = \frac{V_{PRIM/RMS}}{f \cdot S_r \cdot B_{Gauss} \cdot 4.4 \cdot 10^{-8}} = \frac{33.5}{50 \cdot 30 \cdot 10^4 \cdot 4.4 \cdot 10^{-8}} = 50.75 \quad (12)$$

$$N_{SEC} = \frac{V_{SEC/RMS}}{f \cdot S_r \cdot B_{Gauss} \cdot 4.4 \cdot 10^{-8}} = \frac{227.7}{50 \cdot 30 \cdot 10^4 \cdot 4.4 \cdot 10^{-8}} = 345 \quad (13)$$

The turns can be or not an entire number. In this case it has been decided to have an entire number, then the primary winding will have 51 turns and the secondary will have 350 to maintain the relation (and increase a bit more the secondary voltage to obtain 230 RMS volts).

$$N_{PRIM} = 51$$

$$N_{SEC} = 350$$

Considering a conservative current density, J, of 3 A/mm^2, the diameter of the wire is easily obtained.

Primary winding:

$$Section: S_p = \frac{I_{PRIM/RMS}}{J} = \frac{23.8\ A}{3\ \mathrm{A}/mm^2} = 7.93\ mm^2 \quad (14)$$

$$Diameter: D_p = \sqrt{\frac{4 \cdot S_p}{\pi}} = 3.17\ mm \quad (15)$$

To standardize, the wire selected for the primary would be an AWG8 of 3.264 mm.

$$D_p = 3.264\ mm$$

Secondary winding:

$$Section: S_s = \frac{I_{SEC/RMS}}{J} = \frac{3.5\ A}{3\ \mathrm{A}/mm^2} = 1.16\ mm^2 \quad (16)$$

$$Diameter: D_s = \sqrt{\frac{4 \cdot S_p}{\pi}} = 1.21\ mm \quad (17)$$

To standardize, the wire selected for the secondary would be an AWG16 of 1.291 mm.

$$D_s = 1.291\ mm$$

For the EI 195 chosen, the window height is 12.5 cm. Since the bobbin will use a small part of this window height, the effective height would be approximately 12 cm. Depending on the number of turns needed, the height of the window and the diameter of the wire it is possible to wind in more than one layer.

For each winding, the maximum number of turns that fit each layer will depend on the diameter of the wire and the height of the core.

As in the primary, the number of turns is 51, two layers will be needed. One of 26 and the other of 25.

$$Number\ \max of\ turn\ per\ layer, primary: N_P = \frac{height}{D_p} = \frac{120\ mm}{3.264\ mm} = 36.76 \quad (18)$$

$$Number\ \max of\ turn\ per\ layer, secondary: N_s = \frac{height}{D_S} = \frac{120\ mm}{1.291\ mm} = 92.95 \quad (19)$$

In the secondary winding, the number of turns is 350, so 4 layers will be needed. There will be 2 of 88 turns and 2 of 87 turns.

A final check with the window width must be done. The sum of the diameter of each wire multiplied by its number of layers must be smaller than the window width of the EI core selected.

$$Window\ width: A_{EI\ 195} = 42.5\ mm \leq 2 \cdot 3.264 + 4 \cdot 1.291 = 11.692\ mm \quad (20)$$

3.1.3.2 Inductor

For the inductor design, the ferroxcube magnetics design tool has been used. The L_f value obtained from the previous calculation in the LC filter section is equal to 30 µH. For the proper operation of the filter it is usual to half the filter value and twice the number of elements to place each one of them at both wires connected ("positive and negative"). Then, there should be two inductors of 15 µH.

Filling several blank parameters (L_f, I_{RMS}, temperature rise…) in the software, a list of suitable cores appear. The one chosen is a PQ 32-30 of 3C90 ferrite material. This family has been chosen due to its small cost and volume. About 800 µm of gap will be used in order to decrease the permittivity of the core.

The parameters of the selected inductor (PQ32/30-3C90-E315) are:

$I_e = 74.7\ mm$	$\mu_e = 112$	$R_{DC} = 0.0019\ \Omega$	$Op\ temp = 75ºC$
$A_e = 167\ mm^2$	$A_L = 320\ nH$	$D_{CU} = 2.5\ mm$	Wind dissip =1.1 W
$V_e = 12500\ mm^3$	$N = 7$	$B = 326\ mT$	$\Sigma(l/A) = 0.447\ mm^{-1}$

And checking that the desired inductance is reached, the following equation is applied:

$$L = \frac{N \cdot Ø}{i} = \frac{N}{i} \cdot A_e \cdot B = \frac{N}{i} \cdot A_e \cdot \mu_r \mu_o \frac{N \cdot i}{I_e} = \frac{N^2 \cdot A_e \cdot \mu_r \mu_o}{I_e} = \frac{7^2 \cdot 167 \cdot 112 \cdot 4\pi 10^{-7}}{74.7} = 0.0154\, mH = 15.4\, \mu H \quad (21)$$

3.1.3.1 Capacitor

The capacitor used in this topology cannot be electrolytic but it has a big value of capacitance, so some in parallel should be placed. This is a drawback in the topology as, as it will be seen, the cost will increase.

The selected device will be a ceramic capacitor of 10 µF and 100 V with manufacturing reference: C5750X7S2A106M230KB. Three of them will be placed in parallel to obtain an approximate capacitance of 30 µF.

3.1.3.2 Transistor

The selection of the transistor must be made according to the voltage it has to support between drain and source, the resistance it presents in continuous mode and the maximum current allowed. Additionally in applications where the efficiency is a matter of high importance, the switching features can bend the scales towards one or another, always regarding the price.

The voltage of the batteries is around 48-50 V but it can increase up to almost 60 V at the beginning. Then the maximum drain source voltage at the transistors will be 60 V. The current peak through them is 35 A according to simulated results.

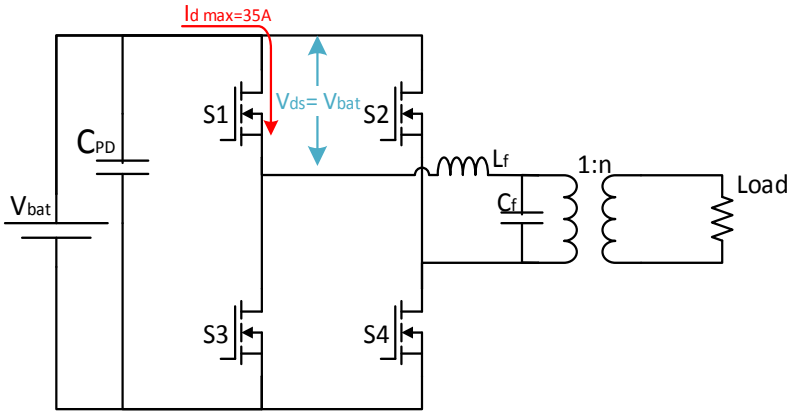

Fig. 24: Transistor selection:

With this information, the transistor selected is a MOSFET due to its good performance at low voltages and high frequencies. The manufacturer Infineon suggests several alternatives and the one chosen is the IPP180N10N3 G because of the cost.

3.1.3.3 Heat sink

After the transistor selection and the loss calculation performed in the following section, 3.1.4.1 Transistor losses, a heat sink must be selected in case of over temperature in the device.

The maximum junction temperature according to the datasheet is 175 ºC. Then, the first step is to evaluate if this temperature is reached without a heat sink or not.

The maximum ambient temperature is considered 45 ºC (this inverter would be place in the elevator shaft where there is a high ambient temperature) and the power dissipated at each transistor is 5.8 W according to simulation results.

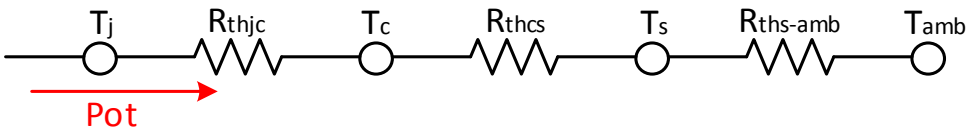

Fig. 25: Thermal circuit representation

$$\widehat{T_j} - T_{amb} = Pot \cdot R_{thJA} \qquad (22)$$

The maximum junction temperature get without a heat sink is obtained from the previous equation. For a $R_{thJA} = 63\ ºK/W$, the junction temperature is 404.6 ºC. Very much over the maximum permitted 175 ºC. A heat sink is needed.

The union between the junction of the device and the heat sink will be performed by the Silpad HF300P of $R_{thCase\ Sink} = 0.48$.

For the heat sink selection, the maximum junction temperature will be 140 ºC. Then resolving the circuit, the $R_{th\ Sink\ Amb}$ should be obtained.

$$\frac{T_J - T_c}{Pot} = R_{thJC} \quad \Rightarrow \quad T_c = T_J - Pot \cdot R_{thJC} = 140 - 5.8 \cdot 2.1 = 128\ ºC \qquad (23)$$

For a maximum temperature of junction of 140, the case shouldn't be over 128 ºC.

$$\frac{T_c - T_S}{Pot} = R_{thCS} \quad \Rightarrow \quad T_s = T_C - Pot \cdot R_{thCS} = 128 - 5.8 \cdot 0.48 = 125\ ºC \qquad (24)$$

And finally, the $R_{thSink-Ambient}$ to select the heat sink is obtained from the sink temperature.

$$R_{thS-AMB} = \frac{T_S - T_{AMB}}{Pot} \leq \frac{125 - 45}{5.8} = 13.8\ ºK/W \qquad (25)$$

An individual heat sink for T0220 package of 8ºC/W has been selected. The referenced from the manufacturer Wakefield is 274-1AB.

3.1.4. Efficiency

The efficiency of the topology will depend on two main elements, the magnetics and the switching devices. The transistors will have conduction losses and switching losses. A heat sink was already dimensioned in the previous section taking into account the losses. For magnetic elements, iron and cooper losses will appear.

3.1.4.1 Transistor losses

As it has been mentioned, the losses from the transistors arrives from two of their operation modes. The conduction and the switching. For the energy loss estimation, the features of the selected transistor, IPP180N10N3 G, are going to be used:

- IPP180N10N3 G features:
  - $R_{DS_{ON}} = 18\ m\Omega$
  - $T_{J\_max} = 175\ ºC$
  - $R_{\mathrm{th_{JC}}} = 2.1\ K º/W$
  - $R_{\mathrm{th_{JA}}} = 62\ K º/W$
  - $t_r = 12\ ns$
  - $t_f = 5\ ns$

The area under the transistor current to the square multiplied by the on resistance of the MOSFET, $R_{DS_{ON}}$, is the energy lost in a switching period. Integrating it along the whole 50 Hz period, the conduction loss is obtained.

$$W_{cond}(i) = \int_0^{T_{on}} (i(t))^2 \cdot R_{DS_{on}}\, dt \qquad (\ 26\ )$$

As the $R_{DS_{on}}$ in this case is relatively high for a MOSFET and the switching times quite small, the conduction losses are bigger than the switching ones for each transistor.

$$W_{switch}(i) = \frac{1}{2} \cdot \mathrm{V}_{bat}\left(i_{on} \cdot t_{rise} + i_f \cdot t_{off}\right) \qquad (\ 27\ )$$

For the switching losses the switching current is the only requirement for its calculation since the voltage is supposed invariable.

From the equation (26)and (27), integrated along the period, the power dissipation for each transistor is:

$$P_{cond} = 5.7385\ W$$

$$P_{switch} = 0.0705\ W$$

Then, for the whole bridge, the power dissipated is four times these two values:

$$P_{tot\_transistores} = 23.2362\ W$$

3.1.4.2 Transformer

Transformers have iron and cooper power losses. The transformer designed in section 3.1.3.1 is a laminated steel transformer of 50 Hz operating frequency. Because of this low frequency, the cooper loss will be the conduction one as there will be almost no presence of the skin and proximity effect.

The cooper losses are obtained via the conduction power dissipation equation.

$$P_{Cu} = \mathrm{I}_{RMS}{}^2 \cdot R_{DC} = \mathrm{I}_{RMS\_Prim}{}^2 \cdot R_{DC\_Prim} + \mathrm{I}_{RMS\_Sec}{}^2 \cdot R_{DC\_Sec} \quad (28)$$

The RMS currents in both the primary and the secondary winding are easily extracted from the simulation. The resistance of the cooper will depend on the length of the wire and the size of it (AWG size of wires).

Primary wire: AWG8 → $R_{CU\_Prim} = 2{,}061\ m\Omega/m \cdot \text{ length} = 23{,}08\ m\Omega$

Secondary wire: AWG16 → $R_{CU\_sec} = 13{,}17\ m\Omega/m \cdot \text{ length} = 1{,}014\ \Omega$

The length of the wire depends on the core central column perimeter and the number of turns. The perimeter is 22 cm. Then, the length is 11,2 m for the primary and 77m for the secondary wire.

The cooper power loss caused by low frequency current conduction with three threads per wire is:

$$P_{Cu} = \frac{24^2 \cdot 0{,}023}{3} + \frac{3{,}51^2 \cdot 1{,}04}{3} = 4{,}416 + 4{,}01 = 8{,}426\ \mathrm{W} \quad (29)$$

The core losses have been estimated from datasheets and supplier information. Knowing the form of the sheets that compound the core, the area of each one of them can be calculated. The thickness of the core has also been calculated in the transformer selection section so the volume of the core is obtained.

For the EI 195, the useful area is 244,74 cm^2 and the thickness 5,45 cm. That gives a core volume of 125,9 cm^3. Taking a density of 7,65 g/cm^3 from a steel sheet manufacturer datasheet, a total weight of around 1 kg is got.

Core Loss in Watts per Kilogram (WPKg) at 50 Hz				
Induction Tesla	0.18mm M-2 WPKg	0.23mm M-3 WPKg	0.27mm M-4 WPKg	0.35mm M-6 WPKg
1.0	.268	.283	.338	.437
1.1	.325	.343	.410	.525

Fig. 26: Core losses according to induction

Having in mind the 10k Gauss induction taken in the design (equivalent to 1 tesla) and the 0.35 mm of sheet depth, the core losses should be close to 0.437 W/kg.

$$P_{FE} = \text{Wpkg} \cdot \text{weight} = 0.437 \cdot 1 = 0.437 \text{ W} \quad (30)$$

So the estimation of total power loss in the transformer is equal to 8,863 W.

3.1.4.3 Inductor

The losses found in the inductor, as well as in the transformer, will be cooper and iron losses. The cooper losses have been given by the ferroxcube software as winding dissipation. They are about 1.1 W which is not quite elevated considering the high current that crosses the inductor.

The iron ones are obtained from the datasheet, and an approximate value would be 1.5 W for 20 kHz and 200 mT, data that doesn't differs a lot from the own one.

3.1.4.4 Efficiency of the topology

The efficiency, taking into account all the power losses, is:

$$\text{Efficiency} = \frac{P_{out}}{P_{out} + P_{transistor} + P_{transformer} + P_{ind}} = \frac{800}{800 + 23{,}23 + 8{,}863 + 2 \cdot 2{,}6} \approx 0.955 \quad (31)$$

3.1.5. Cost

The cost of the system itemized is shown below. Each item/element has its description, price (for 10 units) and the total amount is given below.

Description	Qtty	Cost/ud	Total
Trans 100 V, R18m, Infineon	4	0,77 €	3,09 €
Core PQ 32/30 3C90	2	4,50 €	9,00 €
Laminated Sheet core	1	10,00 €	10,00 €
Bobbin PQ 32/30	2	1,00 €	2,00 €
Ceramic capacitor, 2.2 uF	3	1,91 €	5,73 €
Heat sink T0220, Rd-amb8	4	0,22 €	0,89 €
AWG8	12	0,90 €	10,80 €
AWG10	1	0,80 €	0,80 €
AWG16	80	0,25 €	20,00 €
		Total	**62,31 €**

3.2. DC/AC/DC/AC design, multi-stage inverter

The second design selected is a multi-stage inverter that is controlled by a PWM signal at 20 kHz. The reactive energy that could appear in case the load is not a pure resistance will be carried out by the intermediate capacitor.

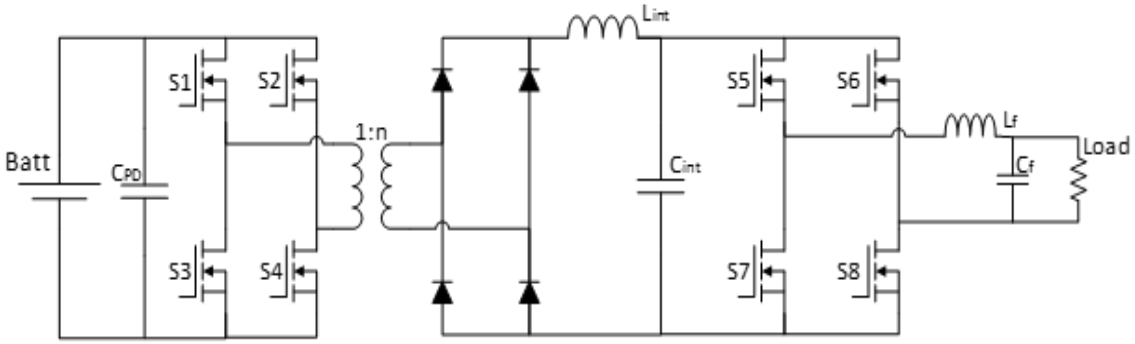

Fig. 27: DC/AC/DC/AC, multi-stage inverter

According to the desired voltage at the output and the voltage drop across the elements of the circuit (transistors and diodes) the transform relation has to be close to 7.

$$Tr = \frac{V_{load} + V_{dropbridge2} + V_{dropdiode}}{V_{bat} - V_{dropbridge1}} \approx \frac{325 + 0{,}5 + 7}{48 - 0{,}5} = 7 \qquad (32)$$

The control for this topology is a variable phase PWM at 20 kHz. As it was explained in section 2.3.2, it is needed a zero medium voltage control wave, symmetric, to reduce the magnetic flux along the transformer core to make it operate at high frequency.

Then, the control applied is a variable-phase PWM that creates an output waveform like the one depicted in Fig. 28

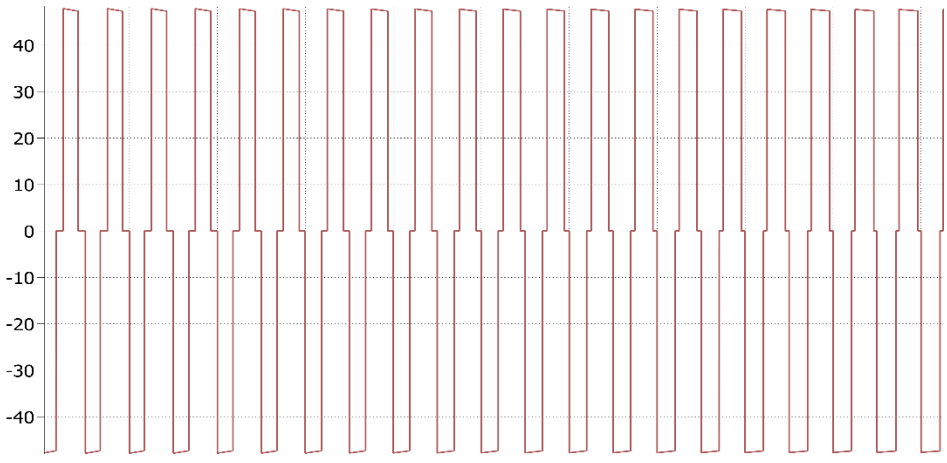

Fig. 28: Variable-Phase PWM

From this AC voltage, the diode bridge will make the conversion to DC and the final transistor bridge will only carry out with the function of rectifying the full wave reached in the intermediate capacitor.

3.2.1. LC filter calculation

For the design of Fig. 27 there are two LC structures, one intermediate that builds the full wave (low-frequency pass filter) and the second one just behind the load, to treat the emissions at high frequencies.

The first LC filter needs to be designed to act like a low pass filter at a frequency at least half the switching frequency. That means that the cut frequency should be less than 10 kHz.

$$f_c = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{int} \cdot C_{int}}} \qquad (33)$$

As there's a diode bridge that blocks the current to return to the source in case of reactive energy existence, the intermediate capacitor must be designed big enough to be able to hold that energy.

The charging and discharging time for the capacitor, τ, has to be small enough (fast) to follow the 50 Hz wave inherited in the incoming wave and big enough to hold additional energy without changing a lot its voltage.

As the switching frequency is 20 kHz, the limit frequency the capacitor must be able to follow should be at least 10 times down the switching frequency to avoid the catching of the harmonics at 20 kHz.

The selected limit frequency will be 1 kHz with a period time of 1ms (the τ value).

$$C_{int} = {}^{\tau}/_{R_L} = {}^{1e-3}/_{66.125} = 15\mu F \qquad (34)$$

This load introduced is at maximum power, as the steady power of the inverter should not over pass the 400 W, the capacitor value can be smaller. A value of 5 μF for the capacitor is taken.

With this selection, the calculation for the inductor is immediate.

$$L_{int} = \frac{1}{C_{int}}\left(\frac{1}{2 \cdot \pi \cdot f_c}\right)^2 = \frac{1}{5\mu F}\left(\frac{1}{2 \cdot \pi \cdot 10\ kHz}\right)^2 \geq 5 \cdot 10^{-5} \qquad (35)$$

Taking into account this condition onto simulations, the conclusion is to go to a conservative selection of an inductor of 500 μH.

- L_{int}=500µH
- C_{int}=5µF

$$L_{int} \cdot C_{int} = 2.5 \cdot 10^{-9} \longrightarrow f_c = 3.18\ kHz$$

The second LC filter can be found right before the load. It is much smaller as its function is basically to filter the high frequency harmonics (over 150 kHz).

Then, applying another time the equation (33) for a desired cut frequency below 150 kHz, a LC product limit value is obtained:

$$L_f \cdot C_f = \left(\frac{1}{2 \cdot \pi \cdot f_{c2}}\right)^2 = \left(\frac{1}{2 \cdot \pi \cdot 150\ kHz}\right)^2 \geq 1.125 \cdot 10^{-12} \qquad (\ 36\ )$$

And performing simulations with the range of possible values, a selection of 500 nH for the inductor and 3.3 µF for the capacitor is made.

- L_f=500 nH
- C_f =3.3 µF

$$L_f \cdot C_f = 1{,}65 \cdot 10^{-12} \longrightarrow f_c = 124\ kHz$$

3.2.2. Simulation

Once the values for the elements are reached, a PLECS simulation of the design can be performed. The objective at this section is to evaluate the validity of the output obtained with the normative.

3.2.2.1 Output

Filling in PLECS the inductor, capacitor and transformer values it is easy to simulate the behavior of the topology under an established load. The output obtained with all the previous values is depicted in Fig. 29.

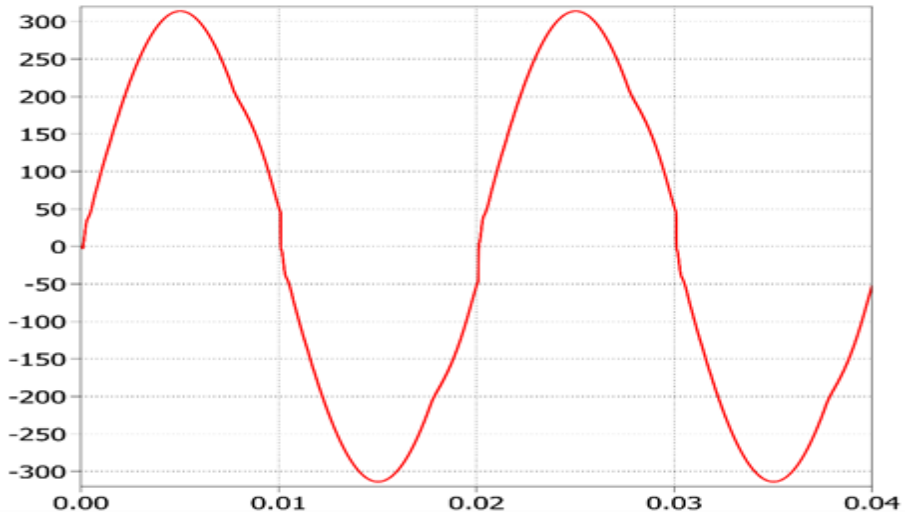

Fig. 29: Multi-stage inverter output

There is almost no observable ripple in this figure since the intermediate LC structure acts as low pass filter. The maximum ripple is about 1V, pretty small compared with the 5 V of the DC/AC design since the cut frequency in this case is selected shorter (3.18 kHz instead of 5 kHz).

This small ripple appears at 40 kHz, twice the switching frequency because of the characteristics of the full diode bridge that twice the frequency. Each diode let the current pass half the period time so the frequency at its output result doubled. Also the zero crosses are not perfect because of two issues. The first one is that the full wave obtained after the diode bridge doesn't reach the zero because of the reactive elements in the circuit (inductors and capacitors) , then a straight vertical line can be observed. The second one is that the rectification (the second transistor bridge) of the full wave is not perfectly reached.

Because of those issues it is important to check the frequency specter obtained at low frequencies.

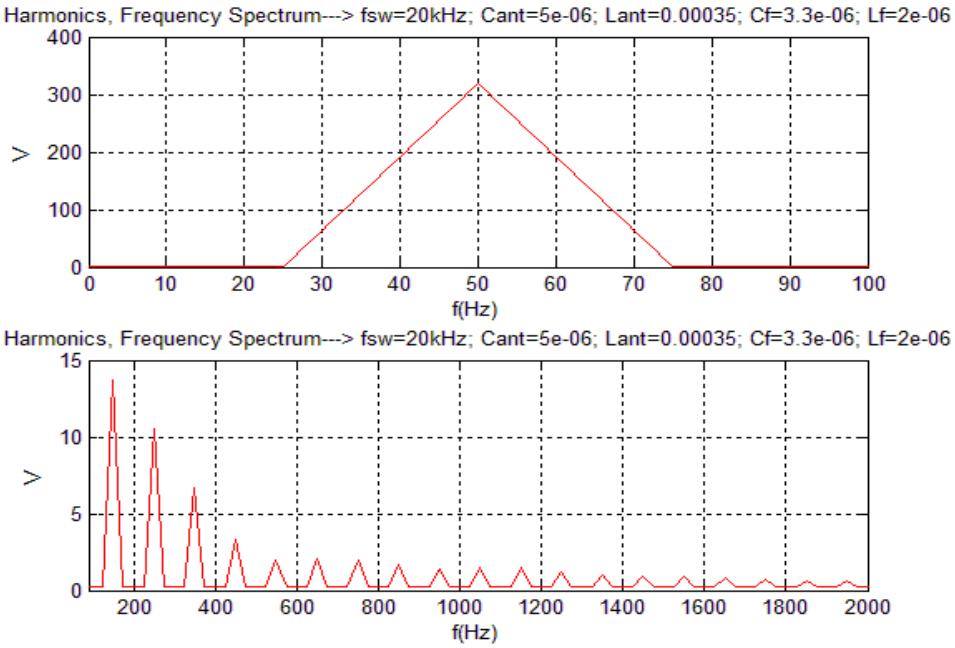

Fig. 30: Multi-stage inverter harmonic specter

In the low frequency harmonics figure depicted, it can be observed that at the line frequency, 50 Hz, the amplitude value is at 328 V. After that frequency, several harmonics peaks appear as well because of the full-wave issues before mentioned.

3.2.2.1 Comparison with normative

Taking into account the normative UNE-EN_61000-3-2 for low-frequency harmonics and comparing it with the output voltage specter simulation in a grid leaves the result observed in Fig. 31.

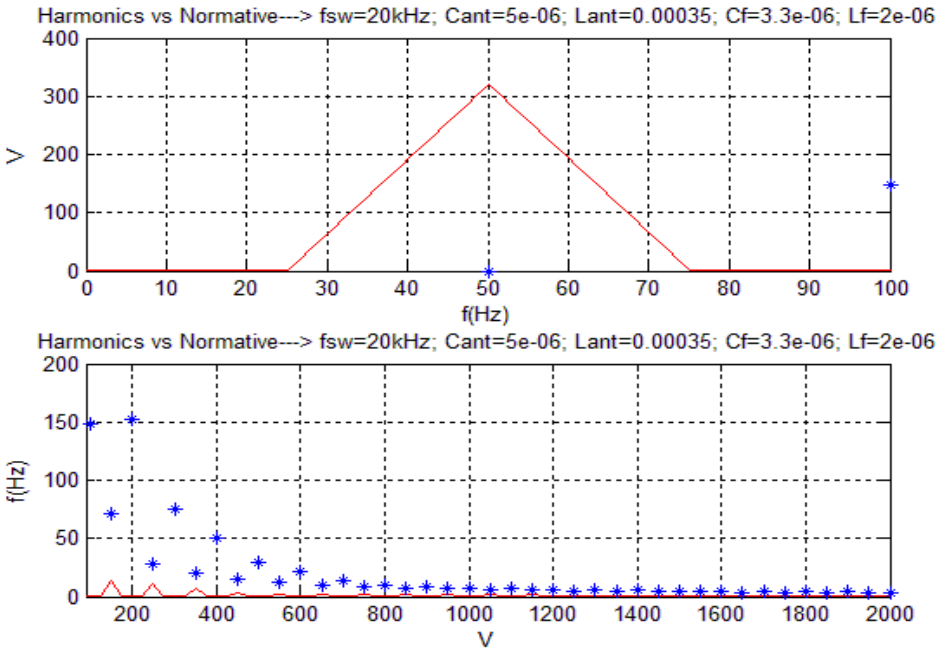

Fig. 31: Multi-stage inverter low frequency comparison

Because of the over modulation control, the switching frequency is 400 times the line frequency which makes the achievement of the low frequency normative quite easy to obtain. The real challenge is then to achieve the high-frequency one since the more the switching frequency is increased, the higher the high-frequency emission peaks are.

The limits and the specter at high-frequencies is depicted in Fig. 32.

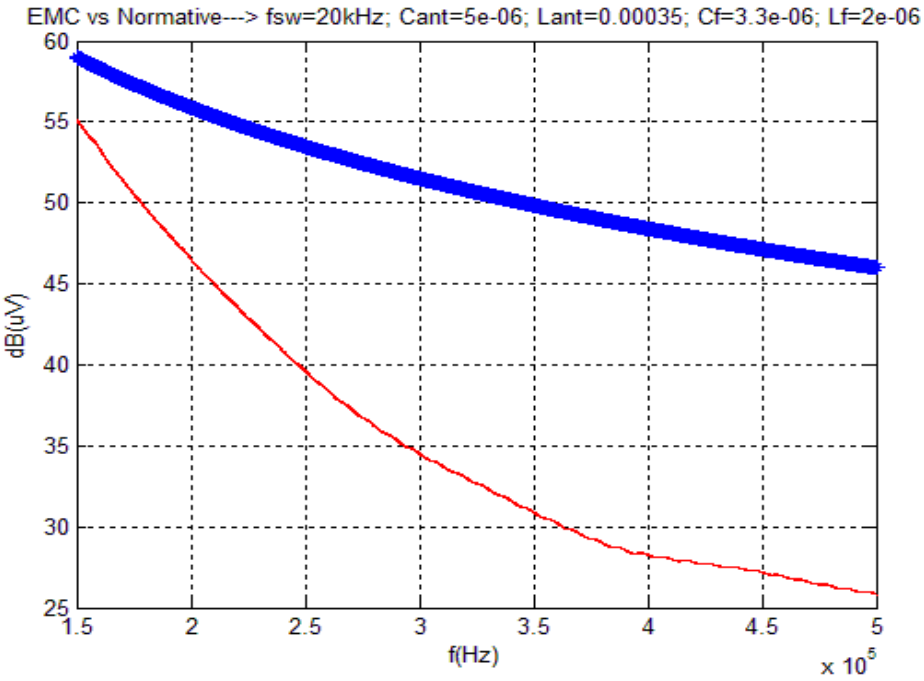

Fig. 32: Multi-stage inverter EMIs vs Normative

Once the waves of the topology are checked, the selection of the components must be carried out.

3.2.3. Selection of components

3.2.3.1 Transformer

The frequency operation of the transformer will be 20 kHz. That allows the use of ferrite cores instead of the laminated sheets from the previous topology. Some values needed for the transformer design have been extracted from the simulation:

$$V_{P_{RMS}} = 38\ V \qquad V_{S_{RMS}} = 258.4\ V$$
$$I_{P_{RMS}} = 22.457\ A \qquad I_{S_{RMS}} = 3.3\ A$$

With these values, either the primary or the secondary, the maximum power exigency is obtained. That will be used with the ferroxcube software to get a list of possible suitable cores.

$$P = V_{P/RMS} \cdot I_{P/RMS} = V_{S/RMS} \cdot I_{S/RMS} = 853.36 \approx 860\ W \qquad (37)$$

From 850 W to 1 kW these below are the valid cores for the application according to ferroxcube.

Nr.	Shape	Core type	Ferrite	Pthr (W)	Bmax (m
1	E	E55/28/25	3C94	880	360
2	E	E55/28/25	3C92	900	380
3	ETD	ETD59/31/22	3C90	920	340
4	ETD	ETD59/31/22	3F3	960	340
5	ETD	ETD59/31/22	3C95	960	360

Fig. 33. Valid cores for the application

The one chosen is the ETD59/31/22 3C90 with maximum power of 920 W and $B_{MAX} = 340\ mT$. With the core information obtained from the datasheet after the election, the number of windings are gotten from the following expressions.

$$N_P \geq \frac{V_{P/min}}{f \cdot 2 \cdot B_{max} \cdot A_e} = \frac{48}{20 \cdot 10^3 \cdot 2 \cdot 340 \cdot 368 \cdot 10^{-6}} = 9.59 \qquad (38)$$

$$N_S \geq \frac{V_{S/min}}{f \cdot 2 \cdot B_{max} \cdot A_e} = \frac{326.4}{20 \cdot 10^3 \cdot 2 \cdot 340 \cdot 368 \cdot 10^{-6}} = 65.212 \qquad (39)$$

Selecting 10 turns for the primary and 68 to the secondary winding, the relation is maintained and the core does not saturate (B ≈ 120 mT). Then, the selected turns are:

$$N_{Prim} = 10 \quad ; \quad N_{Sec} = 70$$

The theoretic magnetizing inductance would be $L_{mag} = N^2 \cdot A_L$. ($A_L = 6000\ nH \pm 25\%$).

$$L_{mag_{Prim}} = 600\ \mu H \quad ; \quad L_{mag_{Sec}} = 29{,}4\ mH$$

To calculate the diameter of the wire, a maximum current density of 3 A/mm^2 is supposed. Then for the primary winding:

$$Section: S_p = \frac{I_{P/RMS}}{J} = \frac{22.457\ A}{3\ \mathrm{A}/mm^2} = 7.48\ mm^2 \qquad (41)$$

$$Diameter: D_p = \sqrt{\frac{4 \cdot S_p}{\pi}} = 3.08\ mm \qquad (40)$$

To standardize, the wire selected for the primary would be an AWG8 of 3.264 mm.

$$D_p = 3.264\ mm$$

Secondary winding:

$$Section: S_s = \frac{I_{S/RMS}}{J} = \frac{3.3\ A}{3\ \mathrm{A}/mm^2} = 1.1\ mm^2 \qquad (\ 42\ )$$

$$Diameter: D_s = \sqrt{\frac{4 \cdot S_s}{\pi}} = 1.21\ mm \qquad (\ 43\ )$$

To standardize, the wire selected for the secondary would be an AWG16 of 1.291 mm. The number of layers will be 1 for the primary winding and 2 for the secondary.

3.2.3.2 Inductor

Both inductors, L_{int} and L_f have been designed using the ferroxcube inductor design tool.

The intermediate inductor of 400 µH is going to be split up in two of 200 µH in order to decrease its value and increase its performance.

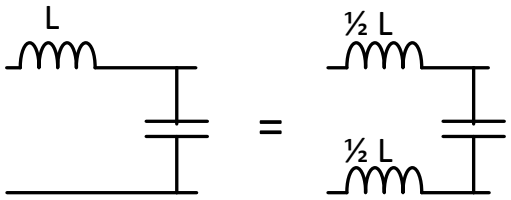

Fig. 34: L split

The current that crosses this element is equivalent to 4 A RMS, then using the ferroxcube inductor design tool, a PQ 20/20 3C90 with 428 µm of gap is suggested.

$l_e = 45{,}7\ mm$	$\mu_e = 124$	$R_{DC} = 0.071\ \Omega$	$Op\ temp = 79ºC$
$A_e = 62{,}6mm^2$	$A_L = 214\ nH$	$D_{CU} = 0.71\ mm$	Wind dissip =0.64 W
$V_e = 62850\ mm^3$	$N = 31$	$B = 317\ mT$	$\Sigma(I/A) = 0.372\ mm^{-1}$

The checking for the inductance obtained with this core is performed in the below equation:

$$L_{int} = \frac{N^2 \cdot A_e \cdot \mu_r \mu_o}{I_e} = \frac{21^2 \cdot 121 \cdot 118 \cdot 4\pi 10^{-7}}{45} = 0.205\ mH = 205\ \mu H \qquad (\ 44\ )$$

Which is a bit under the expected value but it works since the inductance has not been decided pretty to the limit.

Due to the zero average current condition of the second inductor, before the load, the inductor selected is a SMD 1206 inductor of 560 nH. The reference from Murata Electronics is LQH31MNR56K03L.

3.2.3.3 Transistors

There are two sides in this design, one close to the batteries of low voltage and fast switching, and the side close to the load, high voltage and slow switching. Then different sort of devices must be taken. For the low voltage side it is clear that MOSFET transistors will be the chosen ones because of their good performance under these conditions. For the other side, either IGBT or cool MOSFET could be taken. For simplicity MOSFET transistors have been taken at both sides and with a standard T0220 3 pins package.

The selection for the first bridge is the IPP100N08N3 G from Infineon that supports the voltage (up to 60 V) and current (up to 48 A at the beginning) requirements. Besides, the switching features are good enough for the application and the price is acceptable.

For the rectifier transistor bridge, the device selected is the IPP50R500CE that accounts with a considerable low on resistance and supports both current and voltage through the component.

3.2.3.4 Diodes

The diode bridge must be composed of four fast switching high voltage diodes. Also it must assure their capacity of peak currents passing treatment. With these three requirements, the diode selected is STTH8ST06 from ST.

3.2.3.5 Heat sink

In this topology there are several power devices. The transistors that switch at low voltage high current, the transistors that switch at high voltage low current and the diodes.

As there is no much power dissipated in these transistors (according to efficiency calculations of the following section), the first thing is to check whether a heat sink is needed or not. For both types of transistor it is done via de equation (22). The result of the equation conclude that both junction temperatures without a heat sink are over the limit.

Then for the low voltage high current transistors, applying equations (23)(24)(25), considering a maximum junction temperature of 140 ºC and an ambient temperature of 45 ºC, a heat sink of $R_{thS-AMB} \leq 26{,}76\ ºK/W$ is needed in conclusion.

Taking a $R_{thS-AMB}$ of 19.7 ºC/W, the selected heat sink for each transistor is one designed for operate with TO-220 package. The reference number is 7136DG from Aavid Thermalloy.

Following the same steps, and a maximum junction temperature of 120 ºC, a heat sink with $R_{thS-AMB} \leq 10{,}84\ ºK/W$ is needed for the high voltage low current transistors.

The heat sink selected for the second transistor bridge is 504222B00000G from Aavid Thermalloy. It has a thermal resistance of 6.4 ºC/W and is designed for TO-220 package.

3.2.3.6 Capacitor

Both capacitors, the intermediate and the EMIs one, will have to operate at high voltage. The intermediate can be electrolytic as there's only DC voltage in there. Otherwise, the final capacitor, before the load, must be selected for AC voltages.

The election for the intermediate capacitor of 5 µF, will be performed around this range of electrolytic capacitors and for a maximum voltage range of 450 V. Taking that into account, the capacitor selected is the 475CKE450MLN from Cornell Dubilier- CDE. It is an aluminum electrolytic capacitor of 4.7 µF with a voltage rate of 450 VDC.

The capacitor in parallel with the load has a capacitance of 3.3 µF. In this case it cannot be electrolytic as the voltage is not DC but AC. The selected capacitor is C5750X6S2W225K250KA, a ceramic capacitor of 2.2 µF from TDK that has a voltage rating up to 450 V.

3.2.4. Efficiency

To obtain the efficiency for this inverter design it is necessary to obtain first the switching and conduction losses in the switching devices and the iron and cooper losses in the magnetic components (transformer and inductors).

3.2.4.1 Low-voltage side switching transistors

Taking the features from the selected switching devices, the result obtained will approach quite a lot to reality. The below parameters from the datasheet, current and voltage values from simulation are taken into account.

- IPP100N08N3 G, features:
  - $R_{DS_{ON}} = 11\ m\Omega$
  - $T_{J\_max} = 175\ ºC$
  - $R_{\text{th}_{\text{JC}}} = 1.5\ K º/W$
  - $R_{\text{th}_{\text{JAmb}}} = 62\ K º/W$
  - $t_r = 46\ ns$
  - $t_f = 5\ ns$

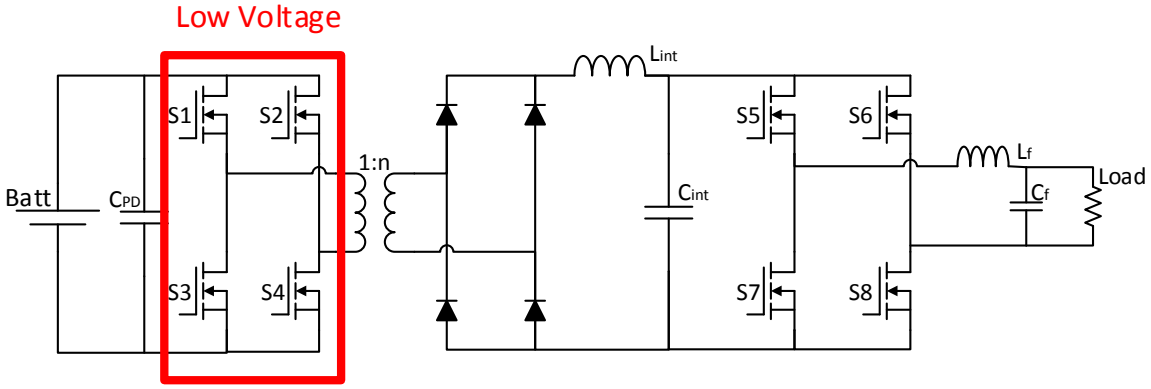

Fig. 35: Multi-stage inverter, low voltage bridge power loss

As the switching frequency for these transistors is 20 kHz, there will be some energy loss each period of 50 µs ($^{1}/_{20\text{kHz}}$). Then, the current levels one instant after the turn on and one instant before the turn off of the device are important to be able to calculate the losses.

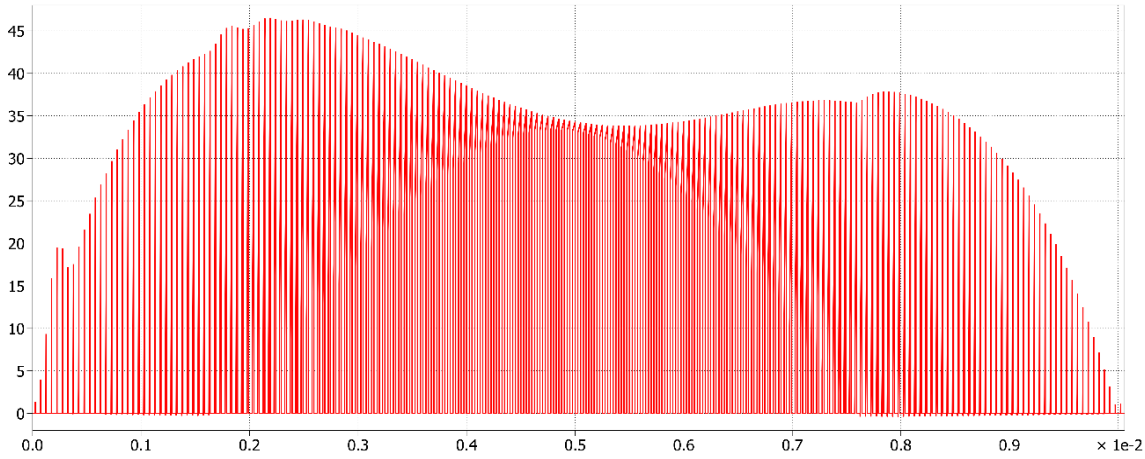

Fig. 36: Current through low-voltage transistor bridge

Above, in Fig. 36, a representation of the simulated current crossing the low voltage transistors is depicted. The peak current can be found at 47 A at 2ms from the beginning of the period and it appears because of the reactive energy present in the circuit. At the middle, it stabilizes and shows the expected 34 peak volts demanded by the nominal load simulated.

$$I_{s1} = rt \cdot \frac{V_{Peak}}{R_L} = 7 \cdot \frac{325\ V}{66.125} = 34\ A \qquad (45)$$

The shape of the current through the transistors is not flat, to calculate the conduction losses a straight line equation between the turn on and turn off current level must be used.

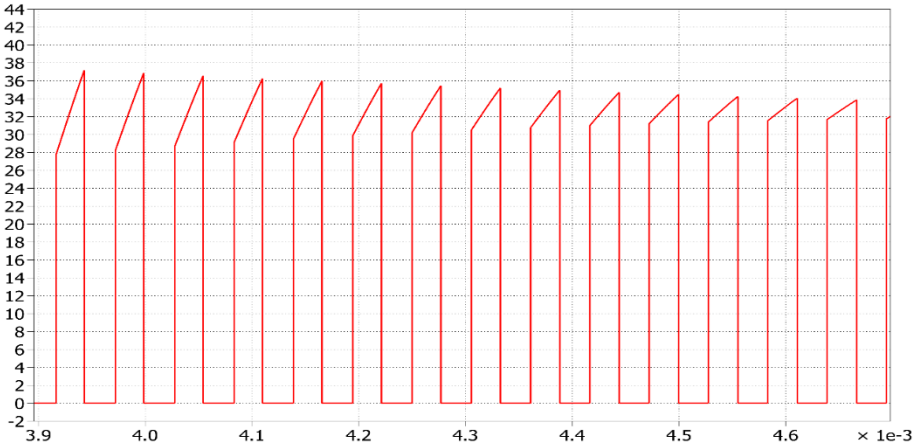

Fig. 37: Switching current zoomed

As it's been said, the turn on and off current values are saved (in a vector). These are used to obtain the conduction energy spent in each one of the switching.

$$W_{cond}(i) = \int_0^{T_{on}} (i(t))^2 \cdot R_{DS_{on}}\, dt = \int_0^{T_{on}} \left(i_o + \frac{i_f - i_o}{T_{on}} \cdot t\right)^2 \cdot R_{DS_{on}} dt \quad (46)$$

$$W_{cond}(i) = R_{DS\_on} \cdot \left({i_o}^2 + i_o \cdot (i_f - i_o) + \frac{(i_f - i_o)^2}{3} \right) \cdot T_{on} \quad (47)$$

Being $i_o$the turn on current, i_f the turn off current and $T_{on}$the time while the transistor is on, $t_{c_{off}} - t_{c_{on}}$. Then, with all the energy parameters known, the power dissipated by one transistor in a period time is:

$$P_{cond} = \frac{\sum_{i=1}^{n} W_{cond}(i)}{T} = 2.9\ W \quad (48)$$

For the switching losses calculation the turn on and off currents are used to make an estimation of the power dissipation. The MOSFET devices introduced into the simulated circuit are ideal, so these effects are not seen in the previous figure depicted.

$$W_{switch}(i) = \frac{1}{2} \cdot \mathrm{V}_{bat}(i_o \cdot t_{rise} + i_f \cdot t_{fall}) \quad (49)$$

Then, the power dissipated in the switching of one of the transistors can be obtained in the same way as the conduction ones.

$$P_{switch} = \frac{\sum_{i=1}^{n} W_{switch}(i)}{T} = 0.35\ W \quad (50)$$

The total power dissipated in the low-voltage transistor bridge (four switching devices) is:

$$P_{tot\_ladoBajo} = 4 \cdot (P_{switch} + P_{cond}) = 13.06\ W \quad (51)$$

3.2.4.2 High-voltage side switching transistors

The losses at the high-voltage side will be overall the conduction ones as there are only two switching events each 50 Hz period.

- IPP50R500CE features:
  - $R_{DS_{ON}} = 0.5\ \Omega$
  - $R_{\mathrm{th_{JC}}} = 2.19\ ºC/W$
  - $R_{\mathrm{th_{CA}}} = 62\ ºC/W$
  - $t_r = 2\ ns$
  - $t_f = 12\ ns$

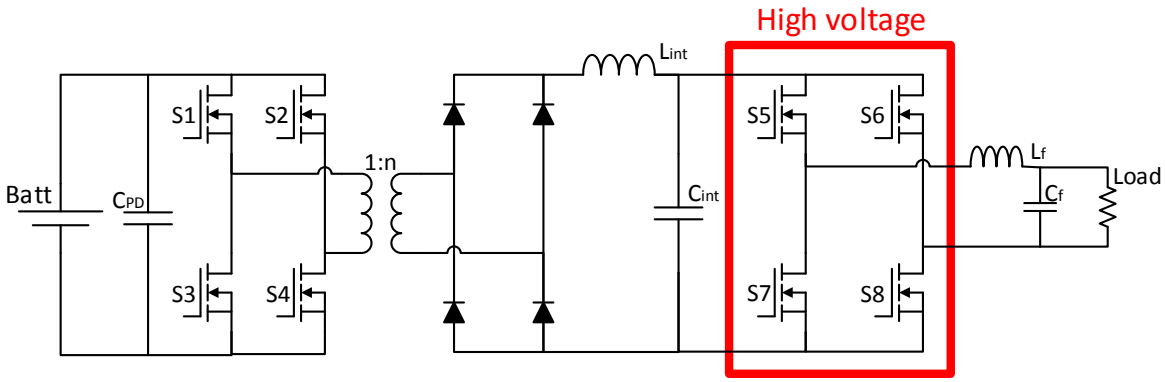

Fig. 38: High voltage transistor losses

The switching losses in this case will be very small due to the triggering of the switching time with the zero-crossing time and the fact that these transistors are only switched twice per period time. The switching frequency for these transistors is the line frequency.

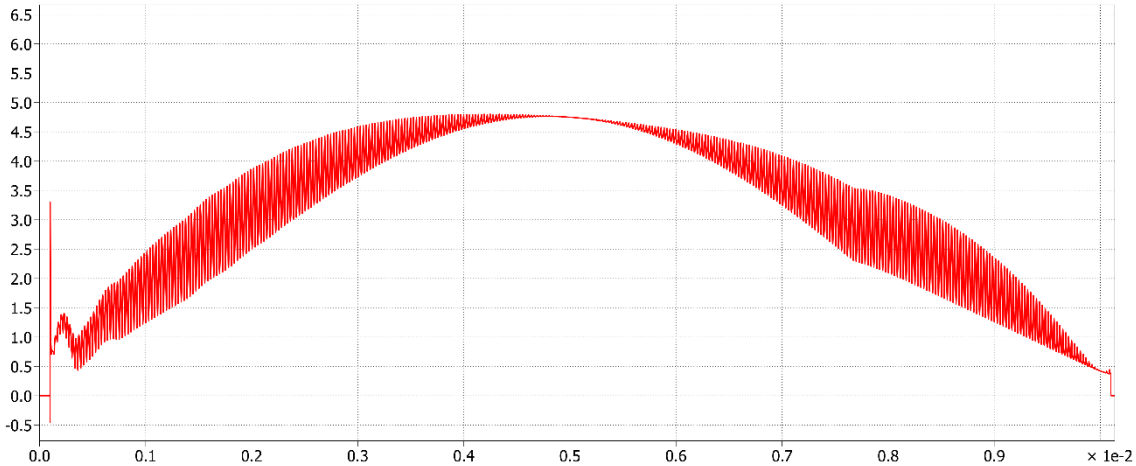

Fig. 39: Multi-Stage inverter High-voltage side transistor current

The duty is 0.5 so just 50 % of the time will be conducting, the rest of the time will be off, then holding the voltage and no current through.

In this case, the energy consumed by the transistor has been worked out using results from simulation.

$$W_{cond}(i) = \int_0^{DT} (i(t))^2 \cdot R_{DS_{on}}\, dt + \int_{\mathrm{DT}}^{T} (i(t))^2 \cdot R_{DS_{on}}\, dt = R_{DS_{on}} \cdot D \cdot T \cdot (i_{RMS})^2 \quad (52)$$

Being $i_{RMS} = 2{,}45$, the conduction power dissipated in each one of these transistors is:

$$P_{cond} = \frac{R_{DS_{on}} \cdot D \cdot T \cdot (i_{RMS})^2}{T} = 3\ W \quad (53)$$

And then, the overall power for the four transistors in the high-voltage side is:

$$P_{tot_{ladoAlto}} = 4 \cdot P_{cond} = 12\ W \quad (54)$$

3.2.4.3 Diodes

The diode bridge included in the circuit deliver two kind of power losses as well, the conduction and the reverse recovery one.

The conduction loss is obtained from an equation provided by the device (STTH8ST06) datasheet. The forward average and RMS values are extracted from simulation.

$$P_{cond_{diode}} = 2{,}22 \cdot I_{F_{AVG}} + 0{,}113 \cdot {I_{F_{RMS}}}^2 = 2{,}22 \cdot 1.5 + 0{,}113 \cdot 2{,}5^2 = 4{,}22\ W \quad (55)$$

The reverse recovery losses will be quite small compared with the continuous ones. Qrr is the reverse recovery charge parameter and it is got from the datasheet.

$$P_{rr_{diod}} = Q_{rr} \cdot V_{in} \cdot f_{sw} = 15 \cdot 10^{-9} \cdot 336 \cdot 20 \cdot 10^3 = 0{,}1\ W \quad (56)$$

Then, the total power losses in the diode bridge is four times the power lost at each one of them.

$$P_{tot_{diodo}} = 4\left(P_{cond_{diode}} + P_{rr_{diod}}\right) = 17{,}28\ W$$

3.2.4.4 Transformer

The efficiency got in the transformer depends on two aspects, the core and the cooper losses. In this case, the core losses will be higher than in the previous case in the 50 Hz transformer. The high frequency of operation of this transformer will cause also more cooper losses because of the skin effect.

The core losses are obtained from the datasheet of the manufacturer. The estimation at 25 kHz of operation and 200 mT for 3C90 material is 6 W of power losses inside the core.

The cooper losses have been calculated considering the skin depth. Then, at high frequencies, the wire section used by the current to go through decreases.

$$\delta = \sqrt{\frac{2 \cdot \rho}{\mu \cdot w}}$$

Because of the skin effect, the current tends to circulate in the surface of the wire and the δ is the width introduced from the surface. That leaves at 20 kHz, the switching frequency, an effective area of wire of 4 mm^2 for the primary and 1,2 mm^2 for the secondary winding.

From this section and the length of the cooper wire, the resistivity is obtained and then, the losses. For the primary, the losses are about 1 W, for the secondary 0.35 W.

3.2.4.5 Inductors

The intermediate inductor efficiency is calculated similarly to the transformer. There will be core and cooper losses. In this case they are expected to be smaller.

According to the PQ 20/20 datasheet, at 25 kHz and 200 mT the core loss is less than 0.35 W. This maximum value is taken for the efficiency calculation. The cooper losses will depend on the diameter, the switching frequency and the medium length of the core. Taking into account all these variables, the cooper loss estimation is 0.25 W.

3.2.4.6 Total efficiency

The efficiency, taking into account all the power losses, is:

$$\text{Efficiency} = \frac{P_{out}}{P_{out} + P_{transis_{low}} + P_{transis_{high}} + P_{transformer} + P_{diod} + P_{ind}} = \frac{800}{800 + 13{,}06 + 12 + 7{,}35 + 17{,}28 + 0{,}7} \approx 0.94 \quad (57)$$

3.2.5. Cost

The final cost of the topology designed and simulated would be depicted in the below table. Each item is shown with a description, the quantity and the cost (for 10 units).

Description	Qtty	Cost/ud	Total
Transistor 80 V, R10m, Infineon	4	1,55 €	6,20 €
Transistor 550 V, R0.5, Infineon	4	0,84 €	3,34 €
Extra fast diode, 600V	4	1,44 €	5,76 €
Core PQ 20/20 3C90	2	1,50 €	3,00 €
Core ETD59/31/22	2	4,00 €	8,00 €
Bobbin PQ 20/20	1	0,80 €	0,80 €
Inductor 560nH	1	0,48 €	0,48 €
Electrolytic capacitor, 4.7 uF	1	0,17 €	0,17 €
Ceramic capacitor, 2.2 uF	1	2,80 €	2,80 €
Heat sink T0220, Rd-amb19,7	4	0,71 €	2,85 €
Heat sink T0220, Rd-amb6.4	4	0,40 €	1,60 €
AWG8	1	0,90 €	0,90 €
AWG16	5	0,25 €	1,25 €
AWG20	2	0,29 €	0,58 €
		Total	**37,73 €**

4. Conclusion

The study of market available topologies, their behavior and operation, the simulation performed, the control used, the sizing of the elements and their losses calculation have made me increase my technical knowledge. Besides, engineering tools as Matlab, Simulink, Plecs… have been used and knowledge previously acquired during the Electronics and Automation degree has been applied.

Several designs for a power inverter have been considered along the report. The requirements for the designs to be valid were the RMS voltage value of 230 Vac, an efficiency over 90 %, the applicable normative achievement, the reactive energy acceptance and an overall reduced cost.

Having in mind all these variables, the final topologies that have been further studied are the DC/AC/AC and the DC/AC/DC/AC (multi-stage) design. Both designs have followed the same steps in their study. The values of the elements have been calculated, then the topology for each design has been simulated in order to check the achievements of the technical requirements. Once it is checked as operative, the selection of the components, the efficiency and the cost calculation for each one of the topologies has been performed.

In order to select one of the two studied topologies for the application, several arguments and comparisons have been introduced.

In terms of reliability the DC/AC/AC design offers a good option because of its simplicity and its reactive energy acceptance. No matter how inductive the load is since the energy has always a way back to the source. The multi-stage design must treat this reactive energy via the intermediate capacitor. This capacitor can operate with an inductive load but its waveform would get deformed, it is limited.

Both topologies have reached the requirements with different controls, filters and facility. In the DC/AC/AC design, the control is unipolar PWM at 18 kHz and in the multi-stage design it is a variable phase PWM in order to use a high-frequency operating transformer. The unipolar PWM has not zero medium voltage along the switching period (as the variable-phase has) then, a 50 Hz laminated core transformer is needed. These are big, heavy and less efficient than a high frequency ferrite one.

Considering both designs valid, the cost of the multi-stage inverter is much smaller than the DC/AC/AC. That is because of the 50 Hz transformer used in the design which needs a high number of turns in a big size core which result in an important amount of money spent on wire. The multi-stage design has besides more integration grade because of the reduced transformer size, being the inclusion of the inverter in the P2S system a possibility in the future.

Then, the DC/AC/DC/AC design with the multi-stage topology has been selected as most suitable for the application. The next step would be its construction on proto board for real measurement of each one of the components and their behavior. That would easy the adjustment of the values, selection of different references and a real efficiency calculation.

5. Bibliography

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