ISSN 0280-5316
ISRN LUTFD2/TFRT--5691--SE

Automatic Gain Control in High Speed WCDMA Terminals

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September 2002

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Document name
MASTER THESIS

Date of issue
September 2002

Document Number
ISRN LUTFD2/TFR--5691--SE

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Sponsoring organization

Title and subtitle
Automatic Gain Control in High Speed WCDMA Terminals. (Skattning av inertialparametrar)

Abstract
In this study, it is investigated how different parameters influence 16QAM modulation. The focus is on how different parameters in the Automatic Gain Control algorithm influence raw bit error rates, but other parameters such as frequency error and misplaced decision levels are also investigated. The goal is not to develop optimal parameter configurations, but to gain some understanding on what parameters that are of great importance. The simulations are made with several types of fading multi path channels as well as Additive White Gaussian Noise (AWGN)channels. The investigations are carried out through simulations in a simulation environment implemented in Matlab.

From the simulations the conclusion is drawn that 16QAM is more sensitive to frequency errors than QPSK and that an important parameter in the AGC is the DC blocker bandwidths.The optimal AGC design with repsect to bit error rate depends on the type of channel model used, but it seems that a slower AGC design is preferred when compared to a faster one. The step resonse simulations indicate that there is no problem with using a fast AGC. The AGC seems to be more important at high signal to noise ratios because the fading become more visible in that case.

Keywords

Classification system and/or index terms (if any)

Supplementary bibliographical information

ISSN and key title
0280-5316

ISBN

Language
English

Number of pages
82

Recipient's notes

Security classification

Automatic Gain Control in High Speed WCDMA Terminals

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September 16, 2002

Preface

This Master Thesis was done in cooperation between Ericsson Mobile Platforms AB (Research Department), Lund and the Department of Automatic Control at Lund Institute of Technology during the spring and summer 2002.

I would like to thank my supervisors at Ericsson, Bo Bernhardsson and Bengt Lindoff, and my supervisor at the Department of Automatic Control, Anders Rantzer, for their great support and innovative ideas. I would also like to thank the Research Department at Ericsson for their support and for giving my some insight on corporate research.

Lund, September 2002

Peter Alriksson

Contents

1 Introduction

1.1 Background

The first nation wide mobile phone network in Sweden was the Nordic Mobile Telephony or NMT network. To be able to allow more than one user at the same time, each terminal was assigned a different frequency. The NMT network is referred to at the first generation or 1G of mobile networks.

The most common mobile network in use today is the Global System for Mobile Communication or GSM network. At present the GSM network is mainly used for speech services and simple messaging services like Short Messaging Service (SMS). The introduction of the Wireless Application Protocol or WAP gave the GSM users the possibility to use World Wide Web services. In a GSM network the Time Division Multiple Access allows more then one user to use the network at the same time. The GSM network is often called the second generation mobile network or 2G. For more information on GSM see for example [7].

The third generation or 3G of mobile networks will offer speech and data services just as the GSM network, but at much higher data rates. The third generation mobile network uses Code Division Multiplexing or CDMA instead. In a CDMA system many users share both time and frequency, this is accomplished by assigning a unique spreading code to each transmitter as further described below. Another advantage with CDMA is the possibility to allow each user to have access to multiple data channels with variable bit rates. This is accomplished by assigning an orthogonal code to each individual data channel within the same transmitter. The system that will be used in Europe is called Wide band Code Division Multiplex or WCDMA and is a CDMA system.

When a user wants to download large amounts of data from the base station to the terminal, the data rates achieved might be to low. To be able to further increase peak data rates, new modulation techniques together with new protocols will be introduced. One such protocol is the High Speed Downlink Packet Access or HSDPA, which is an evolution of WCDMA. One idea in HSDPA is to direct a very big portion of a base stations total power to one user for a short period of time. This together with new modulation techniques will hopefully give great improvements to peak data rates. HSDPA also introduces new protocols at higher levels, but that is beyond the scope of this thesis. HSDPA will be present along the basic services in 3G. The goal of HSDPA is to be able to deliver very high data rates if the receiving conditions are propitious.

1.2 Problem Formulation

When changing modulation technique, the requirements of both transmitter and receiver increase. This thesis focuses on the problems that might occur due to imperfections in the receiver. The main focus is how Automatic Gain Control (AGC) degrades performance. For more information on different modulation techniques see for example [1]. To investigate this, a number of simulations will be made. Different AGC parameters will be investigated together with general parameters in the communication system. All simulations will be made in a self made simulation environment implemented in Matlab. Implementing the simulation environment is the most time consuming part of the thesis work and

thus the main part. The goal of this thesis is to try to isolate important parameters in the AGC and to evaluate how much the influence of these parameters degrades the total performance of 16QAM in means of raw bit error. There is no intention to truly optimize the parameters, but to gain an understanding of where problems might occur.

2 A WCDMA Transmission System

2.1 Transmitter

This section describes the basic principles of a WCDMA communication system. This thesis only describes the link between base station and user equipment or UE. This link is referred to as the down link. First a transmitter will be developed, then a multi path fading channel model will be described and finally a receiver structure able to cope with the multi path properties of the communication channel will be suggested.

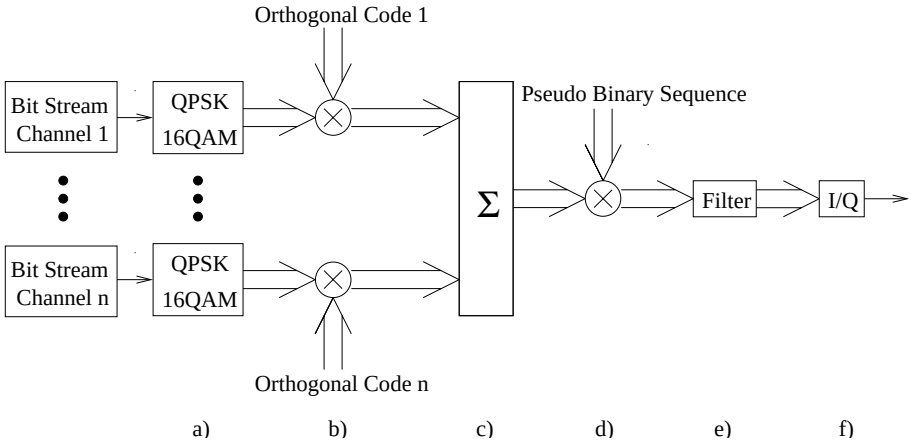

Figure 1: A WCDMA base station transmitter contains: a) binary to complex mapping (either QPSK or 16QAM), b) orthogonal spreading, c) power weighting, d) multiplication with a pseudo binary sequence, e) low pass filtering and f) radio modulation (I/Q).

2.1.1 Coding and Interleaving

The first step in the transmitter chain is coding and interleaving of the raw signal. This is used to correct bit errors. This is however beyond the scope of this thesis, so from here on we will only investigate the raw error rate, without coding and interleaving. The bit stream displayed in Figure 1 is the bit stream after coding and interleaving. For a description of coding and interleaving see e.g. [1].

2.1.2 Binary To Complex Mapping

To be able to transmit a binary sequence over a radio channel the binary sequence has to be transformed to an analog waveform. One way to do this is to first map the binary digits to complex symbols using e.g. QPSK or 16QAM modulation. This is represented as block a) in Figure 1. For more information concerning different modulation techniques see [1]. The binary sequence is mapped to complex symbols using gray coding (see figure 2). The reason for this coding is that if a received symbol is misinterpreted as a neighboring

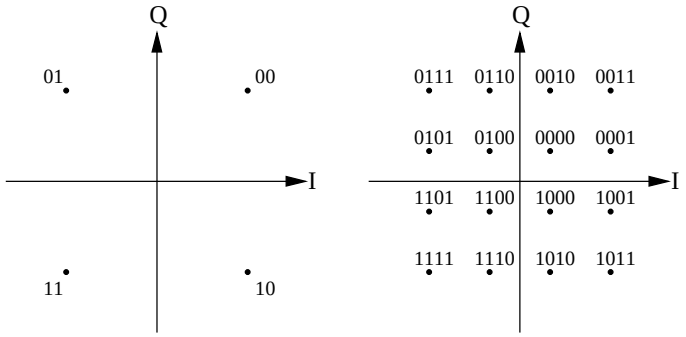

Figure 2: Quadrature Phase Shift Keying (QPSK) and 16 Quadrature Amplitude Modulation (16QAM) signal space diagram

symbol only one of the data bits will be wrong. In QPSK there are 4 different symbols, one in each quadrant of the complex space. This implies that each symbol represents two information bits. The modulation scheme 16QAM on the other hand has 16 evenly spaced symbols, therefore every symbol represents 4 bits.

2.1.3 Spreading

A Code Division Multiple Access or CDMA system is built on the principle that a narrow band signal i spreaded to a much wider bandwidth and therefore is less sensitive to disturbances. The technology was first used by the military in the 1950s. In a general CDMA system each complex user symbol U is multiplied with a complex spreading sequence, referred to as chips. The length of this sequence is called the spreading factor S_f. As a result of this the sequence will have a rate of R times S_f where R is the user symbol rate. That is, for each user symbol an entire sequence of length S_f is transmitted. The reason for the name spreading is that a narrow band signal is widened, spread, to a wider spectrum. As a result of this all user data signals, independent of bandwidth, occupy the same bandwidth after spreading. Spreading is represented as block b) in Figure 1.

In WCDMA,which is a cellular CDMA system, each transmitter can use several independent data channels. Each channel n is assigned a real valued spreading sequence C_n^o. The sequence C_n^o is chosen to be orthogonal to all other spreading codes within the same transmitter. One way to choose such codes is to use the so called Walsh Code Tree, see Appendix A. To be able to support variable data rates in WCDMA the orthogonal spreading codes can be chosen to have different lengths. The length is chosen so the total chip rate after spreading is constant equal to 3840000 chips per second (cps). The spreading factor can be chosen as multiples of 2 in the interval [4,512] which implies symbol rates between 960k symbols per second (sps) and 7.5ksps. A commonly used unit in WCDMA contexts is a slot. A slot is defined as 2560 chips. For more details on WCDMA see [3].

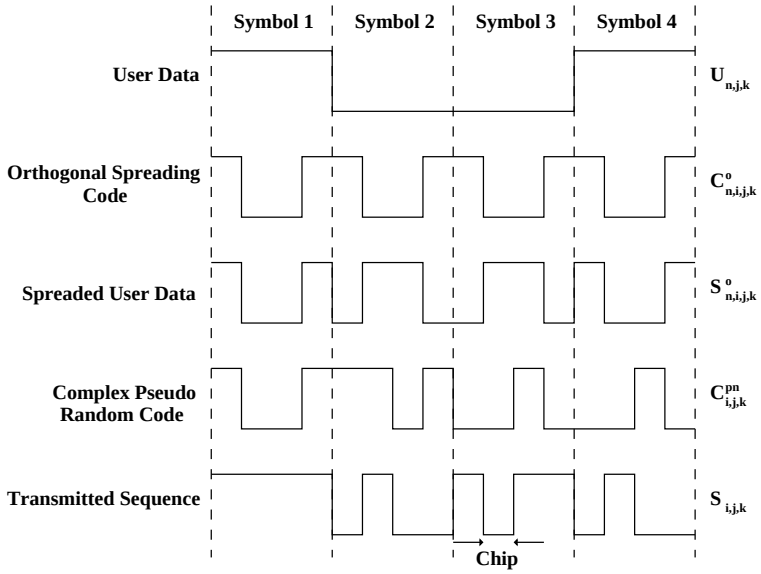

Figure 3: First each user symbol is multiplied with a Walsh code of length 4. This corresponds to a spreading factor $S_f = 4$. Then the spread user sequence is chip-wise multiplied with a pseudo random sequence. The resulting sequence is then transmitted. In this example only the real parts of the complex sequences are considered. For simplicity only one channel is considered.

The spread user symbol sequence from channel n can be written as

$$S^o_{n,i,j,k} = C^o_{n,i,j,k} \cdot U_{n,j,k} \tag{1}$$

The notation above gives the signal of interest from channel n, for chip i in symbol j and slot k, where $i = 0, 1...S_f - 1$ and $j = 0, 1...N_s - 1$. The user symbols $U_{n,j,k}$ are constant during one symbol ($i = 0...S_f - 1$) and N_s denotes the number of symbols per slots

$$N_s = \frac{2560}{S_f}$$

After spreading, all different channels are weighted and added together in the transmitter:

$$S^o_{i,j,k} = \sum_n \alpha_{n,k} \cdot S^o_{n,i,j,k} \tag{2}$$

Equation (2) corresponds to part c) in Figure 1.

To be able to distinguish between different transmitters the weighted sum $S_{i,j,k}$ is then multiplied with a complex pseudo random sequence denoted $C^{pn}_{i,j,k}$

$$S_{i,j,k} = S^o_{i,j,k} C^{pn}_{i,j,k} \tag{3}$$

Equation (3) corresponds to part d) in Figure 1 Because of the white noise properties of $C^{pn}_{i,j,k}$ all other transmitters will appear as a white noise disturbances at the receiver. For a graphical representation of spreading see figure 3.

To gain further understanding of the principles behind WCDMA a short example will be given. Let us assume that the binary sequences [10] and [00110110] are to be transmitted on two different channels. Channel one could for example be a slow speech channel whereas channel two could be a high speed video channel. To achieve different data rates spreading codes of different lengths must be chosen. Channel one will be assigned the real valued spreading code [1,1,1,1,-1,-1,-1,-1] and channel two the spreading code [1,1,-1,-1]. These two codes are orthogonal to each other. To further increase the data rate of channel two 16QAM modulation will be used whereas the slow channel one will use QPSK modulation. First the binary sequences are transformed to a complex representation according to figure 2. The two complex representations would then be:

$$\begin{aligned} U_1 &= \frac{1}{\sqrt{2}}[1-i] \\ U_2 &= \frac{1}{\sqrt{10}}[3+3i, -1+3i] \end{aligned}$$

To simplify calculations the complex symbols are normalized so that a sequence of symbols which are equally probable has mean power 1. After spreading, the complex sequences are given by:

$$\begin{aligned} S_1^o &= \frac{1}{\sqrt{2}}[1-i, 1-i, 1-i, 1-i, -1+i, -1+i, -1+i, -1+i] \\ S_2^0 &= \frac{1}{\sqrt{10}}[3+3i, 3+3i, -3-3i, -3-3i, -1+3i, -1+3i, 1-3i, 1-3i] \end{aligned}$$

Then both sequences are weighted with α_1 and α_2 respectively and added together. To be able to separate different transmitters from each other the weighted sum is chip wise multiplied with a complex pseudo random sequence. The next step is filtering and I/Q modulation which is covered in the next section.

2.1.4 Filtering and I/Q Modulation

To contain RF bandwidth the complex sequence $S_{i,j,k}$ has to be filtered through a low pass filter. This can be represented by first converting the complex sequence $S_{i,j,k}$ to a continuous complex function given by

$$s(t) = \sum_{k=0}^{\infty} \sum_{j=0}^{N_s-1} \sum_{i=0}^{S_f-1} \delta\left(t - T_c[i + S_f(j + kN_s)]\right) \cdot S_{i,j,k} \tag{4}$$

where T_c denotes the pulse length. In WCDMA $T_c = \frac{1}{3.84MHz} \approx 0.26\mu s$. Further let

$$s_f(t) = s(t) * h(t) \tag{5}$$

denote the convolution between the complex function and a pulse shaping filter $h(t)$. This filtering is represented as block e) in Figure 1. At the receiver the received signal is once again filtered through $h(t)$ and thus the total filter is $h(t) * h(t)$. The received signal is then sampled at chip rate. To avoid inter symbol interference at the receiver, $h(t)$ is often chosen so that $h(t) * h(t)$ has its

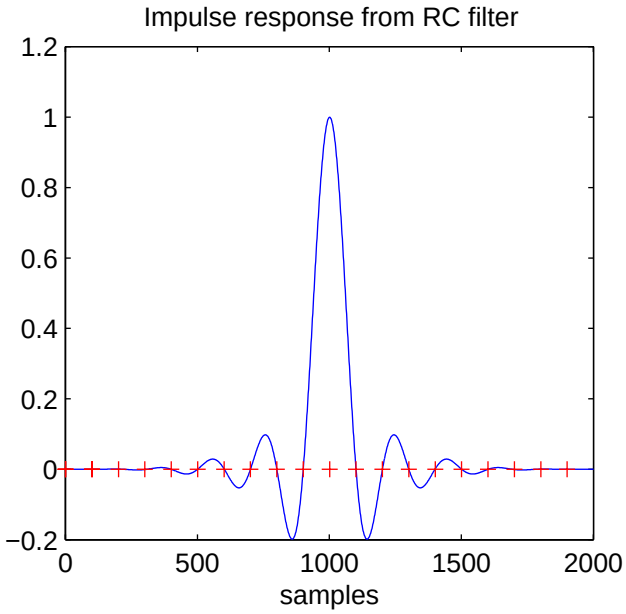

Figure 4: Impulse response from Raised Cosine pulse shaping filter. Note that the ideal impulse response is zero at sample points marked with a plus sign.

zero-crossings at multiples of T_c, see figure 4. In WCDMA the filter is chosen as a Root Raised Cosine filter which implies that the total filter is a Raised Cosine filter.

The resulting waveform $s_f(t)$ is called the low pass equivalent of the transmitted signal

$$s_{HF}(t) = \Re\left\{s_f(t)\sqrt{2}e^{2\pi i f_c t}\right\} \tag{6}$$

Equation (6) corresponds to part f) in Figure 1. Because the low pass equivalent can be written as $s_f(t) = I(t) + iQ(t)$, the last step is referred to as I/Q-modulation at carrier frequency f_c. The carrier down link frequencies in WCDMA ranges from 2110MHz to 2170MHz. To maintain power normalization the low pass equivalent is multiplied with $\sqrt{2}$. Using this notation the transmitted signal can be written as

$$s_{HF}(t) = I(t)\sqrt{2}cos(2\pi f_c t) - Q(t)\sqrt{2}sin(2\pi f_c t) \tag{7}$$

2.2 Multi Path Fading Channels

When a radio signal is transmitted over land the radio channel is characterized by multiple reflections and therefore strong variations in received signal energy. This is caused by reflection against natural objects in the environment, a phenomena called multi path propagation.

In WCDMA the chip duration corresponds to a distance of about 78m ($cT_c = 3 \cdot 10^8/3840000 \approx 78$). Typical path length differences in urban areas range from 200m to 300m. This means that multiple copies of the same chip do not

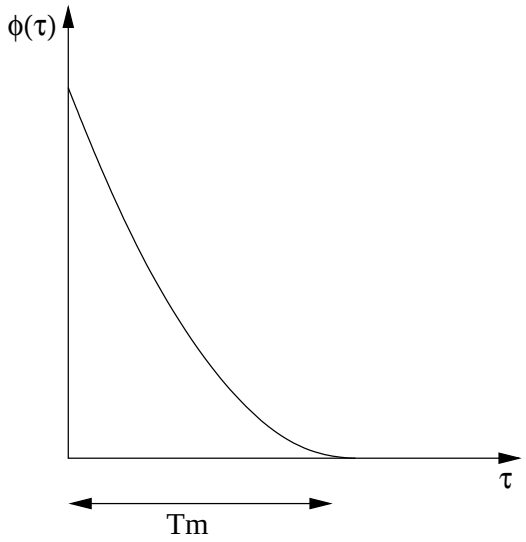

Figure 5: Intensity profile of one fading path in a radio channel. The delay spread Tm is usually much shorter than the chip duration T_c.

overlap. Under that assumption reflections from different objects can be treated as separate paths and thus separated by the receiver (see [3]). In the following section a model for one such path will be developed, see [2].

2.2.1 Flat Fading Channels

A general model of a time-varying communication channel can be represented as a time-variant linear system with noise added at its output. In this section the noise will be neglected. The output from such a channel can be written as

$$r(t) = \int h(\tau; t) s_f(t - \tau) d\tau \tag{8}$$

where $h(\tau; t)$ denotes the complex time-varying impulse response and $s_f(t)$ the low pass equivalent output from the transmitter. Further let

$$H(f; t) = \int h(\tau; t) e^{-i2\pi f \tau} d\tau \tag{9}$$

denote the Fourier transform of $h(\tau; t)$ with respect to τ. Now lets investigate some of the statistical properties of $h(\tau; t)$. If $h(\tau; t)$ is assumed to be wide Sense Stationary the autocorrelation function of $h(\tau; t)$ with respect to τ can be defined as

$$\phi(\tau_1, \tau_2; \Delta t) = E[h(\tau_2; t + \Delta t) h^*(\tau_1; t)] \tag{10}$$

If components of the received signal with delay τ_1 are uncorrelated with components with delay τ_2 the channel is called an Uncorrelated Scattering Channel. Under this assumption (10) can be written as

$$\phi(\tau_1, \tau_2; \Delta t) = \phi(\tau_2; \Delta t) \delta(\tau_2 - \tau_1) \tag{11}$$

The intensity profile of the channel $\phi(\tau, 0) = \phi(\tau)$ is a measure of the expected received power as function of delay. The delay spread Tm (see figure 5) is typically less than the chip duration T_c, which implies that each path can be treated as a flat fading channel (see [3]). Under the assumption of flat fading the output can be written as (see [2])

$$r(t) = H(0;t)s_f(t) \tag{12}$$

Now let's investigate the time variations of $H(0;t)$. Let's assume a receiver moving at speed v m/s receiving multiple signals with different delays all less than T_c. Due to the Doppler effect different waves experience different frequency shifts

$$f_D = \frac{f_c v}{c}\cos(\theta) \tag{13}$$

where f_c denotes the carrier frequency and θ the angle of incidence.

2.2.2 Multi Path Channels

Under the assumptions in Section 2.2, a multi path channel can be view as several flat fading channels added together and with white noise added to the output. The output can thus be written as

$$r(t) = \sum_p H_p(0,t)s_f(t-\tau_p) + e(t) \tag{14}$$

Where τ_p denotes the delay of path p and $e(t)$ is white noise with variance I_{oc}.

2.3 WCDMA Receiver

2.3.1 I/Q Demodulation

To retrieve the complex signal $s_f(t)$ the received signal $s_{HF}(t)$ (see 6) is first split into two parts. Then each part is multiplied with $\sqrt{2}\cos(2\pi f_c)$ or $-\sqrt{2}\sin(2\pi f_c)$ respectively.

$$\begin{aligned} \hat{I}(t) &= s_{HF}(t)\sqrt{2}\cos(2\pi f_c) = & (15)\\ &= I(t)(1+\cos(4\pi f_c t)) - Q(t)sin(4\pi f_c t) & \\ \hat{Q}(t) &= -s_{HF}(t)\sqrt{2}\sin(2\pi f_c) = & (16)\\ &= Q(t)(1-\cos(4\pi f_c t)) - I(t)sin(4\pi f_c t) & \end{aligned}$$

The next step is low pass filtering of the signals $\hat{I}(t)$ and $\hat{Q}(t)$ and then forming the complex signal

$$\hat{s_f}(t) = \hat{I}(t) + \hat{Q}(t)i = I(t) + iQ(t) \tag{17}$$

Now lets assume a frequency error Δf in the receiver and thus

$$\begin{aligned} \hat{I}(t) &= s_{HF}(t)\sqrt{2}\cos(2\pi(f_c+\Delta f)) & (18)\\ \hat{Q}(t) &= -s_{HF}(t)\sqrt{2}\sin(2\pi(f_c+\Delta f)) & (19) \end{aligned}$$

Using basic trigonometric identities it is possible to show that the resulting received signal equals

$$\hat{s_f}(t) = s_f(t)e^{-2\pi\Delta f} \tag{20}$$

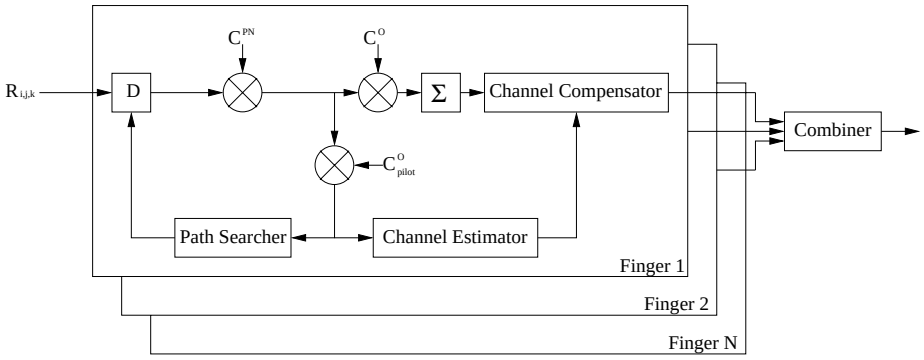

Figure 6: Principles of the RAKE receiver. Input to the RAKE receiver is the I/Q demodulated, filtered, sampled and A/D converted signal $R_{i,j,k}$.

2.3.2 Filtering and A/D Conversion

To retrieve the complex sequence $S_{i,j,k}$ the received signal $\hat{s}_f(t)$ is filtered, sampled and A/D- converted. Choosing the filter as the exact same filter used in the transmitter and sampling at the correct moments, minimizes the probability of error (see e.g. [1]). Because of the strong amplitude variations in the received signal, the A/D converter must have a very big dynamic range. In a mobile terminal this is not cost and power efficient, which motivates another solution. One possible approach is the use of an amplifier with variable gain prior to A/D conversion. This device is constructed in such a way that it tries to keep the signal power constant in the dynamic range of a much simpler A/D-converter. This device, called AGC, will be described in further detail in Section 3.

2.3.3 RAKE Receiver

A receiver has to be able to cope with the fading and multi path properties of the channel mentioned in Section 2.2. One such receiver is the so called RAKE receiver. The RAKE receiver can be view as a number of receivers each tracking its own signal path, these are referred to as RAKE fingers. The output from each finger is then combined to a total received signal. The receiver can be split into four parts, where each finger contains the first three parts (see Figure 6).

- Path searching and path tracking
- Correlators
- Channel estimation and compensation
- Combining

2.3.4 Path Searching and Path Tracking

The task of this part is to identify the time delay positions with significant energy and delay the signal sent to the correlators. This is a rather complicated area that is beyond the scope of this thesis. For information on Path Searching and Path Tracking see [8],[6] and [9].

2.3.5 Correlators

Assuming the channel model in section 2.2, perfect sampling and perfect path tracking the received signal in each finger is given by

$$R_{i,j,k} = S_{i,j,k} \cdot h_{i,j,k} + e_{i,j,k} \tag{21}$$

and according to section 2.1

$$S_{i,j,k} = \sum_{n} \alpha_n C^{PN}_{i,j,k} C^{o}_{n,i,j,k} U_{n,j,k} \tag{22}$$

The notation above gives the signal of interest from channel n, for chip i in symbol j and slot k, where $i = 0, 1...S_f - 1$ and $j = 0, 1...N_s - 1$. The noise $e_{i,j,k}$ consists of both thermal noise and signals transmitted by other transmitters at the same frequency band. The disturbance $e_{i,j,k}$ is assumed to be white Gaussian noise with mean value 0 and variance I_{oc}.

To retrieve the complex sequence of user data symbols for channel n, $U_{n,j,k}$, the received sequence is first multiplied with the conjugate of the transmitters complex spreading code $C^{PN}_{i,j,k}$ and then multiplied with the orthogonal code $C^{o}_{n,i,j,k}$ corresponding to channel n. This product is then integrated over one symbol

$$\hat{U}^{''}_{n,j,k} = \frac{1}{S_f} \sum_{i=0}^{S_f - 1} (C^{PN}_{i,j,k})^* C^{o}_{n,i,j,k} (S_{i,j,k} h_{i,j,k} + e_{i,j,k}) \tag{23}$$

using the properties of $C^{o}_{n,i,j,k}$ and $C^{PN}_{i,j,k}$ together with the assumption that the channel is constant during one symbol (23) reduces to

$$\hat{U}^{''}_{n,j,k} = \alpha_n U_{n,j,k} h_{j,k} + e^{'}_{j,k} \tag{24}$$

The noise component $e^{'}_{j,k}$ is still considered white Gaussian noise but is now suppressed by a factor S_f compared to $e_{i,j,k}$.

2.3.6 Channel Estimation and Compensation

To be able to retrieve the transmitted symbols after the fast phase and amplitude disruption of the fading channel, a channel compensation has to be made. The first task is to make a channel estimate. WCDMA transmitters are always equipped with a so called Pilot Channel. This is a channel with spreading factor $S_f = S^p_f$ only transmitting a prior known sequence of symbols. By multiplying the received pilot symbols with the conjugate of the known pilot symbols and then summing over N_p symbols a primary channel estimate is obtained as

$$\begin{aligned} \hat{h}_{j,k} &= U^*_{pilot,j,k} \hat{U}^{''}_{pilot,j,k} \\ \hat{h}_k &= \tfrac{1}{N_p} \textstyle\sum_{j=0}^{N_p - 1} \hat{h}_{j,k} \\ \hat{h}_k &= \alpha_{pilot} \overline{h_{j,k}} + e^{''}_k \end{aligned} \tag{25}$$

where $\overline{h_{j,k}}$ denotes the mean value of $h_{j,k}$ during slot k. Because the close relationship in structure of (23) and (25) the noise component $e^{''}_k$ is also assumed

to be white Gaussian noise but with variance $\frac{I_{oc}}{S_f^p N_p}$ and mean 0. The primary channel estimate could then be used in other channel estimate algorithms or used as a channel estimate for slot k itself. A simple channel compensation is to multiply the received symbols $\hat{U}''_{j,k}$ from channel n with the conjugate of the primary channel estimate $\hat{h}_k$ for slot k according to

$$\hat{U}'_{n,j,k} = \alpha_n h_{j,k} \hat{h}_k^* U_{n,j,k} + e'_{j,k} \tag{26}$$

If the variations of $h_{j,k}$ are slow compared to the slot rate, that is if the channel experienced during symbol j is approximately constant equal to the mean value of the channel experienced during the entire slot k or

$$h_{j,k} \approx \overline{h_{j,k}} \tag{27}$$

This assumption is reasonable for moderate vehicle velocities. Under that assumption (26) reduces to

$$\hat{U}'_{n,j,k} \approx \alpha_n \alpha_{pilot} |\overline{h_{j,k}}|^2 U_{n,j,k} + e'''_{j,k} \tag{28}$$

This thus leads to a good phase compensation for moderate vehicle velocities, but the amplitude disruption, i.e. $\alpha_n \alpha_{pilot} |\overline{h_{j,k}}|^2$ is not compensated for.

2.3.7 Combining

To be able to utilize all received power the output from each finger has to be combined in some way. Here three different methods will be briefly described; Select Biggest, Equal Gain Combining and Maximal Ratio Combining.

The Select Biggest approach simply selects the finger which receives most power, that is the finger for which $|\hat{h}_k|$ is the greatest. Equal Gain Combining adds all fingers as

$$\hat{U}_{n,j,k} = \sum_{f=0}^{N_f - 1} (\hat{U}')_{n,j,k}^f \tag{29}$$

where $(\hat{U}')_{n,j,k}^f$ denotes the compensated complex sequence from finger f and N_f the number of fingers.

In the Maximal Ratio approach the first step is to statistically describe how good each finger is. This can be done by e.g. estimating the variance of the channel estimate for each finger. Let $\hat{h}_k^f$ denote the channel estimate for slot k in finger f. Then one possible variance estimate can be obtained as

$$I_k^f = Var(\hat{h}_{j,k}^f) = \frac{1}{N_p - 1} \sum_{j=0}^{N_p - 1} |\hat{h}_{j,k}^f - \hat{h}_k^f|^2 \tag{30}$$

Using this estimate in (29) the following combined output can be obtained

$$\hat{U}_{n,j,k} = \sum_{f=0}^{N_f - 1} \frac{(\hat{U}')_{n,j,k}^f}{I_k^f} \tag{31}$$

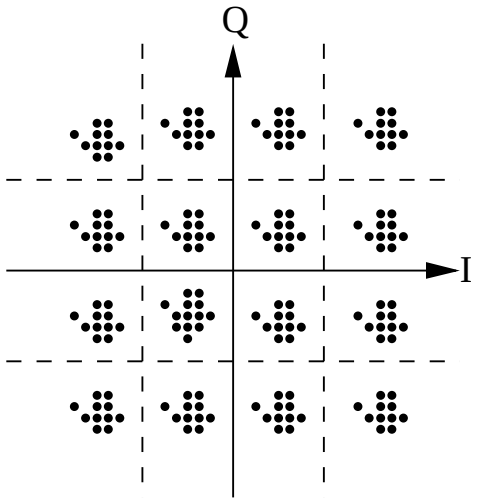

Figure 7: Ideal location of decision levels for 16QAM (dashed).

2.3.8 Hard Detection

After retrieving the complex sequence $\hat{U}_{n,j,k}$ a decision on which symbol that was transmitted has to be made. A real WCDMA system uses so called soft decisions because of the coding of the bit sequence prior to transmission. Coding and soft decisions are however beyond the scope of this thesis, so only hard decision will be considered. For a description of soft decisions see for example [1]

The channel compensation mentioned in Section 2.3.6 leads to a phase compensation whereas the amplitude disruption is uncompensated for. When QPSK modulation is used the amplitude information is not necessary to make a correct decision. The decision is only based on the phase of the received symbol. To be able to make a decision for a symbol sent using 16QAM the amplitude information is however essential.

2.3.9 Choice of Decision Levels

When using 16QAM the choice of decision levels, see Figure 7, is a non trivial problem. In this section two simple methods will be presented. One way of making the decision is to let the base station signal the transmitted power, that is the specific α values, to the UE. To be able to decide where to put the decision levels the channel estimate $\hat{h}_k$ has to be close to the real channel $h_{j,k}$. If this is the case the levels can be placed using equation (28) with $U_{n,j,k}$ equal to $\frac{2}{\sqrt{10}}$. A problem with this approach is that $|\overline{h_{j,k}}|^2$ is unknown. This can be solved by using the channel estimate from (25). When more then one finger is used the channel estimate from all fingers are used with or without weights depending on combining method. One reasonable choice of decision level for Maximal Ration combining would thus be

$$D_{n,k} = \frac{2}{\sqrt{10}} \frac{\alpha_n}{\alpha_{pilot}} \sum_{f=0}^{N_f-1} \left| \frac{\hat{h}_k^f}{I_k^f} \right|^2 \tag{32}$$

The Equal Gain Combining and Select Biggest Combining are just special cases of Maximum Ratio Combining. The method used above has one big drawback, the base station has to send power information once every slot. A way around this involves making a power estimate of the received symbols in the receiver. Such an estimate could for example be made as follows

$$\hat{P}_{n,k} = \frac{1}{N_s} \sum_{j=0}^{N_s-1} \hat{U}_{n,j,k} \hat{U}^*_{n,j,k} \tag{33}$$

Using this estimate and knowledge of the amplitude levels in 16QAM, the amplitude decision levels could be determined. If the complex representation from section 2.1.3 is used one possible way of choosing the decision levels would be

$$D_{n,k} = \frac{2}{\sqrt{\hat{P}_{n,k}}} \tag{34}$$

Now lets investigate the quality of this choice compared to the number of symbols N_s. To simplify calculations the received user symbols $U_{n,j,k}$ will be assumed to be normal distributed with mean value 0 and variance $P = E\{U_{n,j,k}U^*_{n,j,k}\}$. It is also assumed that they are independent of each other, which is a good approximation for single path channels. To simplify notation the indexes n, k will be skipped. Now lets study the squared quotient between the true decision level

$$D^0 = \frac{2}{\sqrt{P}} \tag{35}$$

and the decision level D. Let the quotient equal

$$x = \frac{D}{D^0} = \frac{P}{\hat{P}} = \frac{P}{P+\epsilon} = \frac{1}{1+\frac{\epsilon}{P}} \tag{36}$$

, where ϵ has mean 0. Under the assumption that $\frac{\epsilon}{P} < 1$ it is possible to do a series expansion of (36) which gives

$$x = \frac{1}{1+\frac{\epsilon}{P}} \approx 1 - \frac{\epsilon}{P} \tag{37}$$

Now lets derive an expression for the standard deviation of x.

$$\begin{aligned}
Var\{\hat{P}\} &= E\{\hat{P}\cdot\hat{P}\} - E\{\hat{P}\}^2 = \\
&= \frac{1}{N_s^2} E\left\{ \sum_{i=0}^{N_s-1} U_i U_i^* \cdot \sum_{j=0}^{N_s-1} U_j U_j^* \right\} - P^2 = \\
&= \frac{1}{N_s^2} \sum_{i=0}^{N_s-1} \sum_{j=0}^{N_s-1} E\{U_i U_i^* U_j U_j^*\} - P^2 = \\
&= \frac{1}{N_s^2} \sum_{i=0}^{N_s-1} \sum_{j=0}^{N_s-1} (E\{U_i U_i^*\} E\{U_j U_j^*\} + \\
&+ E\{U_i U_j^*\} E\{U_j U_i^*\}) - P^2 = \\
&= P^2 + \frac{P^2}{N_s} - P^2 = \\
&= \frac{P^2}{N_s}
\end{aligned} \tag{38}$$

Which gives that

$$Var\{\epsilon\} = \frac{P^2}{N_s} \tag{39}$$

$$D\{x\} \approx \sqrt{\frac{1}{P^2} Var\{\epsilon\}} = \frac{1}{\sqrt{N_s}} \tag{40}$$

If for example a level error of y% percent is expected $x = 1 + y$. A good hint on the number of symbols, N_s, what should be used would then be

$$N_s \approx \frac{1}{y^2} \tag{41}$$

3 Automatic Gain Control

As mentioned in Section 2.3.2 the main function of the AGC is to limit the dynamic range of the AD converter. One of the two main requirements of the AGC is to have a large dynamic range. According to the 3G specifications (see [4]) the receiver must be able to handle signal levels between -106.7dBm and -25dBm, where x dBm= $10^{x/10}$ mW. This corresponds to a dynamic range of 81.7dB. The other main requirement is the settling time, i.e. the time it takes for the AGC to stabilize at a new gain level after a step has been made in received power. Such a step occurs for example when the WCDMA receiver makes measurements on the signal quality from neighbouring base stations. One possible scenario is that a neighbouring base station is transmitting at a different carrier frequency. The I/Q demodulator then changes carrier frequency for a short period of time, which leads to a abrupt change in received power. To minimize the measuring time the AGC must compensate for the new received power as fast as possible.

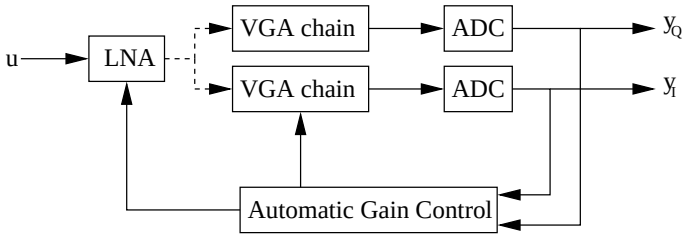

Figure 8: Simplified view of Automatic Gain Control, Variable Gain Amplifier Chain and Low Noise Amplifier.

To be able to understand the Automatic Gain Control or AGC algorithm, the surrounding blocks have to be briefly described. An overview of the AGC and the surrounding blocks can be found in figure 8.

3.1 Low Noise Amplifier

The LNA is implemented in the radio frequency part of the receiver and thus the first amplifier the received signal encounters. The low noise properties of the LNA is critical to the function of the receiver. The making of RF amplifiers with low noise properties is a difficult matter so therefore it is not efficient to have more than a few operating modes. The gain changes are modeled as instantaneous, which in reality of course is not the case.

3.2 Variable Gain Amplifiers

The next step after the LNA is two chains of Variable Gain Amplifiers or VGAs. The signal from the LNA is split up into its I and Q parts (see section 2.3.1) and then fed to the VGA chains. To be able to meet the dynamic requirements of 81.7dB the VGA chain consists of a number of VGAs with gains in the interval -15 to 15dB and with a resolution of between 0.5dB to 2dB.

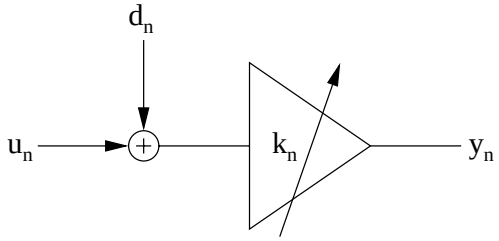

Figure 9: Model of one Variable Gain Amplifier with DC error d_n.

The VGAs are all modeled as a static gains, without any dynamics at all. The changes in gain happens instantaneously and to the exact value. In reality this is of course not the case. There is both a small time delay and a lack of accuracy in the gain. In this thesis these errors are not modeled. The DC offset induced by imperfections in the VGAs is modeled as a constant disturbance on the input of each VGA (see figure 9). This disturbance only changes when the gain of the amplifier is changed. If a very small DC disturbance, typically in the range of -5mV to 5mV, enters at the first amplifier the impact at the last step in the amplifier chain is very big. Lets assume a chain with 10 amplifiers each at their maximum gains 12dB. The disturbance will then be amplified a factor 120dB which equals a factor 10^6 in amplitude or a factor 10^{12} in power. This will probably lead to saturation somewhere in the amplifier chain and thus a great decay in performance. To counteract this, a DC compensation loop is inserted somewhere in the amplifier chain. If the compensation loop is inserted too early in the chain the risk of saturation will be greater towards the end. On the other hand if the compensation loop is inserted at the end of the amplifier chain saturation might occur before the loop. If the compensation loop is not placed at the last amplifier there will be a remaining DC error at the output of the chain. To compensate for this, the output from the amplifier chain is high-pass filtered.

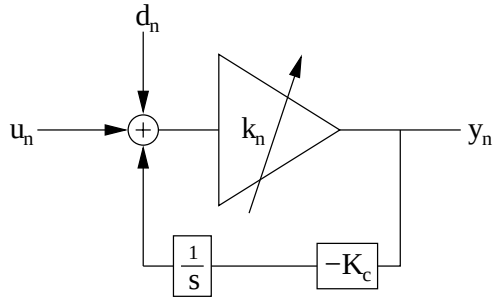

Figure 10: Model of one Variable Gain Amplifier with DC error d_n and DC compensation loop with gain K_c. The notation $\frac{1}{s}$ denotes an integrator.

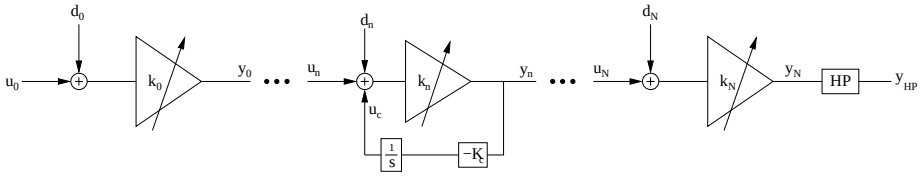

Figure 11: Model of VGA chain.

3.2.1 DC Compensation Loop

As mentioned in section 3.2 a DC compensation loop has to be inserted in the amplifier chain. A simple such compensation is to try to determine the DC level at the output y_n and the simply subtract it at the input. Perhaps the simplest way to determine the DC level at the output is to integrate the signal y_n. To be able to change the bandwidth of the compensation loop a constant K_c is inserted in the loop (see Figure 10). Using the notation in figure 10 an expression for the closed loop transfer function can be obtained as

$$G(s) = k_n \frac{s}{s + k_n K_c} \tag{42}$$

Using the common definition of bandwidth it is easily obtained that the bandwidth ω_c of $G(s)$ equals $k_n K_c$. Here one can observe that ω_c depends on k_n. To maintain the same bandwidth the integrator gain K_c has to be changed according to

$$K_c = \frac{\omega_c}{k_n} \tag{43}$$

3.2.2 State Space Model

The AGC is a nonlinear time varying system, which is hard to model analytically. The VGA chain on the other hand is a linear time invariant system as long as the gains are constant. Because the controller runs at a low speed compared to the chip rate it is possible to use this model between the sample points of the controller. Now lets derive a state space model (see e.g. [11]) for the VGA chain under the condition of constant gain k_n. Lets consider the VGA chain in Figure 11. The output from stage i can be written as

$$\begin{aligned} y_i &= k_i(u_i + d_i) && (44)\\ u_i &= y_{i-1} && (45) \end{aligned}$$

where i takes the values $i = 0, 1, .., N$ except for $i = n$. For this special case we have to consider the DC compensation loop. Using the notation in Figure 11 the output y_n from stage n can be written as

$$\begin{aligned} \frac{du_c}{dt} &= -K_c \cdot y_n && (46)\\ y_n &= k_n(d_n + u_c + u_n) && (47) \end{aligned}$$

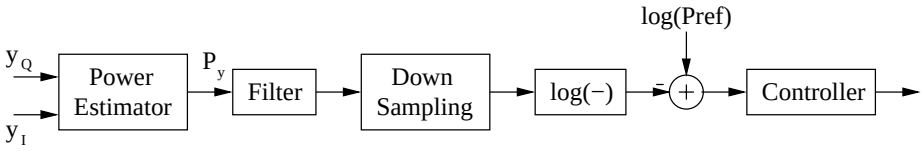

Figure 12: The control algorithm first forms the average instantaneous power P_y. Then P_y is low pass filtered and fed through a log function. The control error is then formed and fed to the regulator which calculates a new gain.

The last part of the VGA chain is the high pass filter HP. This filter is modeled as a first order HP filter with bandwidth ω_{HP}. One possible state space representation of such a filter is

$$\frac{dx}{dt} = -\omega_{HP} \cdot x + y_N \tag{48}$$

$$y_{HP} = y_N - \omega_{HP} \cdot x \tag{49}$$

Putting the equation above together gives a second order state space model as follows

$$\begin{bmatrix} \dot{x}(t) \\ \dot{u}_c(t) \end{bmatrix} = A \begin{bmatrix} x(t) \\ u_c(t) \end{bmatrix} + B \begin{bmatrix} u_0(t) \\ d_0(t) \\ \vdots \\ d_N(t) \end{bmatrix} \tag{50}$$

$$y_{HP}(t) = C \begin{bmatrix} x(t) \\ u_c(t) \end{bmatrix} + D \begin{bmatrix} u_0(t) \\ d_0(t) \\ \vdots \\ d_N(t) \end{bmatrix} \tag{51}$$

The matrixes A,B,C,D are all dependent on the gain $k_0 ... k_N$ and the chosen bandwidths ω_c and ω_{HP}.

3.3 The AGC Algorithm

The task of the controller is to control the two chains of VGAs and the LNA so that the estimated power is as close to a preferred value as possible. Because of the large dynamic range of the VGA chain the desired gain values A_k are represented in the logarithmic domain. A control algorithm that performs this task is presented in Figure 12.

First the I and Q channel are fed to a power estimator. One way to develop a power estimator is to first form the instantaneous mean power of the I and Q channel as

$$\hat{P}_y = \frac{y_I^2 + y_Q^2}{2} \tag{52}$$

The next task is to low pass filter $\hat{P}_y$ to form a time average of the received power. The low pass filter has bandwidth ω_{pow}, the choice of bandwidth is a trade of between speed and noise. A very low bandwidth will result in a

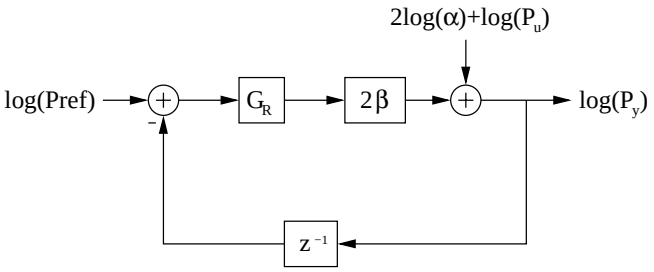

Figure 13: The control problem in the logarithmic domain.

slow tracking of received power which might lead to decreasing step response performance of the AGC. On the other hand a very high bandwidth will lead to a noisy power estimate which might lead to a lot of unnecessary gain changes. As mentioned in section 3.2 changes in gain induces DC disturbances.

Next the low pass filtered instantaneous power estimate is down sampled and compared to the reference value $Pref$. This control error is used as input to the controller which controls the VGA chain and LNA. The controller can send gain changes to the VGA chain and LNA one or several times per slot.

Now lets derive a simple model of the AGC. First lets assume that the LNA and VGA can be viewed as one amplifier placed after I/Q demodulation. If all VGA and LNA dynamics are neglected the output from the VGA chains and LNA can be written as

$$y_{I,Q} = \alpha e^{\beta A_k} u_{I,Q} \tag{53}$$

where α and β are constants depending on the dynamic range of the VGA chain. The approximation of no VGA dynamics is based on the fact that the controller works at a speed much lower then the bandwidth of the DC blockers and thus it is assumed that all DC transients have disappeared before the next gain change. The instantaneous power of y can then be written as

$$P_y = P_u(\alpha e^{\beta A_k})^2 \tag{54}$$

where P_u is the instantaneous power of the input u. If the time constant of the low pass filter is much shorter than the update rate of the controller the dynamics are reduced to a time delay and the problem can be viewed as a linear control problem in the logarithmic domain. Taking the logarithm of (54) gives

$$\log(P_y) = \log(P_u) + 2\beta A_k + 2\log(\alpha) \tag{55}$$

Using the control structure in figure 12 the problem can be viewed as a linear control problem with $\log(P_y)$ as the measured variable and A_k as controller output. The process to be controlled consists of a static gain 2β and a disturbance $\log(P_u) + 2\log(\alpha)$, see figure 13. The measured output P_y can then be written as

$$\log(P_y) = G_1(z)log(P_u) + G_2(z)log(P_{ref}) \tag{56}$$

where

$$G_1(z) = \frac{1}{1+2\beta G_R(z)z^{-1}} \quad G_2(z) = 2\beta G_R(z)G_1(z) \tag{57}$$

There are two objectives in the choice of $G_1(z)$. The AGC should be able to track and compensate for the fadings in P_u and have a low settling time after a step change in P_u. This implies a high pass structure of $G_1(z)$ with cut off frequency higher then the speed of the fadings. On the other hand the AGC must not destroy the modulation of the signal. That is, the cut off frequency must not be too high. The requirements on $G_2(z)$ is only to be able to keep a constant reference value, this correlates to a low pass structure with sufficiently high cut off frequency. Choosing a PI-controller on the form

$$G_R(z) = K_P + \frac{K_I}{z-1} \tag{58}$$

gives the transfer functions

$$G_1(z) = \frac{(z-1)z}{z^2 + (2\beta K_P - 1)z + (K_I - K_P)2\beta} \tag{59}$$

$$G_2(z) = \frac{(zK_P + (K_I - K_P))2\beta}{z^2 + (2\beta K_P - 1)z + (K_I - K_P)2\beta} \tag{60}$$

To be able to make a control design the constant β has to be determined. To be able to calculate β an assumption on the so called gain resolution must be made. As an example the VGA gain resolution could be chosen as 1dB. The constant β is determined by the following equation.

$$\alpha e^{\beta A_k} = 10^{\frac{\Delta G A_k}{20}} \tag{61}$$

Putting $\alpha = 1$ and the gain resolution Δ G=1dB gives

$$\beta = \frac{\Delta G}{10 log_{10}(e^2)} \approx 0.115 \tag{62}$$

One reasonable pole placement could for example be $z_{1,2} = 0.27 \pm 0.58i$ which corresponds to continuous poles with $\omega \approx 1.83 \cdot 10^4$ rad/s and $\zeta \approx 0.36$ if the AGC is run 10 times per slot. These poles correspond to $K_I = 3.8$ and $K_P = 2$. The Bode diagram for $G_1(z)$ and $G_2(z)$ can be found in figures 15 and 16. If both K_I and K_P are increased equally the poles will move according to the root locus in Figure 14. The system becomes instable if $K_I > 9.12$ and $K_P > 4.8$ which corresponds to a factor 2.4 larger then the original design.

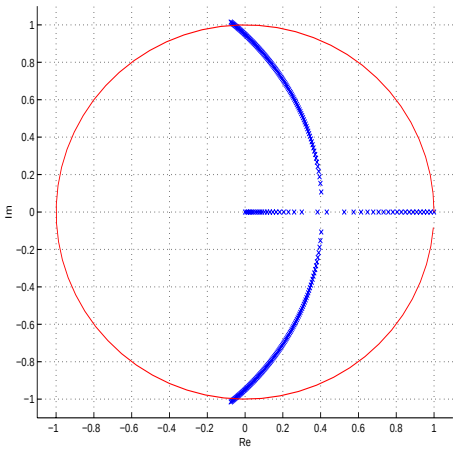

Figure 14: Root locus for $G_1(z)$. The system becomes instable for $K_I > 9.12$ and $K_P > 4.8$ which corresponds to a factor 2.4 larger then the original design.

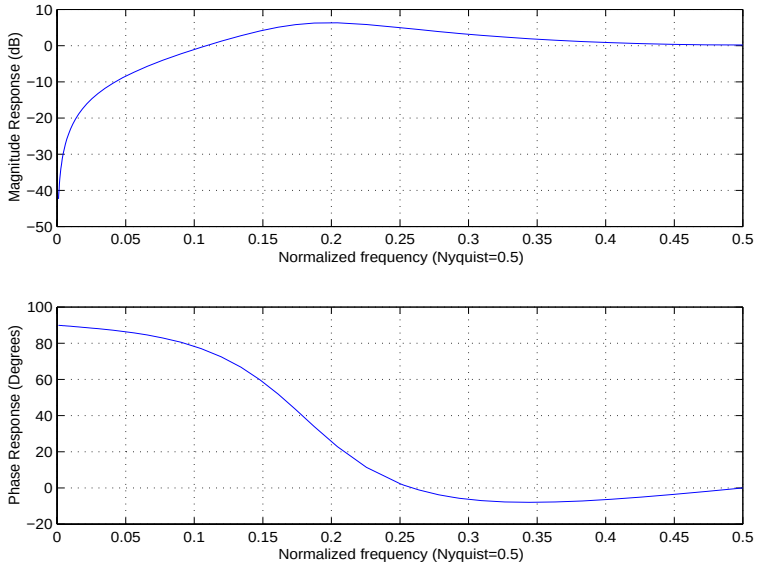

Figure 15: Bode diagram for $G_1(e^{i2\pi f/f_s})$.

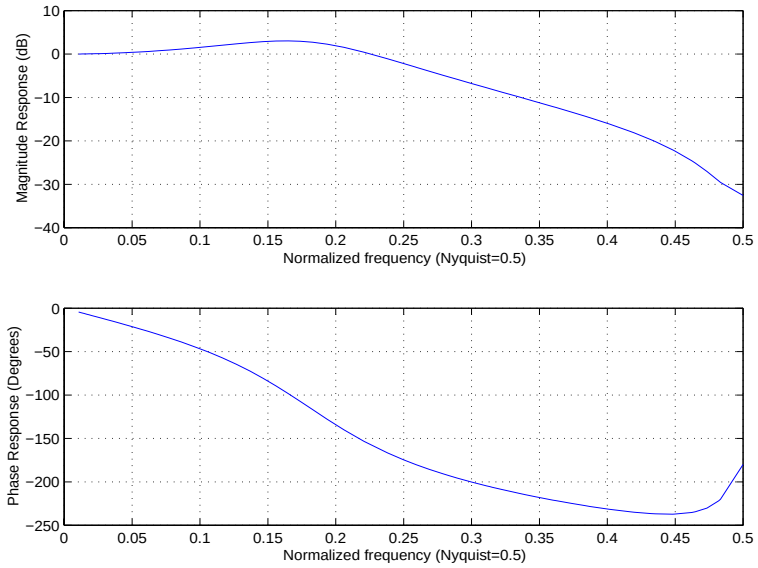

Figure 16: Bode diagram for $G_2(e^{i2\pi f/f_s})$

3.4 Selection of Power Reference Value

When choosing the power reference P_{ref} one has to take both underflow and overflow into account. Choosing P_{ref} is a trade off between both these cases. Now lets derive an optimum P_{ref} for different number of bits.

Let $x(t)$ denote the AD converter input and $\hat{x}(t)$ the AD converter output. In this section $x(t)$ is assumed to be normal distributed with variance σ^2 and mean 0. The AD converted signal is represented as an odd integer in the range $\pm(2^n - 1)$, where n is the number of bits. Choosing $Pref$ could be viewed as optimizing the signal to quantization noise ratio

$$SNR = \frac{\sum_t (x(t) - \hat{x}(t))^2}{\sum_t x^2(t)} \tag{63}$$

with respect to the ratio between σ and dynamic range of the AD converter. To simplify the optimization the AD converter decision levels are chosen so that it operates as a quantifier and limiter. This implies that the problem is reduced to minimizing the SNR with respect to σ and choosing $P_{ref} \approx \sigma^2_{opt}$.

The results for different number of bits in the AD converter together with AD converter dynamic range, AD_{range}, are given in table 1.

Number of Bits	σ_{opt}	AD_{range}	AD_{range}/σ_{opt}	P_{ref}
3	3.60	± 7	1.94	13
4	6.10	± 15	2.46	37
5	10.6	± 31	2.92	112
6	19.5	± 63	3.23	380

Table 1: Optimal power references

4 Simulation environment

To be able to investigate the AGC impact on the total performance, a simple WCDMA system had to be simulated. This is the main contribution of this thesis. The choice of simulation environment fell on Matlab much due to its simple user interface and powerful matrix algebra routines. In this section it will be described how each of the parts described in section 2 were implemented.

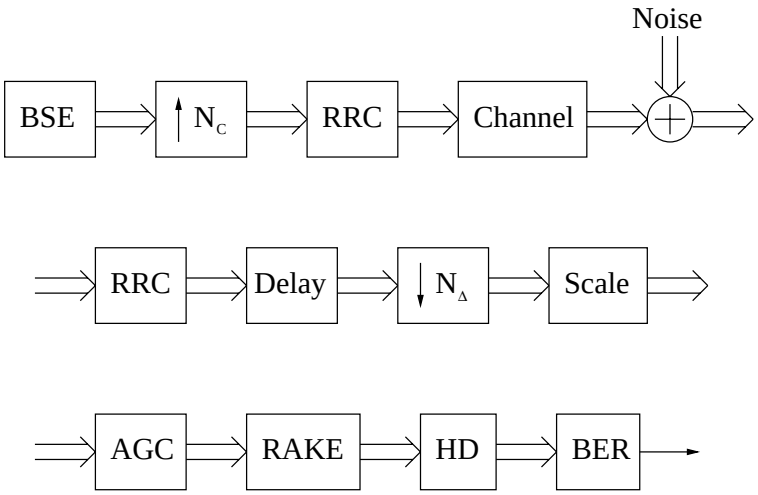

Figure 17: The different block of the simulation environment. First the Base Station Emulator (BSE) generates a complex sequence which is up sampled and fed to a Root Raised Cosine filter (RRC). The signal then passes through a multi path fading channel and is then disrupted by white Gaussian noise. In the receiver the signal is once again filtered and then delayed and down sampled. Then the signal is scaled and then fed to the AGC. The RAKE receiver then tries to isolate the different components and despreads the user symbols. A hard detection is then made on which symbol that was transmitted and the Bit Error Rate (BER) is then calculated.

4.1 Base Station Emulator

The first block in the simulation chain is the Base Station Emulator (BSE). To get realistic results it is preferable that the signal fed to the channel is a good approximation of the real signal from a base station. To achieve this the BSE was equipped with 5 user-data channels , one channel only transmitting zeros corresponding to the pilot channel (CPICH) and one channel to emulate all remaining channels. Implementing every channel exactly as in a real base station would be way to complicated and would not make the simulations more exact. For simplicity the BSE power is normalized to 1. The channelization codes are denoted $C^o(l, nr)$ where l denotes the level in the Walsh code tree and nr the code number see Appendix A.

4.1.1 Common Pilot Channel

The Common Pilot Channel (CPICH) is implemented as a binary sequence of only zeros sent using QPSK with spreading factor $S_f = 256$. This corresponds to just sending the complex sequence $e^{\frac{\pi}{4} \cdot i}$. In the simulations the CPICH uses 10 percent of the total transmitted power of the BSE which implies that $E_c^{CPICH} = 0.1$. This correspond to $\alpha_{CPICH} = \sqrt{0.1}$. This corresponds to the power used for the pilot channel in a fully loaded cell according to the specification [4]. The orthogonal channalization code used for CPICH is $C^o(9, 0)$.

4.1.2 Dedicated Down Link Physical Data Channel

The five user-data channels are implemented as five independent random binary sequences sent using 16QAM or QPSK and with variable spreading factors ranging from 4 to 512. The powers and the spreading factors of the different channels can be specified as an input to the BSE.

4.1.3 Orthogonal Channel Noise Simulator

The Orthogonal Channel Noise Simulator or OCNS is used to emulate all remaining channels transmitted from the BS in WCDMA. It is implemented as a random binary sequence sent using QPSK with spreading factor $S_f = 256$. The OCNS uses the remaining power of the BS. The orthogonal channalization code used for OCNS is $C^o(9, 1)$.

4.1.4 Spreading

The next step is to add all channels and multiply the resulting sequence with a complex spreading code. In a real WCDMA system this code is generated using two shift registers with feedback. In the simulations however the spreading sequence is generated as a random binary sequence modulated using QPSK. Implementing the shift register generation is unnecessarily complicated and would not help improve the simulations, because the main objective is to generate a random process which is easily done using Matlab's random number generator instead.

4.2 Filtering and I/Q Modulation

The output from the BSE consists of a complex sequence of length 2560 times the number of slots generated. In reality the complex sequence is now fed through an analog pulse shaping filter. To simulate this the complex sequence is oversampled a factor N_c. This is done by inserting $N_c - 1$ zeros between each sample. The choice of over sampling factor N_c is based on a requirement to be able to simulate a sample mismatch of $1/N_c$ chip in the receiver. The pulse shaping filter, as mentioned in section 2.1.4, is chosen so that $h(t) * h(t)$ has its zero-crossings at multiples of the chip period. A filter fulfilling this property is the Root Raised Cosine filter which is specified in [4]. The RRC has the

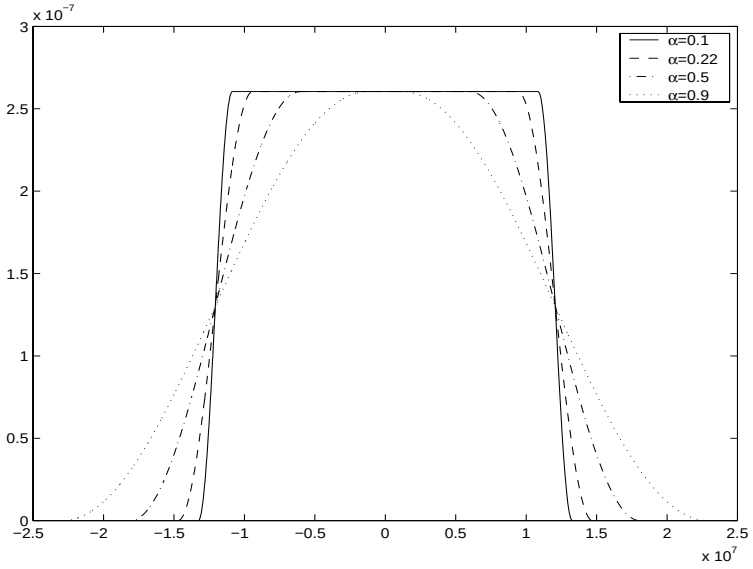

Figure 18: Total frequency response from data filters used in WCDMA. In WCDMA $\alpha = 0.22$ i used.

following spectral properties

$$H(\omega) = \begin{cases} \sqrt{T_c}; & 0 \leq |\omega| \leq \frac{1-\alpha}{T_c}\pi \\ \sqrt{\frac{T_c}{2}\left\{1 - \sin\left[\frac{T_c}{2\alpha}\left(|\omega| - \frac{\pi}{T_c}\right)\right]\right\}}; & \frac{1-\alpha}{T_c}\pi \leq |\omega| \leq \frac{1+\alpha}{T_c}\pi \\ 0; & |\omega| \geq \frac{1+\alpha}{T}\pi \end{cases} \tag{64}$$

Taking the inverse Fourier transform of (64) gives the impulse response (see [4])

$$h(t) = \frac{\sin\left(\pi\frac{t}{T_c}(1-\alpha)\right) + 4\alpha\frac{t}{T_c}\cos\left(\pi\frac{t}{T_c}(1+\alpha)\right)}{\pi\frac{t}{T_c}\left(1 - \left(4\alpha\frac{t}{T_c}\right)^2\right)} \tag{65}$$

where T_c is the pulse width. Choosing α is a tradeoff between narrow spectrum and low ringing amplitude. Theoretically, even a very low α provides no ringing at the sample points, but due to timing jitter a low α in practise leads to inter chip interference (ICI). So a high α provides a narrow spectrum and a low α provides less ICI. WCDMA uses $\alpha = .22$. Figure 18 shows the total frequency response $|H(\omega)|^2$.

When implementing the RRC filter the impulse response must be finite. This is achieved be simply truncating $h(t)$ so that the remaining part represents more than 99% of the total energy. It can be shown that choosing $t = -5T_c...5T_c$ fulfills this property. The continuous impulse response $h(t)$ is then sampled with a frequency of $\frac{N_c}{T_c}$. Let the sampled impulse response be denoted

$$h(\tau) = h(t) \quad , t = \tau\frac{T_c}{N_c} \quad , \tau = -5N_c, ..., 5N_c \tag{66}$$

and the sampled complex sequence

$$s(l) = s(t) \quad , t = l\frac{T_c}{N_c} \quad l = ..., -1, 0, 1, ... \tag{67}$$

To maintain the BSE power normalization after up sampling and filtering the transmitted signal $s(l)$ has to be scaled. To do this an expression for the power of the received, filtered and down sampled sequence $R_{i,j,k}$ has to be derived. To simplify calculations the channel will be ignored in this section. This is not a problem if the different paths are treated as independent and the noise is uncorrelated with the transmitted sequence. Under these assumptions the received and filtered signal $r_f(l)$ is equal to

$$r_f = s * h * h + e * h \tag{68}$$

where $e(l)$ is complex white noise with variance σ_e^2. To retrieve the complex sequence $R_{i,j,k}$ the received signal $r_f(l)$ is down sampled a factor N_c. Because the noise is assumed to be independent to the transmitted signal it is possible to separate the two contributions to the total power. Lets consider the contribution from the transmitted signal. If the noise is ignored the received down sampled signal can then be written as

$$R(n) = r_f(nN_c) = \sum_{\tau_1=-2\cdot 5N_c}^{2\cdot 5N_c} h_{RC}(\tau) \cdot s(nN_c - \tau) \tag{69}$$

where $h_{RC} = h * h$, which is of length $4 \cdot 5N_c - 1$. To simplify notation the sequence $R_{i,j,k}$ is denoted $R(n)$ where $n = i + S_f(j + kN_s)$. Now lets derive an expression for the mean power of $R(n)$. The mean power can be written as

$$E[R(n)R^*(n)] = \sum_{\tau_1} \sum_{\tau_2} h_2(\tau_1) \cdot h_2(\tau_1) E[s(nN_c - \tau_1)s^*(nN_c - \tau_2)] \tag{70}$$

Using the properties of $s(t)$ (see (5)) it is possible to show that

$$E[R(n)R^*(n)] = \sigma_s^2 \sum_{m=-10}^{10} h_{RC}^2(mN_c) \tag{71}$$

where

$$\sigma_s^2 = E[S_{i,j,k}S_{i,j,k}^*] \tag{72}$$

To maintain power normalization the transmitted signal $s(t)$ thus has to be scaled with

$$\left(\sum_{m=-10}^{10} h_{RC}^2(mN_c) \right)^{-1/2}$$

Throughout the simulations only the low pass equivalent (see section 2.1.4) is used. Implementing the radio frequency signals in Matlab would be much too memory and processing demanding. The possible decay in performance due to this approximation is assumed negligible.

4.3 Simulating Multi Path Fading Channels

The channel implementation is split into three parts. First the complex fading multi path components $H_p(0;t)$ are generated then the signal is delayed and multiplied and finally complex white Gaussian noise is added (see (14)).

$H_p(0;t)$ is generated as an average of a variable number of phasors of equal amplitude and initially equally distributed random phase rotating at random frequencies according to

$$H_p(0,t) = \frac{1}{N}\sum_{n=0}^{N-1} c_{n,p} e^{i2\pi t f_{D,n,p}} \tag{73}$$

The Doppler frequencies $f_{D,n}$ are generated using (13). To reduce the computational effort $H_p(0;t)$ is sampled at a lower speed (typically a factor 100) than e.g the $N_c T_c$ used in the filtering. This is possible because at moderate vehicle speeds, typically 3km/h, the channel varies much slower than the chip rate. To achieve a good channel approximation the sample rate is changed according to vehicle speed. The sample speed is then increased to match the rest of the channel. When simulating many slots typically more than 100, the memory requirements become vary large. This is solved by dividing the $H(0,t)$ into smaller parts, typically 10-100 slots. To accomplish this, the state i.e. the position of the N phasors is used as initial phase for the next part. A problem with this approach is that it is impossible to scale $H_p(0,t)$ so that

$$\frac{1}{T}\sum_{t=0}^{T-1} H_p(0,t)H_p(0,t)^* = 1 \tag{74}$$

without generating $H_p(0,t)$ twice. When $H_p(0,t)$ is very long this is not a problem because it is possible to show that $E[H_p(0,t)H_p^*(0,t)] = 1$. For shorter channels the average channel power has to be compensated for. Another approach is to first calculate the mean power of the channel and then use this as a scaling factor. The drawback with this method is that the channel has to be generated twice. This method is however used in the simulations.

The complex white Gaussian noise is generated as $e(t) = K(e_1(t) + e_2(t)\cdot i)$ where $e_1(t)$ and $e_2(t)$ are white normal distributed random process with variance equal to 1 and K a real valued constant. Now lets derive an expression for K. Using the same type of calculation as in section 4.2 it is possible to show that the power contribution from the noise is equal to

$$E[R(n)R^*(n)] = \sigma_e^2 \sum_{\tau=-5N_c}^{5N_c} h^2(\tau) \tag{75}$$

In section 2.3.5 the noise, $e_{i,j,k}$, effecting the received sequence $R_{i,j,k}$ is defined to have variance I_{oc}. Using (75) it is possible to show that if

$$K = \sqrt{\frac{I_{oc}}{2\sum_{\tau=-5N_c}^{5N_c} h^2(\tau)}} \tag{76}$$

the variance of $e_{i,j,k}$ will equal I_{oc}.

4.4 Sample Mismatch and Rate Conversion

When the analog signals are sampled in a real receiver a sampling jitter is present. To be able to simulate this jitter the channel and pulse shaping filters are sampled at a higher speed than the sampling frequency used in the actual receiver. To emulate the sampling jitter a delay of D samples is inserted before the LNA amplifier in the receiver chain. Depending on the sample rate of the channel,N_c, sampling jitters down to T_c/N_c seconds can be simulated.

To match the actual sampling rate of the receiver the signal has to be down sampled a factor $N_\delta = \frac{N_c}{N_r}$, where N_r is the over sampling factor in the receiver. Then the down sampled signal is fed to the LNA.

4.5 AGC

In a real WCDMA receiver the LNA is placed in the RF part of the receiver. Because all signals in this thesis are so call low pass equivalents, this proposes a problem when the system is to be simulated. This problem was solved by placing the LNA after I/Q demodulation. This approximation was also used in section 3.3 where the control design was made. To be able to simulate the AGC in a realistic way the incoming signal is scaled to a level comparable to the actual voltage level in a real receiver. This helps the modeling of e.g. DC components. Because the low pass filter in the power estimator has very poor damping of high frequencies one can't really talk in classical terms of bandwidth. Instead a parameter p will be used to describe the properties of the low pass filter. Lets assume a low-pass filter on the form

$$y(n) = 2^{-p}y(n-1) + (1-2^{-p})x(n-1) \tag{77}$$

Then the p parameter determines the memory of the low pass filter. Old samples have a relative weight of $(1-2^p)^n$. So for example if p is equal to 7 the relative weight will be less than 1 percent for $n > 600$.

4.5.1 VGA model

To be able to simulate the model derived in section 3.2.2, it has to be discretized. One possible way to do this is to use the so called Euler Forward approximation

$$\frac{d}{dt} \approx \frac{q-1}{h} \tag{78}$$

where q denotes the forward shift operator, i.e. $qx(t) = x(t+1)$, and h the sampling interval. Using this approximation (50) becomes

$$\begin{bmatrix} x(k+1) \\ u_c(k+1) \end{bmatrix} = (1+hA)\begin{bmatrix} x(k) \\ u_c(k) \end{bmatrix} + hB\begin{bmatrix} u_0(k) \\ d_0(k) \\ \vdots \\ d_N(k) \end{bmatrix} \tag{79}$$

$$y_{HP}(k) = C\begin{bmatrix} x(k) \\ u_c(k) \end{bmatrix} + D\begin{bmatrix} u_0(k) \\ d_0(k) \\ \vdots \\ d_N(k) \end{bmatrix} \tag{80}$$

4.5.2 Automatic Gain Control Algorithm

As mentioned in section 3.2.2 the entire AGC system is a non linear time varying system, which implies that the use of fast linear system models is out of the question. But as mentioned in Section 3.2.2 the VGA chain can be viewed as a linear time invariant system, if only observed between gain changes. This property is of course utilized in the simulations. First a state space model according to Section 3.2.2 is calculated for all possible combinations of gains. Then the VGA chain is simulated by block wise usage of Matlab's LTI tool box. The state at the end of each block is used as initial state to the following. The length of each block, N_b, depends on how often the AGC is run (AGCperSlot) and the over sampling factor (N_r) as

$$N_b = \frac{2560 \cdot N_r}{\text{AGCperSlot}} \tag{81}$$

Each block is then fed to to the power estimator and a control signal is calculated according to (58).

4.6 RAKE

The RAKE receiver is implemented as one Matlab function calling one other correlator function. In the simulations the path delays τ_p are predefined and thus known, so no path tracking is done. This is of course an idealized situation. The correlators are implemented as proposed in Section 2.3.5. The complex pseudo random spreading code $C^{PN}_{i,j,k}$ and the orthogonal channalization code $C^{o}_{i,j,k}$ are inputs to the correlator function. Channel estimation and compensation is done as mentioned in Section 2.3.6. There, it was mentioned that if α_{pilot} was known it could be compensated for. As a result of this, both a raw version with only phase compensation and a version for which α_{pilot} is compensated for are available as output from each finger. To be able to use the Maximal Ratio combining approach a variance estimate also has to be calculated. This is done as proposed in Section 2.3.6. The three combining methods mentioned in Section 2.3.6 are implemented as proposed and are chosen as a parameter to the RAKE function.

5 Simulations

To evaluate different parameter configurations a number of simulations were made. The main focus of this thesis is the AGC impact when changing from QPSK modulation to 16QAM modulation, but other parameters will also be investigated. Through out all simulations a number of parameters are used, they will be explained below. All simulation blocks have a large number of parameters, but all are not of interest in these simulations. These are all described in a separate internal Ericsson user manual. To start with, a number of power definitions will be explained. Some are mentioned in other sections as well, but they will all be put together here. Then all other parameters of interest in the simulations will be described.

I_{or} is the total transmitted power of the base station (default value 1).

I_{oc} is the total received noise power after filtering.

E_c is the transmitted power of a specific channel. The Base Station Emulator allows the specification of one E_c for each of the five DPCCHs (default value -2dB for the first channel and $-\infty$ dB for the rest).

S_f is the spreading factor used for the channel in interest (default value 16).

E_s is the power per symbol according to

$$E_s = S_f \cdot E_c$$

E_b is the power per bit. For QPSK the number of bits per symbol, N, equals two and for 16QAM four.

$$E_b = \frac{E_s}{N}$$

BER is the raw bit error rate, i.e. the number of bit errors divided by the total number of transmitted bits. Depending on the code rate, i.e. the ratio between the number of data bits and the actual number of transmitted bits. If a code rate of 1/3 is used, i.e. three bits are transmitted for each data bit, a BER of approximately 10% is acceptable. To be able to use code rates of 3/4 BER of approximately 5% or less must be achieved.

nbits is the number of bits used in the AD converter (default value 4).

N_r is the over sampling factor used in the AGC (default value 4)

AGCperSlot is the number of AGC sampling points per slot.

p is a parameter describing the memory of the power estimator low pass filter (see Section 4.5). The default value for p is 7.

One of the ideas with HSDPA (High Speed Down link Packet Access) is to direct a very big portion of the total base station energy I_{or} to one user for a short period of time. Therefor a very big E_c/I_{or} is used in most simulations, typical values used in simulations are -1dB to -3dB. This corresponds to directing 80% to 50% of the total base station power to one user. In an actual WCDMA system each HSDPA channel is mapped to five channels with less relative power. The

method used in the simulations is however equivalent to this. When comparing different implementations or modulation techniques a common measure is to investigate what the corresponding decay in signal to noise ratio would be. If for example a 1 path fading channel is to be compared with an AWGN channel, the BER versus SNR is plotted for both channels. Then the difference in SNR is measured for a given BER. The difference between the two graphs is then a measure of the loss in SNR ratio due to a 1 path fading channel. This will be referred to as SNR loss from here on.

The simulations marked as ideal slow AGC refers to a very slow ideal AGC that is not able to track the fast power changes due to fadings. The AGC used in the simulations models DC disturbances and have a DC blocker bandwidth of 20kHz.

The slow ideal AGC is implemented as a static gain scaled as follows. The signal is scaled to generate as less under- and overflow as possible. This is achieved if the signal is scaled so that the dynamic range of the AD converter, AD_{range}, divided by the standard deviation of the signal, σ, equals the ratio in table 1.

5.1 Theoretical QPSK Verification

When implementing such a large simulation system in a quite short period of time it is important to be able to verify the results. One way to do so is to compare simulated raw bit error rates with theoretical results. Now lets derive an expression for the BER as function of signal to noise ratio. Lets assume a WCDMA system as described in Section 2, but under the assumption of a one path AWGN channel. Let us also assume that all symbols are equally probable and contribute in the same way to the bit error. The last assumption is valid because the modulation scheme for QPSK is symmetric. Now lets derive an expression for the probability of bit error given that the symbol $\left[\frac{1+i}{\sqrt{2}}\right]$ corresponding to [00] was transmitted (see Figure 2). If $\hat{U}_{n,j,k}$ denotes the received symbol the probability for error equals

$$\begin{aligned} P_b &= \frac{1}{2}P(\Re\{\hat{U}_{n,j,k}\} < 0, \Im\{\hat{U}_{n,j,k}\} > 0) \\ &+ \frac{1}{2}P(\Re\{\hat{U}_{n,j,k}\} > 0, \Im\{\hat{U}_{n,j,k}\} < 0) \\ &+ P(\Re\{\hat{U}_{n,j,k}\} < 0, \Im\{\hat{U}_{n,j,k}\} < 0) \end{aligned} \tag{82}$$

Now lets assume that the real ($\Re$) and imaginary ($\Im$) parts of $\hat{U}_{n,j,k}$ are independent and equally distributed. Under this assumption (82) simplifies to

$$P_b = P(\Re\{\hat{U}_{n,j,k}\} < 0) = P(\Im\{\hat{U}_{n,j,k}\} < 0) \tag{83}$$

Now the distribution of $\Re\{\hat{U}_{n,j,k}\}$ must be determined. If the channel is assumed to be an AWGN channel Equation (24) in Section 2.3.5 simplifies to

$$\hat{U}_{n,j,k} = \hat{U}''_{n,j,k} = \alpha_n U_{n,j,k} + e'_{j,k} \tag{84}$$

where $e'_{j,k}$ is Gaussian noise with variance $\frac{I_{oc}}{S_f}$. If the real and imaginary parts of $e'_{j,k}$ are assumed to be independent $\Re\{\hat{U}_{n,j,k}\}$ is normally distributed with

mean $\frac{\alpha_n}{\sqrt{2}}$ and variance $\frac{I_{oc}}{2S_f}$. Then

$$P_b = 1 - \Phi\left(\sqrt{\frac{E_c S_f}{I_{oc}}}\right) \tag{85}$$

where

$$\Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} e^{-t^2/2} dt \tag{86}$$

is the cumulative probability function for a normal distributed variable with mean 0 and variance 1. In figure 19 the theoretical bit error rate together with a simulated BER is plotted. The channel energy ratio E_c/I_{or} was kept constant equal to -2dB. All other relevant parameters where kept at their defaults. As can be seen in Figure 19 the theoretical BER is almost identical to the simulated BER, which verifies the function of the simulation environment used in this simulation.

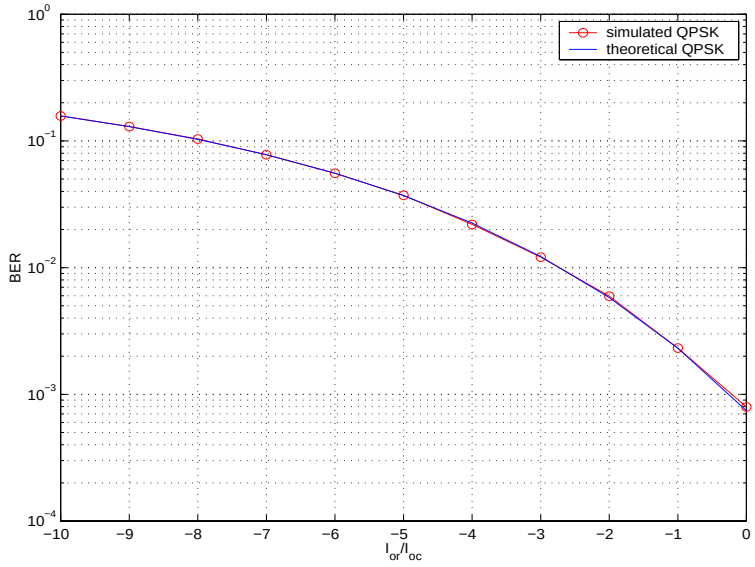

Figure 19: Theoretical and simulated BER versus I_{or}/I_{oc} for QPSK with AWGN channel and fixed E_c/I_{or}=-2dB. The theoretical BER is identical to the simulated BER, which verifies the function of the simulation environment used in this simulation.

5.2 Automatic Gain Control Investigations

To gain an understanding on how the AGC works a number of simulations with two different channels and two different control designs were made. Theses simulations are mainly to illustrate the different signals and the basic principles of AGC. The hardest channel cases for the AGC are the single path cases. Therefore one channel case with one path corresponding to a vehicle velocity of 30km/h and one corresponding to 120km/h was simulated for 30 slots using 16QAM modulation for the different cases. To only see the effects of AGC no noise was added, this corresponds to $I_{or}/I_{oc} = \infty$. All other parameters were kept at the defaults. In figures 20 to figure 23 the real part of the input to the AGC together with the real part of the AD converted output is shown. The power estimate, AGC gain output and bit errors are also given. To be able to compare the AGC with a receiver without an AGC the bit error is also plotted for a receiver only using an AD converter.

In 20 the terminal is traveling at a velocity of 30km/h. Here a big gain in performance can be seen with the use of an AGC. This is because when traveling at moderate speeds the channel estimator is able to make good estimations of the channel, so most bit errors are due to quantization effects, which are reduced by the AGC. The output from the AGC seems to be saturated all the time, but this is not the case. Because of the large amount of data points plotted the signal looks saturated. To save power it is desirable to be able to run the controller as seldom as possible. In Figure 21 the controller is only run 1 time per slot compared to 10 times in the other cases. This corresponds to making the control design 10 times slower. As can be seen the controller is too slow to be able to track the fast fadings of the channel, but this doesn't have a very big impact on bit error rate.

When a 120km/h channel model is used (see Figure 22) the channel estimator can't make an accurate estimate of the channel and thus most bit errors are due to the poor channel estimate. The performance gain due to AGC is thus not as big as for the 30km/h channel model. Another problem is that the AGC seems to be too slow to handle the fast fadings of the channel. In Figure 23 the same channel model is used but now with a faster control design. The designed used is the 40krad/s design from Section 5.7. There doesn't seem to be any large improvement when a faster control design is used. This is probably as mentioned before due to the poor channel estimate.

In general it can be seen that most bit error occur when the channel is fading. This is because the signal to noise ratio drops when the terminal enters a fade, and thus more bit errors are generated. The quantization effects also become more significant if the AGC is unable to track the fadings.

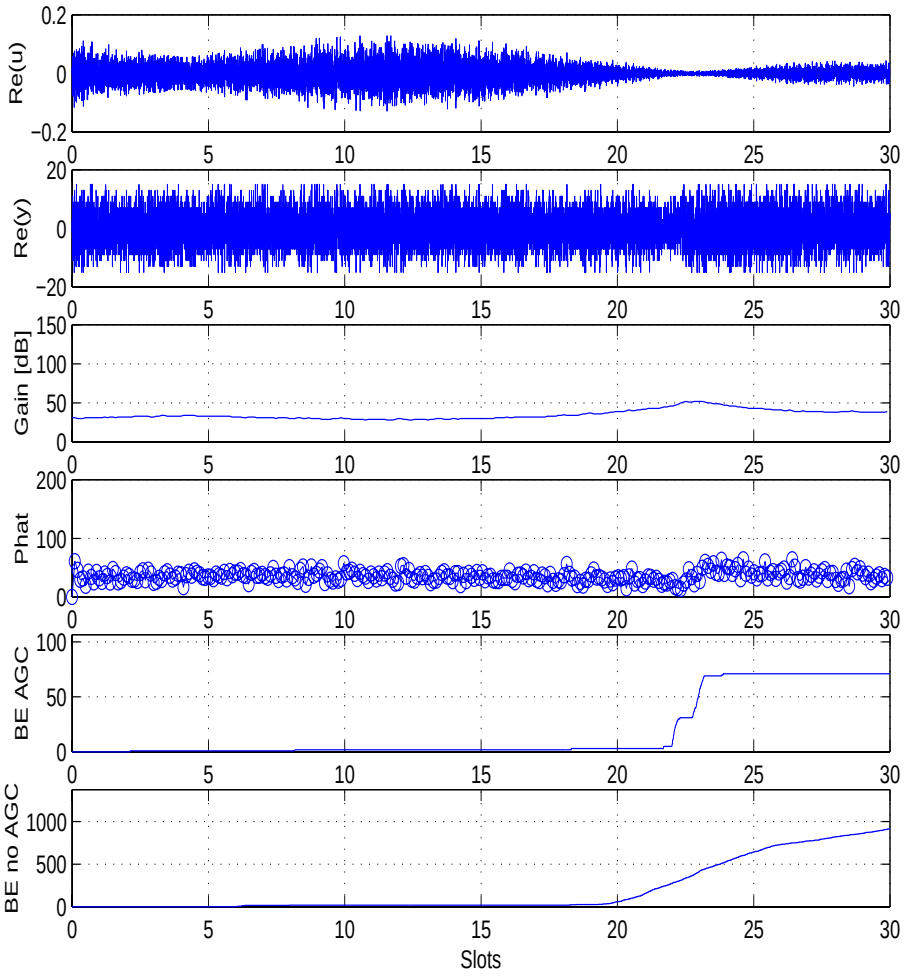

Figure 20: Real parts of input and output together with power estimate, gain output and bit errors for $I_{or}/I_{oc} = \infty$. 1 path channel model corresponding to a vehicle velocity of 30km/h. Slow control design with ω=18.3k rad/s. The AGC is able to track the fadings and thus greatly reduces the number of bit errors compared to just using a AD converter and a static gain.

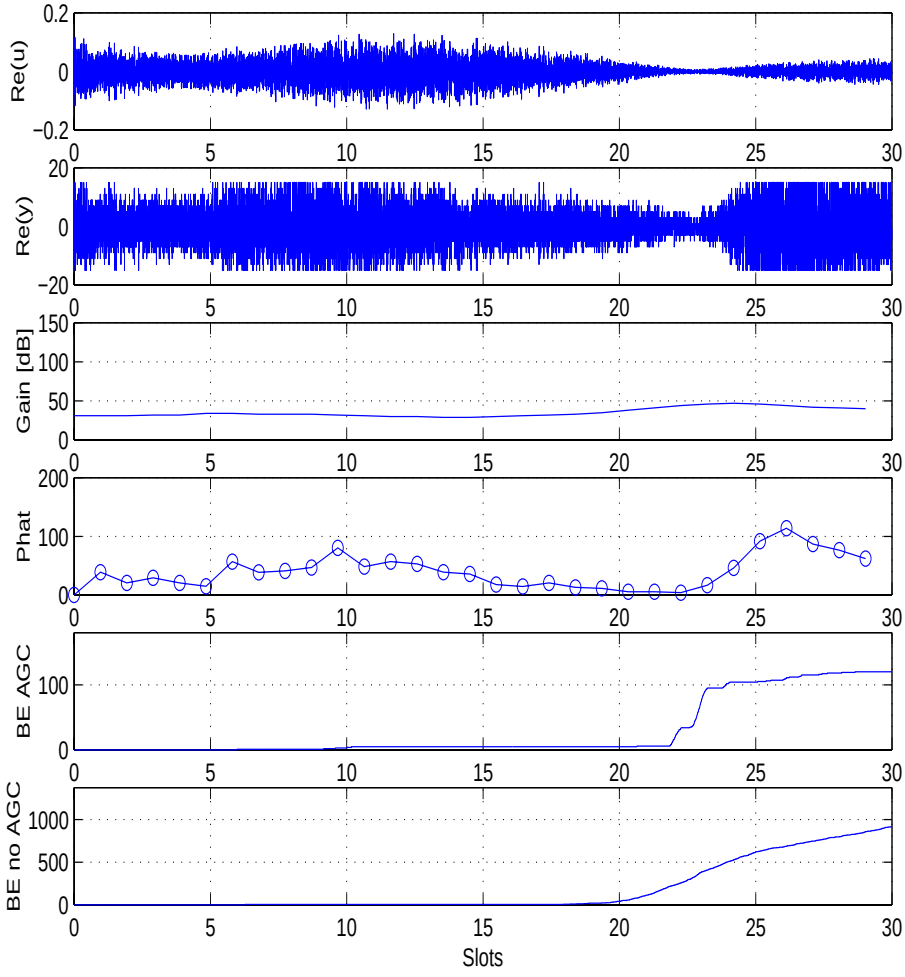

Figure 21: Same prerequisites as in Figure 20 but with an AGC working once per slot instead of 10 times a slot. The AGC is unable to track the fadings, but this does not seem to degrade performance greatly compared to having the AGC run 10 times per slot.

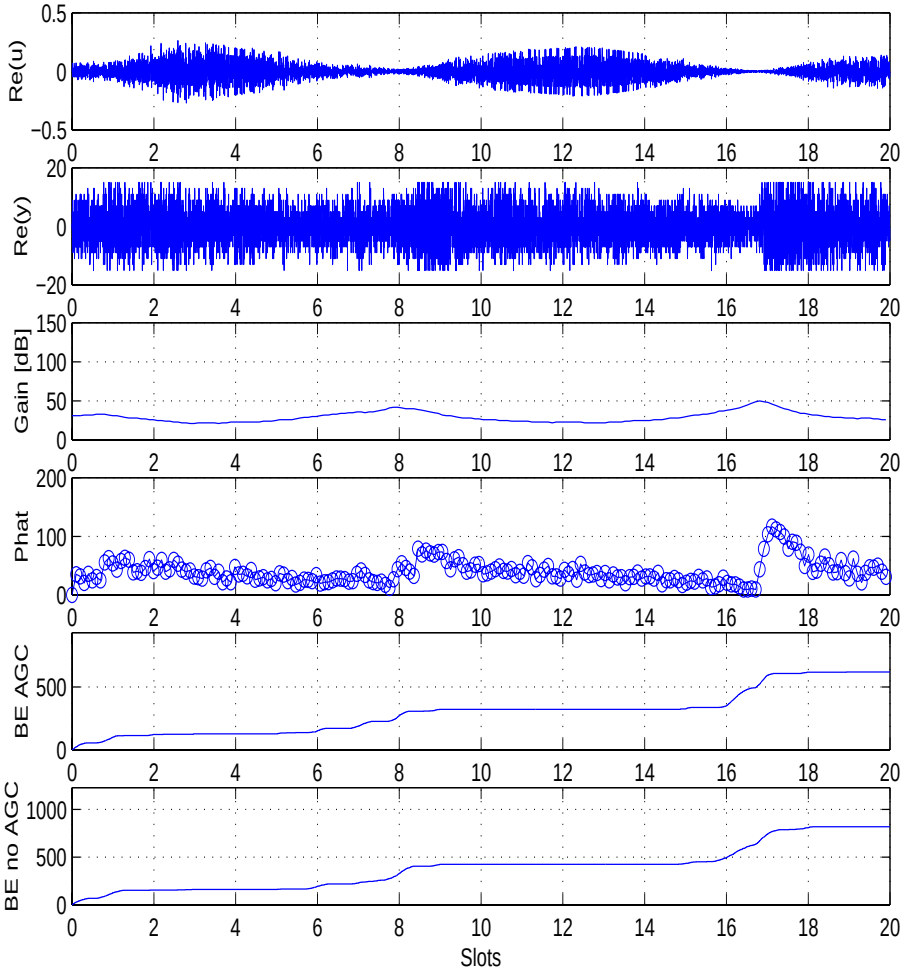

Figure 22: Same prerequisites as in Figure 20 but with a channel corresponding to 120km/h. The AGC design is too slow to be able to follow the fast fading of the channel. The increased bit errors are probably due to the fact that the channel estimator is two slow to make a good channel estimate at velocities that high.

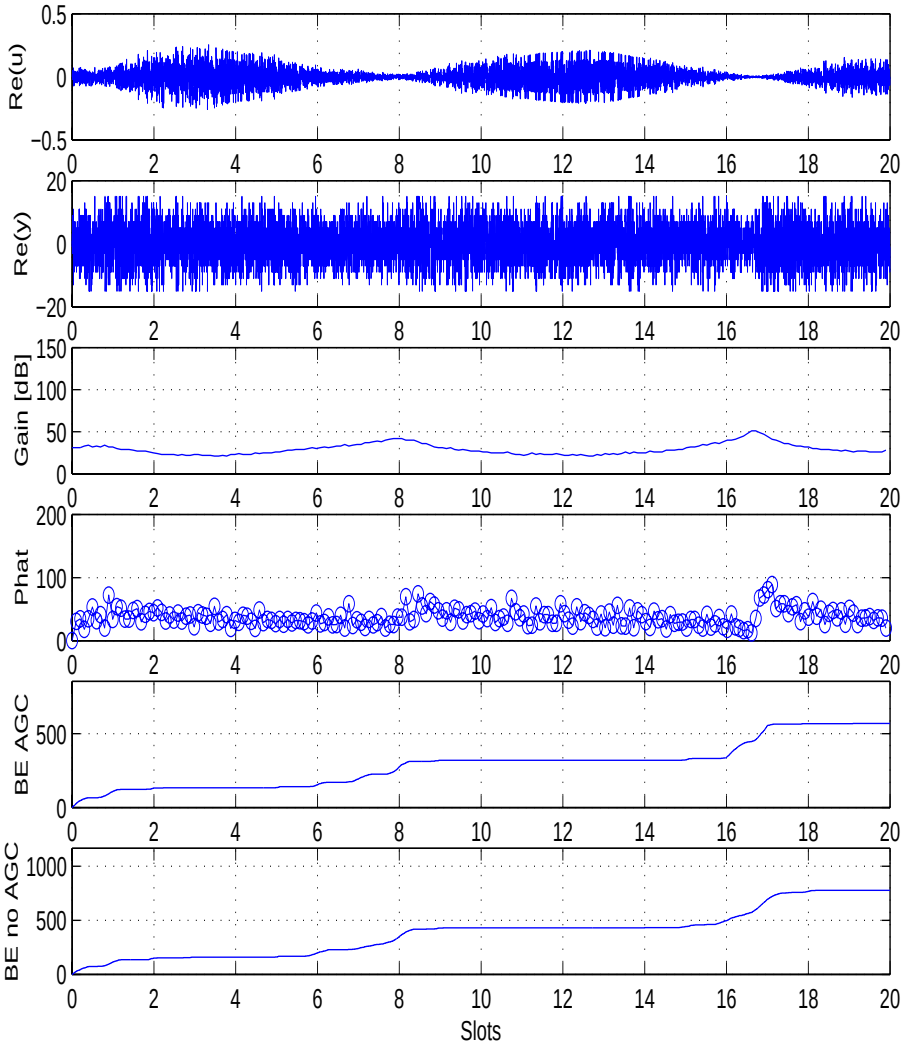

Figure 23: Same prerequisites as in Figure 22, but with a faster control design with ω=40k rad/s. This does not seem to improve performance very much, because of the poor channel estimate.

5.3 AGC Step Response Evaluation

To gain a further understanding of the AGC problem a number of step response simulations were made. The step response was created by multiplying the incoming signal with a constant corresponding to the desired step amplitude. In the simulations a positive and negative step of 40dB was used. The AGC algorithm is implemented so that when the LNA changes value the VGA chain must change the gain in the opposite direction to maintain the same gain level.

To be able to see the effects of the DC disturbances the DC levels were varied from 0mV to 1000mV. A realistic level in the receiver would be between 0mV and 10mV. The DC blocker bandwidths were chosen to 5kHz to make the DC effects more visible. The input consisted of a complex normal distributed random process with mean 0 and variance according to the desired input level.

In figures 24 and 25 different control designs are simulated. One observation that can be made is that the positive step response is faster than the negative. If we assume a 4 bit AD converter, the discrete power levels range between 1 and 225. The reference value used in this simulation is 35. The controller works in the logarithmic domain which implies that the maximum differences between desired power and the current power is -15dB and 8dB respectively. For a positive 40dB step, the power level saturates at 1, which leads to a difference of -15dB. For a negative step of 40dB the power level saturates at 225 which gives a difference of 8dB and thus leads to less control action than the positive step.

Figure 26 shows the positive step response with an AGC design with bandwidth, ω=18.3krad/s, and damping $\zeta = 0.36$ for 1mV and 50mV DC disturbances. In the power estimate figure the DC transients can be seen. The DC transient is larger after the LNA switch because the VGA chain changes gain very fast and thus the DC level changes fast as well.

If the DC levels are very high the system can become instable, this is illustrated in Figure 27. DC levels that high are however not realistic in a real receiver.

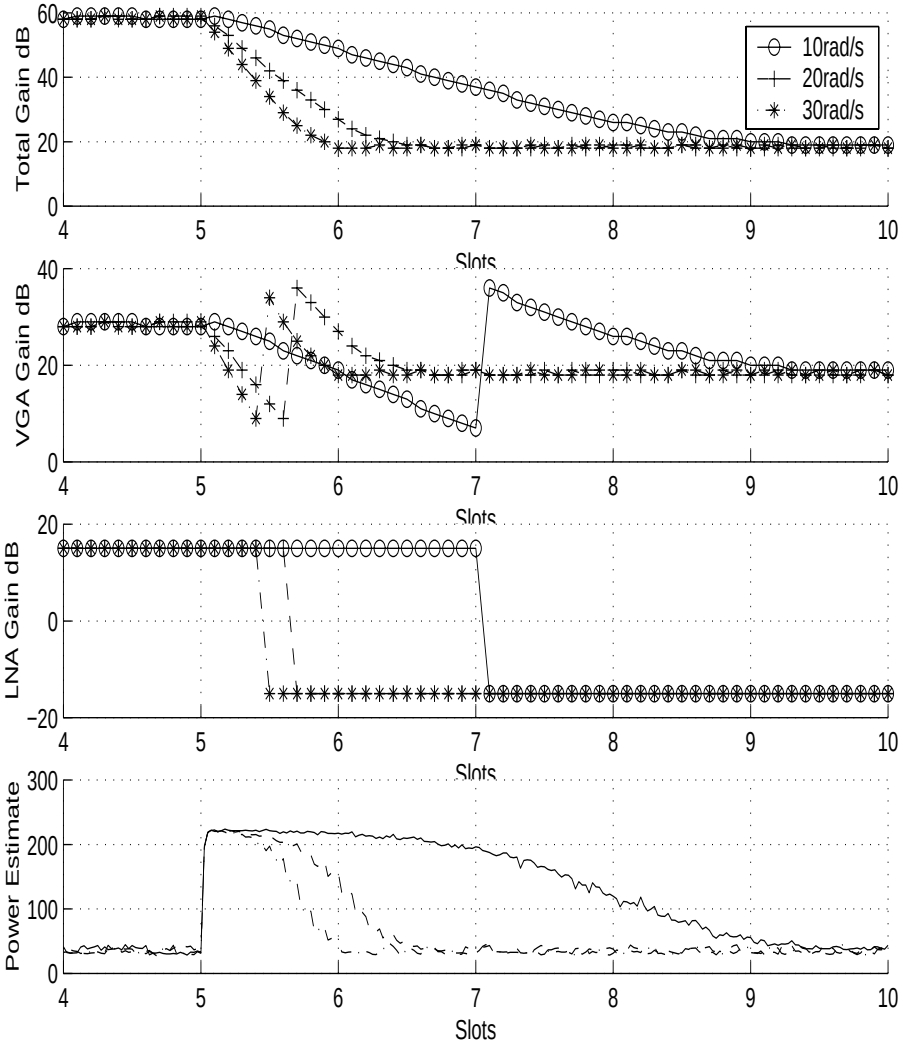

Figure 24: Negative step of 40dB at t=5 slots for three different AGC designs. All controllers have relative damping $\zeta = 0.36$. The AGC algorithm is implemented so that when the LNA changes value the VGA chain must change the gain in the opposite direction to maintain the same gain level.

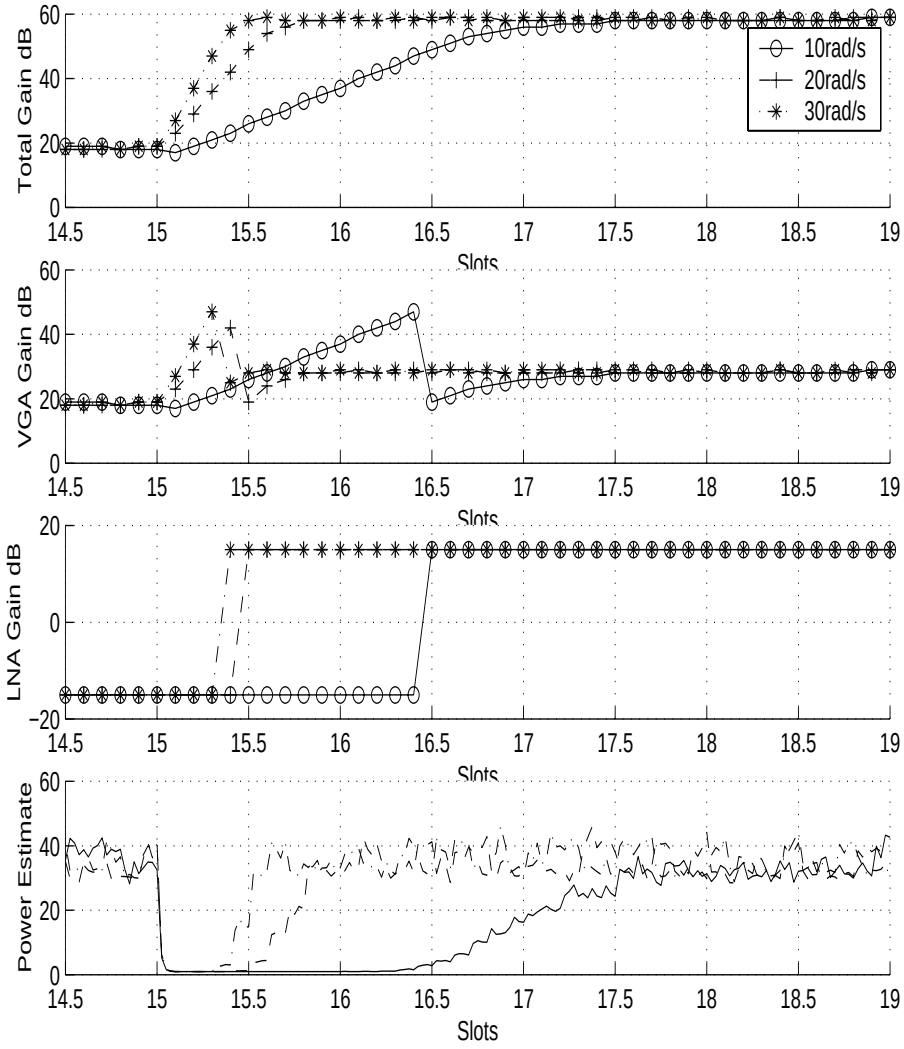

Figure 25: Positive step of 40dB at t=15. The positive step is faster than the negative one in Figure 24. If we assume a 4 bit AD converter, the discrete power levels range between 1 and 225. The reference value used in this simulation is 35. The controller works in the logarithmic domain which implies that the maximum differences between desired power and the current power is -15dB and 8dB respectively. For a positive 40dB step, the power level saturates at 1, which leads to a difference of -15dB. For a negative step of 40dB the power level saturates at 225 which gives a difference of 8dB and thus leads to less control action than the positive step.

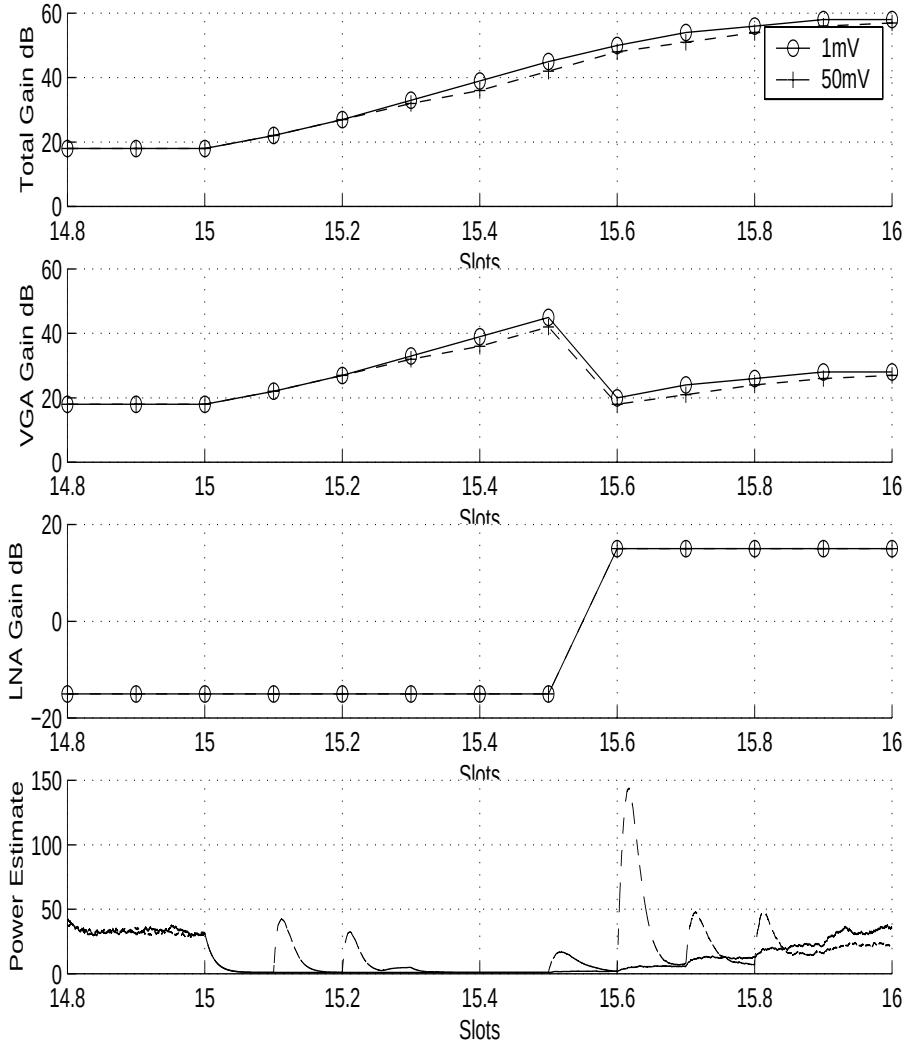

Figure 26: Positive step response with an AGC design with bandwidth, ω=18.3krad/s, and damping $\zeta = 0.36$ for 1mV and 50mV DC disturbances. In the power estimate figure the DC transients can be seen. The DC transient is larger after the LNA switch because the VGA chain changes gain very fast and thus the DC level changes fast as well. As long as the transients have disappeared before the next AGC sample point, the DC disturbances does not effect the performance very much.

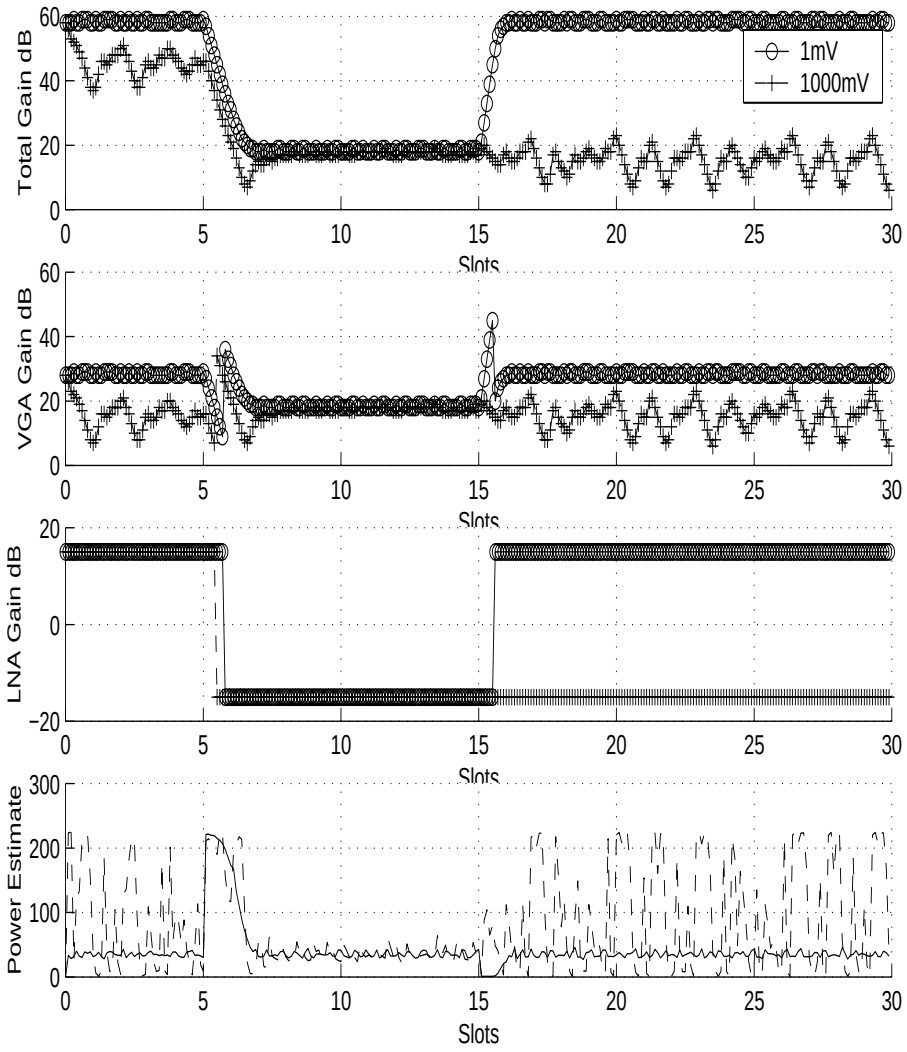

Figure 27: Same AGC design as in figure 26. If the DC levels are very high the system can become instable. DC levels that high are however not realistic in a real receiver.

5.4 Automatic Gain Control Evaluation

To gain an understanding of the different parameters in the AGC a number of simulations with different channels and parameters will be made. In the early version of the High Speed Data Packet Access or HSDPA specification three different delay profiles are proposed [5]. The delay profiles can be found in tables 2, 3 and 4.

Relative Delay (ns)	0	110	190	410
Relative Power (dB)	0	-9.7	-19.2	-27.8

Table 2: Delay Profile Pedestrian-A (PA)

Relative Delay (ns)	0	200	800	1200	2300	3700
Relative Power (dB)	0	-0.9	-4.9	-8.0	-7.8	-23.9

Table 3: Delay Profile Pedestrian-B (PB)

Relative Delay (ns)	0	310	710	1090	1730	2510
Relative Power (dB)	0	-1.0	-9.0	-10.0	-15.0	-20.0

Table 4: Delay Profile Vehicular-A (VA)

The three different delay profiles are specified with velocities between 3km/h and 120km/h according to Table 5. An extra delay profile with only one path and delay 0ns was also simulated. This channel is referred to as vehicular-B or VB. The two channels corresponding to a velocity of 120km/h are to be seen as tests of robustness. The HSDPA system is not intended to operate at vehicle velocities higher then 30km/h, and therefore high bit error rates are expected.

BER versus I_{or}/I_{oc} was simulated for the five different channel models. The ration E_c/I_{or} was kept constant equal to -2dB, which corresponds to 63% of the total base station energy. This is a realistic choice in HSDPA contexts. The results with no AGC are made with just an AD converter instead of the AGC. The AGC was run at 10 times per slot and all other parameters were kept at their defaults.

All simulations marked ideal slow AGC are as mentioned before performed with a very slow ideal AGC implemented as a static gain chosen to minimize the quantization errors.

In Figure 28 the Pedestrian-A channel corresponding to a velocity of 3km/h was simulated. The AGC improves performance more at low noise powers because the quantization effects are relatively small compared to the noise effects. The Select Biggest Combining (SBC) gains some from the AGC, whereas the Equal Gain Combining (EGC) does not gain anything compared to not using the AGC. This is because in channel PA-3 the second strongest path is -9.7dB weaker than the strongest one, which means that the SBC probably chooses the first path most of the time and thus is very sensitive to fadings. The EGC on the other hand uses more then one path and thus it not as sensitive to fadings.

Channel	Velocity	Delay Profile	Note
PA-3	3km/h	PA	
PB-3	3km/h	PB	
VA-30	30km/h	VA	
VA-120	120km/h	VA	
VB-120	120km/h	-	One path with delay 0ns

Table 5: Different channels used in simulations.

Another interesting result of the simulation is that the SBC method is better than the Equal Gain Combining (EGC) method. This is also due to the fact that the second strongest path has a very low energy compared to the strongest one. The strongest path disrupts the information in the other paths, and thus it is better to ignore that information. The loss of power when ignoring the weaker paths is only 0.5dB compared to if all path powers would have been collected.

At high noise powers however the performance is worse with an AGC even for the SBC method. This is probably due to the fact that the inaccuracy induced by the fading channel is small compared to that from the noise. The imperfections in the AGC then degrades the performance more then the AGC improves inaccuracy due to fadings. What parameters in the AGC that dominates the decay in performance will be investigated in later sections.

Then the PB channel corresponding to a velocity of 3km/h was simulated. The PB-3 channel has two paths with almost equal power (0dB and -0.9dB) and one third with a bit less power (-4.9dB). One would expect this channel to be less sensitive to fadings and thus the AGC shouldn't improve the performance much. Because the three major paths are almost equal in power one would expect that they should disrupt each other which should lead to a performance decay compared to the PA-3 channel where there is one dominating path. Figure 29 confirms these predictions. The SBC methods is, as expected, better then the EGC method. The reason for this is that the power in the second and third most powerful paths are significant compared to the first one. Ignoring the information in all other paths will lead to a loss of performance. The AGC doesn't improve performance for any combining method, not even for very low noise powers. This is because the quantization effects are much smaller then e.g. the inter chip interference caused by multi path propagation.

The delay profile Vehicular-A is similar to the delay profile Pedestrian-B, so one should expect similar results. Because of a higher vehicle velocity in the channels VA-30 and VA-120 the AGC is expected to improve performance more than for the PB-3 channel. In Figure 30 and Figure 31 the results from the simulations can be found. As expected the performance improvement due to the AGC increases with higher velocities.

As can be seen in figure 32 the performance improvements due to AGC become more significant for lower signal to noise ratios. The VB-120 channel is a one path channel which makes it more sensitive to fadings. If there is a deep fade there are no other paths carrying information and thus the quantization effects become more significant. When there is only one path present the two combing methods EGC and SBC merge in to one method.

From these simulations one could draw the conclusion that the AGC doesn't

really improve the performance of the receiver very much. This is however not true. To be able to track very slow variations in received power, slow fading, that occurs i.e. when a receiver moves behind a house or another big obstacle, the receiver has to be equipped with an AGC. Another task for the AGC is to improve performance when entering compressed mode, that is when the terminal i.e. wants to perform measurement on neighbouring base stations or other carrier frequencies.

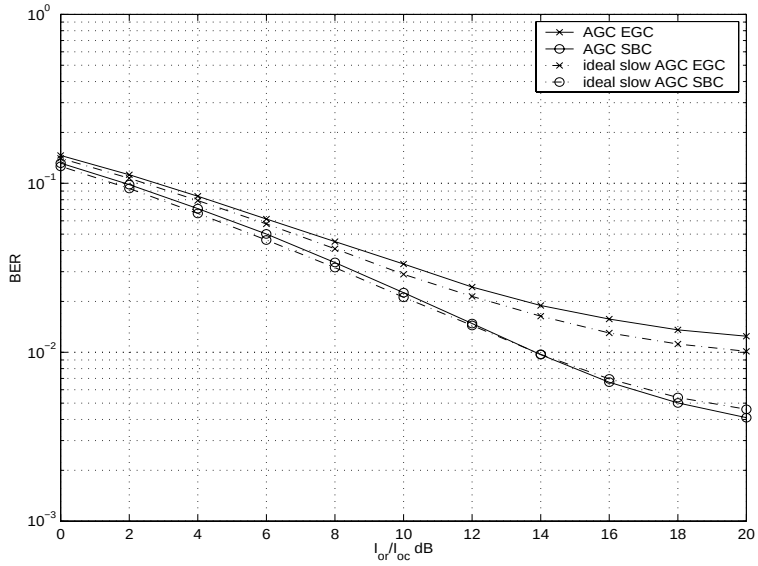

Figure 28: BER with and without AGC and different combining methods versus I_{or}/I_{oc} for 16QAM with channel PA-3 and fixed E_c/I_{or}=-2dB. The two combining methods are Equal Gain Combining (EGC) and Select Biggest Combining (SBC). The AGC improves performance for SBC at low noise levels. Select Biggest Combing is better than Equal Gain Combining because of the similarities to a single path delay profile. The slow ideal AGC simulations are performed with a very slow ideal (no DC filters) AGC that is unable to track the fadings.

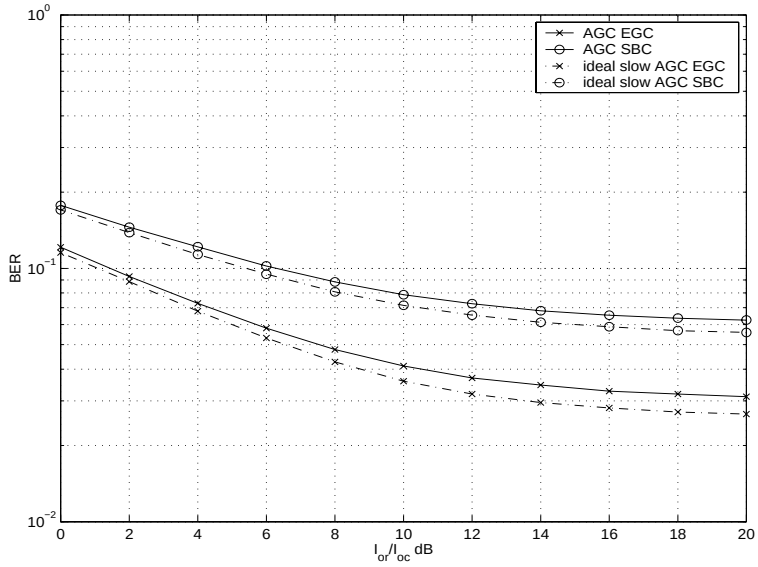

Figure 29: Same prerequisites as in Figure 28 except for the use of channel model PB3. Channel model PB3 has a delay profile with two dominating paths. That makes the receiver less sensitive to fadings and thus no improvement is gained with AGC. The slow ideal AGC simulations are performed with a very slow ideal (no DC filters) AGC that is unable to track the fadings.

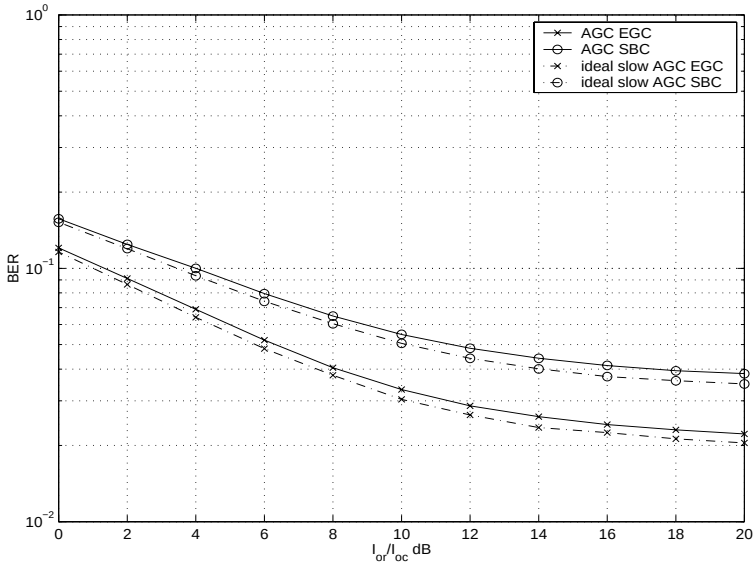

Figure 30: Same prerequisites as in Figure 28 except for the use of channel model VA30. The delay profile used in VA30 is similar to the one used in PB3 and thus the same results are expected. Because the two dominating paths are further separated, the VA30 channel model gives a bit better result despite the higher velocity. The disruption caused by inter chip interference still dominates over the disruption caused by fading and thus nothing is gained with AGC. The ideal slow AGC simulations are performed with a very slow ideal (no DC filters) AGC that is unable to track the fadings.

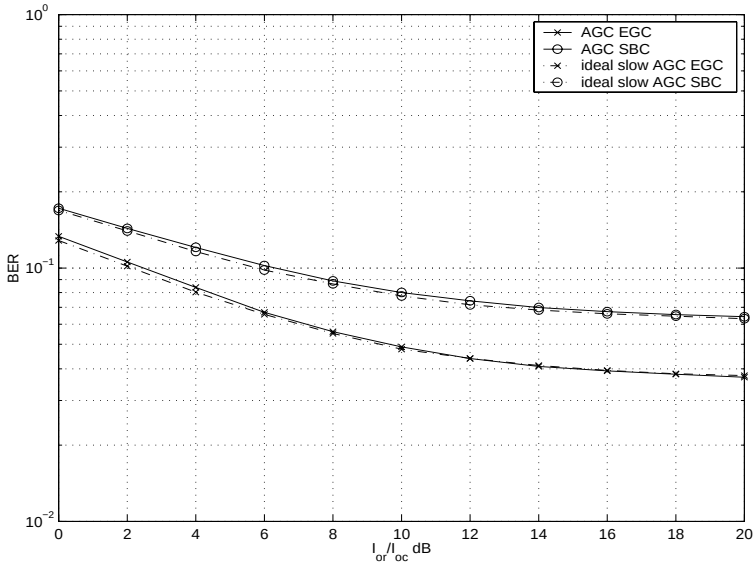

Figure 31: Same prerequisites as in Figure 30 except for the use of channel model VA120. Because of the higher velocity the effect of fading become more significant and thus the receiver gains more from AGC than in Figure 30.The slow ideal AGC simulations are performed with a very slow ideal (no DC filters) AGC that is unable to track the fadings.

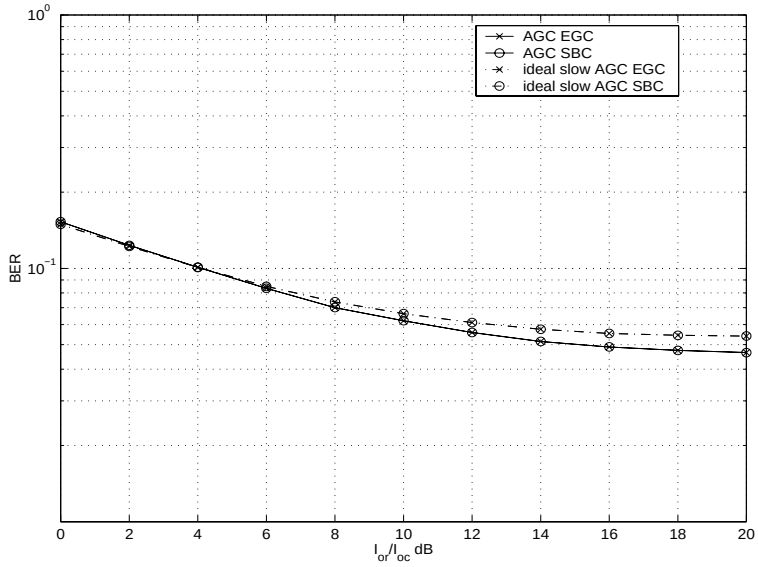

Figure 32: Same prerequisites as in Figure 31 except for the use of channel model VB120. Because VB120 has a single path delay profile the receiver is much more sensitive to fadings and thus the AGC improves performance compared to not using AGC. The ideal slow AGC simulations are performed with a very slow ideal (no DC filters) AGC that is unable to track the fadings.

5.5 Impact of DC Blocker Bandwidth

As could be seen from the simulations in Section 5.4 the use of AGC does not always improve performance. The reason for this is that the AGC disrupts the signal which causes inter chip interference. In this section the impact of DC blocker bandwidths will be investigated.

To be able to isolate the impact from DC blocker bandwidth the DC disturbances were set to zero. The raw bit error rate BER was simulated versus I_{or}/I_{oc} for different bandwidths. The channel was chosen as PA-3, because the difference between AGC and no AGC was most conspicuous for this channel. The Select Biggest Combing method was chosen, because it gave the best results in previous simulations with the PA-3 channel. All other parameters were set to their default values.

The result from the simulation together with the BER for the simulation without AGC can be found in Figure 33. As a comparison it could be mentioned that the simulations in Section 5.4 were all made with bandwidth equal to 20kHz.

In figure 33 one can see that the AGC with DC blocker bandwidth equal to 0kHz is almost as good as no AGC at all at BER equal to 10%. From this the conclusion is drawn that the DC blockers play a very important role. It seems that the performance loss due to AGC is almost totally due to the DC blockers. This implies that if the DC disturbance levels can be improved so that the bandwidth of the DC blockers can be lowered a significant gain in SNR can be accomplished. There are no big differences at BER equal to 5% compared to BER equal to 10%. At high SNRs the drawback with a very slow ideal AGC become visible.

It is difficult to optimize the DC blockers bandwidths using simulations. The reason for this is that it is essential to model the DC disturbances very accurate, which is very hard. Such an optimization must be done using measurements. Therefor it is pointless to draw any conclusions on absolute optimal bandwidths.

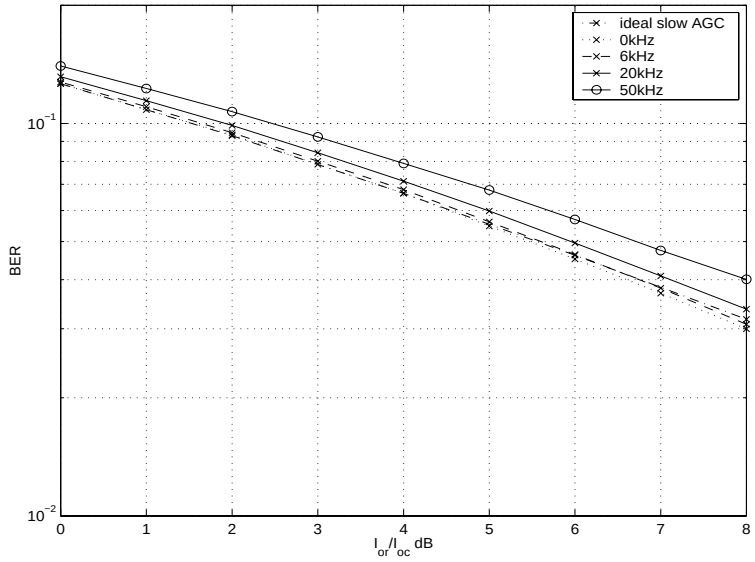

Figure 33: BER versus I_{or}/I_{oc} for different bandwidths and fixed E_c/I_{or}=-2dB. Increasing the DC blockers bandwidths leads to more inter chip interference and thus increased BER. The difference between AGC with bandwidths equal to 0kHz and an ideal slow AGC is less than 0.02dB at 10% BER, so the decay in performance is almost totally due to the DC blockers. The difference between 0kHz and 20kHz, which is the bandwidth used in most simulations, is approximately 0.35dB at 10% BER. There are no big differences at BER equal to 5% compared to BER equal to 10%. At high SNRs the drawback with a very slow ideal AGC become visible.

5.6 Impact of number of bits in AD converter

Another parameter in the WCDMA receiver is the number of bits used in the AD converter. In this simulation 4 versus 5 bits will be investigated. The raw bit error BER was simulated versus I_{or}/I_{oc} for 4 and 5 bits. The choice of channel once again fell on PA-3 because the big difference with and without an AGC. The results for 4 and 5 bits with and without AGC can be found in Figure 34.

When the number of bits is increased to 5 the receiver without AGC gains more than the one with AGC. The SNR gain is approximately 0.1dB respectively 0.05dB at BER equal to 10% and 0.25dB and 0.1dB at BER equal to 5%. The reason for this is that when a larger dynamic range is used in the AD converter the receiver is less sensitive to quantization effects induced by the fading channel. Increasing the number of bits is cost full and power demanding because the memory size must be increased. From this the conclusion is drawn that 4 bits is enough, because other problems such as the DC blocker are of greater importance.

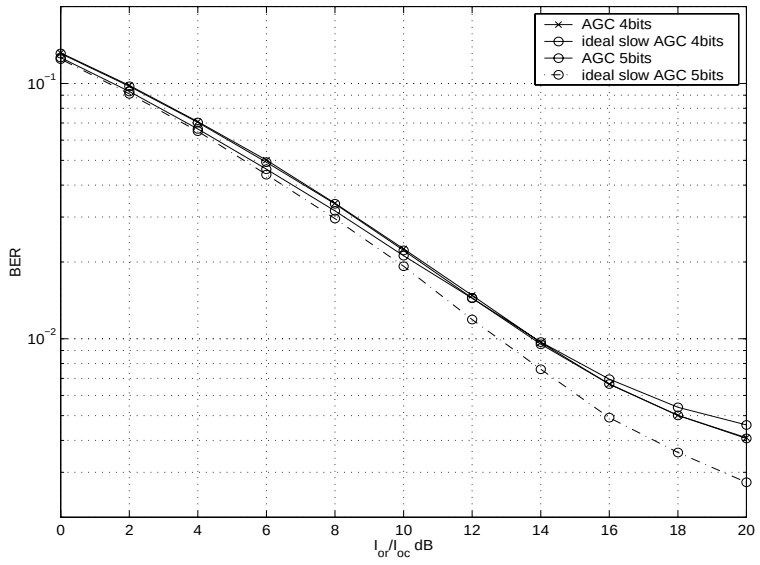

Figure 34: BER versus I_{or}/I_{oc} for different number of bits in the AD converter and fixed E_c/I_{or}=-2dB. The AGC uses 20kHz DC blockers. The performance gain for the receiver with AGC is approximately 0.05dB for 4bits compared to 5bits at BER equal to 10%, whereas the receiver with an ideal slow AGC gains approximately 0.1dB at 10% BER. At BER equal to 5% the corresponding differences are 0.1dB and 0.25dB.

5.7 Impact of Different AGC Designs

In this section a number of control designs will be evaluated. There is no ambition to optimize the design with respect to raw bit error but to see how different designs influence performance in different cases. Two different channel models will be used, the PA-3 model and the VB-120 model. The second one is a one path channel which is more AGC critical, because there is no diversity at all. Simulations were made both with and without DC error and DC blockers. There were no principle differences for different DC blockers bandwidths, so only the simulations with DC disturbances and DC blockers with bandwidth 20kHz will be presented here. The raw bit error BER was simulated versus I_{or}/I_{oc} for different control designs. The designs were made according to the design method used in Section 3.3 but with the controller bandwidth, ω, ranging from 10krad/s to 40krad/s. The relative damping was kept constant equal to 0.36. The AGC was run at 10 times a slot with all other parameters at their default values. The different designs can be found in Table 6

Speed (krad/s)	10	13	15	18.3	20	30	40
K_P	-1.2	-0.1	0.7	2.0	2.6	5.6	7.0
K_I	1.5	2.3	2.8	3.8	4.3	6.6	7.6

Table 6: Different AGC designs with relative damping equal to 0.36.

For the PA-3 channel it seems that it is better to have a slow AGC compared to having a faster one. This is due to the fact that the fadings of the PA-3 channel are very slow so there is no problem for a slow controller to compensate for them. If however a fast controller is used unnecessary gain changes decay performance. There is also no difference between high and low signal to noise ratios. The results from this simulation can be found in Figure 35. At BER equal to 10% the SNR loss from 40krad/s to 10krad/s is approximately 0.07dB and at BER equal to 5% 0.13dB.

When using the VB-120 channel model however, there are differences between high and low signal to noise ratios. For a low SNR the noise is almost equal in amplitude compared to the fading part of the signal. This leads to that the fadings do not dominate the received signal. For a high SNR however the fading part of the signal is totally dominant and thus the speed of the AGC is more important. The optimal AGC speed differs in the two different cases. The low signal to noise ratio case is more equal to the slow fading channel PA-3 whereas the high signal to noise ratio case requires a faster AGC design. The BER versus I_{or}/I_{oc} results can be found in Figure 36.

To determine the optimal bandwidth for the VB-120 channel in these simulations the BER was plotted versus bandwidth for I_{or}/I_{oc} equal to 14dB and 4dB, which correspond to 5% BER and 10% BER. The optimum bandwidth decreases with decreasing I_{or}/I_{oc}. For I_{or}/I_{oc} equal to 14dB the optimum is approximately 30krad/s whereas the optimum for 4dB is close to 20krad/s. The investigation is not to be seen as real optimization, but only to give some insight. As mentioned before the AGC has to be faster if SNR is lower, which is proved by this simple simulation.

The SNR loss for the 10krad/s AGC, which is the optimal choice among the simulated for the PA-3 channel, is approximately 0.25dB compared to the

20krad/s AGC at 10% BER. At 5% BER the 10krad/s is to slow to achieve such low bit error rates, and thus no results are available.

These simulations indicate that the SNR loss is bigger if a slow AGC is used compared to a fast one, but as mentioned in Section 5.4 the VB-120 channel is not a realistic case for HSDPA and thus a slower AGC design is preferred.

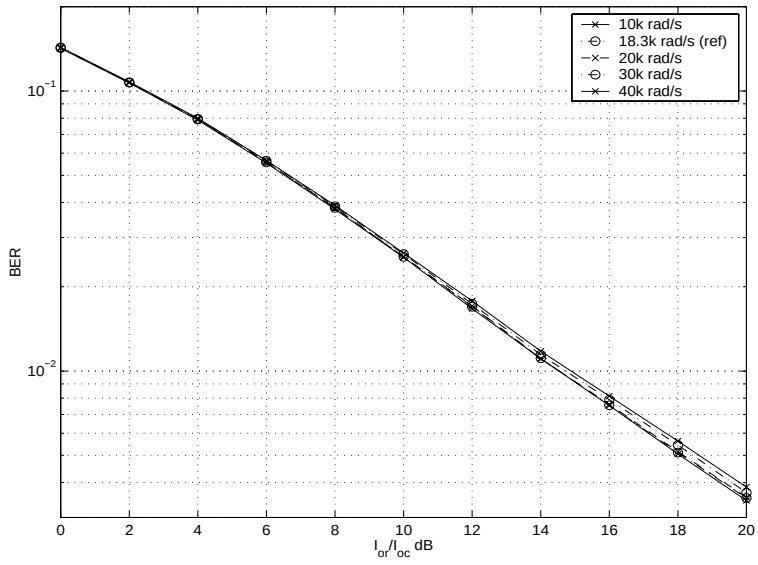

Figure 35: BER versus I_{or}/I_{oc} for different bandwidths (ω) with constant relative damping equal to 0.36 and fixed E_c/I_{or}=-2dB. The channel used in this simulation is the PA-3 channel model. Because of the low velocity a slow AGC design is better. At BER equal to 10% the SNR loss from 40krad/s to 10krad/s is approximately 0.07dB and at BER equal to 5% 0.13dB. From this the conclusion is drawn that the AGC design does not effect BER significantly for the PA-3 channel.

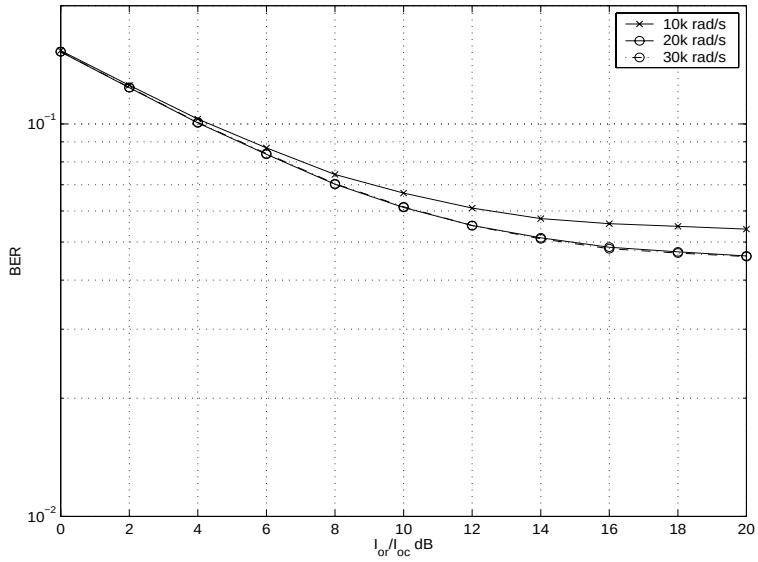

Figure 36: Same prerequisites as in Figure 35 except for the use of the channel model VB-120. The optimal bandwidth is 20krad/s for I_{or}/I_{oc} equal to 4dB, which corresponds to 10% BER. For 5% BER (at 14dB) the optimal bandwidth is 30krad/s. The SNR loss for the 10krad/s AGC, which is the optimal choice among the simulated for the PA-3 channel, is approximately 0.25dB compared to the 20krad/s AGC at 10% BER. At 5% BER the 10krad/s is to slow to achieve such low bit error rates, and thus no results are available.

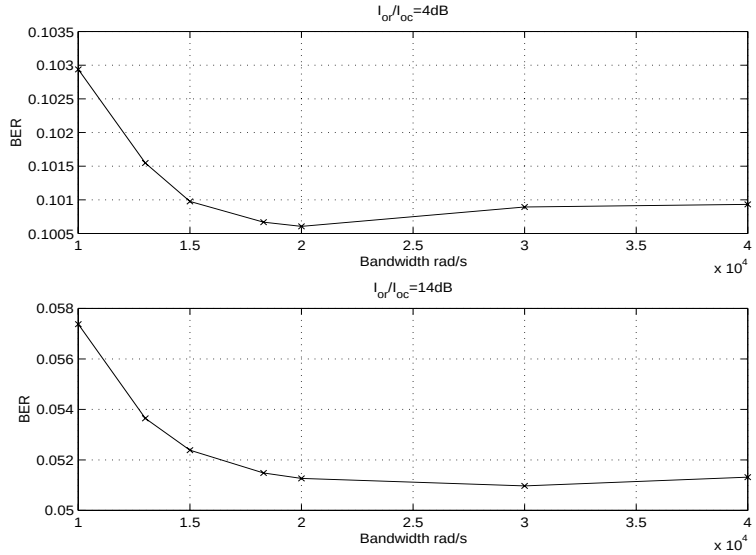

Figure 37: To determine the optimal bandwidth for the VB-120 channel in these simulations the BER was plotted versus bandwidth for I_{or}/I_{oc} equal to 14dB and 4dB, which correspond to 5% BER and 10% BER. The optimum bandwidth decreases with decreasing I_{or}/I_{oc}. For I_{or}/I_{oc} equal to 14dB the optimum is approximately 30krad/s whereas the optimum for 4dB is close to 20krad/s. The investigation is not to be seen as real optimization, but only to give some insight.

5.8 Frequency Error

The goal of this simulation is to investigate the impact of an error in the carrier frequency f_c on the raw bit error. For a description of frequency error see Section 2.3.1. Simulations with both static AWGN (Additive White Gaussian Noise) channel and 1 path fading channels were made. To be able to compare the 16QAM results to the present modulation technique QPSK both modulation techniques were simulated. The transmitted power E_c is assumed to be known and thus no power estimation of the received symbols was made.

First two simulations with a static AWGN channels were made. The bit error rate (BER) was simulated versus I_{or}/I_{oc} for a fixed E_c/I_{or}. Because no fading channel was used the simulations were made without an AGC. 16QAM modulation is more signal to noise ratio demanding so a higher I_{or}/I_{oc} was used to get the same BER as for QPSK. In the AWGN simulations a 4 bit AD converter was used and the channel versus base station energy E_c/I_{or} was fixed to -2dB. All other relevant parameters were kept at their defaults.

In Figure 38 the result for different frequency errors are presented. In the current 3GPP specification the requirement on frequency error is 200Hz or less. For QPSK modulation a frequency error of 200Hz gives a loss in SNR of approximately 0.7dB, whereas a frequency error of 50Hz only gives a loss of 0.06dB at 10% BER compared to no frequency error. At 5% BER the SNR loss increases somewhat, 50Hz gives 0.07dB and 200Hz gives 1.1dB.

In figure 39 BER versus I_{or}/I_{oc} for 16QAM modulation is plotted. 200Hz frequency error gives a SNR loss of 2.2dB, 50Hz error a loss of 0.1dB and 100Hz a loss of 0.5dB at 10% BER. At 5% the corresponding figures are 0.2dB for 50Hz and 1dB for 100Hz. This shows that the frequency error must be kept at a level below 100Hz to have the same impact as for QPSK with frequency errors at 200Hz.

To investigate if the performance degrades further with a 1 path fading channel and an AGC working at 10 times per slot basis another simulation was made. The 1 path fading channel corresponds to the channel experienced by a terminal moving at a speed of 100km/h. All other parameters were fixed to their default values (see section 5). In Figure 40 it can be seen that the performance degrades further with a fading channel and an AGC. The corresponding SNR loss at 10% BER is for 200Hz is 4dB, 0.65dB for 100Hz and 0.15dB for 50Hz. At 5% BER the corresponding figures are 0.65dB for 50Hz and 4.6 dB for 100Hz.

From these simulations the conclusion is drawn that a frequency error below 100Hz is acceptable for AWGN channels whereas the frequency error must be kept below 50Hz for high speed fading channels.

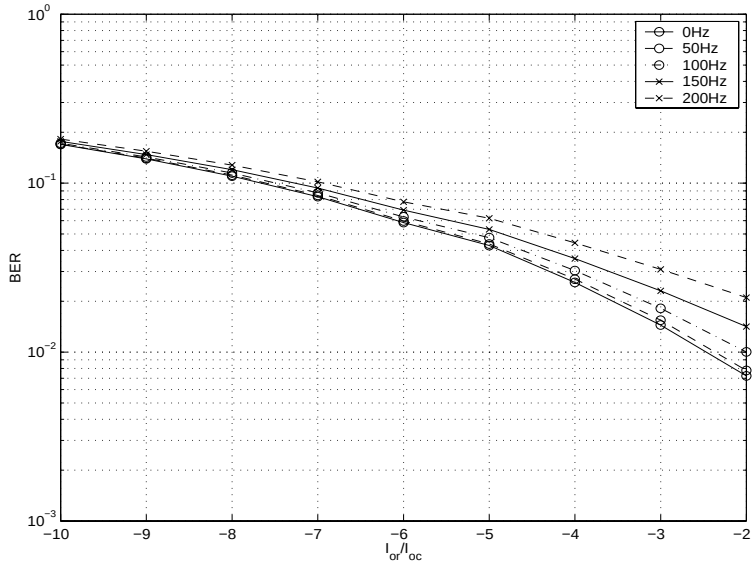

Figure 38: BER for different frequency errors versus I_{or}/I_{oc} for QPSK with AWGN channel and fixed E_c/I_{or}=-2dB. A frequency error of 200Hz gives a SNR loss of 0.7dB.

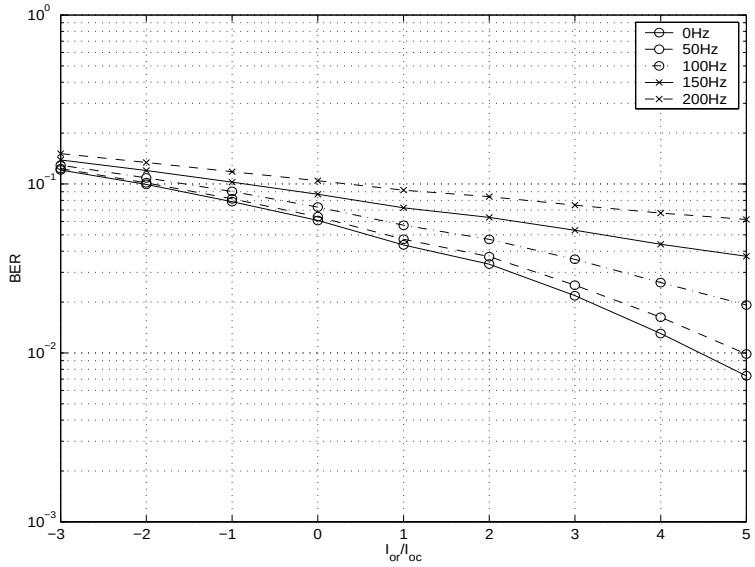

Figure 39: Same prerequisites as in Figure 38 except for 16QAM modulation. If the frequency error is kept below 100Hz the SNR loss is comparable to the SNR loss for QPSK at 200Hz.

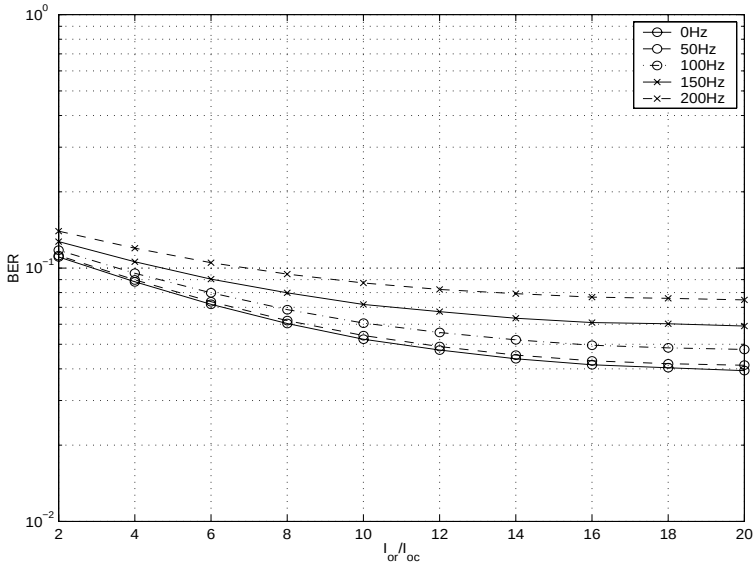

Figure 40: Same prerequisites as in Figure 39 except for a one path fading channel model corresponding to a vehicle velocity of 100km/h. Here the frequency error must be kept below 50Hz have a SNR loss comparable to QPSK at 200Hz.

5.9 Decision Level Error

There are several imperfections in the receiver that influence bit error. LO Leakage and IQ-Imbalance are investigated in [12] and frequency errors were investigated in the previous section. When the modulation technique 16QAM is used, the hard decision making is a bit more complicated than for QPSK modulation. In QPSK the only relevant information is the phase of the received symbols, whereas 16QAM is dependent on amplitude information as well. The purpose of this simulation is to investigate how sensitive 16QAM is to errors in the decision levels. 1000 slots of 16QAM modulated data over a 1 path fading channel corresponding to a velocity of 100km/h was simulated and the decision levels were changed in the interval -20dB to 20dB. This notation is defined as $20log_{10}(\frac{level}{level_0})$, where $level_0$ is the correct decision level. The AGC was run 10 times per slot and E_c/I_{or}=-2dB and I_{or}/I_{oc}=-4dB. All other parameters were set at their defaults.

In figure 41 it can be seen that, as expected, only bit 3 and 4 are influenced by the decision level error. The reason for this is that bit 1 and 2 can be view as QPSK modulated because of the coding mentioned in section 2.1.2. The BER for bit 3 and 4 appears to be unsymmetrical. The reason for this is that the absolute error for i.e. 1dB and -1dB are unequal. If the correct decision level is assumed to be unity, then the absolute errors equal 0.1220 and -0.1087 respectively. To further investigate the impact of decision level error the BER was simulated under the same circumstances as above, but now versus I_{or}/I_{oc}. The result is shown in figure 42. In figure 42 one can see that i.e a decision level error of 2dB corresponds to a SNR loss of 1.95dB at 10% BER. The SNR loss due to decision level error for different level errors is presented in table 5.9.

$level/level_0$ [dB]	*SNR Loss [dB] at 10%*	*SNR Loss [dB] at 5%*
-0.6	0.14	0.2
0.6	0.1	0.25
-1.2	0.49	1.0
1.2	0.51	1.4
-2	1.28	3
2	1.95	7

Table 7: SNR losses at 5% and 10% BER due to decision level errors for 16QAM.

To get an idea on achievable decision level errors let us calculate the level error in dB for a situation where the power estimate (33) is made over one slot. The calcualtions are made according to Section 2.3.9. Both positive and negative absolute errors will be presented. The decision level errors for different spreading factors would then be

Spreading factor	*D(x)*	*Positive level/level$_0$ [dB]*	*Positive level/level$_0$ [dB]*
4	0.040	0.34	-0.35
8	0.056	0.47	-0.50
16	0.079	0.66	-0.72
32	0.11	0.92	-1.0
64	0.16	1.3	-1.5
128	0.22	1.8	-2.2
256	0.32	2.4	-3.3

Table 8: Level errors in dB corresponding to an absolute error equal to the standard deviation for different spreading factors. A spreading factor of about 16 gives acceptable results at 10% BER.

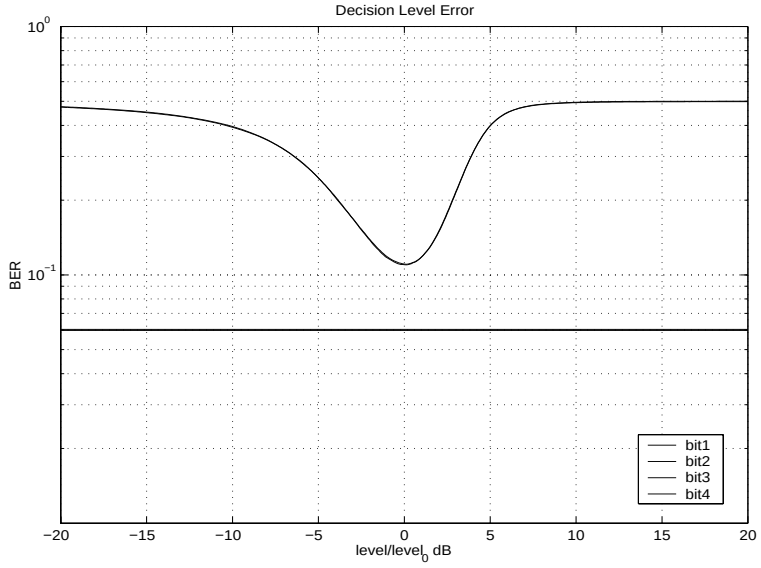

Figure 41: BER versus decision level error using 16QAM for vehicular velocity equal to 100km/h. Amplitude information only crucial for bit 3 and 4. E_c/I_{or} fixed at $-2dB$ and I_{or}/I_{oc} equal to $-4dB$.

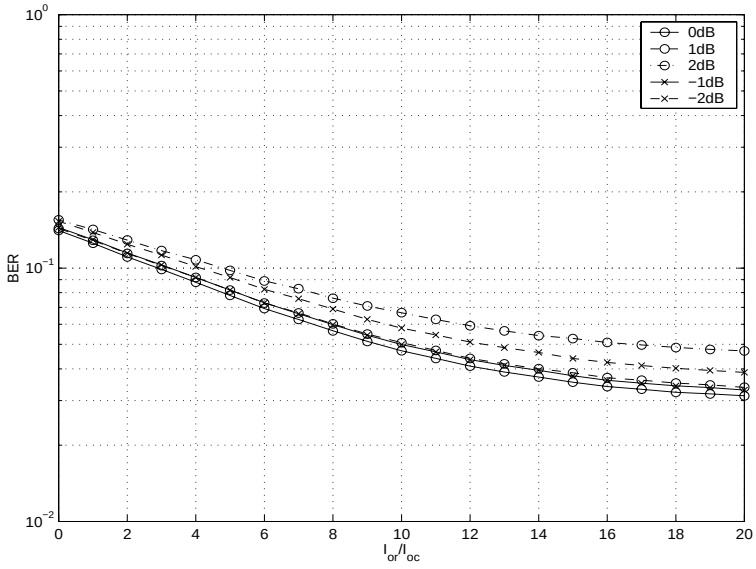

Figure 42: BER versus I_{or}/I_{oc} for different decision level errors using 16QAM for vehicular velocity equal to 100km/h with $E_c/I_{or} = -2dB$.

5.10 Quantization Effects on Orthogonality

In Section 2.1.3 it was described how different channels within the same transmitter are separated by the use of orthogonality. But how do imperfections in the receiver influence the orthogonality between channels? To investigate this BER was simulated versus E_c/I_{or} with E_c/I_{oc} constant. In theory the raw bit error should not be affected when changing E_c/I_{or} if E_c/I_{oc} is kept constant, but when a channel is using a very small part of the total base station energy imperfections in the receiver become significant. 1000 slots of 16QAM and QPSK was simulated with an AWGN channel. Because no fading channel was used no AGC was necessary. If a simulation with an AGC would have been done, the problem of choosing P_{ref} for different number of bits occurs. This would have introduced another parameter, which would have influenced the results. All other parameters were kept at their default values.

In Figure 43 BER versus E_c/I_{or} using QPSK modulation is simulated for different number of bits in the AD converter. To be able to have channels with a very small portion of the total base station energy the AD converter should have at least 5 bits. If for example 50 speech channels share the same base station the corresponding E_c/I_{or} equals approximately -17dB. To maintain good separation between channel in this case a 6 bit AD converter is needed.

One of the ideas in HSDPA is however to direct a very large portion of the total base station energy to on channel. Typical E_c/I_{or} rates range from 1dB to perhaps -5dB. To investigate the quantization impact on 16QAM 1000 slots were simulated and the result is given in Figure 44. Because a large portion of the base station energy is used, quantization effects are moderate. As seen in the simulation a 4 bit AD converter is sufficient.

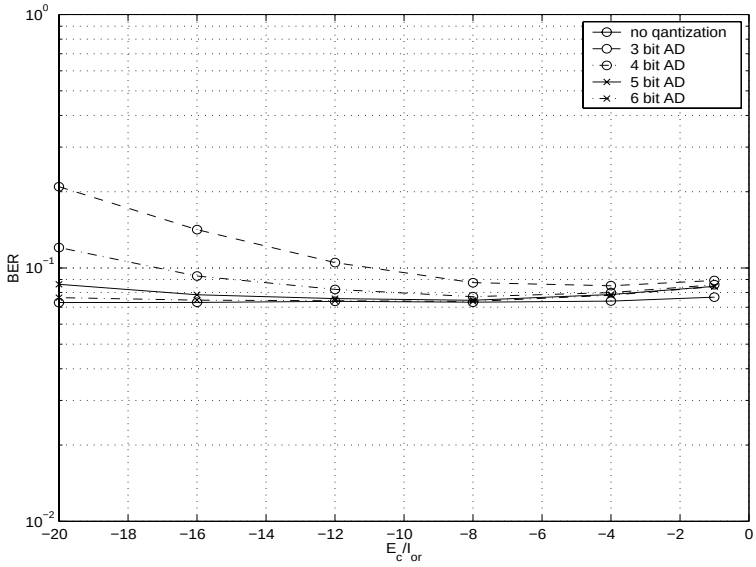

Figure 43: BER versus E_c/I_{or} for constant E_c/I_{oc}=-3dB using QPSK modulation and with a AWGN channel. The quantization effects become more visible with lower signal to noise ratios. In an ideal receiver all BER should have been constant.

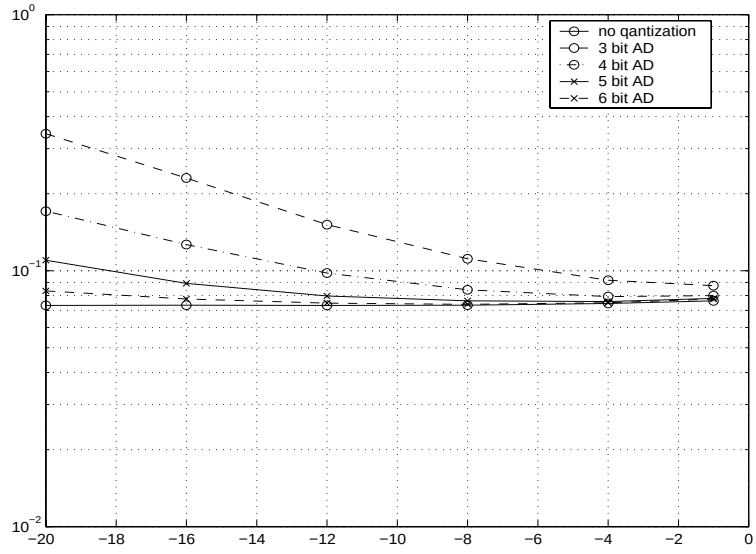

Figure 44: Same as Figure 43 but with 16QAM modulation and E_c/I_{oc}=3dB. The quantization effects become more visible for 16QAM than for QPSK modulation.

6 Conclusions and Future Research

From the simulations the conclusion is drawn that 16QAM is more sensitive to frequency errors than QPSK and that an important parameter in the AGC is the DC blocker bandwidths. It looks like the current requirement of 200Hz frequency error must be lowered to 50Hz for the receiver to be able to use 16QAM modulation.

The optimal AGC design depends on the type of channel model used, but it seems that a slower AGC design is preferred when compared to a faster one in respect to bit error rate. In the step response simulations however a faster AGC design is preferable. What controller to choose thus depend on the requirements of the step response. The AGC seems to be more important at high signal to noise ratios because the fading become more visible in that case.

Some of the simulation results might give the impression that the AGC does not improve performance at all. If however the results of slow fading are also considered the AGC is crucial to the functionality of the receiver.

The choice of DC blocker bandwidth is an important parameter that must be given some attention. Choosing the DC block bandwidth is a trade off between disrupting the signal and rejecting DC. Today the DC levels are relatively small and thus the DC blocker bandwidth can be lowered compared to the 20kHz used in most simulations.

All simulations have been made without making a power estimate of the received symbols. This implies that the base station must signal the current power to the UE. In a real WCDMA system this is not the case, and thus future investigations should implement for example the power estimation solution instead.

A subject of future research would be to add coding and interleaving to the simulation environment, which will give some more insight in the subject.

It could also be investigated how the receiver performs with a GRAKE structure, see [10].

One way to improve the DC disturbance rejection would perhaps be to estimate the DC disturbances and then use some kind of feed forward in the compensation loop. This could be a field of future investigations.

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A Orthogonal Code Generation

To be able to fully separate individual channels from each other the real valued spreading codes $C^o_{i,j,k}$ have to be orthogonal to each other. Orthogonal codes must fulfill the following properties

- Full correlation with itself
- No correlation with another orthogonal codes

These two properties can be summarized as

$$\frac{1}{S_f}\sum_{i=0}^{S_f-1} C^o_{n,i,j,k}C^o_{m,i,j,k} = \begin{cases} 0, & n \neq m \\ 1, & n = m \end{cases} \tag{87}$$

One way of generating such codes is to use a Walsh code tree, see Figure 45. The basic principle behind this method is that every code on level i forms two codes on level $i+1$. The first consists of two copies of the previous one and the second of one copy and one inverted copy. These codes have the property that they are all orthogonal within the same level, but only orthogonal to codes higher up in a different branch. The codes are numbered $C^o_{i,j,k}(l, nr)$ where $nr = 0, 1, .., 2^j - 1$ and l denotes the level in the tree starting at 1.

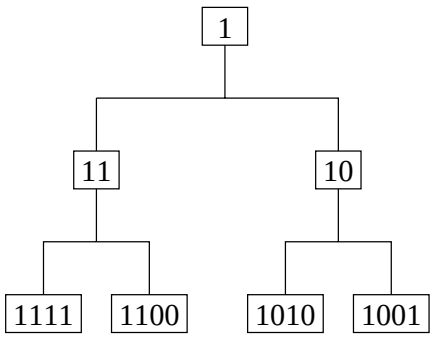

Figure 45: Generation of orthogonal Walsh codes. A 0 represents -1 and a 1 a 1 when converted to complex representation.