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A carbon nanotube gated carbon nanotube transistor with 5 ps gate delay**

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Abstract

Semiconducting carbon nanotubes (CNTs) are attractive as channel material for field-effect transistors due to their high carrier mobility. In this letter we show that a local CNT gate can provide a significant improvement in the subthreshold slope of a CNT transistor compared to back-gate switching and provide gate delays as low as 5 ps. The CNT-gated CNT transistor devices are fabricated using a two-step CVD technique. The measured transfer characteristics are in very good agreement with theoretical modelling results that provide confirmation of the operating principle of the transistors. Gate delays below 2 ps should be readily achievable by reducing the thickness of the gate dielectric.

Introduction

Carbon nanotubes exhibit excellent electronic properties that make them attractive as nanoelectronic components. Metallic CNTs can withstand current densities higher than 10^{10} A/cm^2 [1], they have a thermal conductivity of around 2000 W/mK [2] and their conductivity does not degrade with diameter in contrast to normal metal wires, which makes them ideal for interconnect applications [3]. On the other hand, quasi-one-dimensional FETs using semiconducting CNTs as channels are competitive with silicon-based devices [4] due to the long mean free path of CNTs resulting in a high mobility [5] and their small diameter enabling excellent electrostatic control by a gate electrode.

So far improvements in the characteristics of CNT field effect transistors (CNTFETs) have been made through introducing better contact metals [6], using high-k dielectrics as gate insulators to improve the gate to channel capacitance [7] and by reducing the length of the CNT channel to achieve ballistic transport. A limiting factor of scaling down the length of devices is the resolution of electron beam lithography which gives a minimum device length of around 20 nm [1]. These limitations can be circumvented by using a single metallic CNT as a gate [8-10]. The small diameter of the CNT gate gives a short effective channel length while reducing parasitic capacitances detrimental to high frequency operation. Moreover, in a recent theoretical study, a possibility to overcome the thermal limit for the subthreshold slope has been demonstrated in a CNTFET with a suspended CNT gate [11].

In this letter, we present results on the fabrication, characterisation and modeling, of CNTFETs that utilise semiconducting CNTs as channel material and metallic CNTs as gate electrodes (see Figure 1a). We use a doubly-gated structure where a back gate is used to create source and drain regions within the semiconducting CNT by electrostatic doping, and a local CNT gate controls carrier transport through the central section of the channel CNT. We demonstrate that improved subthreshold characteristics and shorter gate delay times are achieved compared to using a back gate alone. A device with a local gate also enables bulk switching which is desirable due to the variability of the properties of metal-CNT contacts [12]. Other devices using CNTs as local gates have either used bundles of tubes giving a poor on/off ratio due to the presence of metallic CNTs [13] or

have used manipulation of individual CNTs using atomic force microscopy (AFM) which is not suitable for large scale production or integration [10]. While our previous work relied on CVD growth of the channel CNT and dielectrophoretic deposition of the CNT gate [8, 9] we here present a more reproducible method of fabricating CNT gated CNTFETs utilising two CVD process steps to grow both the channel CNT and the gate CNT. We also provide a theoretical model for operation of CNT-gated CNTFETs based on diffusive transport in the channel CNT with concentration-dependent carrier mobility [14]. The calculated transfer characteristics based on this model are in good agreement with experimental results. We use the model to extract the gate capacitance, which allows an estimation of the gate delay time, and to explore the performance of different device geometries. For instance, we examine how the gate delay time scales with gate dielectric thickness and conclude that a gate delay time of less than 2 ps can be readily achieved with a dielectric thickness less than 10 nm.

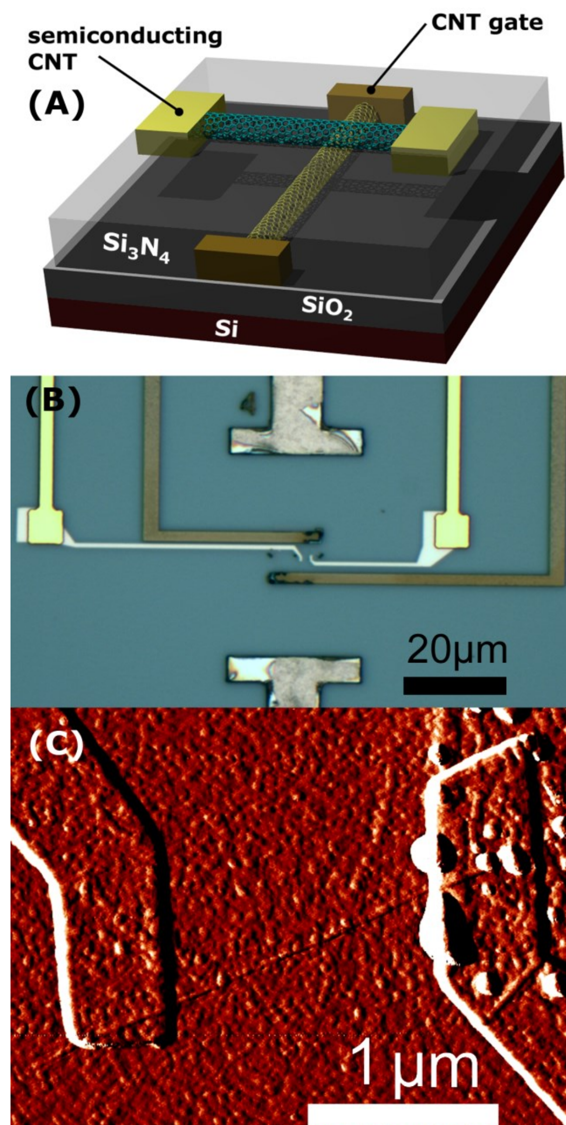

Figure 1. (A) Schematic illustration of a CNTFET with a CNT gate. The lower CNT gate is connected by two metal contacts (brown) and separated from the upper channel CNT by 30 nm Si_3N_4. The source and drain

contacts for the channel CNT are shown in yellow. (B) Optical microscopy image of a device. Upper and lower T-shaped electrodes are used for electric field directed growth. The L-shaped electrodes are Mo contacts to gate CNTs. Pd electrodes to the semiconducting CNT are seen in between the Mo electrodes. (C) AFM amplitude image of the device showing a horizontal semiconducting CNT crossing over a vertical gate CNT. The particles close to the right electrode are from catalyst material used for the 2nd CVD step.

Device fabrication

The substrates used for the devices are highly n-doped Si with a 1 μm thermally grown SiO_2 layer on top. The CNTs acting as gate electrodes are grown from 5 nm Al_2O_3 / 0.5 nm Fe catalyst islands, patterned with electron beam lithography, using thermal chemical vapour deposition (CVD) at 900°C with 1000 sccm of CH_4 and 100 sccm of H_2. An electric field with an average strength of 1V/μm is applied using pairs of Mo electrodes in the vicinity of the catalyst areas to direct the growth of CNTs yielding straight, oriented tubes (Figure 1c) [15]. Ti/Mo electrodes are patterned as contacts to the gate CNTs. A 30 nm Si_3N_4 layer acting as gate dielectric is deposited on the entire substrate using plasma enhanced CVD (PECVD) at 300°C and holes are etched in the film using a CF_4/Ar plasma to achieve electrical contact to the gate CNTs. Si_3N_4 is chosen due to its excellent thermal stability and in addition the lack of oxygen makes the deposition process benign to CNTs [16]. The deposition has no effect on the electrical properties of metallic CNTs while the initially p-type semiconducting CNTs change to n-type due to desorption of oxygen, which is a hole donor, and subsequent passivation. Other gate dielectrics such as SiO_2 deposited by PECVD damage the CNTs, while Al_2O_3 deposited by atomic layer deposition, which has proved to be a good dielectric for CNTFETs [8, 17] does not withstand CVD growth of CNTs. If Al_2O_3 is used as a dielectric the highly reducing atmosphere at the high growth temperature results in electrical shorting through the SiO_2 possibly due to metal diffusion into the oxide. After deposition of the dielectric layer, new catalyst is patterned and a second CVD step is performed to grow the CNTs used as channel materials in the CNTFETs. Perpendicular crossings are located using scanning electron microscopy (SEM) or AFM and 0.5 nm Ti / 30 nm Pd contacts are patterned on the upper CNTs. Electrical measurements are performed in a Cascade probe station using a Keithley S4200 parameter analyser using both the Si back gate (V_{BG}) and the CNT gate (V_{CNTG}) to modulate the source drain current (I_d). Several devices with similar electrical characteristics have been fabricated using this method.

Experimental Results

An optical image and an AFM image of a CNT gated CNTFET with a semiconducting CNT with a diameter of 1.8 nm are shown in Figure 1. The diameter of the CNT gate underneath the Si_3N_4 is difficult to estimate

using AFM since the Si_3N_4 does not conformally coat the CNTs. However, AFM and transmission electron microscopy studies confirm that the CNTs are mostly single walled with an average diameter of 1.6±0.8 nm.

We first study whether both the back-gate and CNT gate can be used to switch a device between ON and OFF states. We measure I_d as a function of both V_{CNTG} and V_{BG}, with the source grounded and drain bias set to V_d=100 mV. Results are presented in Figure 3 for the device shown in Figure 1. It is clear that either of the gates can be used to switch the device only if the voltage on the other gate is sufficiently negative to open the transport channel.

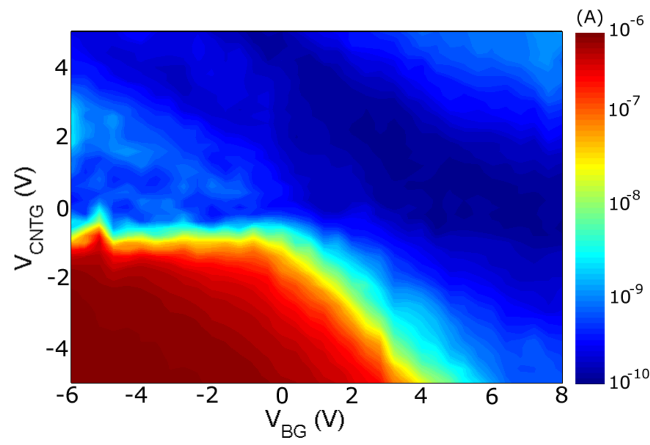

Figure 3. The drain current I_d as a function of both V_{CNTG} (sweeping) and V_{BG} (stepping) at V_d=100 mV on a logarithmic scale. The colour scale is from I_d=150 pA (dark blue) to I_d=0.6 µA (red).

We extract quantitative switching parameters of the device from transfer characteristics measured at three different V_d. These characteristics, obtained by sweeping V_{CNTG} (V_{BG}) using a fixed V_{BG} (V_{CNTG}) are shown in Figure 4a (b). The maximum on/off ratio is around 10^3 and the on state resistance R_{ON}=125 kΩ for both gates but the inverse subthreshold slope $(d(\log_{10} I_d)/dV_g)^{-1}$ at V_d=100 mV is S=259 mV/dec for the CNT gate and S=667 mV/dec for the back gate sweep. The inverse subthreshold slope is still far from the ideal S=60 mV/dec at 300K but, as will be discussed later, it can be improved by using a thinner dielectric. The output characteristics shown in the inset of Figure 4a saturate for high V_d in the ON state which is expected for a device not suffering from short channel effects [[18]]. The appearance of a threshold voltage for I_d in the output characteristics for positive V_{CNTG} is due to the doubly gated structure: a current can only flow in the device if the Fermi level of the drain is below the valence band edge in the CNT gated region. This condition can either be achieved by decreasing V_{CNTG} or increasing V_d.

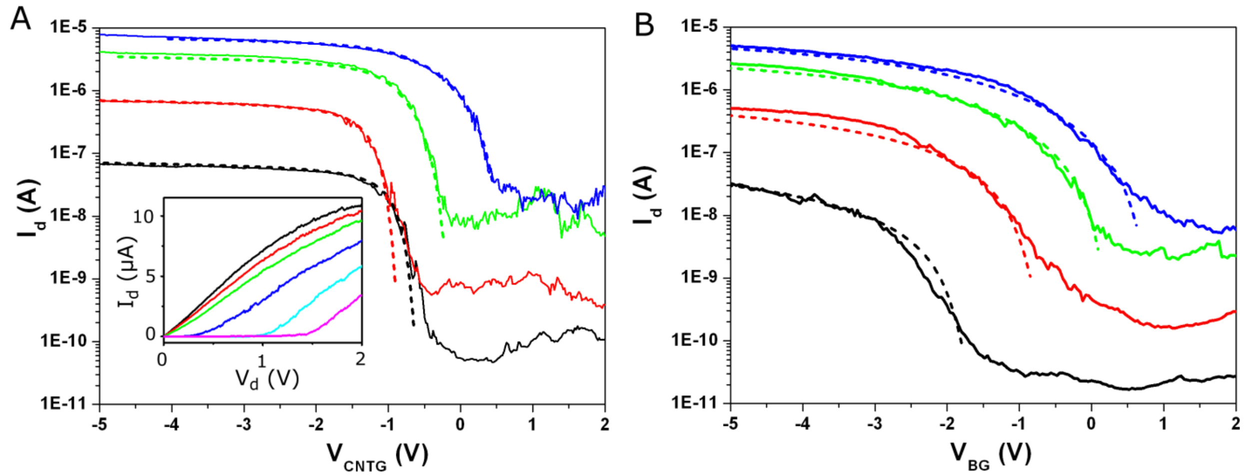

Figure 4. (A) Transfer characteristics obtained by sweeping V_{CNTG} at V_d=10,100,500,1000 mV (bottom to top) with a fixed V_{BG} = -10 V. The inset shows output characteristics for V_{CNTG} from -3 to 2 V in increments of 1V top to bottom. (B) Transfer characteristics obtained by sweeping V_{BG} with a fixed V_{CNTG} = -5 V. Solid lines show experimental data and dashed lines the predictions of the theoretical model.

Theoretical Modelling

To study the operation of the CNT gated CNTFET, we use a theoretical model which has been developed to describe the operation of a CNTFET with a suspended CNT gate [11]. The model assumes the transport in the channel CNT to be diffusive [14, 19, 20] and describes the charge transfer between source and drain electrodes and CNT channel using thermionic emission and tunneling [19]. Since Pd, which has a high work function giving a high Schottky barrier for electrons, is used for the contacts in the experimental device, the electron current is disregarded in the theoretical model. In the simulation, the channel and gate CNT lengths are set to 1500 and 1800 nm respectively and their diameters to 1.8 nm, as determined experimentally. The contact widths and heights are 1500 and 50 nm, respectively. The dielectric constants of the Si_3N_4 gate spacer and SiO_2 substrate are 6.5 and 3.9, respectively. The Schottky barrier height for holes is set to 100 meV. We use a simplified geometry in the simulation compared to the experimental device, which assumes that the channel and gate CNTs cross at their central points and the channel CNT ends are attached to the centers of the contacts. Changing the position of the crossing point between the nanotubes i.e. moving the CNT gate closer to the source or drain contacts does not affect the simulation results substantially which serves as a further evidence of the local switching mechanism by the CNT gate.

The calculated carrier concentration profiles in the ON and OFF states for devices with only a back gate or with both a back gate and a CNT gate are shown in Figures 2a and 2b. We see that the back gate controls the overall carrier density on the channel while the CNT gate has a local effect and can be used to create a localized depletion region. The depletion width, estimated to be around 170 nm, is the effective length of the

CNT gated device. This is to be contrasted to back-gated CNTFET, in which the effective length is the whole length of the channel CNT. The channel to gate capacitance is smaller in the CNT gated case, but the amount of charge that needs to be removed in order to turn the device OFF is much lower compared to the back gated structure. Since a small change in gate voltage results in a large change in concentration in the effective channel, and therefore conductance, this provides a steep inverse subthreshold slope as well as a short switching time. Moreover, the barrier for electrons in the OFF state is as high as in the on state, as seen from the insets in Figure 2, which ensures a monopolar behavior of the device.

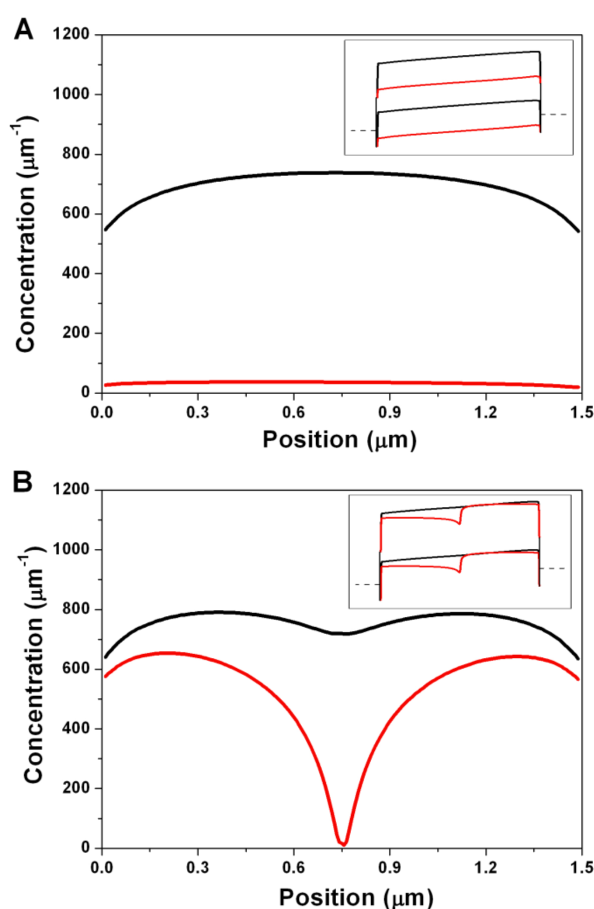

Figure 2. (A) Calculated concentration profiles along the channel CNT in back-gate controlled CNTFET for V_{BG}=-8V (black line) and V_{BG}=-0.5 V (red line). (B) Concentration profiles in a CNT-gate controlled CNTFET for V_{CNTG}=-3V (black line) V_{CNTG}=2.3V (red line). The insets show the band profiles of the channel CNT.

Discussion

The calculated transfer characteristics are plotted in Figure 4, for the back gate, CNT gate, source and drain voltages that are used in the experiments. The threshold voltages of the calculated data have been adjusted to

the experimental ones since hysteresis effects from charge trapping are not included in the theoretical model. The only fitting parameter of the model, the scattering time at high energies τ_0 [14], is found to be 0.13 ps. The agreement between experimental and calculated results is remarkably good over a large range of CNT gate and back gate voltages. However the calculation can not accurately account for the off state current since only hole currents are considered in the model.

The intrinsic gate delay is given by τ=CV/I, where C is the capacitance between the channel and the gate, $V=V_{dd}$ the supply voltage used to switch the device between the ON and OFF states, and $I=I_{on}$ is the on state current [21]. This defines a minimum switching time neglecting effects from parasitic capacitances, and gives an indication of the maximum possible operating frequency. The threshold voltage (V_{th}) of a CNTFET is difficult to control mainly due to charge trapping [22] whereas in Si MOSFETs it can be controlled by doping or by selecting a gate metal with a suitable work function. To compare devices with different V_{th} a method described in Ref.[21] is used where τ is plotted against I_{on}/I_{off} for different positions of a gate voltage window of width V_{dd} that is moved along the gate voltage axis in the transfer characteristics (Figure 5a). The CNT gate to channel capacitance of $C_{CNTG}=dQ/dV_{CNTG}$=10 aF and a back gate capacitance of C_{BG}=15.2 aF are extracted from the theoretical model and used in the calculation of the delay time. At the maximum on/off ratio of 100 and $V_{dd}=V_d$=1 V the delay time is τ =5 ps for the CNT gate, while using the back gate gives a delay time of τ =57 ps at a poor on/off ratio of 15 for the same $V_{dd}=V_d$=1 V. This shows that the CNT gate gives both an improvement in on/off ratio and shorter gate delay compared to the back gate. The delay time obtained using the CNT gate is comparable to recent results on Ge/Si nanowires [23] and p-MOSFETs with ~100 nm channel length [21].

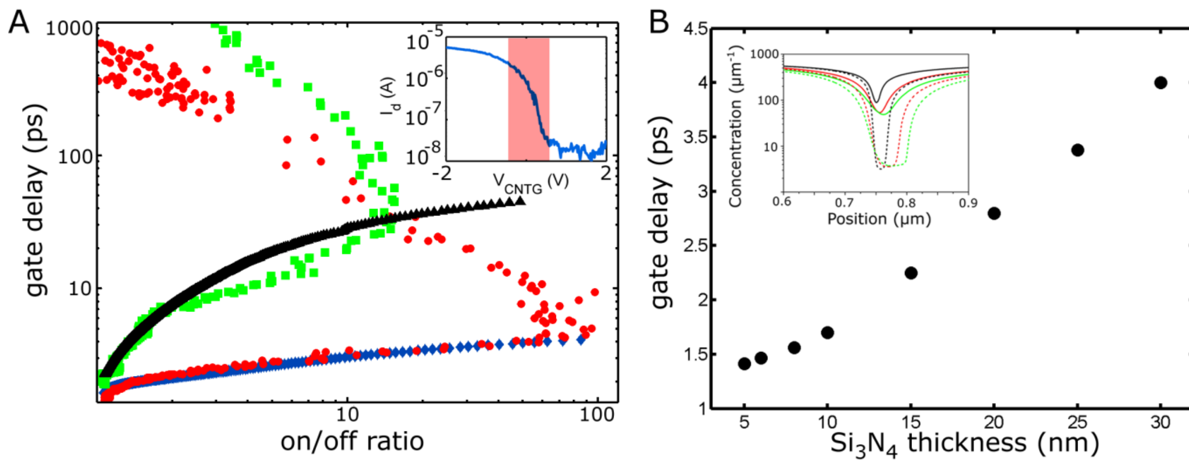

Figure 5. (A) Delay time as a function of on/off ratio calculated from the experimental (red circles) and theoretical (blue diamonds) data for the CNT gate and experimental (green squares) and theoretical (black triangles) data for the back gate sweep in Figure 3 using $V_{dd}=V_d$=1 V. The inset shows the transfer characteristics for the back gate sweep with the V_{dd} window corresponding to the maximum on/off ratio

highlighted. (B) Gate delay at an on/off ratio of 100 as a function of thickness of the Si_3N_4 gate dielectric obtained from numerical calculation. The inset shows the charge distribution along the channel CNT for a Si_3N_4 thickness of 10 (black), 20 (red) and 30 (green) nm for both the on (solid lines) and the off state (dashed lines).

To explore possible improvements obtained by reducing the gate dielectric in CNT gated CNTFETs we have carried out the theoretical analysis for different Si_3N_4 thicknesses. We find that the delay time, which is calculated with V_{dd}=1 V at an on/off ratio of 100, is reduced with a decreasing thickness of the Si_3N_4 (Figure 5b). A device with thinner dielectric also has a steeper subthreshold slope due to the stronger gate to channel coupling. For a dielectric thickness of 5 nm, which is well within experimental limitations, an inverse subthreshold slope of S=68 mV/dec and a delay time of τ =1.4 ps, i.e. a maximum operating frequency of 700 GHz, can be achieved. The fast switching is due to the fact that the potential from the CNT gate becomes more local as the dielectric thickness is reduced and thus a smaller amount of charge has to be moved in the semiconducting CNT to switch the device OFF as seen in the hole concentration profiles in the inset of Figure 5b. The effective device length is reduced to ~40 nm for a 5 nm thick gate dielectric. We also find that reducing the length of the channel CNT does not considerably reduce the gate delay time since the effective channel length is not affected. However, the ON state conductance increases with decreasing CNT length, which is beneficial for high frequency operation. On the other hand, too short CNT length would result in increased parasitic gate to source and gate to drain capacitances which would limit the high frequency performance.

Conclusion

In summary, we have used a novel method to reproducibly fabricate CNTFETs locally gated by metallic CNTs. Due to the short gate length, fast gate delay times are achieved. Further improvements can be made by making the Si_3N_4 thinner which would improve the subthreshold slope while allowing for an even shorter gate delay time. The work presented here shows that it is possible to construct individual high performance transistors based on crossed nanotubes, but to produce entire integrated circuits of such devices will require more exact control of the position and electrical characteristics of the CNTs to obtain a sufficient yield of operational devices. However, recent success in producing more complex patterns of CNTs [[24]] and making electromechanical devices entirely out of CNT material [[25]] shows that techniques for tailoring CNT structures are progressing.

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