Vapor Deposition of Highly Conformal Copper Seed Layers for Plating Through-Silicon Vias (TSVs)

Journal of The Electrochemical Society, **159** (6) D382-D385 (2012)
0013-4651/2012/159(6)/D382/4/$28.00 © The Electrochemical Society

Vapor Deposition of Highly Conformal Copper Seed Layers for Plating Through-Silicon Vias (TSVs)

Yeung Au,[a] Qing Min Wang,[b] Huazhi Li,[b] Jean-Sebastien M. Lehn,[b] Deo V. Shenai,[b] and Roy G. Gordon[a,*,z]

[a]*Department of Chemistry & Chemical Biology, Harvard University, Cambridge, Massachusetts 02138, USA*
[b]*Dow Electronic Materials, North Andover, Massachusetts 01845, USA*

Through-silicon vias (TSV) will speed up interconnections between chips. Manufacturable and cost-effective TSVs will allow faster computer systems. In this paper, we report the successful formation of seed layers for plating copper TSVs with aspect ratios greater than 25:1. Following the rapid atomic layer deposition (ALD) of a conformal insulating layer of silica inside the silicon vias, manganese nitride (Mn_4N) is deposited conformally on the silica surface by chemical vapor deposition (CVD). Mn_4N forms an effective copper diffusion barrier and provides strong adhesion between the silica and the subsequently-deposited copper. Conformal copper or copper-manganese alloy films are then deposited by an iodine-catalyzed direct-liquid-injection (DLI) CVD process. Diffusion of manganese during post-deposition annealing further enhances the barrier and adhesion properties at the copper/dielectric interface.
 [DOI: 10.1149/2.097206jes]

Manuscript submitted December 16, 2011; revised manuscript received March 27, 2012. Published April 13, 2012. This was Paper 1948 presented at the Boston, Massachusetts, Meeting of the Society, October 9–14, 2011.

Metal interconnections in microelectronics have been typically fabricated in a planar, 2-dimensional (2-D) fashion. 3-dimensional (3-D) integration has gained a lot of interest as a way to enhance the performance of microelectronic systems.[1] 3-D integration has been shown to reduce the number and the average lengths of 2-D global wires by providing shorter vertical paths for connection. In addition, 3-D integration has the potential to further improve system performance and to enable new system architectures.[2] Through-silicon vias (TSV) will provide faster interconnections between multiple dies in advanced 3D-packaging applications.[3] Metallization of TSVs will become more and more challenging as the aspect ratios of vias continue to increase. The 2010 International Technology Roadmap for Semiconductors (ITRS) calls for copper TSVs with aspect ratios of 10:1 by 2012 and 20:1 by 2015.[4] One critical step in the production of TSVs is the preparation of a continuous barrier that will keep metals from diffusing out from the vias. A smooth and conductive copper seed layer is also necessary to initiate copper electroplating. Strong adhesion must also be provided between the copper seed layer, the diffusion barrier and the underlying insulator. Due to their poor step coverage, conventional physical vapor deposition (PVD) methods will no longer be able to cover the sidewalls of these high aspect ratio features with the necessary layers.[5]

In this report, we introduce a new method to make conformal, smooth and strongly adherent barriers and copper seed layers inside holes with aspect ratios greater than 25:1 by vapor deposition. A rapid ALD process is first applied to form a conformal insulating layer of silicon dioxide (SiO_2) inside the vias.[6] Next manganese nitride (Mn_4N), an effective copper diffusion barrier and adhesion layer, is deposited conformally on the silica surface by CVD. Iodine is then chemisorbed onto the surface of the thin manganese nitride layer to catalyze the CVD of smooth copper or copper-manganese alloy seed layers.[7] A direct-liquid-injection (DLI) CVD method is used to deliver consistent and high vapor concentrations of copper precursor and to coat the high aspect ratio holes with conformal copper or copper-manganese seed layers. A post-deposition annealing step diffuses manganese from the copper film to the surfaces of the insulators to further strengthen the copper/insulator interface by forming a self-aligned barrier and adhesion layer. Thus, TSVs are provided with conformal and smooth copper seed layers that adhere strongly to a very thin diffusion barrier just inside the surface of the conformal silica insulator.

*Electrochemical Society Active Member.
[z]E-mail: Gordon@chemistry.harvard.edu

Experimental

Patterned silicon substrates with TSV-like holes were obtained from Tokyo Electron (TEL) with aspect ratio of 26 to 1. These substrates were cleaned by a UV/ozone cleaner (Samco model UV-1, wavelengths = 185 nm and 254 nm) for 5 minutes at room temperature to remove organic contaminants from the substrates. An insulating layer of aluminum-doped silicon dioxide 20 nm thick was deposited by ALD, as described in an earlier report.[6] This rapid ALD process forms a highly conformal layer on silicon by reacting trimethyl aluminum (TMA) with tris(*tert*-butoxy) silanol [$(Bu^tO)_3SiOH$]. More than 12 nm of insulator can be deposited in each ALD cycle even in holes with aspect ratio greater than 50:1.[6] This silica layer can plug pores in the underlying insulator layer,[8] and creates a clean, uniform silica surface which promotes dense, uniform nucleation and growth of the films made by the subsequent CVD processes.

A schematic diagram of the CVD system is shown in Figure 1. The compound that serves as a precursor for manganese and manganese nitride is bis(*N*, *N*′-di-*iso*-propylpentylamidinato)manganese(II), whose chemical formula is shown in Figure 2a. The precursor for copper deposition is (*N*,*N*′-di-*sec*-butylacetamidinato)copper(I) dimer and has the chemical structure shown in Figure 2b. To prepare manganese nitride by CVD, the manganese precursor was evaporated from the liquid in a bubbler at a temperature of 90°C into a 60 sccm flow of highly purified nitrogen. 60 sccm of ammonia (NH_3) and an additional 60 sccm of purified nitrogen were mixed with the manganese precursor vapor just before entering the reactor held at a temperature of 130°C and a pressure of 5 Torr, controlled by an MKS Baratron pressure gauge coupled to an automatic throttle valve. After deposition of manganese nitride was complete, the substrate was cooled in the reactor in a flow of pure nitrogen in order to protect the manganese nitride film from oxidation. Ethyl iodide (CH_3CH_2I) was then used as an iodine source to adsorb iodine atoms onto the fresh surface of the manganese nitride film at room temperature. The liquid ethyl iodide was contained in a bubbler at room temperature and its vapor was fed directly into the reactor without a carrier gas, controlled by a needle valve to a pressure of 0.05 Torr. Conventionally, the copper precursor was evaporated from the liquid in a bubbler at a temperature of 130°C into a 40 sccm flow of highly purified nitrogen.[7] Here, a direct-liquid-injection (DLI) CVD method was adopted instead to provide consistently higher partial pressure of copper precursor vapor, thereby enhancing the growth rate and the conformality of the copper films. To prepare copper films using the DLI-CVD method, 25 g of copper precursor was first dissolved in 100 mL of dodecane ($C_{12}H_{26}$), a solvent with vapor pressure close to that of the copper precursor, to

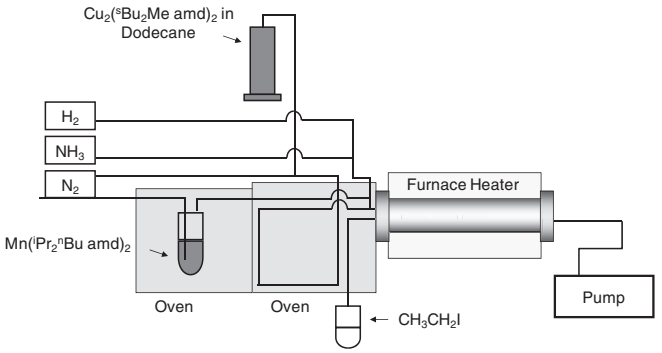

Figure 1. Schematic diagram of the DLI-CVD system.

make a solution with a concentration of 0.72 molal or 0.43 molar and a density of 0.79 g/mL, measured at 21°C. The saturated solubility of the copper precursor in dodecane was determined to be ∼1.3 molar. The precursor solution was kept at room temperature in a stainless steel syringe sealed by 2 O-rings. The flow of the precursor solution was controlled by a syringe pump (KD Scientific model 210) at flow rates from 0.05 cm^3/min. The precursor solution was mixed with 40 sccm of nitrogen carrier gas at room temperature in a tee, from which the precursor solution was vaporized while flowing down into a coil of stainless steel tubing (1.8 m long, 1/4 inch outside diameter) kept at 160°C in an oven.[9] Completeness of the vaporization process can be checked by inserting a glass viewport into the lowest point at the end of the tubing, to make sure that no liquid collects there. An oven temperature of 120°C was found to be too low to completely evaporate the liquid, while 160°C was sufficiently high to evaporate all the liquid at the flow-rates used. The vapor mixture exiting from this tubing was then mixed at a tee with 100 sccm of hydrogen just before entering the reactor held at a temperature of 180°C and a pressure of 5 Torr. Under these conditions, the injection rates of copper precursor, dodecane, hydrogen (100 sccm) and nitrogen (40 sccm) are 3.6×10^{-7} mol s^{-1}, 2.9×10^{-6} mol s^{-1}, 7.4×10^{-5} mol s^{-1}, and 3.0×10^{-5} mol s^{-1}, respectively, for a total vapor and gas injection rate of 1.1×10^{-4} mol s^{-1}. Based on these flow rates, the mole fraction of copper precursor in the total gas plus vapor flow is 0.0033. The reactor is held at a total pressure of 5 Torr, so the partial pressure of copper precursor vapor inside the reactor is 0.017 Torr, and the partial pressure of hydrogen gas is 3.4 Torr. If manganese was to be co-deposited with the copper, a flow of 60 sccm of purified nitrogen gas was passed through the manganese bubbler at 90°C. This flow of manganese precursor vapor in nitrogen was mixed with copper precursor vapor just prior to entering the deposition zone.

In a typical CVD process to form copper seed layers in TSV features, ∼ 20 nm of silica layer was first deposited by ALD at 250°C to insulate the metal from silicon. Manganese nitride was then deposited at 130°C for 5 minutes to form 2.5 nm of film. Ethyl iodide was then introduced into the chamber at room temperature for 30 seconds. Copper or copper-manganese alloy was finally deposited at 180°C until a sufficiently conductive layer (sheet resistance below 0.8 ohms per square) was formed in the vias, which typically took around 10 minutes. The Mn/Cu ratio was quantified by X-ray fluorescence (XRF). A post-deposition annealing step at 350°C for one hour in nitrogen ambient was carried out after the iodine-catalyzed CVD process to diffuse the manganese from the copper-manganese alloy to the copper/insulator interface. The conformality of the Mn_4N and the copper seed layers were evaluated by scanning electron microscopy (SEM). A thicker Mn_4N layer was deposited for 100 minutes so that its conformality could be observed more clearly by SEM. The surface morphology of the copper seed layer was studied by atomic force spectroscopy (AFM). The sheet resistance of the films was measured by a four-point probe.

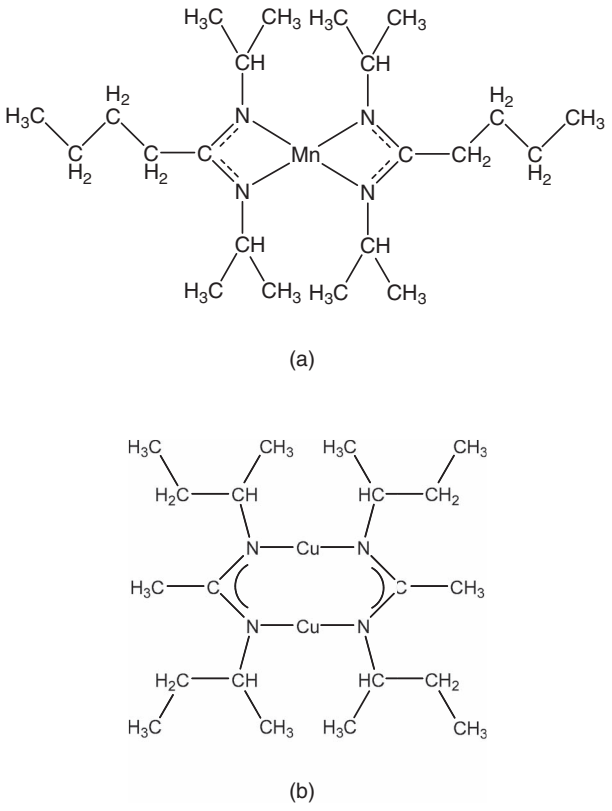

Figure 2. Formula for the (a) Mn precursor and (b) Cu precursor.

Results and Discussion

A conformal layer manganese nitride film can be prepared by CVD at 130°C in holes with aspect ratios of 26:1. A thick (95–100 nm) Mn_4N layer is shown in Figure 3 to demonstrate conformal deposition. The effective aspect ratio of the holes is much greater than 26:1 as the diameter of the holes is narrowed during the course of deposition. The defect in the bottom of the via is caused by damage during the hand-cleavage of the sample. The polycrystalline manganese nitride film is conductive, with a resistivity value of 198 mΩ-cm. Annealing the manganese nitride film at 200°C for one hour promotes the formation of larger grains and results in a lower resistivity value of 2.01 mΩ-cm. It is possible to prepare conformal manganese nitride films at higher substrate temperatures, but the flow rate of NH_3 must then be decreased to prevent fast surface reactions, which lead to poor conformality. For example, vias with aspect ratios up to 50:1 can be coated with conformal Mn_4N using NH_3 and H_2 flow rates of 5 and 55 sccm, respectively, at a substrate temperature of 180°C. Surface reactivity may also be lowered by choosing a manganese amidinate precursor with bulkier ligands, such as *tert*-butyl groups, attached to the nitrogens in place of the smaller *iso*-propyl groups. Manganese nitride films as thin as 2.5 nm form barriers against copper diffusion.[7] A four-point bend method was used to evaluate the adhesion between silica and the later-deposited CVD of copper, and the debonding energies were found to be greater than 6.5 J m^{-2}, which is high enough to survive further fabrication by chemical-mechanical polishing.[4,7,10,11]

When vapors of ethyl iodide are exposed to manganese nitride films, iodine atoms are chemisorbed onto the surface. During subsequent CVD of copper, the iodine desorbs from the Mn_4N surface and floats on the surface of the growing copper film. The presence of iodine atoms may weaken the bond between copper and its ligands and facilitate the dissociative chemisorption of the precursor on the copper surface,[12] resulting in the enhancement of the growth rate and surface smoothness of the copper films.[7,13]

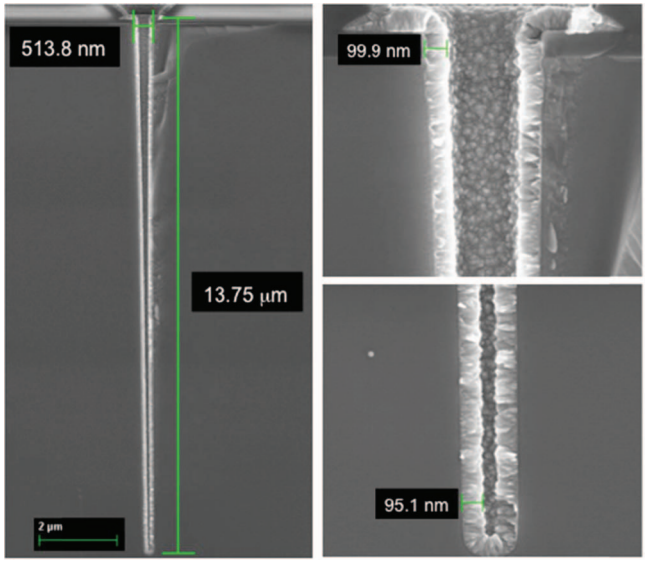

Figure 3. Cross-sectional SEM image showing highly conformal step coverage of manganese nitride underlayer in vias with aspect ratio 26:1.

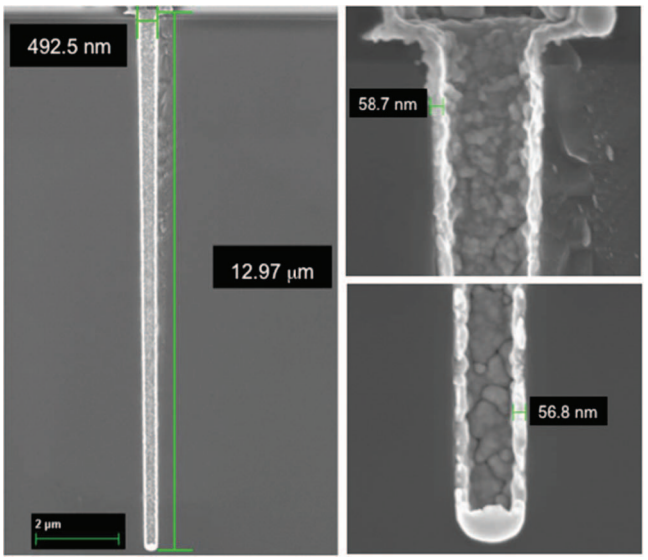

Figure 4. Cross-sectional SEM image showing highly conformal step coverage of Cu-Mn seed layer in vias with aspect ratio 26:1.

Smooth and continuous copper seed layers can be deposited by vaporizing the copper precursor from a conventional bubbler. TSV via features with aspect ratios up to 4.6:1 can be conformally coated with a copper seed layer. Vias with aspect ratio up to 10:1 can be conformally coated by increasing the copper precursor carrier gas to 100 sccm and the working pressure to 10 Torr, both of which changes increase the partial pressure of the copper precursor inside the deposition region. This conventional bubbler delivery of precursor vapor, however, fails to form a continuous copper layer in the bottoms of vias with aspect ratios beyond 10:1 due to insufficient concentration of precursor vapor, especially for substrates with extremely high via density (9×10^6 holes cm^{-2}). The direct-liquid-injection (DLI) method delivers a much higher partial pressure of the precursor vapor than vaporization from conventional bubblers. By supplying a high concentration of copper precursor vapor, the deposition is operating in the surface reaction-controlled regime. At deposition temperatures around 180°C, slow surface reactions permit a uniformly high concentration of precursor vapor to be delivered to the entire length of the vias. As a result, continuous and highly conformal copper-manganese films are deposited on manganese nitride underlayers inside via holes with aspect ratio over 26:1 (Figure 4). The vapor delivery rate from the DLI system is stable, reproducible and accurately known because the concentration of the solution and the liquid and carrier gas injection rates are known and steady. In contrast, the vapor delivery rate from a conventional bubbler is subject to uncertainty in vapor pressure, temperature variation, thermal decomposition, and effects of fill level.

Cross-section SEM and AFM images of a thicker copper film on a planar substrate show that the copper seed layer deposited on an iodine-exposed manganese nitride underlayer is fairly smooth, with a root-mean-square roughness equal to 6.2% of its thickness (Figure 5). Manganese content in the copper-manganese alloy was analyzed by XRF to have approximately 0.5 atomic% of manganese in copper. Adjusting the temperature of the manganese precursor bubbler or the flow rate of the nitrogen carrier gas through the bubbler can vary the concentration of manganese in the alloy film.

A post-deposition annealing step at 350°C is incorporated to diffuse the manganese from the copper-manganese alloy to the copper/insulator interface and to return the resistance of the copper seed layer to a lower value. Our earlier report[11] showed that manganese diffuses through the grain boundaries of the polycrystalline copper, and this diffusion process enhances the interfacial adhesion between copper and insulators such as silicon oxide, silicon nitride and low-k dielectric. While manganese nitride provides sufficient adhesion energy to survive chemical-mechanical polishing, the presence of additional manganese in the seed layer can further strengthen the copper/insulator interface and potentially achieve longer electromigration lifetime.[14] The debonding energy increases approximately linearly with the manganese content at the interface, up to values beyond 14 J m^{-2}.[11] The resulting self-aligned interfacial layer, manganese silicate ($MnSi_xO_y$), forms within a few nm of the surface of the insulator, and is an excellent barrier to diffusion of copper,[15,16] oxygen and water.[15] By diffusing the manganese out from the copper-manganese alloy

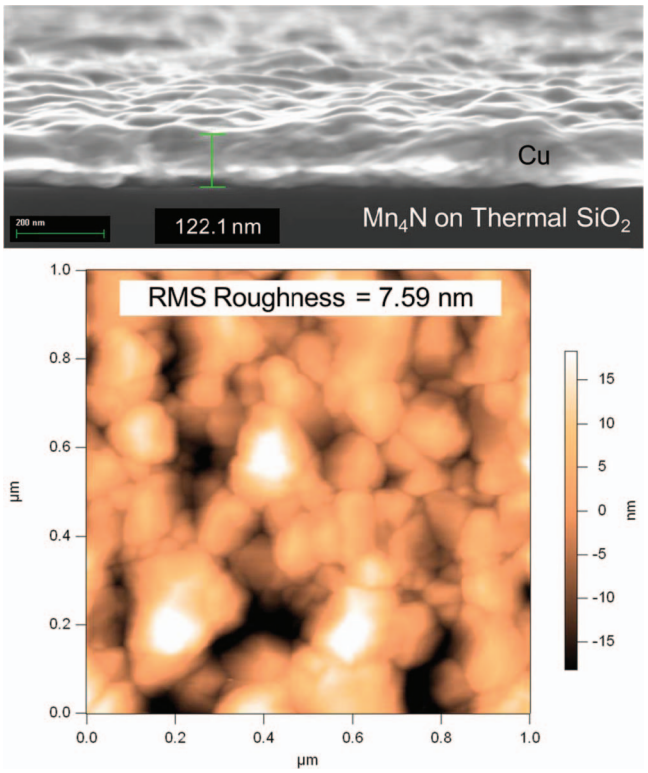

Figure 5. Cross-section SEM and AFM images measuring a root-mean-square roughness equals to 6.2% of the thickness of the Cu seed layer.

film, the sheet resistance is determined to be 0.46 ohms per square for the copper seed layer shown in Figure 4, which is sufficiently conductive for the later electroplating step (<0.8 ohms per square). The resistivity of this seed layer is about 2.69 μΩ cm, which is about the resistivity expected for a pure copper layer 58 nm thick.[17] It is also possible to carry out the annealing step after the electroplating of copper to diffuse manganese in the seed layer to the Cu seed/electroplated Cu interface, thereby preventing delamination of the plated Cu film from the seed layer.

Conclusions

Conformal and conductive copper seed layers for metallization of TSVs were successfully prepared in high aspect ratio holes by DLI-CVD. A conformal insulator layer was first deposited by ALD to separate the metal from the substrate silicon, and a manganese nitride liner layer was then deposited on the insulator. The CVD process was catalyzed by iodine as a catalytic surfactant to achieve higher growth rate and smoother morphology. The DLI-CVD method enhanced the delivery of precursor vapors even to the bottoms of dense arrays of vias and resulted in nearly perfect conformality. The presence of manganese at the copper/insulator interface further improves the adhesion and barrier properties at the interface. This process forms a highly robust and conductive seed layer for metallizing future generations of copper vias in advanced 3-D integration. It satisfies the ITRS requirements beyond the end of the roadmap.

Acknowledgments

We appreciate the advice of Dr. Zhefeng Li in constructing the DLI system. The copper and manganese precursors were supplied by Dow Chemical Company. The high aspect ratio via substrates were provided by TEL. This work was performed in part at the Center for Nanoscale Systems (CNS), a member of the National Nanotechnology Infrastructure Network (NNIN), which is supported by the National Science Foundation under NSF award no. ECS-0335765. CNS is part of the Faculty of Arts and Sciences and the School of Engineering and Applied Sciences at Harvard University.

References

1. E. Beyne, *Proceedings of the IEEE International Interconect Technology Conference (IITC) IEEE*, 1 (2006).
2. R. Havemann and J. Hutchby, *Proc. IEEE* **89**, 586 (2011).
3. J. Van Olmen, A. Mercha, G. Katti, C. Huyghebaert, J. Van Aelst, E. Seppala, Z. Chao, S. Armini, J. Vaes, R. C. Teixeira, M. Van Cauwenberghe, P. Verdonck, K. Verhemeldonck, A. Jourdain, W. Ruythooren, M. de Potter de ten Broeck, A. Opdebeeck, T. Chiarella, B. Parvais, I. Debusschere, T. Y. Hoffmann, B. De Wachter, W. Dehaene, M. Stucchi, M. Rakowski, P. Soussan, R. Cartuyvels, E. Beyne, S. Biesemans, and B. Swinnen, *IEDM Tech. Dig.*, 603 (2011).
4. The International Technology Roadmap for Semiconductors (2009).
5. S. Armini, Z. El-Mekki, K. Vandersmissen, H. Philipsen, S. Rodet, M. Honore, A. Radisic, Y. Civale, E. Beyne, and L. Leunissen, *J. Electrochem. Soc.*, **158**(2), H160 (2011).
6. D. Hausmann, J. Becker, S. Wang, and R. G. Gordon, *Science*, **298**, 402 (2002).
7. Y. Au, Y. Lin, and R. G. Gordon, *J. Electrochem. Soc.*, **158**(5), D248 (2011).
8. P. de Rouffignac, Z. Li, and R. G. Gordon, *Electrochem. Solid-State Lett.* **7**(12), G306 (2004).
9. Z. G. Xiao, *Rev. Sci. Instrum.* **74**(8), 3879 (2003).
10. E. Andideh, J. Blaine, C. Block, B. Jin, T. Scherban, and B. Sun, *Proc. IEEE 2001 Int. Interconnect Technology Conf.*, 257 (2001).
11. Y. Au, Y. Lin, H. Kim, E. Beh, Y. Liu, and R. G. Gordon, *J. Electrochem. Soc.* **157**(6), D341 (2010).
12. Q. Ma, H.-S. Guo, R. G. Gordon, and F. Zaera, *Chem. Mater.* **22**(2), 352 (2010).
13. E. S. Hwang and J. Lee, *Chem. Mater.* **12**, 2076 (2000).
14. M. Lane, E. Liniger, and J. Lloyd, *J. Appl. Phys.*, **93**, 1417 (2003).
15. R. G. Gordon, H. Kim, Y. Au, H. Wang, H. B. Bhandari, Y. Liu, D. K. Lee, and Y. Lin, *Advanced Metallization Conference 2008* XXIV, 321 (2009).
16. J. Iijima, M. Haneda, and J. Koike, *IEEE Int. Interconnect Technol. Conf., Proc.*, 155 (2006); J. Koike and M. Wada, *Appl. Phys. Lett.*, **87**, 041911 (2005).
17. Z. Li, A. Rahtu, and R. G. Gordon, *J. Electrochem. Soc.*, **153**(11), C787 (2006).