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GaAs Enhancement-Mode NMOSFETs Enabled by Atomic Layer Epitaxial $(\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3)$ as Dielectric

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GaAs Enhancement-mode NMOSFETs Enabled by Atomic Layer Epitaxial $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ as Dielectric

L. Dong, X. W. Wang, J. Y. Zhang, X. F. Li, R. G. Gordon and P. D. Ye, *Fellow, IEEE*

Abstract—We demonstrate high performance enhancement-mode (E-mode) GaAs NMOSFETs with an epitaxial gate dielectric layer of $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ grown by atomic layer epitaxy (ALE) on GaAs(111)A substrates. A 0.5- μm -gate-length device has a record-high maximum drain current of 336 mA/mm for surface-channel E-mode GaAs NMOSFETs, a peak intrinsic transconductance of 210 mS/mm, a subthreshold swing of 97 mV/dec and an $I_{\text{ON}}/I_{\text{OFF}}$ ratio larger than 10^7 . Thermal stability of the single crystalline $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ -single crystalline GaAs interface is investigated by capacitance-voltage (C - V) and conductance-voltage (G - V) analysis. High temperature annealing is found to be effective to reduce the D_{it} .

Index Terms—Atomic Layer Epitaxy (ALE), enhancement mode (E-mode), GaAs MOSFET

I. INTRODUCTION

As the device scaling and performance improving continues, silicon CMOS technology is approaching its fundamental physical limits. Meanwhile, III-V semiconductors have gained more and more attention, as they are promising candidates for replacing silicon owing to their high electron mobility and high saturation velocity [1-5]. During the past decades, tremendous efforts have been made to improve the oxide-GaAs interface, which is crucial for device performance [6-9]. However, despite some encouraging progress, the surface channel E-mode GaAs NMOSFETs still exhibit relatively low current drivability due to the high interface trap density (D_{it}) at the oxide-GaAs interface even on (111)A substrate [9,10]. In this letter we demonstrate, for the first time, that by using atomic layer epitaxy (ALE) [11,12] to deposit the gate dielectric, high-performance GaAs surface channel NMOSFETs can be achieved. These devices show low subthreshold slope (SS) around 97 mV/dec and high on-state current (I_{ON}) of 336 mA/mm, which is one order of magnitude higher than that of other reported devices [9,10]. Systematic

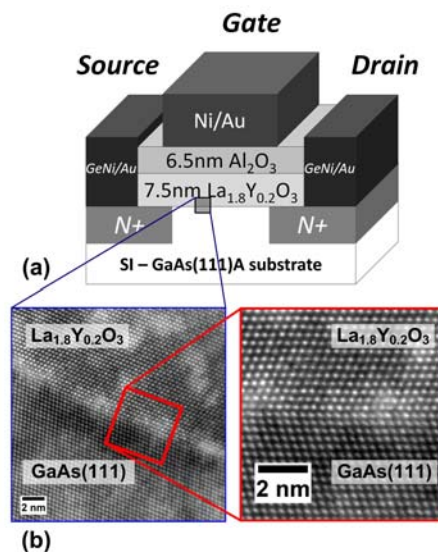


Fig. 1. (a) Cross section of a GaAs(111)A surface channel E-mode NMOSFET. (b) High-resolution TEM image and enlarged view of the single crystalline GaAs – single crystalline $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ interface after 860°C RTA annealing. The epitaxial $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ forms a flat and sharp interface on GaAs(111)A substrate.

study of C - V and G - V characteristics confirms that this novel epitaxy has excellent quality of interface, and it is thermally stable for the fabrication process of the inversion-mode GaAs NMOSFETs.

II. FABRICATION OF GAAS NMOSFETS

The cross-sectional view of a GaAs(111)A NMOSFET is schematically illustrated in Fig. 1(a). The fabrication started on 2-inch GaAs(111)A semi-insulating wafers. (111)A surface is favorable for GaAs NMOSFET since it's difficult to form As-As bonds which would pin the Fermi-level in GaAs [13]. As received GaAs wafers were first degreased by acetone, methanol and isopropanol, and then dipped in diluted HCl to remove native oxide. Then the wafers were soaked in 10% $(\text{NH}_4)_2\text{S}$ for 15 minutes at room temperature for surface passivation. After the sulfur passivation and de-ionized water rinse, the wafers were quickly transferred into the deposition chamber within less than 1 minute for dielectric deposition. 7.5 nm $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ was deposited by ALE in this work, followed by 6.5 nm Al_2O_3 serving as a capping layer to prevent La-oxide reacting with water in the air and/or during the process. The deposition of $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ film involves precursors of lanthanum tris($\text{N,N}'$ -diisopropylformamidinate), yttrium tris($\text{N,N}'$ -diisopropyl-acetamidinate) (from the Dow Chemical Company) and H_2O , and the deposition of Al_2O_3

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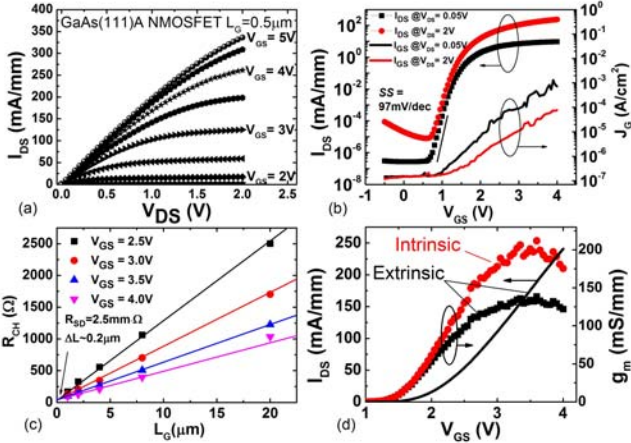


Fig. 2. (a) Current-voltage (I - V) characteristic of a 0.5 μ m-gate-length GaAs NMOSFET with ALE $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ gate oxide. (b) Transfer characteristics and gate leakage current density of the same GaAs NMOSFET as (a). (c) Measured channel resistance versus different mask gate length as a function of gate bias. R_{SD} of 2.5 Ω -mm and ΔL of ~ 0.2 μ m are determined from the fitting lines. (d) Extrinsic and intrinsic transconductance (g_m) and extrinsic drain current versus gate bias of the same GaAs NMOSFET in (a).

used trimethylaluminium(TMA) and H_2O as the precursors. The base pressure of the reactor chamber was 0.3 Torr. In each cycle, the exposure of the La and Y precursors was 0.003 Torr-seconds and the exposure of H_2O was 0.06 Torr-seconds. After each H_2O pulse, the chamber was purged under nitrogen flowing for 80 s to minimize the amount of water and/or hydroxyl groups trapped in the oxide film, as they considerably degrade the crystallinity and permittivity. More detailed deposition process is described elsewhere [12]. To fabricate the devices, source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 30 keV and 1×10^{14} cm^{-2} at 80 keV. Implantation activation was achieved by rapid thermal anneal (RTA) at 860 $^\circ\text{C}$ for 15 seconds in N_2 ambient. The source and drain areas were defined by photolithography and then covered by evaporated Au/Ge/Ni/Au metal stack. After a lift-off process, RTA at 400 $^\circ\text{C}$ for 30 seconds in 1 atm. pressure of N_2 was performed to form ohmic contacts. The device fabrication process was completed with electron beam evaporation of Ni/Au as gate electrodes, followed by a lift-off process. The fabricated devices have a nominal gate length (L_G) varying from 0.5 μm to 40 μm , while the gate width is fixed at 100 μm . The MOS capacitors were fabricated on p-type (Zn doped) GaAs(111)A substrates with doping level of $5\text{-}7 \times 10^{17}$ cm^{-3} and n-type (Si doped) GaAs(111)A substrates with doping level of $6\text{-}9 \times 10^{17}$ cm^{-3} . The same oxide stacks of 7.5 nm $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/6.5$ nm Al_2O_3 were used. Ni/Au as the top gate metal was used for the capacitor fabrications. Some of the oxide-GaAs stacks were annealed in N_2 prior to gate electrode formation for studying the thermal stability of the oxide-GaAs interface.

III. RESULTS AND DISCUSSION

As shown in Fig. 1(b), the high-resolution transmission electron microscopy (HRTEM) image shows that the single crystalline $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ -single crystalline GaAs (111)A interface is atomically sharp and flat, and the lattice planes are well aligned. This epitaxial structure of $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}$ was further confirmed by high resolution X-ray diffraction

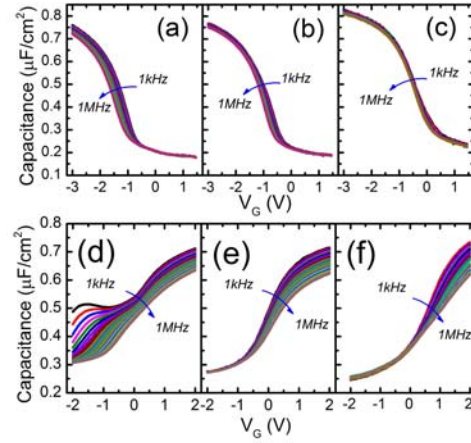


Fig. 3. C-V characteristics of the Ni/ Al_2O_3 / $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ /GaAs(111)A p-type and n-type MOS capacitors of as-deposited samples (a and d), 600 $^\circ\text{C}$ annealed samples (b and e) and 800 $^\circ\text{C}$ annealed samples (c and f). The samples b, c, e and f were annealed in a rapid thermal anneal (RTA) system for 30 seconds in nitrogen atmosphere.

(HRXRD) [12], and the lattice mismatch between $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ and GaAs, determined by HRXRD, is -0.67%. The output characteristics and transfer characteristics of a $L_G = 0.5$ μm GaAs(111)A NMOSFET are plotted in Fig. 2(a) and (b), respectively. The gate leakage current density is also plotted in Fig. 2(b). At gate bias of 5 V and drain bias of 2 V, a high maximum drain current of 336 mA/mm is achieved, which is a significant improvement of the on-state current compared with the previously reported GaAs (111)A NMOSFETs with amorphous Al_2O_3 as the gate dielectric [10]. We believe this is due to the novel high-quality $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ -GaAs epitaxial interface that passivates surface dangling bonds on GaAs surface such that the interface traps are greatly reduced. [11, 12] Peak mobility of these devices is determined to be 310 cm^2/Vs at inversion charge density of $2 \times 10^{12}/\text{cm}^2$ by split-CV method. It reduces to 230 cm^2/Vs at $7 \times 10^{12}/\text{cm}^2$ inversion charge density. Drive current and channel mobility could be further enhanced using GaAs buried channel structure [7] or incorporation of InGaAs higher mobility channel materials [3-5]. Our GaAs NMOSFETs also exhibit a high I_{ON}/I_{OFF} ratio greater than 10^7 (I_{OFF} at $V_G = 0.5$ V and $V_D = 2$ V; I_{ON} at $V_G = 2.3$ V and $V_D = 2$ V). This high I_{ON}/I_{OFF} ratio is a promising feature for GaAs as compared to InGaAs, since the latter usually suffers from high S/D leakage current as a result of its relatively narrower bandgap. The NMOSFETs with any gate length fabricated in the work (i.e. from 0.5 μm to 40 μm) consistently show a low $SS \sim 97$ mV/dec, suggesting a low D_{it} of $\sim 3.0 \times 10^{12}/\text{cm}^2\text{-eV}$ in the mid-gap using $SS = 60$ mV/dec ($1 + qD_{it}/C_{ox}$). We notice that the gate leakage current increases from $\sim 10^{-7}$ A/cm² to $\sim 10^{-3}$ A/cm² as the gate bias increases from 0 V to 4 V, but still the leakage current is 5 orders of magnitude lower than the drain current ($V_G = 4$ V). Fig. 2(c) shows the effective gate length (L_{eff}) and the series resistance (R_{SD}) extracted by plotting R_{CH} versus L_G , where R_{CH} represents the total channel resistance measured from devices with various gate lengths under gate bias from 2.5 V to 4 V. R_{SD} is determined to be 2.5 Ω -mm, which can be further reduced by optimizing the processes of ion implantation and

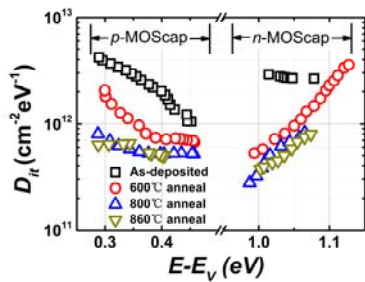


Fig. 4. D_{it} distribution in GaAs band gap obtained on p-type and n-type capacitors with $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ interface. The values are obtained by the conductance method at room temperature.

S/D contact fabrication. The ΔL , defined as the difference between mask gate length (L_G) and L_{eff} , is estimated to be ~ 0.2 μm , due to the lateral dopant diffusion caused by high temperature activation and/or the photolithographic misalignment. As shown in Fig. 2(d), the maximum intrinsic transconductance (G_m) of the $L_G = 0.5$ μm GaAs NMOSFET is ~ 210 mS/mm after subtracting $R_{\text{SD}}/2$, whereas the maximum extrinsic G_m is ~ 138 mS/mm. The G_m can also be improved by reducing the thicknesses of $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ and Al_2O_3 capping layer. The equivalent oxide thickness (EOT) is about 4.5 nm.

We further investigate the thermal stability of the oxide-GaAs interface by comparing the C - V and G - V characteristics measured on samples with and without RTA treatment. Fig. 3 summarizes the C - V characteristics of n-type and p-type $\text{Ni}/\text{Al}_2\text{O}_3/\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3/\text{GaAs}(111)\text{A}$ MOS capacitors. The annealing treatments at 600 $^\circ\text{C}$ and 800 $^\circ\text{C}$ were both performed in nitrogen ambient for 30 seconds. For the p-type C - V characteristics, the frequency dispersion at accumulation ($V_G = -3$ V) and depletion regions clearly reduced after the annealing at high temperature, which suggests that the interface trap density near the valence band edge decreases after RTA. Quantitatively, the frequency dispersions ($\Delta C/C_{\text{max}}$) from 1 kHz to 1 MHz at the gate bias of -3 V measured on as-deposited, 600 $^\circ\text{C}$ RTA and 800 $^\circ\text{C}$ RTA samples are 5%, 2.1% and 1.8%, respectively. As for the n-type C - V characteristics, the “bump” of the capacitance caused by the high density of traps in the depletion region for the as-deposited capacitors is effectively eliminated after 600 $^\circ\text{C}$ or 800 $^\circ\text{C}$ annealing. The frequency dispersion at the depletion region is also reduced by RTA.

We also used the conductance method to extract the D_{it} of the novel epitaxial interface. [14] The distributions of D_{it} in the GaAs band gap are summarized in Fig. 4. The D_{it} for both upper half and lower half band gaps of GaAs is effectively reduced by the high temperature annealing, which is consistent with the C - V data shown in Fig. 3. In the lower half of the band gap, which is close to the valence band edge, the D_{it} at the position of $E - E_V = 0.35$ eV drops from 3×10^{12} $\text{cm}^{-2}\cdot\text{eV}^{-1}$ for the unannealed sample to 5.5×10^{11} $\text{cm}^{-2}\cdot\text{eV}^{-1}$ for the 800 $^\circ\text{C}$ and 860 $^\circ\text{C}$ annealed samples. Similarly, in the upper half band gap, which is close to the conduction band edge, at the position of $E - E_V = 1.05$ eV, the D_{it} is reduced from 2.6×10^{12}

$\text{cm}^{-2}\cdot\text{eV}^{-1}$ for the unannealed sample to 7×10^{11} $\text{cm}^{-2}\cdot\text{eV}^{-1}$ for the 800 $^\circ\text{C}$ and 860 $^\circ\text{C}$ annealed samples. This significant reduction of D_{it} near the conduction band edge and also mid-gap is the key to realize high-performance surface channel GaAs NMOSFETs at epitaxial oxide/semiconductor interface.

IV. CONCLUSIONS

In summary, we have demonstrated high performance surface channel E-mode GaAs(111)A NMOSFETs with ALE $\text{La}_{1.8}\text{Y}_{0.2}\text{O}_3$ gate dielectric showing record-high drain current and sub-100 mV/dec subthreshold slope. We believe this high-quality epitaxial structure with excellent interface quality is very promising for future high-speed low-power logic and RF device applications.

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