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Chemical Vapor Deposition of Thin Film Materials for Copper Interconnects in Microelectronics

Abstract

The packing density of microelectronic devices has increased exponentially over the past four decades. Continuous enhancements in device performance and functionality have been achieved by the introduction of new materials and fabrication techniques. This thesis summarizes the thin film materials and metallization processes by chemical vapor deposition (CVD) developed during my graduate study with Professor Gordon at Harvard University. These materials and processes have the potential to build future generations of microelectronic devices with higher speeds and longer lifetimes.

Manganese Silicate Diffusion Barrier: Highly conformal, amorphous and insulating manganese silicate ($MnSi_xO_y$) layers are formed along the walls of trenches in interconnects by CVD using a manganese amidinate precursor vapor that reacts with the surfaces of the insulators. These $MnSi_xO_y$ layers are excellent barriers to diffusion of copper, oxygen and water.

Manganese Capping Layer: A selective CVD manganese capping process strengthens the interface between copper and dielectric insulators to improve the electromigration reliability of the interconnects. High selectivity is achieved by deactivating the insulator surfaces using vapors

containing reactive methylsilyl groups. Manganese at the Cu/insulator interface greatly increases the strength of adhesion between the copper and the insulator.

Bottom-up Filling of Copper and Alloy in Narrow Features: Narrow trenches, with widths narrow than 30 nm and aspect ratios up to 9:1, can be filled with copper or copper-manganese alloy in a bottom-up fashion using a surfactant-catalyzed CVD process. A conformal manganese nitride (Mn_4N) layer serves as a diffusion barrier and adhesion layer. Iodine atoms chemisorb on the Mn_4N layer and are then released to act as a catalytic surfactant on the surface of the growing copper layer to achieve void-free, bottom-up filling. Upon post-annealing, manganese in the alloy diffuses out from the copper and forms a self-aligned barrier in the surface of the insulator.

Conformal Seed Layers for Plating Through-Silicon Vias: Through-silicon vias (TSV) will speed up interconnections between chips. Conformal, smooth and continuous seed layers in TSV holes with aspect ratios greater than 25:1 can be prepared using vapor deposition techniques. Mn_4N is deposited conformally on the silica surface by CVD to provide strong adhesion at Cu/insulator interface. Conformal copper or Cu-Mn alloy seed layers are then deposited by an iodine-catalyzed direct-liquid-injection (DLI) CVD process.

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To my parents

獻給 我的父親母親

Chapter 1

Introduction

Gordon Moore, co-founder of Intel Corp., noted in his 1965 paper that the number of transistors in integrated circuits (IC) had doubled every year from the invention of the IC in 1958 until 1965 and predicted that the trend would continue for at least ten years.[1] His prediction was proven to be accurate and Moore's Law, which states that the number of transistors that can be placed inexpensively on an IC doubles approximately every two years, has been used to guide long-term planning and to set targets for research and development in the semiconductor industry for over 40 years. The periodic enhancements in IC density and performance gave rise to more powerful microelectronic devices with ever-increasing processing speed and memory capacity. Today, the impact of digital electronic devices has been witnessed on the global scale.

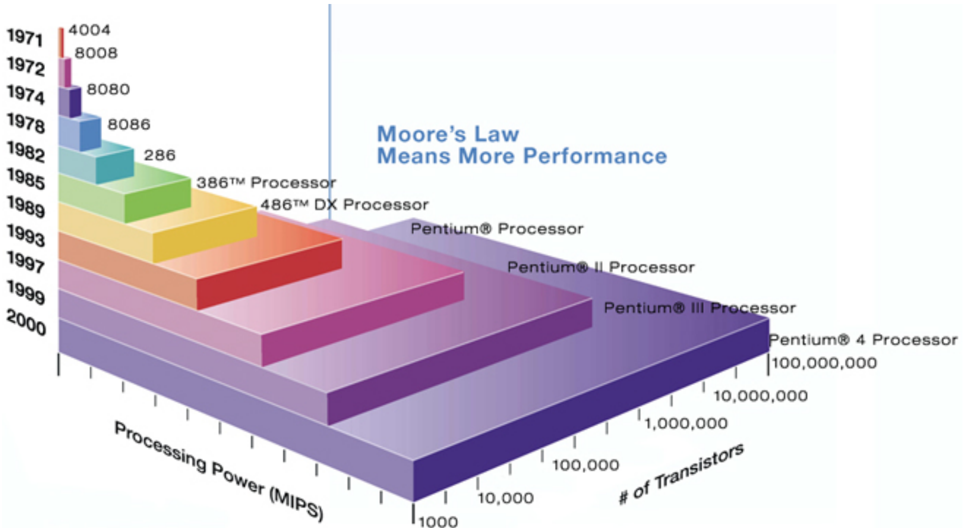

Figure 1.1 Moore's Law (Source: The Internet)

1.1 Copper Interconnects in Microelectronics

Device Scaling and RC Delay

Continuous improvements in microelectronic devices have been achieved through evolutionary device scaling. On the transistor level, device density and performance improve as the gate length, gate dielectric thickness, and junction depth of the transistors are scaled. Each new technology generation generally represents a 0.7x reduction in feature size.[2] Intel's recent generation of microprocessors, fabricated by the 32 nanometer (32 nm) technology node manufacturing process, contain over one billion transistors while the average half-pitch (half the distance between identical transistors) was approximately 32 nm.

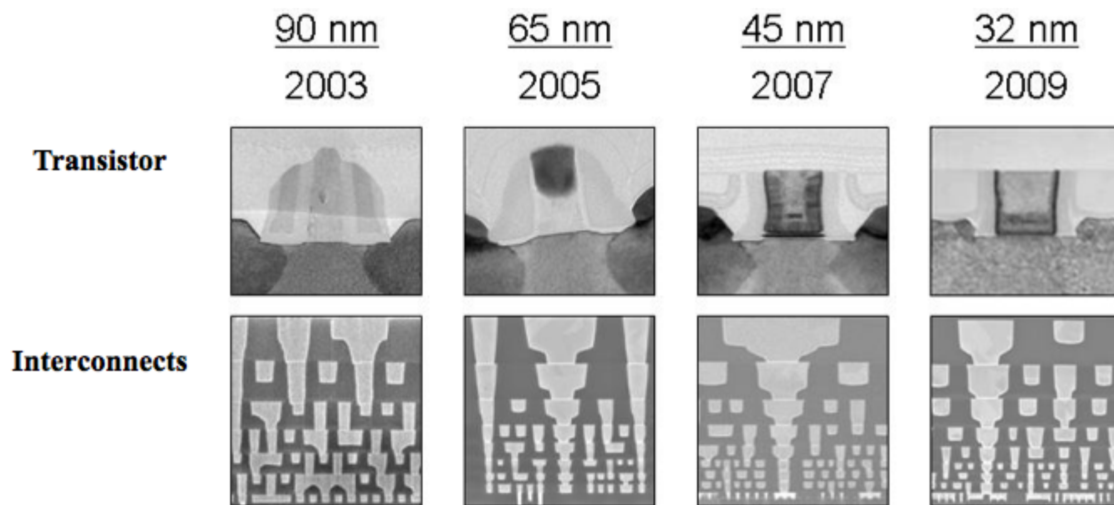

Figure 1.2 Cross-section of a transistor (top) and metal interconnects (bottom) in recent generations of processors (Source: Intel)

Transistors in microelectronics are formed in the front-end-of-line (FEOL) portion of IC fabrication. Metal wirings, also known as interconnects, are then deposited during the back-end-of-line (BEOL) portion to connect the individual transistors. Aluminum alloys were originally chosen for interconnect fabrication because of their low resistivity (3.0 – 5.0 μΩ-cm) and

relatively low production costs. As the dimension of the devices scales to increase density and clock speed of the microprocessors, scaled interconnects suffer from increased resistance due to decreased conductor cross-sectional area and may also suffer from increased capacitance.[3] The interconnect delay (RC delay), which is proportional to the product of resistance and capacitance of the interconnect structure, degrades at a rate of 2x per technology generation assuming a constant metal aspect ratio and no change in conductor (i.e. Al) or dielectric materials (i.e. SiO_2).[2] The RC delay is becoming dominant in determining the overall delay time, as shown in Figure 1.3. As a result, interconnect resistance and capacitance have become important parameters in determining IC design, packing density, and device performance. Interconnect delays must be minimized to build faster devices with lower power consumption.

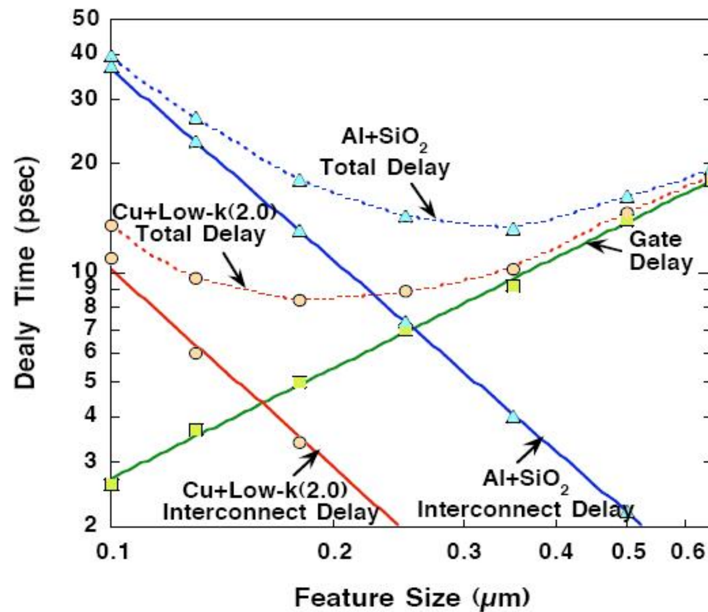

Figure 1.3 Delay times versus feature size (Source: EE 311, Stanford University)

Low-*k* Dielectric Materials

Numerous low-*k* dielectric materials, from air (k = 1) to carbon doped oxide dielectrics (k ~ 3.8), have been explored to replace silicon dioxide (SiO_2, k = 3.9) to reduce the capacitance in

the interconnect systems.[4] Insertion of the low-*k* dielectric between the metal wires results in a significant reduction in RC delay. However, only a limited number of low-*k* materials have been introduced into production due to a significant number of integration and reliability issues, including thermally and mechanically induced cracking or adhesion loss, poor mechanical strength, moisture adsorption, low electrical breakdown, and poor thermal conductivity.[5] Dielectric materials with permittivity values less than ~ 2.5 are generally achieved by introducing porosity, which further increases moisture adsorption and reduces the mechanical strength of the materials.[3]

Copper Interconnects

To lower the resistance of the metal lines, copper (Cu) was first introduced in 1997 to replace aluminum alloy metallization due to its abundance, low resistivity (1.67 μΩ-cm, Table 1.1), and better reliability against electromigration (Table 1.2).[6] Highest performance is achieved when copper and low-*k* dielectrics are combined, as evidenced by the industry trend.

Table 1.1 Resistivity of selected metals

Metal	**Bulk Resistivity** [μΩ-cm]
Ag	1.63
Cu	1.67
Au	2.35
Al	2.67
W	5.65

Table 1.2 Comparison between Al and Cu

	Al	**Cu**
Melting Point	660 °C	1083 °C
E_a for Lattice Diffusion	1.4 eV	2.2 eV
E_a for Grain Boundary Diffusion	0.4 – 0.8 eV	0.7 – 1.2 eV

While copper metallization offers significant performance improvements, it also presents several integration and reliability challenges. One major concern is that copper atoms readily ionize and penetrate into most dielectric materials and then accumulate in the dielectric as Cu^+ space charge (Figure 1.4). Contamination to silicon devices leads to increased leakage in SiO_2, increased junction leakage, and lower junction breakdown voltage.[7] As a result, copper must be encapsulated with diffusion barriers. In addition, the barrier layer must also provide adequate adhesion to both the dielectric material and the copper layers. High adhesive strength are required for copper interconnect microstructures to withstand the high residual stresses associated with thermal expansion mismatch and film growth processes, as well as the chemical mechanical planarization (CMP) process currently used in IC fabrication.[8]

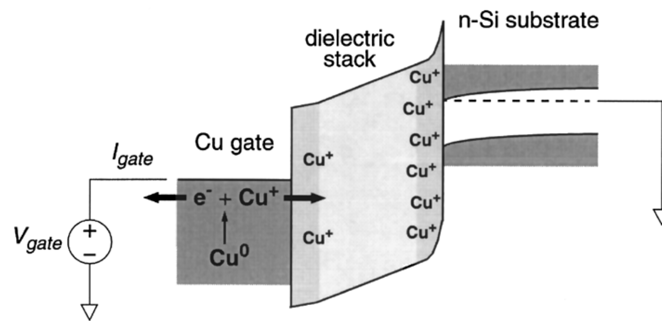

Figure 1.4 Energy band diagram illustrating Cu^+ penetration and accumulation under positive V_{gate} stress (Ref. 7)

Diffusion Barriers

Copper wires are encapsulated with diffusion barriers to prevent copper diffusion into silicon and dielectric materials under electric fields imposed during device operation (~ 1×10^5 V/cm).[3] The barrier materials are generally refractory metals or refractory metal nitrides.[6] Early studies used titanium (Ti), a highly reducing metal that binds strongly to oxygen, and titanium nitride (TiN) as barrier materials, but most companies in the industry have now settled on using

tantalum-based materials, such as tantalum metal (Ta) and tantalum nitride (TaN), as the diffusion barriers.[9,10] A list of various barriers for copper from previous studies and a comparison of tantalum- and titanium-based barriers are discussed in Reference 11.

Copper resistivity has been projected to increase dramatically with smaller feature size due to electron scattering from grain boundaries and conductor walls.[12] Although the resistivity of copper is greatly lower than that of aluminum alloys, the effective resistance of the copper line is determined by the actual cross-section of the line. As a result, diffusion barriers should be as thin as possible and those with high resistivity should be avoided. An ideal diffusion barrier must be free of defects, smooth, continuous, and conformal at minimal thickness. The barrier should also provide good adhesion strength and show no interaction with dielectric insulators and the copper seed layer. A dense, amorphous barrier is usually preferred to avoid fast diffusion path for copper, such as grain boundaries.[6]

Seed Layers

Copper interconnects are built by electroplating copper in the open trenches in the patterned insulator layer.[13] Electroplating is typically carried out in a bath that contains copper sulfate ($CuSO_4$) electrolytes and other additives (accelerators, suppressors, etc.) to achieve consistent fill and to improve film quality. The electroplating method allows low process temperature, high deposition rates, and complete via- and trench-filling capabilities. Most plating techniques require a thin seed layer as an electrode. These seed layers must have low resistivity, conformal step coverage, smooth surface morphology, and strong adhesion to the underlying barrier layer. If the seed coverage is discontinuous, then feature fill during copper electroplating becomes difficult and voids will typically be observed along the feature sidewalls.[6]

The Damascene Process

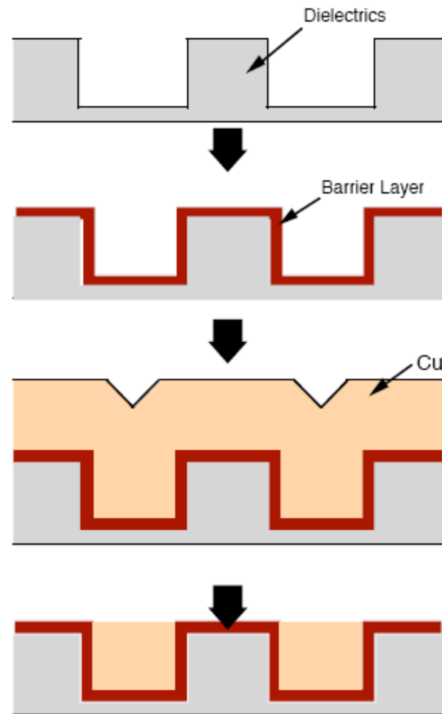

Figure 1.5 A typical damascene process (Source: The Internet)

The damascene process[13] is adopted by the semiconductor industry to fabricate copper interconnects. The most common process integration steps to form copper interconnects are: (1) deposit the damascene or dual damascene interlevel or intermetal dielectric materials, (2) pattern and etch the damascene or dual damascene structure into the dielectrics, (3) deposit a barrier/seed stack and fill the openings with electrodeposited copper, (4) anneal the wafers to stabilize the microstructure, (5) polish the excess copper and barrier away using CMP (Figure 1.5). Steps 1 through 5 are repeated for multi-layered interconnects. The final copper layer is then passivated and prepared for packaging and assembly.

Electromigration Reliability

Electromigration is a reliability problem in which metal atoms move in the direction of the current flow due to momentum transfer. J. R. Black developed an empirical model in the 1960's to estimate the mean time to failure (*MTTF*) of a metal wire, taking electromigration into consideration:

$$MTTF = AJ^{-n}e^{\frac{\Delta H}{kT}} \tag{1.1}$$

where A is a constant based on the cross-sectional area of the interconnect, J is the current density, ΔH is the electromigration activation energy, k is the Boltzmann's constant, T is the temperature, and n a scaling factor.[14] It is clear that electromigration is becoming a major concern due to the aggressive scaling of interconnect dimensions and the ever-increasing current densities at operation. Compared to aluminum interconnects, copper interconnects are more robust against electromigration failure due to stronger Cu-Cu bond and higher melting temperature relative to that of aluminum.[15] The mass transport mechanism of copper electromigration, unlike that of aluminum electromigration, is almost exclusively interfacial or surface diffusion. As a result, copper electromigration is more a function of the nature of the interfaces available for mass transport.[16] In today's copper damascene processes, copper wires are typically protected by a liner to prevent diffusion through the intralevel dielectric. Unfortunately, the CMP process does not allow protection of the top copper surface by a liner. Therefore, the chemical-mechanical polished surface, which is usually covered with a dielectric capping layer, is the fast diffusion path.[16]

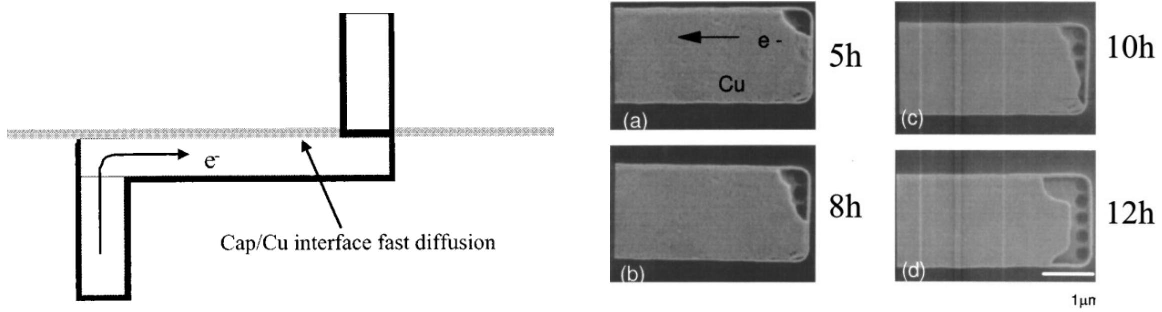

Figure 1.6 Schematic of a Cu interconnect showing the Cu/capping layer interface is the fast diffusion path in an electromigration test (left), SEM showing copper electromigration during the test (right) (Ref. 16)

Lane *et al.* demonstrated that the adhesion strength at the Cu/capping layer interface is directly correlated to the electromigration lifetime of copper conductors (Figure 1.7).[16] As a result, capping and liner materials must be carefully chosen and adhesion at Cu/capping layer interface must be improved to achieve better electromigration reliability and longer lifetime.

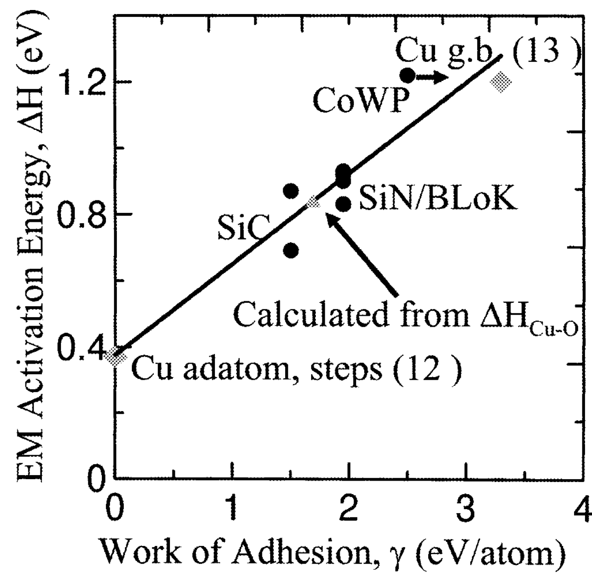

Figure 1.7 Electromigration activation energy as a function of the work of adhesion at Cu/capping layer interfaces (Ref. 16)

1.2 Deposition Techniques

Microfabrication is a highly complex collection of technologies that is used to make microelectronic devices. Over 1000 steps, in which the first 500 steps belong to the FEOL portion and the next 500 steps belong to the BEOL portion, are involved in building today's microprocessors. Thin film deposition is the most ubiquitous and critical of the processes used to manufacture microelectronic devices, and the deposition techniques typically fall into two broad categories: physical vapor deposition and chemical vapor deposition.

Physical Vapor Deposition (PVD)

The two physically based methods for depositing thin films are evaporation and sputtering. They are called physical vapor deposition processes because these techniques do not involve chemical reactions. The vapors of the material to be deposited are produced either by heating or by energetic ion bombardment.

The metal layers for all of the early generations of semiconductor technologies were deposited by evaporation. In an evaporator, the wafers are loaded into a high-vacuum chamber that is commonly pumped with a cryopump. The material to be deposited is loaded into a crucible and is heated by an embedded resistance heater and an external power supply. Since the pressure inside the chamber is very low ($< 10^{-5}$ Torr), vapors of the material travel across the chamber in a straight line until they strike the substrate surface, where they accumulate and form a film.[17] A mechanical shutter is typically used in front of the container to start and stop the deposition abruptly. There are two basic types of crucible heating systems: resistive heating and electron-beam heating.

Sputtering has the ability to achieve better step coverage and to produce well-controlled layers of compound materials and alloys than evaporation techniques. In a sputtering system, the plasma chamber is arranged so that high-energy ions strike the target that contains the material to be deposited. Because of the higher pressure (~ 10^{-3} Torr) in sputtering systems, the atoms experience more gas-phase collisions and produce films with higher conformality. Due to the physical nature of the process, sputtering can be used to deposit a wide variety of materials. DC sputtering is usually favored while depositing elemental metals due to its high sputter rates. RF plasma is used to deposit insulting materials such as SiO_2.[17] Sputtering is now the primary technique used to deposit diffusion barrier (TaN, TiN), adhesion layer (Ta, Ti), and seed layer (Cu) in copper interconnect systems.

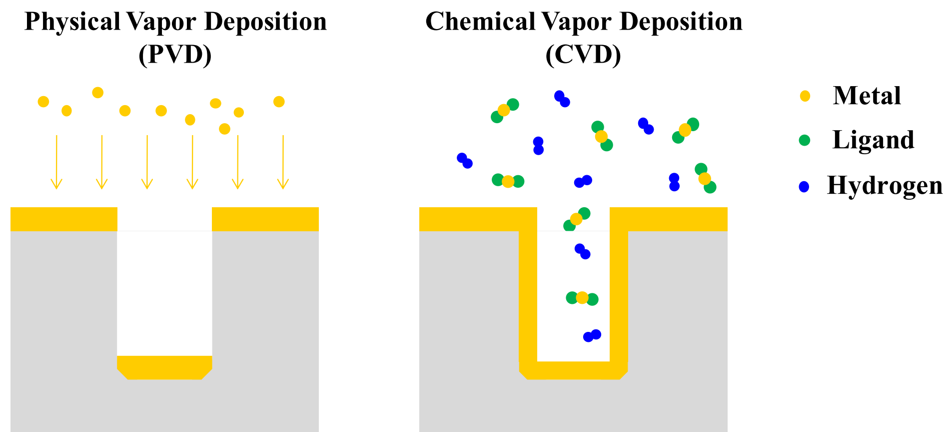

Figure 1.8 Schematic diagrams of physical vapor deposition and chemical vapor deposition

Chemical Vapor Deposition (CVD)

Although most metal films for silicon ICs are deposited using physical vapor deposition methods, they have major problems associated with step coverage. This is a particular concern with future technologies where very small, high aspect ratio features require conformal step

coverage. Chemical vapor deposition has the best ability to achieve conformal step coverage and produces the least substrate damage. [17]

Chemical vapor deposition is the process of chemically reacting a volatile compound of a material to be deposited, with other gases, to produce a nonvolatile solid that deposits atomistically on a substrate. CVD methods have been used to produce a variety of films and coatings of metals, semiconductors, and insulators with desirable electrical, optical, and mechanical properties. [18] CVD processes are often chosen over other vacuum deposition techniques for their affordable equipment cost and operating expenses, suitability for both batch and semi-continuous operation, and compatibility with other processing steps. Other advantages of CVD processes include the ability to achieve surface-selective deposition and to coat or super-fill high aspect ratio 3-dimensional structures. These features will be highlighted in the following chapters. Many variants of CVD processing, including atmospheric pressure (APCVD), low-pressure (LPCVD), and plasma-enhanced (PECVD), have been researched and developed. Metalorganic CVD (MOCVD) is now widely used to grow epitaxial compound semiconductor, dielectrics insulators, and metal films. While other CVD process variants are differentiated physically on the basis of pressure or use of plasmas, MOCVD is distinguished by the chemical nature of the precursor gases. One advantage of metalorganics is their generally high volatility at moderately low temperatures. Carbon contamination of film, however, is a major disadvantage. [18]

The fundamental sequential steps that occur in a typical CVD process include: (1) convective and diffusive transport of reactants from the gas inlets to the reaction zone, (2) transport of the initial reactants and their products to the substrate surface, (3) adsorption (chemical and physical) and diffusion of these species on the substrate surface, (4) heterogeneous reactions catalyzed by the surface leading to film formation, (5) desorption of the volatile by-

products of surface reactions, and (6) convective and diffusive transport of the reaction by-products away from the reaction zone.

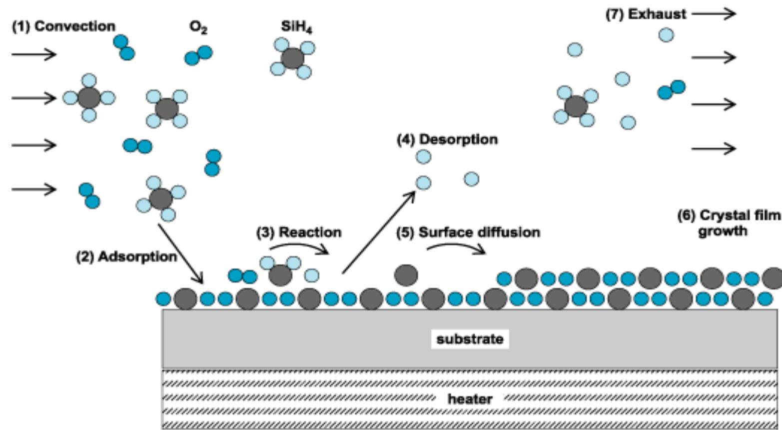

Figure 1.9 Sequence of transport and reaction processes during CVD SiO_2 film growth

(Source: The Internet)

First Order Model of Deposition

A first order model of is presented here to better understand the process of chemical vapor deposition.[17]

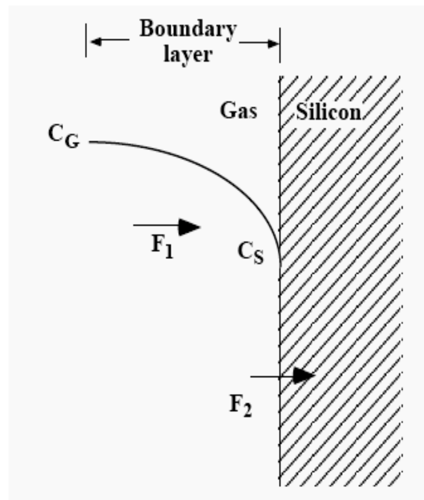

Figure 1.10 Mass transfer of reactants (F_1) and surface reaction (F_2) during a CVD process

(Source: ES 174, Harvard University)

Mass transfer of reactants through the boundary layer is one of the two most important steps that determine the overall growth rate. F_1 denotes the flux of the mass transfer of reactants and can be described as:

$$F_1 = h_G\left(C_G - C_S\right) \tag{1.2}$$

where h_G is the mass transfer coefficient, C_G is the concentration of the reactant in main gas flow, and C_S is the concentration of the reactant at wafer surface. The other important step in determining the growth rate is the surface reaction step. The flux, F_2, can be described as:

$$F_2 = k_S C_S \tag{1.3}$$

where k_S is the chemical surface reaction rate. At steady-state, the two processes act in series and must be equal to each other, $F_1 = F_2$, so:

$$C_S = C_G\left(\frac{h_G}{k_S + h_G}\right) \tag{1.4}$$

The film deposition rate is given by:

$$v = \frac{F}{N} = \frac{k_S h_G}{k_S + h_G}\frac{C_G}{N} \tag{1.5}$$

where N is the number of atoms per unit volume incorporated into the film. From Equation 1.5, it is clear that the deposition rate is determined by the smaller of k_S or h_G, therefore leading to two limiting cases:

1. If $k_s << h_G$, then:

$$v \approx k_S \frac{C_G}{N} \tag{1.6}$$

This is called the surface reaction-controlled regime. When deposition occurs in this regime (usually at lower temperatures), the deposition process is very sensitive to temperature as the surface reaction rate constant obeys the Arrhenius equation:

$$k_S = k_0 e^{-E_a/kT} \tag{1.7}$$

2. If $k_s >> h_G$, then:

$$v \approx h_G \frac{C_G}{N} \tag{1.8}$$

This is called the mass transfer-controlled regime. When deposition occurs in this regime (usually at higher temperatures), the deposition rates depend primarily on mass transfer, or the gas phase diffusion, of the reactants and are relatively insensitive to temperature. C_S in this case approaches zero because the reactants are used up at the surface as soon as they arrive. Figure 1.11 summarizes the temperature dependence of the deposition rates of CVD processes.

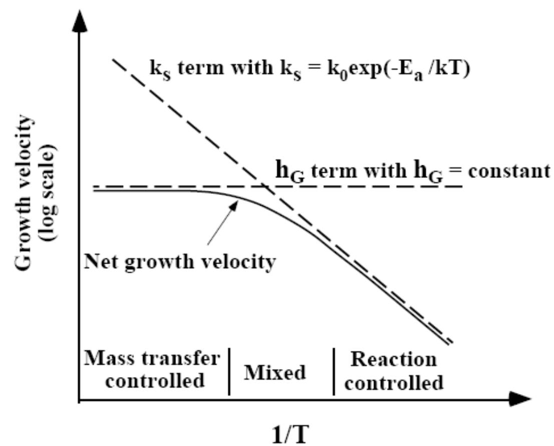

Figure 1.11 Temperature dependence of CVD growth velocities (Source: ES 174, Harvard University)

1.3 Characterization of Thin Films

Characterization techniques are crucial to the development of thin film science and technology. Information about various structural and chemical properties can be evaluated by modern analytical techniques with high levels of precision and accuracy. A list of modern techniques employed in the characterization of thin film materials in this thesis is shown in Table 1.3.

Table 1.3 Analytical techniques employed in thin film science and technology (Ref. 18)

Primary beam	**Energy range**	**Secondary signal**	**Technique**	**Application**
Electron	0.3 – 30 keV	Electron	Scanning electron microscopy (SEM)	Surface morphology
	100 – 400 keV	Electron	Transmission electron microscopy (TEM)	High-resolution structure
	1 – 30 keV	X-ray	Energy-dispersive X-ray spectroscopy (EDX)	Surface region composition
	100 – 400 keV	Electron	Electron energy loss spectroscopy (EELS)	Local small-area composition
Ion	1 – 15 keV	Ion	Secondary ion mass spectrometry (SIMS)	Trace composition *vs.* depth
	> 1 MeV	Ion	Rutherford backscattering spectrometry (RBS)	Composition *vs.* depth
Photon	> 1 keV	Electron	X-ray photoelectron spectroscopy (XPS)	Surface composition
	> 1 keV	X-ray	X-ray fluorescence (XRF)	Composition
	> 1 keV	X-ray	X-ray diffraction (XRD)	Crystal structure

Thickness and Structural Characterization

Thickness, refractive index, and other optical properties of dielectric thin films are typically measured by ellipsometry. Ellipsometry is an optical technique that measures the change of polarization state of a linearly polarized light beam upon reflection or transmission at the surface of a film. Surface morphology of the thin films can be evaluated using an atomic force microscope (AFM). AFM consists of a microscale cantilever with a sharp tip that is used to

scan the specimen surface. When the tip is brought into proximity of a sample surface, forces between the tip and the sample lead to a deflection of the cantilever according to Hooke's law, the deflection is then measured using a laser spot reflected from the top surface of the cantilever.

Scanning electron microscope (SEM) is used to analyze surface morphology and step coverage of the thin films in high aspect ratio (AR) features. SEM is a powerful, perhaps the most widely employed, imaging tool with high resolution (~ 10 nm) and element-dependent contrast. Sample preparation for top-view and cross-section analyses is straightforward. SEM detects the intensity of the backscattered electrons or secondary electrons produced from interaction of the high-energy electron beam with the atoms at or near the surface of the sample, producing images that contain information about the sample's surface topography, composition, and electrical conductivity.

Transmission electron microscope (TEM) transmits a high-energy focused beam of electrons through an ultra-thin specimen that is transparent to electrons. An image is formed from the interaction of the electrons transmitted through the specimen and is magnified and focused onto an imaging device. The resolution of the TEM is about an order of magnitude better than that of the SEM. TEM is used to obtain structural information of specimens. Cross-sectional TEM samples can be prepared by two different methods. The first method sandwiches two pieces of the same sample together and the center of the sample is thinned down to a few hundred microns using a mechanical polishing method. The thinned sample is then ion-milled to a desired thickness of 10 – 50 nm. The second method is a lift-out method using a focused ion beam (FIB). The area of interest is first covered by a protective coating (typically platinum, tungsten, or carbon). A wedge is then milled by the FIB and the lamella is lifted out from its hole using an AutoProbe®. Next, the wedge is welded to the top of the TEM grid post by depositing

platinum or tungsten. The wedge is thinned to about 1.5 micron with a current < 300 pA and to the desired thickness using a lower current (20 – 40 pA).

Chemical Characterization

Energy-dispersive X-ray spectroscopy (EDX), X-ray photoelectron spectroscopy (XPS), Rutherford backscattering spectroscopy (RBS), and secondary ion mass spectrometry (SIMS) are useful techniques for elemental analysis or chemical characterization of the thin film samples.

EDX uses a high-energy incident beam to excite and eject an electron in an inner shell of the atoms in a sample, which creates a hole that is then filled by an electron from an outer shell. The difference in energy between the energy shells is released in the form of an X-ray, which is characteristic of the material, and is measured by an energy-dispersive spectrometer.

XPS measures the elemental composition, empirical formula, chemical state, and electronic state of the elements within a material. The sample is analyzed by irradiating of a beam of X-ray while simultaneously measuring the kinetic energy and number of electrons that escape from the top 1 – 10 nm of the material being analyzed. Because the energy of a particular X-ray wavelength (E_{photon}) is known, the electron binding energy ($E_{binding}$) of each of the emitted electrons can be determined by:

$$E_{binding} = E_{photon} - (E_{kinetic} + \phi) \qquad (1.9)$$

where $E_{kinetic}$ is the kinetic energy of the electron measured by the instrument, and ϕ is the work function of the spectrometer.

RBS is used to determine the structure and composition of materials by measuring the backscattering of a beam of high-energy ions impinging on a sample. Rutherford backscattering

can be described as an elastic collision between a high kinetic energy particle from the incident beam (the projectile) and a stationary particle located in the sample (the target). Considering the conservation of momentum and kinetic energy, the energy of the scattered projectile (E_1) is reduced from the initial energy (E_0):

$$E_1 = kE_0 \tag{1.10}$$

where k is the kinematical factor:

$$k = \left(\frac{m_1 \cos\theta_1 \pm \sqrt{m_2^2 - m_1^2 (\sin\theta_1)^2}}{m_1 + m_2} \right)^2 \tag{1.11}$$

where m_1 is the mass of the projectile, m_2 is the mass of the target nucleus, and θ_1 is the scattering angle of the projectile.

SIMS is the most sensitive surface analysis technique and is used to analyze the composition of thin films by simultaneously sputtering the surface of the sample with a focused primary ion beam and collecting and analyzing the ejected secondary ions that are then measured with a mass spectrometer.

Adhesion Test

The adhesion (debonding) energy in multi-layer thin film structures is quantitatively measured by a fracture mechanics technique called the four-point bend test. A schematic illustration of a four-point bend test sample is shown in Figure 1.12.

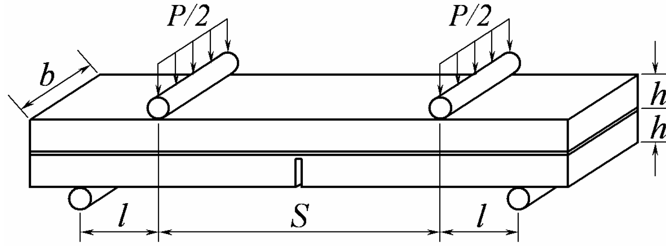

Figure 1.12 Schematic illustration of a four-point bend sample (Ref. 19)

Adhesion samples are prepared by cleaving the Si-based substrates into 12 mm x 60 mm strips. These strips are then bonded face-to-face using epoxy. Notches are made in the samples using a diamond saw. The sample is loaded at a constant displacement rate until interfacial cracks are achieved. If P is the load at which the crack propagates along the interface, then to corresponding adhesion energy (G) is: [19]

$$G = \frac{21P^2 l^2 (1-\nu^2)}{16Eb^2 h^3} \tag{1.12}$$

where E and ν are the elastic modulus and Poisson's ratio of the Si substrate, l is the distance between the inner and outer loading pins, b is the width of the specimen, and h is the wafer thickness. The four-point bend test is now used as a standard method in the semiconductor industry for determining interfacial adhesion energy.

More detailed discussions on thin film deposition techniques, film growth mechanisms, and characterization methods can be found in Referenecs 18 and 20.

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Chapter 2

Chemical Vapor Deposition (CVD) of Manganese Silicate ($MnSi_xO_y$) Diffusion Barrier

2.1 Introduction

Copper (Cu) is now becoming the standard material for connecting transistors in microelectronic devices. However, transistors cannot function properly if copper diffuses into them. Diffused copper may also reduce the resistance of the insulating material between the metal wires. For these reasons, copper must be confined inside diffusion barriers. In addition, barriers to oxygen and water are desired to separate copper from oxidants in the environment and to prevent oxidation. Sputtered tantalum nitride (TaN) diffusion barriers are currently used in the semiconductor industry. Although TaN is an effective diffusion barrier, copper does not adhere strongly to TaN. As a result, tantalum (Ta) metal, which adheres much stronger to copper metal, is sputtered on top of the TaN barrier as an adhesion layer to enhance the durability of interconnect structures. Following Ta deposition, a thin copper seed layer is sputtered and the trenches and holes are filled with electroplated copper.

As the dimensions of microelectronic circuits are being reduced, the non-conformal nature of sputtered barrier (TaN), adhesion (Ta) and seed (Cu) layers has caused problems. These layers tend to be thicker near the top openings, so that the remaining openings are narrower at the top than the bottom of the features. Electroplating copper in these features can cause formation of voids, which can later lead to failure of the interconnections. Another challenge arises from the roughness on the sidewalls of the features, which may prevent deposition on recessed regions

that are shielded from the line of sight to the sputtering target. If the barrier layer is missing in these areas, copper may diffuse out through these holes contaminate the underlying layers. If the adhesion layer is missing, the reliability of the interconnect system may be affected due to reduced adhesion between copper and the barrier. If the seed layer is missing, copper electroplating will not take place on the oxidized surface of the exposed underlying layer, producing voids in the copper. Therefore, there is a need for methods that can produce highly conformal diffusion barriers, adhesion layers, and seed layers in the interconnect system. CVD and atomic layer deposition (ALD) are methods that can potentially achieve such high conformality.[1]

One other problem with current technology is that both TaN and Ta have much higher resistivity values than copper. Thus by displacing copper metal, these layers increase the overall resistance of interconnects. The RC delay time increases with the resistance of the system, and therefore the volume of barrier material should be minimized in order to form the fastest circuits. Ideally, a barrier should not occupy any of the volume reserved for copper. Such a "zero-thickness barrier" can be realized by sputtering a manganese-copper alloy, from which manganese diffuses into the surface of silica insulator at 450 °C.[2,3] The resulting self-aligned barrier layer of amorphous manganese silicate ($MnSi_xO_y$), just a few nanometers thick, remains part of the insulator surface, whose dimensions are not significantly changed by in-diffusion of the manganese. The resulting interconnects have lower resistance than ones made with conventional TaN barriers, and have proven to be even more durable.[4,5]

The self-aligned $MnSi_xO_y$ barriers are formed by sputtering Mn-Cu alloy, therefore, they are still subject to the conformality problems of sputtered barriers. Voids in electroplated copper may form under overhangs near the tops of features or inside rough areas on the sidewalls. In this

chapter, a new way to make conformal self-aligned $MnSi_xO_y$ barriers using CVD of manganese metal is proposed. Vapors of a manganese compound react with silica surfaces to form a thin amorphous layer of manganese silicate mainly within the surface of the silica. The $MnSi_xO_y$ layer is found to be an excellent barrier against diffusion of copper, O_2 and H_2O. CVD Mn also greatly increases the adhesion of copper to capping layers of SiCNOH. The layer is completely conformal inside the surfaces of holes and trenches.

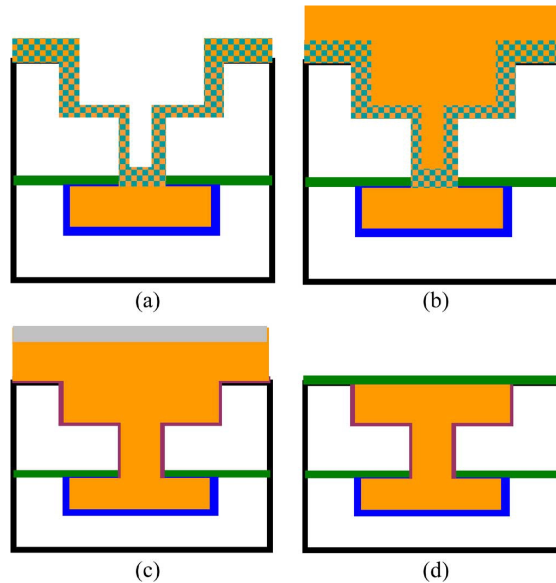

Figure 2.1 Schematics of the fabrication process for Cu dual-damascene interconnects with self-formed $MnSi_xO_y$ barrier layer. (a) Deposition of CuMn seed layer by sputtering, (b) Cu deposition by electroplating, (c) Annealing for $MnSi_xO_y$ layer, (d) Removal of excess Cu and Mn by CMP and deposition of dielectric capping layer (Ref. 4)

2.2 Experiments

Metal Amidinate Precursors

The compound that serves as a precursor for manganese is called bis(*N,N'*-diisopropylpropionamidinato) manganese(II). The compound was synthesized by methods

similar to those described in Reference 6 (Figure 2.2). It is a pale yellow crystalline solid that melts at about 60 °C to a clear liquid.

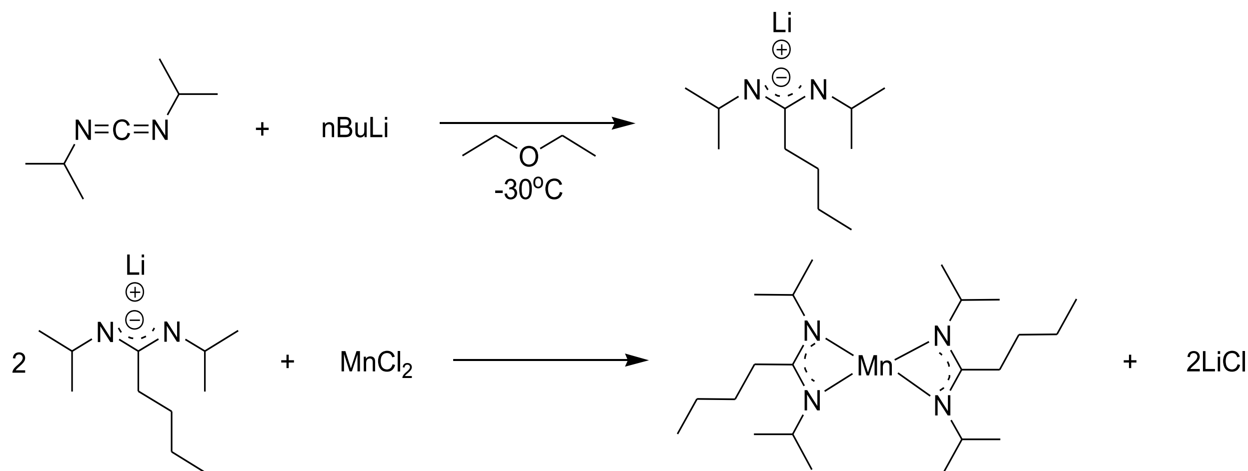

Figure 2.2 Synthesis of manganese (II) amidinate

CVD and ALD precursors need to be highly reactive toward the surfaces of substrates and also to the surface prepared by a complementary precursor such as H_2O, NH_3, or H_2. These compounds must also be volatile and thermally stable at growth temperatures, and preferably the reaction byproducts should be nonreactive and noncorrosive. CVD precursor chemistry has been dominated by halides, alkoxides, β-diketonates, alkyls, and cyclopentadienyl derivatives.[6] Alkylamide precursors have attracted more attention in recent years because these compounds do not have M-C bonds, resulting in minimal carbon incorporation in the deposited films, and the low M-N bond strengths as compared to the M-Cl and M-O bonds allowed deposition at relatively low temperatures.[7] These amide derivatives produce no corrosive byproducts, unlike metal halides. Metal amidinates are alternatives to alkylamides. The amidinate ligand can be tuned by substitution of the alkyl groups to be bulky enough to limit oligomerization and therefore increase the volatility of metal amidinate compounds. The bidentate chelating effect, on the other hand, should increase the thermal stability of resulting metal compounds.[6]

CVD Reactor Setup and Characterization Methods

For the CVD experiments, the manganese precursor was evaporated from the liquid in a bubbler at a temperature of 90 °C into a 60 sccm flow of highly purified nitrogen (concentrations of water and oxygen less than 10^{-9} of the N_2). The manganese precursor would react immediately with oxygen or water to form a black material when it is exposed to air. The vapor pressure of the precursor is estimated to be around 0.1 mbar at 90 °C.

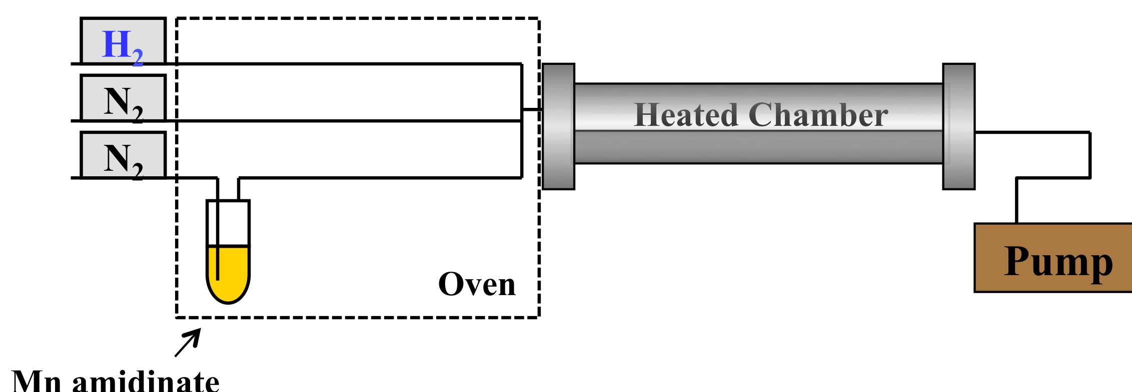

Figure 2.3 Schematic diagram of the CVD system

The substrates of silica were either thermally oxidized silicon or silica deposited by ALD. The CVD process was carried out in a hot-wall tube reactor (diameter 36 mm) within a tube furnace at temperatures between 200 and 400 °C and a total pressure of about 5 Torr. The amount of manganese deposited was measured by Rutherford backscattering spectroscopy (RBS). The $MnSi_xO_y$ formation was evaluated by cross-sectional high-resolution transmission electron microscopy (HRTEM). The effectiveness of the $MnSi_xO_y$ as a barrier to diffusion of copper was tested in four ways: (1) optical appearance, (2) sheet resistance, (3) copper silicide formation, and (4) capacitance-voltage (CV) analysis of capacitors. For copper diffusion tests, 8 nm of SiO_2 were grown on HF-etched silicon wafers by ALD at 250 °C, followed by CVD Mn at 350 °C for

10 min, which formed 2.3 nm of manganese metal. Control samples of SiO_2 omitted the CVD Mn treatment. Then copper layers with thicknesses around 200 nm were deposited on top of the CVD $MnSi_xO_y$ or SiO_2 layers. Post-deposition annealing treatments were carried out at temperatures of 400, 450, and 500 °C for one hour in a pure nitrogen atmosphere. For CV analysis, CVD Mn layer is deposited on 300 nm thermal SiO_2 on Si. Copper pads (500 μm diameter circle) were thermally evaporated using a shadow mask. CV characteristics of the metal-oxide-semiconductor (MOS) structure were measured with a HP 4275A meter in a shielded probe station at room temperature. The copper pad samples were used for Bias-Temperature Stress (BTS) test that was conducted at 250 °C under 1 MV/cm bias condition in Ar ambient. CV was then measured at room temperature after the stress treatment.

2.3 Results and Discussion

Formation of Manganese Silicate ($MnSi_xO_y$)

Thin manganese layers (2.3 nm) deposited on SiO_2 did not contribute to any conductivity by 4-point probe (> 10^6 ohm/square). Since manganese metal may be oxidized when the sample was taken out into the air for measurement, it is not clear from this measurement whether the CVD process had deposited manganese metal or some insulating manganese compound. To confirm manganese metal deposition, CVD was carried out on 50 nm of Cu film that had been evaporated onto SiO_2/Si substrates. The resulting structure was examined by cross-sectional HRTEM. Figure 2.4 shows that the manganese metal had diffused through the thin copper layer and reacted with the SiO_2 to form an amorphous manganese silicate ($MnSi_xO_y$) layer, with thickness about 2 – 5 nm, between copper and SiO_2. The $MnSi_xO_y$ layer is thicker near grain

boundaries in the copper, along which manganese diffusion is faster. This result is an evidence of manganese metal deposition.

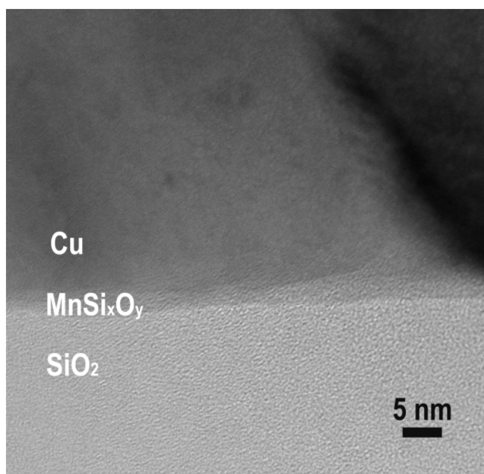

Figure 2.4 Cross-sectional HRTEM of CVD Mn on PVD Cu/SiO_2

Copper Diffusion Barrier Tests

The effectiveness of $MnSi_xO_y$ as a copper diffusion barrier was evaluated using a sample structure PVD Cu (200 nm)/CVD Mn (2.3 nm)/ALD SiO_2 (8 nm)/Si. A $MnSi_xO_y$ layer was formed between the copper and ALD SiO_2 layers. The shiny copper color and sheet resistances of these samples were unchanged by anneals in nitrogen at 400 or 450 °C. After a 500 °C anneal, the control sample, which did not have any $MnSi_xO_y$ layer, turned black and its sheet resistance increased by a factor of 200 as a result of massive copper diffusion through the thin ALD SiO_2 into the silicon. The sample treated with CVD of manganese, by contrast, retained its shiny copper color and increased its resistance only slightly.

To further analyze the diffusion of copper, the remaining copper layers were dissolved in nitric acid and the manganese silicate and silica layers were removed by dilute HF. The etched surfaces were then analyzed by an energy-dispersive X-ray spectrometer (EDX) and scanning

electron microscope (SEM). Figure 2.5 shows the SEM results after a 500 °C anneal for 1 hour. The few Cu-containing spots appeared to be copper silicide crystallites oriented by the crystal directions of the silicon. The surface of the control sample was covered by copper silicide. The control sample showed a large Cu signal in EDX analysis that was even stronger than the silicon signal, indicating that the thin ALD SiO_2 allowed copper diffusion. The CVD Mn-treated samples did not show copper by large-area EDX. A few small areas of the SEM image did show some copper by EDX, indicating some localized breakdown of the $MnSi_xO_y$ barrier at 500 °C. These spots might arise from dust or other defects in the films, which were not processed in a clean-room environment.

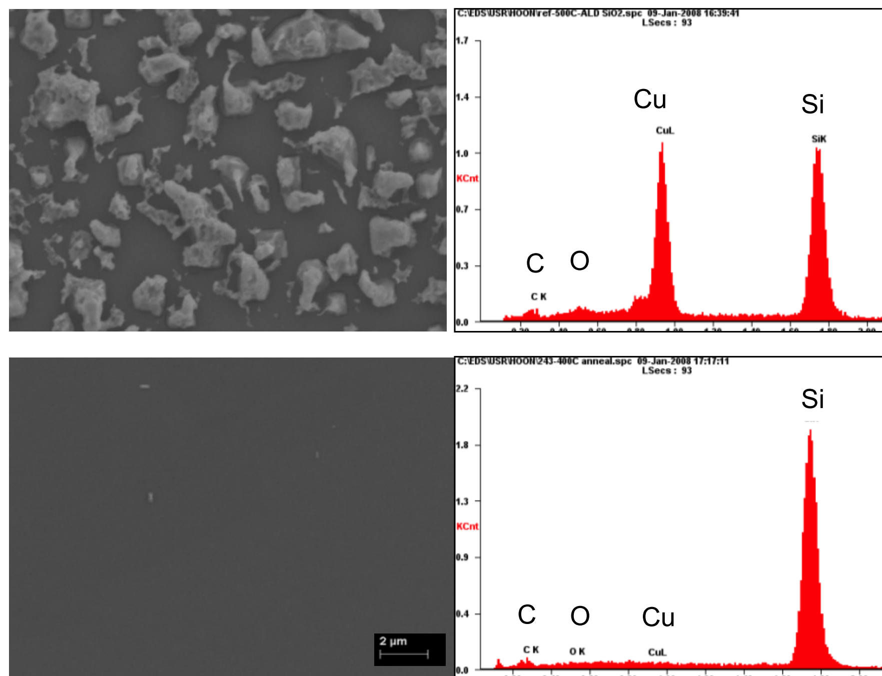

Figure 2.5 SEM and EDX of etched Si surface after annealing at 500 °C (a) with SiO_2 alone, and (b) with CVD $MnSi_xO_y$ on SiO_2

An electrical test of barrier properties was carried out by patterning the Cu into capacitor electrodes. CV curves for samples annealed at 450 °C for 1 hour are shown in Figure 2.6. The

large shift (-4.9 V) to negative voltages in the control sample was caused by positive Cu ions diffusing into the silica insulator.[8] On the other hand, the silica protected by $MnSi_xO_y$ only showed a very small shift (-0.1 V). This electrical test is more sensitive to diffusion of small amounts of copper than the other tests. These CV curves also demonstrate that the capacitance of the SiO_2 is not changed significantly by the CVD treatment. Thus, this process should be compatible with recent developments in low-*k* integration.

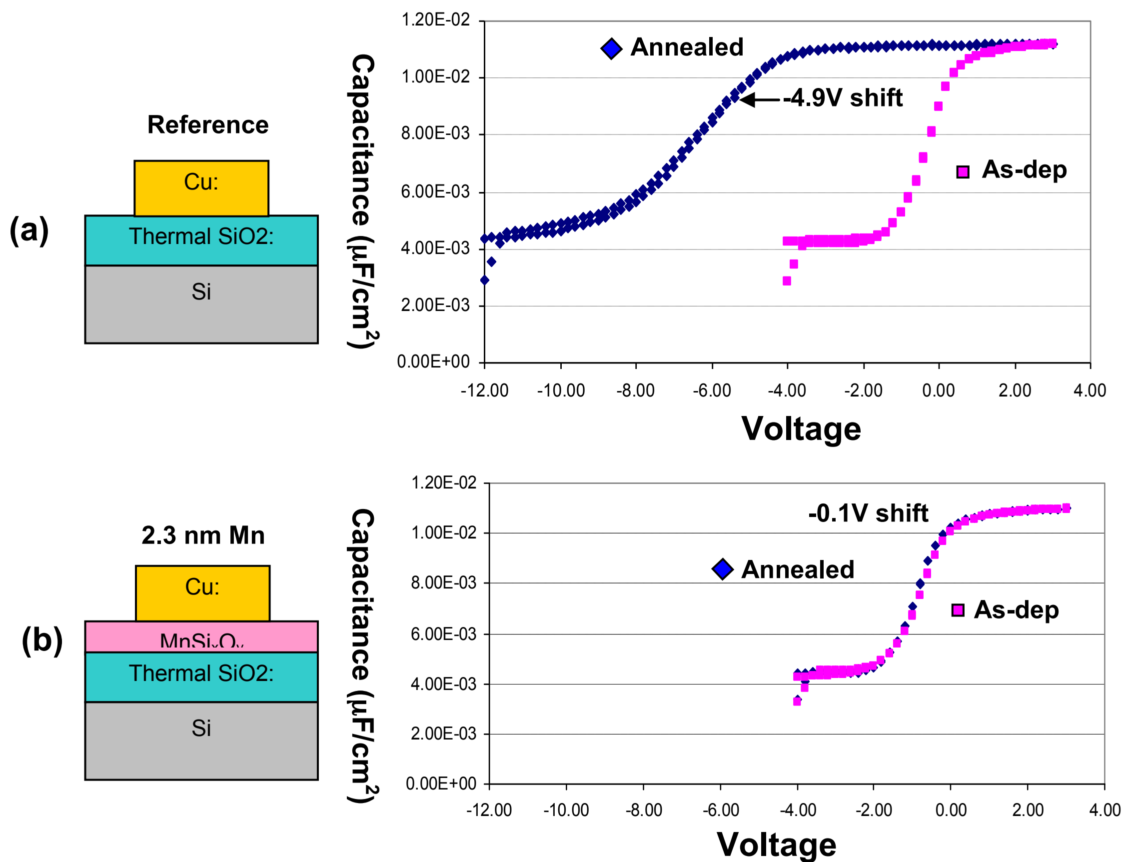

Figure 2.6 CV curves of samples before and after annealing at 400 °C (a) with SiO_2, and (b) with CVD $MnSi_xO_y$ on SiO_2

Anneals of similar capacitors were also conducted under an applied voltage of 1 MV/cm at 250 °C. Bias temperature stress (BTS) test is a more sensitive method for detection of copper

diffusion into SiO_2 because ion diffusion is accelerated by an electric field.[8] BTS condition is closer to the environment of chip operation. The control sample lost its capacitance behavior just after 2 minutes under the BTS condition, implying that a large amount of copper had diffused into the Si and the Si would no longer work as a semiconductor. In contrast, the CVD Mn-treated sample had no significant change in its CV curve (Figure 2.7). The BTS test results confirm the superior barrier properties of the $MnSi_xO_y$ layers.

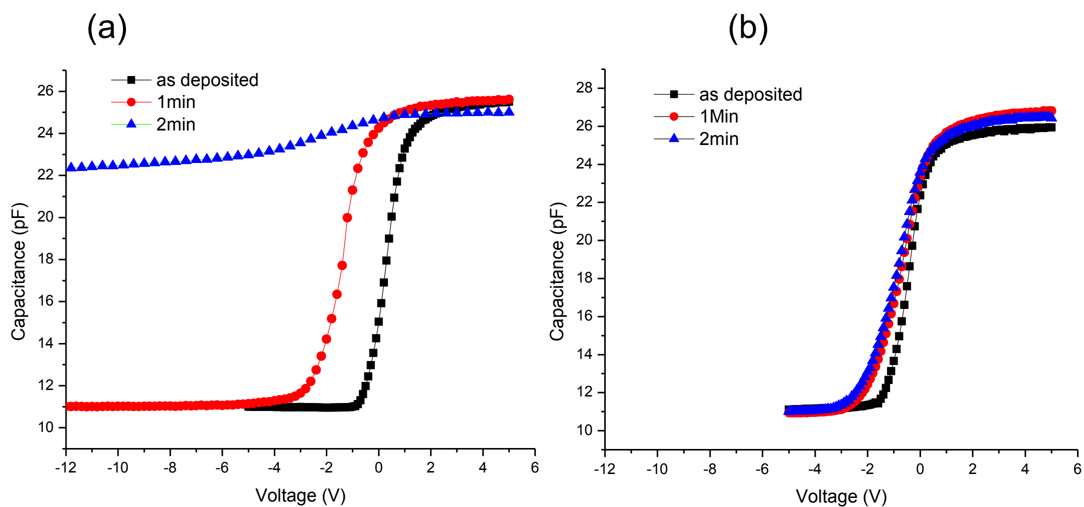

Figure 2.7 CV curves of samples before and after annealing at 250 °C under a 1 MV/cm field (a) with SiO_2, and (b) with CVD $MnSi_xO_y$ on SiO_2

Oxygen Barrier Tests

The $MnSi_xO_y$ layers were also found to be excellent barriers to oxygen and water. To test oxygen barrier properties of the manganese silicate layers, commercial low-*k* porous insulator layers from Applied Materials were coated with 8 nm of manganese silicate using methods described above, followed by 20 nm of PVD copper. The top surface of the copper was protected with 40 nm of ALD silica.[9] The sample was cut into pieces to expose the edges of the low-*k*

insulator so that oxygen or water vapor could diffuse into the low-*k* layer by the pathways shown in Figure 2.8.

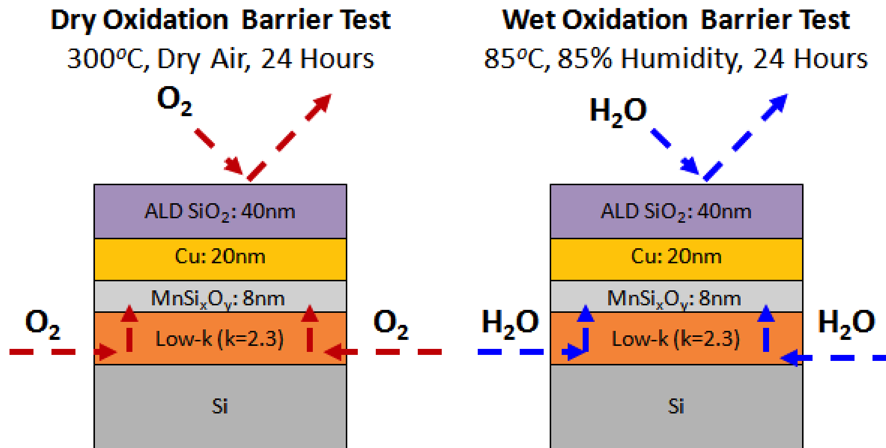

Figure 2.8 structures and pathways for tests of $MnSi_xO_y$ as an oxidation barrier

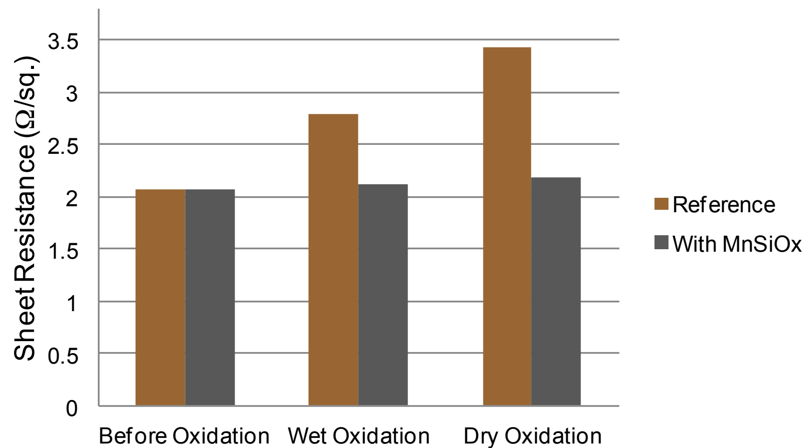

Figure 2.9 Sheet resistance of copper before and after oxidation

After exposure to dry air at 300 °C for 24 hours, the CVD Mn-treated sample maintained its shiny copper color. A control sample without the CVD manganese treatment was corroded near its edges to dark copper oxide by the same exposure. This test shows that the manganese silicate layer is a good barrier to oxygen. Similar tests in a humid atmosphere (85% humidity at 85 °C for 24 hours) showed that the manganese silicate layer is a good barrier to water vapor.

These exposures to water and oxygen also significantly increased the sheet resistance of the unprotected control copper layers, whereas the resistance of the Mn-protected copper layers remained nearly constant (Figure 2.9).

Adhesion Enhancement

The formation of the $MnSi_xO_y$ layer remarkably increased the adhesion of the Cu/SiO_2 interface, which failed the tape adhesion test prior to the CVD of manganese but easily passed after the CVD treatment. Adhesion strength was quantitatively measured by 4-point bend tests.[10] The samples were prepared by depositing manganese onto thermal SiO_2 on silicon wafers. CVD was used to form copper oxynitride (CuON) at 160 °C. CuON was then reduced to Cu metal by hydrogen plasma at room temperature.[11] The adhesion energy was found to be 10 ± 1 J m^{-2}, which exceeds the value of 5 J m^{-2} that is considered to be sufficient for making durable interconnections.[12]

The CVD manganese process can also be used to strengthen the adhesion between copper and SiCNOH, a commonly used capping layer. To test the effect of adhesion enhancement, 50 nm of copper was evaporated onto SiCNOH layers (BLoK™, Applied Materials). The Cu showed very poor adhesion, with adhesion energy less than 3 J m^{-2}. A similar Cu/SiCNOH layers were treated by CVD of Mn at 350 °C for 10 minutes. This process increased the sheet resistance from 0.5 ohms/square to 1 ohm per square because of the addition of manganese impurity in the copper. The structure was then annealed at 400 °C for 1 hour in a nitrogen atmosphere. The sheet resistance returned to 0.5 ohms per square because the manganese diffused to the surfaces or the interface. The out-diffusion of the manganese from the copper film was confirmed by SIMS analysis. After the manganese treatment, the adhesion energy was increased remarkably to values greater than 12 J m^{-2}, because manganese diffused to the interface and formed an interfacial layer.

XPS confirmed the presence of manganese at both surfaces created by delamination of the 4-point bend test sample.

This manganese metal diffusion process could be used to strengthen the bond between copper and the SiCNOH capping layers. To do this, CVD of Mn could be applied just after chemical-mechanical polishing (CMP), thereby dissolving manganese into the upper portions of the copper below its polished surface. After SiCNOH deposition, the dissolved manganese would diffuse up to the surface of the SiCNOH and strengthen its bonding to copper, which could probably increase the electromigration lifetime of the interconnects.

Because the $MnSi_xO_y$ layers are too thin to be imaged by SEM, the distribution of CVD $MnSi_xO_y$ was tested by EDX for Mn. The substrates were holes in silicon with an aspect ratio of 52:1 and a native oxide surface with which the manganese precursor reacted. The amount of manganese at the bottom of the hole was 18% of the amount at the top entrance to the hole. This result shows that the manganese precursor has a fairly slow reaction with silica surfaces at 350 °C. As a result, interconnect trenches and vias with typical aspect ratios less than 5:1 can be coated fairly uniformly with CVD $MnSi_xO_y$ at 350 °C. At lower temperatures, the surface reactions are expected to be slower, and the conformality should be even higher. Even when roughness is present on sidewalls, the CVD process should form a complete $MnSi_xO_y$ diffusion barrier without pinholes or gaps.

2.4 Conclusions

A simple CVD method is presented to make conformal self-aligned diffusion barriers of manganese silicate. This $MnSi_xO_y$ layer is an effective barrier to diffusion of copper, oxygen and water. Because the $MnSi_xO_y$ is formed within the insulator, it does not decrease the volume

available for copper, as happens with conventional Ta/TaN barriers. Also, the CVD Mn dissolves into copper surfaces, such as at the tops of vias, so no resistive barrier exists between the tops of vias and the copper in the next higher level. The CVD process can also be used to strengthen the interfacial bonding between copper and a capping barrier layer of SiCNOH. Thus, more conductive and more durable interconnections are possible using the self-aligned $MnSi_xO_y$ barriers. The CVD Mn-CuON process should allow formation of conformal seed layers for void-free electroplating of copper in even the narrowest interconnects.

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Chapter 3

Selective Chemical Vapor Deposition (CVD) of Manganese Capping Layer

3.1 Introduction

The power of computers has increased exponentially. This technological feat has been enabled by the fact that transistors improve their performance as they are scaled to smaller and smaller sizes. On the other hand, the endurance of the copper (Cu) wires that connect the transistors becomes poorer as their size is reduced. Until now, the performance of the copper wires has been sufficient to meet the industry standard lifetime of ten years. As the size of the wires is projected to become still smaller, their operational lifetime before failure would become too small.[1]

The fundamental problem is that copper metal forms rather weak bonds to metal oxides and nitrides. Adhesive tape is usually sufficient to remove copper films from these surfaces. Quantitative measurements of debonding energy by the 4-point bend test usually give values less than 1 J m^{-2}. This poor adhesion between copper and silicon nitride leads to the most common failure mechanisms of copper interconnects in integrated circuits. An open circuit can form when a copper line breaks after an electric current drives copper along the weak interface between copper and an overlying silicon nitride layer. Short circuits between neighboring lines can also form after this electromigration process extrudes copper from the channels in which it lies.[2]

Placing a metal such as cobalt on the top surface of the copper lines increases the lifetime before failure by electromigration. Cobalt (Co) or cobalt alloys with tungsten and phosphorus or

boron have been placed on copper lines by electroless plating.[3] However, avoiding some metal plating on adjacent insulator surfaces has been difficult to achieve, resulting in higher leakage and/or short circuits between lines. CVD has also been used to deposit Co on Cu lines, but some Co is also deposited on the insulator surfaces, potentially reducing reliability because cobalt on the dielectric can increase leakage and lower breakdown voltage.[4] Cobalt also diffuses from the capping layer into the Cu, increasing its resistance,[5] while manganese can be removed from the Cu by annealing.[6] Selective CVD of ruthenium (Ru) has also been used as a capping layer to increase the lifetime, but some Ru metal is still deposited on the insulator.[7]

In this chapter, a chemical vapor deposition process is presented to selectively deposit manganese on the desired surfaces of copper wires, while completely avoiding any deposition of manganese on insulators between the copper wires. Gas-phase silylation is essential to achieving this high degree of selectivity, presumably by replacing reactive SiOH groups on the insulator surface with inert $SiCH_3$ bonds. Manganese metal also dramatically strengthens the interface between copper and silicon nitride, as well as between copper and silicon oxide and low-*k* dielectrics. The debonding energy is found to increase nearly linearly with manganese content at the interface, up to values so large that the interfaces could not be broken apart. Increased adhesion strength has been linked to increased electromigration lifetime.[8] The remarkably high diffusion constant of manganese in polycrystalline copper at 300 °C is evaluated to understand the distribution of manganese in the samples prepared for the study of adhesion. This selective CVD Mn process should allow the construction of multilevel interconnects with longer lifetime and higher speed than previously possible.

3.2 Experiments

Structure of Samples for Measurements

Substrates for various measurements are shown schematically in Figure 3.1. They include blanket films of thermal SiO_2 on Si, plasma-deposited SiO_2 on Si, CVD Si_3N_4 on Si, SiCOH low-k insulator (BDII^{TM}, k = 2.5, from Applied Materials) on Si, and SiCNOH capping barrier and etch-stop (BLoK^{TM} from Applied Materials). Thermal oxide and plasma oxide substrates were cleaned of organic contamination by 5 minutes of UV-ozone treatment at room temperature. CVD silicon nitride samples were similarly cleaned by UV ozone, then dipped in dilute HF for one minute, rinsed with distilled water and blown dry. BDII^{TM} and BLoK^{TM} samples were used as received without any cleaning. Blanket copper substrates were either evaporated or sputtered onto thermally oxidized silicon wafers. A layer of titanium was sputtered prior to the copper in order to provide stronger adhesion to the sputtered copper films. The copper substrates were loaded into the CVD reactor after only a few minutes of air break, so they were fairly clean, except for a thin layer of native oxide.

Patterned substrates with interdigitated comb structures were supplied by IBM and by SELETE. These substrates have copper lines up to 10 meters long with 50, 70 or 100 nm copper linewidths separated by dense SiCOH insulators with the same linewidths. These substrates had received a final step of chemical-mechanical polishing (CMP), leaving the copper surfaces covered by a protective layer of benzotriazole (BTA). These patterned substrates were not cleaned prior to use.

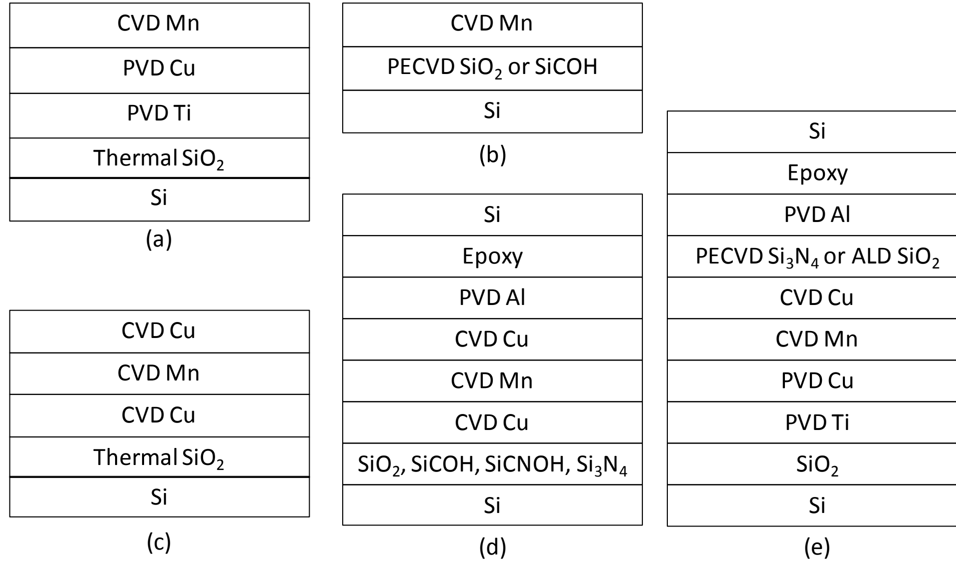

Figure 3.1 Structures of samples for measuring CVD manganese (a) deposition rate and diffusion rate, (b) SIMS depth profile, (c) selectivity, (d) purity, (e) adhesion to substrates, and (f) adhesion to superstrates.

CVD of Manganese and Copper

The compound that serves as a precursor for manganese is called bis(*N,N'*-diisopropylpentanamidinato) manganese(II), whose chemical formula is shown in Figure 3.2. The compound was synthesized by methods similar to those used for other metal amidinates.[9] The vapor pressure of the precursor is estimated to be around 0.1 mbar at 90 °C. For the CVD experiments, the manganese precursor was evaporated from the liquid in a bubbler at a temperature of 90 °C into a 60 sccm flow of highly purified nitrogen (concentrations of water and oxygen less than 10^{-9} of the N_2). This vapor mixture was mixed with 60 sccm of purified hydrogen at a tee just prior to entering one end of a tubular reactor. The reactor tube has an inner diameter of 36 mm. A half cylinder of aluminum supports the substrates inside the reactor. For most depositions of manganese, the reactor temperature was controlled at 300 °C. The pressure in the reactor was maintained at 5 Torr by a pressure sensor controlling a butterfly valve between the reactor and the vacuum pump.

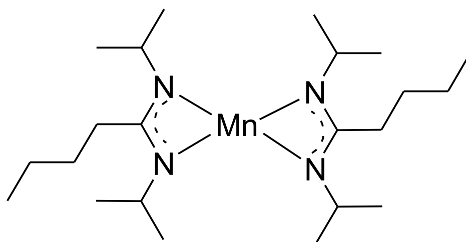

Figure 3.2 Formula for the manganese precursor

CVD copper was deposited in the same reactor using copper (*N,N'*-di-*sec*-butyl-acetamidinate) dimer[10] as a copper precursor maintained as a liquid in a bubbler at 130 °C through which 40 sccm of pure nitrogen flowed. 40 sccm of hydrogen was mixed with the copper precursor vapor just before entering the reactor held at a temperature of 200 °C and a pressure of 5 Torr. About 30 nm of copper deposited in 5 minutes under these conditions.

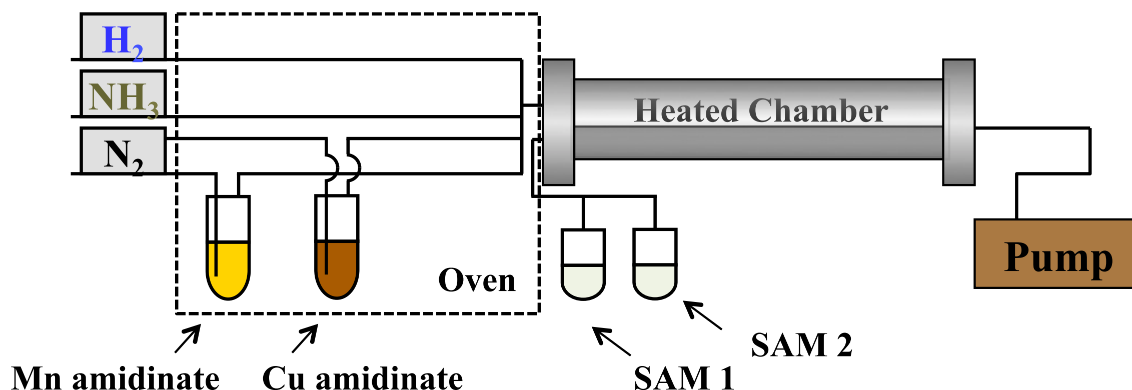

Figure 3.3 Schematic diagram of the CVD system

After the substrates were loaded into the reactor they were flushed with purified nitrogen while they were heated to 200 °C for ½ hour and 350 °C for ¼ hour in flowing purified nitrogen at 1 Torr. During this anneal water was desorbed from the dielectrics and the BTA was evaporated from the copper. Next the native oxide on the copper surfaces was reduced in flowing purified hydrogen gas at 1 Torr for 1 hour at 250 °C. In some runs, manganese was

deposited at this point. In most runs, two silylation vapor pretreatments were applied before the manganese deposition.[11,12] Prior to the silylation treatments, the reactor was cooled to room temperature, pumped down to the base pressure (about 20 mTorr), and then filled with vapor (about 14 Torr) from a room-temperature source of bis(*N,N*-dimethylamino) dimethylsilane, $(CH_3)_2Si(N(CH_3)_2)_2$ (Figure 3.4a), and heated to 90 °C for ½ hour. Then the reactor was again pumped to base pressure, cooled to room temperature and refilled with the vapor (about 75 Torr) of (*N,N*-dimethylamino) trimethylsilane, $(CH_3)_3SiN(CH_3)_2$ (Figure 3.4b), and heated to 90 °C for ½ hour. After the vapor exposures, the reactor was pumped to base pressure and the samples were then heated to the deposition temperature (typically 300 °C for manganese or 200 °C for copper).

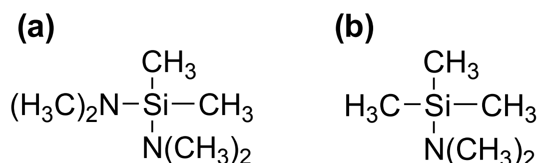

Figure 3.4 Formula for (a) bis(*N,N*-dimethylamino) dimethylsilane and (b) (*N,N*-dimethylamino) trimethylsilane

After the temperature was stabilized, a CVD vapor mixture was passed through the reactor for a time, typically 30 minutes. Some depositions were just manganese, while other runs deposited copper, then manganese and then a second copper deposition, to make Cu/Mn/Cu sandwich structures.

Characterization Methods

Samples for measuring adhesion of Cu/Mn/Cu to the substrate by the 4-point bend method[13,14,15] were taken through an air break into a chamber in which they received 0.13 μm of sputtered aluminum, and then they were attached by high-strength epoxy (EPO-TEK 353ND

from Epoxy Technology) to a piece of a second silicon wafer. The bonded wafers were cut into 50 x 6 mm beams. A notch was scribed at the center on one of the substrates to initiate the crack. Samples for testing adhesion of copper-manganese to a superstrate silicon nitride layer received an additional PECVD Si_3N_4 or ALD SiO_2 coating before the sputtered aluminum.

Rutherford Backscattering (RBS) was used to measure quantitatively the amount of manganese deposited on various substrates. The detection limit for manganese on substrates containing the elements silicon, oxygen, nitrogen, hydrogen and/or carbon is very low, $< 5 \times 10^{13}$ cm^{-2}, because there is no background signal from these light elements. On thick copper layers, a large background could obscure the manganese RBS signal. Therefore thin copper films (10 – 20 nm thick) were used as substrates for RBS analysis of Mn/Cu, so that the manganese and copper peaks could be resolved. X-ray photoelectron spectroscopy (XPS) was also used for semi-quantitative analysis of the films. XPS and secondary ion mass spectrometry (SIMS) were used for studying the depth distribution of the elements. Transmission electron microscopy (TEM) was also used to study the structure of the deposited material. Electron energy loss spectroscopy (EELS) and energy-dispersive X-ray spectroscopy (EDX) were used for elemental analysis after the selective CVD process. Test comb structures were used to measure the leakage current between copper lines as well as the resistance along the copper lines before and after CVD of manganese. Two types of dielectric capping layer insulators, silica and silicon nitride, were applied to these structures after CVD Mn. 20 nm of SiO_2 was deposited by atomic layer deposition (ALD) at 250 °C,[16] or 17 nm of Si_3N_4 was deposited by plasma-enhanced CVD (PECVD) at 300 °C. Electrical measurements of leakage and resistance before and after Mn capping layer deposition were carried out with a HP 4275A meter in a shielded probe station at room temperature.

3.3 Results and Discussion

Diffusion of Manganese in Polycrystalline Copper

A manganese film was deposited on 20 nm of copper for 30 minutes. The RBS detected 6.75×10^{16} Mn atoms cm^{-2}, or 8 nm if this material had the normal density of bulk manganese. A cross-sectional TEM of this film is shown in Figure 3.5. The Cu appears slightly darker than the Mn because its electron density is about 25 % higher than that of the Mn. The boundary between the Mn and the Cu is not sharp because the Mn has partly diffused into the Cu.

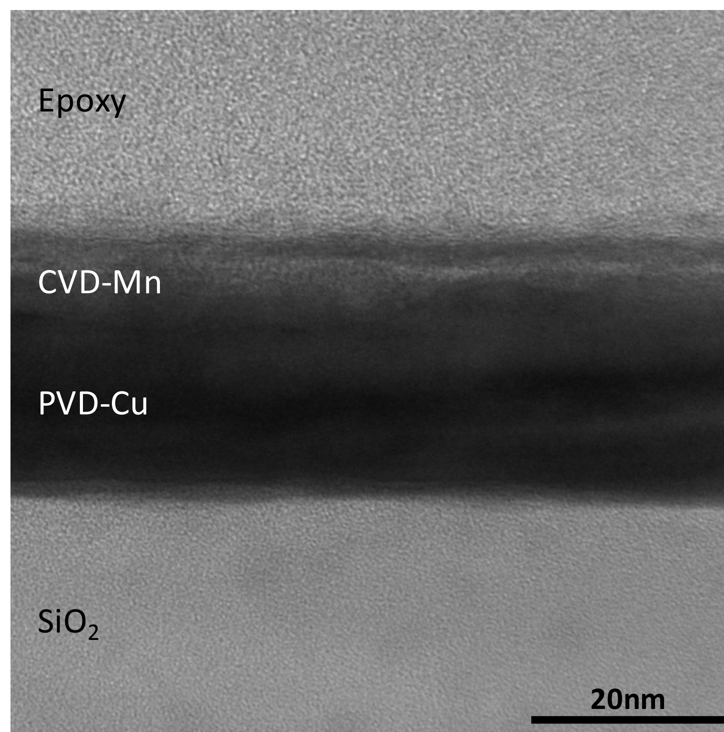

Figure 3.5 Cross-sectional TEM of CVD Mn on PVD Cu

To study this diffusion process more carefully, manganese was deposited onto a thicker copper layer for 20 minutes without H_2, resulting in about 10^{16} Mn atoms cm^{-2}. The surface composition of this sample was determined by XPS to be about 1/3 Mn and 2/3 Cu. Sputtering

this sample under 3.8 x 10^{-7} Torr of argon atmosphere provided the depth distribution of manganese shown in Figure 3.6. The line is the solution to Fick's second law of diffusion on the assumption that the surface concentration of the manganese remains constant during the CVD process, and that diffusion is then quenched by cooling after the deposition is complete. The diffusion constant determined from this fit is 3 x 10^{-21} m^2 s^{-1}, although this value may be slightly too high because of ion mixing during the depth profiling and because of the penetration depth (~ 1 nm) of the XPS analysis. This estimated value is about 30 times larger than the value reported for diffusion of Mn into single-crystal copper at 300 °C.[17] Presumably, the higher diffusion rate observed in our sample is due to rapid diffusion of the manganese along grain boundaries in the polycrystalline sputtered copper layer.

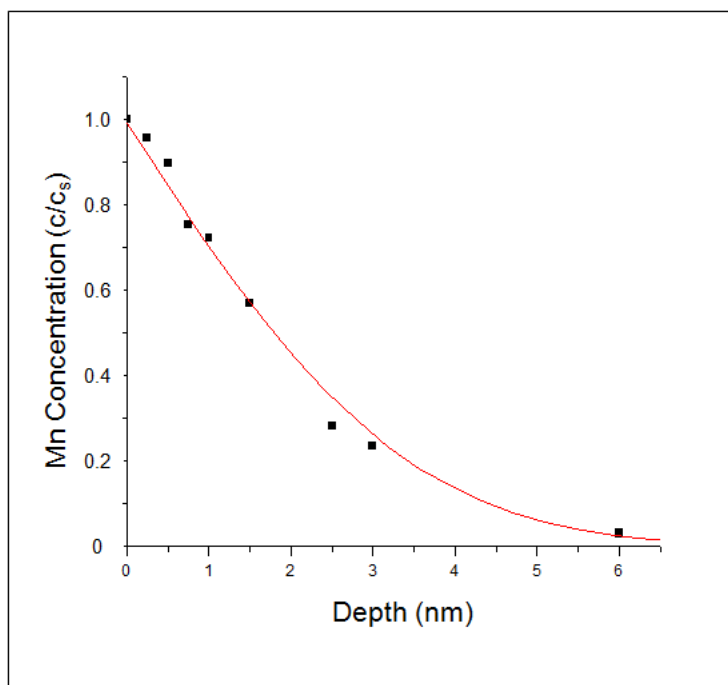

Figure 3.6 Distribution of Mn in Cu after CVD (c_s is the surface concentration)

A sample was prepared for the SIMS depth profile shown in Figure 3.7. Manganese was deposited on 20 nm of Cu, followed by a post-deposition anneal at 350 °C to diffuse the manganese into the copper layer. 20 nm of SiO_2 was the deposited by ALD on top of the Mn/Cu alloy. The sample was then annealed at 400 °C for two hours to allow manganese to diffuse out from copper. The depth distribution confirms the diffusion of manganese through copper to form manganese silicate ($MnSi_xO_y$) at the Cu/SiO_2 interfaces.[6]

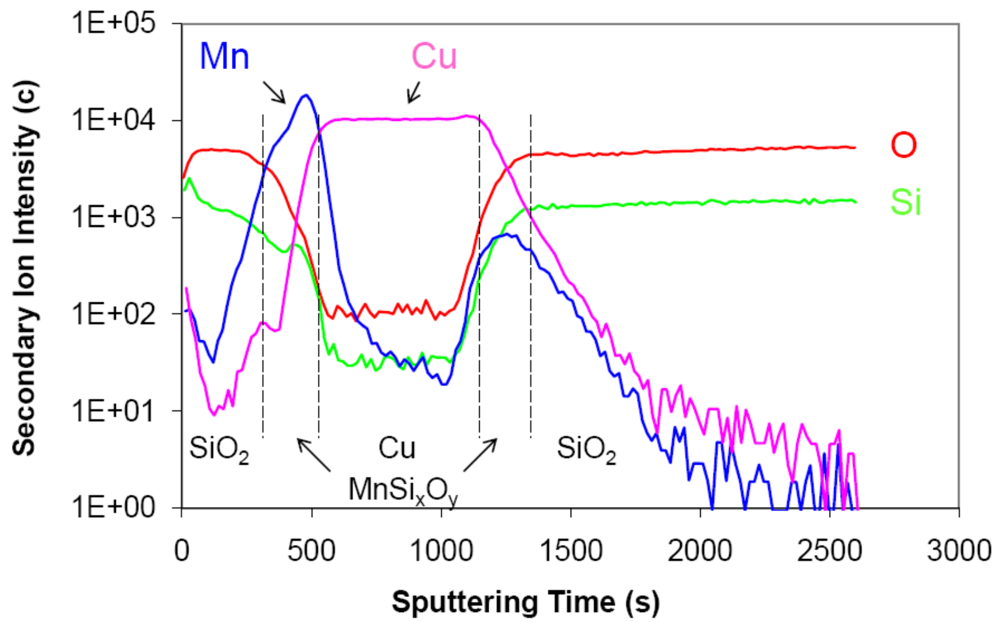

Figure 3.7 SIMS depth profile of SiO_2/Mn/Cu/SiO_2 structure after post-annealing at 400 °C

The purity of the deposited manganese was determined by depositing CVD Cu, then CVD Mn, and then CVD Cu again without removing the substrate from the reactor. This structure protects the manganese from contamination by elements such as carbon and oxygen from the ambient atmosphere. This surface contamination is confined to the surface of the outer copper layer, which is removed by the initial sputtering during the XPS analysis. No carbon,

nitrogen or oxygen impurities were found within the Cu/Mn/Cu layers, at the level of sensitivity of XPS, ~ 1 %.

Adhesion Enhancement at Copper/Capping Layer Interface

The effect of manganese concentration on the adhesion strength of copper-manganese alloys to various insulators was tested by the 4-point bend method. Various thicknesses (10 to 50 nm) of the copper and manganese layers were chosen, so that the amount of manganese diffusing through the copper to the copper/insulator interfaces of the Cu/Mn/Cu layers could be varied widely. The top copper layer is necessary to protect the manganese from oxidation during the air break between CVD Mn and PECVD Si_3N_4 depositions. After the debonding test, the fracture surfaces were analyzed by XPS to determine which interface had cracked apart. On debonded insulator surfaces, the ratio of Mn to Si was estimated from the XPS data. The resulting interface fracture energies between the copper and the insulator are plotted in Figure 3.8 as a function of the Mn/Si ratio on the insulator surface from the fractured interface.

When no manganese is present at the interface, the pure copper layer is detached very easily from the surface of the insulating substrates, with interface fracture energy 0.7 J m^{-2} for Si_3N_4 and about 1.2 J m^{-2} for SiO_2 or SiCNOH. These pure copper films are easily removed from the insulators with adhesive tapes. Copper films through which manganese diffused to the insulator surface adhere much more strongly, and they cannot be removed by tape. The interface fracture energy is found to increase nearly linearly with the amount of Mn at the interface, to very high values over 10 J m^{-2}. Samples were also prepared under conditions (longer Mn deposition times, thinner Cu layers) that should provide still more manganese at the interface than those samples that were plotted Figure 3.8. However, these higher-Mn interfaces were so

strongly bonded together that the samples debonded at the Al/epoxy interface with measured fracture toughness of more than 30 J m^{-2}. Therefore, specific interface energies could not be these very strongly-bonded interfaces.

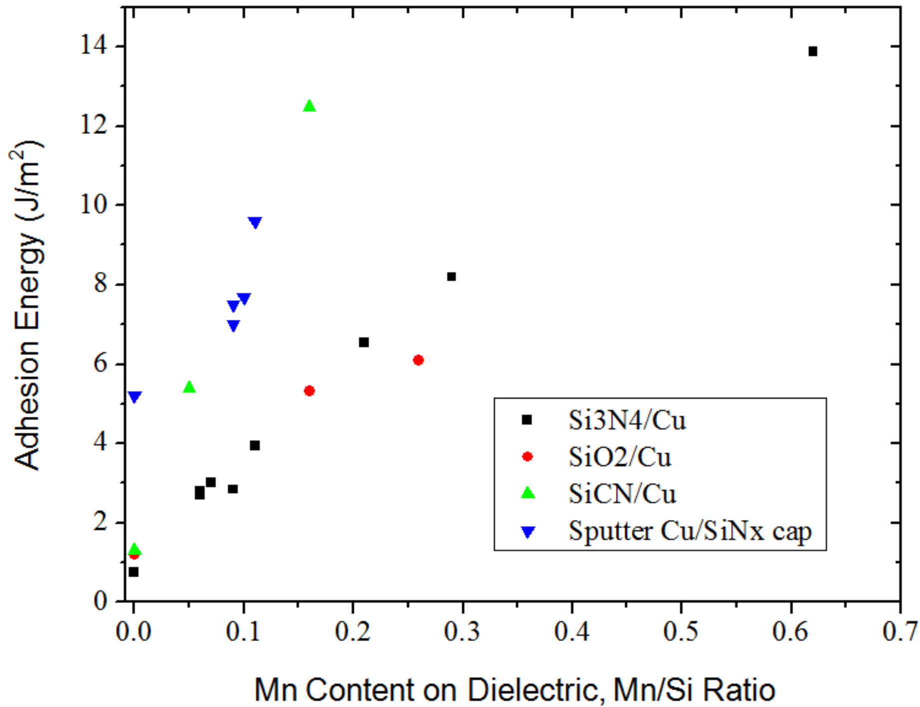

Figure 3.8 Adhesion energy of Cu(Mn) versus Mn/Si ratio on the surface of the dielectric

Manganese was also found to increase the adhesion of silicon nitride deposited on top of copper. First CVD manganese and then CVD Cu were applied to sputtered Cu/Ti/SiO_2/Si substrates. After an air break, this surface was cleaned by ammonia plasma, and 300 nm of Si_3N_4 was applied by PECVD, followed by 0.13 μm of sputtered aluminum. The resulting debonding energies in Figure 3.8 show that the addition of Mn/Si = 0.1 also strengthens the adhesion of PECVD Si_3N_4 deposited on top of copper to about 10 J m^{-2}. Si_3N_4/Cu-Mn interfaces having Mn/Si ratios larger than 0.1 could not be broken apart.

Selective Deposition of Manganese

When insulator surfaces were used as substrates for CVD Mn, much less Mn is deposited than on copper substrates. For thermal SiO_2 substrates, about 1.93×10^{15} cm^{-2} Mn atoms were found, which is 35 times less Mn than is deposited on Cu under the same conditions. Similar results were found for a low-*k* insulator (Applied Materials BDII, dielectric constant 2.5), on which 1.79×10^{15} cm^{-2} Mn atoms were measured, or 38 times less Mn than deposited on Cu. To understand this selectivity better, a cross-sectional TEM was taken of this sample (Figure 3.9). Manganese nuclei are seen scattered on the surface, but no continuous layer of manganese has formed. Evidently most of the insulator surface is not reactive to the manganese precursor in the presence of hydrogen, so growth takes place only on a small number of reactive sites on the surface. This result is in surprising contrast to the uniform layer of manganese silicate formed on the surface of silica by the same manganese precursor in the absence of hydrogen.[18]

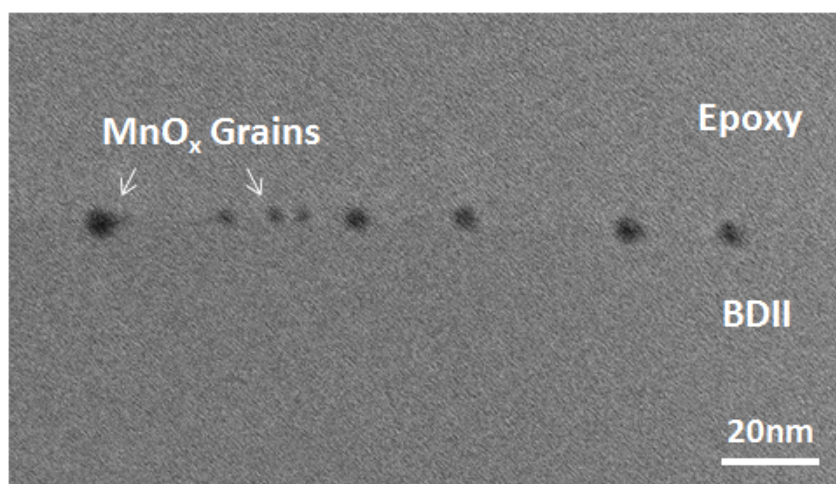

Figure 3.9 Cross-sectional TEM of CVD Mn on unpassivated low-*k* dielectric, BDII

In order to prevent growth on these reactive sites, silylamides were applied to pre-react the substrate surface and replace the reactive SiOH sites with Si-methyl bonds, which are notably unreactive. As the first step in this passivation process, the vapor of bis(*N,N*-dimethylamino) dimethylsilane, $(CH_3)_2Si(N(CH_3)_2)_2$, was reacted with the insulator surfaces, because it should

react with pairs of neighboring SiOH groups, as well as with isolated SiOH groups. A vapor of (*N,N*-dimethylamino) trimethylsilane, $(CH_3)_3SiN(CH_3)_2$, was then applied, because this compound should react with any remaining isolated SiOH bonds. Successive application of these two treatments was found to completely inhibit growth of CVD manganese on the treated insulator surfaces even after 30 minutes of Mn deposition. RBS found no manganese at all on any of the insulator surfaces, with a detection limit of < 5×10^{13} Mn atoms cm^{-2} (Figure 3.10). This limit is less than 0.07% of the amount of Mn deposited on Cu under the same conditions, or a selectivity at least 1300:1.

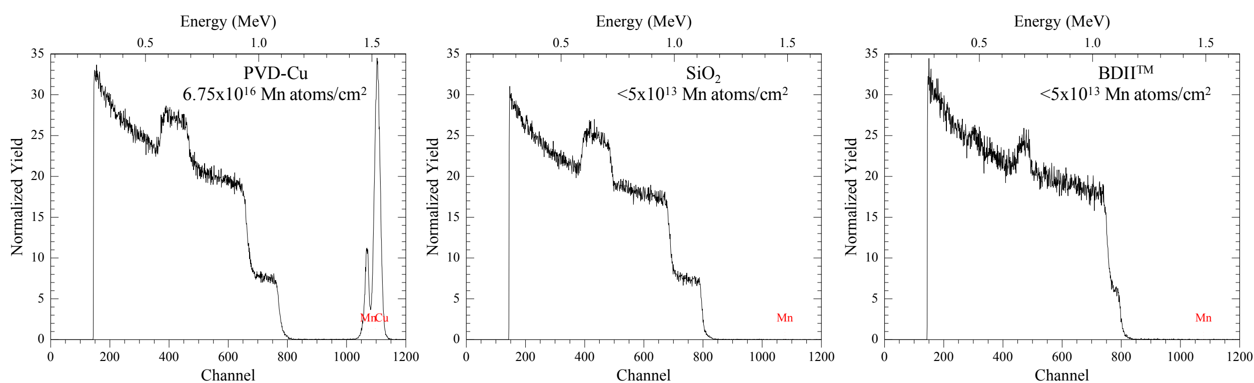

Figure 3.10 RBS of CVD manganese on silylated (a) copper, (b) SiO_2, and (c) BDII low-*k* dielectric

This high selectivity was confirmed by XPS, which could not detect any Mn on the treated insulator surfaces. If only one of the silylation treatments was applied, then residual Mn was detected by RBS and XPS (Figure 3.11) on insulator surfaces after CVD Mn. Thus the combination of the two treatments is much more effective in deactivating the surface than either one applied individually.

In order to study the effect of these two silylation treatments on copper surfaces, air-exposed copper films were exposed to the two silylamide vapors. XPS analysis of the treated surface showed the presence of silicon. Thus copper oxide does have sites, probably CuOH

bonds that are reactive to the silylamides. In order to remove these reactive sites from Cu, air-exposed Cu was heated to 250 °C in a flow of hydrogen gas for 1 hour, cooled down to room temperature in the reactor and then exposed in sequence to the two silylamides without any intervening air exposure. The resulting copper surface was free of silicon, according to XPS analysis. Therefore, it is evident that a clean copper surface does not react with the silylamide vapors.

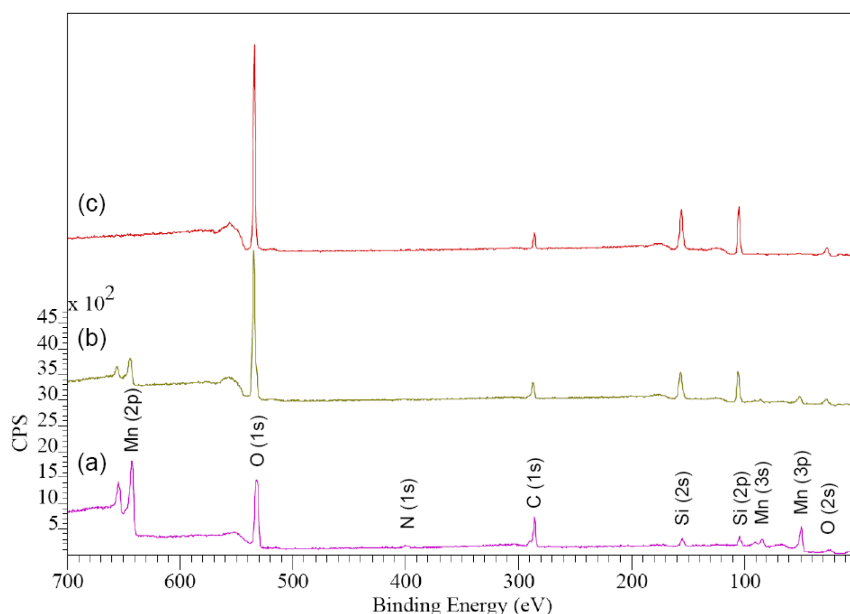

Figure 3.11 XPS showing the effectiveness of SAM treatments on surface passivation (a) (*N*,*N*-dimethylamino) trimethylsilane only, (b) Bis(dimethylamino) dimethylsilane only, and (c) Bis(dimethylamino) dimethylsilane followed by (*N*,*N*-dimethylamino) trimethylsilane

High selectivity was also confirmed by EELS/EDX elemental analysis, in which manganese contents were observed only on the top surface of copper and not on the insulator or the tantalum liner (Figure 3.12).

Figure 3.12 EELS/EDX showing selective deposition of Mn on Cu surface (Substrate and image courtesy of IBM)

Line-to-line Leakage Measurements

Test comb structures with interdigitated copper lines and insulators were used as substrates for manganese deposition. After drying, reduction, and silylation as described above, the reactor was heated to 300 °C and the Mn precursor vapor and hydrogen were applied together for 20 minutes. The reactor was cooled down to room temperature before removing the samples for electrical testing. Samples were then transferred to other reactors for capping by plasma-enhanced CVD Si_3N_4 or by ALD SiO_2.[16]

Line-to-line leakage current remained unchanged by manganese deposition on these patterned substrates (Figure 3.13). Resistance along a line increased by 1 to 4 % after manganese deposition, but then decreased by 9 to 12 % after post-annealing at 400 °C for 1 hour. During this anneal process, the manganese diffuses out of solution in the copper and forms a manganese

silicate ($MnSi_xO_y$) layer within the surface of nearby silica surfaces, and forming direct Cu-to-Cu contact between levels without any intervening manganese.[19] The final resistivity is lower than the starting value because of copper grain growth during the anneal. Manganese silicate has been shown in Chapter 2 to be an excellent barrier to diffusion of copper,[20] as well as to water and oxygen.[18] Thus copper wiring could be capped by silica-based low-*k* dielectrics instead of the currently-used silicon nitride, which has a much higher dielectric constant. This replacement would lower the overall dielectric constant of the interconnect structure, and therefore increase its speed of operation.

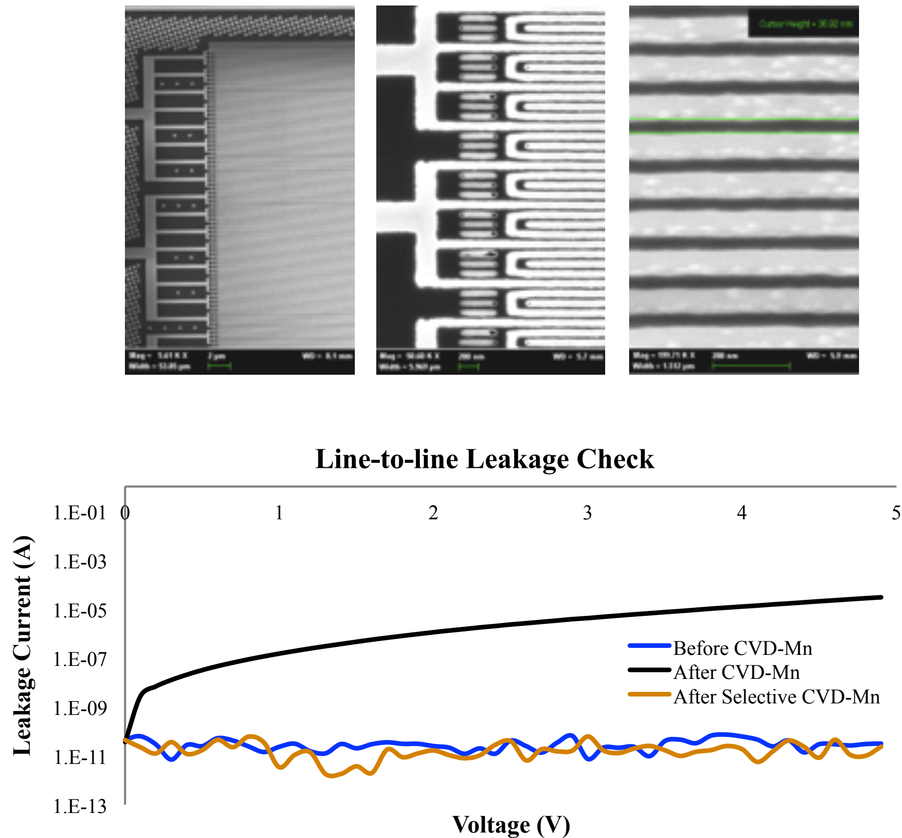

Figure 3.13 Line-to-line leakage measurement before and after CVD Mn process on test comb structures

3.4 Conclusions

The presence of manganese metal at the interface between copper and insulators is shown to increase the adhesion strength dramatically. The debonding energy increases approximately linearly with the amount of manganese at the interface. A selective CVD process was developed to deposit the manganese only on copper surfaces while completely avoiding any deposition on adjacent silylated surfaces of insulators, such as silica or SiOC low-*k* dielectrics. This selective CVD process has the potential to increase the lifetime of copper wires in microelectronics without any increase of resistance due to capping metal between levels of interconnects. At the same time, the process can reduce the capacitance and increase the speed of interconnects by eliminating the need for a high-*k* diffusion barrier on top of each level of wiring.

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Chapter 4

Surfactant-catalyzed Bottom-up Filling of Copper and Copper-manganese Alloy in Narrow Features

4.1 Introduction

Continuous enhancements in device performance and functionality have been achieved by reducing of the physical size of devices and increasing the number of metal wiring levels. With increasing packing density in microelectronic devices, copper (Cu) is used as an interconnecting metal due to its superior electrical conductivity and excellent resistance against electromigration.[1,2] The dual-damascene process, which involves copper electroplating in preformed trenches and vias in interlayer dielectrics, followed by chemical-mechanical polishing (CMP) of the copper, has been commonly adopted for patterning copper.[3] Compared to traditional vacuum deposition techniques such as chemical vapor deposition (CVD) and physical vapor deposition (PVD), the electroplating process has the ability to fill sub-micrometer trenches and via holes in a bottom-up fashion while avoiding the formation seams and voids.[4]

Iodine adsorbed on a copper seed layer has been shown to act as a catalytic surfactant to improve growth rate and surface smoothness of copper films deposited by CVD. When Cu(I)-hexafluoroacetylacetonate-vinyltrimethylsilane [Cu(I)(hfac)(vtms)] is used as the precursor, the electronegative iodine atom adsorbed on copper surface weakens the Cu^{+}-(β-diketonate)$^{-}$ ionic bond, thus facilitating the dissociation of the precursor molecule and promoting 2-D lateral growth.[5] During iodine-catalyzed CVD in sub-micrometer trenches and via holes, the growth rate of copper at the bottom of the features is continuously accelerated due to reduction of surface

area and increasing concentration of iodine catalyst. As a result, bottom-up filling of copper could be achieved (Figure 4.1).[6,7] Modeling of bottom-up filling during iodine-catalyzed CVD was done using the curvature-enhanced accelerator coverage (CEAC) model.[8,9] This catalyst-enhanced process, however, requires a conformal copper seed layer on top of the diffusion barrier and adhesion layer. Preparation of this seed layer is challenging on sub-30 nm features. Moreover, the stack of diffusion barrier, adhesion layer and seed layer will occupy substantial portions of these features, leaving less room for the more conductive copper. The remaining smaller amount of copper has higher resistance and thus slower circuit speeds. The narrower copper wires have a shorter lifetime before the higher current density destroys them by electromigration.

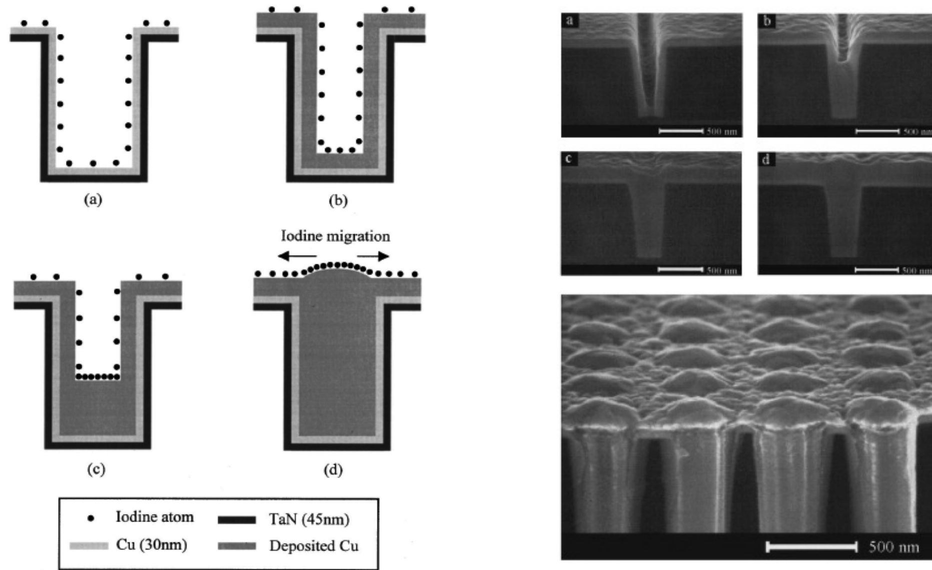

Figure 4.1 Schematic diagram of the surfactant-enhanced CVD growth mechanism and cross-sectional SEM images of the copper bottom-up filling of a trench with a width of 0.3 μm and a depth of 1.0 μm (Ref. 6)

In this chapter, a process for the bottom-up filling of sub-30 nm trenches with copper or copper-manganese alloy is presented. Iodine is chemisorbed onto the surfaces of a thin, conformal manganese nitride layer that prevents diffusion of copper and also enhances adhesion

between copper and the insulating substrates. When CVD of copper or copper-manganese alloy begins, the iodine is released from the surface of the manganese nitride. The iodine then floats on the surface of a growing copper layer and catalyzes the bottom-up filling of trenches without leaving any seams or voids. Upon post-annealing, manganese in the alloy diffuses out from copper through the grain boundaries and forms a self-aligned layer on nearby insulator surfaces, thereby further improving adhesion and barrier properties at the copper/insulator interface. This process should facilitate the fabrication of future generations of nanoscale microelectronic devices with faster and more robust interconnections.

4.2 Experiments

Deposition of Manganese Nitride, Copper, and Copper-manganese Alloy Films

Patterned substrates with trench structures were obtained with widths around 30 to 40 nm and aspect ratio of about 5 to 1. These substrates were cleaned by an oxygen plasma with 10 watt RF power at 0.01 Torr pressure for 3 minutes at room temperature to remove contaminants on the surface and deep in the trenches. Some of the substrates received an additional deposition of silicon dioxide by atomic layer deposition (ALD) to further reduce the widths of the trenches to as narrow as 17 nm.[10]

A schematic diagram of the CVD system is shown in Figure 4.2. The compound that serves as a precursor for manganese and manganese nitride is called bis(*N*,*N'*-diisopropylpentylamidinato) manganese (II), whose chemical formula is shown in Figure 3.2. The precursor for copper deposition is a copper (*N*,*N'*-di-*sec*-butylacetamidinate) dimer and has

the chemical structure shown in Figure 4.3. These compounds were synthesized by methods similar to those described previously.[11,12]

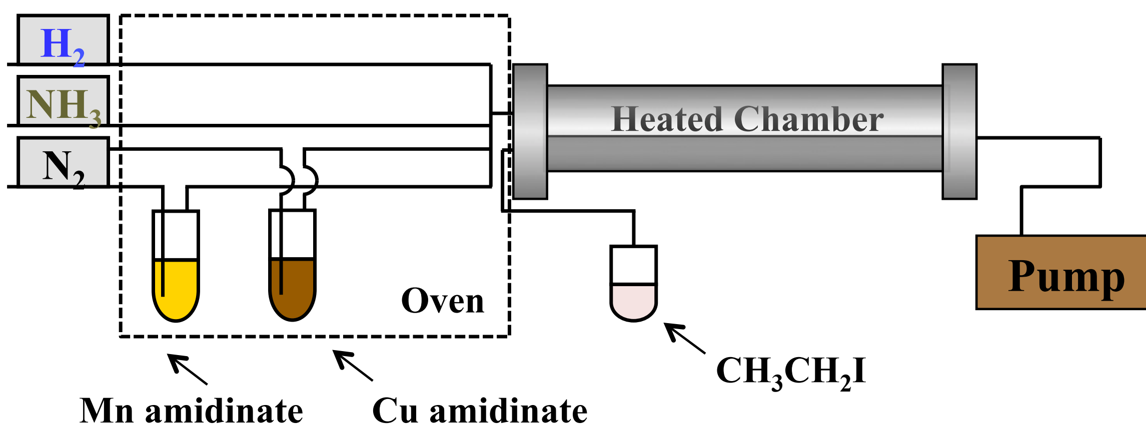

Figure 4.2 Schematic diagram of the CVD system

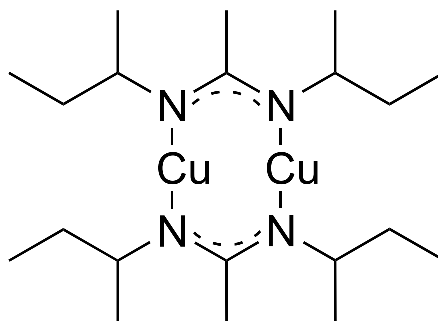

Figure 4.3 Formula for the copper precursor

To prepare manganese nitride by CVD, the manganese precursor was evaporated from the liquid in a bubbler at a temperature of 90 °C into a 60 sccm flow of highly purified nitrogen (concentrations of water and oxygen less than 10^{-9} relative to N_2). This vapor mixture was mixed with 60 sccm of purified nitrogen and 60 sccm of purified ammonia (NH_3) in a tee just before entering one end of a tubular reactor. The reactor tube had an inner diameter of 36 mm. A half-cylinder of aluminum supported the substrates inside the reactor. The reactor temperature was controlled at 130 °C and the pressure in the reactor was maintained at 5 Torr by a pressure sensor

controlling a butterfly valve between the reactor and the vacuum pump. After deposition of manganese nitride was complete, the substrate was cooled in the reactor in a flow of pure nitrogen in order to protect the manganese nitride film from oxidation.

Ethyl iodide (CH_3CH_2I) was then used as an iodine source to adsorb iodine atoms onto the fresh surface of the manganese nitride film at 50 °C. The liquid ethyl iodide was contained in a bubbler at room temperature and its vapor was fed directly into the reactor without a carrier gas, controlled by a needle valve to a pressure of 0.05 Torr. For CVD of copper, the copper precursor was evaporated from the liquid in a bubbler at a temperature of 130 °C into a 40 sccm flow of highly purified nitrogen. Hydrogen (40 sccm) was mixed with the copper precursor vapor just before entering the reactor held at a temperature of 180 °C and a pressure of 5 Torr.

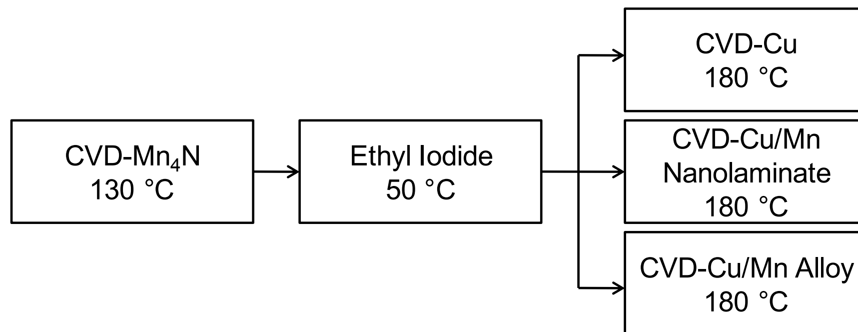

Figure 4.4 Schematic diagram of the CVD process flow

A schematic diagram of the CVD process flow is shown in Figure 4.4. In a typical process that the trenches are filled with pure copper, manganese nitride was first deposited at 130 °C for 5 minutes to form 2.5 nm of film. Ethyl iodide was then introduced into the chamber at 50 °C for 30 seconds. CVD copper was deposited at 180 °C until the trenches are completely filled, which typically took a few minutes. To fill the trenches with copper-manganese nanolaminate, manganese nitride was first deposited at 130 °C for 5 minutes, followed by an exposure of ethyl iodide at 50 °C for 30 seconds. Copper was then deposited at 180 °C for 5

minutes to form a continuous layer, and ethyl iodide vapors were exposed to the copper surface at 50 °C for 30 seconds. Manganese and copper precursors were then alternately carried into the chamber by 50 sccm of nitrogen and mixed with 50 sccm of hydrogen at a temperature of 180 °C and a pressure of 5 Torr. In one cycle, the manganese precursors were supplied for 3 minutes and the copper precursors were supplied for 5 minutes. This cycle was repeated until the trenches were completely filled with a copper-manganese nanolaminate. To fill the trenches with copper-manganese alloy, manganese nitride was first deposited at 130 °C for 5 minutes, followed by an exposure of ethyl iodide at 50 °C for 30 seconds. Then the manganese precursor vapors were carried by 60 sccm of nitrogen and simultaneously the Cu precursor vapors were carried by 40 sccm of nitrogen. These precursor vapor flows were mixed together with 100 sccm of hydrogen at a temperature of 180 °C and a pressure of 5 Torr.

Characterization Methods

The thickness of manganese nitride was measured by X-ray reflectometry (XRR), and the thickness of copper was measured by scanning electron microscopy (SEM). Atomic force microscopy (AFM) was used to evaluate the surface morphology of the manganese nitride film. The effectiveness of manganese nitride as a barrier to copper diffusion was tested by looking for its reaction with silicon to form copper silicide under an energy-dispersive X-ray spectrometer (EDX) and SEM. The effectiveness of manganese nitride as an adhesion layer was evaluated by a 4-point bend method as described in Chapter 3.[13]

Surface analyses and depth profiles of CVD copper on planar PVD Cu seed/thermal SiO_2/Si substrate were obtained by X-ray photoelectron spectroscopy (XPS). The effectiveness of CVD copper in super-filling narrow trenches was evaluated by cross sectional SEM and

transmission electron microscopy (TEM). The cross sectional SEM and TEM samples were prepared by focused ion beam (FIB). The Mn/Cu ratio was quantified by X-ray fluorescence (XRF).

Samples for electrical characterization at IMEC received an additional 400 nm of thermally evaporated copper to make them more suitable for chemical-mechanical polishing (CMP). The samples were then post-annealed at 350 °C for 2 hours under pure nitrogen gas ambient to diffuse the manganese from the alloy to the copper/insulator interface. Elemental analysis was carried out using energy-filtered TEM (EFTEM). Following CMP, the resistivity values of the copper wires were determined by electrical measurements of line resistance and TEM measurements of Cu cross-sectional area. Distribution of impurities in the Cu-Mn layer was evaluated by time-of-flight secondary ion mass spectrometry (ToF-SIMS).

4.3 Results and Discussion

Conformal Deposition of Manganese Nitride Films

Under the conditions described above, about 2.5 nm of manganese nitride film was deposited in 5 minutes. At a deposition temperature of 130 °C, substrates having holes with aspect ratio (ratio of length to diameter) greater than 30:1 were coated with MnN_x, x ~ 0.25. Figure 4.5 is a SEM image of a cross section through some of these holes, showing that manganese nitride was deposited uniformly and conformally over the inside surfaces of these holes. Electron diffraction showed that the material has the cubic structure known for Mn_4N.[14] AFM showed that Mn_4N films are fairly smooth, with a root-mean-square roughness equal to

7 % of their thickness. The high conformality and smooth morphology allow manganese nitride to be a suitable underlayer to initiate the catalytic CVD processes in deep, narrow trenches.

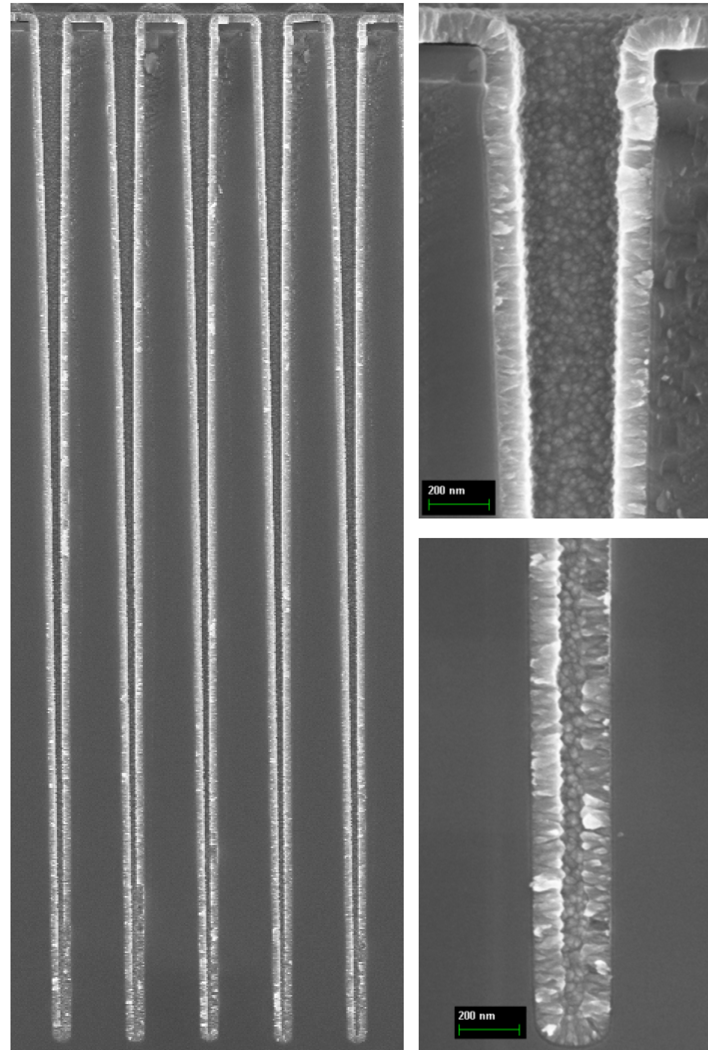

Figure 4.5 Step coverage of manganese nitride films in holes with aspect ratio > 30:1

Barrier and Adhesion Properties of Manganese Nitride Films

Manganese nitride films show barrier properties against copper diffusion. For this copper diffusion test, 9 nm of SiO_2 were grown on HF-etched silicon wafers by ALD at 250 °C, followed by CVD manganese nitride at 130 °C for 5 minutes and a post-deposition anneal at 350 °C for 1 hour under nitrogen ambient. Control samples of SiO_2 omitted the CVD manganese

nitride treatment. Copper layers about 200 nm thick were then deposited on top of the manganese nitride or SiO_2 layers. The samples were then annealed in a pure nitrogen atmosphere at 500 °C for 1 hour. To see if copper had diffused into the silicon substrate, the copper layers were dissolved in nitric acid, and the manganese nitride and silica were removed by dilute HF. The etched surfaces were then analyzed by an EDX and SEM with the results shown in Figure 4.6. The reference sample shows that the majority of its surface is covered by copper silicide crystallites, indicating copper has diffused through the thin silica layer. The manganese nitride-treated sample does not show any copper by large-area EDX, showing that Mn_4N or its reaction product with SiO_2 forms an effective barrier against diffusion of copper.

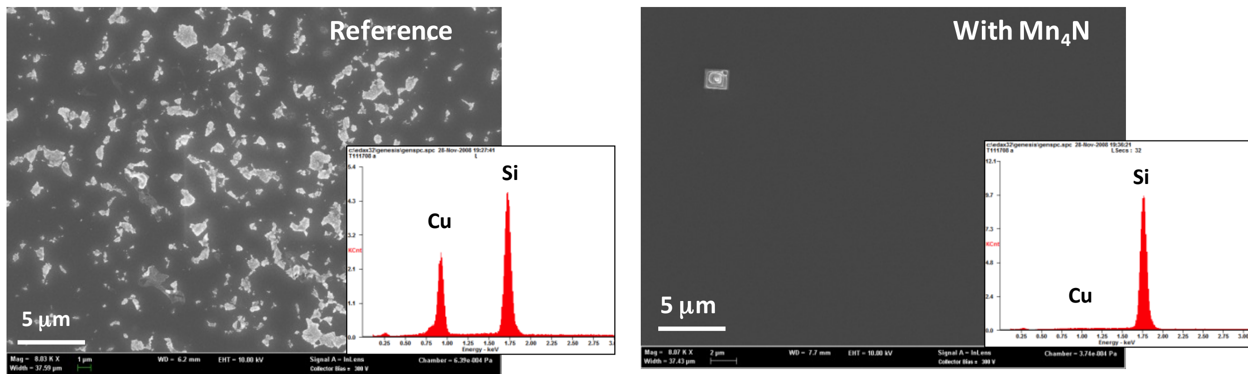

Figure 4.6 SEM and EDX of etched Si surfaces after post-annealing at 500 °C for one hour, indicating manganese nitride is an effective barrier against copper diffusion

One factor that extends the electromigration lifetime is if the adhesion of the copper to the surrounding material is strong. Therefore the adhesion of planar copper films grown on Mn_4N was tested. Following 2.5 nm of manganese nitride and 70 nm of copper depositions, the structures were annealed at 350 °C for one hour in a pure nitrogen gas ambient. 4-point bend tests on these samples showed debonding energies greater than 6.5 Joules per square meter, which is a value high enough to survive further fabrication by chemical-mechanical polishing.

Surfactant-catalyzed CVD of Copper

On a thin PVD copper seed layer that is not exposed to vapors of ethyl iodide, about 18 nm of copper film is deposited in one hour at a deposition temperature of 180 °C and a pressure of 5 Torr. When vapors of ethyl iodide are exposed to the copper seed layer, about 180 nm of copper film is deposited under the same condition (Figure 4.7).

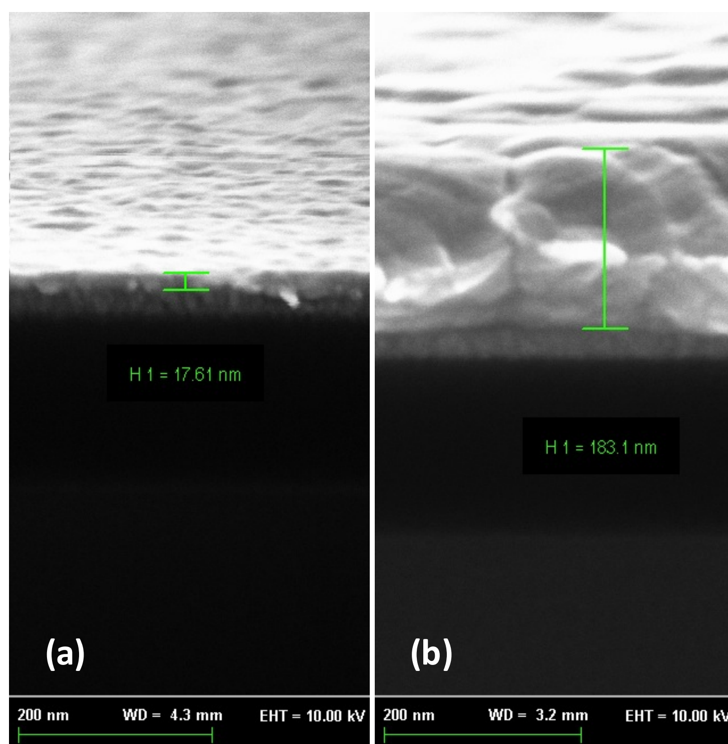

Figure 4.7 Cross sectional SEM showing thickness of CVD Cu film after 1 hour of deposition on (a) fresh PVD Cu seed layer, and (b) ethyl iodide-exposed PVD Cu seed layer

The electronegative iodine atom may be weakening the bond between copper and amidinate ligands and facilitating the dissociation of the precursor, resulting in a 10-fold accelerated growth rate. XPS depth profile of iodine-catalyzed CVD of copper shows iodine contents only on the top surface of copper (Figure 4.8). Signals of iodine disappear together with signals of surface oxygen and carbon as the film is sputtered from the top by argon ions, and no

impurities are detectable in the bulk of the copper film. When vapors of ethyl iodide are exposed to copper or manganese nitride underlayers, enhancement in copper growth rate and surface smoothness is observed. When SiO_2 is exposed to ethyl iodide vapors, no catalytic effects are observed during the CVD process because bare silica surface is unable to dissociate the ethyl iodide molecule.

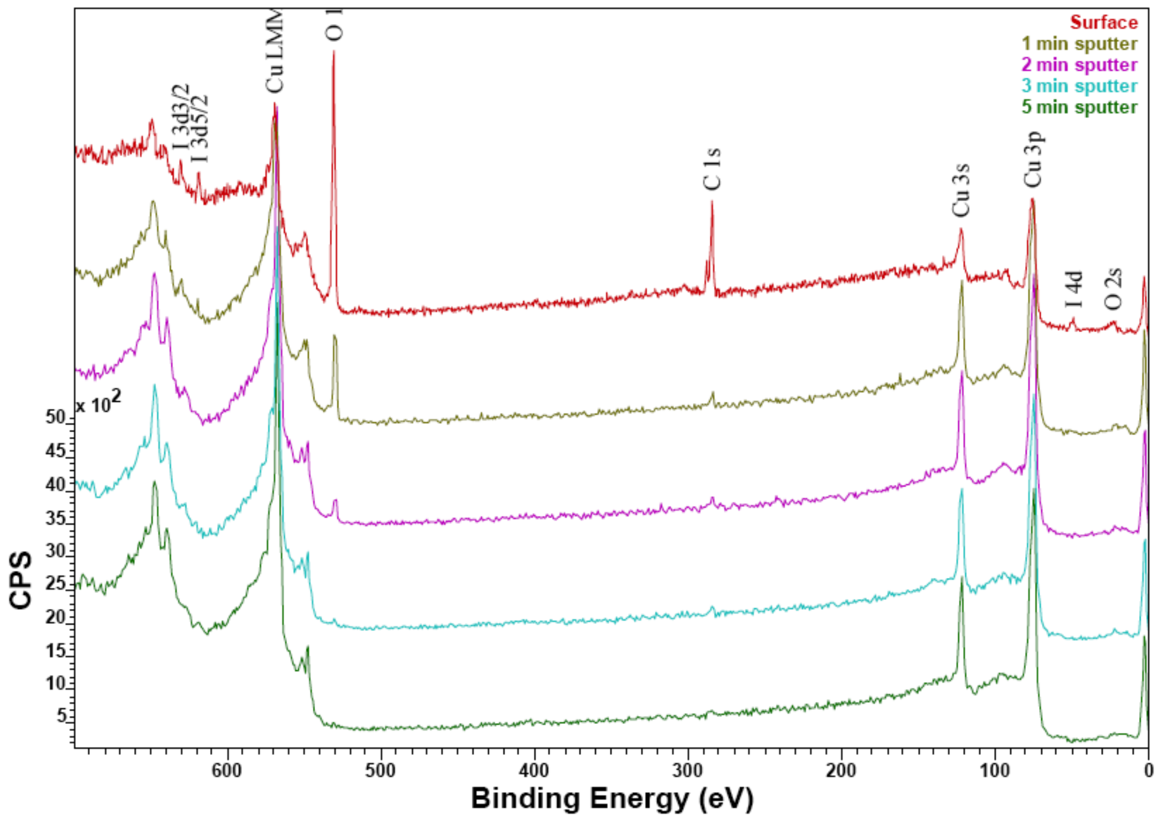

Figure 4.8 Depth profile of iodine-catalyzed CVD of Cu, indicating iodine is a surfactant that is not incorporated into the copper film

Bottom-up Filling of Narrow Trenches by Surfactant-Catalyzed CVD of Copper

Narrow trenches can be filled by copper in a bottom-up fashion without leaving any voids or seams when a thin manganese nitride film is used as the underlayer and iodine is used as the surfactant catalyst. TEMs in Figure 4.9 show that this process completely filled trenches less

than 30 nm wide and over 150 nm deep with copper, with an aspect ratio over 5:1. No seams or voids were seen along the centerline of the copper. Wider trenches were partially filled with copper by the same deposition conditions, as shown in Figure 4.10. The fact that the copper grew faster from the bottom than from the sides of the trench suggests that iodine pre-adsorbed on the Mn_4N was released from the Mn_4N layer and then catalyzed the bottom-up filling of these trenches as a surfactant floating on the growing surface of the copper.

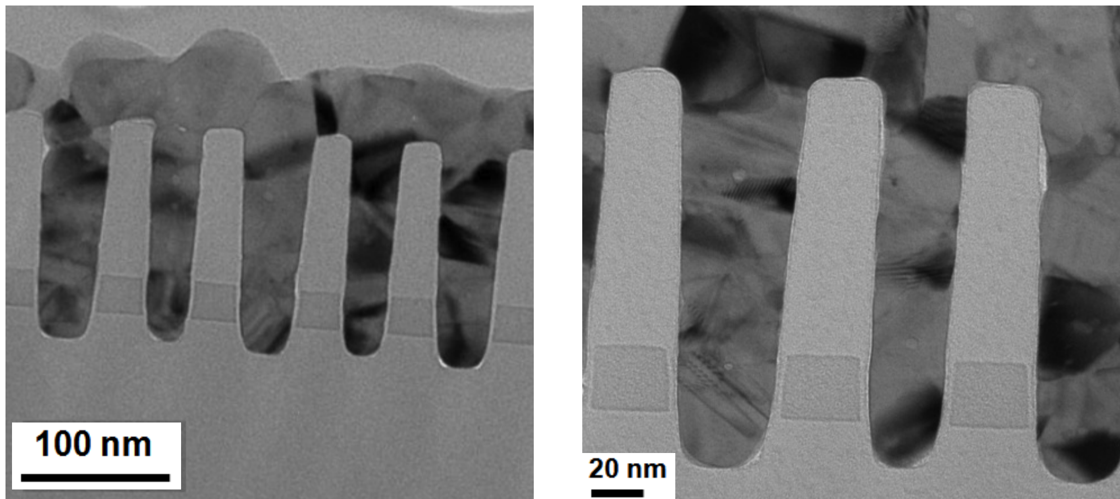

Figure 4.9 Cross sectional TEM showing complete filling of narrow trenches by iodine-catalyzed CVD of copper (Substrate and image courtesy of Applied Materials)

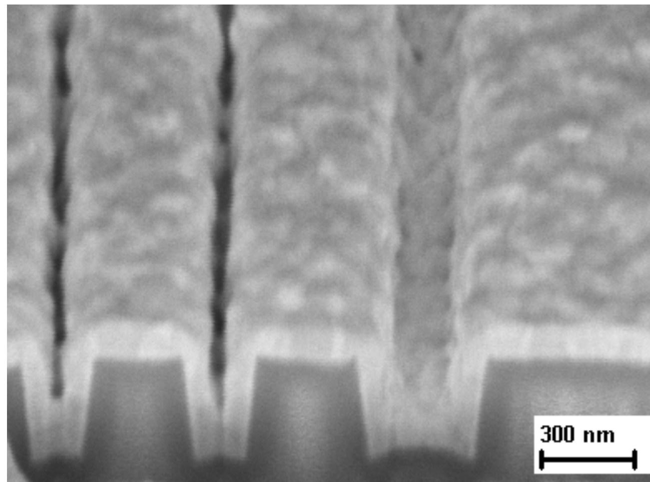

Figure 4.10 Cross sectional SEM showing trenches partly filled by iodine-catalyzed CVD of copper

Even narrower trenches, with widths as low as 17 nm, depths over 150 nm and aspect ratios as high as 9:1, were also filled with copper by this process, as shown by the SEM in Figures 4.11. Some of these high aspect ratio features, however, may contain defects and voids that are unobvious under the SEM.

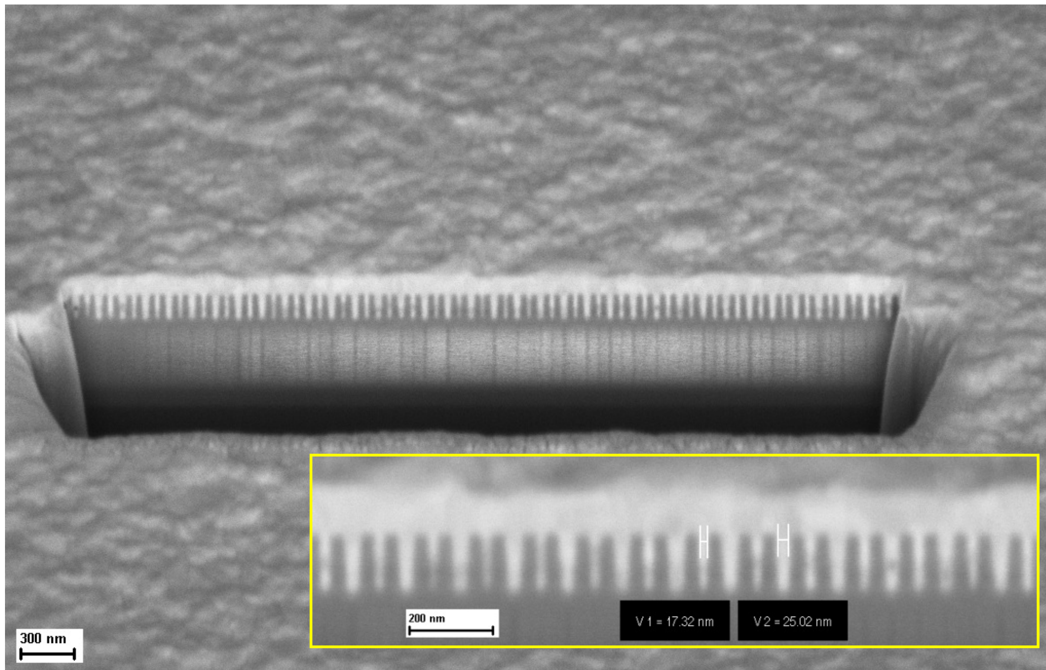

Figure 4.11 Cross sectional SEM showing filling of Cu in narrow trenches (width ~ 17 nm) with aspect ratio of 9:1

Bottom-up Filling of Narrow Trenches by Surfactant-Catalyzed CVD of Cu-Mn Alloy

Manganese was incorporated into this CVD copper process to form either a nanolaminate or an alloy which was analyzed by XRF to have approximately 0.5 to 2.0 atomic percent of manganese in copper. The trenches were once again be completely filled with copper-manganese alloy, as shown in Figure 4.12.

Upon annealing at temperatures above 350 °C, manganese will diffuse through the grain boundaries of copper to the surfaces of insulator such as SiO_2, Si_3N_4 and SiCO low-*k* insulators. This diffusion process, as discussed in Chapter 3, returns the resistivity of copper to its original

value and strengthens the copper/dielectric interface by forming a self-aligned barrier and adhesion layer at the interface.[13] When the ratio of manganese to silicon exceeds about 0.5 at the interface between the Cu-Mn and the insulator, the debonding energy becomes larger than about 15 Joules per square meter. Such strong interfaces cannot be broken during the 4-point bend test. This very strong adhesion is expected to greatly increase the lifetime of copper interconnects before they fail by electromigration. The amount of manganese in the copper that will be needed to achieve this interfacial concentration will depend on the size and shape of the copper interconnects.

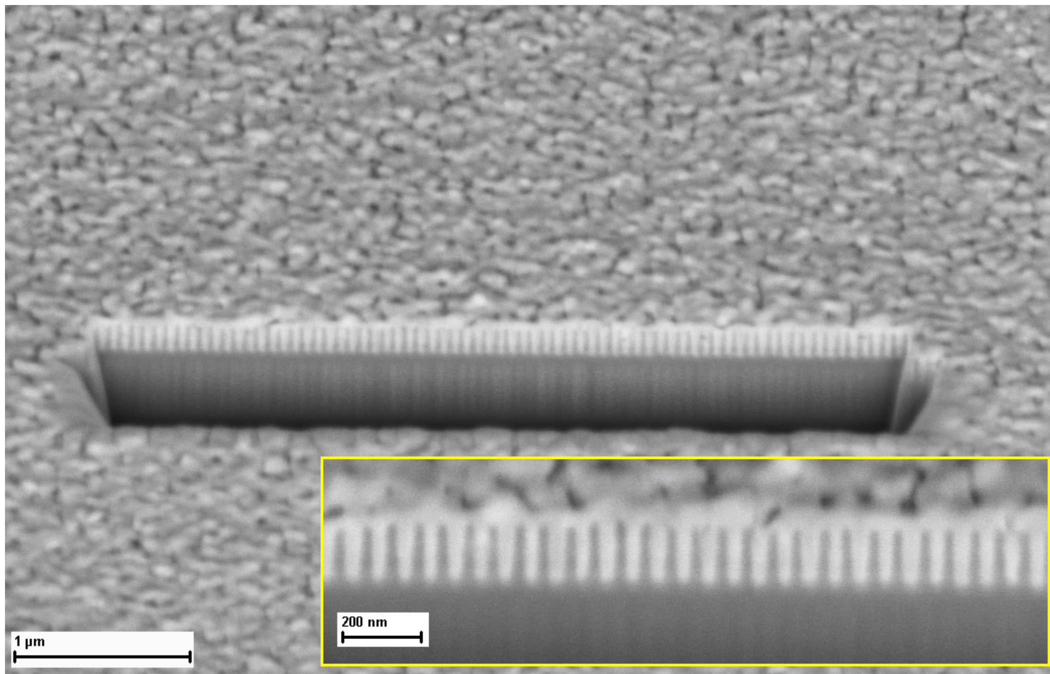

Figure 4.12 Cross sectional SEM showing superfilling of Cu-Mn alloy in trenches with width ~ 27 nm

TEM and EFTEM of a cross-section of a copper wire in a 25 nm trench feature are shown in Figure 4.13. The manganese nitride barrier and adhesion layer is deposited uniformly and conformally along the sidewalls of the trench. Narrow trenches can be completely filled by Cu-Mn alloy in a bottom-up fashion when a thin manganese nitride is used as the underlayer and

iodine is used as the surfactant catalyst. No voids or seams were observed along the centerline of the copper.

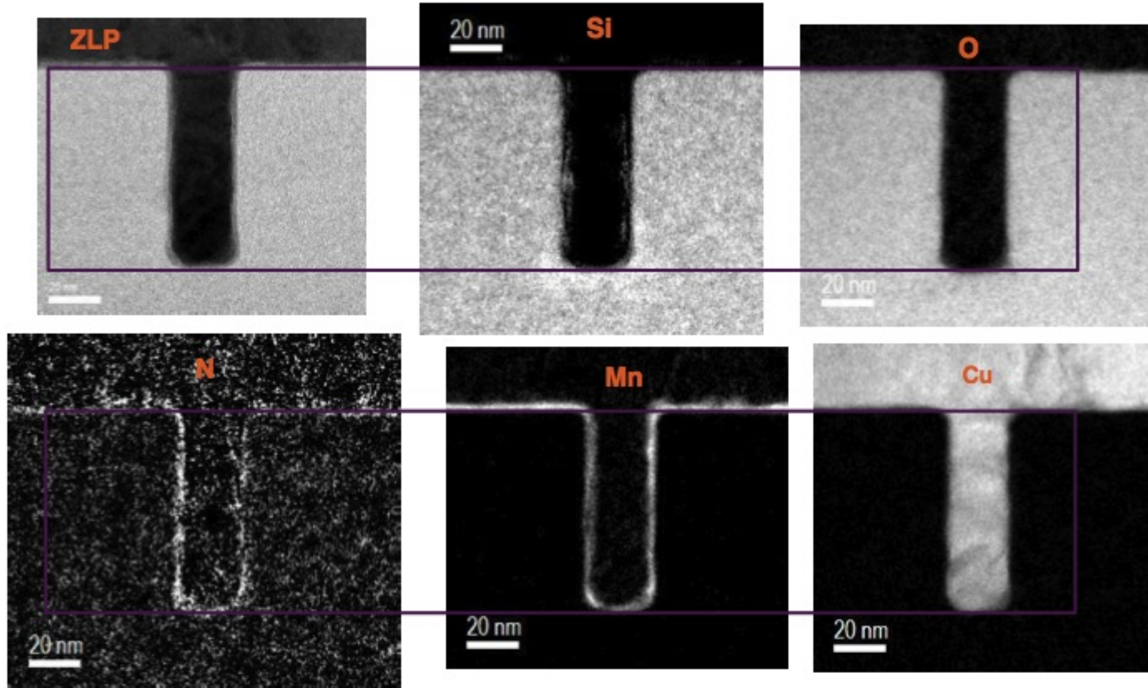

Figure 4.13 TEM and EFTEM of a cross-section of a Cu wire in a 25 nm trench feature (Substrate and image courtesy of IMEC)

Electrical Characterization of Narrow Trenches Filled with CVD of Cu-Mn Alloy

Figure 4.14 shows that, for the same Cu cross-sectional area considered, resistivity values (ρ = 3.19-3.55 μΩ-cm) measured on 25 nm trenches metallized by CVD Cu-Mn alloy with post-annealing are lower than values obtained with conventional PVD RuTa liner/electroplated Cu method. Low resistivity values suggest that residual manganese present in the copper layer after post-annealing is limited. ToF-SIMS analyses confirm that no other contaminants are detected in the copper layer (Figures 4.15). On one hand, this CVD Cu-Mn method incorporates less carbon, oxygen, and other impurities into the copper film than conventional electroplating methods,

which reduces impurity scattering. On the other hand, the post-annealing step following the CVD process promotes copper grain growth to reduce grain boundary scattering. These effects combined to result in lower resistivity values.

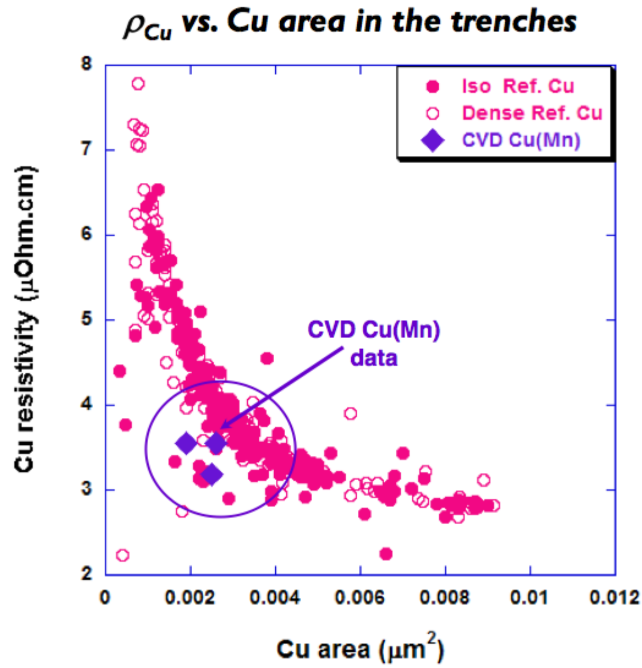

Figure 4.14 Resistivity measurements on trenches metallized by CVD Cu-Mn or by conventional PVD/plating method (Substrate, image, and data courtesy of IMEC)

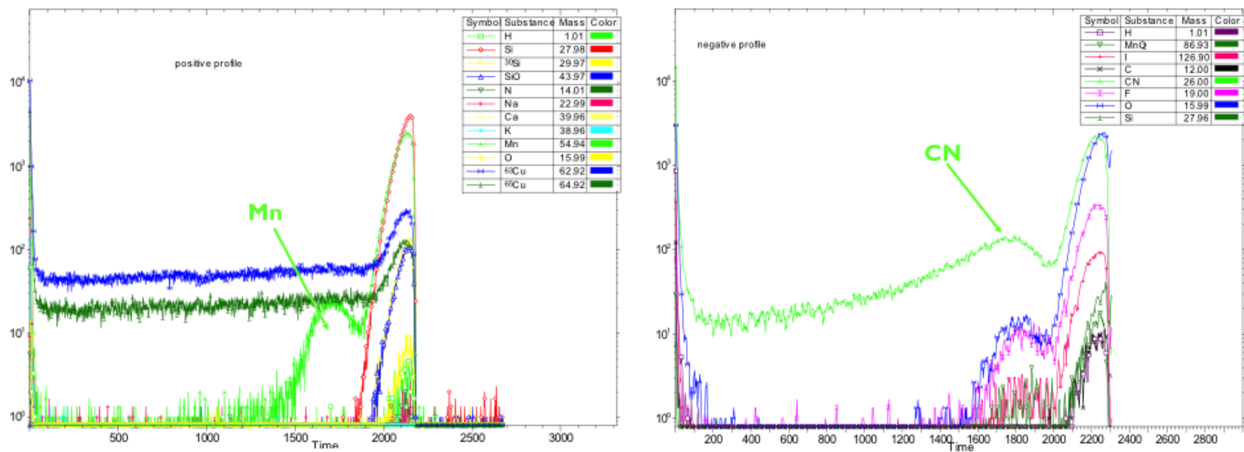

Figure 4.15 ToF-SIMS analysis: positive profile (left) and negative profile (right) showing low contaminant levels in Cu layers (Substrate and data courtesy of IMEC)

Removal of Iodine from Copper Surface

In a substrate with both narrow and wide trenches, the CVD steps may fill the narrow trenches, while conformally coating the wider trenches. Subsequent electroplating can then fill the wider trenches economically. A small amount of iodine (much less than a monolayer) may be attached to the copper surface at the beginning of the electroplating step. There is a possibility that this iodine could dissolve in the copper plating bath and cause corrosion or reliability problems later. Therefore it could be advantageous to remove the iodine from the copper surface prior to plating. Iodine on the surface can be removed by placing the CVD Mn_4N-CVD Cu substrate into a solution of 30% hydrogen peroxide-70% water for 1 minute at room temperature. It was then rinsed in ethanol and deionized water and dried. Examination of the surface by XPS showed that no iodine remained on the surface. Other oxidizing agents, such as sodium hypochlorite, may also be used to remove the iodine from the copper surface. Alternatively, iodine can also be removed by placing the CVD Mn_4N-CVD Cu substrate in a reactive ion-etch (RIE) system. It was first treated by an oxygen plasma with 150 watt microwave power and 50 watt RF power at 0.01 Torr pressure for 30 seconds at room temperature, followed by a hydrogen plasma with 150 watt microwave power and 50 watt RF power at 0.01 Torr pressure for 3 minutes at room temperature. It was then rinsed in ethanol and distilled water and dried. No iodine could be detected on the surface by XPS.

Metallization of Plastic Substrates

This surfactant-catalyzed CVD process can also be extended to metallization of various plastic substrates that are stable up to the deposition temperature of 180 °C. Thermally stable polyimide plastic sheet and fiberglass-reinforced circuit boards were selected for this study. After 20 minutes of manganese nitride deposition, 30 seconds of ethyl iodide exposure, and 40

minutes of copper deposition, the surfaces of the plastics were covered by electrically conductive copper films with sheet resistance around 0.5 ohms per square. The smooth surface of a polyimide plastic sheet remained smooth. The rough surface of a fiberglass-reinforced circuit board (root-mean-square roughness = 150 nm) was covered conformally, as shown in Figure 4.16. The copper adhered strongly to the plastics, and could not be removed by a tape test.

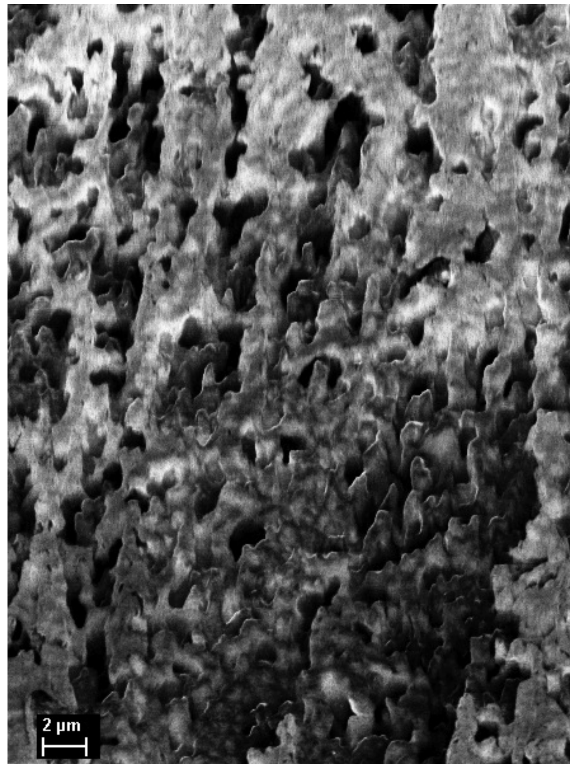

Figure 4.16 SEM of rough plastic circuit board material coated with Mn_4N and Cu

4.4 Conclusions

Narrow trenches, with widths narrower than 30 nm and aspect ratios up to at least 5:1, can be filled with copper or copper-manganese alloy by a CVD method using manganese nitride as an underlayer and iodine as a surfactant catalyst. Copper grows in these trenches in a bottom-

up fashion without leaving any voids or seams. Manganese in the alloy diffuses out at elevated temperature and forms a self-aligned barrier and adhesion layer to strengthen the Cu/dielectric interface. Using this bottom-up filling technique, narrow trenches can be completely filled with copper and wider trenches can be coated by a conformal copper-manganese seed layer for electroplating. Trenches metallized by this CVD Cu-Mn process have lower resistivity values than that obtained with conventional metallization methods, possibly due to reduction in impurity and grain boundary scattering. This CVD metallization process has the potential to increase the performance and lifetime of copper wires in future generations of microelectronics.

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Chapter 5

Conformal Copper Seed Layers for Plating Through-Silicon Vias (TSVs) by Vapor Deposition

5.1 Introduction

Metal interconnections in microelectronics have been typically fabricated in a planar, 2-dimensional (2-D) fashion. 3-dimensional (3-D) integration has gained a lot of interest as a way to enhance the performance of microelectronic systems.[1] 3-D integration has been shown to reduce the number and the average lengths of 2-D global wires by providing shorter vertical paths for connection. In addition, 3-D integration has the potential to further improve system performance and to enable new system architectures.[2] For example, 3-D integration can reduce energy consumption and extend the performance of high-speed transistors to future technology nodes where the global wires are expected to present serious delays. 3-D integration also offers the possibility to integrate dissimilar technologies, such as digital, analog, and radio-frequency (RF) functions, all in the same cube for system-on-a-chip (SoC) applications (Figure 5.1).

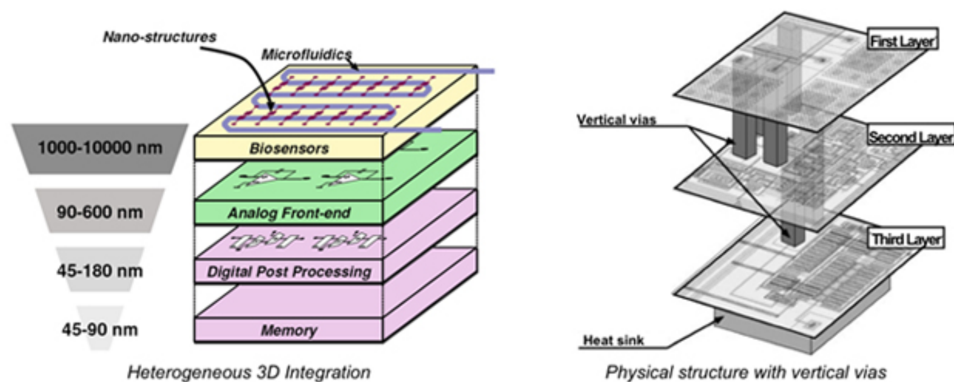

Figure 5.1 Schematic illustration of 3-D integration and system-on-a-chip application

(Source: The Internet)

Through-silicon vias (TSV) will provide faster interconnections between multiple dies in advanced 3D-packaging applications.[3] Metallization of TSVs will become more and more challenging as the aspect ratios of vias continue to increase. The 2010 International Technology Roadmap for Semiconductors (ITRS) calls for copper TSVs with aspect ratios of 10:1 by 2012 and 20:1 by 2015.[4] One critical step in the production of TSVs is the preparation of a continuous barrier that will keep metals from diffusing out from the vias. A smooth and conductive copper seed layer is also necessary to initiate copper electroplating. Strong adhesion must also be provided between the copper seed layer, the diffusion barrier and the underlying insulator. Due to their poor step coverage, conventional physical vapor deposition (PVD) methods will no longer to be able to cover the sidewalls of these high aspect ratio features with the necessary layers.[5]

In this chapter, a new method is introduced to make conformal, smooth and strongly adherent barriers and copper seed layers inside holes with aspect ratios greater than 25:1 by vapor deposition. A rapid ALD process is first applied to form a conformal insulating layer of silicon dioxide (SiO_2) inside the vias.[6] Next manganese nitride (Mn_4N), an effective copper diffusion barrier and adhesion layer, is deposited conformally on the silica surface by CVD. Iodine is then chemisorbed onto the surface of the thin manganese nitride layer to catalyze the CVD of smooth copper or copper-manganese alloy seed layers.[7] A direct-liquid-injection (DLI) CVD method is used to deliver consistent and high vapor concentrations of copper precursor and to coat the high aspect ratio holes with conformal copper or copper-manganese seed layers. A post-deposition annealing step diffuses manganese from the copper film to the surfaces of the insulators to further strengthen the copper/insulator interface by forming a self-aligned barrier and adhesion layer. Thus, TSVs are provided with conformal and smooth copper seed layers that

adhere strongly to a very thin diffusion barrier just inside the surface of the conformal silica insulator.

5.2 Experiments

Patterned silicon substrates with TSV features were obtained from Tokyo Electron (TEL) and Applied Materials (AMAT). These substrates were cleaned by a UV/ozone cleaner (Samco model UV-1, wavelengths = 185 nm and 254 nm) for 5 minutes at room temperature to remove organic contaminants from the substrates. An insulating layer of aluminum-doped silicon dioxide 20 nm thick was deposited by ALD, as described in an earlier report.[6] This rapid ALD process forms a highly conformal layer on silicon by reacting trimethyl aluminum (TMA) with tris(*tert*-butoxy) silanol [$(Bu^tO)_3SiOH$]. More than 12 nm of insulator can be deposited in each ALD cycle even in holes with aspect ratio greater than 50:1.[6] This silica layer can plug pores in the underlying insulator layer,[8] and creates a clean, uniform silica surface which promotes dense, uniform nucleation and growth of the films made by the subsequent CVD processes.

A schematic diagram of the CVD system is shown in Figure 5.2. The compound that serves as a precursor for manganese and manganese nitride is bis(*N*,*N'*-diisopropylpentylamidinato) manganese(II). The precursor for copper deposition is (*N*,*N'*-di-*sec*-butylacetamidinato)copper(I) dimer. To prepare manganese nitride by CVD, the manganese precursor was evaporated from the liquid in a bubbler at a temperature of 90 °C into a 60 sccm flow of highly purified nitrogen. 60 sccm of ammonia (NH_3) and an additional 60 sccm of purified nitrogen were mixed with the manganese precursor vapor just before entering the reactor held at a temperature of 130 °C and a pressure of 5 Torr, controlled by an MKS Baratron

pressure gauge coupled to an automatic throttle valve. After deposition of manganese nitride was complete, the substrate was cooled in the reactor in a flow of pure nitrogen in order to protect the manganese nitride film from oxidation. Ethyl iodide (CH_3CH_2I) was then used as an iodine source to adsorb iodine atoms onto the fresh surface of the manganese nitride film at room temperature. The liquid ethyl iodide was contained in a bubbler at room temperature and its vapor was fed directly into the reactor without a carrier gas, controlled by a needle valve to a pressure of 0.05 Torr. Conventionally, the copper precursor was evaporated from the liquid in a bubbler at a temperature of 130 °C into a 40 sccm flow of highly purified nitrogen.[7]

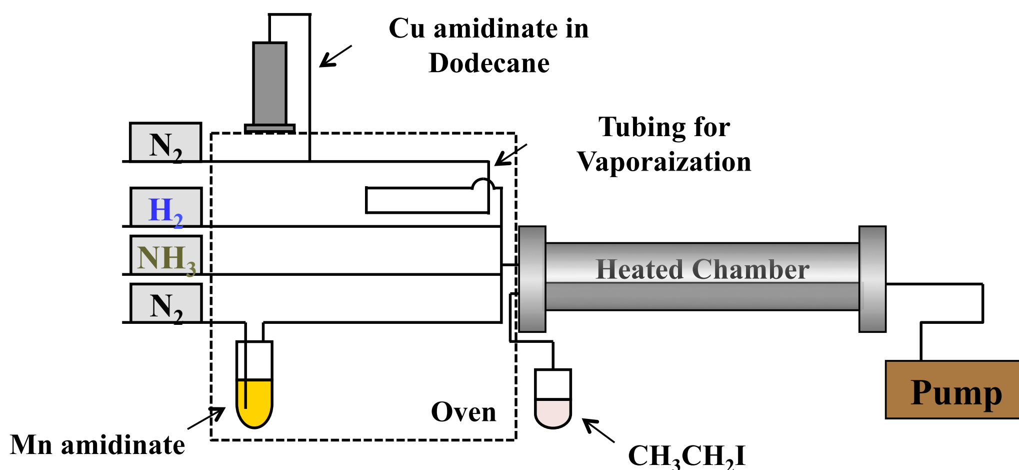

Figure 5.2 Schematic diagram of the DLI-CVD system

A direct-liquid-injection (DLI) CVD method was adopted instead to provide consistently higher partial pressure of copper precursor vapor, thereby enhancing the growth rate and the conformality of the copper films. To prepare copper films using the DLI-CVD method, 25 g of copper precursor was first dissolved in 100 mL of dodecane ($C_{12}H_{26}$), a solvent with vapor pressure close to that of the copper precursor, to make a solution with a concentration of 0.72 molal or 0.43 molar and a density of 0.79 g/mL, measured at 21 °C. T. The saturated solubility of the copper precursor in dodecane was determined to be ~ 1.3 molar. The precursor solution was

kept at room temperature in a stainless steel syringe sealed by 2 O-rings. The flow of the precursor solution was controlled by a syringe pump (KD Scientific model 210) at flow rates from 0.05 to 0.1 cm^3/min. The precursor solution was mixed with 40 sccm of nitrogen carrier gas at room temperature in a tee, from which the precursor solution was vaporized while flowing down into a coil of stainless steel tubing (1.8 m long, 1/4 inch outside diameter) kept at 160 °C in an oven.[9] Completeness of the vaporization process can be checked by inserting a glass viewport into the lowest point at the end of the tubing, to make sure that no liquid collects there. An oven temperature of 120 °C was found to be too low to completely evaporate the liquid, while 160 °C was sufficiently high to evaporate all the liquid at the flow-rates used. The vapor mixture exiting from this tubing was then mixed at a tee with 100 sccm of hydrogen just before entering the reactor held at a temperature of 180 °C and a pressure of 5 Torr. Under these conditions, the injection rates of copper precursor, dodecane, hydrogen (100 sccm) and nitrogen (40 sccm) are 3.6×10^{-7} mol s^{-1}, 2.9×10^{-6} mol s^{-1}, 7.4×10^{-5} mol s^{-1}, and 3.0×10^{-5} mol s^{-1}, respectively, for a total vapor and gas injection rate of 1.1×10^{-4} mol s^{-1}. Based on these flow rates, the mole fraction of copper precursor in the total gas plus vapor flow is 0.0033. The reactor is held at a total pressure of 5 Torr, so the partial pressure of copper precursor vapor inside the reactor is 0.017 Torr, and the partial pressure of hydrogen gas is 3.4 Torr. If manganese was to be co-deposited with the copper, a flow of 60 sccm of purified nitrogen gas was passed through the manganese bubbler at 90 °C. This flow of manganese precursor vapor in nitrogen was mixed with copper precursor vapor just prior to entering the deposition zone.

In a typical CVD process to form copper seed layers in TSV features, ~ 20 nm of silica layer was first deposited by ALD at 250 °C to insulate the metal from silicon. Manganese nitride was then deposited at 130 °C for 5 minutes to form 2.5 nm of film. Ethyl iodide was then

introduced into the chamber at room temperature for 30 seconds. Copper or copper-manganese alloy was finally deposited at 180 °C until a sufficiently conductive layer (sheet resistance below 0.8 ohms per square) was formed in the vias, which typically took around 10 minutes. The Mn/Cu ratio was quantified by X-ray fluorescence (XRF). A post-deposition annealing step at 350 °C for one hour in nitrogen ambient was carried out after the iodine-catalyzed CVD process to diffuse the manganese from the copper-manganese alloy to the copper/insulator interface. The conformality of the Mn_4N and the copper seed layers were evaluated by scanning electron microscopy (SEM). A thicker Mn_4N layer was deposited for 100 minutes so that its conformality could be observed more clearly by SEM. The surface morphology of the copper seed layer was studied by atomic force spectroscopy (AFM). The sheet resistance of the films was measured by a four-point probe.

5.3 Results and Discussion

Deposition of Barrier and Adhesion Layer

A conformal layer manganese nitride film can be prepared by CVD at 130 °C in holes with aspect ratios of 26:1. A thick (95 – 100 nm) Mn_4N layer is shown in Figure 5.3 to demonstrate conformal deposition. The effective aspect ratio of the holes is much greater than 26:1 as the diameter of the holes is narrowed during the course of deposition. The defect in the bottom of the via is caused by damage during the hand-cleavage of the sample. The polycrystalline manganese nitride film is conductive, with a resistivity value of 198 mΩ-cm. Annealing the manganese nitride film at 200 °C for one hour promotes the formation of larger grains and results in a lower resistivity value of 2.01 mΩ-cm. It is possible to prepare conformal

manganese nitride films at higher substrate temperatures, but the flow rate of NH_3 must then be decreased to prevent fast surface reactions, which lead to poor conformality. For example, vias with aspect ratios up to 50:1 can be coated with conformal Mn_4N using NH_3 and H_2 flow rates of 5 and 55 sccm, respectively, at a substrate temperature of 180 °C. Surface reactivity may also be lowered by choosing a manganese amidinate precursor with bulkier ligands, such as *tert*-butyl groups, attached to the nitrogens in place of the smaller isopropyl groups. Manganese nitride films as thin as 2.5 nm form barriers against copper diffusion.[7] A four-point bend method was used to evaluate the adhesion between silica and the later-deposited CVD of copper, and the debonding energies were found to be greater than 6.5 J m^{-2}, which is high enough to survive further fabrication by chemical-mechanical polishing.[4,7,10,11]

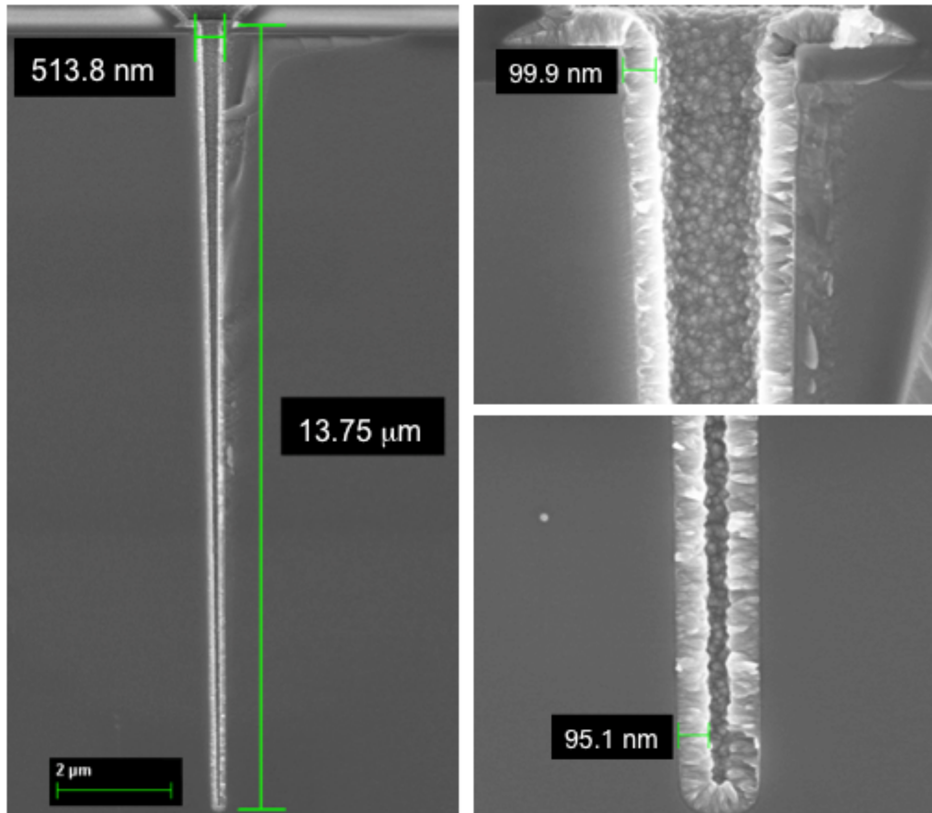

Figure 5.3 Cross-sectional SEM image showing highly conformal step coverage of manganese nitride underlayer in vias with aspect ratio 26:1

Deposition of Seed Layer

When vapors of ethyl iodide are exposed to manganese nitride films, iodine atoms are chemisorbed onto the surface. During subsequent CVD of copper, the iodine desorbs from the Mn_4N surface and floats to the surface of the growing copper film. The presence of iodine atoms may weaken the bond between copper and its ligands and facilitate the dissociative chemisorption of the precursor on the copper surface,[12] resulting in the enhancement of the growth rate and surface smoothness of the copper films.[7,13]

Smooth and continuous copper seed layers can be deposited by vaporizing the copper precursor from a conventional bubbler. TSV via features with aspect ratios up to 4.6:1 can be conformally coated with a copper seed layer. Vias with aspect ratio up to 10:1 can be conformally coated by increasing the copper precursor carrier gas to 100 sccm and the working pressure to 10 Torr, both of which changes increase the partial pressure of the copper precursor inside the deposition region. This conventional bubbler delivery of precursor vapor, however, fails to form a continuous copper layer in the bottoms of vias with aspect ratios beyond 10:1 due to insufficient concentration of precursor vapor, especially for substrates with extremely high via density (9×10^6 holes cm^{-2}).

The direct-liquid-injection (DLI) method delivers a much higher partial pressure of the precursor vapor than vaporization from conventional bubblers. By supplying a high concentration of copper precursor vapor, the deposition is operating in the surface reaction-controlled regime. At deposition temperatures around 180 °C, slow surface reactions permit a uniformly high concentration of precursor vapor to be delivered to the entire length of the vias. As a result, continuous and highly conformal copper-manganese films are deposited on

manganese nitride underlayers inside via holes with aspect ratio over 26:1 (Figure 5.4). The vapor delivery rate from the DLI system is stable, reproducible and accurately known because the concentration of the solution and the liquid and carrier gas injection rates are known and steady. In contrast, the vapor delivery rate from a conventional bubbler is subject to uncertainty in vapor pressure, temperature variation, thermal decomposition, and effects of fill level.

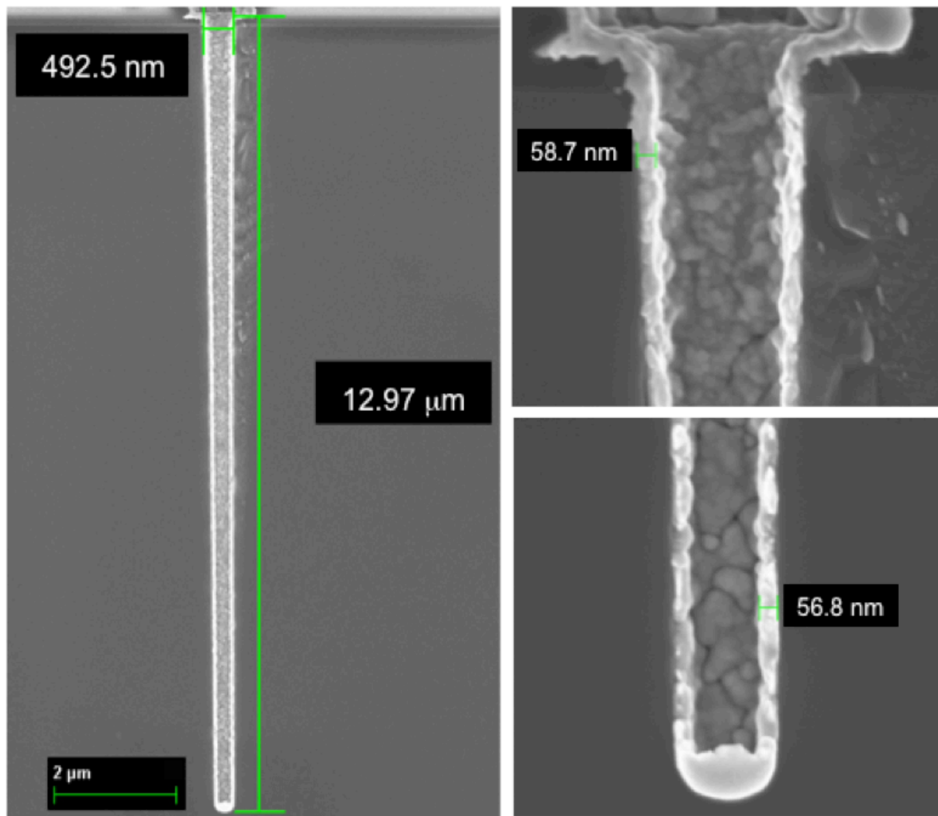

Figure 5.4 Cross-sectional SEM image showing highly conformal step coverage of Cu-Mn seed layer in vias with aspect ratio 26:1

Cross-section SEM and AFM images of a thicker copper film on a planar substrate show that the copper seed layer deposited on an iodine-exposed manganese nitride underlayer is fairly smooth, with a root-mean-square roughness equal to 6.2% of its thickness (Figures 5.5). Manganese content in the copper-manganese alloy was analyzed by XRF to have approximately

0.5 atomic % of manganese in copper. Adjusting the temperature of the manganese precursor bubbler or the flow rate of the nitrogen carrier gas through the bubbler can vary the concentration of manganese in the alloy film.

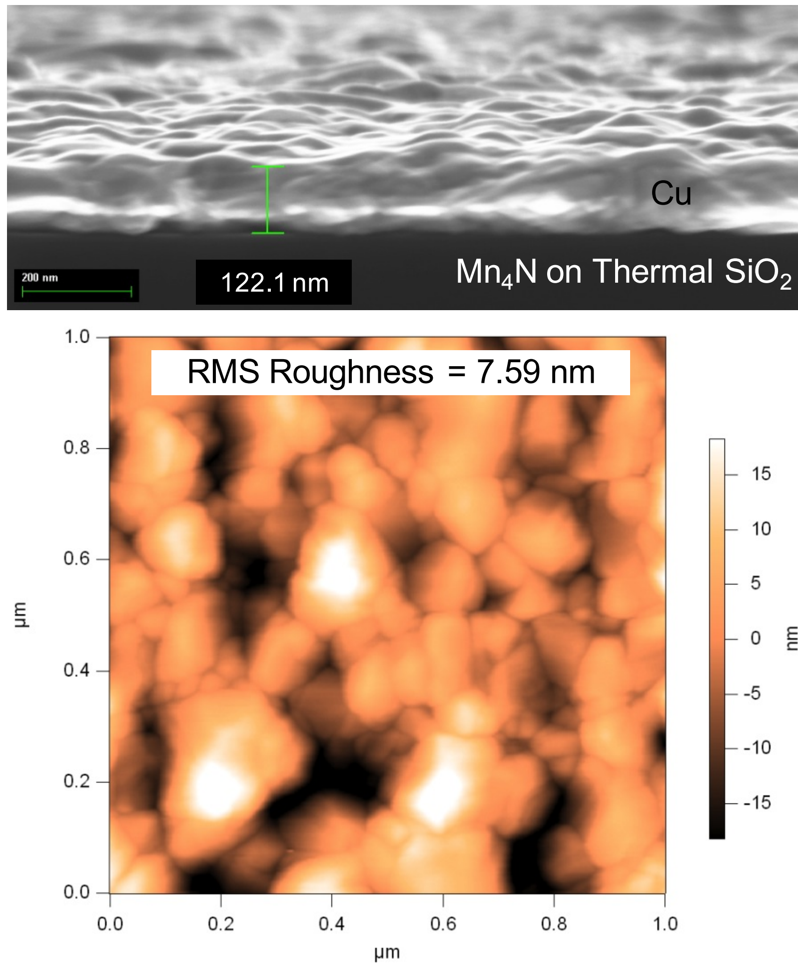

Figure 5.5 AFM image measuring a RMS roughness equals to 6.2% of the thickness of the Cu seed layer

A post-deposition annealing step at 350 °C is incorporated to diffuse the manganese from the copper-manganese alloy to the copper/insulator interface and to return the resistance of the copper seed layer to a lower value. Chapter 3 showed that manganese diffuses through the grain boundaries of the polycrystalline copper, and this diffusion process enhances the interfacial adhesion between copper and insulators such as silicon oxide, silicon nitride and low-*k* dielectric.

While manganese nitride provides sufficient adhesion energy to survive chemical-mechanical polishing, presence of additional manganese in the seed layer can further strengthen the copper/insulator interface and to potentially achieve longer electromigration lifetime.[14] The debonding energy increases approximately linearly with the manganese content at the interface, up to values beyond 14 J m^{-2}.[11] The resulting self-aligned interfacial layer, manganese silicate ($MnSi_xO_y$), forms within a few nm of the surface of the insulator, and is an excellent barrier to diffusion of copper,[15,16] oxygen and water.[15] By diffusing the manganese out from the copper-manganese alloy film, the sheet resistance is determined to be 0.46 ohms per square for the copper seed layer shown in Figure 5.4, which is sufficiently conductive for the later electroplating step (< 0.8 ohms per square). The resistivity of this seed layer is about 2.69 mΩ cm, which is about the resistivity expected for a pure copper layer 58 nm thick.[17] It is also possible to carry out the annealing step after the electroplating of copper to diffuse manganese in the seed layer to the Cu seed/electroplated Cu interface, thereby preventing delamination of the plated Cu film from the seed layer.

Preliminary Electroplating Results

TSV features with aspect ratio of 25 to 1 supplied by Applied Materials were conformally coated with approximately 90 nm of Cu-Mn alloy seed layer as shown in Figure 5.6. Preliminary copper electroplating studies were carried out on these substrates at Dow Chemical Company, following the Interlink^{TM} 9200 TSV Chemistry. A vacuum/immersion “PreWet” step was introduced prior to plating to expel air in the vias and to wet the seed layer. The plating solution contained copper sulfate ($CuSO_4$)/sulfuric acid (H_2SO_4)-based electrolytes and additives, including an accelerator, a suppressor, and a leveler, to achieve bottom-up filling and to control

the morphology of the electroplated copper. As shown in Figure 5.7, void-free TSV filling was achieved across all sections of the via arrays after 30 minutes of electroplating.

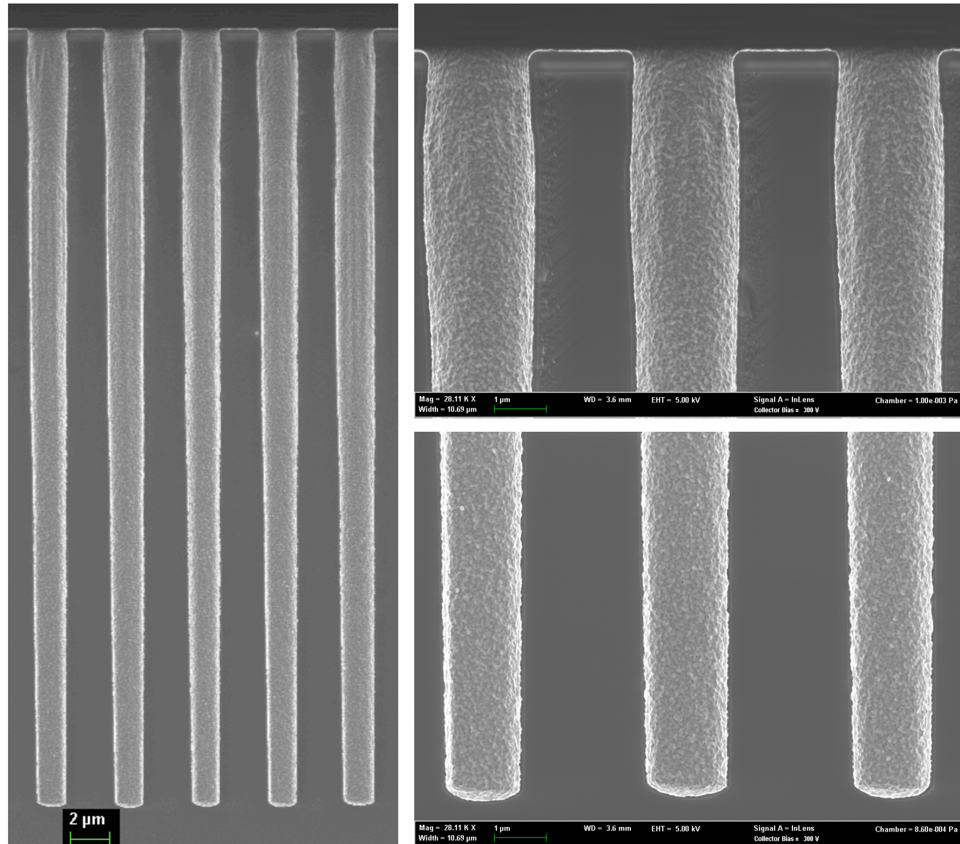

Figure 5.6 Dense AMAT TSV structures (aspect ratio = 25:1) coated by Mn_4N liner and Cu-Mn seed layer

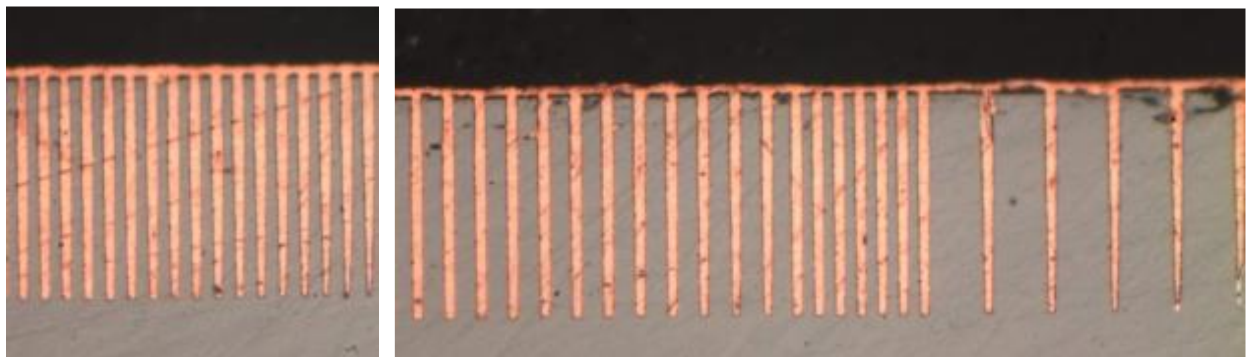

Figure 5.7 Cross-sectional images demonstrating complete filling of high aspect ratio TSVs

5.4 Conclusions

Conformal and conductive copper seed layers for metallization of TSVs were successfully prepared in high aspect ratio holes by DLI-CVD. A conformal insulator layer was first deposited by ALD to separate the metal from the substrate silicon, and a manganese nitride liner layer was then deposited on the insulator. The CVD process was catalyzed by iodine as a catalytic surfactant to achieve higher growth rate and smoother morphology. The DLI-CVD method enhanced the delivery of precursor vapors even to the bottoms of dense arrays of vias and resulted in nearly perfect conformality. The presence of manganese at the copper/insulator interface further improves the adhesion and barrier properties at the interface. This process forms a highly robust and conductive seed layer for metallizing future generations of copper vias in advanced 3-D integration. TSV features with aspect ratio of 25 to 1 can be completely filled using a commercial electroplating process.

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Chapter 6

Conclusions and Future Work

6.1 Conclusions

Chemical vapor deposition (CVD) has the ability to achieve conformal coating and can be applied economically on a large scale to metallize future generations of microelectronic devices. A CVD method is presented in Chapter 2 to make conformal self-aligned manganese silicate ($MnSi_xO_y$) diffusion barrier. This $MnSi_xO_y$ layer is an effective barrier to diffusion of copper, oxygen and water. Because the $MnSi_xO_y$ is formed within the insulator, it does not occupy the volume reserved for copper, as happens with conventional Ta/TaN barriers. Also, the CVD Mn dissolves into copper surfaces, such as at the tops of vias, so no resistive barrier exists between the tops of vias and the copper in the next higher level. This CVD process can also be used to strengthen the interfacial bonding between copper and a capping barrier layer of SiCNOH. Thus, more conductive and more durable interconnections are possible using the self-aligned $MnSi_xO_y$ barriers. This process, together with the CVD CuON process, should allow formation of conformal seed layers for void-free electroplating of copper in even the narrowest interconnects.

A selective CVD manganese capping process is presented in Chapter 3 to strengthen the interface between copper and dielectric insulators without increasing the resistivity of the copper. The presence of manganese metal at the interface between copper and insulators is shown to increase the adhesion strength dramatically. The debonding energy increases approximately linearly with the amount of manganese at the interface. This selective CVD process deposits the

manganese only on copper surfaces while completely avoiding any deposition on adjacent silylated surfaces of insulators, such as silica or SiOC low-*k* dielectrics. This process has the potential to increase the lifetime of copper wires in microelectronics without any increase of resistance due to capping metal between levels of interconnects. At the same time, the process can reduce the capacitance and increase the speed of interconnects by eliminating the need for a high-*k* diffusion barrier on top of each level of wiring.

A surfactant-catalyzed CVD process for the bottom-up filling of narrow trenches with copper or copper-manganese alloy is presented in Chapter 4. Trench features, with widths narrower than 30 nm and aspect ratios up to at least 5:1, can be filled with copper or copper-manganese alloy using manganese nitride as an underlayer and iodine as a surfactant catalyst. Copper grows in these trenches in a bottom-up fashion without leaving any voids or seams. Manganese in the alloy diffuses out at elevated temperature and forms a self-aligned barrier and adhesion layer to further strengthen the Cu/dielectric interface. Using this bottom-up filling technique, narrow trenches can be completely filled with copper and wider trenches can be coated by a conformal copper-manganese seed layer for electroplating. Trenches metallized by this CVD Cu-Mn process have lower resistivity values than that obtained with conventional metallization methods, possibly due to reduction in impurity and grain boundary scattering. This metallization process has the potential to increase the performance and lifetime of copper wires in future generations of microelectronics.

A direct-liquid-injection (DLI) CVD process is introduced in Chapter 5 to make conformal, smooth and strongly adherent barriers and copper seed layers inside through-silicon vias with aspect ratios greater than 25:1. A conformal insulator layer was first deposited by ALD to separate the metal from the substrate silicon, and a manganese nitride liner layer was then

deposited on the insulator. The CVD process was catalyzed by iodine as a catalytic surfactant to achieve higher growth rate and smoother morphology. The DLI-CVD method enhanced the delivery of precursor vapors even to the bottoms of dense arrays of vias and resulted in nearly perfect conformality. The presence of manganese at the copper/insulator interface further improves the adhesion and barrier properties at the interface. This process forms a highly robust and conductive seed layer for metallizing future generations of copper vias in advanced 3-D integration. TSV features with aspect ratio of 25 to 1 can be completely filled using a commercial electroplating process.

6.2 Future Work

Cross-section TEM and Electrical Characterization of Narrower Features

The surfactant-catalyzed CVD process discussed in Chapter 4 can fill trenches with widths as narrow as 18 nm in a bottom-up fashion (Figure 6.1). Cross-section TEM and elemental analyses conducted at IMEC revealed a uniform and continuous layer of manganese nitride barrier/adhesion layer, and the features were completely filled by copper without leaving voids or seams. Chemical mechanical polishing (CMP) and electrical characterization were successfully performed at IMEC. Copper wires prepared by the surfactant-catalyzed CVD method showered low resistivity values, possibly due to reduction in impurity level and in grain boundary scattering. Because of these advantages, the CVD method is a promising candidate for the metallization of future generation of interconnects. Even narrower features, with widths less than 10 nm, can be prepared by depositing thin layers of ALD silica films to narrow the trench structures. These test structures can be used to evaluate the super-filling capabilities of the

surfactant-catalyzed CVD method. The newly developed Total Release FIB Process at Harvard Center for Nanoscale Systems (CNS) is an automated cross-section TEM sample preparation technique that enables local evaluation of these filled features.

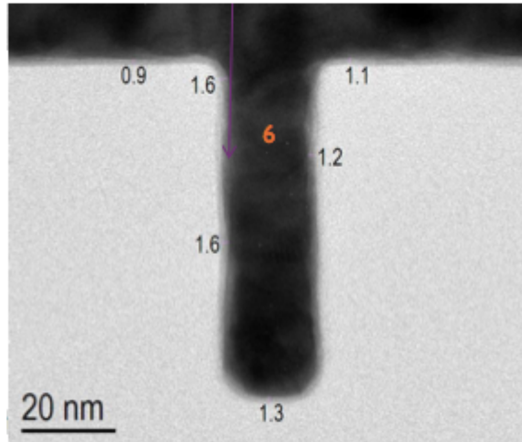


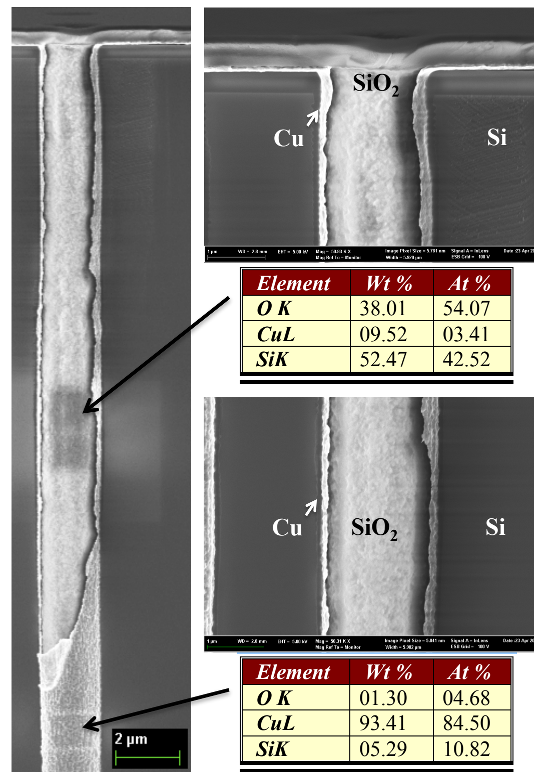
Figure 6.1 Cross-section TEM showing 18 nm trench feature filled by CVD of Cu

Electroplating on Copper-Manganese Seed Layers in High Aspect Ratio TSVs

The vapor deposition method discussed in Chapter 5 has the ability to coat high aspect ratio TSV structures with a continuous (> 20 nm at all location) and conductive (sheet resistance < 0.8 Ω/sq.) layer of copper-manganese alloy seed layer. Preliminary copper electroplating tests were carried out at IMEC and Dow Chemical Company. At IMEC, TSV features with aspect ratio of 10:1 were successfully electroplated in a commercially available alkaline plating bath, which contains a copper complexing agent, a copper ion source, and a *p*H adjuster.[1] Continuous and conformal copper coverage was observed everywhere along the vias after a partial fill. More studies, including methods to improve the interfacial adhesion and to reduce the hydrogen release rate during electroplating[2], may be necessary to prevent delamination and blister formation while plating higher aspect ratio TSV structures. At Dow, TSV features with aspect ratio of 25 to 1 were completely filled using a commercial plating bath with copper

sulfate/sulfuric acid as electrolytes and organic additives, including an accelerator, a suppressor, and a leveler, to control the growth rate and the morphology of the electroplated copper. High-resolution imaging as well as chemical and electrical characterization of these filled features should be carried out locally.

Fabrication and Electrical Characterization of Annular TSVs



Element	Wt %	At %
O K	38.01	54.07
CuL	09.52	03.41
SiK	52.47	42.52

Element	Wt %	At %
O K	01.30	04.68
CuL	93.41	84.50
SiK	05.29	10.82

Figure 6.2 High aspect ratio TSV features coated by CVD-CuMn seed layer and filled with ALD-SiO_2

TSV of various structures, such as cylindrical, annular, and co-axial, have been considered and fabricated in recent years. While conventional cylindrical TSV outperforms in thermal dissipation and signal propagation in DC and low frequency applications, annular TSV has several attractive features including improved thermo-mechanical reliability and compatible fabrication process with conventional structures.[3] It may be worthwhile to investigate the

possibility of building annular TSV that can be combined with cylindrical TSV as a solution to improve the overall system performance. Following the insulator/barrier/seed layer deposition process described in Chapter 5, proper dielectric materials, such as silicon dioxide (Figure 6.2) or benzocyclobutene (BCB) polymer, can be used to fill the hole to alleviate the thermal stress inside the TSV and to improve the electromigration reliability of the structure. The copper seed layer can be used as the conducting layer of the annular TSV. Resistance, self-inductance, and other electrical properties of the annular and cylindrical TSVs in DC, low and high frequency applications should be characterized and compared.

Iodine-catalyzed CVD of Copper on Ruthenium Adhesion Layers

Ruthenium has been proposed to be an excellent liner material for future interconnects due to its high electrical conductivity and low solid solubility with copper.[4] Catalyst-enhanced CVD of copper on ruthenium layer has been demonstrated using diiodomethane as the iodine source and hexafluoroacetylacetonate-copper-vinyltrimethylsilane as the copper precursor.[5] When copper amidinate was used as the precursor, exposing vapors of ethyl iodide to the surface of ruthenium in the presence of hydrogen resulted in a 6.5-fold enhancement in the growth rate of copper at 180 °C. This hydrogen-assisted iodine exposure process is believed to promote decomposition of ethyl iodide into iodine and volatile hydrocarbon compounds and therefore allows adsorption of iodine on ruthenium surface without leaving carbon contamination. Incorporation of hydrogen or ammonia into the iodine exposure step may allow higher temperature treatments without thermally decomposing the alkyl iodide compounds, which can inhibit copper deposition. Super-filling behavior of narrow trench features that use ruthenium as the adhesion layer should be studied as the surfactant-catalyzed CVD method may also promote void-free filling in these features.

Metallization on Transparent Conductors for Solar Cell Applications

Low resistivity metals, such as silver and aluminum, are attractive choices for front contacts on semiconductors for solar cell or display applications. Copper-based metal are also suitable candidates for these applications due to their low resistivity and abundance, but additional process steps are required for adhesion-assistance, diffusion barrier and electrical contact-assistance.[6] Preliminary studies on copper-manganese alloy as front contact material suggested that Cu-Mn might be able to simultaneously achieve low resistivity and high reliability. As described in Chapters 2 and 3, copper-manganese alloy formed a self-aligned diffusion barrier layer on glass and silica substrate upon post-annealing. Diffusion of manganese from copper to copper/oxide interface enhanced the interfacial adhesion and decreased the resistivity of the metal layer.

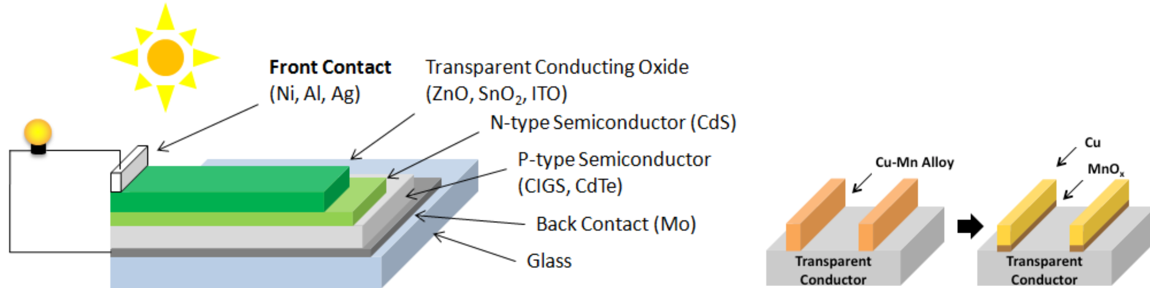


Figure 6.3 Structure of a solar cell (left) and Cu-Mn alloy as front contacts on transparent conductors (right)

To metallize zinc oxide (ZnO), a commonly used transparent conductor, a thin layer of Cu was first deposited to fully cover the surface of the oxide, followed by a brief exposure of ethyl iodide vapors, followed by a longer deposition of Cu-Mn alloy to form ~ 1.5 – 2.0 atomic % of Mn in 60 nm of Cu. Alloy film prepared by this process would partially peel off during the tape test due to weak adhesion at Cu/oxide interface. Upon post-annealing at 350 °C for one hour, manganese diffused out from the copper layer to decrease the sheet resistance of

the film by 34% and to provide sufficient interfacial adhesion strength to pass the tape test. Ohmic contact behavior was confirmed by IV characterization. Like other strong reducing metals, manganese in the Cu-Mn alloy reacts strongly with ZnO upon annealing, leading to a continuous n-type (high concentration of oxygen vacancy) layer to bring about the good Ohmic behavior.[6] The same CVD process, however, did not deposit any Cu-Mn alloy film on tin oxide (SnO_2). To initiate copper growth, a thin layer of manganese nitride layer was first deposited on SnO_2. Formation of manganese nitride was found to be much less surface-sensitive. As a result, the surfactant-catalyzed process could be performed and Cu-Mn alloy film could be deposited. Specific contact resistance should be characterized to decide if Cu-Mn alloy is a suitable material to metallize transparent conductors. Patterning techniques, such as lithography, inkjet printing, or selective surface passivation, should also be investigated to place copper on desired locations of the cell.

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Appendix I. CVD Reactor Operation Guide and Detailed Experimental Description of the CVD Processes

Figure I-1 DLI-CVD Reactor

This CVD reactor is built to prepare diffusion barriers ($MnSi_xO_y$), adhesion layers (MnN_x), and metal seed layers (Cu and Cu-Mn alloy) for the metallization of advanced microelectronic devices. The manganese amidinate precursor is contained in a commercial bubbler, and the copper amidinate precursor is dissolved in an alkane solvent (typically dodecane or tetradecane) to form a ~ 0.7 molal solution and is contained in a stainless steel syringe. A source of ethyl iodide is attached to the system and is used to catalyze Cu deposition and to achieve bottom-up filling of narrow features. Sources of self-assembling monolayers could also be attached to the system to achieve selective deposition. A schematic diagram of the reactor is shown below in Figure I-2.

The flow rates of the nitrogen (N_2) carrier gas and the co-reactant gases (H_2, NH_3) are precisely controlled by the mass flow controllers (MFC) #1-5 (Table I-1). The flow rates could be adjusted by turning the knobs in the MFC controller using a small screwdriver.

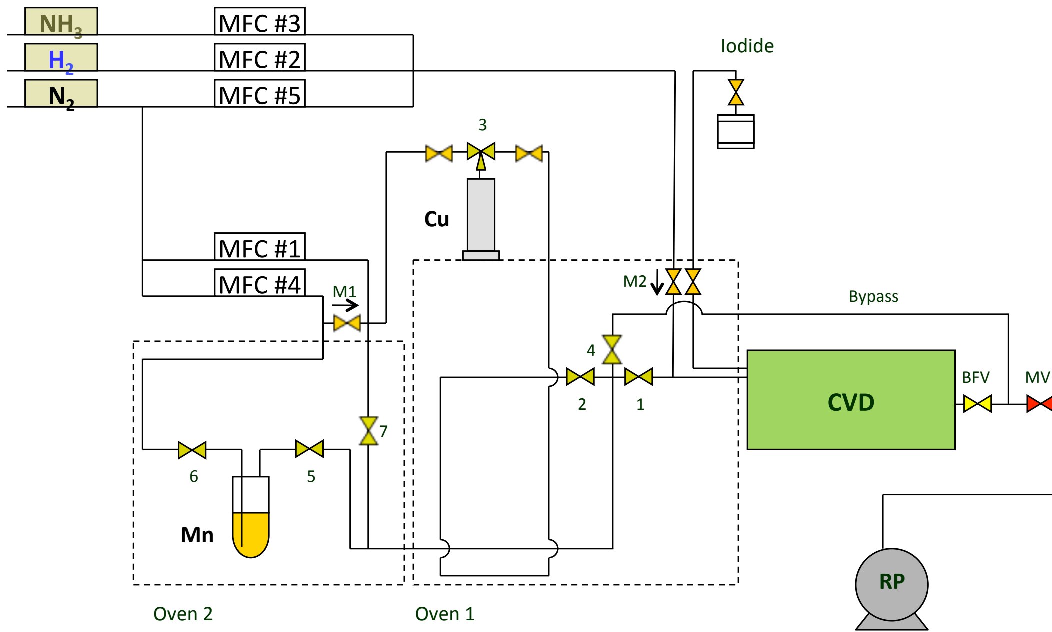

Figure I-2. Schematic Diagram of the DLI-CVD Cu & Mn System

Table I-1

MFC Number	Gas
1	Nitrogen (N_2) carrier for Cu precursor
2	Hydrogen (H_2)
3	Ammonia (NH3)
4	Nitrogen (N_2) carrier for Mn precursor
5	Nitrogen (N_2) assist

The inlet and outlet of the Mn bubbler, the outlet of the Cu syringe line, and the entrance and exit of the tubing for vaporization of the Cu precursor are all controlled by ALD valves (#1-7) using the LabView program. When the reactor is not in use, valves #1 and #7 are usually open

to purge the system, and 100 sccm of N_2 is supplied by turning on MFC #1 (usually set at 40 sccm) and #5 (usually set at 60 sccm). All other valves and MFCs should be turned off.

The pressure controller works together with the baratron gauge and the butterfly valve to maintain a constant operating pressure during deposition. Most of the processes described in this operation guide have an operating pressure of 5 Torr (set point B on the pressure controller).

The Mn bubbler is placed in oven 2, and tubing in oven 1 allows the Cu precursor solution to vaporize. In addition to the two ovens, there are additional thermal controllers to control the temperature of the gas pre-heat line (TC 1), the area between oven 1 and the furnace (TC 2), the area near the exit of the furnace (TC 3), the areas immediately before the pump line (TC 4 and 5) to avoid condensation of unreacted precursors, and the substrate holder (TC 6) to create a temperature gradient, as shown below in Figure I-3.

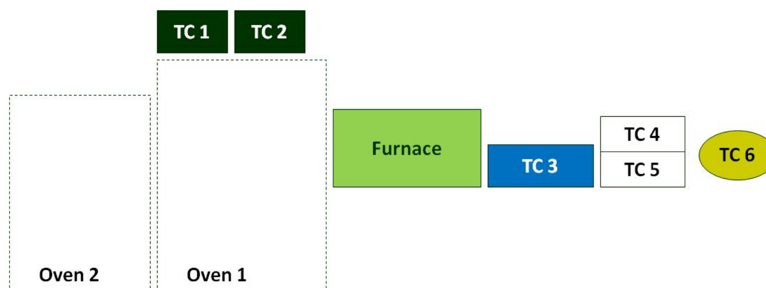

Figure I-3. Location of the Thermal Controllers

Experimental details of the CVD processes are presented in the following section:

CVD Mn Process

Metallic Mn can be deposited on Cu underlayer to form Cu-Mn alloy. Mn can also be deposited on SiO_2 surfaces to form manganese silicate ($MnSi_xO_y$), an amorphous insulator that is found to be an excellent diffusion barrier.

Temperature settings:

Table I-2

Temperature Controller	Temperature Set Point (ºC)
Oven 2 (Mn Bubbler Temperature)	90-120*
Oven 1 (Cu)	120
TC 1	110
TC 2	120
Furnace (Deposition Temperature)	300-350**
TC 3	120
TC 4	110-140
TC 5	110-140
TC 6 (Substrate Holder Heater)	Turn ON to the mark

* Sufficient vapor delivery is usually obtained at 90 ºC, bubbler temperature can be increased to up to 120 ºC (without decomposing the precursors) to achieve higher precursor vapor pressure and deposit rate.

** A deposition temperature of 300 ºC is typically used, together with 60 sccm of hydrogen flow, to deposit metallic Mn on Cu underlayer to form Cu-Mn alloy. A deposition temperature of 350 ºC is typically used, together with 60 sccm of nitrogen assist flow (no hydrogen), to deposit Mn on SiO_2 to form $MnSi_xO_y$ barrier layer.

Heat up time: 1 hour

Operating Procedure

- Leave only MFC #4 (**60 sccm**) on
- Leave ALD valve #1 on, turn off ALD valve #7
- Turn on ALD valve #5, then turn on ALD valve #6 to start Mn precursor flow
- Turn on MFC #2 (**60 sccm**) to start hydrogen flow to deposit Mn on Cu underlayer, **or** turn on MFC #5 (**60 sccm**) to start nitrogen assist flow to deposit Mn on SiO_2
- Set **Operating Pressure = 5 Torr** (set point B)
- **Typical deposition time = 5-30 minutes**, depending on the purpose of deposition
- Upon finish, set pressure controller to OPEN
- Turn off MFC #2 or MFC #5 to terminate hydrogen or nitrogen assist flow
- Turn off ALD valve #6, then turn off ALD valve #5 to terminate Mn precursor flow
- Turn on ALD valve #7 to start purging

Turn off all temperature controllers, oven, and furnace heaters (allow up to 1 hour to cool down)

CVD MnN_x Process

MnN_x can be prepared by supplying both Mn precursor and ammonia, it is found to be a barrier against copper diffusion at elevated temperatures and an adhesion layer that enhances the bonding at the copper/oxide interface. MnN_x also serves as the underlayer that chemisorbs iodine atoms to catalyze CVD Cu or Cu-Mn depositions.

Temperature settings:

Table I-3

Temperature Controller	Temperature Set Point (ºC)
Oven 2 (Mn Bubbler Temperature)	90-120*
Oven 1 (Cu)	120
TC 1	110
TC 2	110
Furnace (Deposition Temperature)	130-180**
TC 3	110
TC 4	110-130
TC 5	110-130
TC 6 (Substrate Holder Heater)	Turn ON to the mark

* Sufficient vapor delivery is usually obtained at 90 ºC, bubbler temperature can be increased to up to 120 ºC (without decomposing the precursors) to achieve higher precursor vapor pressure and deposit rate.

** A deposition temperature of 130 ºC is typically used. MnN_x films can be deposited at higher temperatures but the surface morphology and step coverage tend to be poorer.

Heat up time: 1 hour

Operating Procedure

- Leave only MFC #4 (**60 sccm**) on
- Turn off ALD valve #7
- Turn on ALD valve #5, then turn on ALD valve #6 to start Mn precursor flow

- Turn on MFC #3 (**60 sccm**) to start ammonia flow and MFC #5 (**60 sccm**) to start nitrogen assist flow, this additional nitrogen flow is necessary to improve the uniformity of the films
- Set **Operating Pressure = 5 Torr** (set point B)
- **Typical deposition time = 5 minutes**
- Upon finish, set pressure controller to OPEN
- Turn off MFC #3 to terminate ammonia flow
- Turn off ALD valve #6, then turn off ALD valve #5 to terminate Mn precursor flow
- Turn on ALD valve #7 to start purging

To continue with iodine catalyzed Cu deposition, turn off all temperature controllers, oven, and furnace heaters (allow 40 – 60 minutes to cool down to room temperature)

Iodine Exposure

Iodine exposure is typically carried out at around room temperature to avoid thermal decomposition or formation of manganese iodide compounds.

MFC #1 and MFC #5 are both turned ON to achieve a total of 100 sccm of nitrogen flow

Open both manual valves between the ethyl iodide source and the reactor chamber to allow ethyl iodide vapor to enter reactor chamber, turn on the needle valve to the mark (**50 sccm**) and start the timer

Typical iodide exposure time = 15-30 seconds, upon finish, turn off both manual valves and the needle valve

CVD Cu Process

Pure copper can be prepared by supplying Cu precursor and hydrogen. It can be used to completely fill narrow trenches or to form conformal seed layers for larger through-silicon via (TSV) features.

Temperature settings:

Table I-4

Temperature Controller	Temperature Set Point (ºC)
Oven 2 (Mn Bubbler Temperature)	120
Oven 1 (Cu)	160
TC 1	110
TC 2	120
Furnace (Deposition Temperature)	180-200*
TC 3	120
TC 4	110-140
TC 5	110-140
TC 6 (Substrate Holder Heater)	Turn ON to the mark

* A deposition temperature of 180 ºC is typically used for iodine-catalyzed Cu deposition. In the absence of manganese nitride underlayer and iodide exposure, Cu deposition is typically carried out at 200 ºC.

Heat up time: 1 hour

Operating Procedure

- Leave only MFC #1 (**40 sccm**) on
- Turn off ALD valve #7
- Turn on ALD valve #2 to start nitrogen assist flow
- Turn on ALD valve #3 to open 3-way valve and allow Cu precursor flow
- Press RUN on DLI syringe controller (**typical injection rate = 0.05 mL/min**)
- Turn on MFC #2 (**100 sccm**) to start hydrogen flow
- Set **Operating Pressure = 5 Torr** (set point B)
- **Typical deposition time = 10-20 minutes**, depending on the targeted thickness
- Upon finish, set pressure controller to OPEN
- Turn off MFC #2 to terminate hydrogen flow

- Press STOP on DLI syringe controller to terminate Cu precursor supply
- Turn off ALD valve #3, then turn off ALD valve #2
- Turn on ALD valve #7 to start purging
- Turn off all ovens and heaters, allow up to one hour to cool down

CVD Cu-Mn Alloy Process

This procedure deposits ~0.5-1 atomic percent of Mn in Cu. The concentration of Mn in the Cu-Mn alloy can be varied by changing the bubbler temperature of the Mn precursor or by adjusting the flow rates of the nitrogen carrier gas (MFCs #1 and #4). Upon post-annealing, Mn diffuses out from Cu to reach Cu/insulator interface and therefore enhances barrier and adhesion properties at the interface.

Temperature settings:

Table I-5

Temperature Controller	Temperature Set Point (ºC)
Oven 2 (Mn Bubbler Temperature)	120
Oven 1 (Cu)	160
TC 1	110
TC 2	120
Furnace (Deposition Temperature)	180-200*
TC 3	120
TC 4	110-140
TC 5	110-140
TC 6 (Substrate Holder Heater)	Turn ON to the mark

* A deposition temperature of 180 ºC is typically used for iodine-catalyzed Cu-Mn deposition. In the absence of manganese nitride underlayer and iodide exposure, Cu-Mn deposition is typically carried out at 200 ºC.

Heat up time: 1 hour

Operating Procedure

- Leave only MFC #4 (**60 sccm**) on

- Turn off manual valve M1 to separate nitrogen assist flows
- Turn off ALD valve #7
- Turn on ALD valve #5, then turn on ALD valve #6 to start Mn precursor flow
- Turn on MFC #1 (**40 sccm**)
- Turn on ALD valve #2 to start nitrogen assist flow
- Turn on ALD valve #3 to open 3-way valve and allow Cu precursor flow
- Press RUN on DLI syringe controller (**typical injection rate = 0.05 mL/min**)
- Turn on MFC #2 (**100 sccm**) to start hydrogen flow
- Set **Operating Pressure = 5 Torr** (set point B)
- **Typical deposition time = 10-20 minutes**, depending on the targeted thickness
- Upon finish, set pressure controller to OPEN
- Turn off MFC #2 to terminate hydrogen flow
- Press STOP on DLI syringe controller
- Turn off ALD valve #3, then turn off ALD valve #2 to terminate Cu precursor supply
- Turn off ALD valve #6, then turn off ALD valve #5 to terminate Mn precursor supply
- Turn on ALD valve #7 to start purging
- Turn on manual valve M1

If a post-annealing step is necessary (i.e. to diffuse the Mn out from the Cu-Mn alloy to Cu/insulator interface), turn off both ovens, leave other heats on, set furnace to 350 ºC and the substrate holder to the corresponding mark.

Typical heat up time = 1 hour, typical post-anneal time = 60 to 90 minutes

Selective Deposition of Mn on Cu

Selective deposition of Mn capping layers on Cu is desired to avoid contamination of the neighboring dielectric insulators, which may result in increased line-to-line leakage. The following silylation method is designed to achieve high degree of selectivity by replacing reactive SiOH groups on the insulator surface with inert $SiCH_3$ bonds:

1. Drying: Moisture adsorbed on the surface of porous dielectric materials are removed by flushing the substrates with purified nitrogen at 200 ^{o}C for ½ hour and 350 ^{o}C for ¼ hour.

2. Reduction: To avoid silylation of oxidized copper surfaces, substrates with copper are reduced by flowing purified hydrogen gas at 250 ^{o}C for 1 hour

3. Passivation: Cool the reactor to room temperature, pump down to base pressure (about 20 mTorr), and fill the reactor chamber with bis(*N,N*-dimethylamino) dimethylsilane (SAM 1) vapor (about 14 Torr) and heat to 90 ^{o}C for ½ hour.

After exposure of SAM 1, pump to base pressure, cool to room temperature, and refill the reactor chamber with (*N,N*-dimethylamino) trimethylsilane (SAM 2) vapor (about 75 Torr) and heat to 90 ^{o}C for ½ hour.

After exposure of SAM 2, pump to base pressure and prepare the substrates for CVD Mn process described above.

Appendix II. List of Publications, Patent Applications, and Conference Presentations

Publications

1. **Y. Au**, Q. M. Wang, H. Li, J. M. Lehn, D. V. Shenai, and R. G. Gordon, "Vapor Deposition of Highly Conformal Copper Seed Layers for Plating Through-Silicon Vias", *J. Electrochem. Soc.*, **159** (6) D382-D385 (2012).
2. **Y. Au,** Y. Lin, and R. G. Gordon, "Filling Narrow Trenches by Iodine-Catalyzed CVD of Copper and Manganese on Manganese Nitride Barrier/Adhesion Layers", *J. Electrochem. Soc.*, **158** (5) D248-D253 (2011).
3. **Y. Au**, Y. Lin, H. Kim, E. Beh, Y. Liu, and R. G. Gordon, "Selective Chemical Vapor Deposition of Manganese Self-Aligned Capping Layer for Cu Interconnections in Microelectronics", *J. Electrochem. Soc.*, **157** (6) D341-D345 (2010).
4. R. G. Gordon, H. Kim, **Y. Au**, H. Wang, H. B. Bhandari, Y. Liu, D. K. Lee, and Y. Lin, "Chemical Vapor Deposition of Manganese Self-Aligned Diffusion Barriers for Cu Interconnections in Microelectronics", *Adv. Met. Conf. 2008, Proc.*, 321 (2009).

Patent Applications

1. R. G. Gordon, H. B. Bhandari, **Y. Au**, and Y. Lin, "Self-aligned Barrier and Capping Layers for Interconnects" (U.S. Application No. 61/254,601, filed Oct 23, 2009; International Application No. PCT/US2010/05339, filed Oct 20, 2010).

Conference Presentations

1. **Y. Au** and R. G. Gordon, "Vapor Deposition of Highly Conformal Copper Seed Layers for Plating Through-Silicon Vias," Presented at 220th ECS Meeting, Boston, MA (2011).
2. **Y. Au**, Y. Lin, H. Kim, Z. Li, and R. G. Gordon, "Atomic Layer Deposition and Chemical Vapor Deposition of Copper-Based Metallization for Microelectronic Fabrication," Presented at 11th International Conference on Atomic Layer Deposition, Cambridge, MA (2011).
3. **Y. Au,** Y. Lin, and R. G. Gordon, "Bottom-up Filling of Surfactant-Catalyzed Chemical Vapor Deposition of Copper and Copper-Manganese Alloy in Narrow Trenches," Presented at 2011 MRS Spring Meeting, San Francisco, CA (2011).
4. **Y. Au**, Y. Lin, H. Kim, E. Beh, Y. Liu, and R. G. Gordon, "Selective Chemical Vapor Deposition of Manganese Self-Aligned Adhesion and Barrier Layers for Cu Interconnections in Microelectronics," Presented at 2010 MRS Spring Meeting, San Francisco, CA (2010).
5. H. Kim, **Y. Au**, H. Wang, H. B. Bhandari, Y. Liu, D. K. Lee, Y. Lin, and R. G. Gordon, "Chemical Vapor Deposition of Manganese Self-Aligned Diffusion Barriers for Cu Interconnections in Microelectronics," Presented at AVS 55th International Symposium, Boston, MA (2008).