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First Experimental Demonstration of Gate-all-around III-V MOSFETs by Top-down Approach

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Introduction: Recently, continuous progress has been made in the understanding and improvement of high-k/III-V interfaces. However, to realize III-V FETs beyond the 15nm technology node, emerging 3D device structures are necessary to suppress short-channel effects (SCE). III-V FinFETs [1-2] as well as multi-gate quantum-well FETs [3] have been shown to improve greatly the off-state performance of III-V FETs with deep submicron gate lengths. On the other hand, the gate-all-around (GAA) structure has been proven [4-6] on Si CMOS to be the most resistant to SCE, thanks to having the best gate electrostatic control. Therefore, a III-V GAA FET is the most promising candidate for the ultimate scaling of III-V FETs. In this abstract, we report *the first experimental demonstration* of inversion-mode $In_{0.53}Ga_{0.47}As$ GAA FETs by a top-down approach with atomic-layer-deposited (ALD) Al_2O_3/WN gate stacks. Benefiting from the GAA structure, we have demonstrated the shortest gate length (L_G = 50nm) III-V MOSFETs to date with well-behaved on-state and off-state characteristics. A systematic scaling metrics study has been carried out for $In_{0.53}Ga_{0.47}As$ GAA FETs with L_G from 110nm down to 50nm, with fin widths (W_{Fin}) of 30nm and 50nm, fin height (H_{Fin}) of 30nm and wire lengths (L_{NW}) = 150 to 200nm.

Experiments: Fig. 1 shows a schematic view of a $In_{0.53}Ga_{0.47}As$ GAA FET fabricated in this work. The starting material is 30nm p- $In_{0.53}Ga_{0.47}As$ on p+ (100) InP substrate. Table 1 and Fig. 2 depict the key fabrication processes for $In_{0.53}Ga_{0.47}As$ GAA FETs. Fig. 3 (a)-(b) demonstrates the novel InGaAs channel release process and Fig. 3(c) shows the SEM image of a finished device. Devices with different numbers of parallel channels (1 wire, 4 wires, 9 wires or 19 wires) were fabricated in this work. Fig. 4 shows the fin patterning direction (along [010] direction) and device alignment to the substrate for a successful release process.

Results and discussion: Fig. 5 - 6 show the well-behaved output and transfer characteristics as well as I_g-V_g of a L_G=50nm GAA FET. The current is normalized by the total perimeter of the $In_{0.53}Ga_{0.47}As$ channel, i.e. $W_G = (2W_{Fin}+2H_{Fin})\times$(No. of wires). A representative 50nm L_G device shows on-current over 700μA/μm, transconductance over 500μS/μm and reasonable off-state characteristics with subthreshold swing (SS) of 150mV/dec and drain-induced barrier lowering (DIBL) of 210mV/V. Although operating in inversion-mode, the threshold voltage of the device is -0.68V from linear extrapolation at V_{ds}=50mV due to the relatively small work function of ALD WN metal (~4.6eV). Due to the junction leakage current and a very large area ratio ($>10^3$) between implanted junction and GAA channels, the source current is used to obtain the intrinsic current in the channel. Gate leakage current is minimal in the entire gate voltage range, indicating 10nm Al_2O_3 is sufficient for GAA structure and further EOT scaling is achievable. Source current saturates at negative V_{gs} due to a leakage path underneath the bottom gate and limits the on-off ratio of the device. Fig. 7 shows the extrinsic and intrinsic transconductance at V_{ds}=1V for the same device. The source/drain resistance R_{SD} is extracted to be around 1150Ω·μm. The maximum intrinsic transconductance is 750μS/μm. Fig. 8 shows the I_{ON} and g_m scaling metrics for L_G=50-110nm and W_{Fin}=30nm. Fig. 9 – 11 show the V_T, SS and DIBL scaling metrics for L_G=50-110nm with W_{Fin}=30nm and 50nm. From Fig. 9, 30nm W_{Fin} devices show better V_T roll-off properties when L_G is shrinking. The SS for 30nm W_{Fin} devices are almost unchanged at around 150mV/dec when scaling L_G down to 50nm, indicating excellent control of SCE and improved interface property considering the large EOT, whereas the 50nm W_{Fin} devices show larger SS, which increases with scaling of L_G. Fig. 11 shows that 30nm W_{Fin} devices have smaller DIBL. Further DIBL reduction can be achieved by scaling down EOT. Fig. 12 shows the transfer characteristics for two GAA FETs with 1 wire and 4 wires in parallel, respectively. Fig. 13 – 14 shows a linear relationship of $I_{s,max}$ and $g_{m,max}$ with the number of wires in both the linear and saturation regimes. Each wire can deliver a I_{sat} =90μA and g_m =66μS at V_{ds}=1V. Fig. 15 shows the output characteristic for a hero GAA FET with the I_{ON}=1.17mA/μm. Fig. 16 benchmarks the g_m·EOT product vs. L_G of $In_{0.53}Ga_{0.47}As$ GAA FETs in this work with surface channel InGaAs MOSFETs [1][7-10]. Table 2 compares the device structure and performance of $In_{0.53}Ga_{0.47}As$ GAA FETs in this work with all published non-planar 3D III-V FETs [1-3][7]. Due to the excellent electrostatic control of the channel by GAA structure, L_G has been pushed down to 50nm with excellent on- and off-state performance.

Conclusions: We have demonstrated for the first time inversion-mode $In_{0.53}Ga_{0.47}As$ GAA MOSFETs with ALD Al_2O_3/WN gate stacks. The highest saturation current reaches 1.17mA/μm at V_{ds}=1V. The SCE of III-V MOSFETs is greatly improved by the 3D structure design, making III-V GAA FET a very promising candidate for ultimately scaled III-V device technology.

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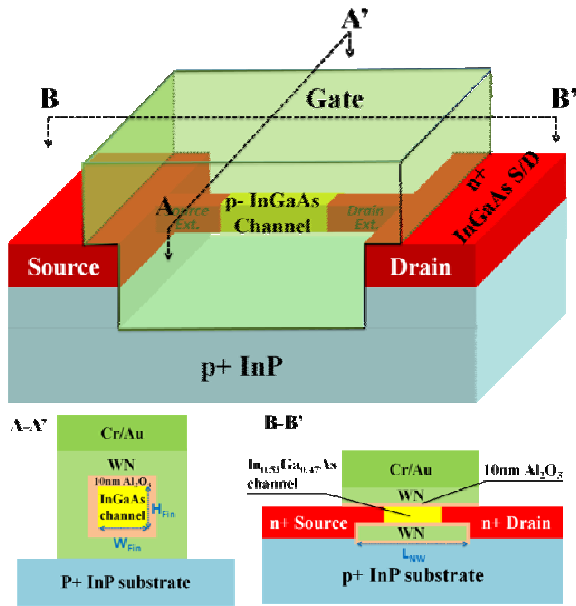

Fig. 1 Schematic view of an inversion-mode GAA n-channel $In_{0.53}Ga_{0.47}As$ ($2\times10^{16}/cm^3$) MOSFET with 10nm ALD Al_2O_3/20nm WN gate stack. A heavily doped wide bandgap InP lies underneath the channel.

- NH_4OH pretreatment and ALD Al_2O_3 10nm deposition
- S/D implantation (Si: 20KeV / 1×10^{14} cm^{-2})
- S/D activation (600°C 15s in N_2)
- InGaAs fin etching by ICP BCl_3/Ar
- Localized nanowire release by selective etching of InP over InGaAs using HCl based solution
- Pre-gate passivation using $(NH_4)_2S$ solution
- ALD 10nm Al_2O_3 and 20nm WN gate stack conformal deposition surrounding nanowire channel
- Gate pad definition and gate etch using ICP CF_4/Ar
- S/D Au/Ge/Ni metallization and 350°C annealing
- Test pad deposition

Table 1 Fabrication process flow for inversion-mode high-k/InGaAs GAA FETs. All patterns were defined by a Vistec VB-6 UHR electron beam lithography system. Dry etching was carried out by a Panasonic E620 high density plasma etcher.

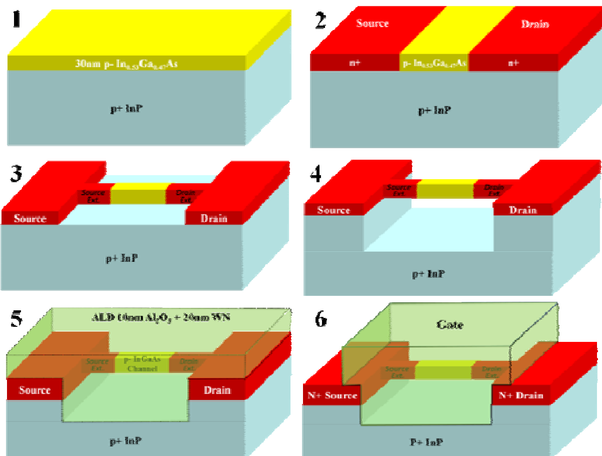

Fig. 2 Schematic diagram of key process steps in the fabrication of InGaAs GAA MOSFETs.

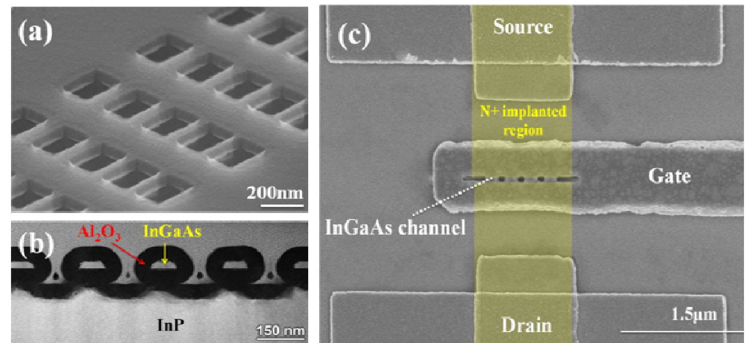

Fig.3 (a) Tilted SEM image of free-standing InGaAs nanowire test structures after the release process. (b) Cross-sectional TEM image of InGaAs nanowire test structures wrapped by 50nm ALD Al_2O_3 on InP substrate, confirming the nanowires are completely released (c) Top view SEM image of a finished InGaAs GAA FET with 4 parallel wires of W_{Fin} = 30nm , L_{NW} = 200nm and L_G = 50nm.

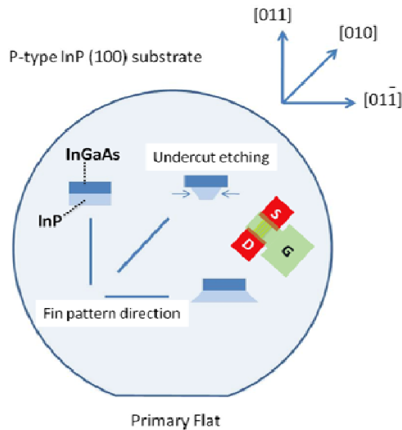

Fig. 4 Schematic diagram of fin patterning direction and etching profile.

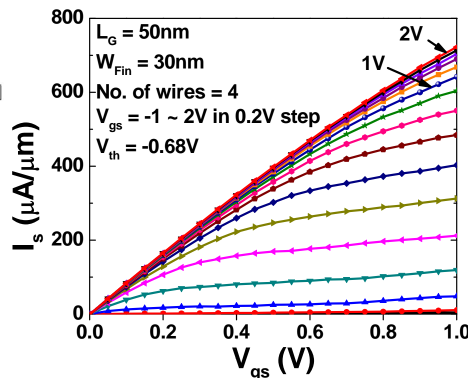

Fig. 5 Output characteristic of a representative GAA FET with L_G=50nm, W_{Fin}=30nm. The current from each wire is normalized by 120nm, the perimeter of the channel

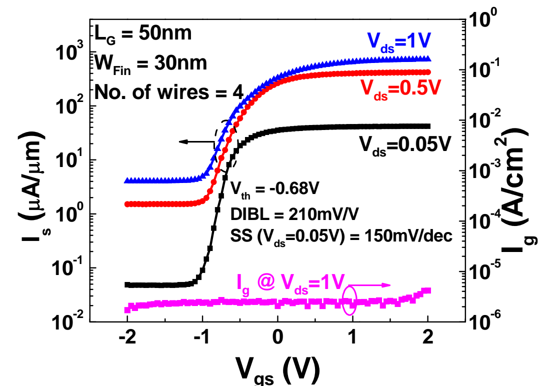

Fig. 6 Transfer characteristic and gate leakage current of a representative GAA FET with L_G=50nm and W_{Fin}=30nm.

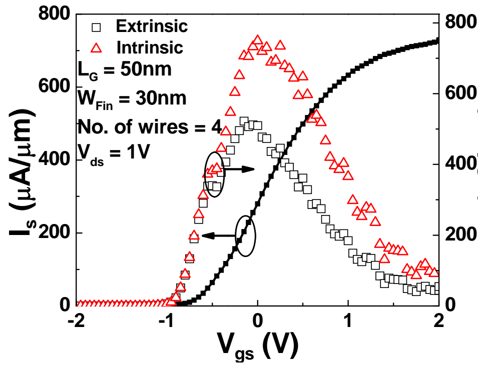

Fig. 7 Current and extrinsic/intrinsic trans-conductance in saturation regime. The source/drain resistance R_{SD} is extracted to be 1150Ω·μm

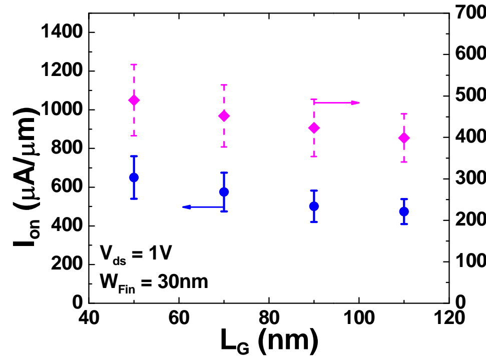

Fig. 8 I_{ON} and g_m vs. L_G for GAA FETs with W_{Fin}=30nm. The values are determined by measuring 20 different devices at the same L_G. Error bar shows statistical variations of multiple devices.

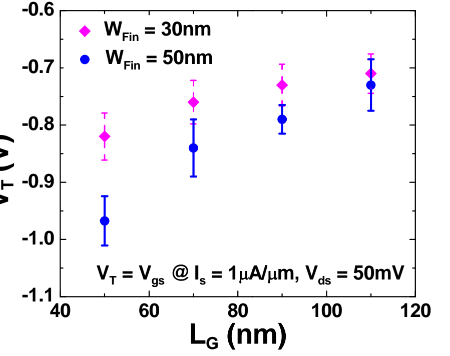

Fig. 9 V_T vs. L_G for GAA FETs with W_{Fin}=30nm and 50nm. Smaller W_{Fin} shows better V_T roll-off.

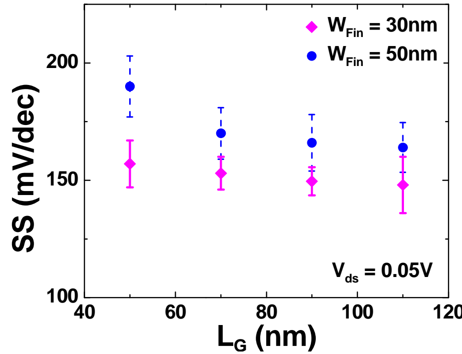

Fig. 10 SS vs. L_G for GAA FETs with W_{Fin}=30nm and 50nm. The estimated upper limit of midgap D_{it} from SS is 5.6×10^{12} /cm²·eV, a factor of 2 lower than those reported in [1].

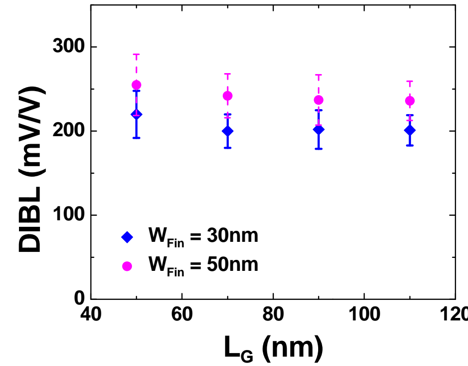

Fig. 11 DIBL vs. L_G for GAA FETs with W_{Fin}=30nm and 50nm.

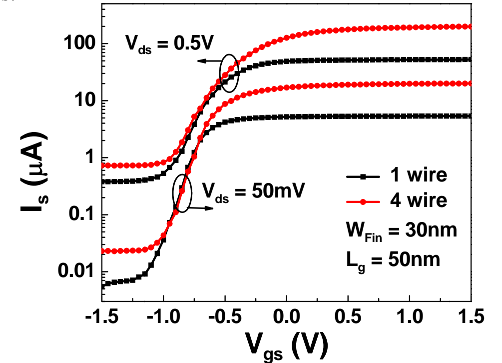

Fig. 12 Transfer characteristic of GAA FETs with 1 and 4 parallel wires.

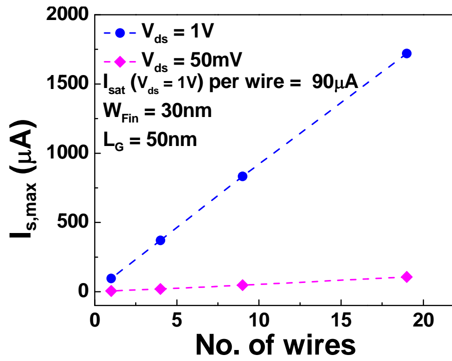

Fig. 13 Linear and saturation current for GAA FETs with different number of parallel wires.

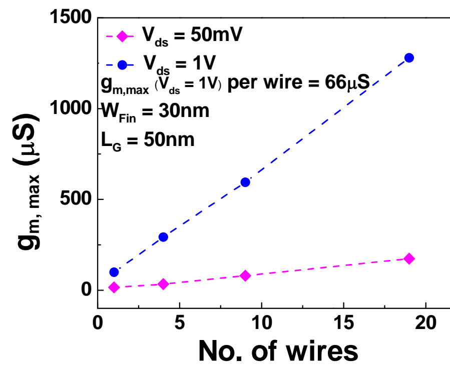

Fig. 14 Linear and saturation transconductance for GAA FETs with different number of parallel wires.

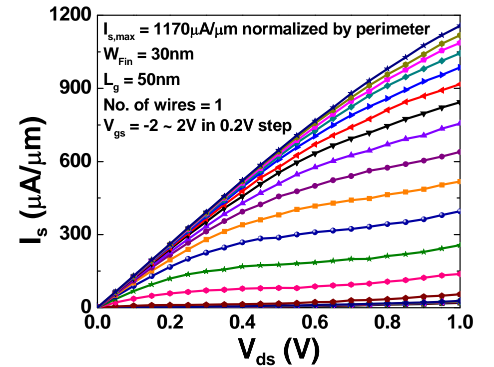

Fig. 15 Output characteristic of a hero GAA FET with saturation current of 1.17mA/μm.

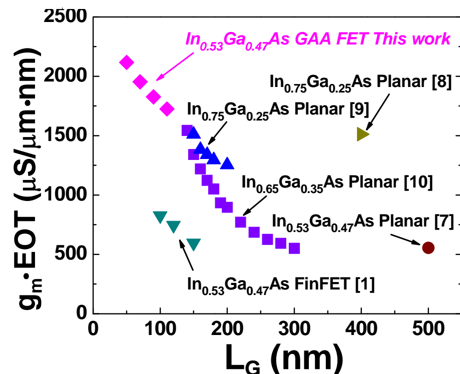

Fig. 16 Benchmarking g_m·EOT of planar and non-planar InGaAs surface-channel MOSFETs.

Structure	$In_{0.53}Ga_{0.47}As$ Planar	$In_{0.53}Ga_{0.47}As$ FinFET	$In_{0.7}Ga_{0.3}As$ FinFET	$In_{0.7}Ga_{0.3}As$ Multi-gate Quantum Well FET	$In_{0.53}Ga_{0.47}As$ GAA FET (This work)
	Ref [7]	Ref [1]	Ref [2]	Ref [3]	
Dielectric	8nm ALD Al_2O_3	5nm ALD Al_2O_3	19nm MOCVD HfAlO	2.1nm ALD $TaSiO_x$	10nm ALD Al_2O_3
L_G [nm]	500nm	100nm	130nm	70nm	50nm
W_{Fin} [nm]		40nm	220nm	60nm	30nm
I_{sat} [μA/μm]	430 (V_{ds}=2V, V_{gs}-V_T=3.2V)	220 (V_{ds}=1V, V_{gs}-V_T=0.85V)	850 (V_{ds}=2V, V_{gs}-V_T=3V)	~300 (V_{ds}=0.5V, V_{gs}-V_T=0.5V)	720 (1170 Max.) (V_{ds}=1V, V_{gs}-V_T=2.7V)
DIBL [mV/V]	350	180	135	110	210
SS [mV/dec]	240	145	230	120	150

Table 2 Comparison of InGaAs GAA FETs in this work and recently reported non-planar III-V FETs.