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Citation	Han, Anpan, Dimitar Vlassarev, Jenny Wang, Jene A. Golvchenko, and Daniel Branton. 2010. Nano Letters 10(12): 5056-5059.
Published Version	doi:10.1021/nl1032815
Accessed	February 19, 2015 7:36:30 AM EST
Citable Link	http://nrs.harvard.edu/urn-3:HUL.InstRepos:4635033
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Ice Lithography for Nano-Devices

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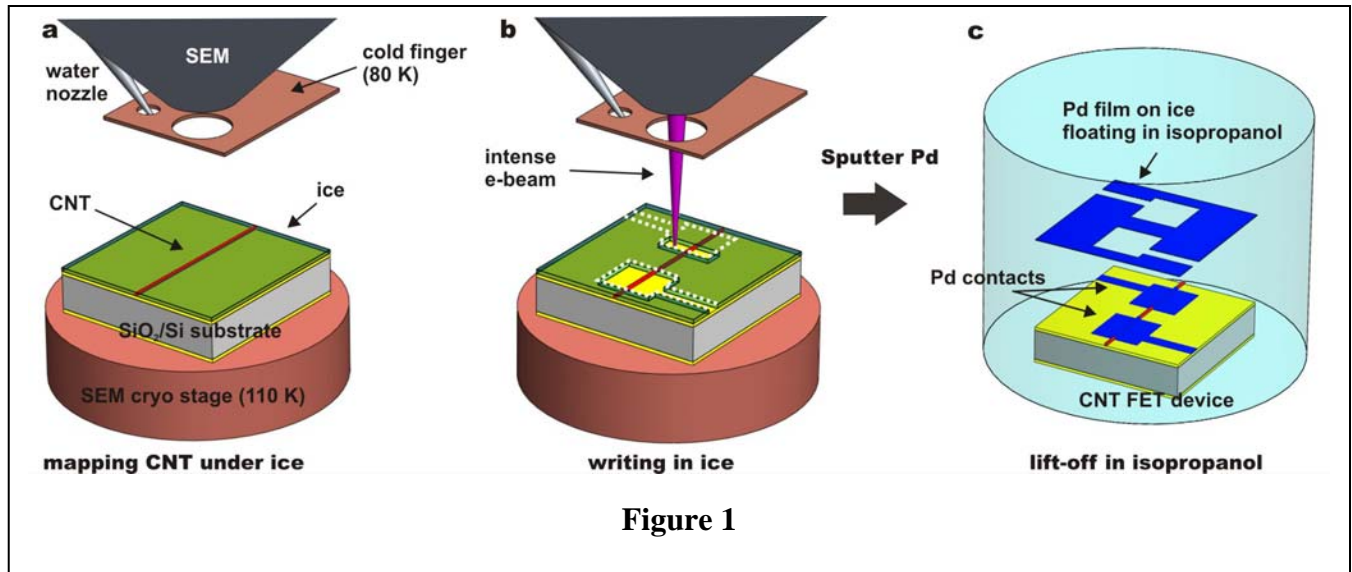
ABSTRACT. We report the successful application of a new approach, ice lithography (IL), to fabricate nanoscale devices. The entire IL process takes place inside a modified scanning electron microscope (SEM), where a vapor-deposited film of water ice serves as a resist for e-beam lithography, greatly simplifying and streamlining device fabrication. We show that labile nanostructures such as carbon nanotubes can be safely imaged in an SEM when coated in ice. The ice film is patterned at high e-beam intensity and serves as a mask for lift-off without the device degradation and contamination associated with e-beam imaging and polymer resist residues. We demonstrate the IL preparation of carbon nanotubes field effect transistors (FETs) with high quality trans-conductance properties.

KEYWORDS. e-beam lithography, carbon nanotube, nano-device, field effect transistor

It was recently shown that water ice can serve as a resist during high resolution e-beam lithography¹, easily achieving sub-10nm features. The special properties of water ice allow direct application in a vacuum environment, conformal coating of complex 3-D structures, through-resist mapping and registration of nanostructures, and simple, contamination-free removal. Here we demonstrate that high quality carbon nanotube FETs can be fabricated with ice lithography.

We extensively modified a field emission scanning and e-beam writing electron microscope (SEM) for device fabrication using IL (Figure 1). Based on our previous work fabricating sub 20 nm-wide metal lines by nano-patterning ice¹, our new instrument is a cluster-tool that allows the entire IL process to be effected and examined within one vacuum system². A sample containing the desired nano-device elements is first cooled to cryogenic temperatures in the microscope vacuum (for detailed methods, see Supporting Materials). Our sample consists of single walled carbon nanotubes (SWCNTs) grown by chemical vapor deposition (CVD) from an iron catalyst pad^{3, 4}. When cooled to ~110 K the sample is exposed to water vapor from a gas injection system. A thin, conformal layer of amorphous ice, several

tens of nanometers thick, forms on the surface of the sample. The nanotubes are then located by imaging



through the ice layer with a low intensity e-beam. As shown below, typical damage and contamination associated with direct e-beam exposure are eliminated when imaging through ice. The ice resist is then appropriately patterned relative to the underlying nanostructures with a high intensity e-beam guided by an e-beam writing system built into the SEM. The patterning removes ice from those regions where metallic contacts are desired. The cold sample is then rapidly transferred through the vacuum onto a second cryostage located in a specially designed metal deposition chamber that had been incorporated onto the SEM. Here, metal films are plasma sputter-deposited onto the ice patterned sample surface. Two different metals can be deposited, including an adhesion layer which is critical for noble metal adhesion onto dielectric surfaces. Finally, the device is removed from the metal deposition chamber and immersed into isopropanol, which lifts off the metal where no ice had been removed. Thus, the standard processes of mapping SWCNT, Poly(methyl methacrylate) (PMMA) resist spinning, resist baking, e-beam exposure, development, and metal evaporation, which normally use 6 different instruments, are accomplished using the IL process in one instrument.

To electrically connect a CVD grown SWCNT to a pre-existing metal contact pad, the first step is to locate a SWCNT and map its position on the device substrate surface.

Figure 2 demonstrates that all SWCNTs visible in an AFM image can also be visualized through ice with the SEM. It normally takes 4 hours to image and map a 50 x 50 μm area with an AFM. We can easily map this area through ice in the SEM in just a few minutes. The e-beam dose used for imaging is

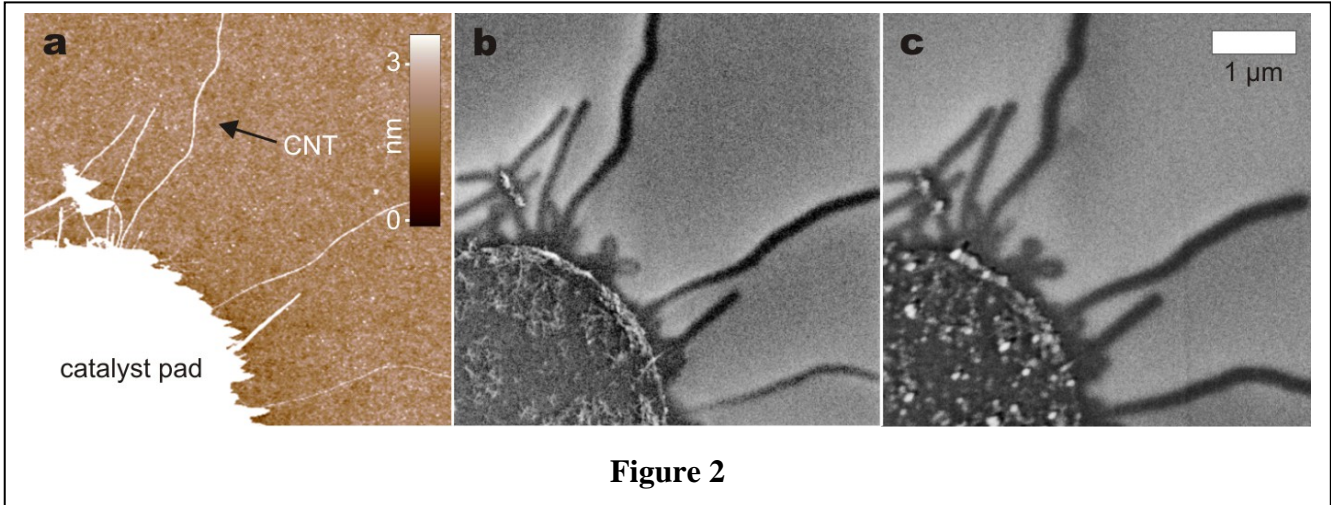


Figure 2

four orders of magnitude smaller than that required for actual patterning, so no significant ice removal occurs during imaging. Aside from the time saving aspects of *in situ* SEM imaging, e-beam damage and contamination⁵ that have previously limited the usefulness of SEM mapping are avoided (see below).

Contrast for imaging SWCNT in the SEM is the result of dynamic charging of insulating layers by the incident e-beam⁶⁻⁹. Here, the underlying SiO_2 back gate insulator and the amorphous ice serve as the charged insulator layer, whereas the conducting SWCNTs are electrically grounded through the iron catalyst pad from which they grow. The insulating layers become negatively charged by exposure to the primary e-beam and the SWCNT remains at ground potential. Consequently, low-energy secondary electrons emitted near the nanotube are collected by the nanotube rather than the microscope's secondary electron detector. This visibly distinguishes the nanotubes as dark lines (Figure 2). Note that the image of the nanotube diameter can be much greater than its geometrical diameter, enabling even low resolution microscopes to image carbon nanotubes. Imaging the SWCNT through a thin dielectric layer can also be used as a non-invasive method for rapid quality control of the electrical integrity of nanodevices after dielectric coating and passivation.

The next step of IL is patterned ice removal to form the mask for metal deposition¹. Guided by the SEM image of the nanotubes, the e-beam patterning system selectively removes ice to form the designed mask (Figure 1b). At 20 kV e-beam energy, typically a dose of 1 C/cm² is required to remove 80 nm thick ice. After the writing process, the sample can be immediately imaged again, at low SEM beam intensity to inspect the writing quality. Such inspection, which is not possible with standard lithography, provides a valuable opportunity to make minor corrections or abort further processing.

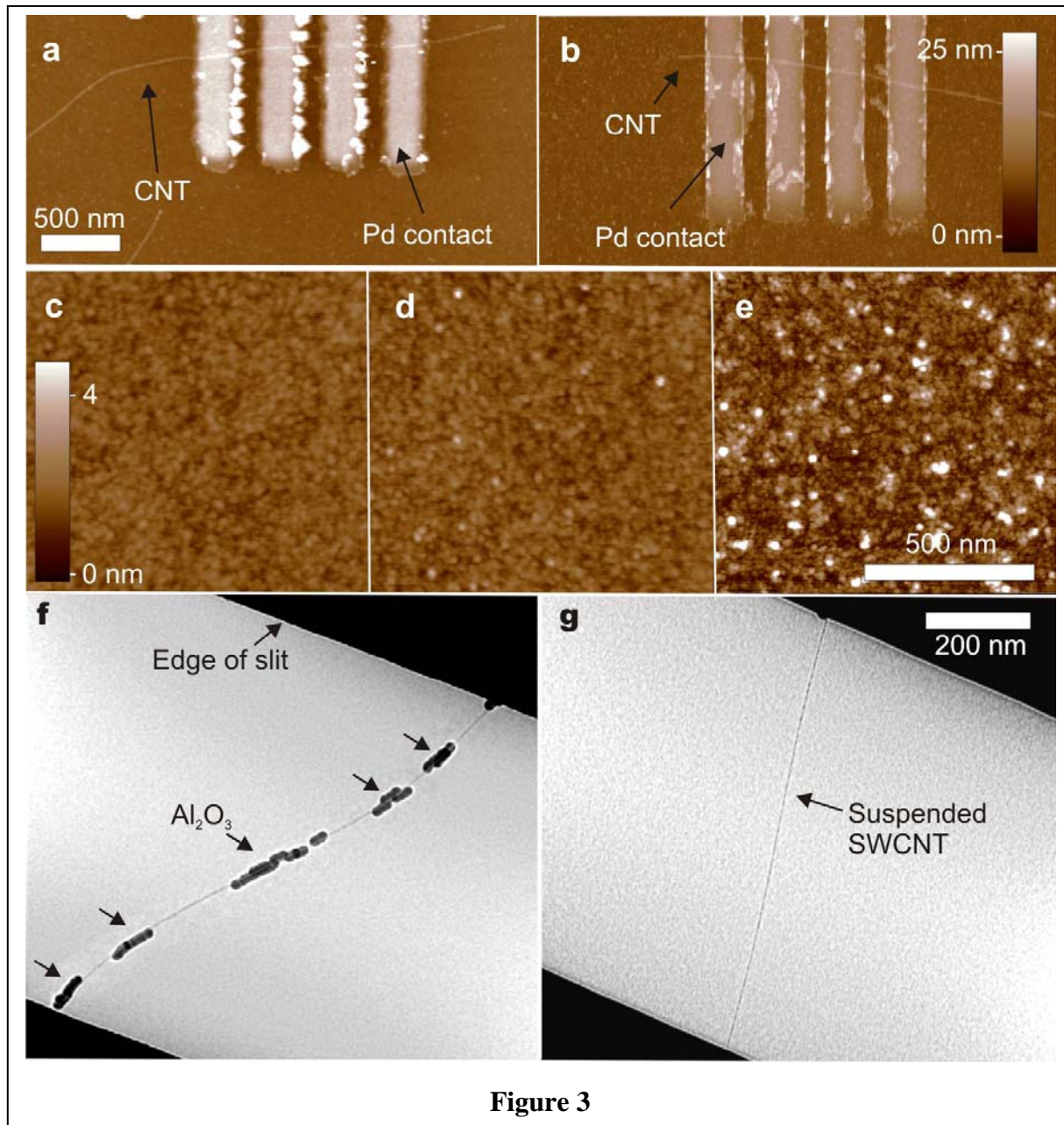


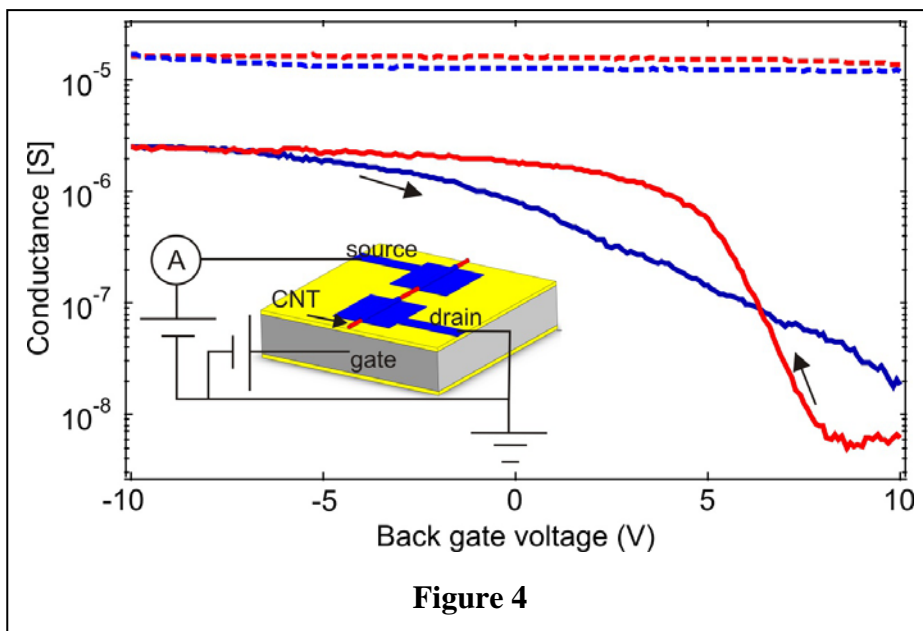
Figure 3

The patterned sample is next transferred onto the metal deposition cryostage held at 165 K. At this temperature, 14 nm of ice sublimates in 1 min. Five nm of ice are allowed to sublime from the entire sample surface to assure that any remaining ice at the bottom of the patterned mask wells is removed before depositing metals., and lift-off is finally carried out in isopropanol (Fig. 1c).

Two methods were used to evaluate e-beam induced defects or contaminants on the finished device. First, tapping mode AFM was used to inspect and compare SWCNT-metal nanostructures made by IL vs. standard e-beam lithography using a PMMA resist (Figure 3a-e). Following IL, the root-mean-

square surface roughness of the device surfaces barely increases from its initial value of 0.25 - 0.27 nm to a value of 0.31 nm. This small increase in surface roughness using IL contrasts with the much greater increase to 0.81 nm after using a standard PMMA resist. Second, we tested the ability of free-standing nanotubes to nucleate the growth of Al₂O₃ during atomic layer deposition (ALD) of Al₂O₃ on the entire sample. Pristine, defect-free nanotubes do not nucleate the growth of Al₂O₃ whereas contaminants or SEM-induced damage sites do¹⁰⁻¹². Figure 3f-g shows an example of how free-standing, unprotected nanotubes imaged by SEM do nucleate Al₂O₃ growth, while those imaged through ice do not. Thus, IL can produce devices that remain free of processing residues and e-beam induced defects.

Electrical measurements under ambient room temperature conditions showed that the SWCNTs contacted by IL contained both semiconducting and metallic tubes at a ratio of 2:1, as commonly observed for CVD grown tubes. Examples of the electrical responses of a metallic and a semiconducting SWCNT FET produced on Si₃N₄ are shown in Figure 4. While sweeping the back-gate bias from -10 V to 10 V, the semiconducting tube switches to its ON state at a negative gate bias, indicating



hole conduction¹³, while the metallic tube did not show a significant back gate response. The hysteresis commonly observed in ambient conditions for conventionally made SWCNT FETs¹⁴ is noted.

Because it is known that metal films deposited onto cold surfaces tend to be nanoporous¹⁵, we were concerned that the metal contacts and leads formed on cold device structures by IL would not be of the highest electrical quality. We compared IL fabricated devices with more conventionally fabricated nanotube devices on SiO₂ coated Si. Each 10-nm-thick source and drain Pd electrode covered a 0.8 μm long segment of the

SWCNT, with 2 μm between the two electrodes. The IL-made SWCNT FET source drain resistances (R_{sd}) ranged between 0.33 and 16 M Ω , significantly higher than the R_{sd} of ~ 50 k Ω for metallic FETs we fabricated using conventional e-beam lithography with PMMA resist (results not shown). But straightforward annealing of IL samples in an Ar atmosphere at temperatures ranging from 300 $^{\circ}\text{C}$ to 600 $^{\circ}\text{C}$ reduced the IL FET R_{sd} by more than 10 fold and yielded contacts whose R_{sd} 's were comparable to those obtained using standard resist based e-beam lithography: metallic FET devices with R_{sd} between 60 and 90 k Ω , and semiconducting tubes with R_{sd} down to 100 k Ω . We attribute the improved contacts to high temperature densification of the cold deposited Pd contacts.

Our results demonstrate a new approach to nano-device fabrication that solves several problems often faced in designing and producing devices. We foresee that IL could also be used to pattern high purity metal onto three dimensional structures. Automation and scaling up are also feasible. We anticipate that IL can be incorporated into more complex cluster tool environments for making graphene nano-ribbons and nanopore devices¹⁶.

ACKNOWLEDGMENT The authors thank Slaven Garaj and Chris Russo for valuable discussions, and John Chervinsky for engineering the SEM modifications required for the IL instrument. Anpan Han was supported by a post-doctoral fellowship from the Carlsberg Foundation, Denmark. Research was also supported by Grant # 5R014G003703 from the National Human Genome Research Institute, National Institutes of Health, to J. A. Golovchenko and D. Branton.

Supporting Information Available: Detailed description of sample preparation and IL process. This material is available free of charge via the Internet at <http://pubs.acs.org>.

FIGURE CAPTIONS

FIGURE 1. IL process. (a) The sample with pre-formed Mo micro-leads and SWCNT on the SiO₂ coated Si substrate is loaded into the SEM via the load-lock and cooled down to ~ 110 K on the SEM cryo-stage. Water vapor is leaked into the SEM through a nozzle just above the sample and condenses

as amorphous ice on the cold sample. Typically, 80 nm of ice is deposited in 30 s. The location of a SWCNT under the ice is mapped. **(b)** An intense e-beam draws patterns for the contacts (white dotted line) and removes ice, forming a mask for metal electrodes contacting the SWCNT. **(c)** The sample with nano-patterned ice resist is transferred onto the metal deposition chamber and Pd is sputtered over the entire sample. The sample is removed from the metal deposition chamber and, while still frozen, immediately immersed into isopropanol held at room temperature, whereupon the Pd film on top of the ice resist drifts away, leaving the pre-formed Mo leads connected to the SWCNT with Pd interconnections only where the ice had been removed by the e-beam.

FIGURE 2. Imaging CVD SWCNT through ice on 300 nm thick SiO₂ coated Si substrates. **(a)** Tapping mode AFM image of nanotubes grown from a catalyst pad on a grounded lead. **(b)** SEM image of same area as in **(a)** with sample at ~110K before ice deposition (primary beam energy 2 keV; probe current 17 pA). **(c)** As in **(b)**, but SEM imaged after deposition of a 25 nm ice layer. (Primary beam energy 1.35 keV; probe current 20 pA.)

FIGURE 3. Detecting contaminants and e-beam damage. Tapping mode AFM images of SWCNT contacted by four 200-nm-wide Pd electrodes using **(a)** IL or **(b)** standard lithography using PMMA resist. **(c-e)** High magnification AFM of **(c)** clean chips before the contacting process (RMSSR=0.25-0.27 nm), **(d)** after IL (RMSSR=0.31 nm), and **(e)** after PMMA lithography (RMSSR=0.81 nm). All samples on identical Si₃N₄ surfaces. **(f)** Transmission electron microscopy image of a typical CVD SWCNT suspended across 750-nm-wide slits in a Si₃N₄ membrane that was SEM imaged at room temperature prior to ALD of 11 nm of Al₂O₃. **(g)** Image of a representative SWCNT after ALD, under identical conditions as in **(f)** except that it was protected with a 120 nm layer of ice prior to SEM imaging.

FIGURE 4. **Conductance measurement in ambient conditions of two SWCNT FETs made by IL.** Si substrates coated with 500 nm of SiO₂ and 60 nm of Si₃N₄. Lower left corner illustrates the measurement set-up. Keeping the source-drain voltage over the SWCNT constant at 10 mV, the gate voltage was swept at 5 V/min from -10 to 10 V (blue) and back from 10 to -10 V (red). Arrows indicate sweep direction. Dotted lines show a 60 kΩ metallic tube after annealing at 300 °C. The solid lines show a semiconducting tube after annealing at 600 °C. The ON resistance is 380 kΩ.

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SUPPORTING INFORMATION

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Sample Preparation

Samples with pre-patterned molybdenum electrode pads and CVD grown SWCNT were fabricated essentially as described^{1, 2}. Iron catalyst pads for SWCNT growth were patterned by standard e-beam lithography and lift-off to overlap preformed Mo pads that could be held at ground potential. The SWCNT samples used for the experiments in Figure 3 were prepared by growing SWCNTs across focused ion beam-milled slits in free-standing 200-nm-thick Si₃N₄ membranes spanning KOH-etched trenches in n-doped Si wafers (1-10 Ωcm⁻¹). This created ideal conditions for imaging the SWCNTs by transmission electron microscopy. The iron catalyst pads for SWCNT growth were patterned to lie near the focused ion beam-milled slits such that the SWCNT would grow across the slits.

ALD of Al₂O₃ was carried out in an in-house designed system using 100 cycles to grow ~1 nm-thick Al₂O₃ with trimethyl aluminum and water as reagents. The reactor temperature was set at 240 °C, and purge pressure was set to 100 mTorr.

Sample annealing was carried out in a tube furnace in Ar gas. For experiments that required annealing temperatures above 300°C, Si₃N₄ rather than SiO₂ coated Si substrate chips were always used and the contacts were made by depositing a 1-nm-thick Cr adhesion layer before the Pd. The rationale for these steps is that Pd diffuses into SiO₂ coatings³ at temperatures above 300°C and causes short circuits between the silicon back-gate and source drain electrodes. A Si₃N₄ substrate inhibits such diffusion. Furthermore, Pd de-wets and forms islands when annealed above 300 °C. The 1-nm-thick Cr layer improves Pd adhesion and inhibits such island formation and the associated metal contact discontinuities.

IL process

The sample was loaded into SEM via a door on the metal deposition chamber that served as a load lock which could be isolated from our modified JEOL JSM-7001F SEM main chamber with a butterfly valve. Design and mechanical details of our modifications will be reported elsewhere⁴. After evacuating the metal deposition chamber, the sample was moved onto the SEM's cryo-stage and cooled down to ~110 K. Base pressure in the SEM was typically $< 0.8 \times 10^{-4}$ Pa. A large cold finger held at ~80 K maintained the partial pressure of water to $< 3 \times 10^{-6}$ Pa as measured by a residual gas analyzer. Sample loading, cooling and stage thermal stabilization required about one hour. Water vapor from a hydrated salt ($\text{MgSO}_4 \cdot 7\text{H}_2\text{O}$) was leaked into the SEM through a nozzle just above the sample and condensed as amorphous ice on the cold sample. Ice thickness was determined by patterning wells into the ice and measuring their height projection by tilting the sample. Typically, 80 nm of ice was deposited in 30 s. The ice deposited even around free-standing SWCNTs.

After ten minutes of beam conditioning the SWCNTs positions were mapped through the ice using a 20 pA beam at 2-4 kV. This exposed the ice to about 10^{-4} C/cm². An intense 15 kV or 30 kV, 1 – 2 nA e-beam was then used to remove the ice in a pattern that formed a mask for metal electrodes contacting the SWCNT. As in King *et al.*⁵, a dose test determined the required number of electrons to remove sufficient ice to expose the underlying substrate, typically 1 C/cm² at 15 kV. Dose testing, computer assisted design of electrodes, alignment, and ice mask patterning required about one hour. The sample with nano-patterned ice resist was then transferred onto the metal deposition chamber cryostage that was held at 165 K, where ~5 nm of ice was allowed to sublime off the entire sample before metal deposition. Metals, such as a 1 nm thick Cr film, when desired, and a 10 to 20 nm thick Pd film, were sputtered over the entire sample. Before sputtering, typical base pressure in the MDC was 3×10^{-6} Pa. During Pd sputtering, at a rate of 1 Å/s, the Ar processing gas pressure was maintained at 0.7 Pa. The sample was removed from the metal deposition chamber while still frozen and immediately immersed into isopropanol held at room temperature, whereupon the Pd film on top of the rapidly melting ice resist drifted away, leaving pre-formed Mo pads connected to the SWCNT by the Pd only where the ice

had been removed by the e-beam. The Pd deposition and lift-off step took about one hour, resulting in a total process time of about three hours.

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