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Radiation hard Depleted Monolithic Active Pixel Sensors with high-resistivity substrates

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High Voltage/High resistivity Depleted Monolithic Active Pixel Sensors (HV/HR-DMAPS) is a technology which is becoming of great interest for high energy physics applications. With respect to hybrid pixel detectors, the monolithic approach offers the main advantages of reduced material budget and production costs due to the absence of the bump bonding process. This aspect is important especially when large areas need to be covered as in the tracking detectors of the LHC experiments. Thus, the possibility of employing this technology in the outermost layers of the upgraded ATLAS pixel detector at the HL-LHC is being investigated. Different HR/HV-DMAPS prototypes have been recently developed for the future ATLAS Inner Tracker (ITk) with the aim of studying their radiation hardness and the feasibility of producing large area devices.

The H35DEMO is a large area demonstrator chip for the ITk designed by KIT, IFAE and University of Liverpool and produced in the AMS 350 nm HV-CMOS technology with an engineering run on four different substrate resistivities: 20, 80, 200 and 1000 Ωcm. It consists of four large matrices, two of which include digital electronics and are thus fully monolithic. All matrices feature pixels with a size of $(50 \times 250)\ \mu m^2$ in which the analog electronics is embedded in a Deep N-WELL (DNWELL) also acting as the collecting electrode. H35DEMO chips with a resistivity of 200 Ωcm were irradiated with reactor neutrons to a particle fluence of 1×10^{15} 1 MeV n_{eq}/cm^2, the expected fluence for the outermost pixel layer of ITk. The monolithic CMOS matrix of the H35DEMO chip, called CMOS matrix, was extensively characterised before and after irradiation in beam tests at Fermilab and DESY, with proton and electron beams, respectively. Results after irradiation show good performance in terms of the hit detection efficiency with thresholds of about 1800 e and a bias voltage of 150 V.

Another production of monolithic HV-CMOS prototypes in LFoundry 150 nm technology (LF2) has been recently completed. It includes sensors with a similar DNWELL concept as the H35DEMO but with a smaller pixel size of $(50 \times 50)\ \mu m^2$. Preliminary measurements of leakage current of the LF2 chips were performed showing good agreement with what was expected from the foundry process.

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1. Introduction

A major upgrade of the Large Hadron Collider (LHC), the High Luminosity LHC (HL-LHC), is planned for 2024 with the purpose of increasing of about one order of magnitude the instant luminosity of the accelerator, to deliver up to 4000 fb^{-1} of data for the two main multipurpose experiments over the following years. To cope with the increased luminosity and consequent particle multiplicity expected at the HL-LHC, the ATLAS detector will undergo an upgrade which foresees the full replacement of the present inner detector with a new Inner Tracker (ITk) fully made of silicon devices.

The full surface of the ITk pixel detector will be of the order of 10 m^2 of which the outermost layers will constitute a significant fraction. At the same time, the particle fluence decreases with the distance from the interaction point up to a total integrated fluence foreseen at the end of the detector lifetime for the fifth barrel layer (layer 4) of about 1×10^{15} $\mathrm{n_{eq}/cm^2}$ [1]. With a relatively relaxed radiation levels for the outermost layers, production times and overall costs become the main concerns which led the ATLAS community to investigate monolithic solutions produced in industrial CMOS technologies as an alternative to standard hybrid pixel detectors. In particular, Depleted Monolithic Active Pixel Sensors (DMAPS) produced in commercial CMOS processes on high resistivity substrates offer a significant cost reduction, and have emerged as promising candidates to meet the ATLAS specifications in terms of radiation hardness for the outermost layers.

Two approaches of DMAPS are presently under investigation for the ITk: The *small fill factor* and the *large fill factor* designs [2]. The former design is based on a small collecting electrode to reduce as much as possible the large capacitance and thus the noise. The latter design has instead a large collecting electrode obtained by a Deep N-WELL (DNWELL) implantation. The analog electronics are embedded inside this DNWELL. On one hand, this approach, with respect to the small fill factor, presents a larger capacitance dominated by the interface between the nested wells. On the other hand, it guarantees a more uniform electric field and depletion, resulting in an intrinsically better radiation hardness.

Results out of two large fill factor prototypes will be presented in the following: The H35DEMO which is a large area demonstrator chip including a fully monolithic part, and the LF2 a DMAPS where the full analog and digital functionalities is fitted inside a (50×50) $\mu\mathrm{m}^2$ pixel cell by means of a triple well technology.

2. H35DEMO

The H35DEMO is a (18.49×24.40) mm^2 chip designed by KIT, IFAE and University of Liverpool and produced in the AMS 350 nm HV-CMOS technology on wafers of four different substrate resistivities: 20, 80, 200 and 1000 Ωcm. It consists of four large matrices, two of which include digital electronics and can thus be operated standalone as fully monolithic detectors. One of these matrices, called CMOS matrix, has comparators made of CMOS transistors in the periphery only, while the other, called NMOS matrix, includes also comparators made of NMOS transistors directly in the pixels. The other two matrices have only analog front-end electronics and are meant to be coupled to the ATLAS FE-I4 chip [3]. All matrices feature pixels with a size of 50×250 $\mu\mathrm{m}^2$

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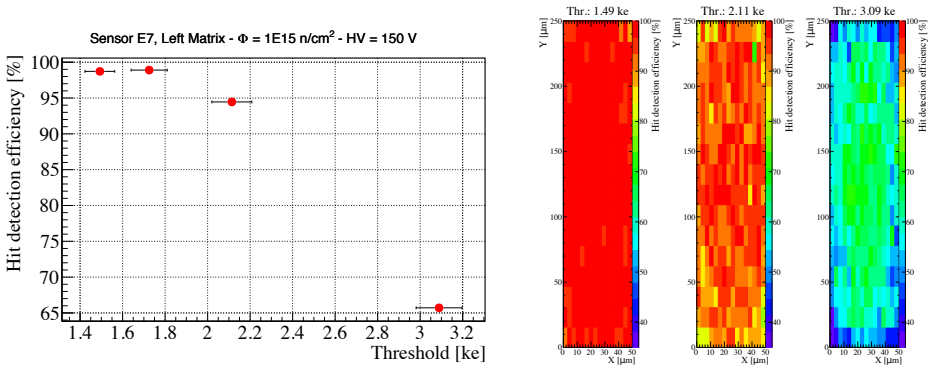
in which the analog electronics are embedded in a Deep N-WELL (DNWELL) also acting as the collecting electrode. More details about this chip and the CMOS matrix characterisation before irradiation can be found in [4, 5].

2.1 Hit detection efficiency

H35DEMO chips of 200 Ωcm resistivity were irradiated with neutrons in the TRIGA Mark II research reactor of the Jožef Stefan Institute (JSI) in Ljubljana. The hit detection efficiency of the CMOS matrix after irradiation to 1×10^{15} n_{eq}/cm^2 has been measured at beam tests in DESY with 4–5 GeV electrons. An AIDA EUDET telescope [8] has been used for reconstructing the particle trajectories and extrapolate the corresponding crossing point on the surface of the Detector Under Test (DUT). A Data Acquisition System (DAQ) system fully developed at IFAE and based on a commercial Xilinx ZC706 FPGA development board [6] has been used to operate and readout the H35DEMO chips [7].

The hit detection efficiency as a function of the threshold is shown in Figure 1(a). A hit detection efficiency of 99 % was measured by applying a bias voltage of 150 V and operating with a threshold lower than about 1800 e. With higher thresholds, inefficiencies due to charge sharing with neighbouring pixels are localised at the pixel borders and in particular in the four corners as shown in Figure 1(b) where the distribution of the hit detection efficiency is shown over the pixel cell surface. For the lowest measured threshold of about 1500 e, a noise occupancy of less than 10^{-6} hits in 25 ns has been measured for the full left sub-matrix which corresponds to a noise occupancy per pixel of less than 4.2×10^{-10} hits in 25 ns.



(a) Hit detection efficiency vs threshold

(b) In-pixel efficiency maps

Figure 1: Hit detection efficiency of the CMOS left sub-matrix after neutron irradiation to a fluence of 1×10^{15} n_{eq}/cm^2 and biased to 150 V. In (a) the hit detection efficiency is shown as a function of the threshold. Error bars indicates the sigma of the gaussian fit to the correspondent threshold distribution. A systematic uncertainty of 0.3 % is assigned to all efficiency measurements. In (b) the hit detection efficiency over one pixel cell is shown for different threshold settings, from left to right: 1490, 2110 and 3090 e. These in-pixel efficiency maps are obtained displaying the reconstructed track impact point expressed in pixel coordinates and projecting the data for all identical structures onto the same image.

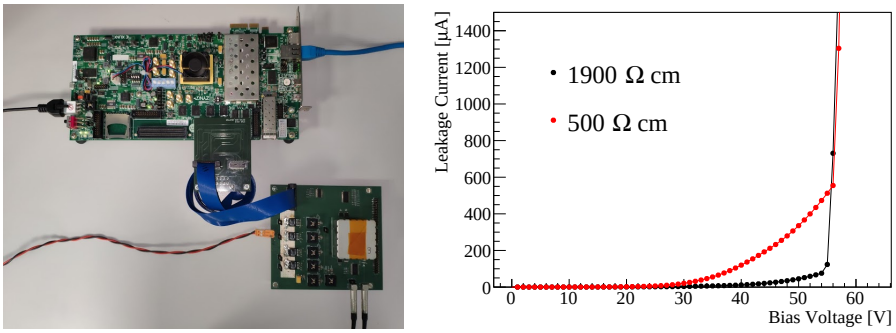
3. LF2

The LF2 is a DMAPS prototype chip produced in 150 nm HV-CMOS process from LFoundry

by the collaboration of IFAE, University of Liverpool, University of Geneva and KIT on two wafer substrate resistivity: 500 Ωcm and 1900 Ωcm. The chip includes a small fully monolithic matrix of 40×78 square pixels with a size of $(50 \times 50)\,\mu m^2$ for a total dimension of the matrix of $(3.9 \times 2)\,mm^2$. It uses a triple well technology with an additional buried isolation layer which allows integration of analogue and digital electronics in the sensitive area of the pixel. In each pixel the time stamp of the leading and falling edge of every event is measured. The Time Over Threshold (TOT) calculation and time walk compensation are performed offline. The matrix is divided into four sub-matrices: Two include pixel with Metal-Insulator-Metal (MIM) feedback capacitors, and two include pixels with diffusion feedback capacitors. Of these a variant featuring enclosed layout transistors is implemented to make the pixels more radiation hard. The other sub-matrices have regular layout transistors. More details about the design of this chip can be found in Ref. [9]. First LF2 chips have been recently delivered.

3.1 Readout system

Initial characterisations were performed using a DAQ system developed at IFAE and based on the Xilinx ZC706 FPGA development board. The full setup is shown in Figure 2(a). LF2 chips are mounted and wire-bonded to small interchangeable PCBs, which are connected to a main readout PCB. The main PCB includes low voltage regulators for powering the chip and connections to apply the reverse bias to the p-n junction. Successful communication with the chip was achieved with the correct reading and writing of the shift registers. The increase of the correspondent currents with the change of DAC register values reproduced the behaviours expected by the design.



(a) DAQ system (b) IV curves

Figure 2: LF2 DAQ system developed at IFAE and electrical characterisation of the test structures. In (a) a picture of the the main PCB holding the wire-bonded chip and connected to the Xilinx board is shown. In (b) the measurement of the current as a function of the bias voltage applied to the test structures of two LF2 chip of different resistivity is shown.

3.2 IV characterisation

A first electrical characterisation has been carried out on the test structures of two chips with different substrate resistivity. The measured test structures consist of a small matrix of 3×3 pixels without electronics. The leakage current as a function of the bias voltage for these two samples is shown in Figure 2(b). In both cases the breakdown occurs at about 55 V. A current rise from few micro amperes up to about 600 µA is observed for the lower resistivity substrate before the

actual breakdown. These results are compatible with expectations from the foundry which foresees a breakdown voltage. around 60 V.

4. Conclusions

To investigate the radiation hardness of the large fill factor design for the upgrade of the ATLAS experiment at HL-LHC different prototypes were fabricated.

The measurements performed on the monolithic part of the H35DEMO prototype, demonstrated the feasibility of producing a full scale DMAPS, which can stand a radiation fluence of $1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ as expected for the outermost layers of the ITk pixel detector. The radiation hardness of this chip was measured at beam tests showing a hit detection efficiency of about 99 % obtained with a bias voltage of 150 V and thresholds lower than 1800 e.

The LF2 prototype was produced in the LFoundry 150 µm CMOS process which includes all the functionalities of the FE-I3 ATLAS chip within a $(50 \times 50)\,\mu\mathrm{m}^2$ pixel cell. A readout system for this chip was developed at IFAE and used to perform preliminary communication tests with the new chip. First measurements of the IV characteristics of test structures present on the chip showed results in agreement with foundry predictions.

The main point which still needs to be addressed by the next generation of large fill factor DMAPS for ATLAS will be the timing and the in-time efficiency to meet the ATLAS specifications. These aspects together with the design of a readout interface compatible with the future ITk hybrid chip, including serial powering, will determine the possibility of employing DMAPS produced in HV/HR-CMOS technology for the pixel detector of ITk.

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