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Paper

Novel Fully Digital-Controlled Point of Load Converter Based on H-bridge DC–DC Converter

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In this paper, we propose a new control algorithm for a novel fully digital-controlled H-bridge DC-DC converter, which can output the power in both boost and buck mode by only rewriting three digital codes: input voltage, output voltage, and maximum load current. In addition, the proposed algorithm improves the transient response.

Keywords: H-bridge, DC-DC converter, programmable power supply, FPGA, sudden load change, parallel connection control

1. Introduction

Point of load converters (POLs) are key parts in increasing the clock frequency of LSIs and reducing the power consumption of the wiring resistance of the circuit board. In order to suppress the voltage fluctuation due to the voltage drop caused by the wiring resistance or the parasitic inductance, it is necessary to place POLs in the immediate vicinity of the LSI. In order to achieve the ultimate miniaturization of power supply, power supply on chip (power-SoC), which can implement power semiconductor devices, passive components, and control circuits on silicon wafers, has attracted much attention and research interest in recent years (Fig. 1) [(1)–(6)].

Power-SoC has two key challenges. First, it is difficult to apply high-frequency (> 10 MHz) DC-DC converters in pulse width modulation (PWM) control. In order to realize power-SoC, high- frequency switching of several tens MHz is required. Therefore, a control technology other than PWM must be developed. Second, the power capacity per POL is small. When we use the power-SoC, the volume is very small and the power density is high because the passive components are small. Therefore, it operates with high efficiency at a light load, and the efficiency drops considerably at a heavy load.

In order to solve these two problems, we proposed a control technique based on parallel connected POLs as shown in Fig. 2 [(7)–(11)]. This control technique only switches the number of working POLs according to the output voltage and does not change the duty ratio. Therefore, this control technique is the open loop type. The proposed control technique can realize high frequency switching and high efficiency operation over a wide load range. Figure 3 shows the control algorithm proposed previously [(8)(10)(11)]. First, the output voltage is read by an FPGA through an AD converter. Subsequently, the output voltage ($V_{out(0)}$) is compared with the target voltage (V_{set}, V_{set} + V_N) and the number of working POLs is varied one by one to regulate the output voltage. However, this control algorithm requires a significant amount of time to change to the appropriate number of POLs to switch the number of POLs to be operated one by one.

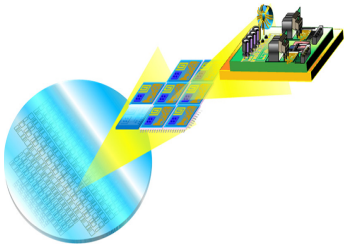

Fig. 1. Power SoC

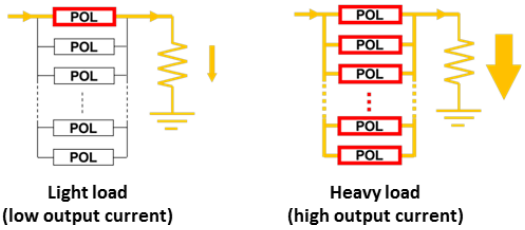

Fig. 2. POL control technology [(7)–(10)]

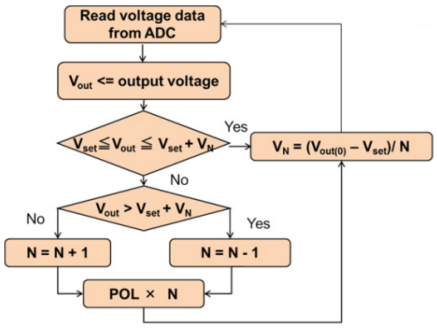

Fig. 3. Previously proposed control algorithm [(8)(10)]

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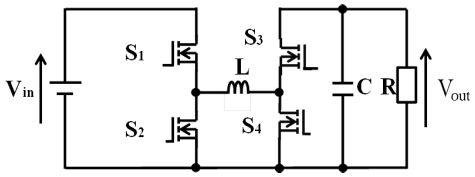


Fig. 4. H-bridge DC-DC converter

In addition, the power-SoC that employs the H-bridge DC-DC converter (Fig. 4) is promising for mobile equipment as the H-bridge converter has a wide range of input voltages due to its capability for various modes of operation for a given output voltage and suitability for a battery-powered system.

In this paper, we propose a new control algorithm for a novel full digital control H-bridge DC-DC converter, which can output the power in both boost and buck modes by rewriting only three digital codes such as the input voltage, output voltage, and maximum load current.

2. Description of the New Control Algorithm for H-Bridge DC-DC Converter

Our previously proposed control technique is the open-loop type and can regulate the output voltage by changing the number of working POLs according to the load current [7]–[11]. For example, a small number of POLs are operated at light loads, and a large number of POLs are operated at heavy loads. Output voltage equations of POLs in the buck mode, boost mode, and buck-boost mode are, respectively, written as

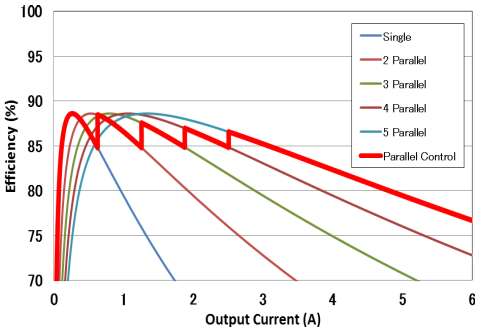
$$V_{out} = D \cdot V_{in} - \frac{r}{N} I \quad \cdots\cdots (1)$$

$$V_{out} = \frac{1}{D'} \cdot V_{in} - \frac{r}{N} I \quad \cdots\cdots (2)$$

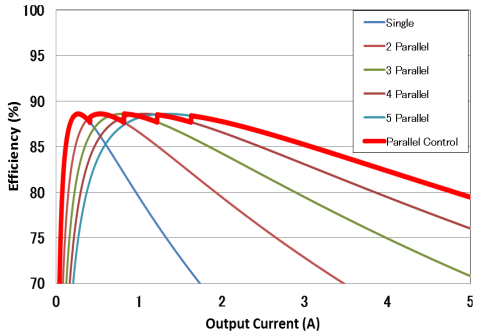
$$V_{out} = \frac{D}{D'} \cdot V_{in} - \frac{r}{N} I \quad \cdots\cdots (3)$$

where D is the duty ratio of "on time", D′ is the duty ratio of "off time", V_{in} is the input voltage, r is the internal resistance, N is the number of POLs connected in parallel, and I is the output current. In this technique, D and r are constant. Thus, the output voltage changes based on I from the equations (1) to (3). Therefore, the output voltage is regulated by adjusting N according to the load current. Figure 5 shows the analysis of the efficiency characteristics of the proposed control technique using equations (1) and (2) [11]. As indicated by the red line in these figures, it is possible to maintain high efficiency over the wide load range.

Figures 6 and 7 show the load characteristics obtained via experiment and the efficiency characteristics of the proposed control technique using equations (1) and (2) [7]. Input voltage for the buck mode is 4.0 V, and boost mode is 1.2 V. From results shown in Figs. 6(a) and 7(a), the slope of the voltage drop becomes gradual as N increases. As indicated by the red line in these figures, the output voltage can be regulated by switching the number of POLs according to the load current. Similarly, it is possible to maintain high efficiency over the wide load range in the boost mode as shown in Fig. 5(b) and Fig. 7(b). However, the efficiency of the buck mode does not remain stable as shown in Fig. 6(b). This result is different from our previously reported experimental [7][11] and analytical

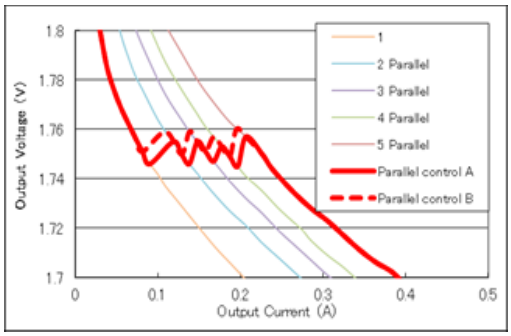


(a) Buck mode

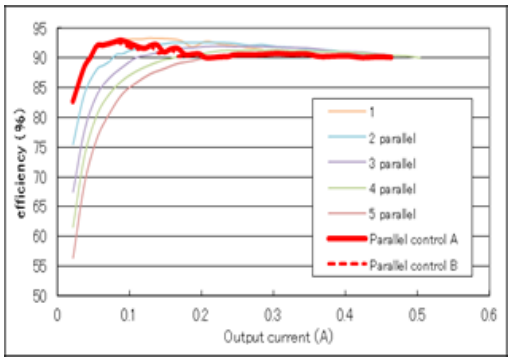


(b) Boost mode

Fig. 5. Analytical efficiency characteristics



(a) Load characteristic



(b) Efficiency characteristic

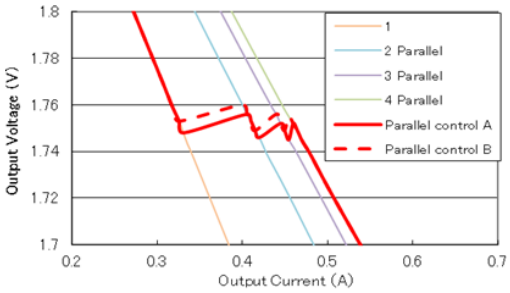
Fig. 6. Experimental results of buck mode

results shown in Fig. 5(a). The different tendency in Fig. 6(b) is caused by the larger conduction loss in the wiring pattern of the printed circuit board.

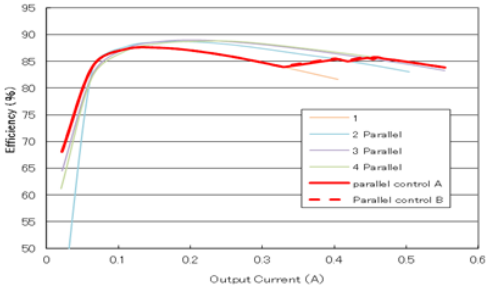
Figure 8 illustrates the dependence of output voltage on output current for each number of working POLs. The slope becomes gradual when the number of working POLs is increased, and the slope is decided by the number of working POLs. The voltage drop between the target voltage and

present output voltage is also defined by the number of working POLs. From the results of Fig. 8, the flowchart for the proposed control algorithm for the buck-boost mode is shown in Figs. 9(a) and (b). The formula used in the proposed algorithm is explained in the range of (i) to (iv) below.

(i) Vout < Vset (Buck-boost mode)
(ii) Vout < Vset (Buck mode)
(iii) Vout < Vset (Boost mode)
(iv) Vout > Vset (Buck-boost mode)



(a) Load characteristic



(b) Efficiency characteristic

Fig. 7. Experimental results of the boost mode

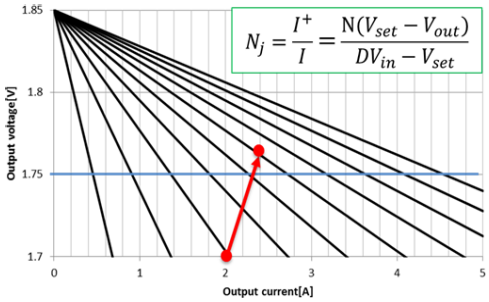
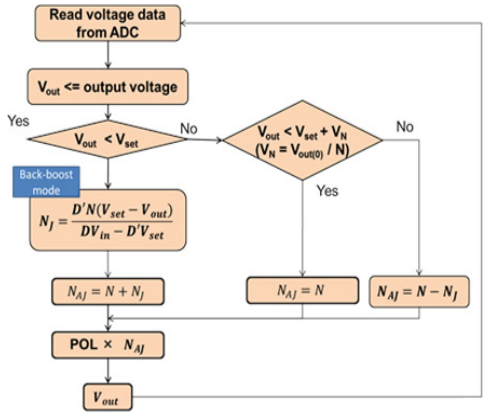
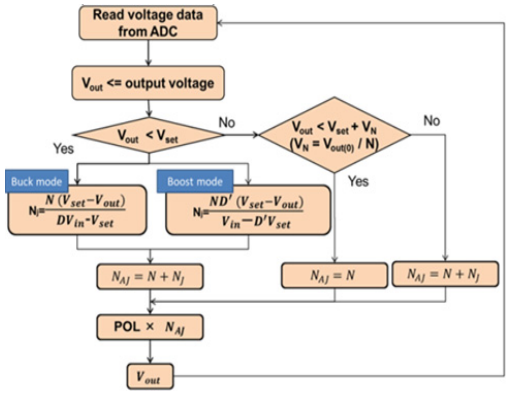


Fig. 8. Behavior of the control algorithm



(a) Control algorithm of buck-boost mode for (i) $V_{out} < V_{set}$



(b) Control algorithm of the buck and boost mode for (iv) $V_{out} > V_{set}$

Fig. 9. New control algorithm

(v) Vout > Vset (Buck mode)
(vi) Vout > Vset (Boost mode)

When the output voltage is lower than the target voltage as shown in (i), the number of working POLs increases. When the output current is increased by the sudden load change, the slope ΔN of the V-I characteristic is as follows.

$$\Delta N = \frac{DV_{in} - D'V_{set}}{D'NI} \cdots\cdots (4)$$

From the equation (4), the current increment I^+ when the output voltage falls below the target voltage is as follows. Also, the output voltage V_{out} is as shown in Equations (1) to (3).

$$I^+ = \frac{D'NI(V_{set} - V_{out})}{DV_{in} - D'V_{set}} \cdots\cdots (5)$$

From the above relations, the number of working converters to be increased, N_J, is

$$N_J = \frac{I^+}{I} = \frac{D'N(V_{set} - V_{out})}{DV_{in} - D'V_{set}} \cdots\cdots (6)$$

Likewise, the numbers of N_J for (ii) and (iii) are, respectively, written as

$$N_j = \frac{I^+}{I} = \frac{N(V_{set} - V_{out})}{DV_{in} - V_{set}} \cdots\cdots (7)$$

$$N_j = \frac{I^+}{I} = \frac{D'N(V_{set} - V_{out})}{V_{in} - D'V_{set}} \cdots\cdots (8)$$

From equations (6) to (8), the number of POLs (N_{AJ}) to be operated can be determined as follows.

$$N_{AJ} = N + N_J \cdots\cdots (9)$$

Also, as shown in (iv), when the output voltage is higher than the target voltage, the output voltage is set to the target voltage by decreasing the number. When reducing the number, hysteresis V_N is used to avoid the oscillation of the output voltage. The conditional expression for reducing one POL is as follows.

$$V_{set} + V_N \cdot 2 > V_{out} \geq V_{set} + V_N \cdot 1 \cdots\cdots (10)$$

The number of N_J to be reduced is given by equation (10).

$$N_J = \frac{V_{out} - V_{set}}{V_N} \cdots\cdots (11)$$

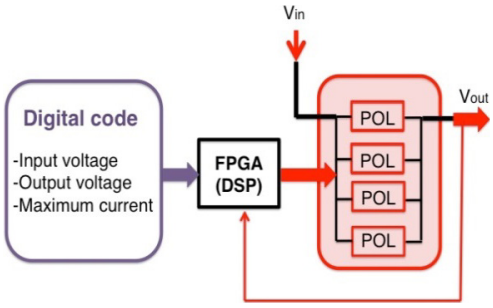


Fig. 10. System control by FPGA [8]–[10]

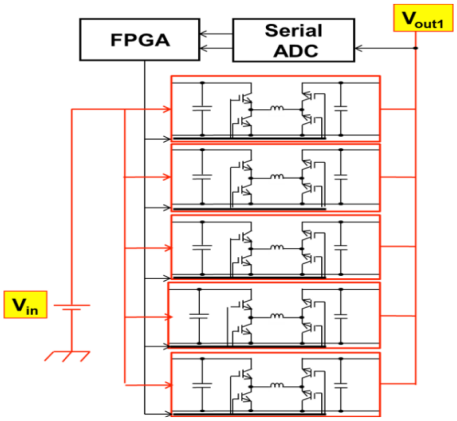


Fig. 11. Block diagram of experimental system

Accordingly, the number of POLs running (N_{AJ}) is obtained as follows.

$$N_{AJ} = N - N_J \cdots\cdots (12)$$

Also in (v) and (vi), the number of units can be controlled in the same way as in (iv).

Figure 10 illustrates the digital control system used in this study [8]–[10]. FPGA controls parallel connected POLs by feeding the control signal from FPGA to the switches (S1-S4) of the H-bridge DC-DC converter. We can set up any output voltage, but can input only three digital codes such as input voltage, output voltage, and maximum current to FPGA. So, it is not necessary to replace external parts for adjusting the parameters.

3. Experimental Results and Discussions

Figure 11 illustrates the block diagram of the experimental system for evaluations. The H-bridge DC-DC converter is used. Figure 12 shows the experimental circuits. Table 1 shows the circuit parameters and system specifications for evaluations. In this system, five DC-DC converters connected in parallel were used. The output voltage was input to the FPGA after it was digitized by a serial-type AD converter, and a gate drive signal was output to the converters based on the control algorithm. The target voltage (V_{set}) was set to 1.75 V. In this experiment, we used the buck mode of the H bridge DC-DC converter.

Transient responses of the (a) previously and (b) newly proposed control algorithms are shown in Figs. 13(a) and (b), respectively. The buck mode was used. The load current (I_{out}) was changed from 70 mA to 300 mA. Also, the settling time is defined as the time until the voltage stabilizes within

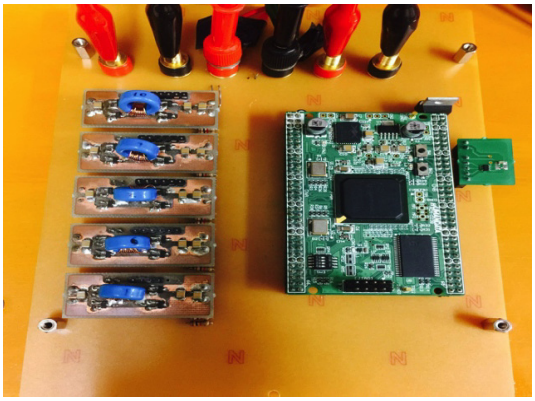
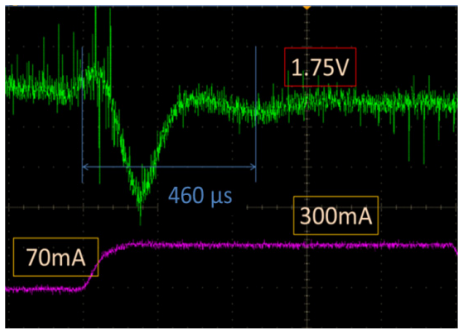


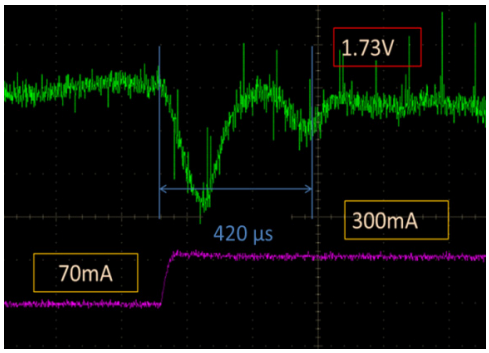
Fig. 12. Circuit used for experiment

Table 1. Circuit parameters and system specifications

Symbol	Description	Value
V_{in}	Input voltage	4 V
V_{out}	Output voltage	1.75 V
L_o	Inductance	25 µH
r_{DC}	Internal resistance	400 mΩ
C_o	Output capacitance	47 µF
f_s	Switching frequency	300 kHz
D	Duty ratio	50 %
N	Number of active POLs	1-5



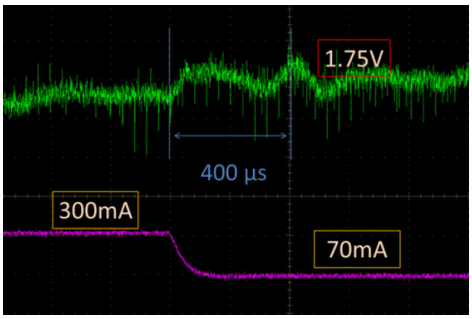
(a) Previously algorithm [10].



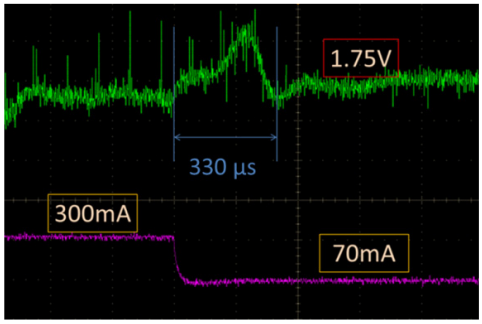
(b) Proposed algorithm.

Fig. 13. Output voltage waveform when output current is changed from 70 mA to 300 mA (buck mode)

±5% after the load current changes. In Fig. 13(a), the output voltage stabilized around 1.73 V at 460 μs after a sudden load change. In Fig. 13(b), after a sudden load change, the output voltage stabilized around 1.73 V at 420 μs. Transient response of the (a) previously and (b) newly proposed control algorithms are shown in Figs. 14(a) and (b), respectively. The buck mode was used. The load current (I_{out})



(a) Previously algorithm [10].



(b) Proposed algorithm.

Fig. 14. Output voltage waveform when output current is changed from 300 mA to 70 mA (buck mode)

Table 2. Calculation results of the damping coefficient

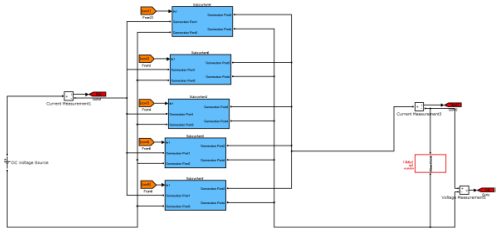
	Switching Frequency			
	300 kHz		30 MHz	
	The number of working POLs		The number of working POLs	
	1	5	1	5
Damping coefficient δ	0.616	0.280	0.309	0.143

Table 3. Calculation results of the settling time

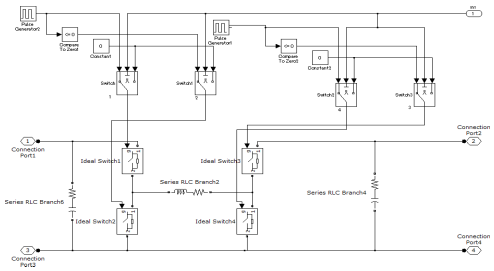
	Switching Frequency	
	300 kHz	30 MHz
Settling Time	437 µs	8.72 µs

Table 4. Circuit parameters and system specifications for simulation

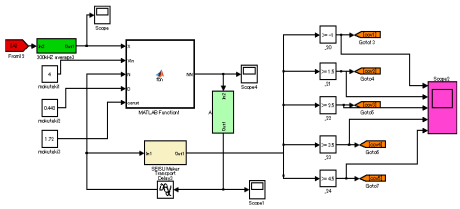
Symbol	Description	Value		
V_{in}	Input voltage	4 V	4 V	4 V
V_{out}	Output voltage	1.75 V	1.75 V	1.75 V
L_o	Inductance	0.25 µH	0.75 µH	25 µH
r_{DC}	Internal resistance	200 mΩ	210 mΩ	400 mΩ
C_o	Output capacitor	0.47 µF	1.41 µF	47 µF
f_s	Switching frequency	30 MHz	10 MHz	300 kHz
D	Duty ratio	50 %	50 %	50 %
N	Number of active POLs	1-5	1-5	1-5



(a) Structural diagram of the entire configuration circuit.



(b) H-bridge DC-DC convertor.



(c) Structure drawing of control unit.

Fig. 15. Simulated H-bridge converter

was changed from 315 mA to 70 mA. In Fig. 14(a), the output voltage stabilized around 1.752 V at 400 μs after the sudden load change. In Fig. 14(b), after the sudden load change, the output voltage stabilized around 1.752 V at 300 μs. These results showed that the newly control algorithm showed faster response time than the previously one. We consider that the fast response time is realized because the excess processing time disappears by the appropriate number of working POLs is calculated and changed. Also, in Fig. 14, the overshoot is larger for the proposed method than for the previous method. From this result, we consider that the time until the number of working POLs starts to change is slightly later than with the previous method due to the need for complex calculations.

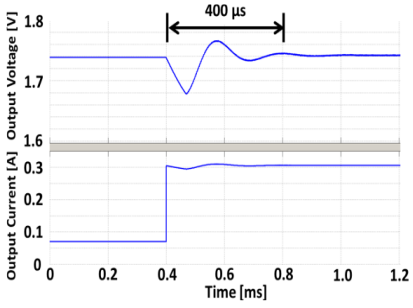
In this system, the transient response time of the output voltage is determined by the characteristics of the LC filter and the processing speed, which changes the number of working POLs. For that reason, we analyze how the transient response is affected by the transfer function when the frequency of the circuit is increased in the future. The dynamic characteristics of the H-bridge converter operating in the buck mode are identical to those of the basic buck-converter. It is well known that, for the buck converter, the damping coefficient δ and the settling time T_s when the damping coefficient is one or less can be, respectively, written as

$$\delta = \frac{r_{DC}}{2}\sqrt{\frac{C_o}{NL_o}} \quad \cdots\cdots (13)$$

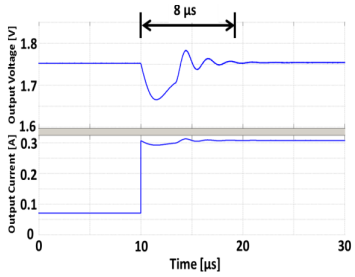
$$T_S = \frac{7L_o}{r_{DC}} \quad \cdots\cdots (14)$$

where r_{DC} is the internal resistance, C_o is the output capacitor, N is the number of working POLs, and L_o is the inductance.

Table 2 and Table 3 show the results of the calculation by using equation (13), equation (14), and the parameters of Table 4. In the case of a switching frequency 10 MHz or more, we assume an air core on-chip inductor, which is reported in the previous research [12]. Comparing Fig. 13(b) with Table 3, the settling time is almost the same at a switching frequency of 300 kHz. Also, it can be considered that the variation of the damping coefficient is the reason for the transient response of Fig. 14(b) being faster than that of Fig. 13(b). From Table 2, the damping coefficient decreases and the ringing increases as the number of working POLs increases. In Fig. 13(b), the

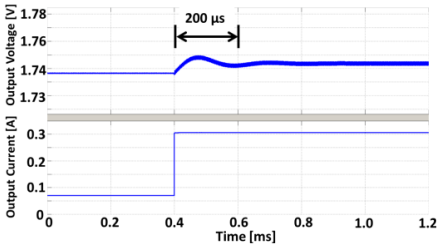


(a) fs = 300 kHz.

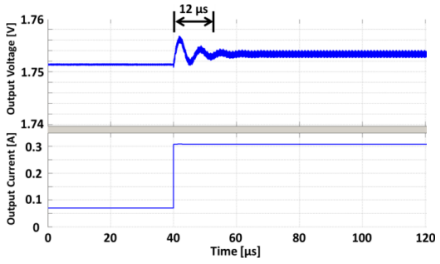


(b) fs = 30 MHz.

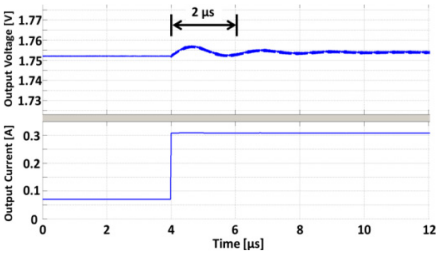
Fig. 16. Output voltage waveform when output current is changed from 70 mA to 300 mA (buck mode)



(a) fs = 300 kHz.



(b) fs = 10 MHz.



(c) fs = 30 MHz.

Fig. 17. Output voltage waveform at load sudden changing in feed forward control

damping coefficient decreases and the ringing increases at a sudden change in the load. In Fig. 14(b), the damping coefficient increases and the ringing decreases at a sudden load change. Therefore, it can be considered that the transient response of Fig. 14(b) is faster than Fig. 13(b).

Next, we obtained the output voltage waveform for the transient response from simulations (MATLAB/Simulink, Figs. 15(a), (b) and (c)). The output voltage waveforms are shown in Figs. 16(a) and (b). The circuit parameters and specifications are listed in Table 4. Comparing Fig. 16(b) with Table 3, the settling time is almost the same. Therefore, these results show that the transient response improves by reducing the inductance and increasing the internal resistance.

The output voltage waveforms in feed forward control are shown in Fig. 17. Therefore, these results show that the transient response improves by reducing the inductance and increasing the internal resistance. In addition, it can be verified that the transient response improves when the feed forward control is used.

4. Conclusions

We proposed a novel, full digital control H-bridge DC-DC converter and its control algorithm. The proposed control algorithm can boost/buck the voltage simply by inputting the input voltage, output voltage, and maximum load current without changing any external part. The proposed digital control H-bridge DC-DC converter can regulate the output with high efficiency changing only three digital codes. In addition, the newly proposed control algorithm can provide an approximately 10% reduction in the settling time. In our future work, we may consider choosing appropriate circuit parameters and an AD converter that can cope with the processing speed of the control function.

References

(1) S. Matsumoto, M. Mino, and T. Yachi: “Integration of a power supply part for a system on silicon”, IEICE Trans. Communication and Computer Science, Vol.80-A, No.2, pp.276–282 (1997)

(2) S. Matsumoto: “Future Power Electronics for Realizing Sustaining Society”, International Workshop on Power Supply On Chip 2010 (PwrSoc’10), Session 6.6 (2010)

(3) T.P. Chow: “GaAs p-HEMT based power ICs for high frequency switching converter applications”, International Workshop on Power Supply On Chip 2010 (PwrSoc’10), Session 2-3 (2010)

(4) D. Anderson: “Applications of power SIP/pwrSoC products”, International Workshop on Power Supply On Chip 2012 (PwrSoc’12), Session 1-6 (2012)

(5) F. Carobolante: “Power Supply on Chip: from R&D to commercial products”, International Workshop on Power Supply On Chip 2014 (PwrSoc’14), Plenary Session 3 (2014)

(6) S. Sanders: “The Road to Integrated Power Conversion via the Switched Capacitor Approach”, International Workshop on Power Supply On Chip 2014 (PwrSoc’14), Plenary Session 2 (2014)

(7) T. Yamamoto, J. Rikitake, S. Matsumoto, and S. Abe: “A New Control Strategy for Power Supply on Chip Using Parallel Connected DC-DC Converter”, IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS) 2013, pp.109–112 (2013)

(8) T. Yamamoto, S. Abe, and S. Matsumoto: “A Novel Concept of Digitally Controlled Multiple Output POL for Power Supply on Chip”, International Telecommunication Energy Conference 2014 (Intelec2014), PO-33 (2014)

(9) M. Higashida, T. Yamamoto, S. Abe, and S. Matsumoto: “A Concept of Field Programmable Power Supply Array Utilizing Power Supply on Chip—Fully digital controlled multiple input and output voltages POL—”, 17th European Conference on Power Electronics and Applications (EPE 2015, ECCE Europe), LS1e.4 (2015)

(10) T. Hashiguchi, S. Abe, and S. Matsumoto: “A fully digitally controlled multiple input and output voltage buck-boost POL for power supply on chip”, International Telecommunication Energy Conference 2015 (Intelec2015), pp.1081–1096 (2015)

(11) S. Abe, S. Matsumoto, and T. Ninomiya: “A novel load regulation technique

for power-SoC with parallel connected POLs", IEEJ Journal of Industry Application, Vol.4, No.6, pp.732–737 (2015)
(12) K. Ono, K. Hiura, and S. Matsumoto: "Design Consideration of a 3D Stacked Power Supply on Chip", Electronic Components and Technology Conference (ECTC) 2018, session 27.7 (2018)

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