
# Power-Aware Testing For Low-Power VLSI Circuits

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Xiaoqing Wen

Department of Computer Systems and Electronics
Kyushu Institute of Technology
Kawazu 680-4, Iizuka, 820-8502, Japan
wen@cse.kyutech.ac.jp

***Abstract***: *Low-power VLSI circuits are indispensable for almost all types of modern electronic devices, from battery-driven mobile gadgets to harvested-energy-driven wireless sensor systems. However, the testing of such low-power VLSI circuits has become a big challenge, especially due to the excessive power dissipation during scan testing. This paper will highlight three major test-power-induced problems (namely heat, false failures, clock stretch) and describe how to mitigate them with power-aware VLSI testing. Future research topics in this field will also be discussed.*

## 1. Introduction

VLSI circuits are at the hearts of all electronic devices used in modern industries as well as daily lives. More sophisticated functions are always important for VLSI circuits; however, in recent years low power has become an even more important requirement. This is because most VLSI circuits are now used in battery-driven mobile gadgets, such as smart phones, tablets, cameras, activity monitors, etc. Given the fact that harvested-energy-driven wireless sensor systems will be widely deployed in the era of IoT, *low-power VLSI circuits* will become more and more critical in the future.

***VLSI testing*** is the process of applying special stimuli to a VLSI chip, measuring its responses, and by which determining whether the chip is free of physical defects inducted in production or during field application [1]. Clearly, testing is indispensable for guaranteeing the quality and reliability of VLSI chips.

*Scan testing* is the most widely adopted methodology for cost-effectively testing a logic VLSI circuit [1]. Its essence is to replace all functional flip-flops in the circuit with scan flip-flops of two operational modes, *shift* and *capture*, controlled with a *scan enable* (*SE*) signal. As illustrated in Fig. 1, the inputs to the combinational portion of the *circuit-under-test* (*CUT*) comprise *primary inputs* (*PI*s) and *pseudo primary inputs* (*PPI*s) as outputs from scan flip-flips; the outputs from the combinational portion comprise *primary outputs* (*PO*s) and *pseudo primary outputs* (*PPO*s) as inputs to scan flip-flips. In *shift mode* (*SE* = 1), scan flip-flops are connected into one or more shift registers (called *scan chains*), over which the *shift operation* is conducted to load a test stimulus *A* to PPIs. The test response consists of one part directly observable at POs and another part appearing at PPOs. In *capture mode* (*SE* = 0), scan flip-flops operate separately as functional flip-flops, over which the *capture operation* is conducted to load the test response *B* at PPOs into scan flip-flops so that the next shift operation bring them out of the circuit for observation. Scan testing is conducted by repeating shift and capture operations to apply all test vectors and observe all corresponding test responses.

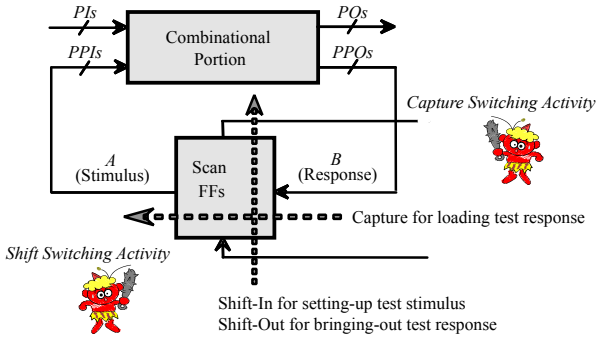



**Fig. 1 Basic concept of scan testing for VLSI logic circuits**.

## 2. Test-Power-Induced Problems

As shown in Fig. 1, scan testing causes two types of test switching activity: *shift switching activity* and *capture switching activity*, Such test switching activity results in significantly elevated power dissipation during test [2, 3]. Fig. 2 illustrates the impact of test power in at-speed scan testing. Here, the *launch-on-capture* (*LOC*) clocking scheme is assumed, where transitions are launched by the first capture clock pulse $C_1$ and the responses to the transitions are captured by the second capture clock pulse $C_2$. "*At-speed*" means that the test cycle be set to the functional clock period in order to detect for excessive delay increase caused by physical defects along sensitized logic paths. From Fig. 2, it can be seen that the impacts of test power in at-speed scan testing are threefold, as described below.

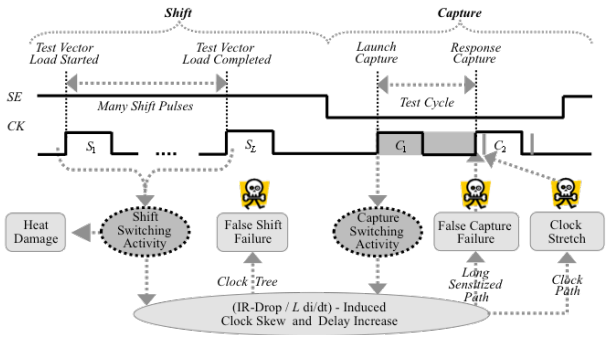



**Fig. 2 Impacts of test power in LOC-type at-speed scan testing**.

### 2.1 Heat Damage

Since a large number of shift clock pulses need to be applied for each shift operation, shift switching activity may cause accumulative impact in term of excessive heat dissipation. This causes extremely high temperature during scan testing, resulting in wafer/chip damage and/or reliability degradation [2].

### 2.2 False Failures

In normal VLSI testing, a chip failing in test indicates that it contains physical defects [1]. However, excessive test switching activity in both shift and capture modes may causes false failures for defect-free chips [2, 3], resulting in costly yield loss [4]. Shift switching activity may cause severe IR-drop and *Ldi/di* induced skew in the clock tree of a circuit, resulting in hold time violations in scan chains and consequently failures in scan shift, i.e., *false shift failures* [4]. On the other hand, capture switching activity triggered by the first capture clock pulse ($C_1$ in Fig. 2) occurs in the neighborhood (called *impact area*) of a logic path, causing IR-drop at its on-path gates and thus increasing the delay along the path. If the logic path is sensitized and the increased delay is larger than the slack of the logic path, a *false capture failure* will occur at the endpoint of the logic path at the second capture clock pulse ($C_2$ in Fig. 2) for a defect-free circuit. False failures are a severe test-power-induced problem, especially for high-speed / low-power VLSI circuits [5, 6].

### 2.3 Clock Stretch

Capture switching activity triggered by the first capture clock pulse ($C_1$ in Fig. 2) also occurs in the impact area of the clock path corresponding to a sensitized logic path. This causes IR-drop at the on-path clock buffers of the clock path and increase the delay of the clock path. As a result, the test cycle becomes larger than the functional clock period. This phenomenon is known as *clock stretch* [7], which makes testing slower (e.g., as much as 15%) than "*at-speed*". This is a major cause for test quality degradation, especially for deep-submicron VLSI circuits with small-delay defects.

## 3. Power-Aware Testing

Test power problems in at-speed scan testing are getting worse with ever-decreasing power supply voltages, ever-increasing clock frequencies, ever-growing circuit sizes, and ever-shrinking process features [8]. As a result, test power needs to be explicitly considered in VLSI testing. In the following, typical power-aware test techniques are described.

### 3.1 Test Heat Reduction

A highly effective and scalable technique is called *scan chain segmentation*, partitions each scan chain into $N$ segments and operates the segments one at a time for each scan chain during scan shift [4]. An example is shown in Fig. 3. Generally, this technique reduces the average power dissipated during scan shift by a factor of $N$, without impacting test time, test quality, and test costs.

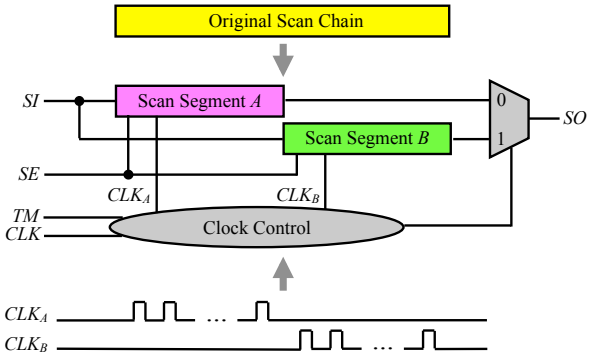



**Fig. 3 Scan chain segmentation.**

### 3.2 False Failure Reduction

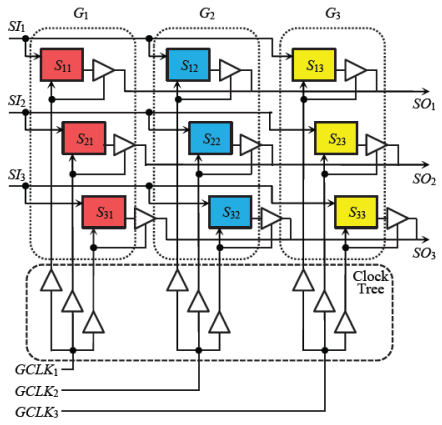
As described in Subsection 2.2, there are two types of false failures, namely false shift failures and false capture failures. The former is caused by hold-time violations of scan FFs due to the instantaneous impact of shift power on the clock tree of a circuit-under-test [4], while the latter is caused by setup-time violations of scan FFs due to the instantaneous impact of capture power on sensitized logic paths in a circuit-under-test [5]. In the following, two state-of-the-art techniques for mitigating such false failures will be described.

#### 3.2.1 Mitigation of False Shift Failures

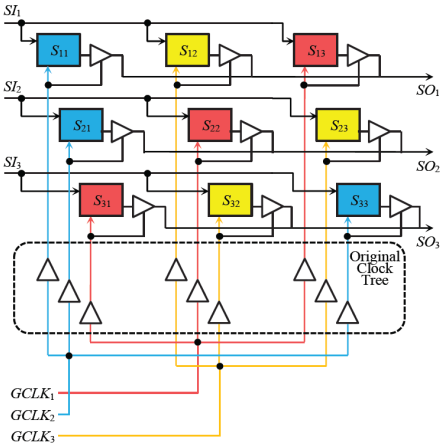
The clock skew caused by shift switching activity needs to be reduced in order to mitigate false shift failures. The *LCTI-SS (Low-Clock-Tree-Impact Scan Segmentation)* technique [9] achieves this by optimizing the design of scan chain segmentation [4].

Fig. 4 shows an example of the LCTI-SS scheme. Fig. 4 (a) is the original scan segmentation scheme and Fig. 4 (b) is its timing diagram [4]. In this example, shift switching activity can be theoretically reduced to one-third of its original level. However, this original scan segmentation scheme [4] can only reduce shift switching activity in a global manner, making it less effective on reducing false shift failures since they are caused by local skews in the clock tree. To solve this problem, the LCTI-SS scheme [9] further tries to carefully re-group the scan segments in a manner that the maximum and average values of the local skews in the clock tree can be minimized.

The basic idea of the LCTI-SS scheme is illustrated in Fig. 4, in which there are three scan chains, each with three scan segments. The current grouping is $\{\{S_{11}, S_{21}, S_{31}\}, \{S_{12}, S_{22}, S_{32}\}, \{S_{13}, S_{23}, S_{33}\}\}$. However, in the case of this grouping, when the group $\{S_{11}, S_{21}, S_{31}\}$ is shifted, excessive shift switching activity may occur and cause severe clock skew in the clock tree related to $S_{11}$, $S_{21}$, and $S_{31}$. The LCTI-SS scheme tries to find a better grouping of scan segments. For example, a new grouping such as $\{\{S_{13}, S_{23}, S_{31}\}, \{S_{11}, S_{21}, S_{31}\}, \{S_{12}, S_{23}, S_{32}\}\}$ may reduce shift switching activity in targeted areas in the corresponding clock tree. Experimental results show that the LCTI-SS scheme can achieve double-digit reduction for large benchmark circuits [9].




(I) Original scan chain segmentation




(II) LCTI scan chain segmentation

**Fig. 4 Basic idea of the LCTI scheme**.

### 3.2.2 Mitigation of False Capture Failures

As discussed in Subsection 2.2, *capture switching activity* can increase the delay of a logic path. The extra delay along a *long sensitized path* (*LSP*) may result in a false capture failure. Therefore, in order to avoid false capture failures, capture switching activity around an LSP needs to be reduced.

**Definition 1**: The *aggressor region* of a gate $G$, denoted by $AR(G)$, is composed of aggressor cells (gates and FFs) whose transitions strongly impact the supply voltage of $G$.

**Definition 2**: The *impact area* of $P$, denoted by $IA(P)$, consists of the aggressor regions of all on-path gates ($G_1$, $G_2$, . . ., $G_n$) of $P$. That is, $IA(P) = AR(G_1) \cup AR(G_2) \cup \ldots \cup AR(G_n)$, as illustrated in Fig. 5.

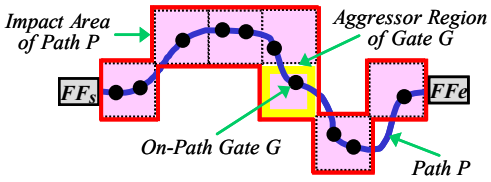



**Fig. 5 Impact area**.

The technique proposed in [6] for mitigating false capture failures is illustrated in Fig. 6. Here, a test cube $C_1$ (with don't-care bits or *X*s) is generated and then turned into a test vector $V_1$ (without *X*s) by detection-oriented *X*-filling (e.g., *random-fill*). A conventional test generation flow ends here, but the proposed technique continues with two more phases as follows:

- ***Rescue***: *LSP-based capture switching activity checking* (①) identifies all *risky paths* of $V_1$ by checking the *capture switching activity* (*CSA*) in the impact area of each *long sensitized path* (*LSP*) under $V_1$. Suppose that $P_a$ and $P_b$ are found to be risky paths. Then, *impact-X-bit restoring* (②) identifies those bits in $V_1$ that are originally *X*-bits in $C_1$ (before *X*-filling) and can reach the impact areas of $P_a$ and $P_b$, and turns them back into *X*-bits (*impact-X-bits*) to create a new test cube $C_2$. After that, *focused low-CSA X-filling* (③) is conducted to turn $C_2$ into $V_2$ with reduced capture switching activity in the impact areas of $P_a$ and $P_b$.
- ***Mask***: *LSP-based capture switching activity checking* (④) identifies that $P_a$ is now safe but $P_b$ is still risky under $V_2$. In this case, *uncertain-test-response masking* (⑤) is conducted to place an *X* at the endpoint (FF input) of $P_b$ in the test response to $V_2$. This makes the uncertain value observed by the FF to be ignored in test response comparison, thus avoiding yield loss induced by false capture failures. Note that this masking needs no additional circuitry.

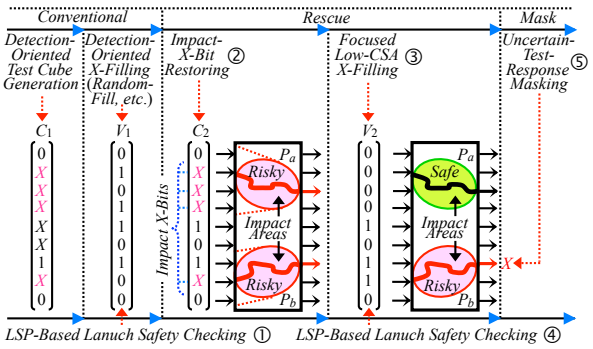



**Fig. 6 Technique for mitigating false capture failures**.

### 3.3 Clock Stretch Reduction

The technique proposed in [6] can be extended for reducing clock stretch. The basic idea is to reduce switching activity in the impact areas of clock paths so as to reduce their test clock stretch. The first step is to select clock paths to be targeted. This is because not all clock paths have the same impact on at-speed test quality in terms of test clock stretch. For example, the clock stretch of the clock path for the endpoint FF of an un-sensitized logic path has no adverse impact on at-speed test quality, while the clock stretch of the clock path for the endpoint FF of a sensitized logic path is less severe if the path is short. Therefore, the sensitization status as well as the length of a logic path need to be considered in order to determine whether its corresponding clock path needs to be targeted in clock stretch reduction or not.

**Definition 3**: A ***target clock path*** of a test vector $V$ is the clock path for the endpoint FF of a *long sensitized* (logic) *path* (*LSP*) of the test vector $V$.

Fig. 7 shows an illustrative example of the technique [6] for reducing clock stretch, which is conducted after the processing shown in Fig. 6. Here, *target clock path selection* identifies two target clock paths of the test vector $V_3$, namely, $cp_1$ and $cp_2$. Since all of the *free bits* (*e*, *h*, *i*) of $V_3$ can reach the impact areas of $cp_1$ and $cp_2$, all of them are turned into *clock-path-impact X-bits*. Then, 1, 0, and 1 are filled into the three *X*-bits at *e*, *h*, and *i*, respectively, for reducing the local LSA in the impact areas of the two target clock paths ($cp_1$ and $cp_2$).

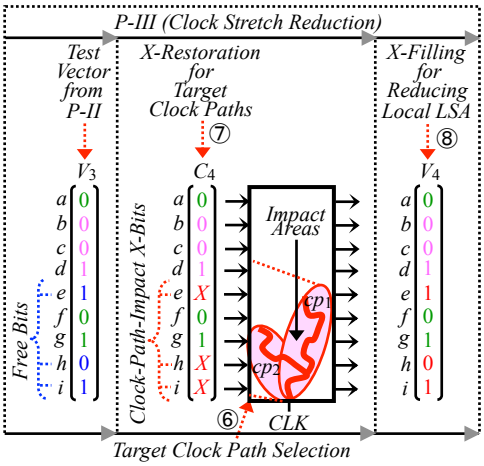



**Fig. 7 Technique for mitigating false capture failures.**

## 4. Future Research Topics

Various techniques have been proposed so far for mitigating the impacts of scan test power [2, 3, 8]. However, more sophisticated techniques still need to be developed in this field. The following is a list of major future research topics.

- *Fast and accurate vector-based and vector-less switching activity analysis under process variance*
- *Scalable and effective test power management in test compression and logic BIST*
- *IP development with predefined low-switching-activity test data and/or infrastructure*
- *On-chip-measurement-based test power control*
- *Fault diagnosis under power supply noise*

In the following, switching activity analysis will be discussed in more detail. As illustrated in Fig. 8, ideal switching activity checking is based on analyzing whether there will be excessive heat and/or excessive delay increase along long sensitized paths and clock paths. However, this ideal approach is prohibitively expensive in terms of computation time and data volume. In reality, simplified metrics, such as *weighted switching activity* (*WSA*), have to be used for switching activity checking. However, these metrics are usually not accurate enough, making it hard to know whether a test vector is safe with respect to test power or whether test power is properly managed. Therefore, establishing a fast and accurate procedure for analyzing switching activity in test mode is extremely important.

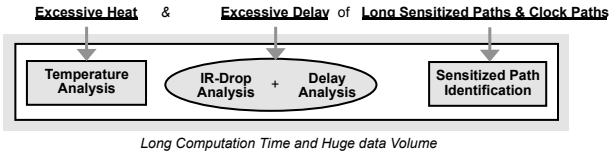



**Fig. 8 Need for fast & accuarte switching activity analysis.**

It is also important to understand that the new target of *test power management* must be added to the existing targets of at-speed scan testing, i.e., *high test quality* and *low test cost*. As illustrated in Fig. 9, test power should be controlled properly in a holistic manner by carefully balancing the impacts of test power management on test quality and test costs. The general rule is that test power management must not degrade test quality and should be traded-off with test costs as optimally as possible.

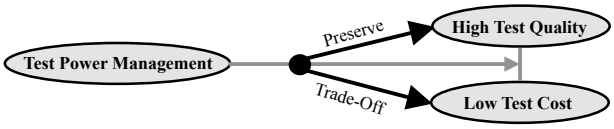



**Fig. 9 Holistic view of various targtes in scan testing.**

## 5. Summary

This paper has highlighted three major problems in the scan testing of low-power VLSI circuits. Typical techniques for mitigating these problems have also been described. More research needs to be conducted in the future, with some important topics listed in this paper.


### Acknowledgements

This work was jointly supported by JSPS KAKENHI Grant Numbers 25280016 and 15K12003, and JSPS Grant-in-Aid for the Promotions of Bilateral Joint Research Projects (Japan-Germany).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