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Electrical and Structural Analysis of CNT-Metal Contacts in Via Interconnects

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Electrical and Structural Analysis of CNT-Metal Contacts in Via Interconnects

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Abstract- **Vertically aligned carbon nanotubes grown by plasma-enhanced chemical vapor deposition offer a potentially suitable material for via interconnects in next-generation integrated circuits. Key performance-limiting factors include high contact resistance and low carbon nanotube packing density, which fall short of meeting the requirements delineated in the ITRS roadmap for interconnects. For individual carbon nanotube s, contact resistance is a major performance hurdle since it is the dominant component of carbon nanotube interconnect resistance, even in the case of vertically aligned carbon nanotube arrays. In this study, we correlate the carbon nanotube-metal interface nanostructure to their electrical properties in order to elucidate growth parameters that can lead to high density and low contact resistance and resistivity.**

Keywords-carbon nanotube; via; resistance; contact resistance.

I. INTRODUCTION

Nanocarbons, in general, and Carbon Nanotubes (CNTs) in particular are expected to be implemented in next-generation integrated circuit (IC) technologies, due to their high tolerance to electromigration and high current-carrying capacity [1-3]. Moreover, with resistivities reported in the range of 10^{-6} Ωcm for single-walled CNTs [3], they are indeed viable materials to replace copper (Cu) in vias and interconnects for ICs with sub-20 nm feature sizes. Attaining a CNT resistivity of 10^{-6} Ωcm for functional devices or simply meeting the industry requirement for interconnect resistance [1] is a daunting challenge for researchers, but its superior current capacity over Cu is already a distinct advantage, as the current capacity of Cu in the sub-20 nm regime is expected to be significantly less than half of its bulk value of 10^6 A/cm^2 [4]. Aside from resistivity, the greatest challenge to overcome is minimization of the resistance between CNT and metal contact, which critically depends on CNT growth and subsequent device fabrication processes.

Recently, we reported individual CNT resistances of about 1 kΩ in a vertically aligned CNT array with average diameter ~100 nm and length ~1.5 μm [4]. Of such resistance, about 800 Ω is attributed to the contact between the CNT and metal electrodes. These results are consistent with prior reports using similar techniques [5,6]. High-resolution transmission electron microscopy (HRTEM) images revealed a clean interface between CNT and the underlayer metal, albeit with significant surface asperity and large metal grains [4].

Further, energy-dispersive x-ray spectroscopy (EDS) showed significant amounts of oxygen and nitrogen present in the interfacial region, which could negatively impact the contact resistance.

Currently, we have succeeded in reducing the average diameter of the PECVD-grown CNTs to about 15 nm, while increasing the packing densities to >10^{11} cm^{-2}. This result is comparable to recent work reported for CNT vias [5] and is closer to values delineated by the current ITRS roadmap [1]. However, initial current-voltage (*I-V)* measurements suggest that the underlayer metal surface graininess is the primary cause for high contact resistance. To improve CNT electrical behavior, we have made changes to the CNT growth process to improve the as-grown CNT-metal contact with the primary objective of reducing the contact resistance, thus yielding a total CNT via resistance closer to that of Cu.

In this paper, the CNT-metal interface is studied extensively using HRTEM to gain a better understanding of the physical origin of contact resistance, and to provide the needed feedback for process improvement. *I-V* characteristics of individual CNTs are measured to allow extraction of electrode contact resistance and CNT resistivity. Correlation of these electrical performance parameters for CNTs grown under different conditions with their respective HRTEM images provides the needed insight that will lead to the eventual functionalization of CNT via interconnects.

In the next sections, we will elaborate on the device fabrication, followed by the characterization of these devices using HRTEM and electrical measurements.

II. CNT GROWTH AND DEVICE FABRICATION

Titanium (Ti) is an excellent underlayer metal due to its compatibility with current IC technology.

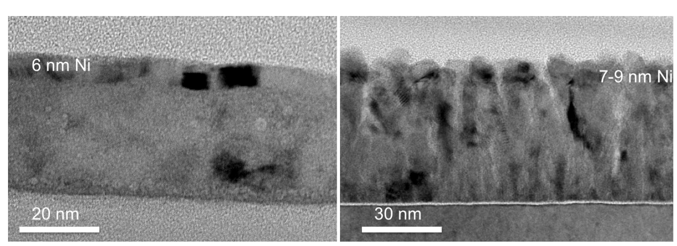

Fig. 1. Cross-sectional SEM images of substrates consisting of Ni catalyst film on Ti underlayer. Smooth or continuous films (a) results in lower contact resistance compared with grainy substrate (b).

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High-density CNT growth is observed on Ti film with significant surface roughness, where the Ti grains serve as templates for the nickel (Ni) catalyst film deposition, as shown in Fig. 1. CNTs appear to grow on the grain boundaries, and smaller grains result in higher density. Different film deposition conditions can be used to study the effect of graininess on CNT packing density and diameter distribution, as well as contact resistance.

The starting wafer consists of a thin silicon dioxide layer that serves as a diffusion barrier to subsequent film deposition. The Ti underlayer and Ni catalyst films are deposited using magnetron sputtering. This underlayer serves as the base electrode, and provides a clean interface to the as-grown CNTs. CNTs are then grown using a plasma-enhanced chemical vapor deposition (PECVD) reactor, with acetylene as the carbon source and ammonia as reducing agent. PECVD growth parameters are optimized for the Ni/Ti layers to yield the highest CNT packing density. Smooth Ti substrates with 6 nm of Ni yield higher CNT array density (1.9 x 10^{10} cm^{-2}), than grainy substrates (1.2 x 10^{10} cm^{-2}) with ~8 nm of Ni. Scanning Electron Microscope (SEM) images of as-grown CNT arrays are shown in Fig. 2.

After CNT growth, the exposed surface is encapsulated in a polymer matrix to fill the interstitial spacing within the CNT arrays. This provides electrical isolation among the CNTs, while providing the structural rigidity necessary to land the nanoprober tips for electrical measurements. The CNT surface is then planarized using ion-beam sputtering and mechanical polishing. Sections of the same substrate are further polished to different lengths for electrical probing, as described below.

III. DEVICE CHARACTERIZATION

A. Electrical Measurements

Due to the geometry of the vertically-aligned CNT array, a four-point-probe measurement is not feasible to directly

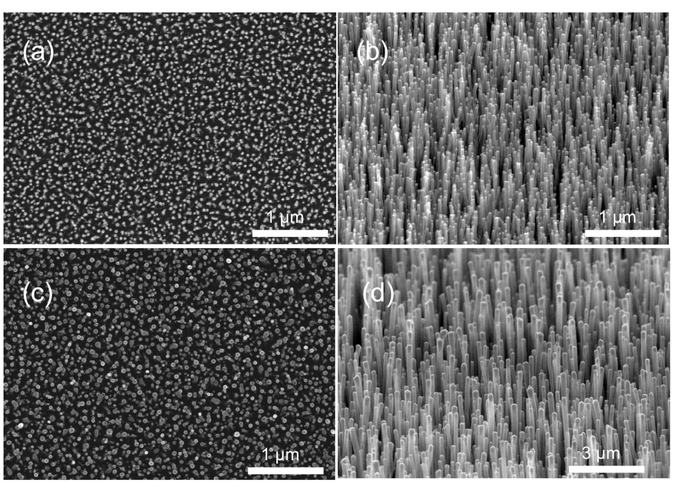

Fig. 2. Top-view (a) and (b) tilted-view SEM images of as-grown CNT arrays on smooth Ti underlayer with density ~ 1.9 x 10^{10} cm^{-2}. (c) Top-view and (d) tilted-view of as-grown CNT on grainy substrate with density ~ 1.2 x 10^{10} cm^{-2}. Growth on smooth Ti substrate shows smaller average diameter and narrower diameter distribution.

determine the CNT resistivity and contact resistance. To extract these values, a linear fit of the CNT total resistance, R_T, versus CNT length, L_{CNT}, behavior is used with the assumption that each CNT and its contacts are ohmic resistors. Because the contact resistance R_C is diameter-dependent, all measurements are performed on CNTs with similar diameters. Thus, R_C and CNT resistivity ρ can be extracted using

$$R_T = R_C + R_{CNT} = R_C + \frac{4\rho}{\pi D_{CNT}^2} L_{CNT} \, . \qquad (1)$$

R_C is simply the resistance intercept of the R_T *vs.* L_{CNT} line as shown in Fig. 3, while L_{CNT} and diameter (D_{CNT}) are determined from SEM images. The CNT resistivity is then determined from the slope of the line and using Eq. (1).

For these measurements, the nanoprober-CNT contact resistance is minimized with Joule heating from current stressing. This improves R_C by several orders of magnitude [4-6]. Despite such improvement, R_C is still the dominant factor governing CNT device performance, as apparent from Fig. 3(a) for CNTs grown on a grainy substrate. With a smooth substrate, we are able to grow CNTs with individual contact resistance below 400 Ω, as shown in Fig. 3(b). And contact resistance around 300 Ω and CNT resistivity in the 10^{-4} - 10^{-5} Ωcm range as given in Table I are now achievable.

B. High-Resolution Transmission Electron Microscopy

HRTEM images of the CNT-Ti interface reveal two significant differences in CNTs grown on the smooth Ti substrate compared with those on the grainy substrate, as

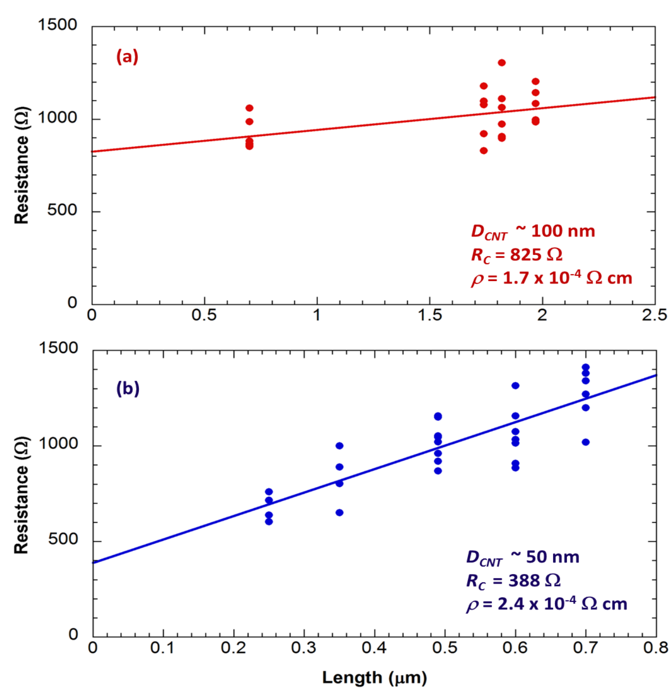

Fig. 3. Total resistance R_T versus CNT length L_{CNT} for grainy substrate (a) and smooth substrate (b). Each data point corresponds to an individual CNT measurement.

TABLE I. PROJECTIONS OF 30 nm-CNT VIA RESISTANCE BASED ON PRESENT RESULTS FROM US AND OTHERS [10], AND COMPARED WITH THAT OF CU. CALCULATED RESULTS ARE BASED ON 120 nm-LONG VIA AND CNT DENSITY OF 4.4 X 10^{11} cm^{-2}.

Via	R_C	ρ (Ω cm)	D_{CNT} (nm)	R_{CNT}	30 nm Via resistance
AIST	N/A	~ 1 x 10^{-4}	~ 4	9.55 kΩ (calc.)	190 Ω [1] (calc.)
SCU	300 Ω	~5 x 10^{-5}	15	340 Ω	160 Ω [2] (projected)
Cu	~15 Ω	5 x 10^{-6}			~25 Ω

shown in Fig. 4. CNTs on the smooth substrate show parallel graphitic planes perpendicular to the metal underlayer, while those on the grainy substrate have structures resembling stacked cups. The latter structure is generally called carbon nanofiber (CNF) [7,8]. These distinct nanostructures near the metal interface appear to be dictated by the catalyst particle shape and size, and defined in the early stages of CNT growth [9]. While both structures appear to have a clean interface with Ti, the smoother substrate shows less grain boundaries and provides a more effective conduction path across the interface. Further, the HRTEM images confirm that a smooth underlayer results in more uniform CNT growth and higher density. And the multi-wall structure near the interface is clearly the primary reason for a lower contact resistance. Such findings are valuable for the eventual optimization of the CNT growth process to yield functional via interconnects.

IV. Conclusion

Using a PECVD reactor, we have grown CNTs on Ni/Ti substrates with different degrees of graininess to elucidate the growth parameters that can eventually lead to via fabrication

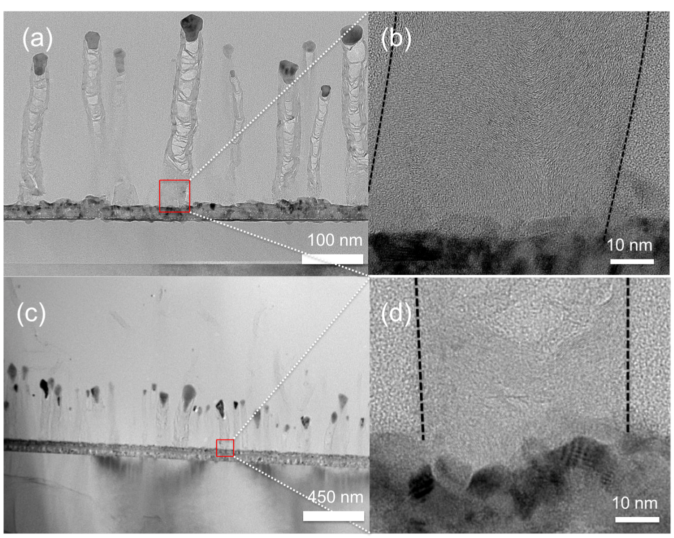

Fig. 4. (a) TEM cross-sectional image of as-grown CNTs on (a) smooth Ti substrate, and (b) HRTEM image of an individual CNT-metal interface as indicated in (a). (c) & (d) Corresponding images for a grainy Ti substrate. Both sets of interface images display a clean interface between CNT and underlayer metal.

process optimization. For a functional CNT via, maximal CNT density, minimal average CNT diameter, very low CNT-metal contact resistance, and parallel multi-wall CNT structure are needed. This study provides the basis to define the growth and fabrication tasks to achieve such targets. To quantify these targets based on our present results, simple projections of resistance for a 30 nm via are given in Table I, where comparison with Cu is also shown.

It is clear from such comparison that the key in “matching” Cu via resistance lies in minimizing the CNT-metal contact resistance and to a lesser extent, maximizing the CNT density. Efforts on CNT growth and device fabrication are underway to achieve densities $>10^{11}$ cm^{-2}, while further improving the CNT-metal interface.

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