Using Modified Bessel Functions For Analysis of Nonlinear Effects In a MOS Transistor Operating in Moderate Inversion

I.M. Filanovsky, L.B. Oliveira, and N.T. Tchamov

***Abstract*—The paper describes analysis of nonlinear effects in a MOS transistor operating in moderate inversion and saturation. The dependence of the drain current on the gate-source and drain-source voltages is described using a modified version of the "reconciliation" model developed by Y. Tsividis. In the new model the current components, which correspond to the terms depending exponentially on normalized gate-source or drain-source modulating sinusoidal voltages, are presented using modified Bessel functions. This approach allows one to find the first, second and third harmonics of the drain current caused by the gate-source or drain-source voltage sinusoidal modulation, and find also the intermodulation terms produced by these two modulating voltages. The results are applied to set the requirements to the gate-source and drain-source bias voltages in design of low-distortion and/or low-voltage amplifiers. It is shown that the realization of the stage with the zero value of third order harmonic requires extremely tight tolerances for the threshold voltage. The suppression of intermodulation terms requires increased drain-source voltage. These recommendations are confirmed by simulations.**

***Index Terms*—MOS transistor model, moderate inversion, saturation, drain current harmonics, low-distortion/ low-voltage amplifier.**

I. Introduction

As anticipated over 30 years ago [1], MOS transistor moderate inversion is an increasingly important region for modern analog circuit design. It provides the best compromise in terms of consumption and speed, especially in low power and low voltage applications.

A very powerful method of analysis and design of linear analog integrated circuits with transistors operating in moderate inversion was described in [2]. This work initiated the analysis of many aspects [3-9]: voltage gain, thermal noise, and settling time of low power/low voltage amplifiers. Yet, in this development, due to the exponential dependence of the drain current on the gate-source voltage, the weak and moderate inversion regions were generally dismissed for low-distortion applications [10] even though some properties of MOS transistors seemingly useful for design of low-distortion amplifiers were found in the course of years.

It was discovered in measurements [11] that when the gate-source voltage is modulated by a sinusoidal signal, the third harmonic of the drain current depending on bias may have two zero values. Other simulations and measurements [12] on the modern sub-micron devices suitable for RF applications indicated a significant peaking, or "sweet spot", in the third-order intercept point, IP3, for the moderate inversion region. This gave a hope [12] that "a significant increase in linearity with low power consumption is possible". Finally, the simulation of the drain current in a low-distortion amplifier [13] indicated that this "sweet" point may exist for IP2 as well.

Yet, these results cannot be directly applied to design of low-distortion amplifiers. The model which allows one to connect the transistor bias and the regions of operation with calculation of harmonic distortions was absent. The g_m / I_D characteristic so successfully used in design of linear circuits [14, 15] is not fully adapted for analysis of nonlinear distortions [16-18], because of the limitations occurring when Taylor series' are used for nonlinear circuit design (a good example is dependence of the 'sweet spot" on the signal strength overlooked in [12]). The Bessel functions used in this paper help to see better the effects when large amplitude sinusoidal signals are applied.

The first step in this direction was done in [19] where the authors tried to use the so-called 'reconciliation' model [20] for this purpose. But this approach, besides of being indirect (via the transconductance derivatives), was still used for evaluation of distortions in small-signal operation. Yet, many features of nonlinear behavior in this case are lost, for example, the dependence of performance on the signal strength when the signal may change the bias voltage.

The goal of this paper is to introduce further modifications of 'reconciliation' model which result in using exponential and algebraic terms only. In this case, one can use the modified Bessel functions for calculation of harmonics. The analysis of third and second harmonic suppression follows. Using full modified "reconciliation" model allows one to calculate the intermodulation harmonics, and this is important for design of low-voltage amplifiers. The approach becomes suitable for analysis of wide range of nonlinear effects (some are included).

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In Section II we are giving a review of this new model and describing its further development for moderate inversion and strong saturation. We also give a clear distinction between the proposed model and the model used in g_m / I_D approach. Section III describes the basic properties of modified Bessel functions required for calculations of harmonics. Section IV describes the harmonics due to the gate-source or drain-source modulations and the intermodulation harmonics occurring when both voltages are modulated and provides the formulas for harmonics calculation. Section V provides an example of harmonics calculations for common-source stage and establishes how the achievable reduction of the third or second harmonic is connected with tolerances of the transistor threshold voltage and gives recommendations on the choice of gate-source bias voltage. Section VI describes the influence of the drain modulation on the choice of the drain-source voltage. Section VII gives the application of the harmonics calculation to calculation of 1-dB compression point and shows how using Bessel functions clarifies two-tone test. Section VIII discusses the results and provides some conclusions.

II. New Transistor Model

In the "reconciliation" model [20], the drain current I_D of an n-channel transistor without body effect is described by the following equation

$$I_D = I_Z \left[\ln^2\left(1+e^{\frac{V_{GS}-V_{TH}}{2n\phi_t}}\right) - \ln^2\left(1+e^{\frac{V_{GS}-V_{TH}-nV_{DS}}{2n\phi_t}}\right)\right]. \quad (1)$$

where $I_Z = 2\mu C'_{ox}(W/L)n\phi_t{}^2$, $\phi_t = (kt)/q$ is the thermal voltage and V_{TH} is the threshold voltage. The substrate factor n will be approximated as [20]: $n \approx 1+[\gamma/\left(2\sqrt{V_{SB}+2\phi_F}\right)]$ where γ is the body-effect factor and ϕ_F is the Fermi voltage. In the model (1), all voltages are taken with respect to the source. The term involving only the gate-source voltage V_{GS} (inversion term) is conveniently separated from the term including both V_{GS} and the drain-source voltage V_{DS} (saturation term). The model (1) usually (for wide and long transistors) provides a good correspondence between theoretical, simulation and **experimental** results [21-22] in typical CMOS technologies.

If the saturation term can be neglected (V_{DS} is sufficiently high), the current can be approximated as

$$I_D = I_Z \ln^2\left(1+e^{\frac{V_{GS}-V_{TH}}{2n\phi_t}}\right) \quad (2)$$

From (2) one can obtain that

$$\frac{g_m}{I_D} = \frac{\sqrt{I_z / I_D}}{n\phi_t\left(e^{\sqrt{I_D/I_z}}-1\right)} \quad (3)$$

where $g_m = \partial I_D / \partial V_{GS}$. The eq. (3) is the basis for the above mentioned [2] g_m / I_D design approach (we are using in (3) slightly different current normalization).

Both (1) and (2) are not well adapted for the analysis of nonlinear distortions when V_{GS} and V_{DS} have the sinusoidal components. Two expansions of logarithmic functions into series' are convenient for further derivation. These are [23]

$$\ln^2(x) = \left[\ln(-1+x) - \sum_{k=1}^{\infty}\frac{(-1)^k(-1+x)^k}{k}\right]^2 \quad (4)$$

for $|-1+x|>1$, and

$$\ln^2(x) = \left[\sum_{k=1}^{\infty}\frac{(-1)^k(-1+x)^k}{k}\right]^2 \quad (5)$$

for $|-1+x|\le 1$. Then, using two terms of (4) with $x = 1+e^{\frac{V_{GS}-V_{TH}}{2n\phi_t}}$ and two terms of (5) with $x = 1+e^{\frac{V_{GS}-V_{TH}-nV_{DS}}{2n\phi_t}}$ (with modified coefficients α_1 and α_2 of second terms; the details can be found in [21]) one can find the modified model for the region of moderate inversion ($V_{GS} > V_{TH}$) and saturation ($|V_{GS}-V_{TH}| \le |nV_{DS}|$) as

$$I_{DMS} = I_Z\left[\left(e^{-\frac{V_{GS}-V_{TH}}{2n\phi_t}} + \frac{V_{GS}-V_{TH}}{2n\phi_t} - \alpha_1 e^{-\frac{V_{GS}-V_{TH}}{n\phi_t}}\right)^2 - e^{\frac{V_{GS}-V_{TH}-nV_{DS}}{n\phi_t}}\left(1-\alpha_2 e^{\frac{V_{GS}-V_{TH}-nV_{DS}}{2n\phi_t}}\right)^2\right] \quad (6)$$

where $\alpha_1 = (1-\ln 2)$ and $\alpha_2 = 1-(\ln 2)^2$. The subscripts in I_{DMS} mean the **D**rain current for **M**oderate inversion and **S**aturation (we suggest that the condition (2) is called **"**Deep saturation").

Here the model (6) is even further simplified. The terms with α_1 and α_2 are omitted, and the model is reduced to

$$I_{DMS} = I_Z\left[\left(e^{-\frac{V_{GS}-V_{TH}}{2n\phi_t}} + \frac{V_{GS}-V_{TH}}{2n\phi_t}\right)^2 - e^{\frac{V_{GS}-V_{TH}-nV_{DS}}{n\phi_t}}\right] \quad (7)$$

The omitted terms provide a continuous and smoother connection between the adjacent regions of operation (weak, moderate and strong inversion, different degrees of saturation). They do not change the techniques of harmonic calculations (the removed terms are also exponential); but the results with inclusion of these terms will be more cumbersome and does not improve comparison with simulations.

The first two terms of (7) (with their sum squared) describe the transition from moderate to strong inversion [21]. The third term is calculated for $|V_{GS}-V_{TH}| < |nV_{DS}|$ for the operation in (say, strong) saturation. This term may be used to calculate

the transistor output impedance

$$g_{out} = \frac{\partial}{\partial V_{DS}} \left(-I_Z e^{\frac{V_{GS} - V_{TH} - nV_{DS}}{n\phi_t}} \right) = \frac{I_Z}{\phi_t} e^{\frac{V_{GS} - V_{TH} - nV_{DS}}{n\phi_t}} \quad (8)$$

One can develop the expression for g_{out} / I_D which can be used in calculation of nonlinearities as well. This topic is outside the scope of this paper.

The velocity saturation is neglected in both models (1) and (7) and can be considered in the same way as it was considered in [20] for model (1), i.e. by inclusion of a channel-length modulation multiplier.

Here (7) is used for calculation of harmonics in the common-source (CS) stage (Fig. 1), and the voltages V_{GS} and V_{DS} may have sinusoidal components $v_{gs} = V_{gm} \cos \omega t$ and $v_{ds} = V_{dm} \cos \Omega t$.

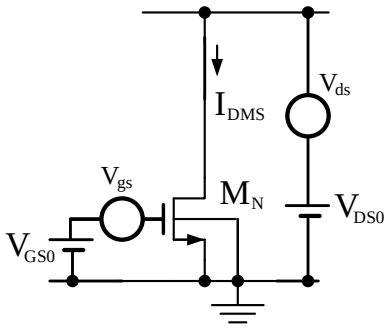


Fig. 1 Common-source stage with gate and drain modulation

III. Modified Bessel functions

The calculation of harmonics using modified Bessel functions is based on the following [24] mathematical identities:

$$e^{x \cos \omega t} = I_0(x) + 2 \sum_{n=1}^{\infty} I_n(x) \cos n\omega t \quad (9)$$

and

$$e^{-x \cos \omega t} = I_0(x) + 2 \sum_{n=1}^{\infty} (-1)^n I_n(x) \cos n\omega t \quad (10)$$

Here $I_0(x), I_1(x), \ldots, I_n(x)$ are modified Bessel functions of the first kind [24, 25, and 26]. In MATLAB routine they are available using script `besseli(n,x)`; otherwise they can be calculated using the following series [24]

$$I_n(x) = \frac{(x/2)^n}{\Gamma(n+1)} + \frac{(x/2)^{n+2}}{1!\Gamma(n+2)} + \frac{(x/2)^{n+4}}{2!\Gamma(n+3)} + \ldots \quad (11)$$

where $\Gamma(k) = (k-1)!$ is gamma-function for positive numbers.

The approximate expressions for the values of $x < 1$ are

$$I_0(x) \approx 1 + \frac{x^2}{4}, I_1(x) \approx \frac{x}{2} + \frac{x^3}{16}, I_2(x) \approx \frac{x^2}{8}, I_3(x) \approx \frac{x^3}{48} \quad (12)$$

(in general, $I_n(x) \approx \frac{(x/2)^n}{n!}$ (for $n \geq 1$)). The approximations (12) are sufficient to avoid the assumptions of signal smallness in the considered electronics problem. An extensive table of these functions can be found in [24]. The relative values of higher order functions for the same value of x are quickly decreasing with respect to $I_0(x)$ when the order n is increasing (a useful property to remember for evaluation of the dominant intermodulation harmonic).

IV. Calculation of Drain Current Harmonics

Let the gate-source voltage include a sinusoidal component, i.e. $V_{GS} = V_{GS0} + V_{gm} \cos \omega t$. Then one can introduce the normalized variables of $X = \frac{V_{GS0} - V_{TH}}{2n\phi_t}$ and $x = \frac{V_{gm}}{2n\phi_t}$. In a similar fashion, if the drain-source voltage also includes a sinusoidal component, i.e. $V_{DS} = V_{DS0} + V_{dm} \cos \Omega t$, one can introduce the normalized variables of $Y = \frac{V_{GS0} - V_{TH} - nV_{DS0}}{n\phi_t}$ and $y = \frac{V_{dm}}{\phi_t}$. Then, using these normalized variables one can rewrite (5) as

$$I_{DMS} = I_Z \left\{ \left[X + x\cos\omega t + e^{-(X + x\cos\omega t)} \right]^2 - e^{(Y + 2x\cos\omega t - y\cos\Omega t)} \right\} \quad (13)$$

Using the approximations

$$e^{-x\cos\omega t} \approx I_0(x) - 2I_1(x)\cos\omega t + 2I_2(x)\cos 2\omega t - 2I_3(x)\cos 3\omega t, \quad (14)$$

$$e^{-2x\cos\omega t} \approx I_0(2x) - 2I_1(2x)\cos\omega t + 2I_2(2x)\cos 2\omega t - 2I_3(2x)\cos 3\omega t, \quad (15)$$

and

$$e^{-y\cos\Omega t} \approx I_0(y) - 2I_1(y)\cos\Omega t + 2I_2(y)\cos 2\Omega t - 2I_3(y)\cos 3\Omega t \quad (16)$$

one finds that

$$I_{DMS} = I_{DMS,G} + I_{DMS,D} \quad (17)$$

Here the term

$$I_{DMS,G} = I_Z \left\{ \begin{array}{l} X^2 + 2Xx\cos\omega t + x^2\cos^2\omega t \\ + 2(X + x\cos\omega t)e^{-X}[I_0(x) - 2I_1(x)\cos\omega t \\ + 2I_2(x)\cos 2\omega t - 2I_3(x)\cos 3\omega t] \\ + e^{-2X}[I_0(2x) - 2I_1(2x)\cos\omega t \\ + 2I_2(2x)\cos 2\omega t - 2I_3(2x)\cos 3\omega t] \end{array} \right\} \quad (18)$$

defines the harmonics of current caused by modulation of the gate-source voltage only, and which do not depend on the saturation term, and

$$I_{DMS,D} = I_Z \left\{ \begin{array}{l} -e^Y \left[\begin{array}{l} I_0(2x) + 2I_1(2x)\cos\omega t + 2I_2(2x)\cos 2\omega t \\ + 2I_3(2x)\cos 3\omega t \end{array} \right] \\ \times \left[\begin{array}{l} I_0(y) - 2I_1(y)\cos\Omega t + 2I_2(y)\cos 2\Omega t \\ - 2I_3(y)\cos 3\Omega t \end{array} \right] \end{array} \right\} \quad (19)$$

defines the harmonics which appear when the drain-source

modulation is added. Continuing calculations one arrives to the following four groups of harmonics

$$\begin{aligned} I_{DMS} &= I_Z\left(A_0 + A_1\cos\omega t + A_2\cos 2\omega t + A_3\cos 3\omega t\right) \\ &+ I_Z(B_0 + B_1\cos\omega t + B_2\cos 2\omega t + B_3\cos 3\omega t) \\ &+ I_Z(D_1\cos\Omega t + D_2\cos 2\Omega t + D_3\cos 3\Omega t) \\ &+ I_Z(IMH_\nu) \end{aligned} \quad (20)$$

We are using below the values of harmonics amplitudes normalized by the current I_Z. The first group of harmonics are produced by the modulation of gate-source voltage only. Their normalized values are the following

$$A_0 = X^2 + \frac{x^2}{2} + 2Xe^{-X}I_0(x) - 2xe^{-X}I_1(x) + e^{-2X}I_0(2x), \quad (21)$$

$$A_1 = 2Xx - 4Xe^{-X}I_1(x) + 2xe^{-X}[I_0(x) + I_2(x)] - 2e^{-2X}I_1(2x) \quad (22)$$

$$A_2 = \frac{x^2}{2} + 4Xe^{-X}I_2(x) - 2xe^{-X}[I_1(x) + I_3(x)] + 2e^{-2X}I_2(2x) \quad (23)$$

$$A_3 = -4Xe^{-X}I_3(x) + 2xe^{-X}I_2(x) - 2e^{-2X}I_3(2x) \quad (24)$$

The second group has the normalized amplitudes

$$B_0 = -e^Y[I_0(2x)I_0(y)]; \quad B_1 = -e^Y[2I_1(2x)I_0(y)];$$
$$B_2 = -e^Y[2I_2(2x)I_0(y)]; \quad B_3 = -e^Y[2I_3(2x)I_0(y)]; \quad (25)$$

They appear when both gate and drain modulations are present. For the amplifiers, the value of Y is negative; the region of saturation requires that $nV_{DS0} > V_{GS0} - V_{TH}$ and increasing V_{DS0} suppresses these harmonics (see Sections V and VI below). In case of the gate-source modulation only they should be considered when V_{DS0} is small (low-voltage power supply). Then, using (25), one must put $I_0(y) = 1$.

The third group of harmonics appears also when the both the gain-source and drain-source modulations are present. The normalized harmonics amplitudes in this case are

$$D_1 = e^Y[2I_1(y)I_0(2x)];$$
$$D_2 = -e^Y[2I_2(y)I_0(2x)]; \quad D_3 = e^Y[2I_3(y)I_0(2x)]; \quad (26)$$

In case of drain-source modulation only one has to put $I_0(2x) = 1$ in calculations using (26). These components are also important in case of small values of V_{DS0}, and are suppressed increasing V_{DS} voltage (see Sections V and VI below again).

Finally, the last group, the normalized intermodulation harmonics IMH_ν, are obtained from the expression

$$IMH_\nu = \begin{Bmatrix} -e^Y[2I_1(2x)\cos\omega t + 2I_2(2x)\cos 2\omega t \\ +2I_3(2x)\cos 3\omega t][-2I_1(y)\cos\Omega t \\ +2I_2(y)\cos 2\Omega t - 2I_3(y)\cos 3\Omega t] \end{Bmatrix} \quad (27)$$

Using the tables in [24] or graphs in [26] one can find that the function $I_1(x)$ increases faster than $I_2(x)$ or $I_3(x)$ (see also remarks under eq. (12)). Hence, the intermodulation harmonics obtained from multiplication of the first terms in the square brackets of (27)

$$IMH_{\Omega-\omega} = 2e^Y I_1(2x)I_1(y)\cos(\Omega - \omega)t \quad (28)$$

and

$$IMH_{\Omega+\omega} = 2e^Y I_1(2x)I_1(y)\cos(\Omega + \omega)t \quad (29)$$

have usually the largest amplitudes.

Table I. Intermodulation Harmonic Coefficients

	$\cos\omega t$	$\cos 2\omega t$	$\cos 3\omega t$
$\cos\Omega t$	$2I_1(2x)I_1(y)$	$2I_2(2x)I_1(y)$	$2I_3(2x)I_1(y)$
$\cos 2\Omega t$	$2I_1(2x)I_2(y)$	$2I_2(2x)I_2(y)$	$2I_3(2x)I_2(y)$
$\cos 3\Omega t$	$2I_1(2x)I_2(y)$	$2I_2(2x)I_3(y)$	$2I_3(2x)I_3(y)$

All other intermodulation harmonics can be obtained from (27) using the formulas of elementary trigonometry. It is convenient to use Table I; the multiplier e^Y and the signs of the terms in the table are omitted. Yet, this multiplier indicates us that these harmonics can also be suppressed increasing the V_{DS} voltage (see Section VI again).

V. Third and Second Harmonics and CS Stage Bias

In this part we consider calculations of harmonics for the transistor designed for 65 nm technology. The basic parameters of this technology are the following: V_{TH} = 0.24 V, $\mu C_{ox} = 983$ μA/V^2 (extrapolated from the data in [22]), the substrate factor n = 1.3, and the thermal voltage $\phi_t = 25.9$ mV. The simulations are done for the device with the aspect ratio W/L = 50μm/0.36μm. This gives the normalizing current of $I_Z = 238$ μA. The simulation dependencies considered in this part are obtained using the drain-source $V_{DS} = 1$ V (nominal voltage for this technology).

Assume that there is no drain modulation. The design of a low-distortion amplifier with low-power dissipation is, first of all, connected with searching the optimal bias point located in the region of moderate inversion and minimizing the third harmonic. Let us see how the third harmonic of current is varying when the bias voltage V_{GS0} is changing. The eq. (7), with omitted saturation term, is describing the transition from moderate (exponential term in the first bracket of (7) is dominating) to strong inversion (the algebraic term is dominating). The border, V_{GST}, between these two regions can be found from the equation

$$e^{-X} = X \quad (30)$$

The solution of (30) is $X = 0.567$ which gives $V_{GST} = 0.278$ V $\approx$ 0.3 V. Hence, below this voltage the transistor operates definitely in moderate inversion.

Let us return to Eq. (24) and rewrite it as ·

$$A_3 = 2e^{-X}[-2XI_3(x) + xI_2(x) - e^{-X} I_3(2x)] \quad (31)$$

Calculating $|A_3|$ as a function of the bias voltage V_{GS} (Fig. 2) for the above mentioned process parameters one observes that there are, indeed, two bias points where this harmonic becomes equal to zero. To find these points one has to solve the nonlinear equation

$$-2XI_3(x) + xI_2(x) - e^{-X} I_3(2x) = 0 \quad (32)$$

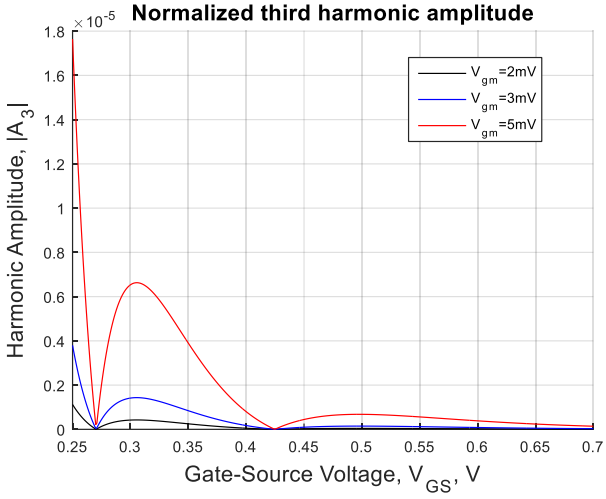


Fig. 2 Calculation of normalized third harmonic

The left side of (32) is a function of both X (i.e. bias) and x (i.e. signal amplitude). Yet, one can separate these variables using approximations (12). Substituting them into (32) one finds that

$$A_3 = \frac{x^3 e^{-X}}{12}(-X + 3 - 4e^{-X}) = x^3 F_3(X) \quad (33)$$

where $F_3(X) = [e^{-X}(-X + 3 - 4e^{-X})]/12$ can be called the third harmonic distortion factor. Hence, if one chooses the bias voltage at the points defined by the equation

$$-X + 3 - 4e^{-X} = 0 \quad (34)$$

the third harmonic amplitude becomes zero. The solutions of (34) are $X_1 = 0.451$ (corresponding to $V_{GS1} = 0.270$ V) and $X_2 = 2.742$ (corresponding to $V_{GS2} = 0.425$ V).

The first point is definitely located in the region of moderate inversion. To estimate the suitability of this point for biasing of a low-distortion amplifier, let us remark that using the bias voltage of $V_{GS0} = 0.270$ V for moderate inversion means that this voltage is always larger than the threshold voltage V_{TH}. This requires an unrealistically tight tolerance of 10% for V_{TH}. Fig. 3 shows how the value of $|F_3|$ changes when, with a given bias voltage, V_{TH} varies within chosen tolerance. Then, for the tolerance of 10%, $0.216\text{ V} < V_{TH} < 0.268\text{ V}$ and, indeed, for the case of $V_{TH} = 0.24$ V and $V_{GS0} = 0.270$ V (Fig. 3, black line) the amplitude $|F_3|$ is equal to zero. But if V_{TH} is close to 0.268 V the amplitude of $|F_3(X)|$ is quickly increases (read:

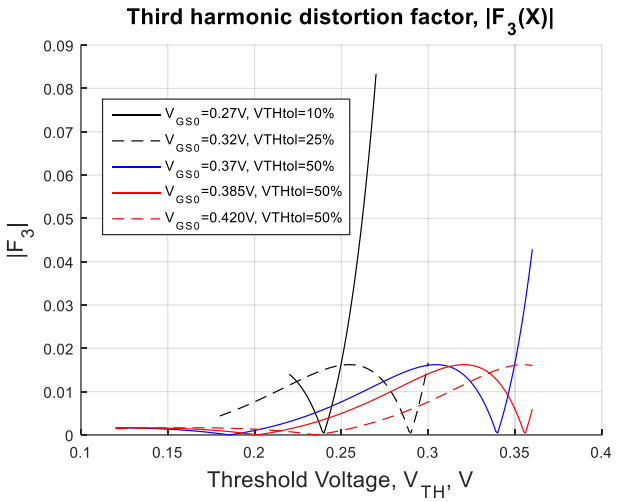


Fig. 3 Bias voltage and threshold voltage tolerances

the third harmonic distortion increases tremendously).

Similar observations should be done for other choices of the bias voltage. Using $V_{GS0} = 0.320$ V requires 25% tolerance for V_{TH}. Then $0.18\text{ V} < V_{TH} < 0.30\text{ V}$, and if V_{TH} satisfies this condition, the maximal value of $|F_3|_{\max} = 0.0162$ located between X_1 and X_2. If the tolerance even wider (say, 50%, which is very realistic), i.e. $0.12\text{ V} < V_{TH} < 0.36\text{ V}$, then, using $V_{GS0} = 0.37$ V may give the increased values of $|F_3| > |F_3|_{\max}$ for transistors with high values of V_{TH} (Fig. 3, blue line). Increasing the bias voltage one can finally find the bias voltage $V_{GS0} = 0.385$ V (Fig. 3, red line) which provides the value of $|F_3|$ which is not exceeding the value of $|F_3|_{\max} = 0.0162$ for the whole possible range of V_{TH} voltage.

Hence, Fig. 3 is the most important plot for the low-distortion one-transistor amplifier design. One concludes that using the first zero solution of (34) is practically impossible; it is better to rely on the value of the distortion factor $|F_3|_{\max} = 0.0162$. Further increasing the bias voltage decreases $|F_3|$ (see the result for $V_{GS0} = 0.425$ V). But now the transistor dissipates more power, and the result is not so spectacular: the curve of $|F_3|$ around maximum is rather flat.

Now consider the contribution B_3 to the third harmonic (see (25)). If the drain voltage modulation is absent, one has to use $I_0(y) = 1$ in calculation of this component. Then, using the approximation for $I_3(2x)$ from (12) one obtains

$$B_3 = -e^{Y}(x^3/3) \quad (35)$$

If it is desirable to suppress B_3 with respect to A_3 one can introduce and specify the suppression coefficient

$$S_{3dg} = |B_3|/|A_3| \quad (36)$$

Then, from (33) and (35) one finds that the required drain-source bias, V_{DS0}, can be obtained from the equation

$$e^{Y} = 3\,|F_3|_{\max}\, S_{3dg} \tag{37}$$

We remind that $Y = (V_{GS0} - V_{TH} - nV_{DS0})/(n\phi_t)$, then, to be on a safe side, one has to use the lowest value of V_{TH} in the calculations of

$$Y = \frac{V_{GS0} - V_{TH} - nV_{DS0}}{n\phi_t} = \ln(3F_{3\max}S_{3dg}) \tag{38}$$

For example, for the considered case with $V_{GS0} = 0.385$ V one must use $V_{TH} = V_{TH\,\min} = 0.120$ V (minimal value of the threshold voltage in case of 50% tolerance). Then, to obtain $S_{3dg} = 0.01$ one finds that the required drain-source bias voltage V_{DS0} = 0.257 V. This voltage is higher than (0.385-0.260) V=0.125 V which would be required to keep the transistor in saturation for the nominal value of the threshold voltage.

The evaluation of the second harmonic can be done in the same order which we used for the third harmonics. The eq. (23) can be rewritten as

$$A_2 = \frac{x^2}{2} + 2e^{-X}\{2XI_2(x) - x[I_1(x) + I_3(x)] + e^{-X}I_2(2x)\} \tag{39}$$

Fig. 4 shows the dependencies of A_2 from V_{GS0}, the bias voltage, and for the same signal amplitudes as in Fig. 3. Then, indeed, one can find the bias voltage for which the value of A_2 is minimal.

Using (12) one finds that eq. (39) can be reduced to

$$A_2 = \frac{x^2}{2}\left[1 + e^{-X}\left(X - 2 - \frac{x^2}{12} + 2e^{-X}\right)\right] = x^2F_2(x, X) \tag{40}$$

The multiplier $F_2(x, X)$ practically does not change for the signal amplitudes shown in Fig. 4, i.e. one can write that

$$F_2(x, X) \approx F_2(X) = \frac{1}{2}\left\{1 + e^{-X}\left[X - 2(1 - e^{-X})\right]\right\} \tag{41}$$

The function $F_2(X)$ has the minimum of $F_{2\min}(X) = 0.412$ located at $X = 0.450$ corresponding to $V_{GS0} = 0.270$ V, and

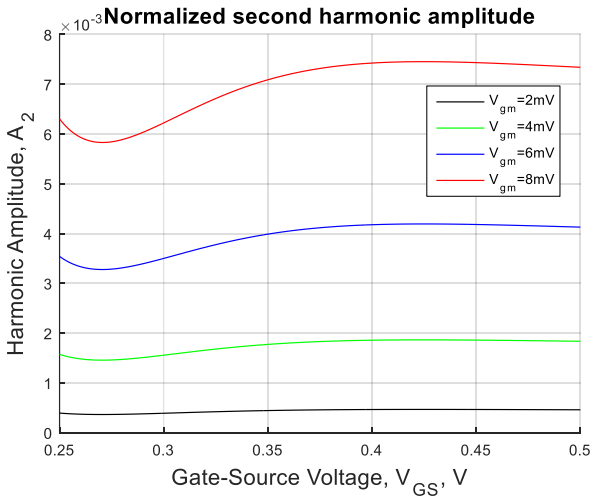


Fig. 4 Normalized second harmonic as the function of bias voltage

the flat maximum of $F_{2\max}(X) = 0.528$ which is located at $X = 2.670$ corresponding to $V_{GS0} = 0.420$ V.

Usually, the main goal is minimization of the third harmonic amplitude $|A_3|$ (with simultaneous minimization of power dissipation). But if it is required to evaluate a possible minimization of A_2 one has to connect it with the V_{TH} tolerances, as it was done previously.

Fig. 5 shows that the minimal value of $F_{2\min}(X) = 0.412$ can be realized for a very narrow range of V_{TH} tolerances (even less than 10%); yet, the result will be only about 20% better than for the case of 50% tolerance. The only satisfying conclusion is that $F_{2\max}(X) = 0.528$ practically does not depend on bias in the range important for minimization of $|A_3|$.

The contribution B_2 to the second harmonic is given in (25). In the absence of the drain voltage modulation one has to use $I_0(y) = 1$ in calculation of B_2. Then, using (12) for $I_2(2x)$ one obtains

$$B_2 = -x^2e^{Y} \tag{42}$$

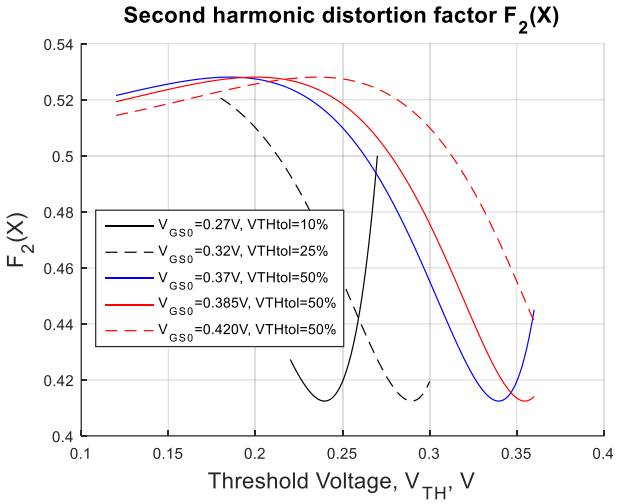


Fig. 5 Bias voltage and threshold voltage tolerances

To quantify the suppression of this contribution, one can introduce and specify the suppression coefficient

$$S_{2dg} = |B_2|/|A_2| \tag{43}$$

If the choice of V_{GS0} is defined by conditions of design for the third harmonic, then one can consider that $A_2 \approx x^2F_{2\max}$ and calculate

$$S_{2dg} = e^{-Y}/F_{2\max} \tag{44}$$

Using (44) and the definition of $Y = (V_{GS0} - V_{TH} - nV_{DS0})/(n\phi_t)$ one can find the required drain-source bias voltage, V_{DS0}, from the equation

$$\frac{V_{GS0} - V_{TH} - nV_{DS0}}{n\phi_t} = \ln(S_{2dg}F_{2\max}) \tag{45}$$

To be on a safe side one must use $V_{TH} = V_{TH\,\min} = 0.120$ V again in this calculation.

As follows from the above given analysis the choice of gate-source voltage for a low-distortion stage operation can be summarized the following way.

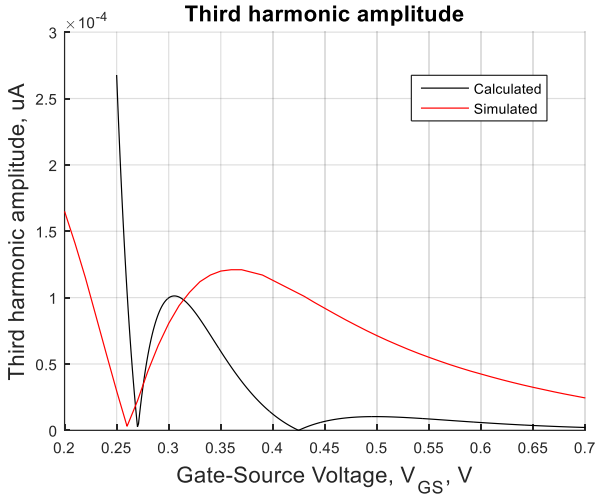


Fig. 6 Dependence of the third harmonic on bias voltage, V_{gm}=2 mV

The designer should assume that the first "sweet" point for the third and the "sweet" point for second harmonics require too tight tolerance for V_{TH}. From the other side, the bias voltage located between the "sweet" points of the characteristics shown in Fig. 2 and corresponding to the maximum value of $|F_3(X)|_{\max}$ may provide a reasonable bias voltage at the condition that the corresponding level of the third harmonic and power dissipation are acceptable.

The most important parameter for the design is the threshold voltage: its nominal value V_{TH}, and its tolerance, i.e. the maximum, $V_{TH\,\max}$, and minimum, $V_{TH\,\min}$, values (these two figures are usually difficult to provide). Then, using the nominal value of V_{TH} one has to find the value of X corresponding to

$$F_3(X) = [e^{-X}(-X + 3 - 4e^{-X})] = 0.0162 \qquad (46)$$

The solution of this equation is $X = 0.971$, and the bias voltage corresponding to this normalized value is $V_{GS} \approx 0.31$ V (all calculations are done for $V_{TH} = 0.24$ V, $n = 1.3$, and $\phi_t = 25.9$ mV). At this stage it is reasonable to simulate the stage using the device with the dimensions satisfying the condition of Y. Tsividis' model (avoiding short and narrow channel effects) and carrying the current which will be used in the application.

An example of such characteristic is shown in Fig. 6. The denormalized value of calculated current is obtained using the normalized values of Fig. 2 and multiplying them by 238 μA, the simulated values are obtained measuring the voltage drop at 1 Ω resistor inserted in the drain circuit. Both the calculated and simulated characteristics are presented for $V_{gs} = 2$ mV. One can see that the simulated "sweet" point is sufficiently close to the calculated one. The point of the maximum is located at $V_{GS} \approx 0.36$ V which is also sufficiently close to the just calculated $V_{GS} = 0.31$ V. The second "sweet" point is not pronounced (it exists, but is located at much higher gate-source voltages), yet this is not so important. We know that we have to take the gate-source voltage around $V_{GS} \approx 0.35$ V and after that the only way to reduce the third harmonic is to increase V_{GS} moving towards the second "sweet" point. A better choice would be 0.42 V or larger value (with higher power dissipation).

The tolerances for V_{TH} are usually not known. Yet, it is well known that V_{TH} depends on the channel length. One way to evaluate the influence of V_{TH} variation is to shorten simultaneously the width and the length of transistor. This does not change the parameter I_Z, so the calculated characteristic will be the same. But the simulated characteristics can change drastically. Fig. 7 shows the result when the width and length both are shortened by two times. The location of the first "sweet" point is about 0.31 V now. And the maximal value is moved to 0.42 V. Hence, this simulation confirms once more that to rely on biasing in the "sweet" point is not advisable.

Then, using the chosen bias (in our case 0.42 V) one must verify that this point is tolerant with respect to the variation of the drain voltage, temperature and process variations (corners).

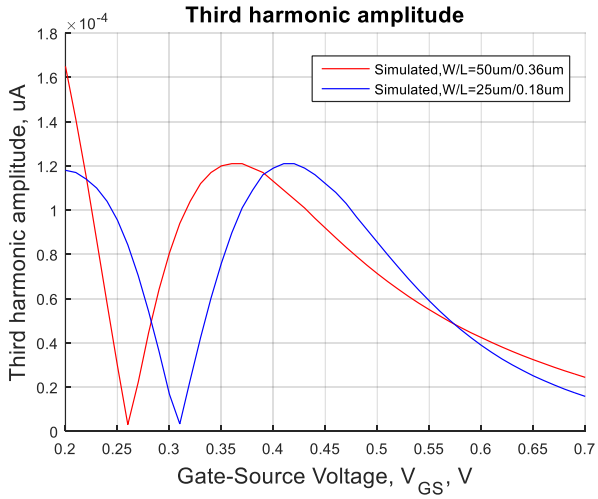


Fig. 7 Dependence of the third harmonic on transistor length, V_{gm}=2 mV

Then, if the requirements to the suppression of the harmonics components connected with the variation of the saturation part of the model are given, one has to correct (read: to increase) the drain-source bias voltage.

This, in general, finishes the recommendations on the common-source stage design.

VI. Intermodulation

The simulation dependencies considered in this section are obtained for non-standard V_{DS} voltages (below 1 V). The increase of this voltage mentioned before was a mean to suppress the variation of the saturation part of the model.

The presence of drain modulation, as shown in Fig. 1, changes the calculation of these components the following way. Using the approximations (12), with $y \neq 0$ and this modulation signal which is comparable in amplitude with the input signal x

one obtains that

$$|B_2| \approx e^Y x^2; \quad |D_2| \approx e^Y (y^2/4) \tag{47}$$

so that the total value of this second harmonic component becomes

$$|B_2| + |D_2| = e^Y \left[x^2 + \frac{y^2}{4} \right] \approx e^Y x^2 \left(1 + \frac{K_{dg}{}^2}{4} \right) \tag{48}$$

Here $K_{dg} = |y|/|x|$. In a similar way one obtains that

$$|B_3| \approx e^Y (x^3/3); \quad |D_3| \approx e^Y (y^3/24) \tag{49}$$

The total value of this third harmonic component becomes

$$|B_3| + |D_3| = e^Y \left[\frac{x^3}{3} + \frac{y^3}{24} \right] \approx e^Y \frac{x^3}{3} \left(1 + \frac{K_{dg}{}^3}{8} \right) \tag{50}$$

One can see that the presence of drain modulation, in case of high level of modulating signal can be also taken care of by increasing the suppression coefficients S_{2dg} and S_{3dg}, i.e. increasing the drain-source voltage.

Table II Values of intermodulation coefficients

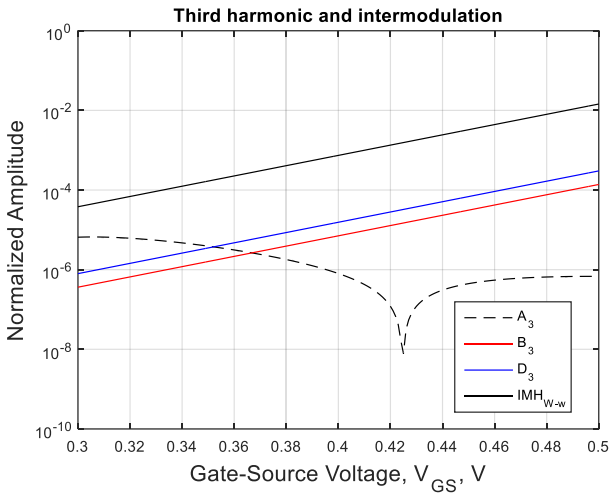
	$\cos\omega t$	$\cos 2\omega t$	$\cos 3\omega t$
$\cos\Omega t$	xy	$(x^2y)/2$	$(x^3y)/12$
$\cos 2\Omega t$	$(xy^2)/4$	$(x^2y^2)/8$	$(x^3y^2)/24$
$\cos 3\Omega t$	$(xy^3)/24$	$(x^2y^3)/48$	$(x^3y^3)/144$

The suppression of intermodulation harmonics is achieved in the similar way. Table II gives the values of the intermodulation coefficients when the approximations (12) are used for the entries in Table I. Recurring to these approximations allows one to evaluate the dominant intermodulation term very quickly: for the same level of the input signal and drain modulation it will be the upper left corner. If the requirement to the suppression are formulated (say, with respect (to the level of gate-source modulation) one can define the required drain-source voltage increase using the same type of calculation as was used for the drain modulation suppression.

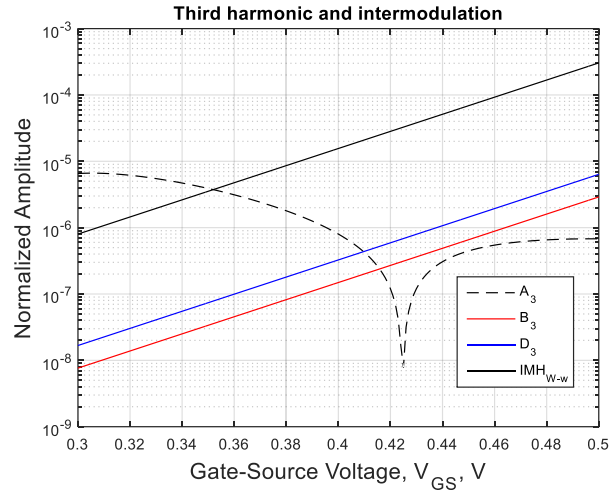
The harmonic A_3, in accordance with eq. (25) does not depend on V_{DS} voltage; but the harmonics B_3 and D_3, and, especially, all intermodulation harmonics strongly depend on this voltage. To demonstrate this dependence, Fig. 8 compares $IMH_{\Omega-\omega}$ (black line), B_3 (red line), D_3 (blue line), and A_3 (dashed line). All are normalized values obtained for $V_{gm} = V_{dm} = 5$ mV.

Let us consider the range $0.32\ \text{V} < V_{GS} < 0.40\ \text{V}$ which is preferable for low distortion amplifier.

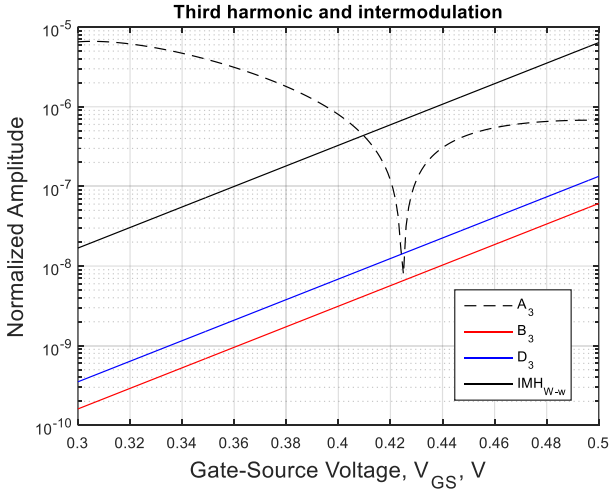
Fig. 8 a) is calculated for $V_{DS} = 0.2$ V. For this drain voltage, with $V_{TH} = 0.24$ V and $n = 1.3$, transistor will work in saturation. But for these voltages, the intermodulation distortion is strongly dominating (it may have the amplitude which is one



(a)



(b)



(c)

Fig. 8 Comparison of intermodulation amplitude with third harmonic and its components: a) V_{DS}=0.2 V, b) V_{DS}=0.3 V, c) V_{DS}=0.4 V

order of magnitude higher than that of $|A_3|$), and even components B_3 and D_3 have the amplitudes which may be higher than that of A_3. This means that, even in the absence of

the drain-source modulation, they may define the choice of V_{DS} voltage. To reduce the level of the intermodulation harmonic to that of A_3 one must increase the drain-source to $V_{DS} = 0.3$ V (Fig. 8 b)). And only when the drain-source voltage is increased to $V_{DS} = 0.4$ V (Fig. 8 c)) the intermodulation harmonic becomes lower than A_3 and one can neglect the components B_3 and D_3.

The diagrams of the Fig. 8 can also be interpreted the following way. The third harmonic components B_3 and D_3 and intermodulation current $IMH_{\Omega-\omega}$ are completely suppressed when the drain-source voltage increases further. But the third harmonic A_3 does not depend on this voltage. Let us look now at the results of simulation at one particular case of gate-source voltage.

Table III shows the result of simulation for the transistor 50um/0.36um with $V_{GS} = 0.35$ V and modulation signals $V_{gs} = 5$ mV ($f = 100$ MHz) and $V_{ds} = 5$ mV ($f = 110$ MHz). One can see that, indeed, the third harmonic, at $V_{DS} = 0$. becomes close to $I_3 = I_Z A_3 = 1.6$ nA (this figure can be verified using Fig. 6 and multiplying the value for $V_{GS} = 0.32$ V by 2.5^3=15.6), then slowly increases with the growth of the drain-source voltage. But $I_{10\text{MHz}}$ is, first, dominating I_3 below $V_{DS} = 0.3$ V and, second, arrives to its final "asymptotic" value instead of being further suppressed, when V_{DS} becomes about 0.5 V.

Table III Suppression of harmonics

V_{DS}, V	0.2	0.3	0.4	0.5	0.6	0.7
I_3, nA	3.77	1.40	1.44	1.50	1.60	1.69
$I_{10\text{MHz}}$,nA	285	96.0	90.6	88.7	87.4	86.4

This "asymptotic" value, in accordance with the used model, does not exist, and one can verify that the values for $I_{10\text{MHz}}$ shown in the Table III for V_{GS} values below 0.3 V are much higher than that calculated in accordance with the model. The proposed simplified model does not provide correct level of intermodulation distortion: it does not indicate the drain-source independent "asymptotic" value of this distortion. This limitation can be corrected using the multiplier representing the channel length modulation factor as it is proposed in [20]. This multiplier, in the analysis of harmonic distortions, will provide the term required for non-attenuated intermodulation distortion. The complexity of derivation will increase, yet this derivation will be "doable' considering the results obtained already in this paper. This could be the matter of further development.

VII. Other Applications

a) 1-dB compression point

The obtained expressions for harmonics allow to evaluate one important parameter, the so-called 1-dB compression point. The total first order harmonic of the drain current is given by

$$A_1 + B_1 = 2Xx - 4Xe^{-X} I_1(x) + 2xe^{-X}[I_0(x) + I_2(x)] \\ -2e^{-2X} I_1(2x) - e^{Y}[2I_1(2x) I_0(y)] \quad (51)$$

Consider $2X$ as a linear gain. Then, in the absence of the drain-source modulation, $I_0(y) = 1$, and the normalized bias $X > 1$. This allows one to write that

$$A_1 + B_1 \approx 2Xx - 2e^{Y} I_1(2x) = [2X - 2e^{Y}(1 + \frac{x^2}{2})]x \quad (52)$$

Then the input signal creating 1-dB compression point can be found from the expression

$$\frac{X}{X - e^{Y}(1 + x^2/2)} = 1.122 \quad (53)$$

Normally, Y is negative. But if it close to zero (low V_{DS}) , the signal x creating 1-dB compression point is decreasing.

b) Two-Tones Intermodulation Test

The two-tone intermodulation test for evaluation of nonlinearity in narrow-band amplifiers consists of introducing two sources of the same amplitude but with different and close frequencies in the input circuit and finding the terms defining the intermodulation.

Choose the stage size using (3) as in g_m / I_D design method. Then, one can return back to (2) and find the current I_D. Let $V_{GS} = V_{GS0} + V_{gm}\cos\omega_1 t + V_{gm}\cos\omega_2 t$. Doing the same normalization as in Section IV one can write

$$I_{DMS} = I_Z \left[\begin{matrix} X + x\cos\omega_1 t + x\cos\omega_2 t \\ +e^{-(X + x\cos\omega_1 t + x\cos\omega_2 t)} \end{matrix} \right]^2 \quad (54)$$

Let the bias is chosen so that (54) can be approximated as

$$I_{DMS} \approx I_Z (X + x\cos\omega_1 t + x\cos\omega_2 t)^2 \\ +2(X + x\cos\omega_1 t + x\cos\omega_2 t) e^{-(X + x\cos\omega_1 t + x\cos\omega_2 t)} \quad (55)$$

Now one can use the expansion (15) and write

$$I_{DMS} \approx I_Z (X + x\cos\omega_1 t + x\cos\omega_2 t)^2 \\ +2I_Z e^{-X} (X + x\cos\omega_1 t + x\cos\omega_2 t)[I_0(x) \\ -2I_1(x)\cos\omega_1 t + 2I_2(x)\cos 2\omega_1 t][I_0(x) \\ -2I_1(x)\cos\omega_2 t + 2I_2(x)\cos\omega_2(t)] \quad (56)$$

From this expression one can choose the terms which provide the most dangerous intermodulation components.

$$I_{DMS} \approx I_Z (X + x\cos\omega_1 t + x\cos\omega_2 t)^2 \\ +2I_Z e^{-X}[\ldots - 4XI_1(x) I_2(x)(\cos\omega_1 t\cos 2\omega_2 t \\ +\cos 2\omega_1 t\cos\omega_2 t) + \ldots + 2I_0(x) I_2(x) x(\cos\omega_1 t\cos 2\omega_2 t \\ +\cos 2\omega_1 t\cos\omega_2 t) + \ldots] \quad (57)$$

Using (12) one can rewrite (57) as

$$I_{DMS} \approx I_Z (X + x\cos\omega_1 t + x\cos\omega_2 t)^2$$
$$+2I_Z e^{-X}[... + (1-X)\frac{x^3}{4}(\cos\omega_1 t\cos 2\omega_2 t \quad (58)$$
$$+\cos 2\omega_1 t\cos\omega_2 t)]$$

Then, eq. (58) shows that one can choose the bias $X = 1$ (i.e. $V_{GS0} - V_{TH} = 2n\phi_t$), and the terms introducing intermodulation will disappear. One can analyze this bias point and find that the designer should not rely on operation in this point. It is more reliable to increase X (i.e. to move towards strong inversion) to suppress the intermodulation terms.

In addition, it was demonstrated how to connect the proposed method of nonlinearities analysis with g_m / I_D design method.

VIII. Discussion and Conclusions

The proposed method of harmonics calculation became possible after essential modification of the initial Tsividis' model. The new model (7) embraces both moderate and strong inversion. In [27] it was shown how to apply this model for static characteristics of integrated circuits. This model includes the saturation term which is important for calculation of intermodulation components and design of low-voltage amplifiers.

The new model allows one to use the modified Bessel function for calculation of the drain current harmonics. The calculations, for the DC component and the first, second, and third harmonic, are reasonably simple, and, what is more important, these calculations do not require any assumption about the smallness of the amplitude of the applied signal. The application of modified Bessel functions for calculation of harmonics is simplified when the MATLAB program is available (which is nowadays, fortunately, the case because this program is a part of nearly all design programs).

Using this approach one can calculate the dependence of the third harmonic amplitude on bias and find that, for a nominal value of the threshold voltage, there are two gate-source bias voltages where the third harmonic amplitude becomes zero. The first bias point is located at the beginning of the moderate inversion region. Yet, using this point to realize a low-distortion amplifier requires a very tight tolerance, not achievable in practice, for the threshold voltage. In addition, one can show [28] that for very large signal amplitudes, when one must use the eq. (34) and the approximations (12) are not sufficient, the first "sweet" point depends on the signal strength as well. The second "sweet' point does not require a tight tolerance for the threshold voltage and can be used for design of low distortion amplifier. Yet, this point is located in the range of strong inversion. The investigation indicates that one can operate the stage after the first "sweet" point with a reasonably constant amplitude of the third harmonic independent on the threshold voltage variations. This choice provides some reduction for the power dissipation.

The same approach indicates that there is a gate-source bias voltage where the second harmonic has a lower value in comparison with other bias points. Yet, the realization of an amplifier with reduced second-order harmonic requires again an unusually tight tolerance for the threshold voltage.

If one is not hunting for the "sweet" points, the design of low-distortion stage is simple. The bias providing operation between these "sweet" points defines the level of third harmonic distortion. As soon as this bias is accepted one can calculate the drain-source voltage required for accepted level of the drain modulation. This basically finishes the design of a CS stage operating in low power and low distortion amplifiers.

The proposed analysis can be added to g_m / I_D design approach. To do this one has to go back to the transistor model, i.e. to move back from (2) to (1) and make the corresponding model modifications. In fact, we demonstrated this doing the calculations in the second part of Section VII. The necessity to return back to transistor model was realized also in [18] but the analysis used there was still a small-signal analysis. This integration of the proposed analysis with g_m / I_D design method is considered as a matter of the future work, and the first step which we are going to do in this direction is to obtain the expression for $g_{out} = \partial I_D / \partial V_{DS}$ (using the analogy between derivation of (3) from (2) and operating with the second term in Tsividis' model.

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