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Circuit Structure and Control Method to Reduce Size and Harmonic Distortion of Interleaved Dual Buck Inverter

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Abstract: A new circuit structure and control method for a high power interleaved dual-buck inverter are proposed. The proposed inverter consists of six switches, four diodes and two inductors, uses a dual-buck structure to eliminate zero-cross distortion, and operates in an interleaved mode to reduce the current stress of switch. To reduce the total harmonic distortion at low output power, the inverter is controlled using discontinuous-current-mode control combined with continuous-current-mode control. The experimental inverter had a power-conversion efficiency of 98.5% at output power = 1300 W and 98.3% at output power = 2 kW, when the inverter was operated at an input voltage of 400 V_{DC}, output voltage of 220 V_{AC}/60 Hz, and switching frequency of 20 kHz. The total harmonic distortion was < 0.66%, which demonstrates that the inverter is suitable for high-power dc-ac power conversion.

Keywords: DC-AC power conversion; inverters; harmonic distortion; low cost

1. Introduction

The full-bridge inverter (FBI, Figure 1a) is widely used for dc-ac power conversion because of its simple structure and easy control [1]. An FBI uses sinusoidal modulation of the switching duty to produce an alternating output voltage. The FBI has a shoot-through problem [2], which occurs when the high side and low side switches (S_1 and S_4, or S_3 and S_2) are turned on at the same time; this problem can cause serious circuit damage. The shoot-through problem can be solved by inserting a dead-time between the gate pulses of the high and low side switches, but inserting a dead-time changes the effective switching duty ratio and increases zero-cross distortion (ZCD) [3]. The FBI has the other disadvantage of requiring high-rated switches and large output filters [4,5].

Various dual-buck inverters [6–15] have been proposed to remedy the disadvantages of the FBI. The dual-buck inverters use freewheeling diodes to solve the shoot-through problem but have high output current ripple. The interleaved dual-buck inverter (IDBI) in [9], as shown in Figure 1b, is basically a parallel connection of four buck converters. In this inverter, S_{U1} and S_{U2} operate to generate positive sinusoidal voltage, S_{D1} and S_{D2} operate to generate negative sinusoidal voltage, and the switching-phase differences between S_{U1} and S_{U2} and between S_{D1} and S_{D2} are set to 180°. Thus, the current of S_{U1} is interleaved with that of S_{U2}, and the current of S_{D1} is interleaved with that of S_{D2}. Using an interleaved mode reduces conduction losses, output current ripple, and current stress in switches and diodes. IDBI requires four inductors, so it is expensive and bulky. When IDBI uses typical sinusoidal pulse width control and operates at a low output power P_o, IDBI has much higher total harmonic distortion (THD) of the output current than that of the FBI.

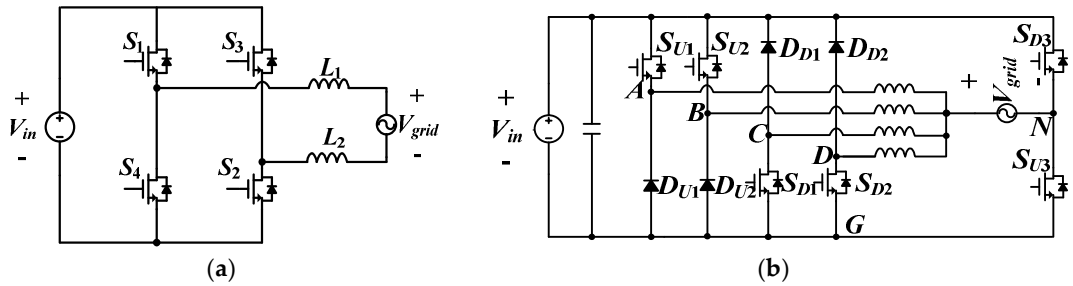

Figure 1. Circuit structure of dc-ac inverters: (**a**) full-bridge inverter (FBI) and (**b**) interleaved dual-buck inverter of [9] (IDBI [9]).

The inverter proposed in this paper (Figure 2) is a modified IDBI. This inverter inherits the IDBI's advantages but uses two reverse-current-protection diodes D_{D3} and D_{U3} to reduce the number of inductors and a new control method to reduce the THD of the output current. The proposed inverter operates in discontinuous conduction mode (DCM) [16] when the output current is below the threshold; otherwise, it operates in continuous conduction mode (CCM). The circuit structure and principle of operation are described in Section 2, experimental results and discussions are given in Section 3, and a conclusion is given in Section 4.

2. Proposed Interleaved Dual-buck Inverter

2.1. Circuit Structure and Principle of Operation

The proposed inverter (Figure 2) uses two dual-buck legs (leg 1: S_{U1}, D_{U1}; leg 2: S_{U2}, D_{U2}) to generate $V_{grid} \geq 0$ V, two dual-buck legs (leg 3: S_{D1}, D_{D1}; leg 4: S_{D2}, D_{D2}) to generate $V_{grid} < 0$ V, two blocking diodes (D_{U3}, D_{D3}) to prevent the current flowing through the body diode of switch during freewheeling mode, and two unfolding switches (S_{U3}, S_{D3}) to determine the polarity of the output current. Legs 1 and 4 are connected to L_1, and legs 2 and 3 are connected to L_2. Therefore, the proposed inverter requires two inductors, unlike interleaved dual-buck inverters, which have four legs and one inductor per leg. The proposed inverter works with the switching states and leg voltages V_{AN_on} and V_{AN_off} in Table I. Leg switches S_{U1}, S_{U2}, S_{D1}, and S_{D2} operate at a fixed switching frequency $f_s = 1/T_s$, where T_s is the switching period. The switching duty D is varied to produce a sinusoidal output voltage $V_{grid}(t) = V_g \sin(\omega t)$.

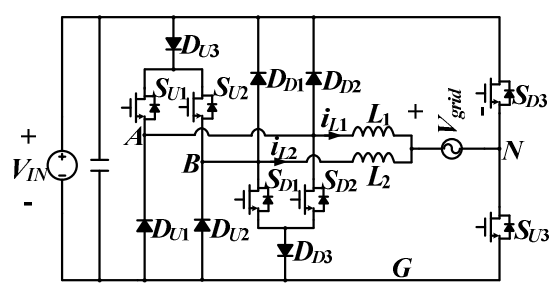

Figure 2. Circuit structure of the proposed inverter.

The simplified gate signals (Figure 3) for the proposed inverter show that legs 1 and 2 operate for $V_{grid} > 0$ V and legs 3 and 4 operate for $V_{grid} < 0$ V. S_{U3} turns for $V_{grid} \geq 0$ V and S_{D3} turns on for $V_{grid} < 0$ V. To obtain interleaved dual-buck operation, the switching phase differences between S_{U1} and S_{U2} and between S_{D1} and S_{D2} are set to $T_s/2$. The difference in switching phases reduces ZCD and prevents shoot-through without inserting dead time between switching pulses (Table 1).

Table 1. Switching states and input voltages for inductors in the proposed inverter.

V_{grid}	≥0 V	<0 V
S_{U1}	ON/OFF	OFF
S_{U2}	ON/OFF	OFF
S_{U3}	ON	OFF
S_{D1}	OFF	ON/OFF
S_{D2}	OFF	ON/OFF
S_{D3}	OFF	ON
V_{AN_on}	V_{in}	$-V_{in}$
V_{AN_off}	0	0

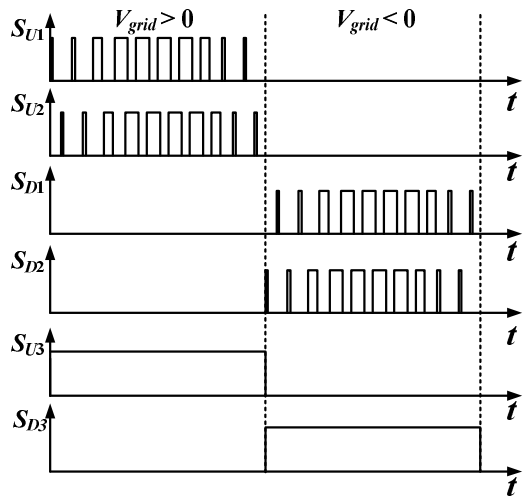

Figure 3. Simplified gate signals of the proposed inverter.

When $V_{grid} > 0$ V, the current i_{L1} and voltage V_{L1} waveforms of the inductor L_1 (Figure 4a) consist of three operating modes: Mode 1 during which the input energy is delivered to L_1 and the load; Mode 2 during which the stored energy in L_1 is delivered to the load; and Mode 3 during which the stored energy in $L_1 = 0$; Mode 3 occurs only when the inverter operates in DCM.

Mode 1 starts at $t_0 = (n-1)T_s$ by turning on S_{U1} (Figure 4b), where the integer n is a switching sequence number. During this mode, the output voltage V_{AN} of leg 1 is V_{in}. The inductor current $i_{L1}(t)$ increases as t increases, because $V_{L1} = V_{AN} - V_{grid} > 0$ V and

$$i_{L1}(t) = i_{L1}(t_0) + \frac{1}{L_1}\int_{t_0}^{t} V_{L1}(t)dt \,. \tag{1}$$

Mode 2 starts at $t_1 = (n-1+D)T_s$ by turning off S_{U1} (Figure 4c). During this mode, V_{AN} is 0 V. $i_{L1}(t)$ decreases as t increases because $V_{L1} = V_{AN} - V_{grid} < 0$ V and

$$i_{L1}(t) = i_{L1}(t_1) + \frac{1}{L_1}\int_{t_1}^{t} V_{L1}(t)dt \,. \tag{2}$$

Mode 3 starts at $t_2 = (n-1+\Delta)T_s$ where ΔT_s is duration of $i_{L1}(t) > 0$, when D_{U1} is turned off (Figure 4d). This mode is skipped when $\Delta = 1$, i.e., when the inverter is operating in CCM. During this mode, $V_{AN} = V_{grid}$ because $i_{L1}(t) = 0$ and the energy stored in L_1 is 0.

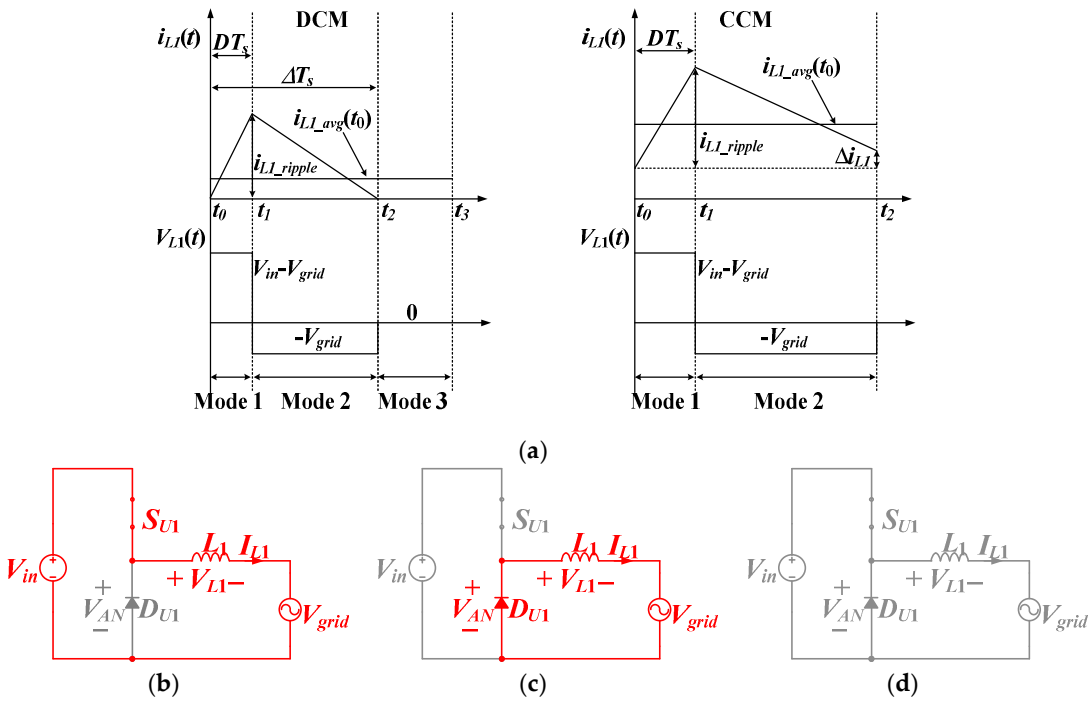

Figure 4. Theoretical waveforms and circuit diagrams for leg 1: (**a**) V_{L1} and i_{L1} for DCM and CCM operation, (**b**) circuit diagrams for Mode 1, (**c**) circuit diagrams for Mode 2, and (**d**) circuit diagrams for Mode 3.

The voltage V_{AN} of node A with respect to node N equals to $V_{grid} + V_{L1}(t)$. The switching states (Table I) produce $V_{AN} = V_{in}$ in Mode 1, $V_{AN} = 0$ V in Mode 2, and $V_{AN} = V_{grid}$ in Mode 3. The average of V_{AN} for one switching period is expressed as

$$V_{AN_avg} = V_{grid} + V_{L1_avg} = V_{grid} + L_1 \frac{di_{L1_avg}}{dt}. \tag{3}$$

S_{U1} operates with a switching duty of $D = D_{SU1}$. V_{AN_avg} can also be expressed as

$$V_{AN_avg} = V_{in} D_{SU1} + V_{grid}(1-\Delta), \tag{4}$$

because $V_{AN} = V_{in}$ in Mode 1, $V_{AN} = 0$ V in Mode 2, and $V_{AN} = V_{grid}$ in Mode 3. Solving for Δ using (3) and (4) yields

$$\Delta = \frac{V_{in} D_{SU1}}{V_{grid}} - \frac{L_1}{V_{grid}} \frac{di_{L1_avg}}{dt}. \tag{5}$$

i_{L1_avg} is calculated using Equations (1) and (2) as

$$i_{L1_avg} \approx i_{L1}(t_0) + \left(\frac{V_{in} - V_{grid}(t_0)}{2L_1} \right) D_{SU1} T_s \Delta. \tag{6}$$

To achieve a power factor of 1, the time average of output current i_{o_avg} should be $I_o \sin(\omega t)$ for $V_{grid}(t) = V_g \sin(\omega t)$. The inverter has $L_1 = L_2 = L$ and operates in interleaved dual-buck mode, so $i_{o_avg} = 2i_{L1_avg}$. When the inverter operates in DCM, D_{SU1} at $t = t_0$ to produce sinusoidal i_{o_avg} is obtained using Equations (5) and (6), $2\pi f_s >> \omega$ and $i_{L1}(t_0) = 0$ as

$$D_{SU1} = \sqrt{\frac{LI_o V_g \sin^2(\omega t)}{V_{in}\left(V_{in} - 2V_g \sin(\omega t)\right)T_s} + \left(\frac{\omega LI_o \cos(\omega t)}{4V_{in}}\right)^2} + \frac{\omega LI_o \cos(\omega t)}{4V_{in}}. \tag{7}$$

When the inverter is operating in CCM, $\Delta = 1$ and D_{SU1} at $t = t_0$ is obtained using Equation (5) as

$$D_{SU1} = \frac{V_g \sin(\omega t)}{V_{in}} + \frac{\omega LI_o \cos(\omega t)}{2V_{in}}. \tag{8}$$

The DCM interval during which the inverter operates in DCM is calculated using Equations (5), (7), and $\Delta \le 1$ as

$$0 < \omega t \le \sin^{-1}\left(\frac{V_{in}}{V_g}\left(1 - \frac{LI_o}{V_g T_s}\right)\right) \tag{9}$$

when V_{grid} increases, and

$$\pi - \sin^{-1}\left(\frac{V_{in}}{V_g}\left(1 - \frac{LI_o}{V_g T_s}\right)\right) \le \omega t < \pi, \tag{10}$$

when V_{grid} decreases.

The condition for operating the inverter only in CCM is obtained by setting the argument of arcsine in Equations (9) and (10) less than 0, and is given as

$$I_o > \frac{V_g T_s}{L}, \tag{11}$$

and the condition for operating the inverter only in DCM is obtained by setting the argument of arcsine in Equations (9) and (10) greater than 1, and is given as

$$I_o < \frac{V_g T_s}{L}\left(1 - \frac{V_g}{V_{in}}\right). \tag{12}$$

The waveforms i_{L2} and V_{L2} of the inductor L_2 for $V_{grid} > 0$ V are the same as i_{L1} and V_{L1} except that they are delayed by $T_s/2$.

The waveforms i_{L1}, V_{L1}, i_{L2}, and V_{L2} for $V_{grid} < 0$ V are identical to the waveforms i_{L2}, V_{L2}, i_{L1}, and V_{L1} for $V_{grid} > 0$ V, respectively, except that the polarity is reversed.

2.2. Design Constraint for L_1 and L_2

The inverter must operate at $I_o \le I_{o,\max}$. The highest switching duty $D_{SU1_\max}$ of S_{U1} is calculated using Equation (8) as

$$D_{SU1_\max} = \frac{\sqrt{4V_g^2 + (\omega LI_{o_\max})^2}}{2V_{in}} < 1 \tag{13}$$

which results in the upper bound of $L_1 = L_2 = L$ as

$$L < \frac{2\sqrt{V_{in}^2 - V_g^2}}{\omega I_{o_\max}}. \tag{14}$$

This condition gives $L < 103.44$ mH when $P_o = 2$ kW and $I_{o_\max} = 12.9$ A.

The current and voltage waveforms for L_2 are same as those for L_1, except the time delay by $T_s/2$; hence, the output current ripple i_{o_ripple} of the proposed inverter can be calculated using Equations (1), (2) and (8) as

$$i_{o_ripple} = \frac{V_{in}T_s}{L} D(1-2D). \tag{15}$$

for $0 < D < 1/2$ and

$$i_{o_ripple} = \frac{V_{in}T_s}{L} (1-D)(2D-1). \tag{16}$$

for $1/2 < D < 1$; the highest i_{o_ripple} occurs at $D = 1/4$ or $3/4$. After allowing the highest i_{o_ripple} of 1 A at $P_o = 2$ kW and $f_s = 20$ kHz (this condition corresponds to THD < 3%), the lower bound of L is obtained using Equations (15) and (16) as

$$L \geq \frac{V_{in}T_s}{8 i_{o_ripple_\max}} \approx 2.5 \text{ mH}. \tag{17}$$

$L_{\min} = 2.5$ mH was used in the experimental inverters to minimize the inductor size.

2.3. Controller Design

The controller (Figure 5) was designed using Texas Instrument's TMS320F28335 digital signal processor (DSP). This controller inputs V_{grid}, i_{o_avg}, and V_{in} and uses the D-Q axis control method [17] to produce gating signals $S_{U1} - S_{U3}$ and $S_{D1} - S_{D3}$ that can generate a sinusoidal i_{o_avg}. The controller consists of a phase-locked loop (PLL), a D-Q axis controller, and a gate pulse generator. The DSP operates at a clock frequency $f_{clk} = 1/T_{clk} = 150$ MHz and the sampling frequency is the same as the switching frequency $f_s = 1/T_s = 20$ kHz. Thus, the sampling sequence number n is in the range of $0 \leq n \leq 332$ when the grid frequency $f = \omega/2\pi = 60$ Hz, and clock sequence number j is in the range of $0 \leq j \leq 7499$.

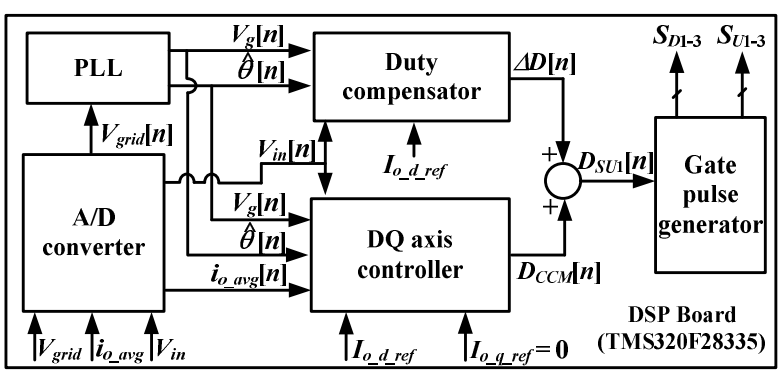

Figure 5. Block diagram of the control circuit for the proposed inverter.

The PLL (Figure 6) sets $n = 0$ and starts to operate when $V_{grid} = 0$ and the enable signal EN = 1. This circuit inputs V_{grid} and estimates the amplitude V_g and phase $\hat{\theta} = \hat{\omega}t$ of V_{grid}. Using $V_{grid}[n] = V_g \sin(\theta[n])$, the PLL generates a virtual grid-voltage V_{grid_qs} as

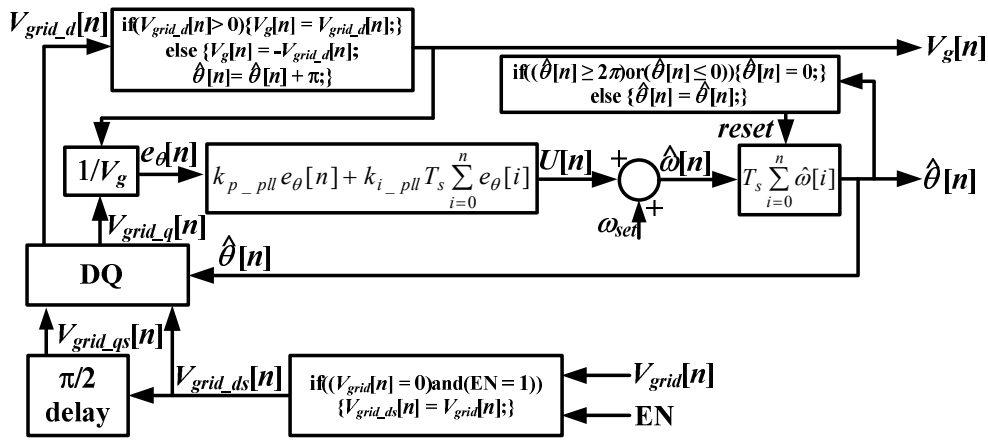

Figure 6. Block diagram of the phase locked loop.

$$V_{grid_qs}[n] = V_g \cos(\theta[n]) \tag{18}$$

$\hat{\theta}[0]$ has been set to 0 if V_{grid_qs} [0] ≥ 0 and to π otherwise. Thus, the initial estimation error $e_\theta[0] = \theta[0] - \hat{\theta}[0]$ is very small. V_{grid} and V_{grid_qs} are transformed into the voltages V_{grid_d} and V_{grid_q} in the synchronous reference frame as

$$\begin{pmatrix} V_{grid_d} \\ V_{grid_q} \end{pmatrix} = \begin{pmatrix} \sin(\hat{\theta}[n]) & \cos(\hat{\theta}[n]) \\ \cos(\hat{\theta}[n]) & -\sin(\hat{\theta}[n]) \end{pmatrix} \begin{pmatrix} V_{grid_ds} \\ V_{grid_qs} \end{pmatrix} \tag{19}$$

Because

$$V_{grid_d} = V_g \cos\left(\theta[n] - \hat{\theta}[n]\right) \approx V_g \tag{20}$$

$$V_{grid_q} = V_g \sin\left(\theta[n] - \hat{\theta}[n]\right) \approx V_g \left(\theta[n] - \hat{\theta}[n]\right) \tag{21}$$

when $\hat{\theta}[n] \approx \theta[n]$, V_g and $e_\theta[n] = \theta[n] - \hat{\theta}[n]$ can be calculated using Equations (20) and (21). The PLL loop filter for a proportional-integral (PI) control produces

$$\hat{\theta}[n] = T_s \sum_{m=0}^{n} \left(\omega_{set} + k_{p_pll} e_\theta[m] + k_{i_pll} T_s \sum_{i=0}^{m} e_\theta[i] \right) \tag{22}$$

This equation is equivalent to

$$\hat{\theta}(s) = \frac{k_p s + k_i}{s^2 + k_p s + k_i} \theta(s) + \frac{\omega_{set}}{s^2 + k_p s + k_i} \tag{23}$$

in the s-domain, where s is the complex frequency. The final value theory $\lim_{s \to 0} s\hat{\theta}(s) = \lim_{t \to \infty} \hat{\theta}(t)$ of the Laplace transform yields $\lim_{t \to \infty} \hat{\theta}(t) = \lim_{t \to \infty} \theta(t)$, i.e., $\hat{\theta} \approx \theta = \omega t$ under steady state. (k_p = 2000 and k_i = 0.1 have been chosen for the experimental inverter; these values result in at a zero at s = −0.00005 and two poles at s ≈ −0.00005 and −2000, so the loop filter operates as a first-order system with a cutoff frequency $f_c \approx 2000/2\pi$ Hz = $f_s/20\pi \approx 5 \times 60$ Hz.)

The D-Q axis controller (Figure 7) consists of a CCM duty-calculator and a duty compensator. The CCM duty-calculator inputs i_{o_avg} and V_{in} from the inverter, and $\hat{\theta}$ and V_g from the PLL. In the CCM duty-calculator, $i_{o_avg} = i_{o_ds}$ is delayed by $\pi/2$ to obtain the virtual current i_{o_qs} of i_{o_avg}. The D-Q

transformation separates i_{o_avg} into a D component I_{o_d} parallel to the grid voltage and a Q component I_{o_q} orthogonal to the grid voltage:

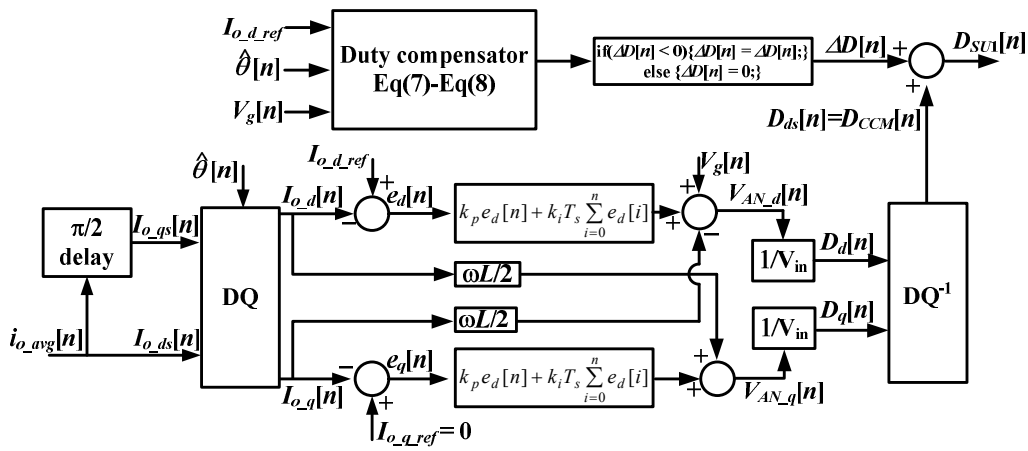

Figure 7. Block diagram of the D-Q axis controller.

$$\begin{pmatrix} I_{o_d} \\ I_{o_q} \end{pmatrix} = \begin{pmatrix} \sin(\hat{\theta}[n]) & \cos(\hat{\theta}[n]) \\ \cos(\hat{\theta}[n]) & -\sin(\hat{\theta}[n]) \end{pmatrix} \begin{pmatrix} i_{o_ds} \\ i_{o_qs} \end{pmatrix} \tag{24}$$

For given I_{0_d} and I_{o_q}, the circuit topology results in the D-Q components of V_{AN} in the synchronous reference frame as

$$\begin{pmatrix} V_{AN_d} \\ V_{AN_q} \end{pmatrix} = \begin{pmatrix} V_g \\ 0 \end{pmatrix} + \frac{\omega L}{2} \begin{pmatrix} -I_{o_q} \\ I_{o_d} \end{pmatrix} + \frac{L}{2} \frac{d}{dt} \begin{pmatrix} I_{o_d} \\ I_{o_q} \end{pmatrix}, \tag{25}$$

and the D-Q components of the switching duty as

$$\begin{pmatrix} D_d \\ D_q \end{pmatrix} = \frac{1}{V_{in}} \begin{pmatrix} V_g \\ 0 \end{pmatrix} + \frac{\omega L}{2V_{in}} \begin{pmatrix} -I_{o_q} \\ I_{o_d} \end{pmatrix} + \frac{L}{2V_{in}} \frac{d}{dt} \begin{pmatrix} I_{o_d} \\ I_{o_q} \end{pmatrix}, \tag{26}$$

because $V_{AN_d} = V_{in} D_d$ and $V_{AN_q} = V_{in} D_q$. The D-Q axis controller inputs $I_{o_d_ref}$ and $I_{o_q_ref}$ as the reference values of I_{o_d} and I_{o_q}, respectively, and calculates the errors $e_d[n] = I_{o_d_ref} - I_{o_d}$ and $e_q[n] = I_{o_q_ref} - I_{o_q}$. Then, the controller generates the D-Q components of the switching duty for CCM operation:

$$\begin{pmatrix} D_d[n] \\ D_q[n] \end{pmatrix} = \frac{1}{V_{in}} \begin{pmatrix} V_g \\ 0 \end{pmatrix} + \frac{\omega L}{2V_{in}} \begin{pmatrix} -I_{o_q}[n] \\ I_{o_d}[n] \end{pmatrix} + \frac{k_p}{V_{in}} \begin{pmatrix} e_d[i] \\ e_q[n] \end{pmatrix} + \frac{k_i T_s}{V_{in}} \sum_{i=0}^{n} \begin{pmatrix} e_d[i] \\ e_q[i] \end{pmatrix} \tag{27}$$

Both D and Q components have equivalent closed-loop transfer function in the s-domain as

$$\frac{I_{o_d}(s)}{I_{o_d_ref}(s)} = \frac{I_{o_q}(s)}{I_{o_q_ref}(s)} = \frac{k_p s + k_i}{Ls^2 + k_p s + k_i} \equiv H(s). \tag{28}$$

$k_p = 5$ and $k_i = 25$ have been chosen for the $H(s)$ of the experimental inverter. These values result in a zero at s = −5 and two poles at s ≈ −5.012, s ≈ −1944.99. The zero at $s = -5$ is close enough to cancel the pole at $s \approx -5.012$; hence, $H(s)$ operates like a first-order system with a cutoff frequency $f_c \approx 2000/2\pi$ Hz = $f_s/20\pi \approx 5 \times 60$ Hz [18].

To operate the inverter with a power factor of 1, the reference inputs must be $I_{o_d_ref} = I_o = 2P_o/V_g$ and $I_{o_q_ref} = 0$; therefore, $I_{o_d} \rightarrow I_{o_d_ref} = I_o$ and $I_{o_q} \rightarrow I_{o_q_ref} = 0$ under steady state. Thus, the inverse D-Q transform produces the switching duty D_{CCM} for CCM operation as

$$D_{CCM} = D_{ds} = D_d \sin(\omega t) + D_q \cos(\omega t) = \frac{V_g \sin(\omega t)}{V_{in}} + \frac{\omega L I_o \cos(\omega t)}{2V_{in}} \tag{29}$$

that is given in Equation (8).

The duty compensator inputs V_{in} from the inverter, $\hat{\theta}$ and V_g from the PLL, and $I_{o_d_ref}$ from CCM duty-calculator. Then, the compensator uses in Equations (7) and (8) to calculate the steady-state duty difference ΔD between the switching duties for CCM and DCM operations. ΔD is given by

$$\begin{aligned}\Delta D[n] = &\left(\frac{LI_{o_d_ref} V_g \sin^2(\hat{\theta}[n])}{V_{in}\left(V_{in} - 2V_g \sin(\hat{\theta}[n])\right)T_s} + \left(\frac{\omega L I_{o_d_ref} \cos(\hat{\theta}[n])}{4V_{in}}\right)^2\right)^{1/2} \\ &- \frac{V_g \sin(\hat{\theta}[n])}{V_{in}} - \frac{\omega L I_{o_d_ref} \cos(\hat{\theta}[n])}{4V_{in}}.\end{aligned} \tag{30}$$

The time fraction Δ in Equation (5) for which $i_L \neq 0$ is calculated using Equation (7) as

$$\begin{aligned}\Delta = &\frac{V_{in}}{V_g \sin(\hat{\theta}[n])}\left(\left(\frac{LI_{o_d_ref} V_g \sin^2(\hat{\theta}[n])}{V_{in}\left(V_{in} - 2V_g \sin(\hat{\theta}[n])\right)T_s} + \left(\frac{\omega L I_{o_d_ref} \cos(\hat{\theta}[n])}{4V_{in}}\right)^2\right)^{1/2}\right. \\ &\left. + \frac{\omega L I_{o_d_ref} \cos(\hat{\theta}[n])}{4V_{in}}\right) - \frac{\omega L I_{o_d_ref} \cos(\hat{\theta}[n])}{2V_g \sin(\hat{\theta}[n])} < 1\end{aligned} \tag{31}$$

which yields

$$\begin{aligned}&\sqrt{\frac{LI_{o_d_ref} V_g \sin^2(\hat{\theta}[n])}{V_{in}\left(V_{in} - 2V_g \sin(\hat{\theta}[n])\right)T_s} + \left(\frac{\omega L I_{o_d_ref} \cos(\hat{\theta}[n])}{4V_{in}}\right)^2} + \frac{\omega L I_{o_d_ref} \cos(\hat{\theta}[n])}{4V_{in}} \\ &< \frac{V_g \sin(\hat{\theta}[n])}{V_{in}} + \frac{\omega L I_{o_d_ref} \cos(\hat{\theta}[n])}{2V_{in}}\end{aligned}. \tag{32}$$

This equation shows that the switching duty in Equation (7) for DCM operation is always smaller than the one in Equation (8) for CCM operation. Thus, the controller uses $D_{SU1}[n] = D[n] = D_{CCM}[n] + \Delta D[n]$ when $\Delta D[n] < 0$, and the inverter operates in DCM. Otherwise, the controller sets $\Delta D[n] = 0$, and the inverter operates in CCM.

The gate pulse generator (Figure 8) inputs D_{SU1} form the D-Q axis controller and generates gate pulses for $S_{U1} - S_{U3}$ and $S_{D1} - S_{D3}$. In the gate pulse generator, two saw-tooth-signals $S_c[j]$ and $S_{cp}[j]$ are generated using two 16-bit up/down (U/D) counters; at each clock (clk) edge, the outputs $S_c[j]$ and $S_{cp}[i]$ of U/D counters increase by 1 when U/D = UP and decrease by 1 when U/D = DOWN. Initial values of saw-tooth signals are $S_c[0] = 0$, $S_{cp}[0] = T_s/(2T_{clk})$, $U/D_1[0]$ = UP, and $U/D_2[0]$ = DOWN to yield an interleave operation.

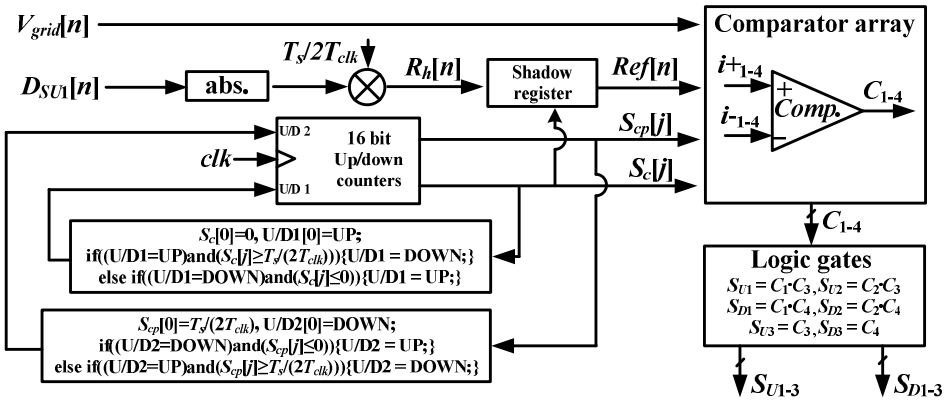

Figure 8. Block diagram of the gate pulse generator.

At each clock edge, $S_c[j]$ increases by 1 for $nT_s \leq t < (n+(1/2))T_s$ during which U/D$_1$ is UP, and $S_c[j]$ decreases by 1 for $(n+(1/2))T_s \leq t < (n+1)T_s$ during which U/D$_1$ is DOWN. When $S_c[j] < 0$, U/D$_1$ changes to UP and the next sequence begins. $S_{cp}[j]$ decreases by 1 for $nT_s \leq t < (n+(1/2))T_s$ during which U/D$_2$ is DOWN, and $S_{cp}[j]$ increases by 1 for $(n+(1/2))T_s \leq t < (n+1)T_s$ during which U/D$_2$ is UP. U/D$_2$ changes to DOWN when $S_{cp}[j] < 0$, and the next sequence begins. Thus, $S_{cp}[j]$ is a time-delayed signal of $S_c[j]$ by $T_s/2$, the maximum values of $S_c[j]$ and $S_{cp}[j]$ are $T_s/(2T_{clk})$, and the minimum values of $S_c[j]$ and $S_{cp}[j]$ are 0. To generate PWM signals using the saw-tooth signals, a reference signal $R_h[n]$ is generated using D_{SU1} and $T_s/(2T_{clk})$ as

$$R_h[n] = \frac{T_s}{2T_{clk}} \left| D_{SU1}[n] \right|. \tag{33}$$

$R_h[n]$ is stored in the shadow register of the PWM generation module in TMS320F28335 and transferred to the comparator reference-input $Ref[n]$ when $S_C[j] = 0$. Two comparators check the sign of $V_{grid}[n]$: $C_3 = 1$ and $C_4 = 0$ for $V_{grid}[n] \geq 0$, otherwise $C_3 = 0$ and $C_4 = 1$ (Table 2). The other comparators output two PWM signals: $C_1 = 1$ for $Ref[n] > S_c[j]$ and $C_2 = 1$ for $Ref[n] > S_{cp}[j]$. Finally, the logic gates produce gate control pulses $S_{U1} = C_1 \cdot C_3$, $S_{U2} = C_2 \cdot C_3$, $S_{U3} = C_3$, $S_{D1} = C_1 \cdot C_4$, $S_{D2} = C_2 \cdot C_4$, and $S_{D3} = C_4$.

Table 2. Input and output relationship of comparator array.

Output	$i+_n$	$i-_n$
C_1	$Ref[n]$	$S_c[j]$
C_2	$Ref[n]$	$S_{cp}[j]$
C_3	$V_{grid}[n]$	0
C_4	0	$V_{grid}[n]$

3. Experimental Results and Discussions

The proposed inverter (Figure 9a, Table 3) was designed to operate at V_{in} = 400 V$_{DC}$, V_{grid} = 220 V$_{AC}$/60 Hz and 150 W ≤ P_o ≤ 2 kW, and it was fabricated and tested using the calculated circuit parameters. An IDBI [9] (Figure 9b, Table 3) and an FBI [1] (Figure 9c, Table 3) were also fabricated and tested for comparison; the circuit elements for these inverters were the same as those for the proposed inverter. The control circuits for all experimental inverters were implemented using the TMS320F28335 digital signal processor (DSP) from Texas Instruments.

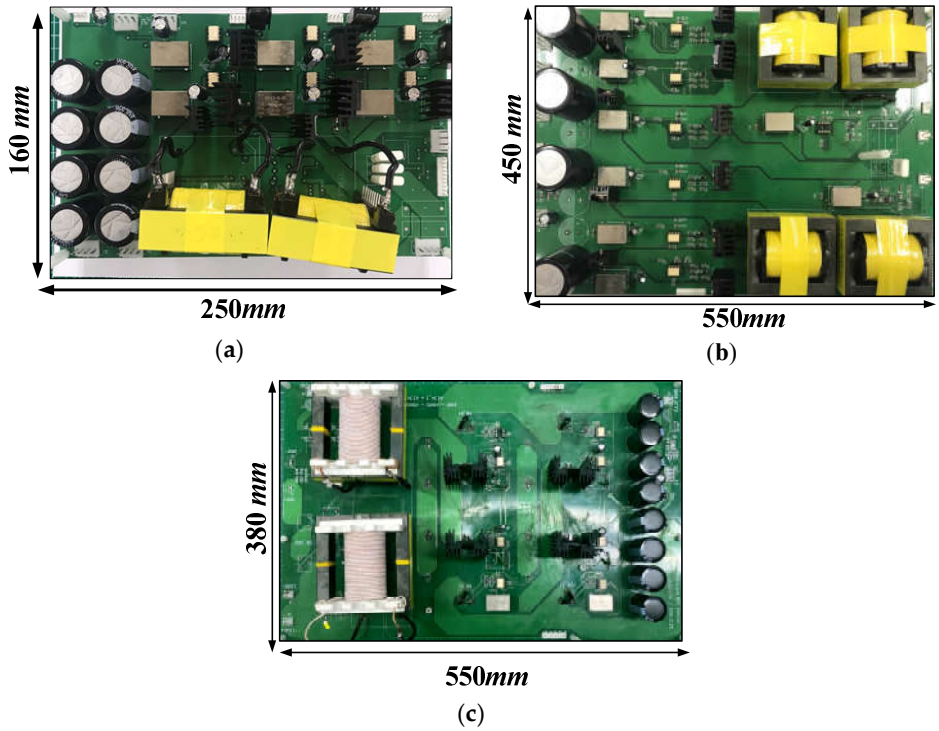

Figure 9. Photographs of the experimental inverters: (**a**) proposed inverter, (**b**) interleaved dual buck inverter (IDBI), and (**c**) full bridge inverter (FBI).

Table 3. Components for the experimental inverters.

Components		IDBI [9]	FBI	Proposed Inverter
HF Switches	Name	FCH110N65F	FCH110N65F	FCH110N65F
	Price ($)	5.03	5.03	5.03
	Number	4 (S_{U1}, S_{U3}, S_{D1}, S_{D2})	4 (S_1 - S_4)	4 (S_{U1}, S_{U3}, S_{D1}, S_{D2})
LF Switches	Name	IXFK80N60P3	-	IXFK80N60P3
	Price ($)	5.03	-	5.03
	Number	2 (S_{U3}, S_{D3})	-	2 (S_{U3}, S_{D3})
Diodes	Name	30ETH06	-	30ETH06
	Price ($)	1.59	-	1.59
	Number	4 (D_{U1}, D_{U2}, D_{D1}, D_{D2})	-	6 (D_{U1} – D_{U3}, D_{D1} – D_{D3})
Inductor core	Part Name	EER6062	EC90	EER6062
	Price ($)	4.94	16.17	4.94
	Number	4	2	2
Electrolytic capacitor	Part	EKMR451VS	EKMR451VS	EKMR451VS
	Name	N681MA50S	N681MA50S	N681MA50S
	Price ($)	2.68	2.68	2.68
	Number	8	8	8
Total costs ($)		77.74	73.9	71.04

The proposed inverter uses two inductors, whereas the IDBI uses four inductors, and the proposed inverter uses a small inductor core (EER6062), whereas the FBI uses a large inductor core. The fabricated inverters had a circuit volume of 160mm × 250 mm × 43.9 mm for the proposed inverter, 450 mm × 550 mm × 43.9 mm for the IDBI, and 380mm × 550 mm × 78.0 mm for the FBI; the proposed inverter reduced 83.8% of the circuit volume compared with the IDBI, and 89.3% compared

with the FBI. The circuit cost was \$71.04 for the proposed inverter, \$77.74 for the IDBI, and \$73.9 for the FBI; the proposed inverter saved 8.62% of the circuit cost compared with the IDBI, and 3.87% compared with FBI.

To verify operation of the proposed inverter, the waveforms of switch-control pulses (Figure 10a) were measured at Vin = 400 VDC, V_{grid} = 220 VAC/60 Hz, P_o = 2 kW, and f_s = 20 kHz. These waveforms show that the switches operated according to the switching states in Table I; when V_{grid} > 0 V, S_{U1} and S_{U2} operated in PWM mode, S_{U3} stayed ON and other switches stayed OFF; when V_{grid} < 0 V, S_{D1} and S_{D2} operated in PWM mode, S_{D3} stayed ON and other switches stayed OFF. The inductor currents i_{L1} and i_{L2}, and the leg voltages V_{GS_SU1} and V_{GS_SU2} (Figure 10b) show that the inverter operated in an interleaved mode; the phase differences between i_{L1} and i_{L2}, and between V_{GS_SU1} and V_{GS_SU2} were $T_s/2$. These switching states produced the sinusoidal leg voltage V_{AN} (Figure 10c).

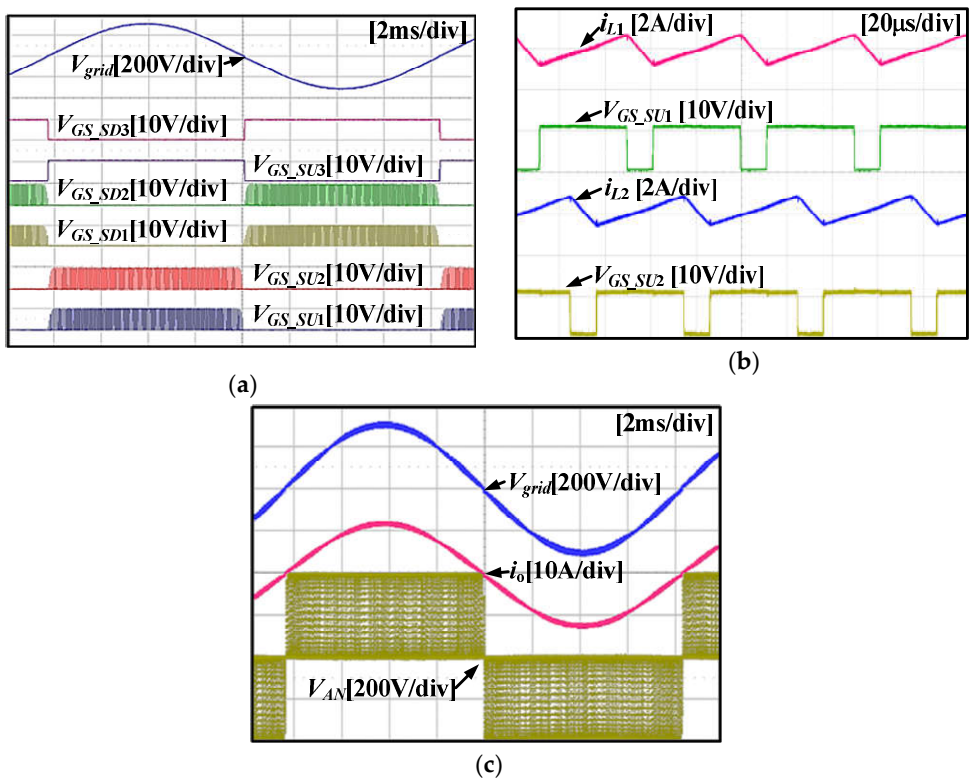

Figure 10. Experimental waveforms of proposed inverter, measured at V_{in} = 400 VDC, V_{grid} = 220 VAC/60 Hz, f_s = 20 kHz, and P_o = 2 kW: (**a**) gate input pulses, (**b**) V_{GS_SU1}, V_{GS_SU2}, i_{L1}, and i_{L2}, and (**c**) i_o, V_{AN}, and V_{grid}.

η_e vs. P_o (Figure 11) was measured at V_{in} = 400 VDC, V_{grid} = 220 VAC/60 Hz, 150 W ≤ P_o ≤ 2 kW, and f_s = 20 kHz and 40 kHz, using a PW3336 (HIOKI E.E. Co.) power meter. At f_s = 20 kHz, the proposed inverter had η_e > 98% for $P_o \geq 500$ W, but η_e for P_o < 500 W decreased as P_o decreased because the inverter operated in DCM. The highest power conversion efficiency $\eta_{e\,\max}$ of the proposed inverter was 98.5% at P_o = 1300 W when the power loss P_{DSP} of the gate control/drive circuit was included. ($\eta_{e\,\max}$ = 99.2% at P_o = 500 W when P_{DSP} was excluded.) The FBI does not use the interleaved buck inversion; hence, the switching and conduction losses in the current path were higher in the FBI than in the proposed inverter; as a result, the FBI had the lowest η_e among the inverters tested. The IDBI has a circuit structure similar to the proposed inverter and operates in interleaved mode, so η_e of the IDBI was very close to that of the proposed inverter. However, the proposed inverter requires two inductors to operate the inverter in interleaved mode, while the IDBI requires four inductors; hence, the proposed inverter can be implemented in a smaller size.

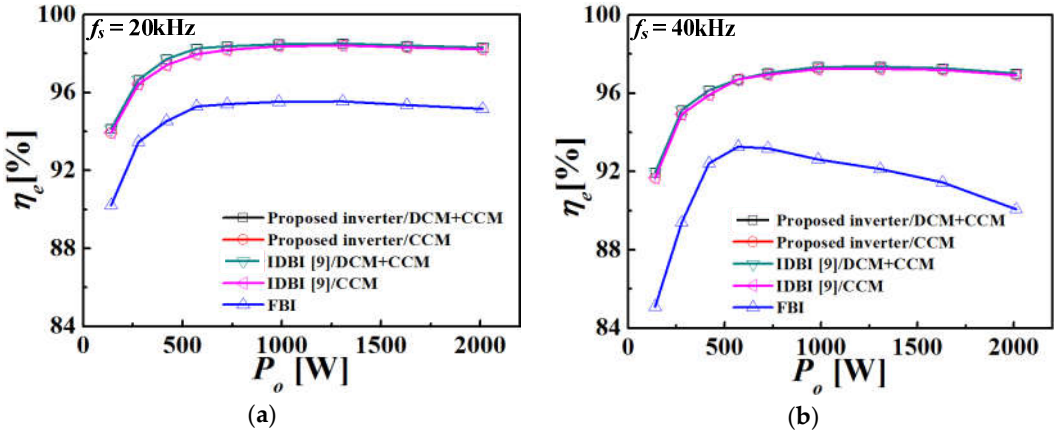

Figure 11. η_e vs. P_o for the experimental inverters operating at (**a**) f_s = 20 kHz and (**b**) f_s = 40 kHz: measured at V_{in} = 400 V_{DC}, V_{grid} = 220 V_{AC}/60 Hz, and Q_o = 0 VAR. The power loss P_{DSP} in the control circuit was included in η_e measurement.

Losses (Figure 12) of the experimental inverters were analyzed at V_{in} = 400 V_{DC}, V_{grid} = 220 V_{AC}/60 Hz, f_s = 20 kHz, P_o = 2 kW and 150 W, and reactive output power Q_o = 0 volt-ampere-reactive (VAR). The switching losses P_{SW} were 13.2 W for proposed, 13.89 W for IDBI, and 29.71 W for FBI at P_o = 2kW, and P_{SW} were 2.18 W for proposed, 2.48 W for IDBI, and 8.42 W for FBI at P_o = 150 W. The inverters operated at $V_{SW} = V_{in}$ and N_{SW} = 666 for proposed and IDBI, and $V_{SW} = V_{in}$ and N_{SW} = 1333 for FBI, where N_{sw} is the total switching number for one cycle of V_{grid}. Thus, the proposed inverter and IDBI had the lowest P_{SW}. The inductor loss P_{IND} was 9.25 W for proposed, 10.33 W for IDBI, and 66.32 W for FBI at P_o = 2kW and 0.155 W for proposed, 0.162 W for IDBI, and 0.66 W for FBI at P_o = 150 W. The proposed inverter uses interleaved inputs; hence, the inductor current i_L is half of the i_L of FBI. Moreover, the proposed inverter uses small inductors with fewer turns than that of the FBI. Thus, FBI had the highest P_{IND}. The diode loss P_D was 7.04 W for proposed, 6.45 W for IDBI, and 0 for FBI at P_o = 2 kW, and P_D was 0.907 W for proposed, 0.885 W for IDBI, and 0 for FBI at P_o = 150 W. The power loss P_{DSP} of the gate control/drive circuit was 6.02 W for proposed, 6.19 W for IDBI, and 6.48 W for FBI at both P_o = 150 W and P_o = 2 kW. The total power loss P_{loss} at P_o = 2 kW was 35.53 W for proposed, 36.87 W for IDBI, and 102.51 W for FBI, and the power conversion efficiency η_e at P_o = 2 kW was 98.2% for proposed, 98.1% for IDBI, and 94.9 % for FBI. P_{loss} at P_o = 150W was 9.279 W for proposed, 9.717 W for IDBI, and 15.5 W for FBI, and η_e at P_o = 150 W was 93.8% for proposed, 93.5% for IDBI, and 89.6 % for FBI.

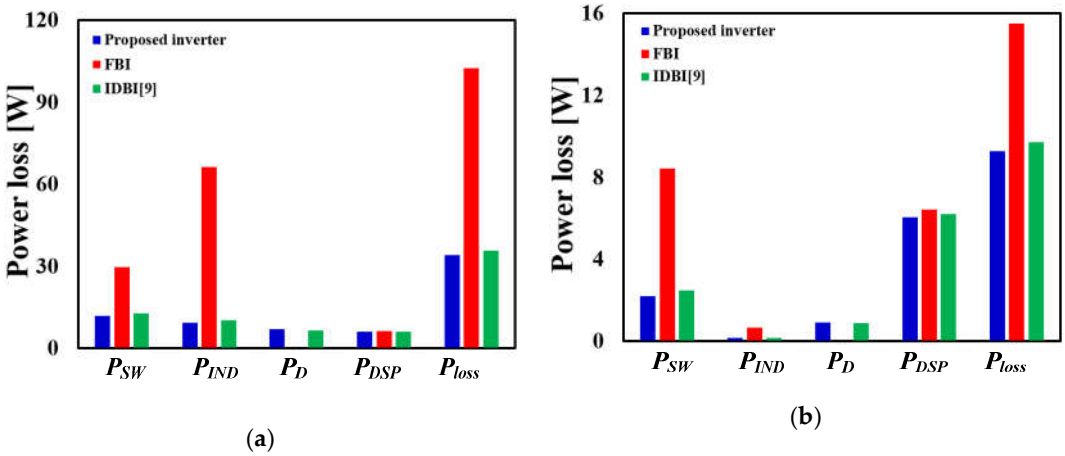

Figure 12. Power losses in the experimental inverters at (**a**) P_o = 2 kW and (**b**) P_o = 150W: calculated using PSPICE at V_{in} = 400 V_{DC}, V_{grid} = 220 V_{AC} / 60 Hz, f_s = 20 kHz, and Q_o = 0 VAR.

The temperature T_{SW} of switch vs. time of operation (Figure 13) was measured while operating the experimental inverters at V_{in} = 400 VDC, V_{grid} = 220 VAC/60 Hz, P_o = 2 kW, and f_s = 20 kHz. T_{SW} was stabilized at ~52 °C (S_{U1}, S_{U2}, S_{D1}, S_{D2}) and ~55 °C (S_{U3}, S_{D3}) in the proposed inverter, ~54 °C (S_{U1}, S_{U2}, S_{D1}, S_{D2}) and ~58 °C (S_{U3}, S_{D3}) in the IDBI, and at ~110 °C in FBI. P_{SW} at P_o = 2 kW were 13.2 W for proposed, 13.89W for IDBI, and 29.71 W for FBI; therefore, T_{sw} of the proposed inverter and IDBI was half that of FBI.

THD of i_o vs. P_o (Figure 14) was also measured at V_{in} = 400 VDC, V_{grid} = 220 VAC/60 Hz, P_o = 150 W ~ 2 kW, and f_s = 20 kHz. THD at P_o = 2 kW was 0.66% for proposed and IDBI and 3.25% for FBI; FBI had the highest THD because this inverter produced a ZCD during the dead-time period. THD at P_o = 150 W was 16.6% for IDBI and the proposed inverter when the switching duties for the inverters were controlled using the CCM control (given in (8)). At a low P_o, the proposed inverter operated in DCM for some time-interval of sinusoidal V_{grid}, as discussed in Section 2.2. This operation produced a distortion in I_o when the inverters were operated under CCM control only.

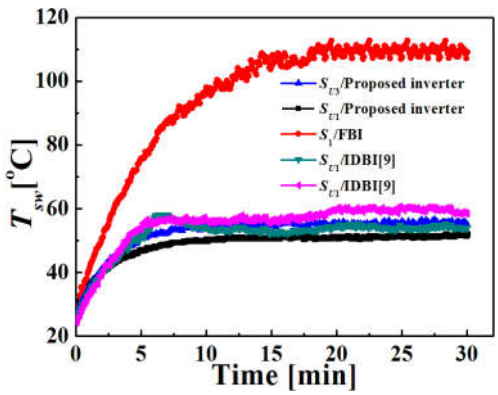

Figure 13. Switch temperature T_{SW} vs. time of operation, measured at V_{in} = 400 VDC, V_{grid} = 220 VAC/60 Hz, f_s = 20 kHz, P_o = 2 kW, and Q_o = 0 VAR.

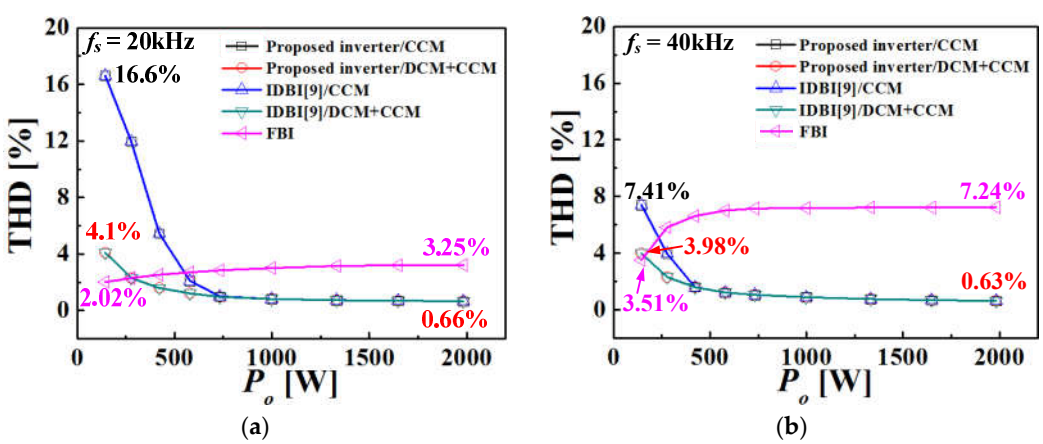

Figure 14. Total harmonic distortion (THD) of i_o vs. P_o for the experimental inverters operating at (**a**) f_s = 20 kHz and (**b**) f_s = 40 kHz: measured at V_{in} = 400 VDC and V_{grid} = 220 VAC/60 Hz.

When the switching duties for IDBI and the inverters were controlled using the proposed DCM+CCM control (a combination of the CCM control and the DCM control given in Equation (7)), the THD at P_o = 150 W was reduced to 4.1% because the combined DCM+CCM control reduced the distortion in I_o significantly.

When f_s was increased to 40 kHz, THD of i_o at P_o = 2 kW was 0.63% for proposed and IDBI and 7.24% for FBI. The FBI nearly doubled the THD at f_s = 40 kHz compared to the value at f_s = 20 kHz, because the change increased the effect of dead-time on the switching duty. The THD at P_o = 150 W

was 7.41% for the proposed inverter using CCM control, 3.98% for the proposed inverter using DCM+CCM control, and 3.51% for FBI. The DCM operating time was reduced at higher f_s (Equations (9) and (10)); hence, THD of the proposed inverter decreased as f_s increased; a DCM control near the zero crossing point increased i_L. In contrast, the THD for FBI increased as f_s increased because the impact of dead-time on the switching duty increased.

The waveforms of i_o and i_{o_avg} for the experimental inverters (Figure 15) were measured at V_{in} = 400 V_{DC}, V_{grid} = 220 V_{AC}/60 Hz, f_s = 20 kHz, P_o = 150 W, Q_o = 0 VAR, and I_o = 0.95 A. The cutoff frequency of the low-pass filter for i_{o_avg} measurement was 2 kHz (=f_s/10). The inverters were controlled using

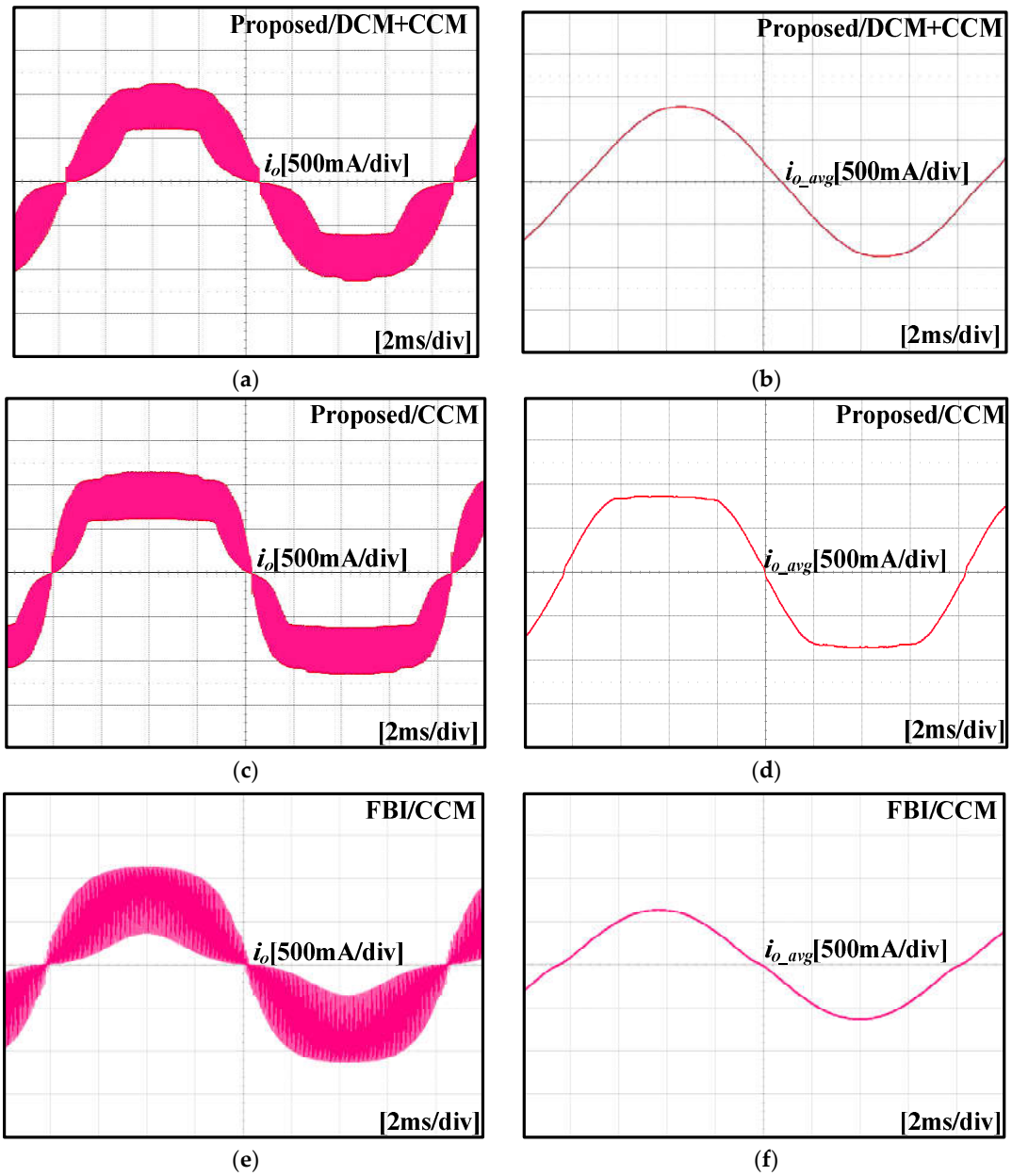

Figure 15. Waveforms of i_o and i_{o_avg} measured at at V_{in} = 400 V_{DC}, V_{grid} = 220 V_{AC} / 60 Hz, fs = 20 kHz, P_o = 150 W, Q_o = 0 VAR, and I_o = 0.95 A: (a) i_o (Proposed, DCM+CCM), (b) i_{o_avg} (Proposed, DCM+CCM), (c) i_o (Proposed, CCM), (d) i_{o_avg} (Proposed, CCM), (e) i_o (FBI, CCM), (f) i_{o_avg} (FBI, CCM).

CCM or DCM+CCM control. The waveforms of i_o show that the proposed inverter had the lowest switching ripple of i_o, and the waveforms of i_{o_avg} show that the DCM+CCM control of the proposed inverter achieved the best sinusoidal waveform. The harmonic components of i_o (Figure 16) show that

harmonics of i_o of FBI were slightly higher than those of the proposed inverter because the proposed inverter operated as an interleaved dual buck inverter.

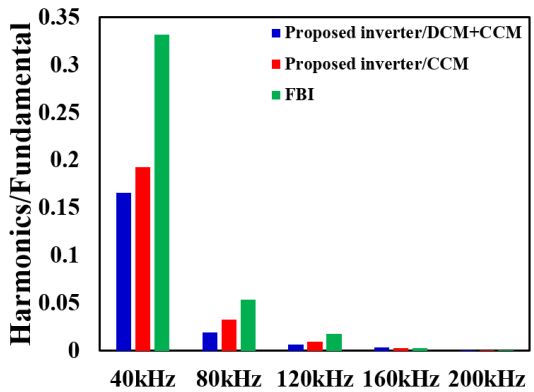

Figure 16. Harmonic components of i_o; measured at V_{in} = 400 VDC, V_{grid} = 220 VAC/60 Hz, f_s = 20 kHz, P_o = 150 W, Q_o = 0 VAR, and I_o = 0.95 A.

The dynamic responses of the proposed inverter (Figure 17) were measured for a step change of P_o from 2 kW to 1 kW and a step change of P_o from 1 kW to 2 kW; the operating conditions for this measurement were V_{in} = 400 VDC, V_{grid} = 220 VAC/60 Hz, f_s = 20 kHz, and Q_o = 0 VAR. For both P_o changes, the output current i_o did not overshoot, and the transient time of i_o was < 2 ms, which is ~1/8 of the sinusoidal period at 60 Hz. PF, THD, and i_o of the proposed inverter were measured for P_o = 666.6 W, 1.333 kW, and 2 kW at V_{in} = 400 VDC, V_{grid} = 220 VAC/60 Hz, f_s = 20 kHz, and line impedance Z = 0.4 + j0.25 Ω. The measured PF was 0.9973 at P_o = 666.6 W (33% of the rated power), 0.9985 at P_o = 1.333 kW (66% of the rated power), and 0.9992 at P_o = 2 kW (100% of the rated power). The measured THD of i_o was 4.20% at P_o = 666.6 W, 3.68% at P_o = 1.333 kW, and 3.43% at P_o = 2 kW. These results fulfill most grid-connected inverter standards for renewable energy [19–22].

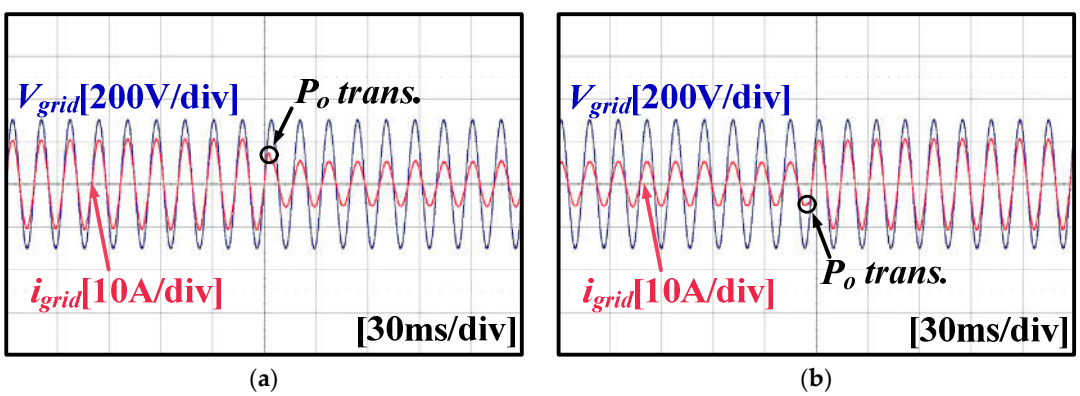

Figure 17. Step responses of the proposed inverter at V_{in} = 400 VDC, V_{grid} = 220 VAC/60 Hz, f_s = 20 kHz, and Q_o = 0 VAR: (**a**) for a decrease of P_o from 2 kW to 1 kW and (**b**) for an increase of P_o from 1 kW to 2 kW.

Comparisons (Table 4) of the circuit parameters and experimental results demonstrate the superiority of the proposed inverter. The proposed inverter has the following advantages: 1) proposed inverter requires two inductors, whereas IDBI requires four inductors; hence, the proposed inverter can be implemented with lower cost and smaller volume than IDBI; 2) it uses interleaved operation, which reduces the current stress of the switch by 1/2 of that in FBI; 3) the number of switching for one period of V_{grid} in the proposed inverter is 1/2 of that in FBI; hence, the switching loss is reduced; and 4) η_e at P_o = 2 kW is as high as 98.3%, compared to 95.0% for FBI. These advantages indicate that the proposed inverter is useful for high-power dc-ac power conversion.

Table 4. Circuit parameters and experimental results for experimental inverters. Parenthesis contain peak switch voltages and currents measured at V_{in} = 404 V.

Circuit Parameters		Proposed Inverter	IDBI [9]	FBI
# of switches		6	6	4
# of diodes		6	4	0
# of inductors		2	4	2
$V_{sw,max}$	Unfolding	V_{in} (404 V)	V_{in} (404 V)	-
	Switching	V_{in} (413 V)	V_{in} (415 V)	V_{in} (423 V)
$I_{sw,max}$	Unfolding	I_o (13.1 A)	I_o (13.5 A)	-
	Switching	I_o/2 (5.8 A)	I_o/2 (6.0 A)	I_o (13.5 A)
Inductance		2.5 mH	2.5 mH	2.5 mH
THD at P_o = 2 kW		0.66%	0.66%	3.25%
Maximum efficiency		98.5%	98.4%	95.2%
Efficiency at P_o = 2 kW		98.3%	98.2%	95.0%

4. Conclusion

This paper proposes an inverter that can achieve high power conversion efficiency η_e at high output power P_o. The inverter uses a dual-buck structure to eliminate zero-cross distortion, operates in an interleaved mode to reduce the current stress of switch, and uses DCM + CCM combined control to reduce the output current distortion at low output power. The size and weight of the circuit are reduced by decreasing the number of inductors and by using blocking diodes; the proposed inverter could reduce 83.8% of the circuit volume compared with IDBI and 89.3% compared with FBI, and it could save 8.62% of the circuit cost compared with IDBI and 3.87% compared with FBI. When the experimental inverter was operated at an input voltage of 400 V_{DC}, an output voltage of 220 V_{AC}/60 Hz, and switching frequency of 20 kHz, η_e was > 94% at 150 W ≤ P_o ≤ 2 kW, 98.5% at P_o = 1300 W, and 98.3% at P_o = 2 kW. The total harmonic distortion was 0.66% at P_o = 2kW. The proposed inverter is well-suited for high power dc-ac power conversion.

Author Contributions: M.-G.C. developed the circuit, constructed the hardware prototype, and conducted the experiments. B.-K.K. provided guidance and key suggestions for this study. S.-H.L., H.-S.L., and Y.-G.C. collected the data and investigated early works. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

$C_1 - C_4$	Output of comparators in the PWM generator.
D	Switching duty of the proposed inverter.
D_d	Amplitude of D_{SU1} parallel to V_{grid}.
D_{D1}, D_{D2}	Low-side freewheeling diodes of the proposed inverter and IDBI [9].
D_q	Amplitude of D_{SU1} orthogonal to V_{grid}.
D_{SU1}	Switching duty of S_{U1} in the proposed inverter.
D_{U1}, D_{U2}	High-side freewheeling diodes of the proposed inverter and IDBI [9].
D_{U3}, D_{D3}	Blocking diodes of the proposed inverter.
e_d, e_q	Control errors of I_{o_d} and I_{o_q} in the D-Q axis controller (A).
e_θ	Estimation error of $\hat{\theta}$ in the phased locked loop (rad).

f_{clk}, T_{clk}	Clock frequency (Hz), and period (s) of TMS320F28335 digital signal processor.
f_s, T_s	Switching frequency (Hz) and period (s).
i_{L1}, i_{L2}	Inductor currents of the proposed inverter (A).
i_{L1_avg}, i_{L2_avg}	Time average of i_{L1} and i_{L2} of the proposed inverter (A).
I_o	Amplitude of i_{o_avg} (A).
i_{o_avg}	Time averaged value of the output current i_o for one switching period (A).
I_{o_d}	Amplitude of i_{o_avg} parallel to V_{grid} (A).
$I_{o_d_ref}, I_{o_q_ref}$	Reference values of I_{o_d} and I_{o_q} for the D-Q axis controller (A).
I_{o_q}	Amplitude of i_{o_avg} orthogonal to V_{grid} (A).
i_{o_ripple}	Ripple in output current of the proposed inverter (A).
k_p, k_i	Control coefficients94768 for the D-Q axis controller.
k_{p_pll}, k_{i_pll}	Control coefficients for the phased locked loop.
L_1, L_2	Output filter inductors (H).
n, j	Sampling and clock sequence numbers.
Ref	Reference input for the comparator array in the PWM generator.
$S_1 - S_4$	High frequency switches of FBI [1].
S_c, S_{cp}	Counter outputs for PWM.
S_{D1}, S_{D2}	Low-side high frequency switches of the proposed inverter and IDBI [9].
S_{D3}	Low-side unfolding switch of the proposed inverter and IDBI [9].
S_{U1}, S_{U2}	High-side high frequency switches of the proposed inverter and IDBI [9].
S_{U3}	High-side unfolding switch of the proposed inverter and IDBI [9].
T_{sw}	Temperature of switches (°C).
V_{AN}	Leg voltage with respect to the ground (V).
V_{AN_avg}	Time averaged value of V_{AN} for one switching period (V).
V_{AN_d}	Amplitude of V_{AN_avg} parallel to V_{grid} (V).
V_{AN_q}	Amplitude of V_{AN_avg} orthogonal to V_{grid} (V).
V_g	Amplitude of V_{grid} (V).
V_{grid}	AC output voltage (AC grid voltage) (V).
V_{in}	DC input voltage (V).
V_{L1}, V_{L2}	Voltages across the output filter inductors L_1 and L_2 (V).
V_{L1_avg}, V_{L2_avg}	Time averaged values of V_{L1} and V_{L2} for one switching period (V).
ΔD	Difference of switching duties for CCM and DCM operations.
ΔT_s	Duration of $i_{L1}(t) \neq 0$ for one switching period (s).
θ	Phase angle of V_{grid} (rad).
$\hat{\theta}$	Estimated θ by the phased locked loop (rad).
η_e	Power conversion efficiency of inverters.
ω	Angular frequency of V_{grid} (rad/s).
ω_{set}	Nominal value of ω (rad/s).

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