Modulation and Capacitor Voltage Balancing Control of Multilevel NPC Dual-Active-Bridge DC-DC Converters

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***Abstract*— The present paper provides a solution to operate multilevel dual-active-bridge (ML-DAB) converters built upon neutral-point-clamped switching legs in a full-bridge disposition and with any number of levels on either side of the converter. The main issue of such converters is addressing the inherent unbalance of the dc-link capacitor voltages, which hinders the proper operation and optimum utilization of the converter. The proposed solution comprises a generalized to *N* levels modulation and control scheme that allows operating these converters while guaranteeing the proper balance of the dc-link capacitor voltages. The suitability of the proposed solution is verified through simulation and experimental tests performed in five different converter configurations, three of them with an asymmetric number of voltage levels, proving that capacitor voltage balance is achievable in a wide range of operation conditions. Moreover, the efficiency of the ML-DAB converters is demonstrated to be superior to the conventional two-level DAB case.**

***Index Terms*—Multilevel converter, neutral point clamped, bidirectional dc-dc converter, dual active bridge, capacitor voltage balancing.**

I. Introduction

GALVANICALLY-isolated bidirectional dc-dc converters (IBDCs) have recently received more attention due to its increasing use in systems requiring energy transfer between two dc networks in both directions, requiring galvanic isolation and a high voltage gain. Two-port single-stage IBDCs (2P-SS-IBDCs) are the most common converters and present the generalized structure of Fig. 1. The single-phase two-level dual-active-bridge converter (2L-DAB) is the most prominent topology among the 2P-SS-IBDCs. The full-bridged and half-bridged versions of the 2L-DAB were first presented in [1] and [2], respectively. The 2L-DAB is composed by a high-frequency (HF) dual-winding transformer, connected on each side to a 2L dc-ac (full-bridged or half-bridged) voltage-fed converter. In the conventional phase-shift modulation (PSM) [1], each dc-ac converter synthesizes a square-wave ac voltage waveform, allowing the transmission of power between both sides by simply phase-shifting the ac waveforms on each side. The magnitude and sign of such phase shift determines the amount and direction of the transferred power, respectively.

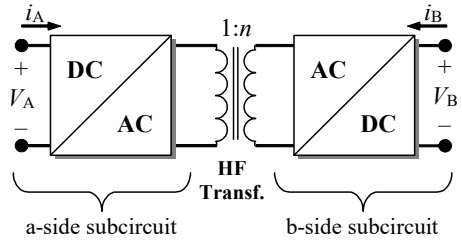

Fig. 1. Common structure of 2P-SS-IBDCs.

Let us define the dc conversion ratio, d, as the a-side-referred dc voltage gain,

$$d = \frac{V_B}{n \cdot V_A}, \tag{1}$$

where V_A and V_B are the dc-link voltages of each side and n is the transformer turns ratio.

When $d = 1$, PSM achieves zero-voltage switching (ZVS) in all switch turn-on transitions over the whole power range [1]. However, when $d \neq 1$, the transformer and dc-link capacitors rms currents, as well as the converter reactive power, increase significantly compared to the $d = 1$ case (for the same transferred power) and ZVS is limited to high powers, hence leading to higher conduction and switching losses, and lower efficiency, especially at low loads [3], [4].

As a consequence of this issue, an extensive and heterogeneous number of studies in the literature [3]–[10] are dedicated to the conventional 2L-DAB converter, focusing on topology variants and multiple modulation schemes with heterogeneous strategies, with the main objective of improving the converter efficiency.

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A natural step to further improve the performance of the DAB converter is to introduce multilevel (ML) topologies in the DAB structure. ML topologies [11] offer several advantages. On one hand, for a given power rating and semiconductor technology, they allow operating at higher dc voltages, which allows increasing the conversion efficiency. On the other hand, for a given dc-link voltage rating, they allow operating with lower-voltage-rated devices with better performance features, reduce both switching and conduction losses, reduce the total harmonic distortion of voltage and current waveforms, and improve the converter fault-tolerance capacity. Although ML topologies require a higher number of components than conventional 2L topologies, ML converters can take advantage of economies of scale. For instance, if converter designs at different voltage ratings are required, these converters could be built from a single widely-used and highly-optimized power device at a very competitive price per unit, by simply adjusting the number of converter voltage levels to each specific converter voltage rating. This may lead to lower converter overall design costs than using a design strategy based on the conventional 2L topology with a set of different devices at different voltage ratings. Moreover, introducing ML topologies into the DAB converter structure allows increasing the available degrees of freedom (DoF), which novel modulations can employ to further improve the converter performance.

Among the existing ML topology families, the neutral point clamped (NPC) topologies are the most promising in terms of efficiency, power density, and reliability [12].

References [13]–[17] introduce 3L-NPC legs on one side of the DAB converter, while on [18]–[21] these are present on both sides. In both cases, the NPC phase legs are present in either half-bridge or full-bridge configurations. A full-bridged four-level (4L)-DAB converter employing 4L-NPC legs on both sides is proposed in [22]. The main purpose to employ ML NPC legs on most of these cases is to enable higher dc-link voltages. Nevertheless, [19]–[21] also take advantage of the gained DoF to propose modulations that optimize the 3L-NPC DAB converter performance.

The main issue on converters employing NPC switching legs whose multiple voltage levels are generated through a capacitor voltage divider, is to maintain the capacitor voltages balanced. Many solutions have been proposed for modulations with high switching-to-fundamental frequency ratios (m_f). However, such modulations would incur in high switching losses in the DAB converter, due to the high-frequency nature of the DAB voltage and current fundamental components. Moreover, all the proposed DAB modulations in the literature feature $m_f = 1$.

References [15]–[17], [20], [21] address the dc-link capacitor voltage balancing on the full-bridged 3L-NPC DAB converter, while [22] does it for the full-bridged 4L-NPC DAB converter. Its principle of operation basically consists on controlling the charge being injected into/drawn from the inner dc-link points by modifying the modulation parameters [15], [16], [20]–[22] or by changing the switching sequence [17]. Nevertheless, references [20]–[22] are the only ones to provide a comprehensive study of the phenomenon, proposing a novel method to analyze and control the capacitor voltage balancing on full-bridged 3L-NPC and 4L-NPC DAB converters.

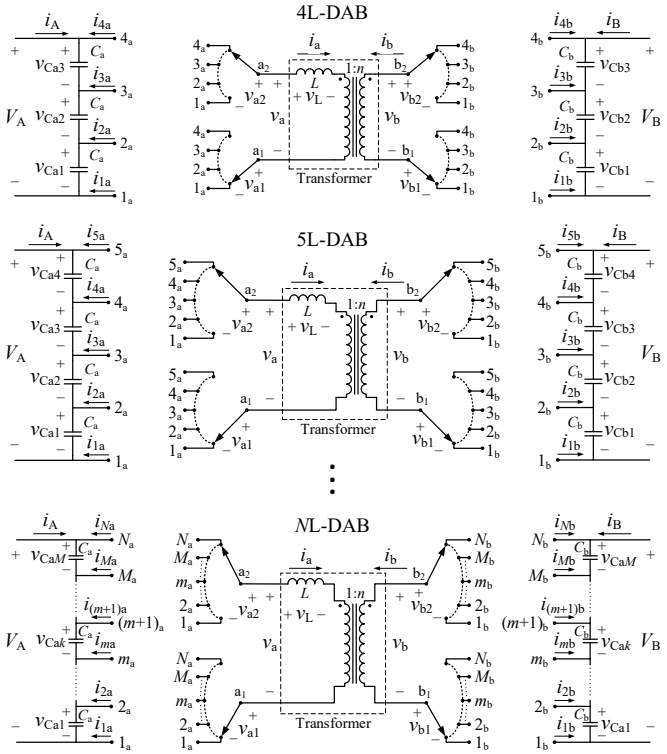


Fig. 2. Topologies of the proposed ML-DAB dc-dc converters.

The main novelty presented in this paper is a solution for the feasible operation of full-bridged NPC ML DAB (ML-DAB) converters with an arbitrary number of levels; i.e., an N-level (NL)-DAB converter. This solution consists on a generalized modulation and capacitor voltage balancing control, inferred from the results obtained in the studies of the full-bridged 3L-NPC DAB [21] and full-bridged 4L-NPC DAB [22] converters (3L-DAB and 4L-DAB from now on, respectively), and also from the novel study of the full-bridged five-level (5L)-NPC DAB converter (5L-DAB). The paper also proves the feasibility of implementing a ML-DAB converter with a different number of levels on each side (an asymmetric ML-DAB converter).

The paper is organized as follows. Section II presents the fundamentals of the 4L-, 5L-, and NL-DAB converters modulation strategies. Section III analyzes the capacitor voltage balancing issue for the same three cases and proposes proper capacitor voltage balancing control schemes for the 4L, 5L, and NL generalized case. Section IV presents simulation and experimental results to verify the feasibility of the proposed 4L-DAB and 5L-DAB converters, and by extension, of the NL-DAB converter, as well as the feasibility of implementing asymmetric ML-DAB converters employing the proposed solution. Section V outlines the conclusions.

II. MODULATIONS

Fig. 2 presents the topologies for the 4L-DAB, 5L-DAB, and *N*L-DAB converters. The *N*L general case is easily inferred from the 4L and 5L cases. These ML-DAB converters present two sides; i.e., a-side and b-side, delimited by a transformer. Each side presents a voltage-sourced dc-link with N connection points, numbered as 1_z, 2_z, …, N_z, where $z \in \{a,b\}$, and a total voltage of V_Z (where $Z \in \{A,B\}$).

Fig. 3 shows the modulation pattern for the 4L, 5L, and the general *N*L cases. The two *N*L-NPC phase legs on each side synthesize voltage-waveforms v_{z1} and v_{z2} with N voltage levels, by connecting its poles to the dc-link connection points. The full-bridge disposition of both legs helps synthesizing transformer voltages v_z, with $2N$–1 voltage levels. The switching-state sequence of side a can be seen on top of each figure, where the switching states are represented as $(xy)_z$, where $x, y \in \{1,2,\ldots,N\}$ indicate the z-side dc-link point to which nodes z_2 and z_1 are connected, respectively.

As in the conventional 2L-DAB, the fundamental components of voltages v_a and v_b are phase-shifted φ degrees in order to induce current i_a in inductor L so as to transfer power between both sides.

The dwell times of the *N*L-DAB z-side switching states are defined by $2M$ (where $M = N$–1) independent variables: inner switching angles $\alpha_{zi1}, \alpha_{zi2}, \ldots, \alpha_{ziM}$, and outer switching angles $\alpha_{zo1}, \alpha_{zo2}, \ldots, \alpha_{zoM}$, with

$$\begin{aligned} -90° \le \alpha_{zi1} \le \alpha_{zi2} \le \ldots \le \alpha_{ziM} \le 90° \\ -90° \le \alpha_{zo1} \le \alpha_{zo2} \le \ldots \le \alpha_{zoM} \le 90°. \end{aligned} \tag{2}$$

The proposed modulation allows maintaining $\overline{v}_z = 0$, $\forall z$, which guarantees a null steady-state transformer dc current and prevents the saturation of the transformer core, even when the dc-link capacitor voltages are not balanced. It also forces a symmetrical operation of both z-side full-bridge legs, as well as guaranteeing odd symmetry in v_a, v_b, and i_a waveforms, which is necessary for the capacitor voltage balancing strategy.

If

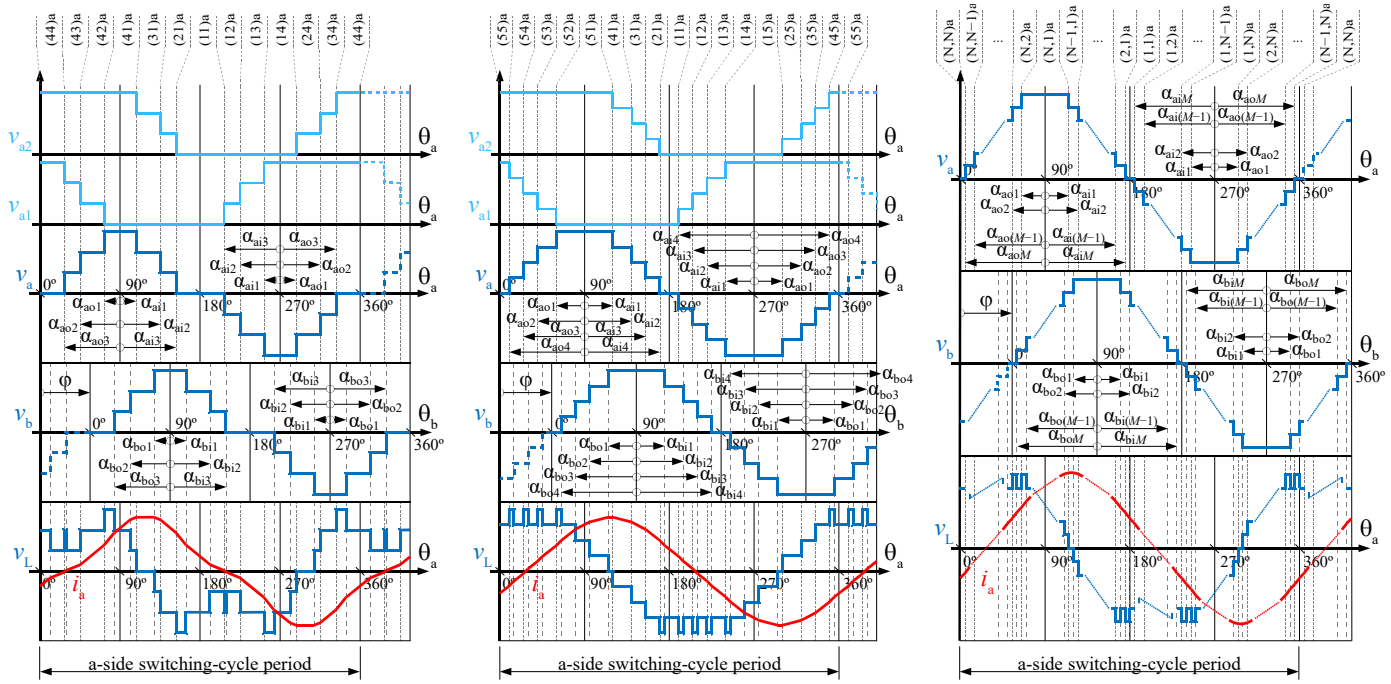
$$\begin{aligned} \alpha_{zo1} &= \alpha_{zi1} = \alpha_{z1} \\ \alpha_{zo2} &= \alpha_{zi2} = \alpha_{z2} \\ &\vdots \\ \alpha_{zoM} &= \alpha_{ziM} = \alpha_{zM} \end{aligned} \tag{3}$$

and the dc-link capacitor voltages are balanced, then quarter-wave symmetry is guaranteed and even-order harmonics are eliminated in v_a, v_b, and i_a waveforms.

With the proposed modulation, the power transfer capability; i.e., the maximum transferred power, of a ML-DAB converter is the same as the conventional 2L-DAB, since both can, ideally, synthesize perfect square-wave transformer voltages. However, in practice, ML converter legs cannot achieve perfect square-wave voltages, since it is necessary to leave at least a blanking time (t_b) between transitions, leading to stepped transitions between voltage levels with dwell times of at least t_b. Hence, a t_b value small enough in relationship to the switching-cycle period should be selected to avoid a reduction in the power transfer capability.

III. CAPACITOR VOLTAGE BALANCING

Fig. 4(a) and Fig. 4(c) present simulation results for the 4L-DAB and 5L-DAB, respectively, showing the dc-link capacitor voltages transient response under an initial balanced



(a) (b) (c)

Fig. 3. Voltage and current waveforms of the proposed ML-DAB dc-dc converters. (a) Four-level case. (b) Five-level case. (c) General *N*-level

state, where v_a and v_b voltage steps are defined with equal-value dwell times, and under the absence of a closed-loop control. In less than 50 ms, the transient reaches a steady state with an unacceptable permanent capacitor voltage unbalance that could destroy the semiconductor devices due to an excessive blocking voltage, besides leading to nonoptimal operating conditions.

Any electrical charge injected into (drawn from) any z-side inner dc-link point (2_z, 3_z, ..., M_z) will decrease (increase) the capacitor voltages above it and increase (decrease) the capacitor voltages below it. Therefore, to analyze the capacitor voltage balancing, the electrical charge provided to each inner dc-link point within a switching cycle should be studied.

Considering the generalized NL-DAB, the z-side inner dc-link point currents are

$$\begin{aligned} i_{2z} &= S_{z12}\cdot i_z - S_{z22}\cdot i_z \\ i_{3z} &= S_{z13}\cdot i_z - S_{z23}\cdot i_z \\ &\vdots \\ i_{Mz} &= S_{z1M}\cdot i_z - S_{z2M}\cdot i_z, \end{aligned} \tag{4}$$

where S_{zjm} is equal to 1 when leg z_j is connected to inner dc-link point m_z and 0 otherwise.

Following the same approach of [20]–[22], let us consider the effect of the fundamental component of i_z ($i_{z,1}$), as its amplitude is greater than each of the harmonic amplitudes. By the sum/difference trigonometric identity, the fundamental component of the current, $i_{z,1}$, can be decoupled into $i^{p}_{z,1}$ component, in phase with $v_{z,1}$ (the fundamental component of v_z), and into $i^{q}_{z,1}$ component, in quadrature with $v_{z,1}$. This can be mathematically expressed as

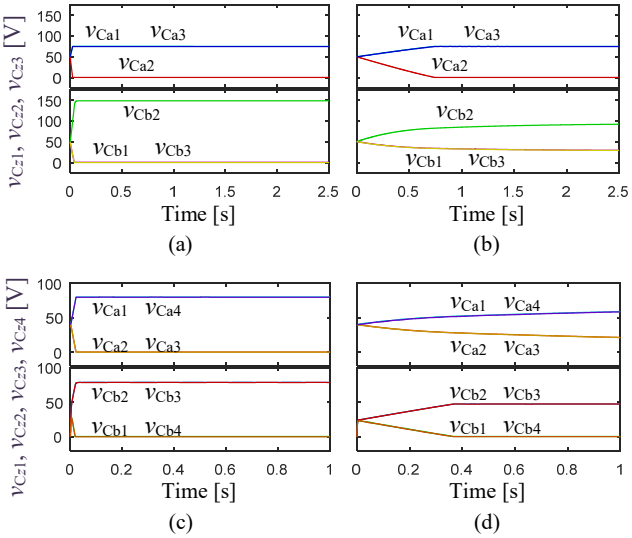


Fig. 4. Transient simulation results showing the natural unbalancing of the dc-link capacitor voltages on the proposed ML-DAB converters. (a) 4L-DAB results with α_{zk} = {15º, 45º, 75º} $\forall z$. (b) 4L-DAB results with α_{zk} = {15º, 37.8º, 75º} $\forall z$. (c) 5L-DAB results with α_{zk} = {11.3º, 33.8º, 56.3º, 78.8º} $\forall z$. (d) 5L-DAB results with α_{zk} = {10º, 26.4º, 45.6º, 80º} $\forall z$.

$$\begin{aligned} v_{z,1} &= V_{z,1}\cdot\sin(\theta_z) \\ i_{z,1} &= I_{z,1}\cdot\sin(\theta_z+\beta_z) = I_{z,1}\cdot\left[\cos(\beta_z)\sin(\theta_z)+\sin(\beta_z)\cos(\theta_z)\right] \\ &= I^{p}_{z,1}\cdot\sin(\theta_z)+I^{q}_{z,1}\cdot\cos(\theta_z) = i^{p}_{z,1}+i^{q}_{z,1}, \end{aligned} \tag{5}$$

where $I_{z,1}$ is the amplitude of $i_{z,1}$, β_z is the phase between $i_{z,1}$ and $v_{z,1}$, and $I^{p}_{z,1}$ and $I^{q}_{z,1}$ are the amplitudes of $i^{p}_{z,1}$ and $i^{q}_{z,1}$, respectively.

Currents $i^{p}_{z,1}$ and $i^{q}_{z,1}$, together with v_z, are plotted in Fig. 5. The shaded areas in Fig. 5 represent the charge injected into (positive sign) or drawn from (negative sign) the z-side inner

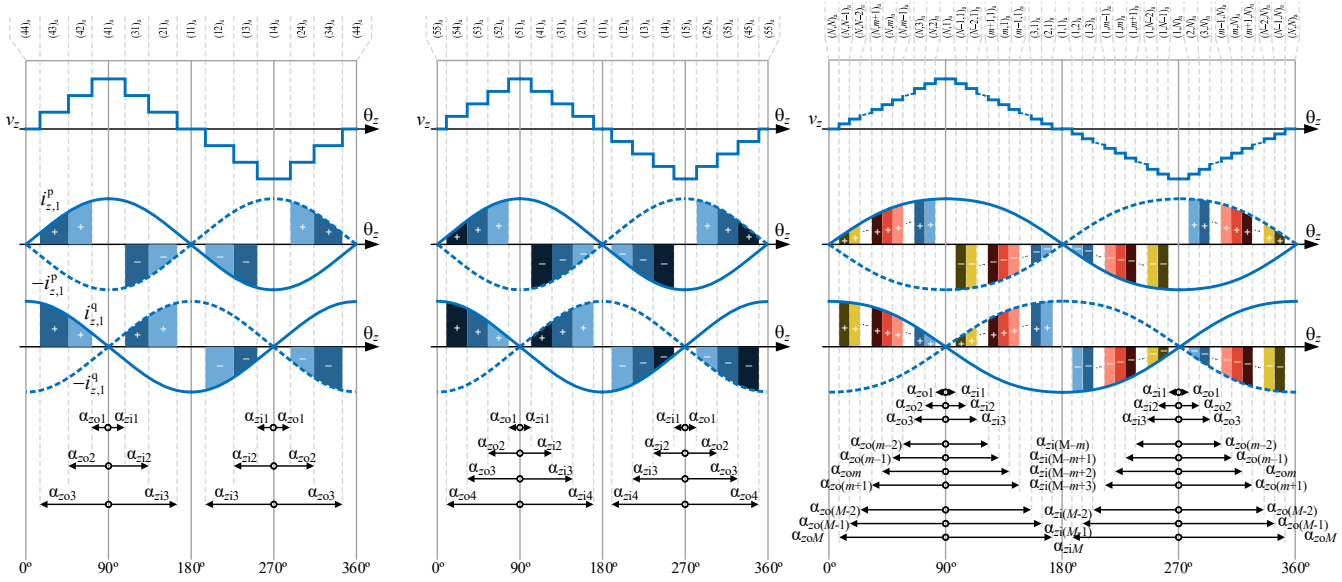


Fig. 5. Voltage v_z and the in-phase and in-quadrature components of i_z fundamental components ($i^{p}_{z,1}$ and $i^{q}_{z,1}$) for the proposed ML-DAB converters. The colored areas depict the charge injected into (+) or drawn from (–) inner dc-link points 2_z to M_z. (a) Four-level case. (b) Five-level

dc-link points (a different color for each dc-link point) of each ML-DAB case by currents $i^{p}_{z,1}$ and $i^{q}_{z,1}$. Looking at the 4L-DAB case (Fig. 5(a)), it can be seen that to keep a preexisting capacitor voltage balance, the sum of the light-blue colored areas must be zero and the sum of the mid-dark-blue colored areas must also be zero. It can be observed, however, that the sum of $i^{q}_{z,1}$ areas for each color is always zero, regardless of the values of the switching angles, thanks to v_z odd symmetry. Therefore, it is only necessary to cancel out the areas of $i^{p}_{z,1}$ for each color.

The same rationale applies to the 5L-DAB case (Fig. 5(b)) and, by extension, to the general *N*L-DAB case (Fig. 5(c)).

A. Operation principle

1) 4L-DAB case

Let us consider only half of the switching period on Fig. 5(a) due to the even symmetry of $i^{p}_{z,1}$ shaded areas. Then, the per-unit charge provided to inner dc-link points 2_z and 3_z is

$$\begin{aligned} q_{2z} &= \sin(\alpha_{zo2}) - \sin(\alpha_{zo1}) - (\sin(\alpha_{zi3}) - \sin(\alpha_{zi2})) \\ q_{3z} &= \sin(\alpha_{zo3}) - \sin(\alpha_{zo2}) - (\sin(\alpha_{zi2}) - \sin(\alpha_{zi1})), \end{aligned} \tag{6}$$

respectively. If (3) is assumed for simplicity, then $q_{2z} = -q_{3z}$. Moreover, in order to force a null charge provided by $i^{p}_{z,1}$ to the inner dc-link points within a switching cycle, $q_{2z} = -q_{3z} = 0$, which results in

$$2\cdot\sin(\alpha_{z2}) - \sin(\alpha_{z1}) - \sin(\alpha_{z3}) = 0. \tag{7}$$

One solution to meet (7) is to set the lowest and highest switching angles (α_{z1} and α_{z3}) as independent design variables and then obtain α_{z2} from

$$\sin(\alpha_{z2}) = \frac{1}{2}(\sin(\alpha_{z1}) + \sin(\alpha_{z3})). \tag{8}$$

2) 5L-DAB case

For the 5L-DAB case, the per-unit charge provided to inner dc-link points 2_z, 3_z, and 4_z is

$$\begin{aligned} q_{2z} &= \sin(\alpha_{zo2}) - \sin(\alpha_{zo1}) - (\sin(\alpha_{zi4}) - \sin(\alpha_{zi3})) \\ q_{3z} &= \sin(\alpha_{zo3}) - \sin(\alpha_{zo2}) - (\sin(\alpha_{zi3}) - \sin(\alpha_{zi2})) \\ q_{4z} &= \sin(\alpha_{zo4}) - \sin(\alpha_{zo3}) - (\sin(\alpha_{zi2}) - \sin(\alpha_{zi1})), \end{aligned} \tag{9}$$

respectively. Again, if (3) is assumed for simplicity, then $q_{3z} = 0$ (the charge provided to the dc-link middle point is inherently cancelled) and $q_{2z} = -q_{4z}$. Forcing $q_{2z} = -q_{4z} = 0$ results in

$$\sin(\alpha_{z2}) - \sin(\alpha_{z1}) - \sin(\alpha_{z4}) + \sin(\alpha_{z3}) = 0. \tag{10}$$

One solution to meet (10) is to set α_{z1} and α_{z4} as independent design variables and then obtain α_{z2} and α_{z3} from

$$\begin{aligned} \sin(\alpha_{z2}) &= \sin(\alpha_{z1}) + \Delta_{z1} \\ \sin(\alpha_{z3}) &= \sin(\alpha_{z4}) - \Delta_{z1}, \end{aligned} \tag{11}$$

where Δ_{z1} is a new independent design variable, which to meet (2), it must verify that

$$0 \le \Delta_{z1} \le \frac{\sin(\alpha_{z4}) - \sin(\alpha_{z1})}{2}. \tag{12}$$

3) General NL-DAB case

Considering the previous particular cases, and by observing Fig. 5(c), it is easy to infer the *N*-level expression for (6) and (9), which is

$$\begin{aligned} q_{mz} &= \sin(\alpha_{zom}) - \sin(\alpha_{zo(m-1)}) \\ &\quad -\left(\sin(\alpha_{zi(M-m+2)}) - \sin(\alpha_{zi(M-m+1)})\right) \\ &\quad m \in \{2,3,\ldots,M\}. \end{aligned} \tag{13}$$

Assuming (3), then

$$\begin{aligned} &q_{2z} = -q_{Mz}, \\ &q_{3z} = -q_{(M-1)z}, \\ &\vdots \\ &q_{\lfloor \frac{M}{2} \rfloor z} = -q_{\lceil \frac{M}{2}+2 \rceil z}, \\ &q_{\lfloor \frac{M}{2}+1 \rfloor z} = -q_{\lceil \frac{M}{2}+1 \rceil z} = \\ &\begin{cases} 0, & \text{odd } N \\ 2\cdot\sin\left(\alpha_{z\left(\frac{M+1}{2}\right)}\right) - \sin\left(\alpha_{z\left(\frac{M+3}{2}\right)}\right) - \sin\left(\alpha_{z\left(\frac{M-1}{2}\right)}\right), & \text{even } N. \end{cases} \end{aligned} \tag{14}$$

In order to guarantee a null charge provided to the inner dc-link points by $i^{p}_{z,1}$,

$$q_{\lfloor mz \rfloor} = -q_{\lceil M-m+2 \rceil} = 0, \quad m \in \left\{2,3,\ldots,M/2+1\right\}. \tag{15}$$

Following the same strategy of the 4L and 5L cases, a solution for N > 3 to (15) is to force

$$\begin{cases} \sin(\alpha_{z(r+1)}) = \sin(\alpha_{zr}) + \Delta_{zr} \\ \sin(\alpha_{z(M-r)}) = \sin(\alpha_{z(M-r+1)}) - \Delta_{zr} \end{cases} r \in \left\{1,2,\ldots,\left\lfloor \frac{M}{2} - 1 \right\rfloor\right\}, N > 4 \tag{16}$$

$$\sin\left(\alpha_{z\left(\frac{M+1}{2}\right)}\right) = \frac{1}{2}\left(\sin\left(\alpha_{z\left(\frac{M-1}{2}\right)}\right) + \sin\left(\alpha_{z\left(\frac{M+3}{2}\right)}\right)\right), \text{ even } N, N > 3,$$

where

$$\begin{aligned} &\Delta_{zr} \ge 0, \forall r \\ &\sum_r \Delta_{zr} \le \frac{1}{2}(\sin(\alpha_{zM}) - \sin(\alpha_{z1})). \end{aligned} \tag{17}$$

However, due to the presence of converter non-idealities and i_z harmonics, verifying (15) is not enough to maintain a preexisting capacitor voltage balance. This fact can be verified in the simulation results of Fig. 4(b) for the 4L-DAB and Fig. 4(d) for the 5L-DAB, where the capacitor voltages get unbalanced even when employing a set of switching angles verifying (8) and (11), respectively. Nevertheless, it is worth noticing that the unbalance is greatly lessened compared to employing arbitrary switching angle values (Fig. 4(a) and (c)).

Consequently, a control action is needed to correct any

capacitor voltage unbalance arising due to the reasons explained above.

B. Control schemes

Fig. 6(a) and Fig. 6(b) present the proposed control schemes for the 4L-DAB and 5L-DAB, respectively. The 4L-DAB control scheme is an enhanced version of the control scheme presented in [22]. Fig. 6(c) shows the generalized control scheme.

The inputs of these control schemes are the dc-link unbalance variables y_{zm} (grouped in vector $\mathbf{y}_z = (y_{z2}, \ldots, y_{zm}, \ldots, y_{zM})$ in Fig. 6(c)), which are equal to

$$y_{zm} = \frac{\sum_{k=1}^{m-1} v_{Czk}}{m-1} - \frac{\sum_{k=m}^{M} v_{Czk}}{M+1-m}, \tag{18}$$

where v_{Czk} are the dc-link capacitor voltages. Variables y^*_{zm} (grouped in vector $\mathbf{y}^*_z$) indicate the command values of the unbalance variables, which are typically equal to zero. The difference between y^*_{zm} and y_{zm} defines error variables e_{zm} (grouped in vector $\mathbf{e}_z$).

In the general case, an $e_{zm} > 0$ means that the average value of $\{v_{Cz1}, \ldots, v_{Cz(m-1)}\}$ is below its desired value and/or that the average value of $\{v_{Czm}, \ldots, v_{CzM}\}$ is above its desired value. In order to correct such error, charge must be injected into inner dc-link point m_z such that the capacitors below it are charged and the capacitors above it are discharged. This can be accomplished by breaking the half-wave symmetry imposed by (3) modifying the appropriate inner and outer switching angles, as discussed below.

Without loss of generality, let us assume that power is transferred from side a to side b. Thus, Fig. 5 waveforms correspond to side a. In b-side waveforms, the current has opposite sign since $i_b = -i_a$. In the 4L-DAB (Fig. 5(a)), if $e_{a2} > 0$, the required control action is to increase switching angle pair $\{\alpha_{ao2},\alpha_{ai2}\}$ and decrease $\{\alpha_{ao1},\alpha_{ai3}\}$, such that charge is injected into inner dc-link point 2_a with $i^{P}_{a,1}$. Extending this analysis for $e_{zm} \neq 0\ \forall z,m$ on the 3L-DAB [21], 4L-DAB, and 5L-DAB (Fig. 5(b)) cases, allows inferring the required control actions for the generalized NL-DAB case.

The results of such analysis are shown in Table I, which indicates which switching angle pairs should be increased and decreased in order to correct any $e_{am} \neq 0$ when power is transferred form side a to side b. The required b-side-switching-angles control action when $\text{sign}(e_{am}) = \text{sign}(e_{bm})$ is opposite to side a, since $i_b = -i_a$. When power is transferred in the opposite direction, side a becomes side b and vice versa.

The described control actions are determined by control variables u_{zm}, obtained after processing e_{zm} variables with compensators $G_{zm}(s)$, grouped in matrix $\mathbf{G}_z(s) = \text{diag}(G_{z1}(s), \ldots, G_{zM}(s))$ in Fig. 6(c). Variables u_{zm} modify the switching angles according to Table I rules and in a per-unit basis from the value of initial switching angles α_{zk}, as seen in the control schemes of Fig. 6.

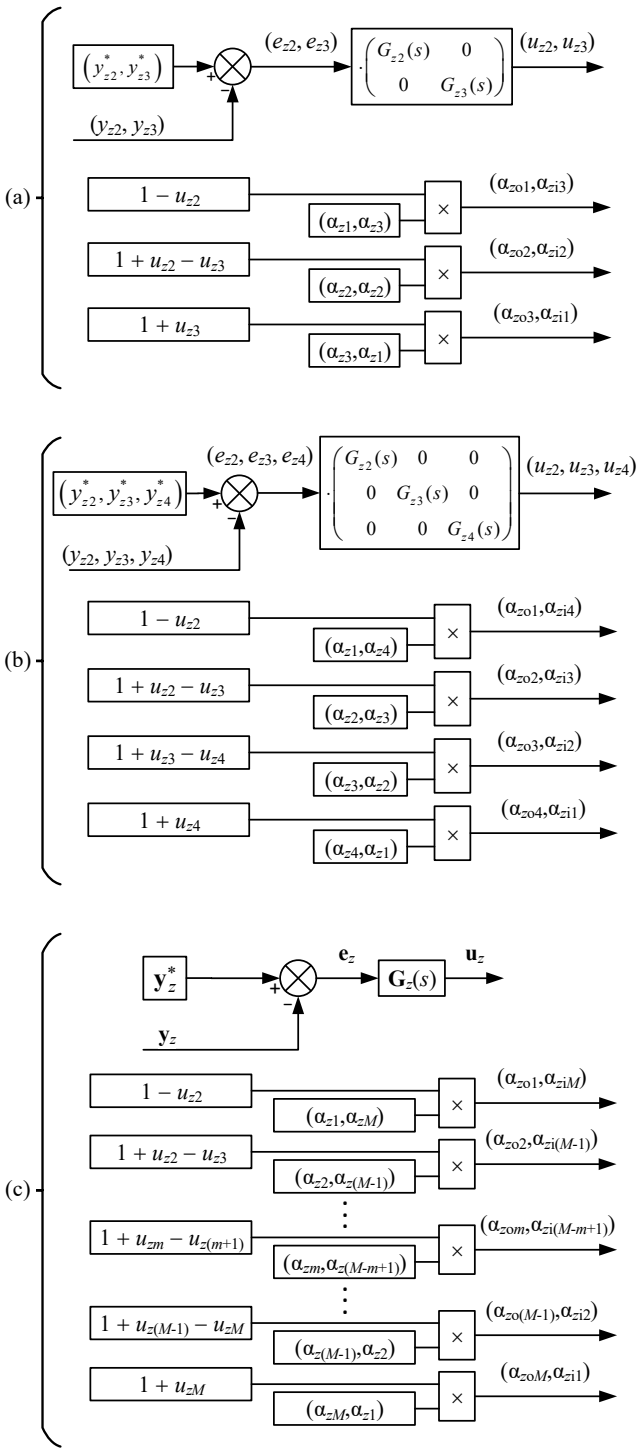


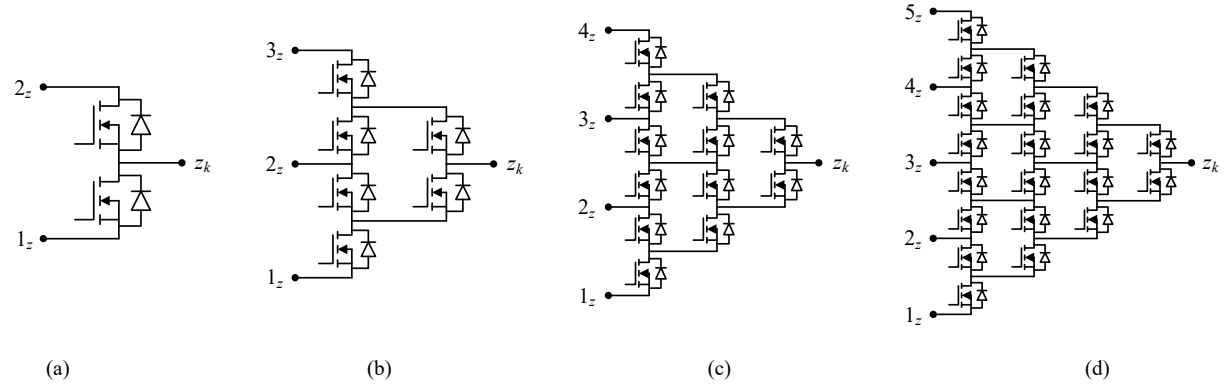
Fig. 6. Control schemes for the *z*-side capacitor voltage balancing of the proposed ML-DAB dc-dc converters. (a) Four-level case. (b) Five-level case. (c) Generalized *N*-level case.

The $G_{zm}(s)$ compensator transfer function is a proportional-integral controller, defined in its standard form as

$$G_{zm}(s) = k_{P,zm}\left(1 + \frac{1}{T_{I,zm} \cdot s}\right), \tag{19}$$

TABLE I
REQUIRED a-SIDE CAPACITOR VOLTAGE BALANCING CONTROL ACTIONS FOR THE *N*L-DAB (POWER TRANSFERRED FROM a-SIDE TO b-SIDE)

m	e_{am}	$\{\alpha_{ao1}, \alpha_{aiM}\}$	$\{\alpha_{ao2}, \alpha_{ai(M-1)}\}$	$\{\alpha_{ao3}, \alpha_{ai(M-2)}\}$	…	$\{\alpha_{ao(m-2)}, \alpha_{ai(M-m+3)}\}$	$\{\alpha_{ao(m-1)}, \alpha_{ai(M-m+2)}\}$	$\{\alpha_{aom}, \alpha_{ai(M-m+1)}\}$	$\{\alpha_{ao(m+1)}, \alpha_{ai(M-m)}\}$	…	$\{\alpha_{ao(M-2)}, \alpha_{ai3}\}$	$\{\alpha_{ao(M-1)}, \alpha_{ai2}\}$	$\{\alpha_{aoM}, \alpha_{ai1}\}$
2	>0 / <0	↓ / ↑	↑ / ↓										
3	>0 / <0		↓ / ↑	↑ / ↓									
⋮	⋮				⋱								
$m-1$	>0 / <0					↓ / ↑	↑ / ↓						
m	>0 / <0						↓ / ↑	↑ / ↓					
$m+1$	>0 / <0							↓ / ↑	↑ / ↓				
⋮	⋮									⋱			
$M-1$	>0 / <0										↓ / ↑	↑ / ↓	
M	>0 / <0											↓ / ↑	↑ / ↓



(a) (b) (c) (d)

Fig. 7. *N*L-DAB switching leg topologies employed in the experimental tests. (a) Conventional 2L topology. (b) 3L active-NPC topology. (c) 4L multilevel active clamped (MAC) topology. (d) 5L MAC topology.

where $k_{P,zm}$ is the general gain of the controller and $T_{I,zm}$ is the integrator reset time. When power is transferred from side a to side b, then $k_{P,am} > 0\ \forall m$. Regarding side b, since $i_b = -i_a$, $k_{P,bm} < 0\ \forall m$. When power is transferred from side b to side a, the sign of $k_{P,zm}$ changes $\forall z,m$.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental test have been carried out to prove the effectiveness of the proposed modulation schemes and capacitor voltage balancing controls on the 4L-DAB, 5L-DAB, and also on three ML-DAB converters with an asymmetric number of levels; i.e., with N_a levels on side a and N_b levels on side b (an N_aL-N_bL-DAB converter). The performance of the proposed ML-DAB converters is analyzed, by comparing the converter losses and the efficiency of the 5L-DAB with the 2L-DAB.

The analyzed asymmetric converters are the 3L-2L-DAB, the 4L-2L-DAB, and the 4L-3L-DAB. The 3L and 4L sides of the asymmetric converters employ the topology, modulation, and capacitor voltage balancing control scheme of the symmetric 3L-DAB [21] and 4L-DAB converters, respectively. The 2L sides employ the conventional full-bridged 2L-DAB converter topology.

A MATLAB-Simulink lossless model of the converters is used to perform the simulations. For the experimental tests, the converter legs are implemented with the topologies shown in Fig. 7. The 4L and 5L switching legs are implemented employing the MAC topology and operated according to [23]. The MAC topology allows guaranteeing that each device blocking voltage is equal to $V_Z/(N-1)$ (assuming balanced dc-link capacitor voltages). The control and modulation is implemented using dSpace processor board DS1006 and three synchronized dSpace digital waveform output boards DS5101 (each contains an FPGA). Fig. 8 shows the 4L-DAB experimental setup.

On both the symmetric and asymmetric converters, the switching angle pair $\{\alpha_{z1},\alpha_{zM}\}$ on the 3L, 4L, and 5L sides is set arbitrarily. On the 4L sides, switching angle α_{z2} is then defined with (8), while on the 5L sides, switching angle pair $\{\alpha_{z2},\alpha_{z3}\}$ is defined with (11) and $\Delta_{z1} = 1/3\cdot(\sin(\alpha_{z4}) -$

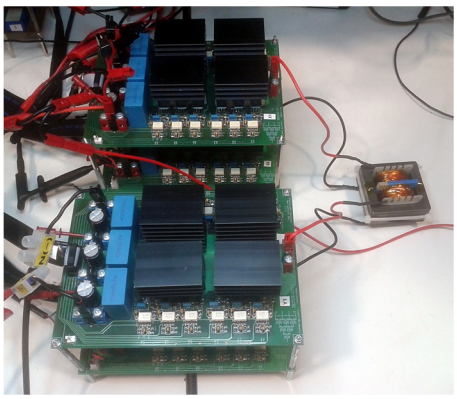


Fig. 8. 4L-DAB experimental setup. Components: FDPF3860T MOSFETs, C_z = 103.4 µF, n = 1, L = 300 µH, transformer magnetizing inductance L_m = 12 mH, HCPL-316J gate drivers, and compact and internal gate driver power supply circuits as described in [24].

TABLE II
SIMULATION AND EXPERIMENTAL TESTS PARAMETER VALUES

Converter	4L-DAB		5L-DAB		3L-2L-DAB	4L-2L-DAB		4L-3L-DAB	
Fig.	9	13	10	14	11(I) 15(I)	11(II)	15(II)	11(III)	15(III)
d	0.89		1.25		1	0.67		0.67	
$\{V_A,V_B\}$ [V]	{180,160}		{160,200}		{100,100}	{180,120}		{180,120}	
f_s [kHz]	10		20		25	25		25	
φ [º]	25		15	60	20	20		60	
$\{C_a,C_b\}$ [μF]	{100,100}		{100,100}		{100,35}	{100,35}		{100,100}	
R_B (sim.) [Ω]	120		271	276	151.9	170.3		46.3	
R_B (exp.) [Ω]	132		-	-	185	181.5		51.9	
$K_{P,zm}$ $\forall z,m$	0.6		0.4	0.3	0.3	0.3		0.3	
$T_{I,zm}$ $\forall z,m$ [ms]	0		20		20	20		20	
K_{PS}	7500		7500	20000	10000	10000		10000	

$\sin(\alpha_{z1})$). On the 2L sides, only one switching angle exists α_z, which defines the dwell time ($2\cdot\alpha_z/(360\cdot f_s)$) where v_z remains at V_Z or $-V_Z$, and it is set arbitrarily. The switching angle values computed with (8) and (11) help lessening the capacitor voltage balancing control effort on the dc-links of the 4L and 5L sides, respectively.

In all simulations and experiments, a dc voltage source with a 10 mΩ series resistance is connected across the a-side dc-link, while a resistive load (R_B) is connected across the b-side dc-link. The converters can operate with any type of load, as in a conventional 2L-DAB dc-dc converter, but a purely resistive load is selected for simplicity. It is necessary to set a different value of R_B in the simulations ($R_{B,sim}$) compared to the value used in the experiments ($R_{B,exp}$), as specified in Table II, to achieve the same value of V_A, V_B and φ in both cases, since a lossless simulation model is used. Forcing the same values of V_A, V_B and φ is interesting since it leads to the same voltage and current waveform shapes, and it is therefore easy to validate the good performance of the system in both simulation and experiments. In the tests to obtain the transient results, the output voltage V_B is controlled by compensator $K_{PS}\cdot(s + 100\pi)/(s\cdot(s + 5000\pi))$, which modifies φ accordingly.

The common parameters on all simulations and experimental tests are $n = 1$ and $L = 300$ μH, with reference to Fig. 2. Table II shows the remaining parameter values. The capacitor-voltage-balancing-control compensator parameter values shown in Table II have been tuned through simulations and experiments to achieve an acceptable control performance while guaranteeing stability.

A. Steady-State Results

Fig. 9, Fig. 10, and Fig. 11 present the steady-state results for the simulation and experimental tests performed with the proposed converters. It can be observed that on all cases both dc-links have capacitor voltage balance, since v_a and v_b present voltage steps of equal amplitudes. The slight differences between the simulation and experimental results in Fig. 11 are due to the experimental prototypes non-idealities.

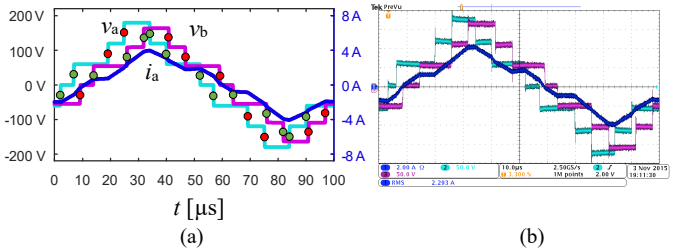


Fig. 9. Steady-state results of the proposed 4L-DAB dc-dc converter. Conditions: $\{\alpha_{z1},\alpha_{z2},\alpha_{z3}\}$ = {15º, 37.8º, 75º} $\forall z$. (a) Simulation results. (b) Experimental results.

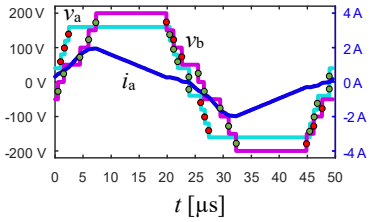


Fig. 10. Simulation steady-state results of the proposed 5L-DAB dc-dc converter. Conditions: $\{\alpha_{a1},\alpha_{a2},\alpha_{a3},\alpha_{a4}\}$ = {72º, 75.2º, 79.3º, 87º}, $\{\alpha_{b1},\alpha_{b2},\alpha_{b3},\alpha_{b4}\}$ = {45º, 53.5º, 64.4º, 87º}.

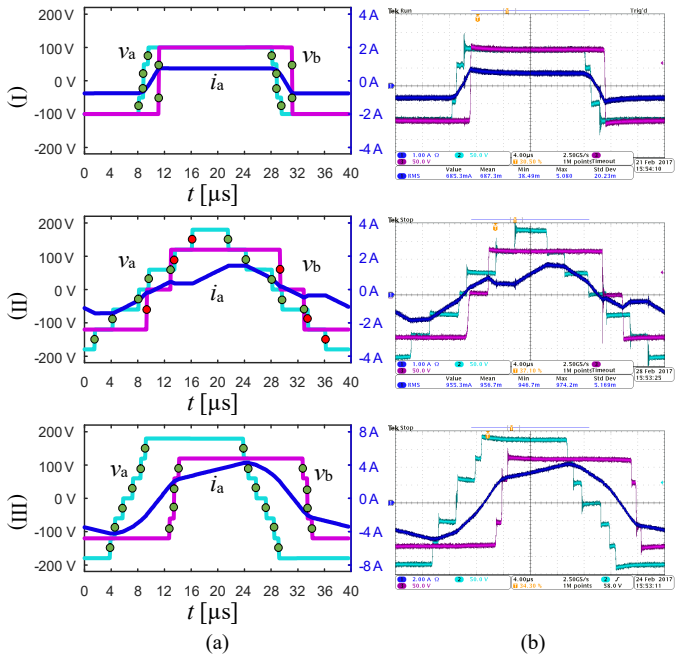


Fig. 11. Steady-state results of the proposed ML-DAB dc-dc converters with an asymmetric number of levels. (a) Simulation results. (b) Experimental results.
(I) 3L-2L-DAB. Conditions: $\{\alpha_{a1},\alpha_{a2}\}$ = {83.7º,90º}, α_b = 90º.
(II) 4L-2L-DAB. Conditions: $\{\alpha_{a1},\alpha_{a2},\alpha_{a3}\}$ = {24.8º, 45.1º, 86º}, α_b = 73.4º.
(III) 4L-3L-DAB. Conditions: $\{\alpha_{a1},\alpha_{a2},\alpha_{a3}\}$ = {74.4º, 76.1º, 78º}, $\{\alpha_{b1},\alpha_{b2}\}$ = {83.7º, 90º}.

The red and green dots indicate the type of switching transition; i.e., green dots denote soft-switching transition, where losses occur during the turn-off of the MOSFETs while ZVS occurs during the MOSFETs turn-on transitions, and red dots denote hard-switching transitions, where losses occur during the turn-on of the MOSFET, increased by the diode reverse recovery current, and also on the diode turn-off, while ZVS occurs during the MOSFET turn-off.

TABLE III
SWITCHING LOSS COEFFICIENTS

		FDPF3860T @ V_{DS} = 50 V			STP13NM60N @ V_{DS} = 200 V		
		a	b	c	a	b	c
Switch	$E_{on,1d}$	0	0.477	0.581	2.915	36.3	120.1
	$E_{on,2d}$	0	0.503	0.828	-	-	-
	$E_{on,3d}$	0.041	-0.093	2.984	-	-	-
	$E_{on,4d}$	0.060	-0.337	4.034	-	-	-
	$E_{off,1d}$	0.046	-0.192	0.398	0.380	0.163	-0.088
	$E_{off,2d}$	0.040	-0.173	0.230	-	-	-
	$E_{off,3d}$	0.033	-0.136	-0.022	-	-	-
	$E_{off,4d}$	0.028	-0.171	0.153	-	-	-
Diode	$E_{off,1d}$	0	0.131	2.366	0.391	16.28	30.85
	$E_{off,2d}$	0	0.145	2.985	-	-	-
	$E_{off,3d}$	0	0.158	3.603	-	-	-
	$E_{off,4d}$	0	0.172	4.222	-	-	-

Fig. 12 compares the semiconductor power losses (P_{loss}) and efficiency (η) of a 2L-DAB operated with 600 V MOSFETs (STP13NM60N, on resistance $R_{DS,on}$ = 280 mΩ) and a 5L-DAB operated with 100 V MOSFETs (FDPF3860T, $R_{DS,on}$ = 30 mΩ), over d = {1, 1.25, 1.5}, and for a transferred power range of [0 P_{max}], where

$$P_{max} = \frac{V_A V_B}{8 n f_s L}. \quad (20)$$

The 2L- and 5L-DAB switching legs are implemented with the topologies shown in Fig. 7(a) and (d), respectively. The modulation parameters for both converters are set such that the conventional PSM is employed; i.e., the switching legs synthesize pure square-wave voltages on each transformer side.

This study follows the same procedure of the study performed for the comparison of the 2L-DAB and 3L-DAB in [21]; i.e., the comparison is performed combining simulation and experimental data. The system is simulated in MATLAB-Simulink. Conduction losses are calculated from

$$P_{cond} = \sum_{j=1}^{J} I_{swj,rms}^2 \cdot R_{DSon,swj}, \quad (21)$$

where $I_{swj,rms}$ and $R_{DSon,swj}$ are the converter j-th device rms current and on resistance, respectively, and J is the total number of semiconductor devices within the converter. Switching losses are calculated from

$$P_{sw} = 10^{-6} \cdot f_s \cdot \sum_{j=1}^{J} \sum_{p} E_{swj,p}, \quad (22)$$

where

$$E_{swj,p} = a \cdot I_{swj,p}^2 + b \cdot |I_{swj,p}| + c \quad [\mu J] \quad (23)$$

is the converter j-th device switching energy loss in transition p, $I_{swj,p}$ is the current being switched by the converter j-th device in transition p, and coefficients a, b, and c depend on the device, the type of switching transition, and the value of the blocking voltage V_{DS}. A suitable set of coefficient values for each different case has been obtained from the switch and diode energy loss during switching transitions experimentally measured using a double pulse board at different blocking voltages V_{DS}, over the full current range up to 16 A, and with a gate resistance of 6.6 Ω for FDPF3860T and 18.7 Ω for STP13NM60N. The gate resistance values are selected such that both switches perform turn-on switching transitions with similar di/dt. Table III presents the value of these coefficients for the V_{DS} value corresponding to d = 1, that together with (23), approximate the experimentally measured losses (in both the switch and diode, at turn-on (E_{on}) and turn-off (E_{off}) transitions, and involving one, two, three, or four diodes ("1d", "2d" , "3d" , "4d")) with a coefficient of determination (R^2) higher than 97.7 % for the switch and higher than 55 % for the diode. Similar sets of coefficient values have been obtained for V_{DS} = {40, 44.5, 50, 55.5, 60} V for FDPF3860T and V_{DS} = {160, 178, 200, 222, 240} V for STP13NM60N. For currents below 2 A, a simple linear regression has been applied. Both P_{cond} and P_{sw} are computed within a switching cycle.

From Fig. 12 it can be observed that in power ranges 0-450 W and 0-665 W for d = 1.25 and d = 1.5, respectively, the converters efficiency decreases, especially in the 2L-DAB, since all or most switching transitions are of hard-switching

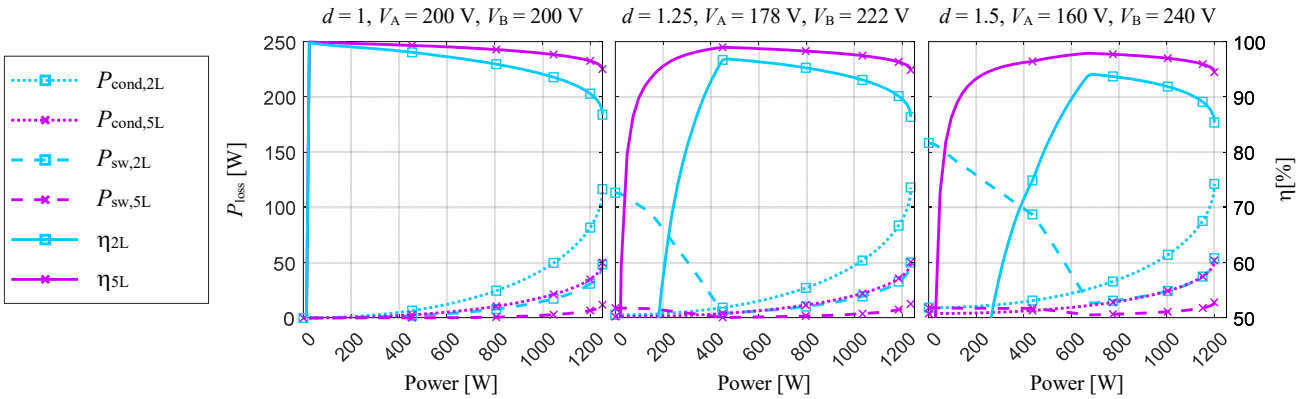


Fig. 12. Comparison of losses and efficiency of a 2L-DAB and a 5L-DAB operated with switching angles α_z = 90° $\forall z$ for the 2L-DAB and α_{zk} = 90° $\forall z,k$ for the 5L-DAB. Conditions: f_s = 100 kHz, L = 40 μH.

type. In the high-power range, terms $I^2_{swj,rms}$, $I^2_{swj,p}$ and $|I_{swj,p}|$ in (21) and (23) increase exponentially with the transferred power [21], causing a decrease of the converters efficiency. Two measures can be taken to maximize the converter efficiency: set its nominal power in the mid-power range or employ alternative modulations to the PSM offering better performance. Nevertheless, both conduction and switching losses are lower in the 5L-DAB case, leading to a higher efficiency in the full power range, thanks to the inherent ML-topology benefits stated in Section I.

B. Transient Results

Fig. 13, Fig. 14, and Fig. 15 present the transient results to analyze the performance and suitability of the proposed control schemes.

In the 4L-DAB (Fig. 13) and 5L-DAB (Fig. 14), an initial unbalance is forced by disabling the b-side capacitor voltage balancing control and loading the b-side capacitors with different resistance values. Once the b-side balancing control is enabled, the capacitor voltage balance is quickly recovered in both converters.

In the asymmetric ML-DAB converters (Fig. 15), a deliberate unbalance is forced (starting from a balanced state) in the 3L- and 4L-side capacitor voltages. This is accomplished by assigning to y^*_{zm} variables a pulsed signal, going from zero to a plateau value ($y^*_{zm,plat}$) and back to zero, with ramped transitions (±3 V/ms). As seen in Fig. 15, the capacitor voltage balancing controls of the three converters are able to modify the capacitor voltages according to the reference values.

The transient results obtained in the simulation and experimental tests are in close agreement in each of the five tested converters.

It is worth noticing that the interaction among the capacitor voltage balancing controls and the output voltage control does not produce any kind of system instability.

V. Conclusion

The present paper proposes a generalized solution to overcome the main problem of ML-DAB converters built upon NPC switching legs in full-bridge disposition: the dc-link-capacitor-voltages unbalancing. This solution comprises a modulation, which allows avoiding that the transformer-current fundamental component affects the capacitor voltage unbalance, and a control scheme, whose duty is to finely adjust the modulation parameter values to counteract the capacitor voltage unbalancing caused by the rest of transformer-current harmonic components and by the converter non-idealities. This solution is given in a generalized form and is valid for ML-DAB converters with any number of voltage levels on either side of the converter. The experimental results demonstrate the suitability of the presented solution, since capacitor voltage balancing is achieved over a wide range of operating conditions. Moreover, the superior performance of the ML-DAB converters compared to the conventional 2L-DAB converter is demonstrated, through a study showing that the efficiency of the 5L-DAB is greater than the efficiency of the 2L-DAB over the whole power range and a wide d range.

The presented modulation features a total of $4N - 3$ DoF (φ, α_{zik}, α_{zok} $\forall z,k$), from which $N + 1$ (for even N) or $N + 2$ (for odd N) DoF (φ, α_{z1}, α_{zM}, Δ_{zr} $\forall z,r$) are employed to control the

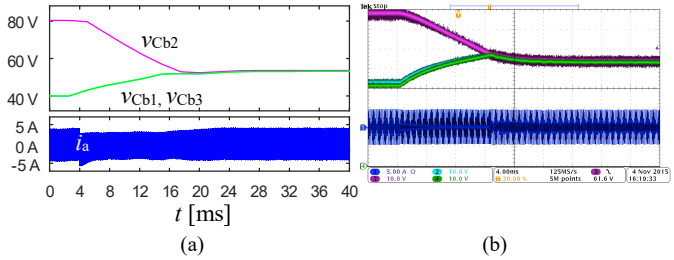


Fig. 13. Transient results of the proposed 4L-DAB dc-dc converter. Conditions: $\{\alpha_{z1},\alpha_{z2},\alpha_{z3}\} = \{15^o, 37.8^o, 75^o\}$ $\forall z$ and b-side capacitor voltage balancing control enabled at t = 4 ms. (a) Simulation results. (b) Experimental results.

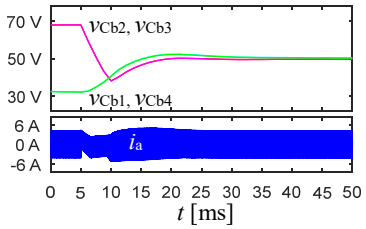


Fig. 14. Simulation transient results of the proposed 5L-DAB dc-dc converter. Conditions: $\{\alpha_{z1},\alpha_{z2},\alpha_{z3},\alpha_{z4}\} = \{10^o, 24.7^o, 41.5^o, 65^o\}$ $\forall z$ and b-side capacitor voltage balancing control enabled at t = 5 ms.

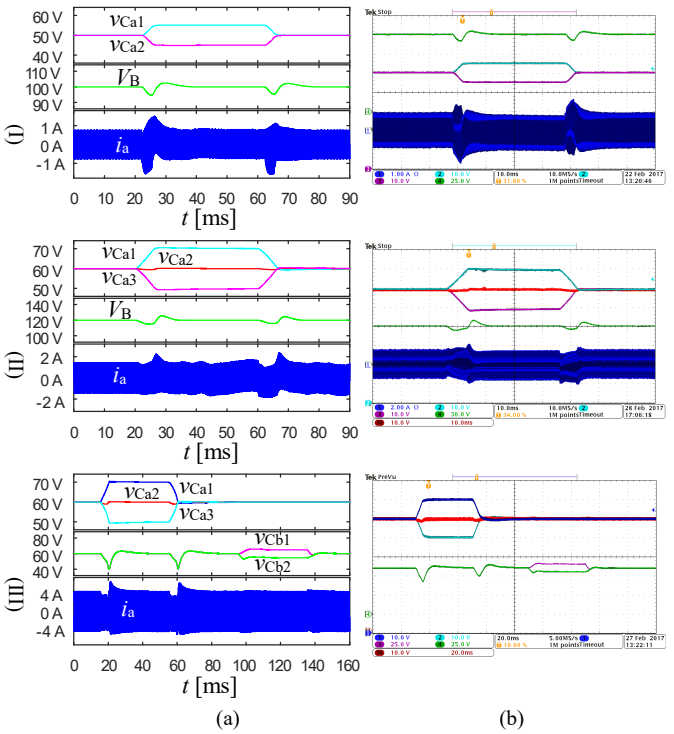


Fig. 15. Transient results of the proposed ML-DAB dc-dc converters with an asymmetric number of levels. Steady-state switching angles are the same of Fig. 11. (a) Simulation results. (b) Experimental results.
(I) 3L-2L-DAB. Conditions: $y^*_{a2,plat}$ = 10 V.
(II) 4L-2L-DAB. Conditions: $\{y^*_{a2,plat}, y^*_{a3,plat}\} = \{15,15\}$ V.
(III) 4L-3L-DAB. Conditions: $\{y^*_{a2,plat}, y^*_{a3,plat}\} = \{15,15\}$ V, $y^*_{b2,plat}$ = 10 V.

power flow between both converter sides and, eventually, optimize the converter performance (as in [21]), while $3N - 4$ (for even N) or $3N - 5$ (for odd N) DoF are employed for the capacitor voltage balancing. Therefore, each time the number of levels is increased to the next odd number, two more DoF are available to potentially optimize the converter performance and control the power flow.

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