MACROPOROUS SILICON FOR HIGH-CAPACITANCE DEVICES USING METAL ELECTRODES.

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1. SUMMARY

A novel technique for high capacitance device fabrication is presented in this paper. Macroporous silicon has been suggested for several applications, one of which is using the 3-D structure to create a high surface-to-volume ratio material for electrostatic capacitors. By the electrochemical etching of silicon is possible to obtain such structures. The devices are further enhanced by using a metal electrode, lowering the series resistance. Several 4 µm pitch, with 3 µm pore diameter devices have been fabricated and tested for different dielectric thicknesses. Up to 110 nF/mm^2 has been achieved with about 1 Ω series resistance.

2. INTRODUCTION

Current trends in device design have passive components integrated into monolithic integrated circuits (IC) as much as possible for the clear benefits in cost savings, performance enhancement, board density, reliability and others. Applications of integrated capacitors include RF, timing, A/D conversion, and more recently for cd-cd conversion and energy-storage where batteries are unpractical. Ultrahigh capacitance devices solve the dilemma for the integration of energy storage elements and minimal space requirements. One of the most interesting applications are as decoupling capacitors (decap). Power requirements of high-speed digital circuitry impose severe strains in power networks, where high current spikes can cause EMI noise and voltage dips. To ensure power quality in logic circuitry, decaps need to be placed near each IC; thus a large portion of the board is devoted to power conditioning.

Research on ultrahigh capacitance devices is a very active topic. From the various techniques reported, the use of macroporous silicon (MPS) is a relatively recent development. First appearance of porous silicon for capacitance in literature was in 1978, but it was not until Lehmann's work in 1996[1] that macroporous silicon was actually used for a capacitor. After a gap in research, it was not until 2000 that MPS was again proposed for RF applications[2]. Some more time passed before MPS was finally reported for high-density energy storage[3].

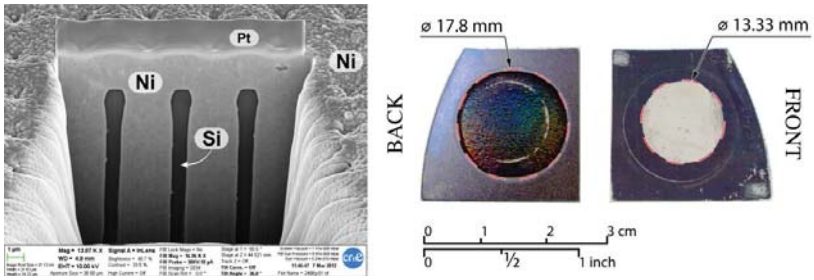

Fig. 1. Fabricated capacitor sample using MPS, the MPS etched area is clearly visible in the sample backside. As can be seen the nickel filled area is smaller than the total achievable area. The SEM micrograph shows the pores filled with nickel, of high quality.

Several techniques are available for the fabrication of macroporous silicon, as well as different methods for the construction of the capacitive structures. This paper deals specifically with electrochemically etched (EE) macroporous silicon, where high aspect ratio micron-scale deep pores are etched on bulk silicon[4]. EE silicon has several advantages over other fabrication techniques as well as being CMOS compatible. Unfortunately one of the disadvantages of devices based on semiconductors, and in particular EE silicon, is the low conductance of the materials. This is especially aggravating for nano-scale deep-trench devices, where current path cross-section is very small, and length is large. Thus these devices all suffer from large equivalent series resistance (ESR) and can only perform well at very low frequencies.

In this paper we report the fabrication of high-density macroporosus silicon capacitors by EE, and enhanced by using metal electrodepositon to build at least one of the electrodes. Using a metal electrode helps reducing the ESR considerably, thus being able to achieve better operating frequencies.

3. Fabrication

The capacitor samples were prepared from 4 micrometre pitch, square lattice EE macroporous silicon. Starting from a low doped ⟨100⟩ silicon substrate, pores are formed by photon assisted EE in hydrofluoric acid, using the method described by Lehmann. The square lattice is defined using a standard photolithography method where the pore growth sites are transferred to a 4" silicon wafer. Smaller samples of about 1"×1" are then cleaved from the prepared wafer and etched on our in-house setup. The structure used for the samples here presented consists of straight pores of 3 µm in diameter and 240 µm long. Once the macroporous silicon is obtained, the sample is prepared for the pore filling with nickel. This is done by opening the backside of the MPS sample using a KOH etching. Once the pores are reached, a porous membrane is formed, which is then filled with nickel to form the second capacitor electrode, the first one being the MPS structure itself. The metal filling is done using a low-temperature, industry standard, process of electrodeposition. The obtained samples and fill results can be seen in Fig. 1. Previous to the metal filling, to increase the conductivity of the semiconductor electrode, a phosphorous diffusion is done. Afterwards, the insulating dielectric layer is thermally grown by silicon oxidation. Several SiO_2 layer thicknesses were tried, ranging from 90 nm down to 15 nm. Once the insulator is in place, the MPS can be filled. The area and depth of the nickel fill is smaller than the maximum possible, this is due to the fact that deeper in the pores, the oxide is of less quality, and the MPS is rougher towards the edges. Nevertheless, the increase in effective area over a plane capacitor is estimated to be 83 times larger.

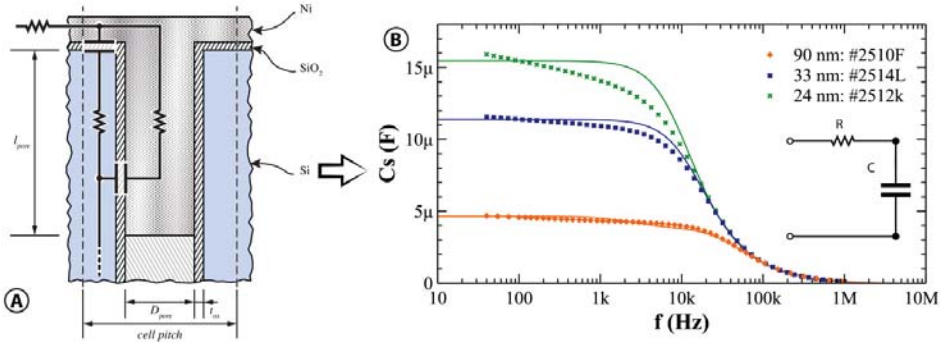

Fig. 2. (a) Cross section schematic view of a single pore of the MPS capacitor. The different circuit elements are superimposed. This model reduces to the simpler one shown in (b) where its response is compared against measurements for the 3 sample devices.

4. Characterization and Modelling

Given that the MPS consists of identical pores, we can extract a model for the capacitance of a single pore. This model is seen in Fig. 2(a): a plane capacitor for the remaining top side of the sample and a cylindrical capacitor for the pore. The devices fabricated were characterized with an Agilent 4992A impedance analyser up to 1 MHz. A simplified electrical model was fitted against the data showing a very good match, as shown in Fig. 2(b). Thus the more complex model can be simplified to a single capacitance with ESR. One point to note is that the thinnest oxide used was 24 nm as for 15 nm samples leakage was too large. Oxide breakdown was estimated to be 8.3 MV/cm, and ESR varied from 1.08 Ω to 1.12 Ω. Thanks to the good ESR, these devices are able to operate within nominal values up to 10 kHz.

5. Conclusion

In this paper we report the fabrication of high-performance, high-density capacitors based on MPS and metal electroplating. For the best device reported, a specific capacitance C_{sp} of 110 nF/mm^2 is achieved. Further work to obtain better C_{sp} will be done in optimizing the oxide and using pore close packing, as well as reducing overall feature dimensions. Applications for these devices include IC decoupling and dc-dc converters.

References

1. Lehmann, V. *et al.* A novel capacitor technology based on porous silicon. *Thin Solid Films* **276,** 138–142 (1996).
2. Roozeboom, F., Elfrink, R., Verhoeven, J., van den Meerakher, J. & Holthuysen, F. High-value MOS capacitor arrays in ultradeep trenches in silicon. *Microelectron. Eng.* **53,** 581–584 (2000).
3. Sancho, A., Arizti, F. & Gracia, F. J. Porous silicon for the development of capacitive microstructures. *Microelectron. Eng.* **86,** 2144–2148 (2009).
4. Lehmann, V. The Physics of Macropore Formation in Low Doped n-Type Silicon. *J. Electrochem. Soc.* **140,** 2836 (1993).