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Master Degree in Electronics Systems Engineering

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Master's Thesis

"VCO-based ADCs Design Techniques for Communication Systems"

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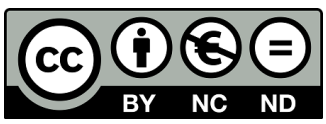

SUMMARY

This work presents a novel technique to implement voltage-controlled oscillator based continuous-time Delta-Sigma analog-to-digital converters (VCO-based CT-$\Delta\Sigma$ ADCs) in closed-loop configuration. Over the past years there has been an upward trend in the use of these type of converters for instrumentation, audio and communication applications. The reason is that they are mostly digital and thus benefit from advances in deep-submicron CMOS processes.

VCO-based ADCs have been widely studied in a great deal of papers and it is known that one of its main drawbacks is the non-linearity it presents. To overcome this issue, to place the VCO within a closed-loop is usually done to attenuate its input magnitude level. However, to do so it is needed a digital-to-analog converter (DAC) as in a conventional CT-$\Delta\Sigma$, therefore it is required for the DAC to be simple and it cannot present a high number of elements, being the latter a bottleneck for implementing VCOs with a high number of inverters. This works presents a technique that enables to use VCOs with severals inverters while keeping the same number of DAC elements as before. Based upon previous theoretical studies of the VCO-based ADCs which model it as a pulse frequency modulation encoder, this new technique is analyzed and linear models are developed in order to study its viability at system level. Moreover, how impairments related to a real implementation affect the use of this technique are also analyzed.

The contributions proposed in this document are focused but not limited to communication applications.

Keywords: Delta-Sigma, Voltage-Controlled Oscillator, Analog-to-Digital conversion, VCO-based ADC.

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Víctor Medina.

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

List of Symbols

ADC Analog-to-Digital converter

BW Bandwidth

CLA Clocked Averaging

CT-ΔΣ Continuous-Time Delta-Sigma

DAC Digital-to-Analog converter

dBFS Decibels Relative to Full Scale

DT-ΔΣ Discrete-Time Delta-Sigma

DWA Data Weigth Averaging

ENOB Effective Number of Bits

FIR Finite Impulse Response

FOM Noise Transfer Function

IIR Infinite Impulse Response

IPFM Integral Pulse Frequency Modulation

LSB Least Significant Bit

MSB Most Significant Bit

NRZ Non-Return-to-Zero

NTF Noise Transfer Function

OSR Oversampling Ratio

PDF Probability Density Function

PFM Pulse Frequency Modulation

PPF Post-Processing Filter

PWM Pulse Width Modulation

SNDR Signal-to-Noise and Distortion Ratio

SQNR Signal-to-Quantization Noise Ratio

STF Signal Transfer Function

T2B Thermometric-to-Binary

VCO Voltage Controlled Oscillator

1. INTRODUCTION

1.1. Motivation of Work

Analog-to-Digital converters (ADC) play an important role every time that a signal from the physical, and thus analog world needs to be quantified in order to be processed later on in the digital domain, for that reason they are present everywhere from test instruments, radio systems, audio systems to an everyday object like a smartphone, where they are used for recording and communications purposes among many others. ADCs are circuits that present both analog and digital electronics, and are implemented on microelectronic circuits where the digital side domains because, depending on the application, they suppose most of the die area, that is, it uses more transistors than its analog counterpart. Digital electronics benefits strongly from the shrink of the semiconductor device fabrication, because transistors are able to switch faster due to that the value of their stray capacitors is decreased, it is possible to reduce the area or to increase functionality on the same area as before. However, although analog electronics also benefits of an increase on maximum operating frequency, it presents a series of disadvantages such as a decrease on the intrinsic gain of the transistor, less transistors in series as the supply voltage decreases faster than the threshold voltage, leading to power inefficient architectures. To fabricate an integrated circuit means to *integrate* on a same waffer, analog and digital designs. Consequently, it is desired that the ADC presents more digital than analog components.

In the last decade, because many advances in different areas of science have been done, the performance of the ADC need also to improve:

-High-speed communications such as 4G or 5G need ADC with wide analog bandwitdh and high resolution.

-Devices related to Internet of Things, or just plain portable devices that require low power circuits because battery life has become very important.

That is why audio and communication ADCs have been using more and more digital structures, such as voltage controlled oscillators (VCO) by means of ring oscillators, since they benefit from the aforementioned advantages. Moreover, the use of VCO-based ADCs can improve instrumentation applications [1], they present a high sensitivity and can possibly dismiss instrumentation amplifiers used for the conventional switched-capacitor ADCs.

According to these precedents, this Master's Thesis arises to develop a novel technique to implement VCO-based ADCs more efficiently, and its viability is studied at system level. The idea behind this Master's Thesis was conceived by the research group of Microelectronics Design and Applications (DMA) within the Electronic Technology Department of the Carlos III University. It was developed through a research scholarship

with Intel Austria to develop a viability study, yielding in a new family of ADCs.

1.2. Goals

A list of objectives is listed below:

- The main goal is to present a theoretical study of the proposed bit-split technique and study its validity for a selected cases of impairments.
- To emphasize the importance that VCO-based ADCs have gained in last years.
- To review and study thoroughly the VCO as a pulse frequency modulation encoder.

1.3. Structure of the document

This document is structured as follows:

- The second chapter presents the state-of-art, starting from the general, ADCs and Continuous-Time Delta-Sigma (CT-$\Delta\Sigma$) to the specific, VCO-based ADC CT-$\Delta\Sigma$, while devoloping a brief overview on the basic theory behind them. It also presents the importance that VCO-based ADCs have gained last years.
- In the third chapter it is first reviewed the theoretical foundations of the VCO as a pulse frequency modulator because it is the basis to understand this work. Then a introduction to the technique Bit-split is presented for a classical CT-$\Delta\Sigma$ and two VCO-based ADCs.
- The fourth chapter develops the theory behind the bit-split technique for the selected first and second order VCO-based ADCs architectures. It presents an analysis and linear models. It is also presented an extension for any order of the previous selected architectures.
- In the fifth chapter a study case is presented, where an architecture for the implementation of the bit-split is given. Different impairments such as, analog-digital mismatch, delay in the loop among others are studied.
- The sixth chapter presents the conclusion of this work, the objectives that have been reached and future work.

2. STATE OF THE ART

There are several types of ADCs, as the successive approximation register (SAR), flash, pipelined, dual-slope, ΔΣ, etc... Each one with its strengths and weaknesses. Figure 2.1[1] shows a graphical comparison in terms of bandwidth and resolution given in effective number of bits (ENOB). ENOB is a measure in bits of the dynamic range of an ADC. It can be observed that ΔΣ data converters are distributed within all frequencies presenting high resolution for low frequencies.

The focus of this work is on applying a novel technique to VCO-based ADCs with wide analog bandwidth which fall within the category of Continuous-Time ΔΣ converters. For this reason, a brief overview on what is an ADC and specifically a ΔΣ modulator is given.

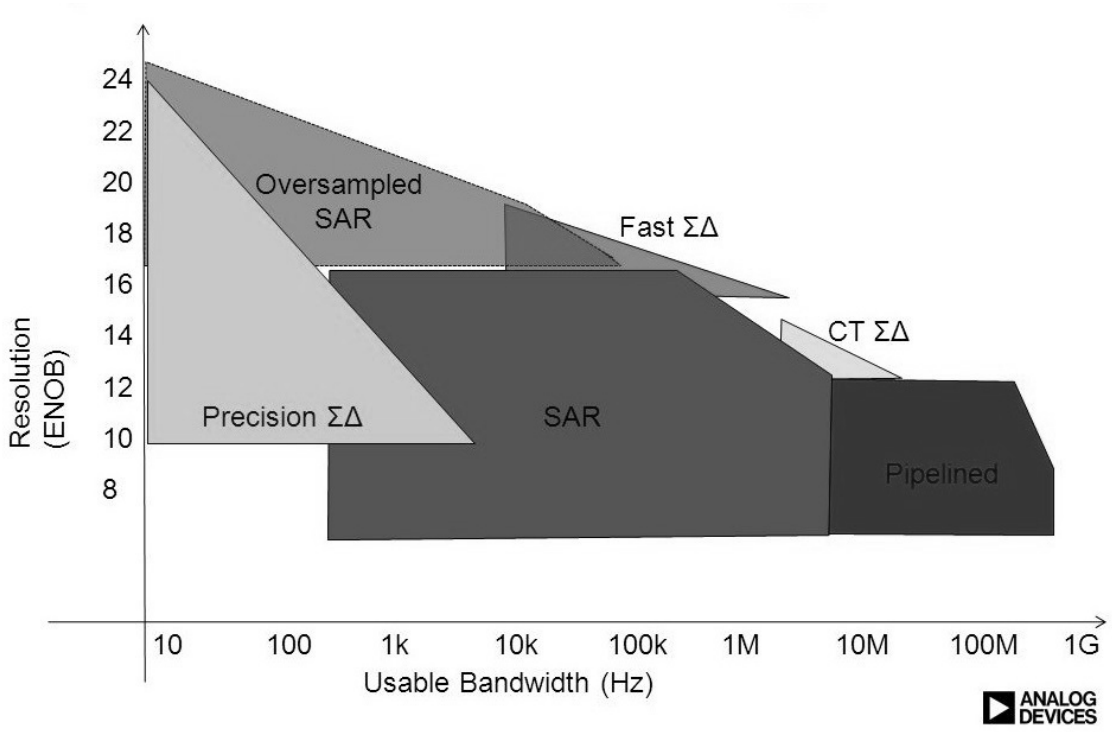


Fig. 2.1. Comparison of various types of ADC. [2]

2.1. ADC Converters

The goal of an ADC is to take a physical signal that can present *infinite* values within an interval, and to transform it at sampling instants into a digital signal which presents

[1] It is noted that the figure is slightly outdated because there are CT-ΔΣ converters with bandwidth greater than 100 MHz. The picture is used for comparison purposes.

discrete values. This is depicted in figure 2.2.

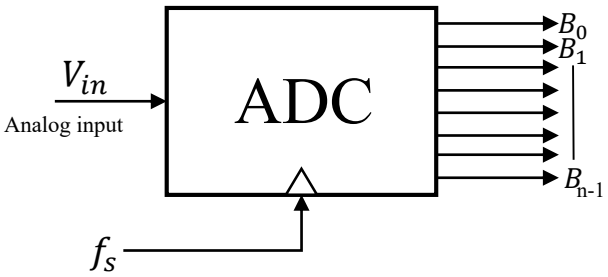


Fig. 2.2. A block diagram of an ADC.

2.1.1. Basics of an ADC converter

The input-output relationship of figure 2.2 is defined as:

$$V_{in}(kTs) = D_{out}[k] + V_x[k] = V_{ref} \sum_{m=0}^{n-1} B_m 2^m + V_x, \tag{2.1}$$

where D_{out} represents the digital representation of V_{in}, V_{ref} is the voltage reference and B_m represent the m^2 bit and V_x is the quantization error, that is, the difference between the input signal and its quantized version. Assuming that quantization steps are equally distributed, each step is given by equation (2.2) and, assuming that the input signal is bounded to the range of the ADC, the quantization error V_x is given by equation (2.3)

$$V_{LSB} = \frac{V_{ref}}{2^n}. \tag{2.2}$$

$$-\frac{1}{2}V_{LSB} \leq Vx \leq \frac{1}{2}V_{LSB} \tag{2.3}$$

To model the quantization noise, usually an stochastic approach is used [3]. It is assumed that the input varies rapidly so the error signal V_x can be approximated to a random variable uniformly distributed between $V_{LSB}/2$ and $-V_{LSB}/2$. Therefore, the probability density function (PDF), $P(\psi)$, is constant as shown in figure 2.3. It is observed that the noise becomes independent from the input signal or sampling frequency. The average value of such PDF is zero:

$$\overline{V_x} = \int_{-\infty}^{\infty} \psi P(\psi) d\psi = \frac{1}{V_{LSB}} \left(\int_{\frac{-V_{LSB}}{2}}^{\frac{V_{LSB}}{2}} \psi d\psi \right) = 0. \tag{2.4}$$

Defining the rms value of V_x as:

$$V_{x(rms)} = \left(\int_{-\infty}^{\infty} \psi^2 P(\psi) d\psi \right)^{1/2} = \left[\frac{1}{V_{LSB}} \left(\int_{\frac{-V_{LSB}}{2}}^{\frac{V_{LSB}}{2}} \psi^2 d\psi \right) \right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.5}$$

[2] B_{n-1} is the most significant bit (MSB) and B_0 the least significant bit (LSB). The factor 2^m indicates the binary weight of each bit.

Thus, for an input sinusoidal with peak-to-peak amplitude of $V_{pp} = 2^n V_{LSB}$, $V_{in(rms)}$ is defined as:

$$V_{in(rms)} = \frac{2^n V_{LSB}}{2\sqrt{12}} \tag{2.6}$$

The relation between the power of the input and quantization error is called *Signal-to-Quantization Noise Ratio* (SQNR):

$$\text{SQNR} = 20\log\left(\frac{V_{in(rms)}}{V_{x(rms)}}\right) = 20\log\left(\frac{V_{LSB}2^n/(2\sqrt{2})}{V_{LSB}/\sqrt{12}}\right) = 6.02n + 1.76 \text{ dB} \tag{2.7}$$

Starting from section 2.3 the term *Signal-to-Noise and Distortion Ratio* (SNDR) will be used instead of SQNR because it is more accurate for the purposes of this work, since it takes into account not only the quantization noise but also distortion. It is observed that the SQNR increases 6.02 dB for every extra bit of the converter.

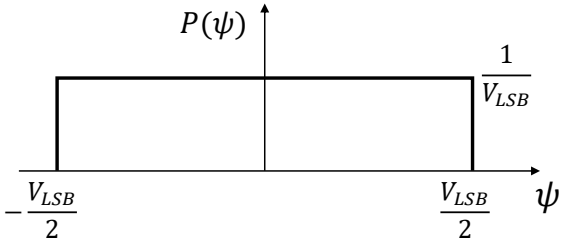


Fig. 2.3. Power distribution noise for the quantization error.

Classification of ADCs Typically, two types of converters are considered:

- Nyquist-rate Converters: The sampling rate is defined by the Nyquist rate, that is, the double of the input bandwidth. However, it is often for they to operate at 1.5 to 10 times the Nyquist rate, because this eases the design of anti-aliasing filters.
- Oversampling Converters: The sampling rate is usually 10 to 512 times faster than the Nyquist rate and thus the SQNR is increased because the noise that do not fall within the band of interest can be filtered.

2.1.2. Oversampled Converters

The increase of the sampling frequency involves that the noise spectral density is defined instead of between $-f_{sN}/2$ and $f_{sN}/2$, where f_{sN} is the Nyquist sampling frequency, to f_s, being f_s higher than f_{sN}. Because the total power of the noise remains constant and it is independent of the sampling frequency, the noise power density within the band of interest is less for the sampling frequency f_s. The Oversampling Ratio (OSR) is the relationship between f_s and f_{sN}:

$$\text{OSR} = \frac{f_s}{f_{sN}} = \frac{f_s}{2f_B}, \tag{2.8}$$

where f_B is the input signal bandwidth. Therefore, assuming a brick-wall filter is used to remove noise outside the bandwidth of interest, a new equation for the SQNR arises and it is as follows:

$$\text{SQNR} = 6.02n + 1.76 + 10\log(\text{OSR})dB. \tag{2.9}$$

It is observed that every time the OSR is doubled, the SQNR is increased by 3dB.

2.2. Delta Sigma Data-Converters

In addition to the oversampling, it is possible to shape the noise spectrum. Architectures that apply noise-shaping are usually referred to ΔΣ modulators. During the last decades, the choice of design has been discrete-time ΔΣ modulators because the use of switched-capacitors has proved to be the best in terms of efficiency and design. Yet recently, because the need to increase the bandwidth of the ADC, continuous-time ΔΣ ADCs have gained popularity in both academia and industry. Furthermore, CT-ΔΣ ADCs do not need an explicit anti-aliasing filter at the input because they do present one implicitly [4]. Figure 2.4 shows a block diagram for a Discrete-Time ΔΣ (DT-ΔΣ), the block " ΔΣ" carries out the noise-shaping. First and second order ΔΣ modulators will be presented. It is noted that the noise can be filtered out in a low-pass, band-pass or high-pass way, depending on the application; the focus on this work is on the low-pass modulators.

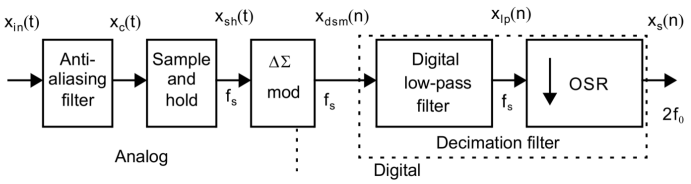


Fig. 2.4. Block diagram for a DT-ΔΣ ADC [5].

2.2.1. First order Delta Sigma modulator

A first order DT-ΔΣ modulator [6] and its equivalent linear model are shown in figure 2.5. It is composed by a discrete-time filter acting as integrator, a quantizer and a negative feedback path. Thus, the name of the modulator can be understood as Σ being the integrator and Δ the subtraction produced at the input of the filter. Because in the previous section the noise has been supposed to be white, in the linear model, it is thought of as an additive random sequence to the integrator output. It is considered that the impulse response of the DAC is a non-return-to-zero (NRZ) pulse.

Being $U(z)$ the input signal, $Q(z)$ the quantization error and $Y(z)$ the output of the modulator, the following relationship yields:

$$Y(z) = z^{-1}U(z) + (1 - z^{-1})Q(z). \tag{2.10}$$

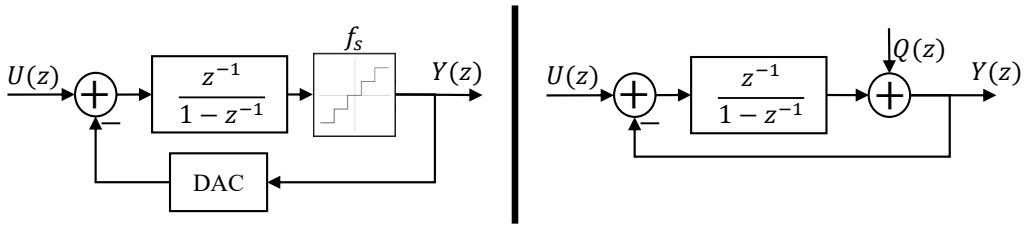


Fig. 2.5. First-order ΔΣ modulator and its linear model.

The relationship between $Y(z)$ and $X(z)$ is called Signal Transfer Function (STF), and Noise Transfer Function (NTF) to the relationship between $Y(z)$ and $E(z)$. The above equation points out that STF is only a delay of one sample, this is why the anti-aliasing filter is needed for the DT-ΔΣ modulators. On the other hand, the NTF is a first difference, thus the noise at the output presents a first-order high-pass shape. Due to this noise-shaping, a new expression for the SQNR arises:

$$\text{SQNR} = 6.02n + 1.76 - 5.17 + 30\log(\text{OSR})\ \text{dB}. \tag{2.11}$$

It is observed that doubling the OSR yields in an increase of 9 dB instead of 3 dB as was the case for plain oversampling (equation (2.9)).

2.2.2. Second and higher order Delta Sigma modulator

To build a generic second order ΔΣ modulator it is only needed to place another integrator; another feedback path is needed to ensure system stability. Thus, the noise presents a second-order high-pass shape. If the transfer function of the filter is considered to be $(1 - z^{-1})^2$, a new equation for the SQNR is found:

$$\text{SQNR} = 6.02n + 1.76 - 12.7 + 50\log(\text{OSR})\ \text{dB}. \tag{2.12}$$

It can be observed that now every time the OSR is doubled, the SQNR increases in 15 dB. This trend in which increasing the order results in a higher SQNR values is also valid for higher order systems; however, as the order goes up, so it does its complexity and it is more prone to different impairments, such as instability [7]. Figure 2.6 shows a comparison of the noise-shaping for first and second order modulator and a Nyquist-rated converter, it is noted that for OSR values greater than 2 the second-order always yields better results.

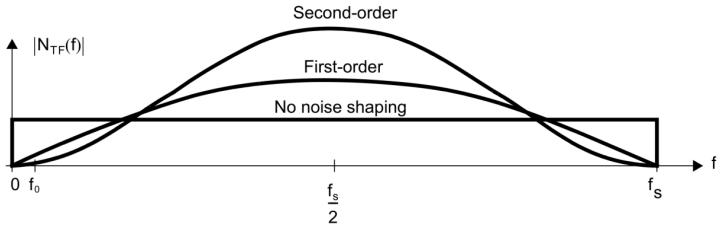


Fig. 2.6. Magnitude of a first and second order ΔΣ modulator and a Nyquist-rate converter [5].

2.2.3. Circuit implementations

Focusing on the CT-ΔΣ modulators different implementations can be used. Continuous-time implementations sample the signal within the loop and as it was the case for the discrete-time they contain integrators. Traditionally, these integrators have been implemented by means of an Opamp-RC, an OTA-RC or a Gm-C [6]. The difference is that two first circuits work on a closed-loop, and thus they present a more linear response while the last one is usually faster. However, in recent years CT-ΔΣ modulators using VCOs have gained popularity because the harmony VCOs present with the shrink of fabrication technology [8]–[11].

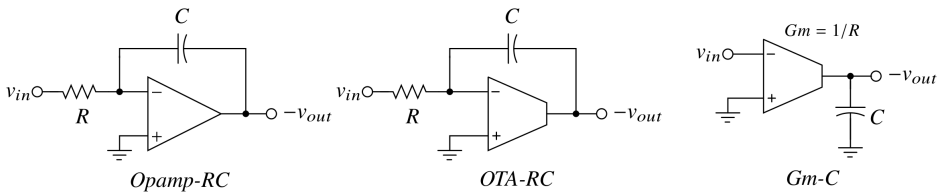


Fig. 2.7. Three methods for implementing an integrator for CT-ΔΣ modulators [6].

2.3. VCO-based ADCs

Even though the first ΔΣ modulator using VCOs was reported more than 20 years ago [12], [13], it wasn't until recently that the spotlight was on them. Several architectures for audio, instrumentation and communication applications using VCOs are already well developed and are very competitive because its mostly digital implementation and low power consumption [14]–[17]. Figures 2.8 and 2.9 presents two plots in which two different of figures of merits (FOM) are represented for several ADCs [18]. FOM is used to compare different ADCs performance; Schreier FOM and Walden FOM are the most used for ADCs [19]. A few implementations using VCOs are remarked on these figures and it can be observed that its performance has gotten better with years.

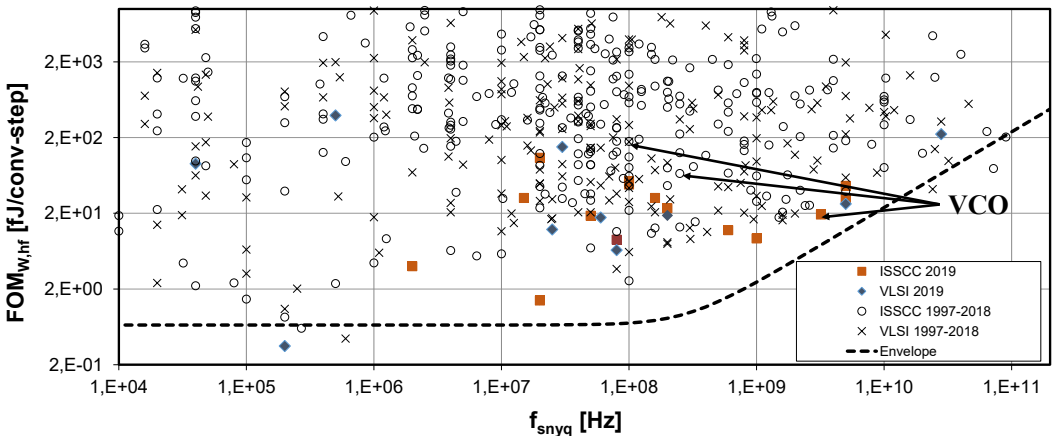


Fig. 2.8. Walden FOM for several ADCs [18].

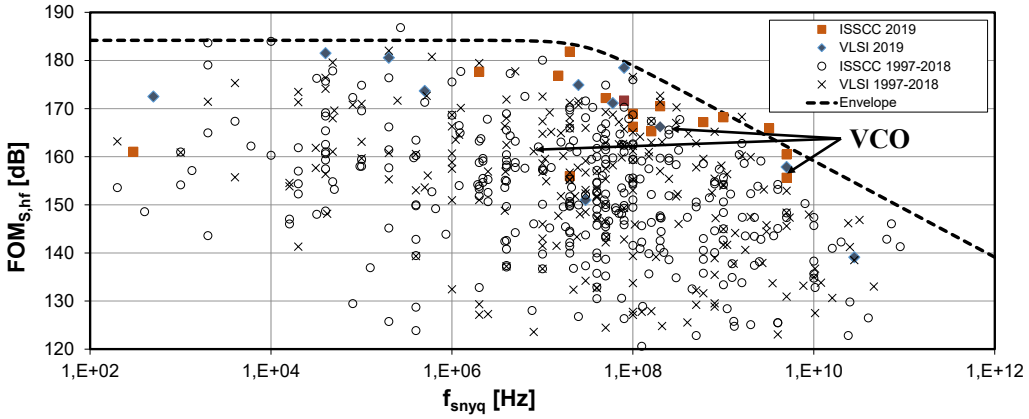


Fig. 2.9. Schreier FOM for several ADCs [18].

Among the several configurations proposed using VCOs, the following are highlighted:

- VCO in open loop configuration: A VCO-based ADC can be built as depicted in figure 2.10. The quantization and first difference blocks are implemented with two flips flops and an XOR operation. Its equivalent but approximate linear model assumes that the quantization noise is white. Then a first difference is applied, and thus the noise present a first-order high-pass shape. The limit of this configuration is the non-linearity of the gain of the VCO (k_{vco}); however new techniques that try to mitigate this issue are reported in [20], [21]. Another limit was the restraint to a first-order noise-shaping, however recent publications have shown that it is possible to extend the order or to implement band-pass modulators [22], [23].

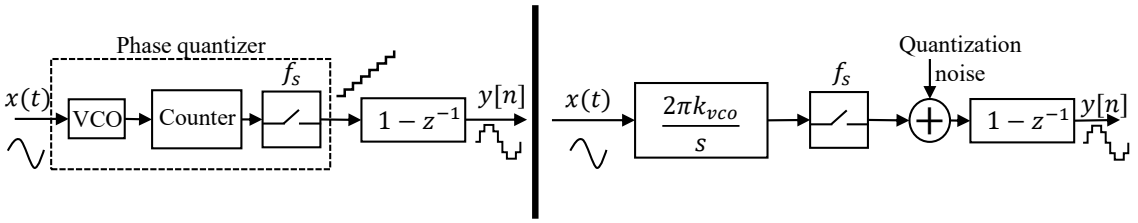


Fig. 2.10. Open loop VCO-based quantizer: block diagram and its linearized frequecy-domain model.

- VCO in closed-loop configuration: The previous structure suffers from the non-linearity of the VCO, therefore when placing it within a closed-loop configuration, the input magnitude to the VCO decreases and thus it works in its linear region producing harmonics with less power, and so the SNDR is not highly decreased. Two structures are usually used for closed loop configurations, frequency and phase feedback, each one with its advantages and disadvantages [24], [25]. Furthermore, using a closed-loop configuration it is possible to increase the order of the modulator by means of using a filter before the VCO, resulting in higher SNDR. This also reduces its input magnitude. It is noted that whereas in the open-loop configuration there was no need for a DAC, in closed-loop configuration DAC plays an important role. The requirement of a low complexity thermometric DAC is an important limit to exploit the possibility of having VCOs with a high number of inverters, because in most of the cases the DAC is only of 5 bits while the number of inverters can easily be over 90. Consequently, VCO taps[3] are limited to the number of elements of the DAC.

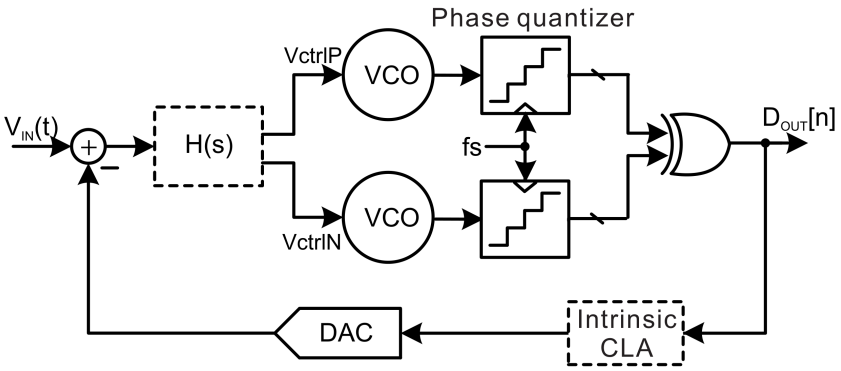


Fig. 2.11. Closed-loop ΔΣ ADC using VCO-based integrator [25].

- Time-interleaving sampling: Both previous configurations can also present time-interleaving which can increase the resolution without increasing the order of the noise-shaping or the sampling frequency. To that end, the effective sampling frequency is increased by a digital delay line connected to the output of the VCO. The

[3]Taps and inverters will be used indistinctly.

output is then decoded with an array of XOR that increases the oscillation frequency of the VCO. This allows that the output data can be processed at a higher frequency and so it presents a higher OSR and yields better SNDR [26]–[28].

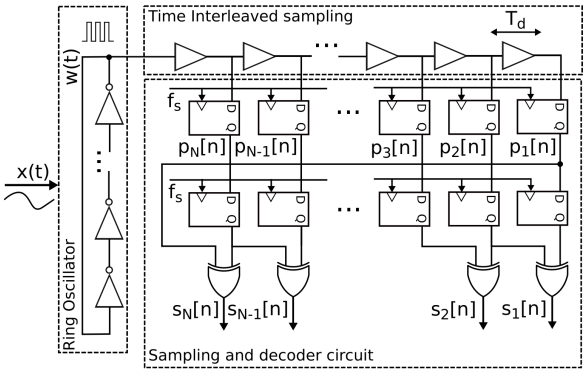


Fig. 2.12. Open-loop VCO-based quantizer using time-interleaving sampling [26].

2.4. Summary

To use a VCO-based ADC has been proven to be a good choice for high bandwidth applications due to its mostly digital implementation and low power consumption as shown in [27] or [15]. However, to fully exploit its capability, issues related to the non-linearity of the ring oscillator must be solved because it is one of the main limitations for the SNDR. Moreover, even though the first-order noise-shaping is easy to achieve circuit-wise, it certainly gets complicated, and somewhat impractical, when extending the order in open loop configurations. Thus, closed-loop architectures are needed, presenting advantages such a reduced input level, but also disadvantages such as to deal with a DAC or problems with stability and delays in the loop.

3. THEORETICAL FOUNDATIONS OF THE VCO AND INTRODUCTION TO THE BIT-SPLIT TECHNIQUE

In this chapter, the equations that describe the VCO as a Pulse Frequency Modulator (PFM) encoder will be presented in order to set the theoretical basis for the correct explanation and understanding of the proposed technique, bit-split. An introduction to this method is given.

3.1. VCO and PFM

PFM is a technique to encode information and it has also been found to be present in biological systems with a nervous system [29]. It represents an analog signal by means of a two level representation as other type of modulations such as pulse-width modulation (PWM), or pulse phase modulation. If any two consecutive pulses are defined by equation (3.1), such a system is called integral pulse frequency modulation (IPFM), but for simplicity on the text it is used PFM instead.

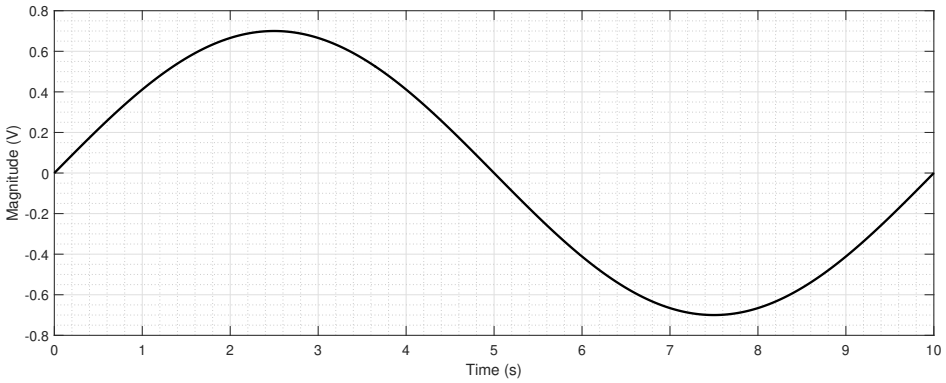
$$r = \int_{t_i}^{t_{i+1}} [m_o + x(t)]\, dt \tag{3.1}$$

$$x(t) = A\cos(2\pi f_x t + \phi_S), \tag{3.2}$$

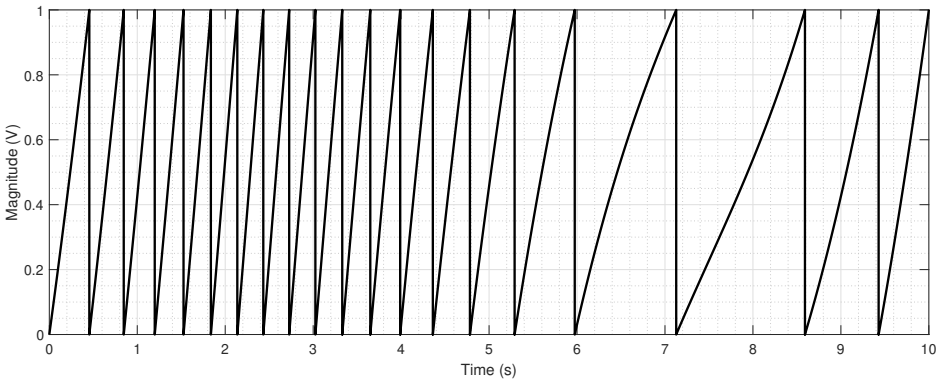
where A, f_x and ϕ_S are the amplitude, frequency and initial phase of the modulating signal $x(t)$, respectively. The unmodulated pulse repetition ($x(t) = 0$) is given by $f_o = m_o/r$; m_o is a constant. Now, diving equation 3.1 by r such that the left-hand side is 1, the following equation yields:

$$1 = \int_{t_i}^{t_{i+1}} \left[f_o + \frac{x(t)}{r} \right] dt. \tag{3.3}$$

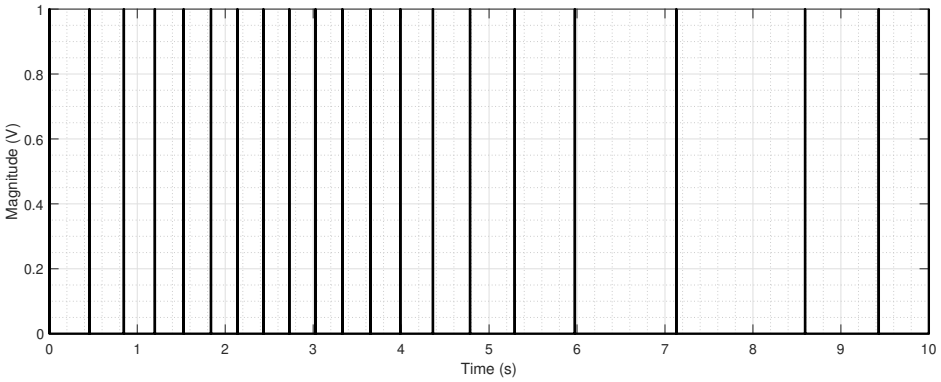
A charging function, $c(t, \alpha)$, is defined as the function equal to the right hand side of the above equation, but each time the threshold, in this case 1, is reached it is reset and a pulse is generated. Therefore, this function is also determined by where the time origin $t = 0$ is considered. The parameter α is defined as the interval, in seconds, between the first preceding pulse and the considered time origin. Figure 3.1 shows the modulating signal, the charging function, the train of pulses and the equivalent block diagram that describe the whole operation; α and ϕ_S are considered to be 0.



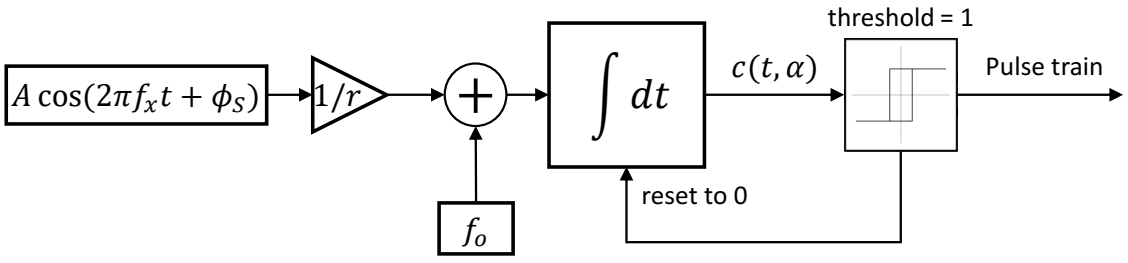
(a)



(b)



(c)



(d)

Fig. 3.1. (a) Input modulating signal, (b) charging function, (c) pulse train, and (d) block diagram of the IPFM [30].

A VCO is a voltage-controlled oscilator whose output, $VCO_{out}(t)$, is given by the equation (3.4); it is related to its phase, $\theta(t)$, that is described by equation (3.6). At the same time, $\theta(t)$ depends on the current oscillation frequency, $f_{osc}(t)$ (equation (3.5)), that also depends on the input signal, that from now on, unless otherwise is stated, it will be considered to be the signal given by equation (3.2). These equations are now defined:

$$VCO_{out}(t) = \sin\left(\theta\left(t\right) + \theta_0\right), \tag{3.4}$$

$$f_{osc}(t) = f_o + k_{vco}x(t), k_{vco} \leq f_o, -1 \leq x(t) \leq 1, \tag{3.5}$$

$$\theta(t) = 2\pi \int_0^t f_{osc}(\tau)d\tau = 2\pi\left(\int_0^t f_o d\tau + k_{vco}\int_0^t x\left(\tau\right)d\tau\right), \tag{3.6}$$

where θ_0 is the initial phase of the VCO, f_o and k_{vco} are the central frequency and gain of the VCO.

By setting $r = 1/k_{vco}$ in equation (3.3) and plotting both $c(t, \alpha)$, with $\alpha = 0$, and $VCO_{out}(t)$ with $\theta_0 = 0$ it is observed that instants where the sine wave passes from negative to positive, it matches the instants where a pulse is generated. This is represented in the following figure:

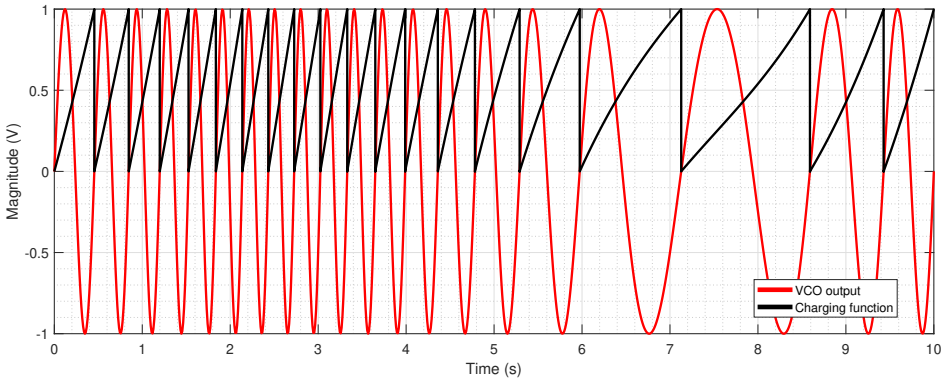


Fig. 3.2. Representation of the charging function and VCO_{out}.

Therefore, the equivalence between a PFM encoder and a VCO is stated, enabling a theoretical study of the VCO [31]. $VCO_{out}(t)$ is redefined as follows to be in harmony with the actual working operation of a VCO implemented with ring oscillators:

$$VCO_{out}(t) = \begin{cases} 0, & \text{if } \sin\left(\theta\left(t\right) + \theta_0\right) < 0 \\ 1, & \text{if } \sin\left(\theta\left(t\right) + \theta_0\right) \geq 0 \end{cases} \tag{3.7}$$

As stated in [22], using an edge detector as an auxiliary block, the new output, $d(t)$ is now a stream of Dirac Deltas following equation (3.8). Figure 3.3 depicts the VCO-PFM equivalence.

$$d(t) = \sum_{k=0}^{\infty} \delta(t - t_k), \forall t_k \mid \theta_{VCO}(t_k) = 2\pi k \tag{3.8}$$

Using [30] it is possible to expand equation (3.8) into a trigonometric series as follows:

$$\begin{aligned} d(t,\alpha) = f_o &+ Ak_{vco}\cos(2\pi f_x t + \phi_S) \\ &+ 2f_o \sum_{q=1}^{\infty}\sum_{r=-\infty}^{\infty} J_r\left(\frac{qAk_{vco}}{f_x}\right)\left(1+\frac{rf_x}{qf_o}\right) \\ &\times \cos\left[2\pi\left(qf_o + rf_x\right)t + r\phi_S\right. \\ &\left. + q\left(2\pi f_o\alpha - \frac{Ak_{vco}}{f_x}\sin(\phi_S - 2\pi f_x\alpha)\right)\right], \end{aligned} \tag{3.9}$$

where, J_r is a Bessel function of the first kind of order r. The value of alpha is given by the following equation[4] for $\theta_0 \in (0, 2\pi]$:

$$\begin{aligned} &\int_{-\alpha}^{0}\left[2\pi f_o + \frac{Ak_{vco}}{f_x}\cos(2\pi f_x t + \phi_S)\right]dt = \\ &2\pi f_o + \frac{Ak_{vco}}{f_x}\sin(\phi_S) - \frac{Ak_{vco}}{f_x}\sin(\phi_S - 2\pi f_x\alpha) = 2\pi - \theta_0, \end{aligned} \tag{3.10}$$

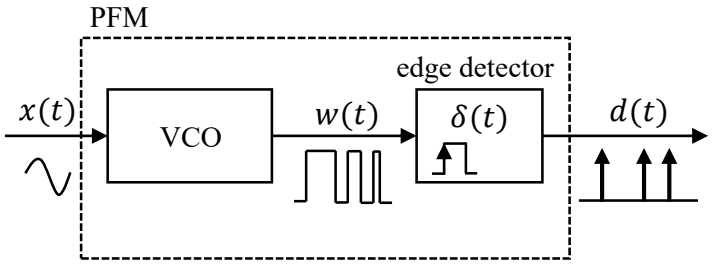


Fig. 3.3. VCO-PFM equivalence.

Applying the Fourier Transform[5] to equation (3.9), but only taking into account positive frequencies[6] and with its power doubled, $D(f)$ is as follows:

$$\begin{aligned} D(f,\alpha) = f_o\delta(f) &+ Ak_{vco}e^{i\phi_S}\delta(f - fx) \\ &+ 2f_o \sum_{q=1}^{\infty}\sum_{r=-\infty}^{\infty} J_r\left(\frac{qAk_{vco}}{f_x}\right)\left(1+\frac{rf_x}{qf_o}\right) \\ &\times e^{i\left(r\phi_S + q\left(2\pi\alpha - \frac{Ak_{vco}}{f_x}\sin(\phi_S - 2\pi f_x\alpha)\right)\right)} \\ &\times \delta(f - (qf_o + rf_x)). \end{aligned} \tag{3.11}$$

This last equation presents a component at f_x which depends linearly on k_{vco} and the amplitude of $x(t)$. There is also modulation sidebands occurring at multiples of f_o. These

[4] Actually, the equation (3.10) cannot be solved analytically but only by means of approximations, i.e., Newton's method [32]

[5] The Fourier Transform and its applications can be reviewed in [33]–[35].

[6] It is assumed that the power contribution of sidebands centered at multiples of $-f_o$ that fall in positive frequencies are negligible in comparison with the power produced by the sidebands centered at multiples of f_o. Consequently, such contributions are disregarded.

sidebands are not symmetrical nor monotonically decaying [31]. These sidebands are depicted in figure 3.4.

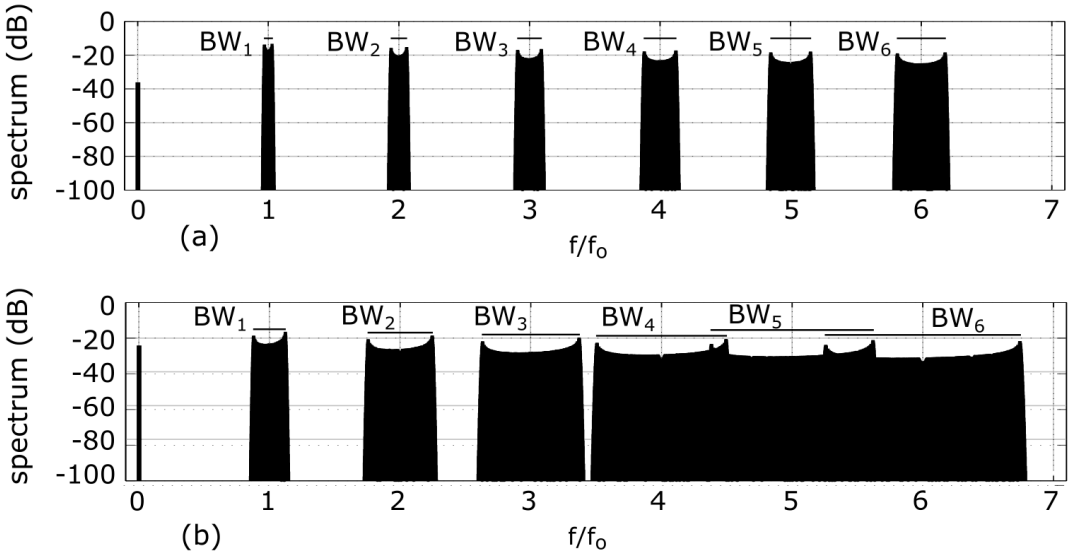


Fig. 3.4. Output spectrum according to (3.11) of the first six sidebands for a $\phi_S = 0$, $\alpha = 0$, $f_x = f_o/1024$, (a) $Ak_{vco} = f_o/32$, and (b) $Ak_{vco} = f_o/32$ [31].

To build a VCO-ADC from this model, a pulse shape filter must be placed after $d(t)$ as depicted in figure 3.5, according to [31], the pulse shape filter must have periodic zeroes at the sampling frequency, so the modulation sidebands that would fall into the signal-band are attenuated. Using [30] again, the new signal, $p(t)$, and its trigonometric series expansion can be calculated. In this work, it is considered a first order filter $H(s)$:

$$H(s) = \frac{1 - e^{-sT_s}}{sT_s} \tag{3.12}$$

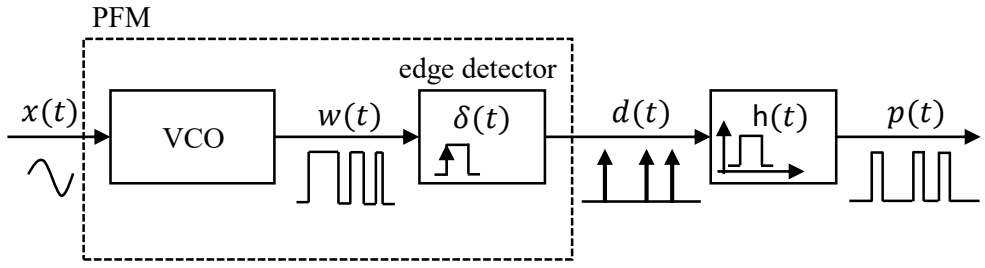


Fig. 3.5. VCO-PFM equivalence followed by a rectangular pulse, $h(t)$.

$$p(t) = \sum_{k=0}^{\infty} u(t - t_k) - u(t - t_k - T_s), \forall t_k \mid \theta_{VCO}(t_k) = 2\pi k \tag{3.13}$$

$$
\begin{aligned}
p(t,\alpha) = {} & T_s f_o + T_s A k_{vco} \frac{\sin(\pi T_s f_x)}{\pi T_s f_x} \cos(2\pi f_x t - \pi T_s f_x + \phi_S) \\
& + 2 T_s f_o \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} J_r\left(\frac{q A k_{vco}}{f_x}\right) \frac{\sin[\pi T_s (q f_o + r f_x)]}{\pi T_s q f_o} \\
& \times \cos\left[2\pi\left(q f_o + r f_x\right) t - \pi (q f_o + r f_x) T_s + r\phi_S \right. \\
& \left. + q\left(2\pi f_o \alpha - \frac{A k_{vco}}{f_x} \sin(\phi_S - 2\pi f_x \alpha)\right)\right].
\end{aligned}
\tag{3.14}
$$

Its Fourier Transform (again only positive frequencies with its power doubled) is as follows:

$$
\begin{aligned}
P(f,\alpha) = {} & T_s f_o \delta(f) + T_s A k_{vco} e^{i\phi_S} e^{-i\pi T_s f_x} \frac{\sin(\pi T_s f_x)}{\pi T_s f_x} \delta(f - fx) \\
& + 2 T_s f_o \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} J_r\left(\frac{q A k_{vco}}{f_x}\right) \frac{\sin[\pi T_s (q f_o + r f_x)]}{\pi T_s q f_o} \\
& \times e^{-i\pi (q f_o + r f_x) T_s} \\
& \times e^{ir\phi_S} \\
& \times e^{iq\left(2\pi f_o \alpha - \frac{A k_{vco}}{f_x} \sin(\phi_S - 2\pi f_x \alpha)\right)} \\
& \times \delta(f - (q f_o + r f_x)).
\end{aligned}
\tag{3.15}
$$

The equation above represents the power spectrum for every frequency before sampling is done, because otherwise alias would occur. Even though it looks like a non-intuitive equation, in the next section $P(f,\alpha)$ will be of importance and its treatment is indeed intuitive.

3.2. Multiphase ring oscillator based ADC

3.2.1. VCO-based quantizer

Figure 3.6 depicts the practical implementation of a multiphase ring oscillator based ADC. There are two sets of ring oscillators, one being drived by the signal input as it is (VCOp), and the other receives its negative (VCOn); each inverter output is sampled twice and then a XOR operation is performed on those samples. Finally, summing all the lines from VCOp and VCOn independently and then subtracting the latter on the former the output is obtained. Equations of the previous section can be used to obtain an equivalent model based on Pulse Frequency Modulation with single bits VCOs.

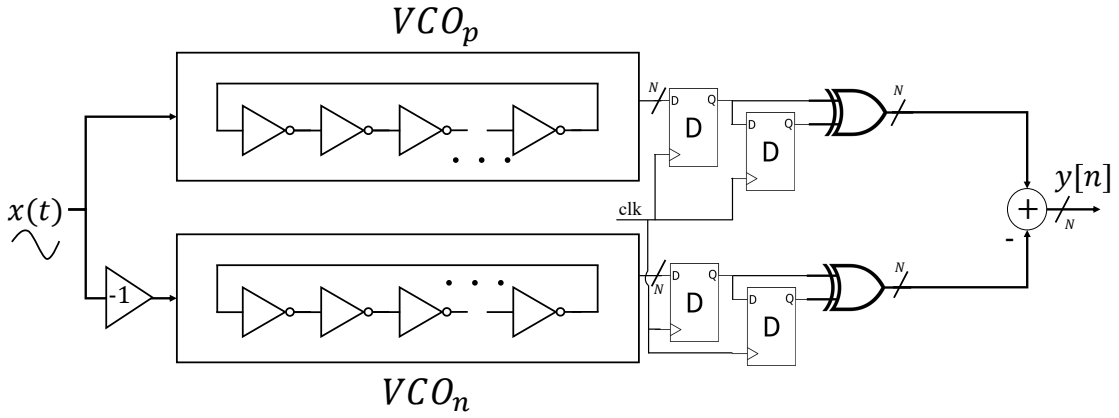


Fig. 3.6. Practical differential implementation for a VCO-based ADC in a open loop configuration.

The XOR operation does the following, whenever there is a change on an inverter, that is, going from 0 to 1 or vice-versa, it produces a pulse of length T_s. Therefore, each inverter produces two pulses per oscillation; this can be modeled as two single bit VCOs, having both the same initial phase as the inverter but, one is shifted π radians. The different phases of a ring oscillator presenting N inverters is given by:

$$\theta_{inv,k} = \begin{cases} -\pi k/N & \text{if } mod(k,2) = 0 \\ -\pi\,(k/N + 1) & \text{if } mod(k,2) \neq 0 \end{cases} \tag{3.16}$$

Where $k = 0, 1, 2, ..., N-1$; it represents the index of the different inverters. The ring oscillator will present equidistant phases only if N is odd. As the equivalent model has $2N$ single-bit VCOs because the XOR-operation, being the first N VCOs the same phase as in equation (3.16) and the rest of them having a phase shitf of π radians, the resultant phases are equidistant as well. Moreover, due to the shift of π by the XOR operation, a ring oscillator with even number of inverters, even though its phases are not equidistant, its equivalent single bit VCO will be equidistant.

Focusing on the VCOp, its output spectrum will be given by the sum of the $2N$ single bit VCOs, therefore summing their corresponding $P(f, \alpha)$ will yield the desired equation for the spectrum. But before that, in order to gain insight about the final spectrum, it is possible to substitute part of the last exponential in the equation (3.15) by part of the equation (3.10):

$$2\pi f_o \alpha - \frac{Ak_{vco}}{f_x}\sin(\phi_S - 2\pi f_x \alpha) = 2\pi - \theta_0 - \frac{Ak_{vco}}{f_x}\sin(\phi_S) \tag{3.17}$$

Now the last complex exponential can be thought of as a rotating vector whose angle is given by the initial phase of the VCO and the input signal; because it is a complex exponential, the term 2π can be omitted because it is mapped as 1. Therefore, summing

each $P(f)$ the following yields:

$$
\begin{aligned}
P(f) = {} & 2NT_s f_o \delta(f) + 2NT_s A k_{vco} e^{i\phi_S} e^{-i\pi T_s f_x} \frac{\sin(\pi T_s f_x)}{\pi T_s f_x} \delta(f - fx) \\
& + 2T_s f_o \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} J_r\left(\frac{qAk_{vco}}{f_x}\right) \frac{\sin[\pi T_s (qf_o + rf_x)]}{\pi T_s q f_o} \\
& \times e^{-i\pi(qf_o + rf_x)T_s} e^{ir\phi_S} e^{-iq\left(\frac{Ak_{vco}}{f_x} \sin(\phi_S)\right)} \\
& \times \sum_{j=1}^{2N} e^{-iq\theta_{VCO,j}} \\
& \times \delta(f - (qf_o + rf_x)).
\end{aligned}
\tag{3.18}
$$

The first two terms are scaled by $2N$, and now the last exponential term is a sum of equidistant phases (the phase shift due to the ϕ_S is constant for all), therefore, it will cancel out unless q is equal to a multiple of $2N$. This implies that sidebands that were before around f_o and its multiples (for a single bit VCO), are now at $2Nf_o$ and its multiples. Therefore, it is expected a better result in regard to the maximum SNDR achievable because the infinite sum of the power of the sidebands falling into the signal band will be much less. It should be noted that only sidebands are affected, the other terms of equation (3.18) are just scaled.

Figure 3.7 shows 6 equidistant phases corresponding to use the circuit of figure 3.6 to a ring oscillator composed by three inverters. Because the equivalent model presents 6 single bit VCOs with equidistant phases, these phases will shift its position and keep canceling out each other, unless q is a multiple of 6, only then they will all collapse in 0 (it is considered that the initial phase is 0).

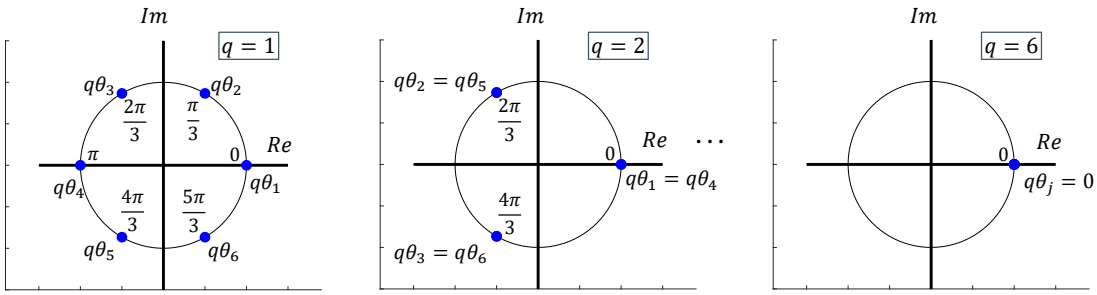


Fig. 3.7. Geometrical example for the cancellation of the phases when $N = 3$.

The equivalent spectrums of VCOp and VCOn are now known and its subtraction can be calculated by means of inspection of equation (3.18) and noting that the difference between the set of VCOs resides in ϕ_S. The first term will cancel out, the second one will be doubled because the phase shift of π on the input signal, it can be thought of the geometrical sum of the vectors on the complex plane, this is represented in figure 3.8, where it is shown that the equivalent vector results in the first vector being doubled in

both real and imaginary axis. The last term is less intuitive as it magnitude depends on several values; however, it is noted that the importance is that the sidebands go to $2N$. Normalizing the final output to $[1, -1]$ and assuming both set of VCOs have the same initial phase, the spectrum $P_n(f)$ is finally given by:

$$\begin{aligned} P_n(f) &= 4T_s A k_{vco} e^{i\phi_S} e^{-i\pi T_s f_x} \frac{\sin(\pi T_s f_x)}{\pi T_s f_x} \delta(f - fx) \\ &+ \frac{2}{N} T_s f_o \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} J_r\left(\frac{q A k_{vco}}{f_x}\right) \frac{\sin[\pi T_s (q f_o + r f_x)]}{\pi T_s q f_o} \\ &\times e^{-i\pi(q f_o + r f_x) T_s} \\ &\times e^{ir\phi_S} e^{-iq\frac{A k_{vco}}{fx}\sin(\phi_S)} \left(1 - (-1)^r e^{2iq\frac{A k_{vco}}{fx}\sin(\phi_S)}\right) \sum_{j=1}^{2N} e^{-iq\theta_{VCO,j}} \\ &\times \delta(f - (q f_o + r f_x)). \end{aligned} \tag{3.19}$$

It is noted that if the initial phases of both set of VCOs are different, each set would present an equation derived from (3.18). Subtracting one from the other, would yield the same first two terms as (3.19) while the third one would be hard to reduce; however, as shown in equation (3.18), each set of VCO would present its first sideband at $2Nf_o$. Because the Fourier Transform is linear, no additional components will be generated that weren't already present when subtracting one from the other.

Thus, the equations that describe a practical implementation of the open loop VCO-based quantizer of figure 3.6 were given.

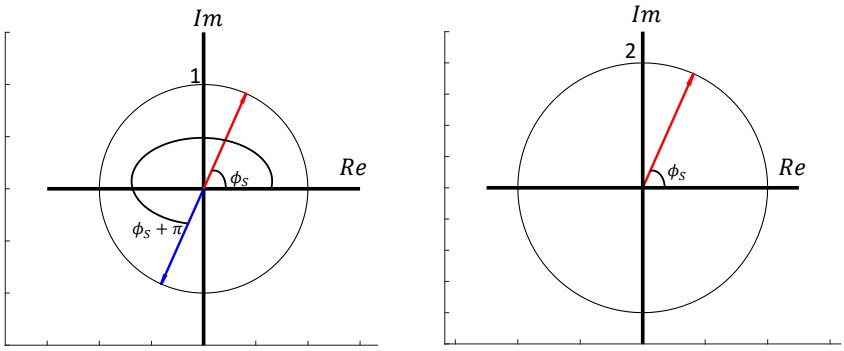


Fig. 3.8. Geometrical demonstration for the doubled power for the component at f_x of equation (3.19) when input signals with a phase shift of π are subtracted one from the other.

3.2.2. VCO-based integrator

It is also possible to build an integrator with a VCO and understanding it by means of the PFM model. The signal $d(t)$ is now connected to an integrator (figure 3.9). It can be seen that when integrating equation (3.9) it results in the first constant term mapped into a growing term with time, thus, in order to cancel it a differential architecture can be used.

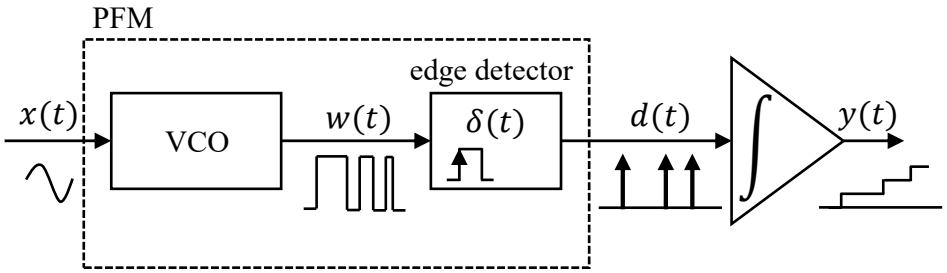


Fig. 3.9. VCO as a pulse frequency modulator followed by an integrator.

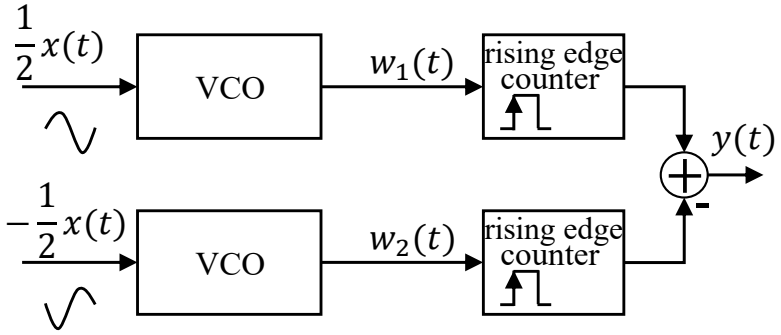


Fig. 3.10. PFM Integrator - Differential implementation using counters.

Figure 3.10 shows a possible implementation of the integrator, that it is, each counter adds 1 on its corresponding VCO rising edge, and then a subtraction is performed, yielding in the cancellation of the growing term. Assuming $\alpha = 0$ and $\phi_S = 0$, from [31] it is known that the output $y(t)$ is given by:

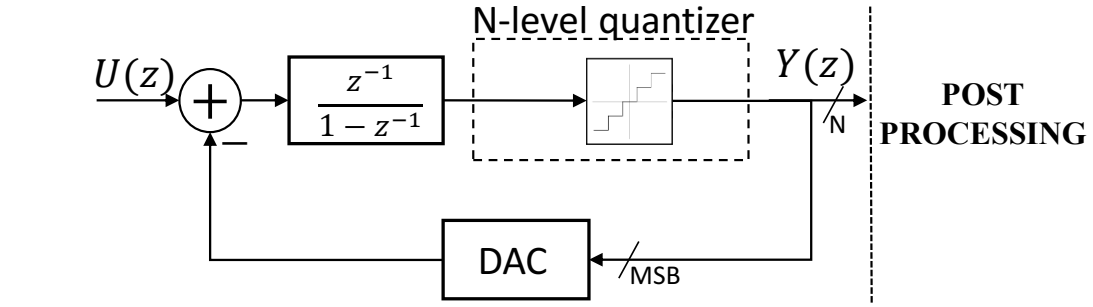
$$\begin{aligned} y(t) = k_{vco} &\int_0^t x(\tau)d\tau \\ &+ f_o \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} J_{2r+1}\left(\frac{qAk_{vco}}{f_x}\right) \frac{1}{\pi(qf_o + (2r+1)f_x)} \\ &\times \left(1 + \frac{(2r+1)f_x}{qf_o}\right) \sin(2\pi(qf_o + (2r+1)f_x)t). \end{aligned} \tag{3.20}$$

It is observed that even modulation tones around each sideband are eliminated; however, this only happens when $\phi_S = 0$. If instead of using a single bit VCO differential architecture, a N odd number of ring oscillators are connected to a counter structure, the phases of the VCOs would be equidistant so it follows naturally that the sidebands, as it was the case for the VCO-based quantizer, will cancel out but for multiples of qN. This architecture will be used as a foundation to understand another architecture that will be studied in chapter 4.

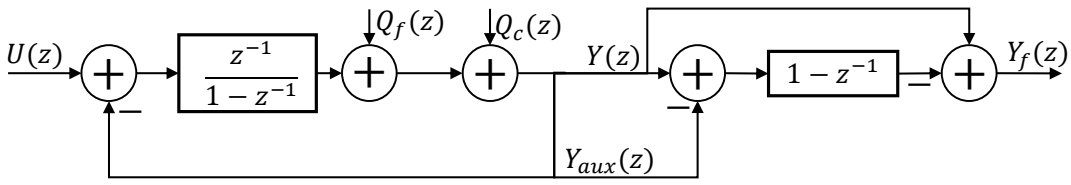
3.3. Bit-Split - Introduction

As stated in the previous chapter, real implementations suffer from the non-linearity of the VCO and the limit of a practical first-order noise shaping. Therefore, a closed-loop system is used in order to mitigate issues related to non-linearity or just to increase the order of the system and so the SNDR. However, closed-loop systems present some disadvantages over the open loop ones: stability, jitter, DAC mismatch, etc... The proposed technique has as objective to reduce the number of DAC elements, and thus the area and complexity of it.

The Bit-Split technique was first proposed by [36] in order to solve issues related with the DAC mismatch, as for then techniques to mitigate this issue for multibit DAC were not so developed as they are now [37]–[39]. It was implemented in a discrete-time ΔΣ modulator. Figure 3.11 shows a first order ΔΣ and its linear equivalent, both normalized to Ts = 1 without loss of generality.



(a)



(b)

Fig. 3.11. Leslie&Singh architecture for a discrete-time ΔΣ modulator and its linear model.

The output $Y_f(z)$ of the linear model is given by the following equation:

$$Y_f(z) = U(z)z^{-1} + Q_f(z)(1 - z^{-1}) \tag{3.21}$$

The system presents a fine and a coarse quantization (1 bit in [36]), being the latter the one that goes into the feedback path; making some operations on the system, it is possible to make the final output to be composed only by the fine quantization because the coarse one can be eliminated. For that, it is mandatory to know the transfer function

of the whole system because only then the coarse noise can be theoretically eliminated, assuming white noise spectrum for both quantization errors and that the post-processing filter (PPF) matches the transfer function seen by the noise. Actually, for practical purposes, as it will be shown later, in most of the cases an approximation can be used. Hence, as a VCO can be used within a ΔΣ modulator as a quantizer, it is possible to apply this technique to VCO-based ADC architectures to reduce the number of DAC elements.

For instance, in order to use a 65 taps VCO in a closed-loop architecture, it is necessary to have a DAC of 65 elements, that is, 6 bits. But, if instead of using all taps into the feedback path, only few of them are used, this eases the DAC design, power consumption and calibration. As it happens with the model of figure 3.11 it will also be expected to improve the SNDR because the coarse noise is eliminated. Therefore, a study is necessary on how this technique can be implemented on different architectures using VCOs.

Two architectures will be the scope of study, frequency-feedback and phase-feedback architectures.

3.3.1. VCO-based quantizer

This architecture can be implemented as an open loop system as depicted in figure 3.6 or within a closed-loop system as in figure 3.12. The former is of no interest because there is no feedback path and therefore the bit-split technique cannot be applied. Thus, the focus is on its use on a closed-loop architecture. It should be noted that the filter that goes before the VCO will be considered to be at least an integrator-like. An implementation of the bit-split technique to a first-order closed-loop architecture is presented in [40].

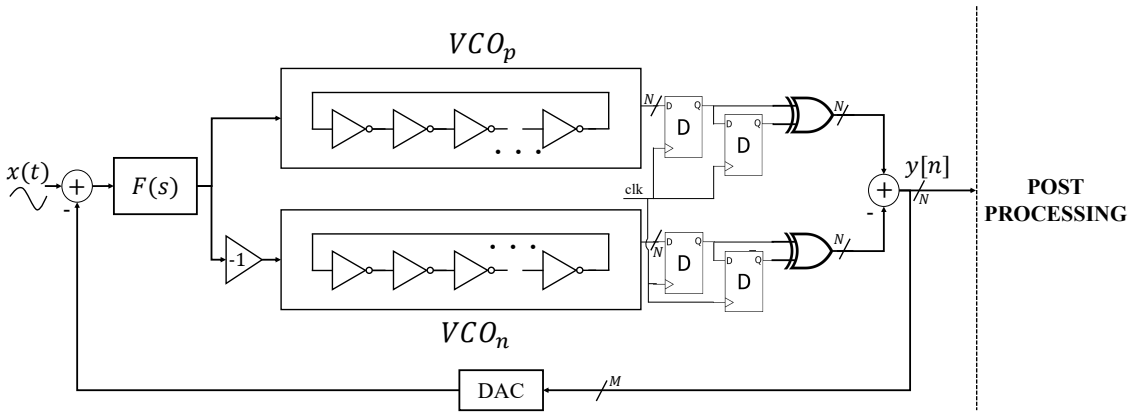


Fig. 3.12. Closed-loop ΔΣ ADC using a VCO-based quantizer.

This architecture is also known as closed-loop ΔΣ using VCO-based quantizers. It presents the following features:

- Advantages: nth order noise shaping but the loop is $(n-1)$th order. This implies that higher SNDR values can be achieved in comparison to a conventional CT-ΔΣ modula-

tors which don't use VCO-based quantizers, without sacrificing stability, as is known that higher order loops are more prone to instability [6]. It presents intrinsic Data Weight Averaging (DWA) [25], which means that it shapes the error produced by the DAC; however, DWA is lost for differential architectures.

- Disadvantages: To exercise the full dynamic range, its input normally has to be large and that produces distortion provoked by the VCO non-linearity that in some cases can degrade seriously the SNDR performance. Its maximum oscillation frequency is limited to $f_s/2$ [31].

3.3.2. VCO-based integrator

Figure 3.13 presents an architecture called closed-loop ΔΣ using VCO-based integrator. This architecture makes use of two set of VCOs receiving half the value of the input, being one also negative. Then, at sampling instants an XOR operation is performed to the VCOs, the XOR acts as a phase detector. It is noted that whereas in the previous architecture, the output was the frequency, here it is the phase. Because phase is the integral of frequency, the input voltage to the VCO-based integrator will be small in comparison with the input to the VCO-based quantizer.

- Advantages: It presents Intrisic Clocked Averaging (CLA) [41] in differential architectures. Its input level is small and can avoid loss of SNDR due to the VCO non-linearity.

- Disadvantages: In comparison with the VCO-based quantizer, for the same number of taps on the VCOs, its SNDR is about 6dB less and the order of the loop is not decreased.

Figures 3.12 and 3.13 will be referred from now on as frequency feedback and as phase feedback architectures.

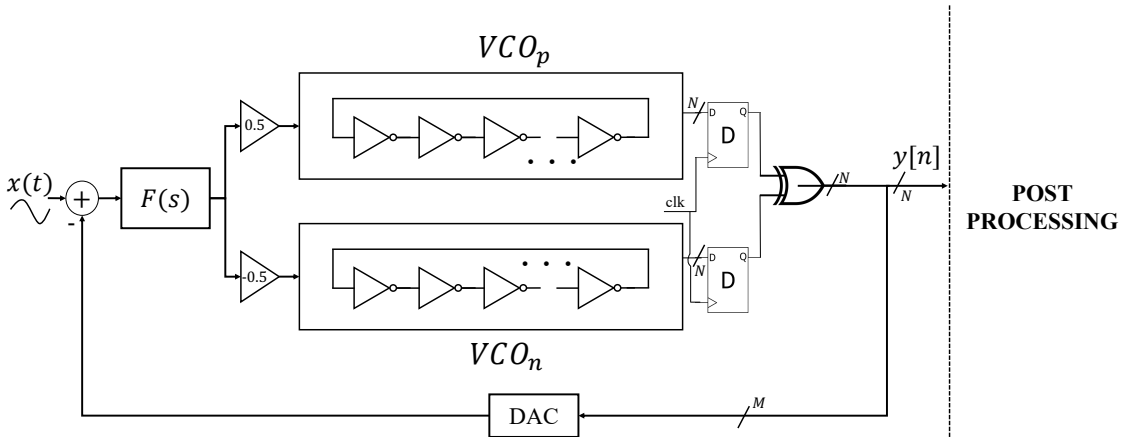


Fig. 3.13. Closed-loop ΔΣ ADC using a VCO-based integrator.

To apply this technique to these architectures implies using a feedback path that only selects a few lines of the output. And with a post-processing filter and some operations, it is desired to obtain an equivalent output spectrum as if all the taps were in the feedback path. Achieving so would enable to build a system containing a VCO as large as possible. However, such equivalence can never be reached, for as studied before, the sidebands produced by the VCO, that would conform an alike white noise spectrum when sampling, depends on the input and thus is not white as the assumption made for figure 3.11. Hence, dynamic of the loop plays an important role because, in contrast to systems depicted in figure 3.12 and 3.13, the VCOs considered do not the see the signal $x(t)$, for they are in a closed-loop system. Thus, if few taps are considered into the feedback loop, the input to the VCOs will be larger than if all taps were used, and consequently the modulation spectrum is *worse* on the former case but depending on the number of taps it can affect more or less the SNDR that can be recovered by applying the bit-split technique. However, the sidebands would be placed on the same frequencies although their magnitudes will differ. The scope of the study is on: a second order frequency feedback architecture; first and second order phase feedback architecture.

4. THEORETICAL STUDY OF THE BIT-SPLIT TECHNIQUE

In this chapter, theoretical analysis is presented for a second order frequency feedback bit-split architecture, and a first and second order phase feedback architectures, based upon the previous study of the VCO-based quantizer and VCO-based integrator. Study will focus onto how apply the bit-split technique for each architecture, regarding its linear models and the criterion for the phase selection.

4.1. Frequency feedback architecture: second Order

A second order frequency feedback system is represented in figure 4.1, it consists of substituting the filter $F(s)$ of figure 3.12 by an integrator with a given gain. As the objective is to use less elements on the feedback path, instead of using a second feedback path, a feedforward path is placed instead; it does not affect what on a conventional $\Delta\Sigma$ would be the NTF, it only changes the STF. The block $P(s)$ denotes the DAC response of the system, that is, its output waveform and the time between a sample is received and an output is produced. Thorough all the text, the output waveform will be considered to be a NRZ pulse of width T_s, that is, no delay and each input value is mapped proportionally to the output.

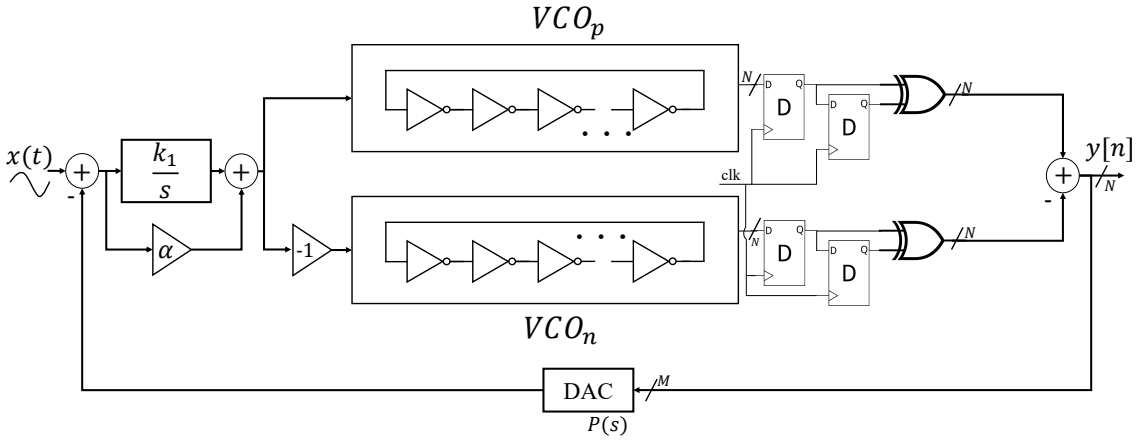


Fig. 4.1. Second order $\Delta\Sigma$ modulator using a VCO-based quantizer.

4.1.1. Linear Model

In order to use the bit-split technique effectively, the loop filter transfer function must be known. Going back to equation (3.19), one can realize that the second exponential term and the sinc normalized function that are with the component at the frequency f_x, are indeed an integrator followed by a first difference (equation (4.1)). Also, by manipulating

the sine and the first exponential of the second term, the equivalence of equation (4.2) is found.

$$e^{-i\pi T_s f}\frac{\sin(\pi T_s f)}{\pi T_s f} = \frac{1}{sT_s}(1 - e^{-sT_s}) \tag{4.1}$$

$$2ie^{-i\pi T_s f}\,sin(\pi T_s f) = (1 - e^{-sT_s}) \tag{4.2}$$

Defining $E(s)$ as the sideband terms in equation (3.19) but applying the substitution of equation (4.2), a linear model can be obtained. Taking into account the sampling, the circuit of figure 3.6 can be decomposed as follows, the input $X(s)$ is integrated with a gain equal to k_2, then it's added $E(s)$, sampling is performed and then the first difference is applied. These transfer functions represent exactly the behavior of figure 3.6. It is noted that the gain k_2[7] is given by equation (4.3) when substituting equation (4.1) into (3.19). $E(s)$ can be thought of as the quantization noise in a conventional $\Delta\Sigma$ modulator. Thus, once all the transfer function are known, it is possible to obtain $NTF(z)$.

$$k_2 = 4k_{vco} \tag{4.3}$$

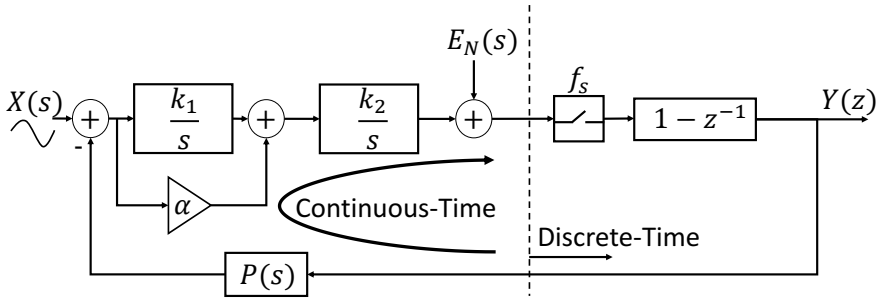


Fig. 4.2. Linear model for the second order $\Delta\Sigma$ ADC using a VCO-based quantizer when all the phases are used in the feedback path.

Figure 4.2 depicts the equivalent linear model of figure 4.1. The NTF is the transfer function seen by the noise, in this case $E(s)$. Because it's a hybrid system, that is, continuous time but with clocked feedback, the output $Y(z)$ only sees the response of the continuous-time loop filter at sampling instants; such system is considered from right after $P(s)$ to before sampling is performed. Therefore, a continuous-to-discrete time transformation must be performed on the loop transfer function. As stated, the equivalent discrete transfer function only needs to match the continous-time filter at sampling instants, this transformation is called Symbol Pulse Invariance [42]. The continuous-time loop filter, $H(s)$, of figure 4.2 is the following:

$$H(s) = k_{2N}\frac{\alpha s + k_{1N}}{s^2} = k_{2N}\left(\frac{\alpha}{s} + \frac{k_{1N}}{s^2}\right). \tag{4.4}$$

[7]It is supposed that the full scale input amplitude is 1. If it weren't the case, k_2 needs to be scaled following the full scale voltage of the input, that is, $k_2 = 4v_{fs}k_{vco}$.

Assuming there is no ELD, the equivalent discrete-time loop filter is:

$$H_d(z) = k_{2N}\frac{\left(\alpha + \frac{k_{1N}}{2}\right)z^{-1} + \left(-\alpha + \frac{k_{1N}}{2}\right)z^{-2}}{(1 - z^{-1})^2}, \tag{4.5}$$

where k_{1N} and k_{2N} refer to the 1 Hz normalization of k_1 and k_2. Hence, the equivalent discrete-time transfer function needed for the post-processing is now known.

4.1.2. Selection of Phases

Before jumping into the post-processing, it is important to select the correct lines of the VCO that will go into the feedback path. As seen in the previous chapter, the output of a VCO-based quantizer consists of a fundamental component located at f_x and infinity sidebands centered at multiples of $2Nf_o$. These sidebands were effectively located around multiples of $2Nf_o$ because the equivalent single bit VCO model shows that only then their components do not cancel out. Therefore, to understand this is key for it is what enables a successful implementation of the bit-split technique.

Figure 4.3 shows the equivalent model from substituting the N inverters by a set of $2N$ single bit VCOs. This way, it is shown that it is possible to isolate those inverters that are not going into the feedback path. Because it is a closed-loop system, it is desired that the power of the sidebands produced by the VCOs is low, this implies that the first one should be located the furthest possible, and this can only happen when the selected phases are equidistant, otherwise these sidebands will only suffer from attenuation but not from frequency shift [8].

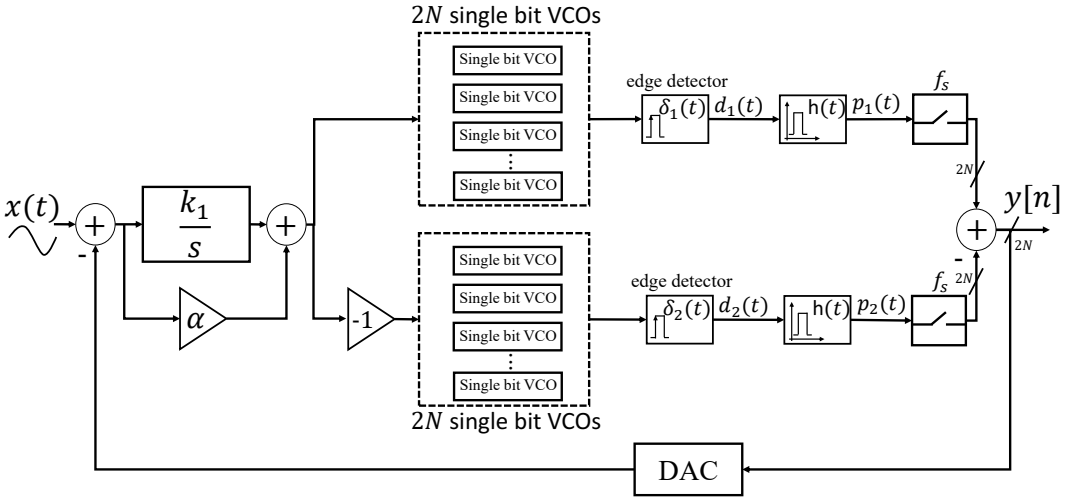


Fig. 4.3. PFM model as $2N$ single bit VCOs model for the second order frequency feedback architecture.

[8]The term frequency shift when applied to the sidebands also implies a change in magnitude due to equation (3.19)

Consequently, if the loop does not see the inverters that are not selected, the equivalent model in figure 4.4 differs from figure 3.11. Nevertheless, the post-processing analysis is similar. $E_M(s)$ refers to the sidebands produced by the M taps going into the feedback path, whereas $E_N(s)$ refers to the sidebands produced by all the taps of the VCO. It is noted that the equivalent model implies that even though the same input signal is being fed to all VCO inverters, only the spectrum of the sum of those that are in the feedback path will present second-order noise shaping.

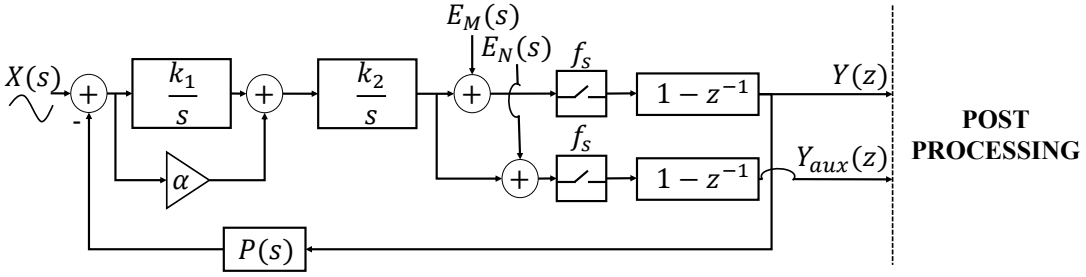


Fig. 4.4. Linear model for the second order frequency feedback architecture when applying the bit-split technique.

Given all the above, it follows that M must be a divisor of N, for only then it is possible to select equidistant phases that would produce a frequency shift which results into less power from the sidebands going into the feedback path. The minimum value of M needs to assure system stability and it also should avoid saturation of the VCO input.

4.1.3. Post-Processing Analysis

The post-processing scheme is depicted in figure 4.5. It is desired that the final output only presents spectrum components due to $E_N(s)$. Working out the operations, the signal $Y_f(z)$ is found to be:

$$Y_f(z) = [STF(s)X(s)]^* + NTF(z)[E_M(s)]^* - PPF(z)(1 - z^{-1})[-E_N(s) + E_M(s)]^*, \quad (4.6)$$

where [.]* is the sampling operator. For the block diagram depicted figure 4.2, the NTF is as follows:

$$NTF(z) = \frac{1 - z^{-1}}{1 + H_d(z)(1 - z^{-1})}. \quad (4.7)$$

Therefore, in order to eliminate $E_M(s)$ from the final output, it is necessary that $PPF(z)$ follows equation (4.8), because only then $Y_f(z)$ won't present the sidebands produced by $E_M(s)$ as shown in equation (4.9).

$$\begin{aligned} PPF(z) &= \frac{NTF(z)}{1 - z^{-1}} = \frac{1}{1 + H_d(z)(1 - z^{-1})} \\ &= \frac{1 - z^{-1}}{1 + \left(1 + k_{2N}\left(\alpha + \frac{k_{1N}}{2}\right)\right)z^{-1} + k_{2N}\left(-\alpha + \frac{k_{1N}}{2}\right)z^{-2}}. \end{aligned} \quad (4.8)$$

$$Y_f(z) = [STF(s)X(s)]^* + NTF(z)[E_N(s)] \tag{4.9}$$

Consequently, $Y_f(z)$ will present sidebands at multiples of $2Nf_o$ instead of $2Mf_o$, resulting in better SNDR, the same expected SNDR for a system with N inverters in the feedback path.

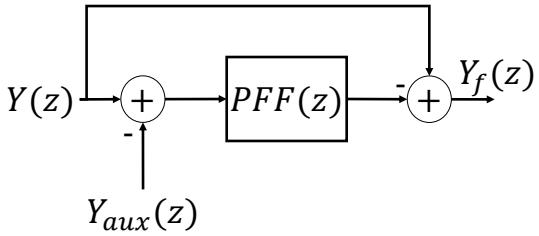


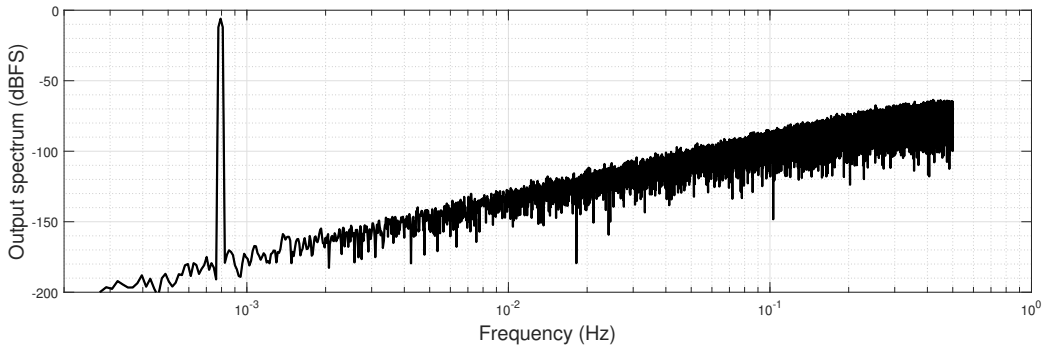
Fig. 4.5. Block diagram for the post-processing scheme.

As an example, figure 4.6 represents two FFT of 32768 points for two systems with and without applying the bit-split technique whose parameters are in table 4.1. It is shown that the post-processing scheme, as expected, recovers the SNDR and changes the output spectrum magnitude at all frequencies, for they only contain now the power equivalent to the sidebands being at $2Nf_o$.

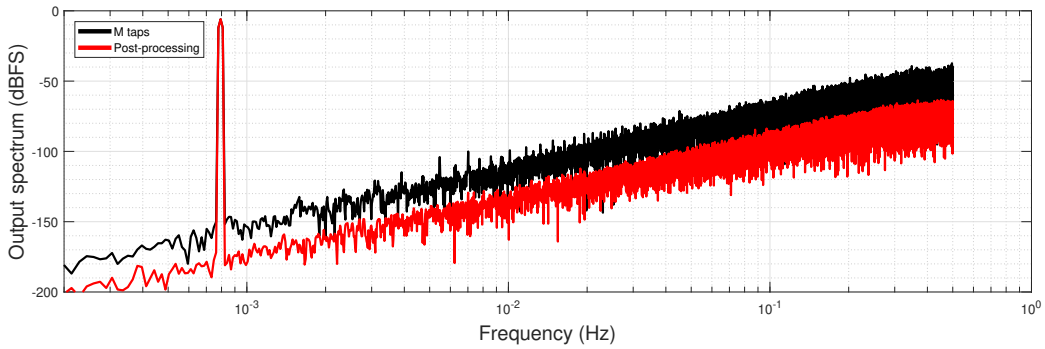
Parameter	Value	Parameter	Value
f_s	1 Hz	k_{vco}	$f_s/4$
OSR	32	f_o	$f_s/4$
ELD	0	N	90
k_1	1	M	6
α	0.5	f_x	BW/150

Table 4.1. SECOND ORDER FREQUENCY FEEDBACK ARCHITECTURE PARAMETERS.

BW is the bandwidth. It should be noted that in practical applications, f_o values are similar to the one in table 4.1, implying that in most of the cases when using a multiphase VCO, all the sidebands will be aliased and possibly no longer distinguishable from a noise-shaped white noise spectrum. Moreover, taking into account that VCOs are composed by several inverters that pushes further away the first sideband, only in certain conditions these sidebands can be observed. For instace, for the parameters of table 4.1, the first sideband will be located at $3f_s$ which alias into fs, that is, it will be suppressed because the magnitude of equation (4.2) around multiples of f_s is very low. Moreover, all sidebands are located at multiples of f_s.



(a)



(b)

Fig. 4.6. Output spectrums for an input of −6 dBFS (a) when all taps are in the feedback path, and (b) when only M taps in the feedback path with its corresponding post-processing scheme. The SNDR is 97dB in both cases.

Parameter	Value	Parameter	Value
f_s	1 Hz	k_{vco}	$f_s/64$
OSR	32	f_o	$f_s/64$
ELD	0	N	15
k_1	1	M	5
α	0.5	f_x	BW/150

Table 4.2. ALTERNATIVE SECOND ORDER FREQUENCY FEEDBACK ARCHITECTURE PARAMETERS.

To prove that the frequency shift only happens when an adequate filter following (4.8) is used, figure 4.7 shows three output spectrums for a system whose parameters are in table 4.2[9]. The first spectrum is obtained with all phases, the second and third ones present the bit-split technique, the second using the PPF as in table 4.2 while the third uses a very

[9]Parameters of table 4.2 would never be used in a real system because its values are too low to get a reasonable SNDR. The example has the only purpose to show the frequency shift of the sidebands; in a well designed system, there would be no a first sideband to look at.

rough approximation $(1 - z^{-1})$. The results are evident, while the second spectrum shifts its sidebands to $2Nf_o \approx 0.45$ Hz as expected when applying the post-processing scheme, the third does not do so (first sideband is at $2Mf_o \approx 0.15$ Hz). Nevertheless, the SNDR values obtained from the three spectrums are indeed similar as the in-band noise is similar as well. This last observation will be discussed on the next chapter.

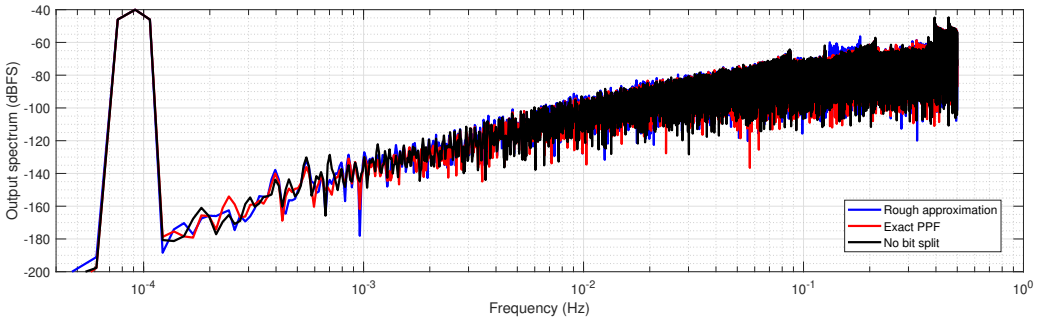


Fig. 4.7. Output spectrums for a system following table 4.2 for an input of −40 dBFS.

4.2. Phase feedback architecture: first and second order

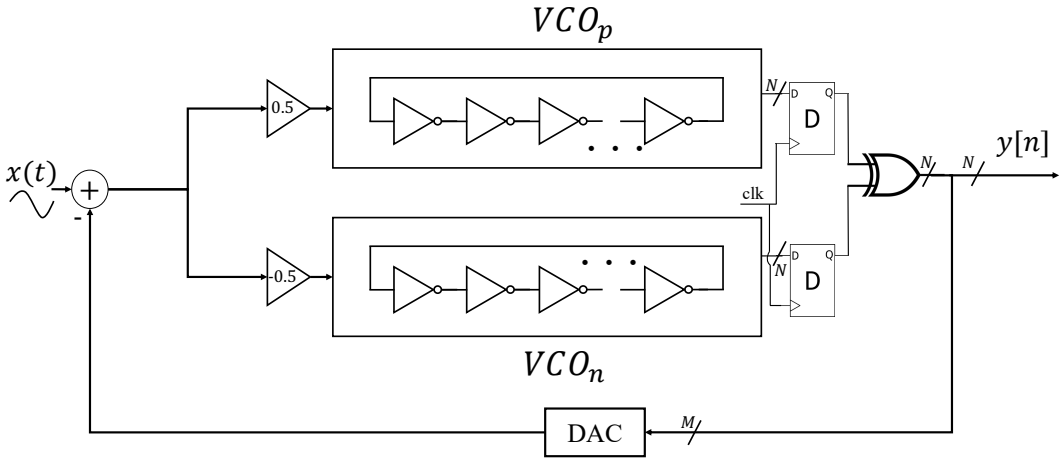
In this section the focus will be on the first and second order phase feedback architectures as depicted in figure 4.8. As in the case for the frequency feedback architecture, for the second order system it is considered a feedforward path instead of a feedback one. Again, this only affects the STF and not the NTF.

4.2.1. Linear model

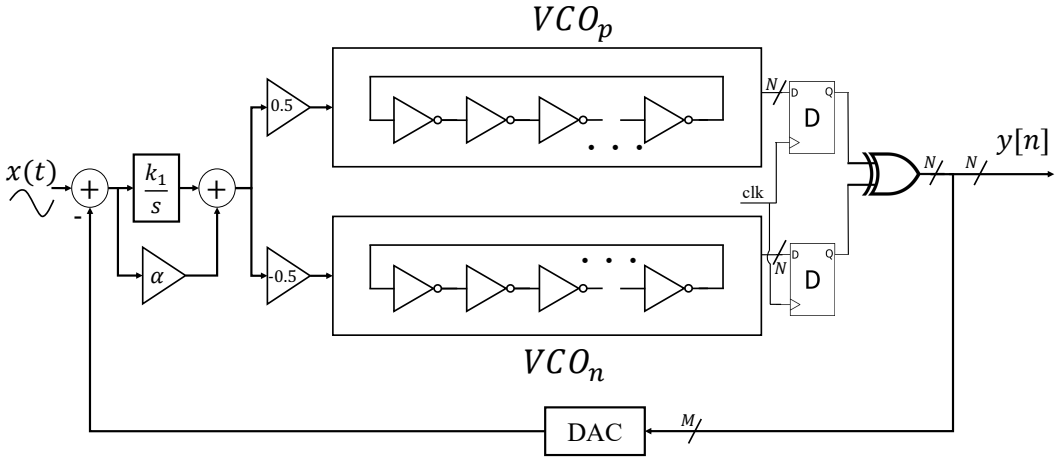
Even though the spectral behavior of this architecture is different from the frequency feedback, crucial insight can be gained by starting from a simple case, that is, supposing a single bit VCOp and VCOn. As depicted in figure 4.8 an XOR operation is performed between each VCO, this operation if thought of as if it were in a open loop configuration, it will be the absolute value of equation (3.20), but replacing each single bit VCO by 2 single bit VCOs having a phase shift of π one from the other. Therefore, the following equation yields:

$$y_{XOR}(t) = |y(t)| = \left| 2k_{vco} \int_0^t x(\tau)d\tau + m_1(t, \theta_{VCO_1}) + m_2(t, \theta_{VCO_2}) \right|, \tag{4.10}$$

where $m_1(t, \theta_{VCO_1})$ represents the second term of equation (3.20) for an initial phase of the VCO_1 of 0, and $m_2(t, \theta_{VCO_2})$ has an initial phase equal to π.



(a)

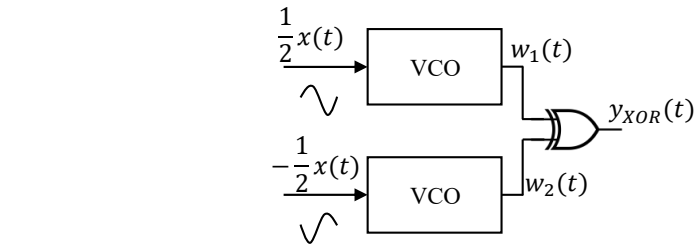


(b)

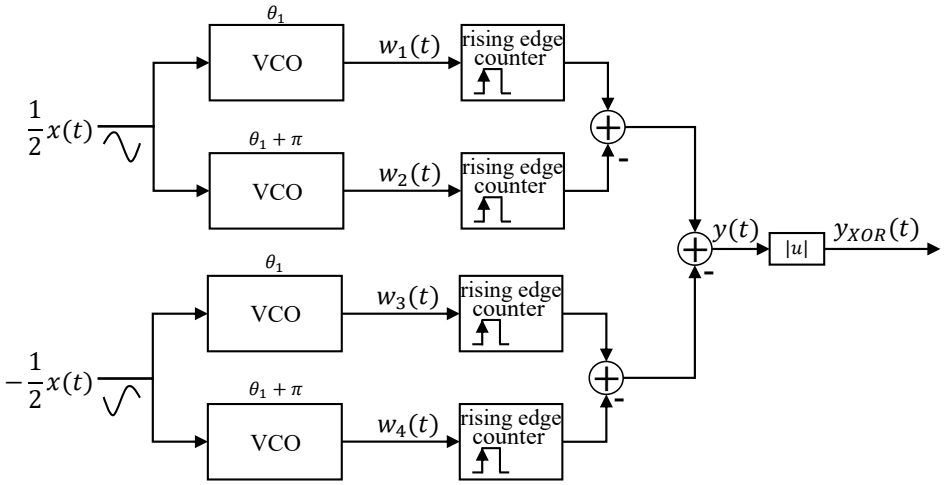
Fig. 4.8. Phase feedback architecture of (a) first order and (b) second order

Figure 4.9 shows the equivalent model based on the PFM for the XOR operation for a single bit VCO. It is observed that when applying the absolute value, the sine wave resulting from the integrator operator over the considered signal, $x(t)$ (input signal to the VCO as in figure 4.9), will be transformed into a infinite sum of decaying sines. Thus, the original signal is lost and an infinite number of harmonics are introduced. However, as the XOR operation is within a loop, the signal that feeds the VCO makes the integration to have no negative values, consequently, it is possible to omit the absolute value and just use (3.20). Therefore, the VCO + XOR operation of figure 4.8 can be substituted by an equivalent model of counters that react to the rising edges of $2N$ single bit VCOs.

If considering that the full scale voltage of the input signal is 1, the signal produced by the DAC must be on the nominal range $[-1, 1]$. The XOR operation results in N signals being 1 or 0 that for simplicity are assumed to be summed before reaching the DAC, thus, the input signal to the DAC is bounded within $[0, 30]$, therefore, in order to reach the nominal range, the input signal to the DAC must be multiplied by $2/N$ and subtracted 1. Hence, the equivalent linear model follows naturally and it is represented and depicted in



(a)



(b)

Fig. 4.9. (a) Open loop VCO + XOR operation and (b) its equivalent model based on pulse frequency modulation.

figure 4.10 and figure 4.11. It consists of substituting the VCO + XOR operation by an integrator of gain k_2 and then summed with the sidebands defined in equation (3.20). The gain k_2 is also defined by equation (4.3) even if such systems are different, because the normalization to $[-1, 1]$ and the equivalent $2N$ single bit VCOs model, the same equation yields. As opossed to the frequency feedback architecture, now sidebands are now being fed directly into the output. Denoting as $H_1(s)$ the continous-time loop filter for the first order system and by H_{1d} its discrete-time equivalent:

$$H_1(s) = \frac{k_2}{s} \tag{4.11}$$

$$H_{1d}(z) = k_{2N}\frac{z^{-1}}{1 - z^{-1}} \tag{4.12}$$

$H_2(s)$ denotes the continuous-time loop filter for the second order system, it follows equation (4.4) and so its equivalent $H_{2d}(z)$. Both equivalent discrete transfer function have been defined.

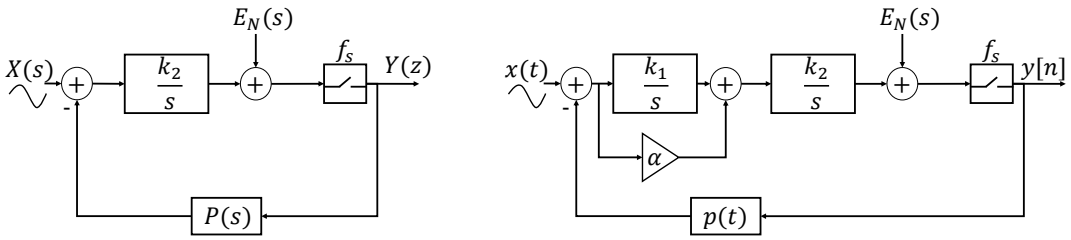


Fig. 4.10. Linear models of (a) first-order and (b) second order phase feedback architectures.

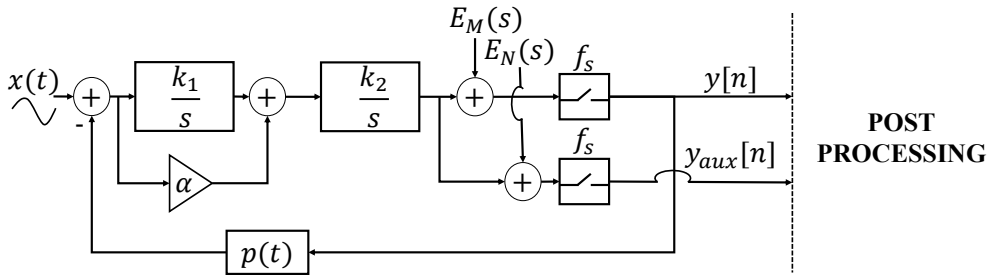


Fig. 4.11. Linear equivalent model when applying the bit-split technique for the second order system.

4.2.2. Selection of Phases

Considering that this architecture can also be seen as $2N$ single bit VCOs per branch, it follows naturally that sidebands are only present at multiples of $2Nf_o$ as it was the case for the previous architecture. Therefore, the best results are met when there are M taps present on the feedback path, being M a divisor of N. Also, the system can be modeled as in figure 4.11, where the loop does not see the taps that are not in the feedback loop. Hence, the same rules for the frequency feedback architecture do apply here: only equidistant phases should be considered into the feedback loop, because otherwise no frequency shift but only attenuation will occur. Therefore, the conclusions obtained from the frequency feedback architecture hold. In this case the minimum value of M is critical, not only because stability but for the correct operation of the XOR, because it acts as a phase detector, if M is too low, system dynamics might lead to a desynchronization of both VCOs.

4.2.3. Post-processing analysis

The post-processing scheme depicted in figure 4.5 is still valid for this architecture. It is noted that the only difference with respect to the frequency feedback architecture is that there is no first difference before the output and consequently the PPF matches the NTF. Equation (4.13) represents $Y_f(z)$ which is the signal after the post-processing is performed.

For the block diagram depicted in figure 4.10, the NTF is given by equation:

$$Y_f(z) = [STF(s)X(s)]^* + NTF(z)[E_M(s)]^* - PPF(z)[-E_N(s) + E_M(s)]^*, \tag{4.13}$$

$$NTF(z) = \frac{1}{1 + H(z)} \tag{4.14}$$

Given that only first and second order systems are considered, and dealing with a null ELD, the post-processing filters for the first and second order take the following expressions:

$$PPF_1(z) = NTF(z) = \frac{1}{1 + H_{1d}(z)} = k_{2N}\frac{z^{-1}}{1 - z^{-1}}. \tag{4.15}$$

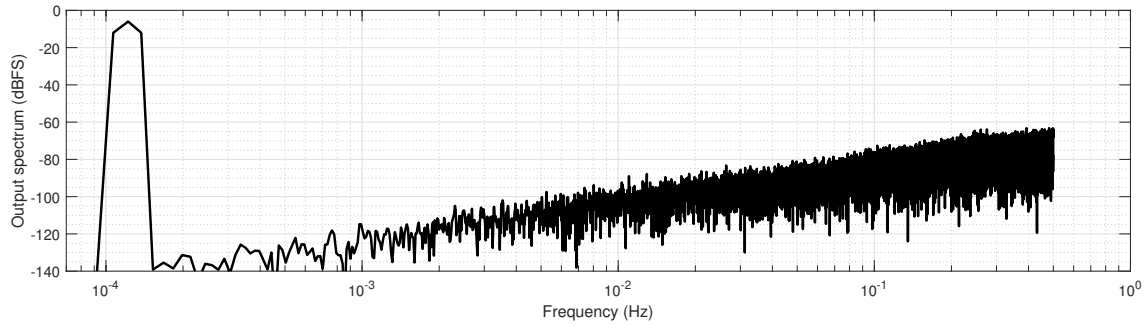
$$PPF_2(z) = NTF(z) = \frac{1}{1 + H_{2d}(z)} = \frac{(1 - z^{-1})^2}{k_{2N}\left(\left(\alpha + \frac{k_{1N}}{2}\right)z^{-1} + \left(-\alpha + \frac{k_{1N}}{2}z^{-2}\right)\right) + (1 - z^{-1})^2} \tag{4.16}$$

Therefore, if the above equations are used when applying the post-processing scheme, equation (4.9) will result.

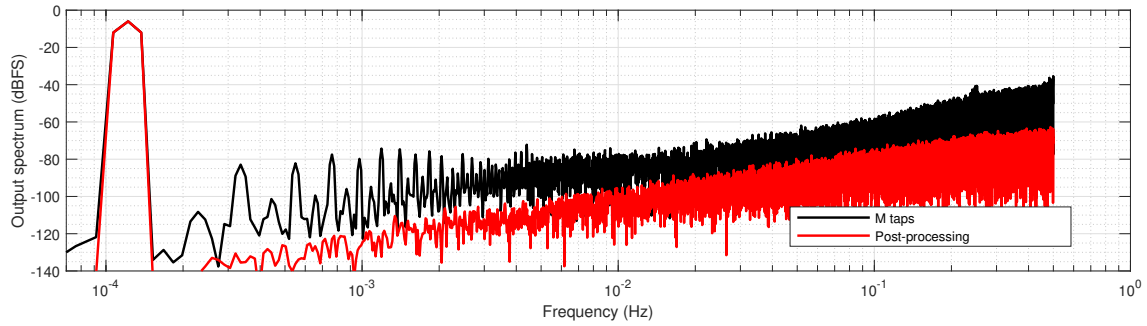
As an example, figure 4.12 presents four 32768 point FFT plots for a first and second order architectures whose parameters are defined in table 4.3. It is shown that the SNDR is recovered, 68dB and 87 dB for the first and second order systems, the input level is -6 dBFS and -10 dBFS respectively. A reduction of magnitude is produced at all frequencies, implying that both, $PPF_1(z)$ and $PPF_2(z)$ are correct. Also, it is observed that the modulation tones produced in figure 4.12b that are within the bandwidth of interest are eliminated when applying the post-processing, implying that the bit-split technique effectively produces the sidebands frequency shift.

Parameter	Value	Parameter	Value
f_s	1 Hz	k_{vco}	$f_s/4$
OSR	32	f_o	$f_s/4$
ELD	0	N	90
k_1	1	M	$\{6, 10\}$
α	1.5	f_x	BW/300

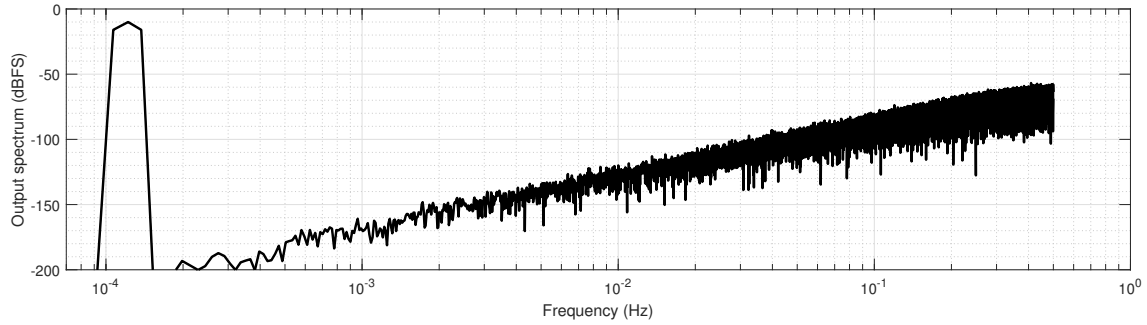
Table 4.3. SECOND AND FIRST ORDER PHASE FEEDBACK ARCHITECTURE PARAMETERS.



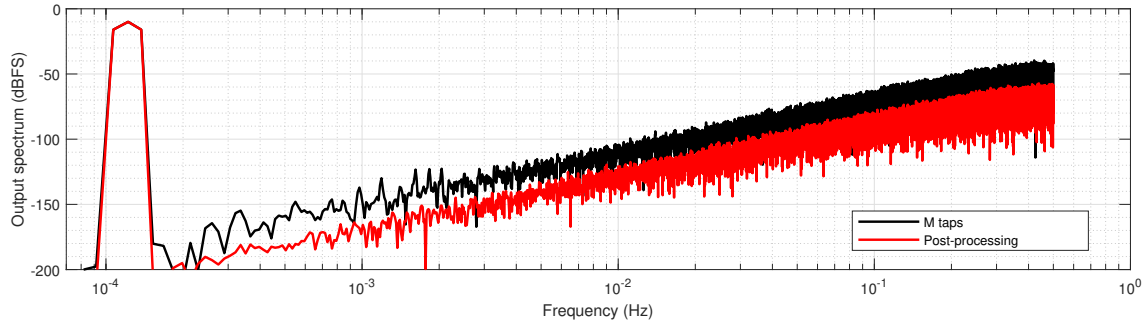
(a)



(b)



(c)



(d)

Fig. 4.12. Output spectrums for (a) first order system with all taps in the feedback path, (b) when only 6 taps are considered. (c) and (d) are the output spectrums for the second order system when 90 and 10 taps are used in the feedback, respectively.

4.3. Extension to a nth order system

So far, only up to second order systems were studied, however, it naturally follows to extend the bit split technique to a *n*th order system. The insights and guidelines developed previously about linear models, phase selection and post-processing scheme still hold whether the system order is 1, 2, or n. As long as the continuous-time open loop transfer function is modeled correctly, and the loop is sufficiently stable for the number of phases selected, there should be no issue in applying the bit split technique to higher order systems. Even so, a brief discussion is given.

- Linear Model: Since only VCO-based quantizers and VCO-based integrators have been considered on the previous study, the *n*th order system will only be composed by them. Therefore, linear models were already presented. It is worth noting the following: if a system is composed by both a VCO-based quantizer and a VCO-based integrator[10], the bit split technique would only be applied to the VCO-based quantizer. Anyhow, for the sake of simplicity, given a n order system, all elements but the last VCO stage can be put into a black box, $H_{BB}(s)$ which would represent its transfer function and by doing so it is omitted whether it contains VCOs or conventional integrators. Therefore, the system can be thought of as if it were the second order case. However, this simplification when a VCO is not part of the last stage is done just to calculate the PPF, its sidebands contributions must be taken into account as for they can possibly affect the VCO on the last stage; furthermore, its sidebands will also be shaped in a way that depends the stage they belong to. Therefore, it is needed to work out its own NTF to be sure whether this arises a problem or not.

- Selection of phases: As for the previous cases, only equidistant phases should be in the feedback path. As the criterion for phase selection is the same whether the last VCO is a based quantizer or integrator, the *n*th order system follows the already settled rules.

- Post-processing analysis: Post-processing analysis: Scheme proposed in figure 4.5 is still valid because the bit split technique it is only applied to the last VCO. As it was the case for the VCO-based integrator and VCO-based quantizer, the loop dynamic is important for it can diminish the expected SNDR and taint the spectrum.

As an example, a third-order system with optimized NTF[11] presenting a VCO-based integrator and a VCO-based quantizer is chosen; this system is presented in [43]. To apply the bit-split technique to this system is very interesting because it presents both

[10] The former being placed at the output, while the latter can be place anywhere for it acts as an integrator.

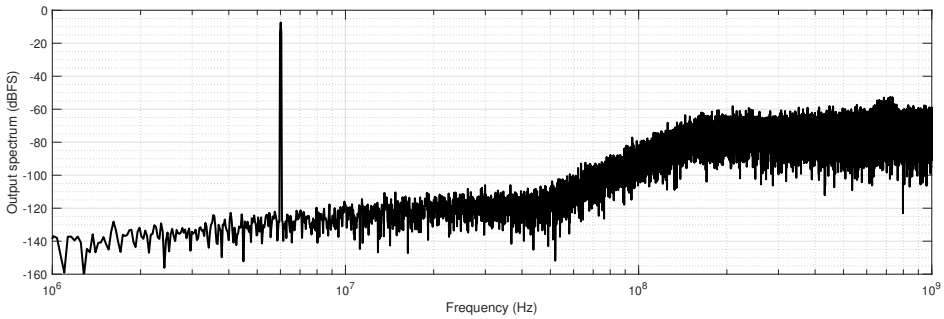
[11] An optimized NTF has complex zeros, thus, the in-band noise can be reduced in comparison to an NTF with only simple zeros.

systems previously presented. Therefore, linear models are of vital importance to mimic the position of the complex zeros on the post-processing scheme.

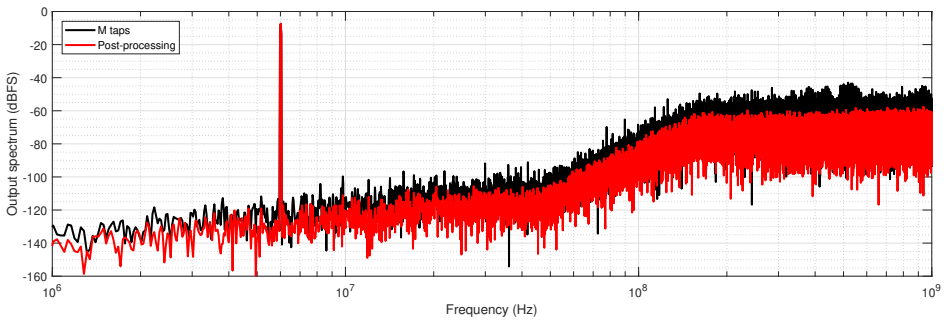
A behavioral simulation is performed following the parameters of table 4.4. A FFT of 32768 points to a system with and without bit-split technique is presented in figure 4.13. It is observed that the SNDR is recovered, and furthermore, the output spectrum is better because there is no hump at high frequencies. The reason behind this is that because only 6 lines were selected, it results in the sidebands being at multiples of 6GHz ($6{\cdot}2{\cdot}f_{o2}$), that is, they are always coincident with the maximum attenuation of the first difference.

Parameter	Value	Parameter	Value
f_s	2 GHz	k_{vco1}	667 MHz/V
BW	60 MHz	f_{o1}	500 MHz
ELD	$0.5T_s$	Elements of 1^{st} VCO	5
k_1	250 Mrads/s	k_{vco2}	500 MHz/V
α	0.375	f_{o2}	500 MHz
β	0.182	N, elements of 2^{nd} VCO	30

Table 4.4. SYSTEM PARAMETERS.



(a)



(b)

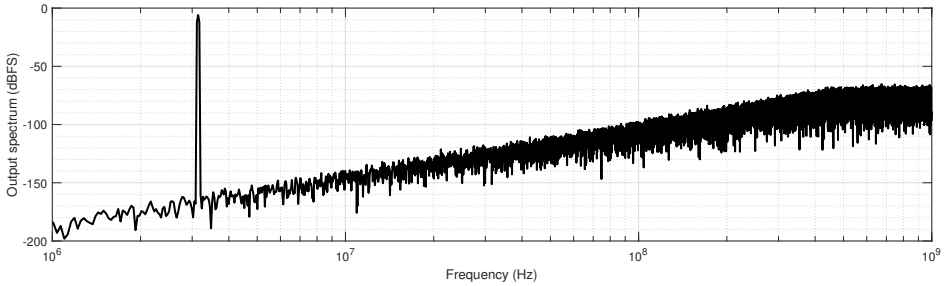
Fig. 4.13. Output spectrums for an input of −6 dBFS(a) when all taps are in the feedback path, and (b) when only 6 lines are in the feedback path with its corresponding post-processing scheme. The SNDR is 76dB in both cases.

5. IMPAIRMENTS AND IMPLEMENTATION STUDY

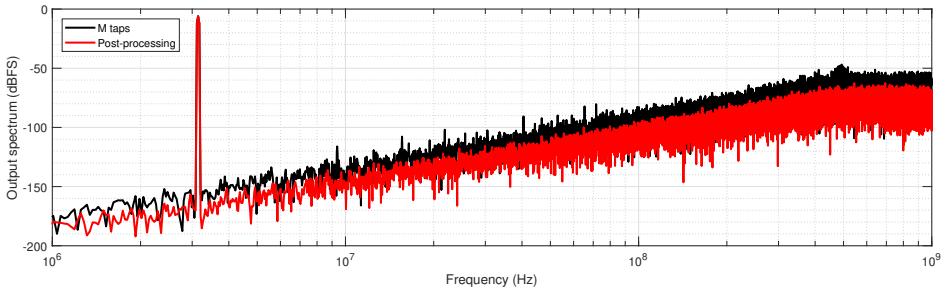
All presented analysis have been hitherto focused on an ideal system with its perfect PPF, no mismatch between the analog and digital sides, no ELD, etc, for it was a theoretical study. In this chapter the focus is on applying a set of impairments in order to know the circuit implementation feasibility of the bit split technique, starting from those related to the technique itself. These impairments will be studied on the second order frequency feedback architecture. Its parameters, unless otherwise is stated, are given by table 5.1. The input level magnitude is considered to be -6 dBFS unless otherwise is stated.

Parameter	Value	Parameter	Value
f_s	2 GHz	k_{vco}	500 MHz/V
BW	83 MHz	f_o	500 MHz/V
ELD	0	N	90
k_1	2 Grads/s	M	15
α	0.25	f_x	BW

Table 5.1. NOMINAL PARAMETERS FOR THE SECOND ORDER FREQUENCY FEEDBACK ARCHITECTURE.



(a)



(b)

Fig. 5.1. Output spectrum for nominal parameters for (a) no bit-split technique and (b) use of bit-split. For both cases the SNDR is 76 dB.

5.1. Implementation of the post-processing scheme

The output data from the VCO presents a thermometric nature, therefore, because the digital side will operate in binary, a thermometric to binary (T2B) converter is needed; several architectures can be used [44]. Figure 5.2 represents a first approach to implement the post-processing part that yields directly from the post-processing scheme. The PPF can be of any order.

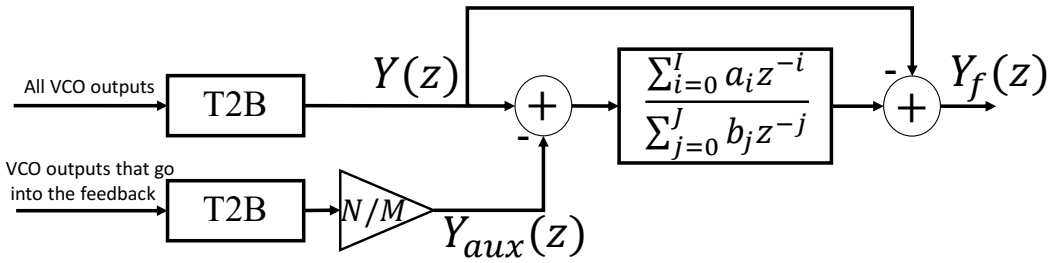


Fig. 5.2. Generic block diagram for the post-processing scheme.

Linearizing the above figure, and using a first difference as the PPF can lead to some serious simplifications on the digital side. Because the first difference has only zeros, that is a Finite Impulse Response (FIR) filter, its implementation is way simpler than if the adequate PPF was implemented, because it would also contain poles, that is a Infinite Impulse Response filter (IIR). The T2B can be implemented using adders. The following figure presents the aforementioned simplification.

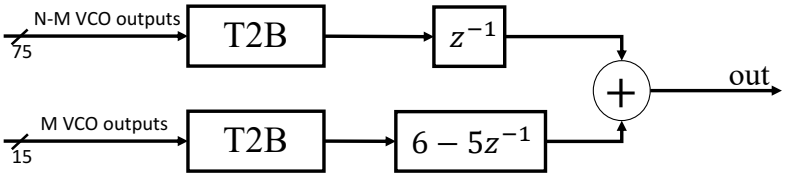


Fig. 5.3. Proposed block diagram for the implementation of the post-processing scheme.

The proposed scheme in comparison to the generic block diagram, it is observed that instead of using a T2B converter that must take as an input 90 and 15 elements, the former can be instead 75 by rearranging operations on the generic block diagram. Because T2B converters are usually big structures of full adders, OR gates, the proposed scheme can spare several transistor, thus, it is expected that the total area is reduced. Figure 5.4 shows the output spectrum for the system of table 5.1 when using a first difference. It is observed that the SNDR is recovered and that the output spectrum is also recovered with some discrepancies at high frequencies. Even though a possible implementation for the digital circuit was given, to do so is out of the scope of this document.

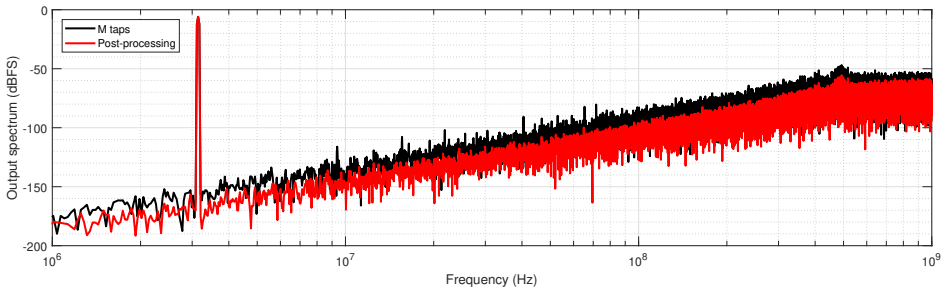


Fig. 5.4. Output spectrum for the system of table 5.1 with a first difference as the PPF. SNDR is 76 dB.

5.2. Analog and digital mismatch

A possible implementation of figure 4.1 is depicted in figure 5.5. The first integrator is implemented by means of a fully differential operational amplifier using resistors and capacitors to obtain the values of table 5.1. However, since R, C and the VCO itself do vary with process and temperature [5], [45], [46], the actual continuous-time loop filter might be different from what it is expected, possibly affecting the post-processing if variations on R, C and VCO do not compensate each other[12], there will be a shift in poles and zeros position and the gain value of the transfer function. Thus, the post-processing filter will not be able to completely cancel the sidebands $E_M(s)$. However, considering that these variations are within the range of 10%, such shift would only affect strongly high frequencies because as the system is considered to be a low pass continuous-time $\Delta\Sigma$ modulator with no optimized NTF [7], the poles of the NTF are located beyond the bandwidth of interest. Hence, even though the gain shift affects all frequencies equally, differences at low frequencies[13] with the PPF, depending on the case, might not be enough to lower considerably the SNDR, at least the sidebands $E_M(s)$ would be strongly attenuated.

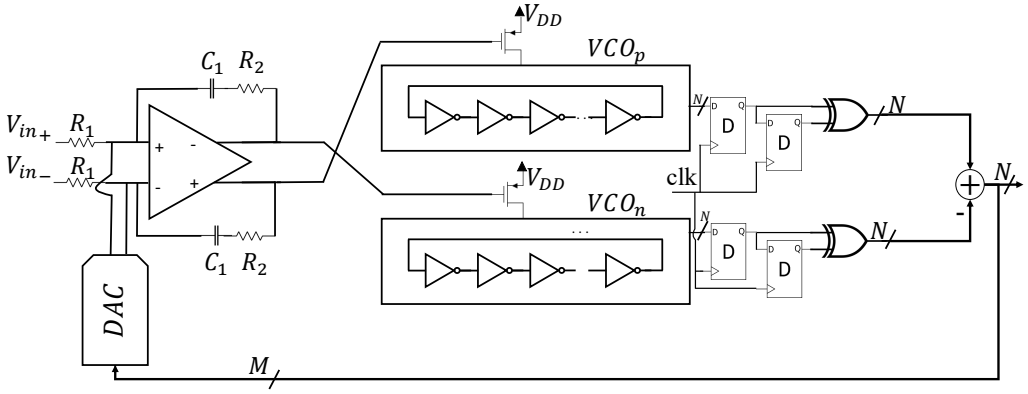


Fig. 5.5. Possible implementation for a second order frequency feedback architecture.

[12] The non-compensation should be expected.

[13] Low frequencies refers to frequencies below the bandwidth of interest.

To prove this, several cases were simulated and the results are shown in figure 5.6. It can be observed that in all cases the SNDR is recovered, as expected. It is also noted that the color distribution is not totally kept passing from the un-processed to the post-processed signal because the frequency responses of the used filter present differences with respect to the adequate one for low OSR values, making the SNDR to differ; however, the SNDR loss is about 1 dB at maximum.

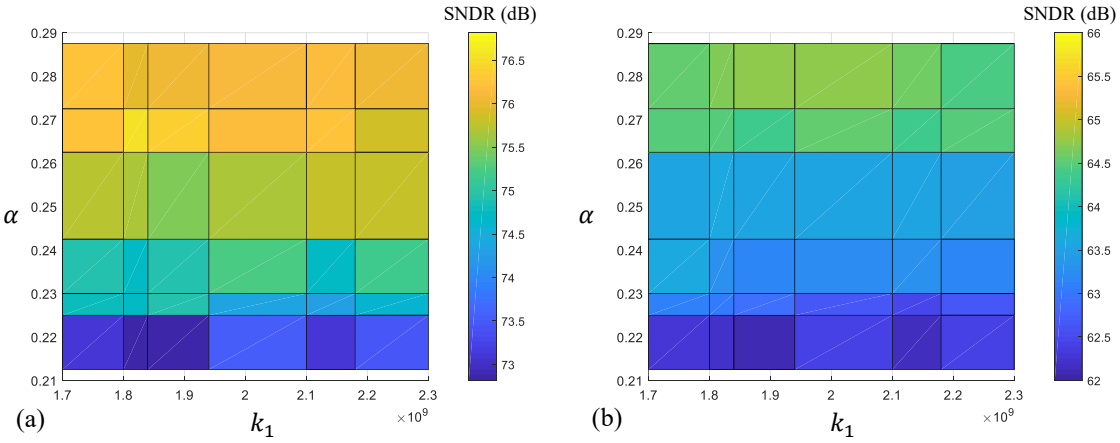


Fig. 5.6. Color-bar representation of the SNDR when applying the bit-split technique. (a) Post-processing and (b) before post-processing.

Figure 5.8 shows two output spectrums for a selected case from figure 5.6 in which α and k_1 are 0.92 and 1.06 times their nominal value respectively. It is shown that the output spectrum for the post-processed signal is reduced at low frequencies but also at high frequencies, being the latter not expected. If instead of using the filter that corresponds to table 5.1, a PPF that takes into account α and k_1 deviations is used, the output spectrum is, as expected, fully recovered (figure 5.7). This lack of discrepancy can be seen explained by means of the Bode plot of both post-processing filters as shown in figure (figure 5.9). It can be observed that the difference between their frequency responses, magnitude and phase wise, is not that enough to produce a difference in the post-processing scheme. Therefore, a more evident difference between Bode plots are needed to produce a severe degradation of the SNDR of the post-processed signal. Both post-processing SNDR are 76 dB.

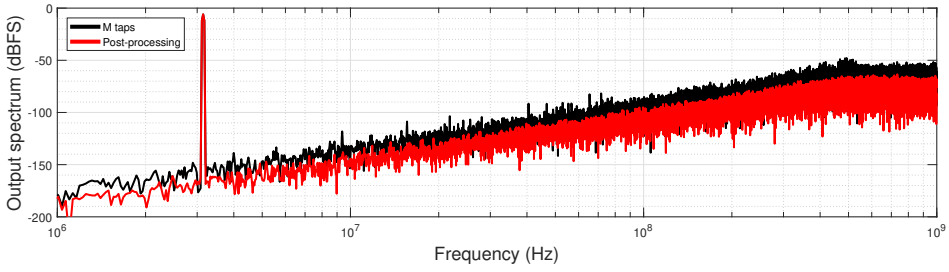
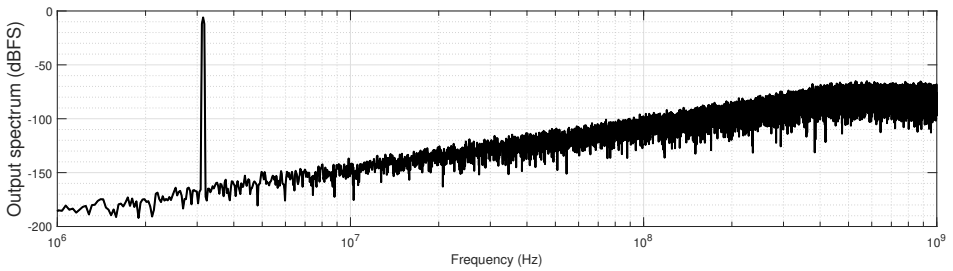
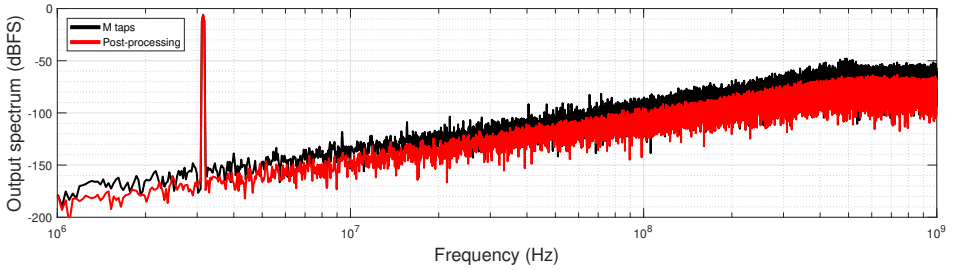


Fig. 5.7. Output spectrum when using the correct PPF.



(a)



(b)

Fig. 5.8. Analog mismatch - Output spectrum for (a) no bit-split technique and (b) use of bit-split.

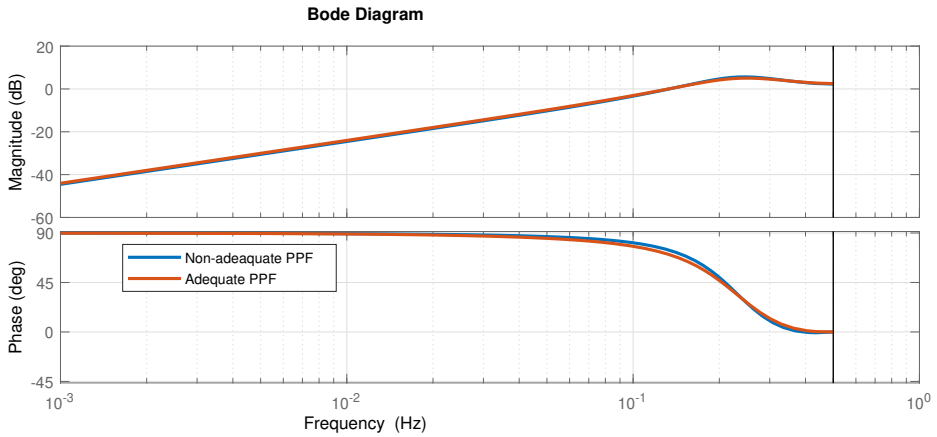


Fig. 5.9. Bode plot for wrong and correct PPFs.

A crucial insight is obtained from the previous example, the lower the bandwidth, the less integrated error between the precise PPF and an approximate one, thus, as long as the spectral shape is kept within the bandwidth of interest and the gain difference is small, it is possible to substitute the possible complicated PPF by a simplified one if spectral properties at high frequencies are not important. For instance, figure 5.10 shows three output spectrums for a system following table 5.1 for which three different PPF are used, one being the correct one (equation 5.1), and the other two having the second and third coefficients on the denominator multiplied by 1.5 and 0.6 respectively. That is, now the digital side presents a mismatch on gain and pole position.

$$PPF(z) = \frac{1 - z^{-1}}{1 - 0.25z^{-1} + 0.25z^{-2}}. \tag{5.1}$$

It is observed that SNDR is kept, but, as expected, at high frequencies the spectrum magnitude is higher on the systems with the wrong PPF. Of course, a shift on zeros position cannot be allowed because if they are not placed at 0, the post-processing scheme will not work; however, that is highly unlikely to happen because the circuit to implement zeros at 0 is very simple.

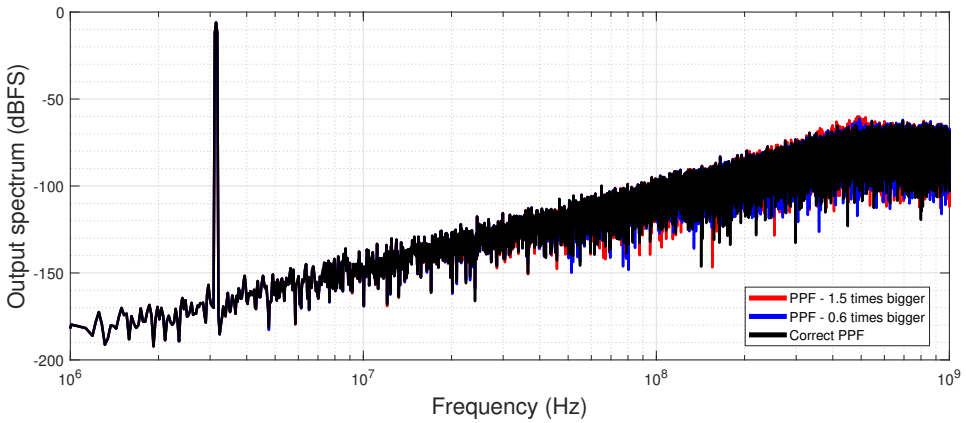


Fig. 5.10. Comparison for a mismatch on the PPFs. SNDR is 76 dB for the three cases.

5.3. Excess Loop Delay

In every closed-loop ΔΣ modulator there is a delay in the output bit generation, it can be modeled as if the DAC presents delay with respect to the ideal generation of bits, that is, by introducing a delay term in the feedback path. Anyway, a different clock for the DAC is used because it helps to avoid metastabilty issues. Figure 5.11 shows a diagram block that represents the ELD. In the literature there are several techniques to compensate ELD [47], [48]; however the scope of this document is not on its compensation but on how it affects the post-processing scheme if the PPF does not take into account this ELD.

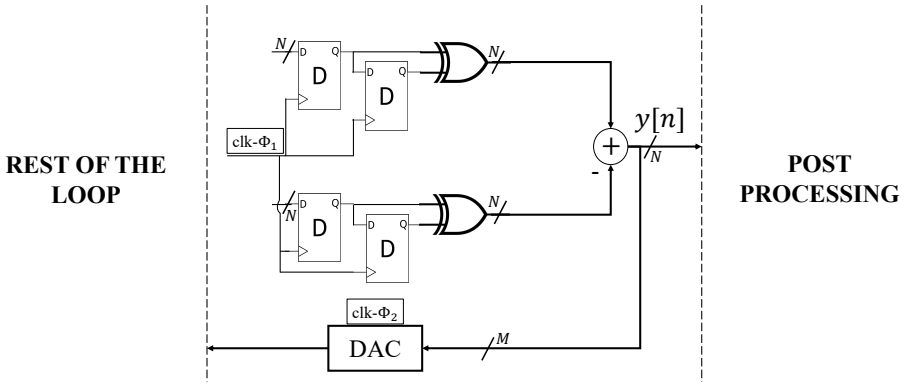
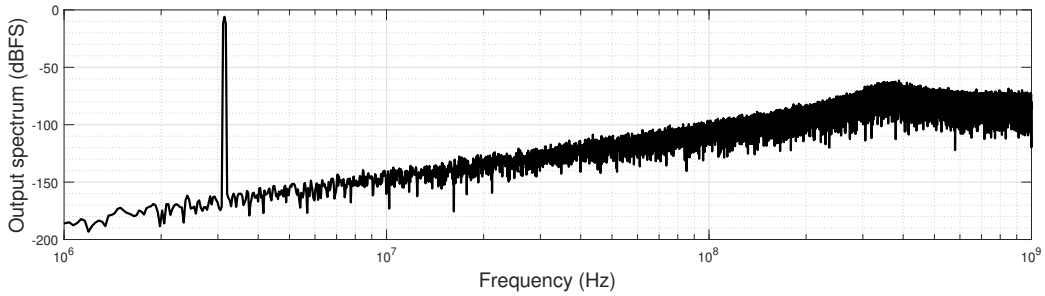
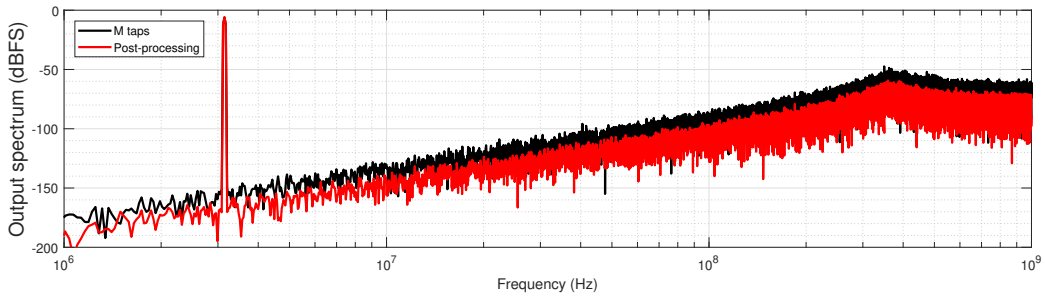


Fig. 5.11. Representation of the excess loop delay.

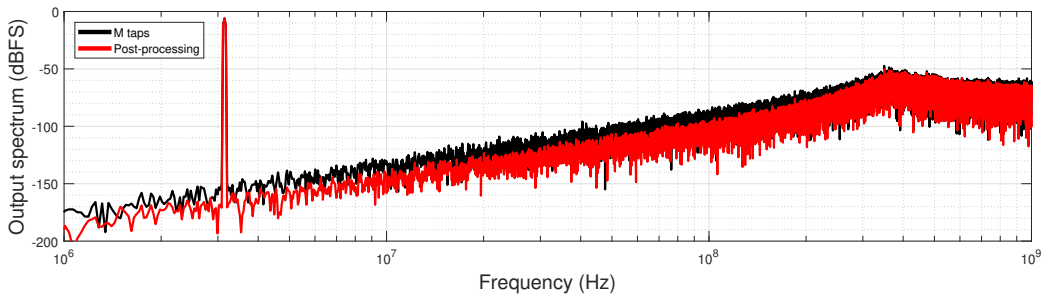
To fulfill this purpose, a behavioral simulation with the parameters of table 5.1 was performed, with an ELD equal to $0.5T_s$, for three different cases (figure 5.12): N taps in the feedback path, only M taps and using PFF as in equation 5.1, and the last one with a PPF for the given ELD. It is shown that even though the SNDR is similar for the three cases, due to that the ELD introduces new zeros in the open loop transfer function that will be transformed into the poles of the NTF, therefore, differences at high frequencies when the correct filter is not used are well defined. However, it is noted that whether PPF values are ones or others, the system stability does not depend upon it. Hence, the following conclusion can be stated: if a system presenting a given ELD with M taps in the feedback path is not stable or if values to VCOs input start to surpass its maximum values, and thus to saturate the VCOs, these conditions will produce effects that will not be removed by the post-processing scheme. Moreover, this extends to not only to ELD but for loop dynamic effects.



(a)



(b)



(c)

Fig. 5.12. Output Spectrum when (a) all taps are used in the feedback path (SNDR = 76 dB), (b) bit-split with a PPF that takes into account the ELD (SNDR = 76dB) and (c) bit-split with a PPF designed for parameters of table 5.1 (SNDR = 75dB).

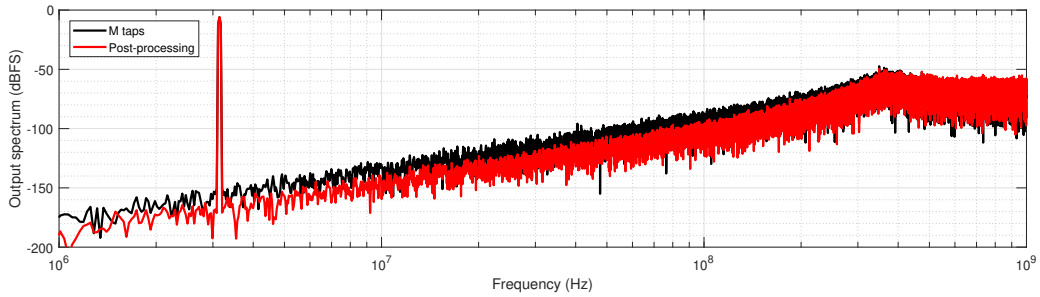


Fig. 5.13. Output spectrum for a PPF equal to $1 - z^{-1}$ (SNDR = 74 dB).

For the parameters chosen in table 5.1 it is possible to replace the filter of equation 5.1 by a first difference, $1 - z^{-1}$, as their gain are similar, and the spectral shape is kept within the band of interests; figure 5.13 shows the output spectrum for this case and it can be observed that the assumptions made are correct and SNDR is mostly recovered, a SNDR loss of about 2 dB occurs when the first difference is used as a post-processing filter.

Hence, depending on the architecture, it might be possible to substitute a complicated PPF by a simple one, because let's not forget that this post-processing scheme is implemented by means of digital logic, thus, there are multipliers, adders and so on, and thus accuracy or the need for simplicity might be a limit to implement a perfect PPF.

5.3.1. Non-equidistant phases in the feedback path

As stated before, the best results are obtained when the feedback path contains only equidistant phases of the VCO; this can only happens when N is a multiple of M. However, it is possible that the number of VCO inverters is not a multiple of the number of elements in the DAC. Let's suppose the following case: A system with the parameters on table 5.1, but instead of having 90 inverters it can only present an odd number of those (non-differential VCO). In order to get an equidistant distribution of phases, the number of inverters should be decreased to 75 or increased to 105, but in the former case, the SNDR would be diminished as the number of its quantization steps are decreased [22], [49], while in the latter, fabrication technology can restrict the maximum oscillation frequency because placing more inverters means that each inverter must delays less time [46]. For instance, if the parameters and SNDR goal are in agreement with a VCO of 91 inverters, two possible options arises for the bit-split: to select 13[14] equidistant phases (M_1), and other 2 that are not equidistant (M_2), or select 15 pseudo-equidistant phases M_{1pe}[15]. Whereas frequency shift will occur to the sidebands of M_1, M_2 sidebands will only present attenuation because the output is normalized to $[-1, 1]$, thus, its power contribution is divided by 15 in this case. For the maximum attenuation of the first sideband,

[14] 91 is a multiple of 13.

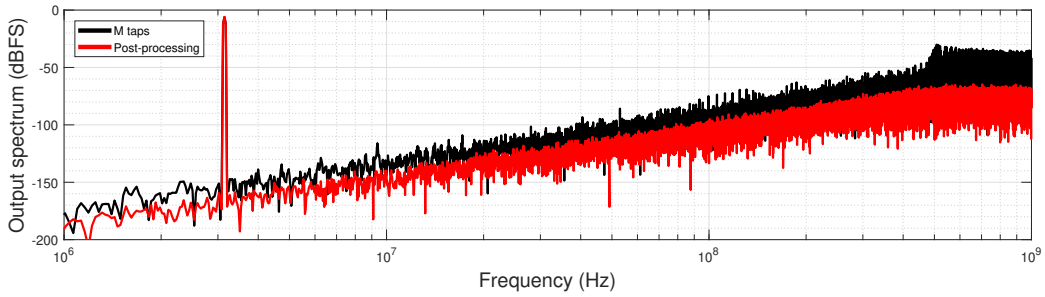
[15] Pseudo-equidistant means to select lines, not phases, that are evenly spaced while keeping a maximum distribution, for this example, it means to take 1 output line every 6 up to a total of 15.

M_2 must present a phase difference close to $\pi/2$. M_{1pe} sidebands will present strong attenuation but for multiples of $30f_o$. Even though the first option looks appealing due to the perfect cancellation but for multiples of $2M_1$, this provokes that the other two phases at best cancel each other sometimes. Because M_2 presents a difference of almost $\pi/2$, this results in the first sideband being attenuated, the second is almost fully amplified, the third will be less attenuated, the fourth is less amplified than the second and so on... On the other hand, it is expected for the pseudo-distribution to work better for small values of q as there will be a pseudo-cancellation as well. Table 5.2 shows the denormalized magnitude of the resultant rotating vector $\vec{v}$ for each case. Only multiples of 2 are considered for q given that the model of each inverter as two single bit VCOs with a phase shift of π has shown that the sidebands of each inverter cancel when q is odd, and this does not depend on the selected inverters. It should be noted that as the value of q increases, the magnitude of the frequency response of the first difference and the values of the Bessel function of equation (3.19) decrease as well, resulting in that for large values of q it turns out that the magnitude of $\vec{v}$ takes less importance, therefore, first sidebands will determine whether there are visible sidebands at the output spectrum or not. Also, for this particular case it is noted that, as it is shown in table 5.2, the magnitude of $\vec{v}_{M_{1,3}}$ is around 2 to 10 larger than the magnitude of $\vec{v}_{M_{pe}}$ for $q < 14$.

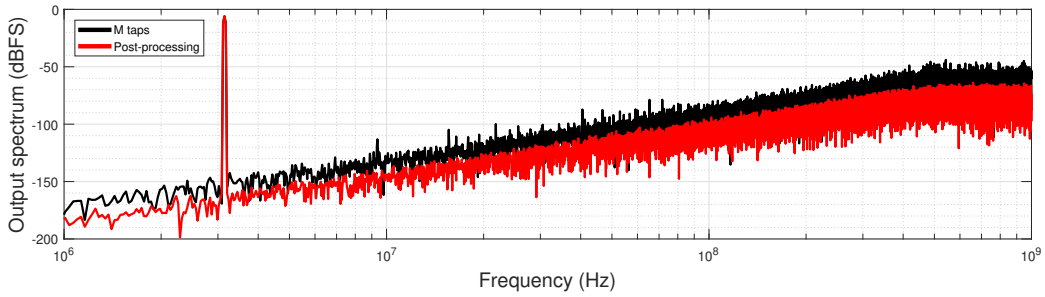
$\mid \vec{v}_{M_1 pe} \mid$	$\mid \vec{v}_{M_{1,3}} \mid$	q	$\mid \vec{v}_{M_1 pe} \mid$	$\mid \vec{v}_{M_{1,3}} \mid$	q	$\mid \vec{v}_{M_1 pe} \mid$	$\mid \vec{v}_{M_{1,3}} \mid$	q
0.33	0.48	2	0.43	2.99	12	0.98	3.88	22
0.34	3.88	4	0.48	2.99	14	1.32	0.48	24
0.36	1.41	6	0.54	2.27	16	2	28.67	26
0.39	3.54	8	0.64	3.54	18	3.88	0.48	28
0.4	2.27	10	0.77	1.41	20	28.68	3.88	30

Table 5.2. MAGNITUDE OF THE ROTATING VECTORS $\vec{v}_{m_{1,3}}$ AND $\vec{v}_{m_1 pe}$.

A behavioral simulation was performed to confirm the previous analysis. It is observed that in figure 5.14 for the case of M_1 and M_2 there is a visible sum of sidebands around $2f_o$ for it is the frequency when actually the sidebands at multiples of $2f_o$ are amplified, whereas for the figure 5.15 there are no sidebands. It is noted that the prior observation between the magnitude of $\vec{v}_{M_{pe}}$ and $\vec{v}_{M_{1,3}}$ is confirmed because the diference between the black output spectrums at high frequencies, where the sidebands of M_2 are located at, goes from 6 to 20dB, as it was already anticipated. Hence, it is clear that if an equidistant selection of phases is not possible, the alternative is to go for pseudo-equidistant ones. For both systems the post-processing recovers SNDR and the spectral shape; even the huge sideband as well as the several spikes around 100 MHz in figure 5.14 are eliminated. However, the first system will be more unstable than the second one.



(a)



(b)

Fig. 5.14. Output spectrum for (a) 13 equidistant and 2 adjacent phases and (b) 15 pseudo-equidistant phases. Input magnitude = −6 dBFS, SNDR = 76 dB for both cases.

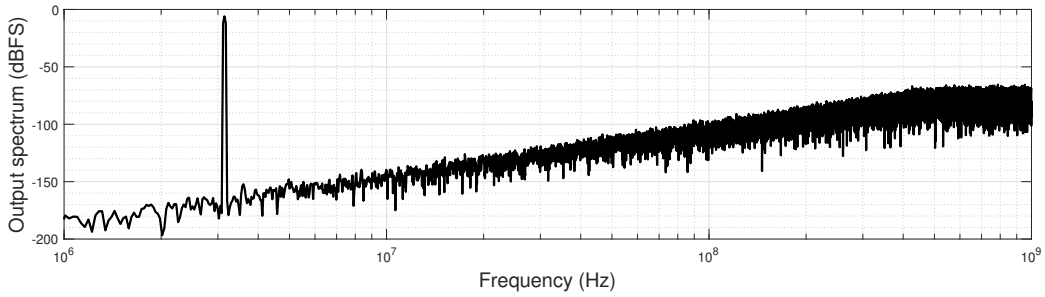
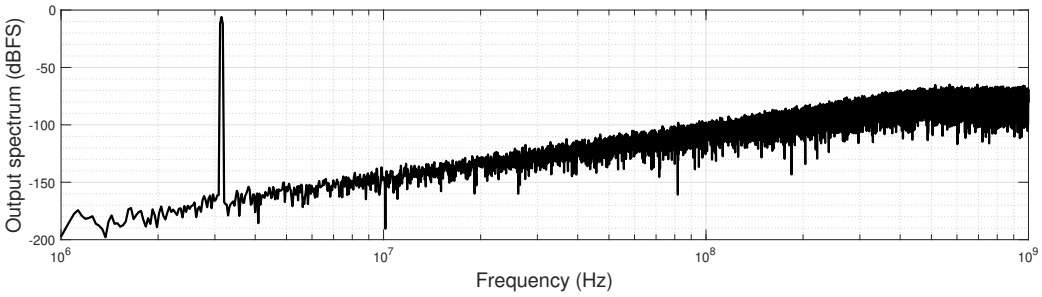
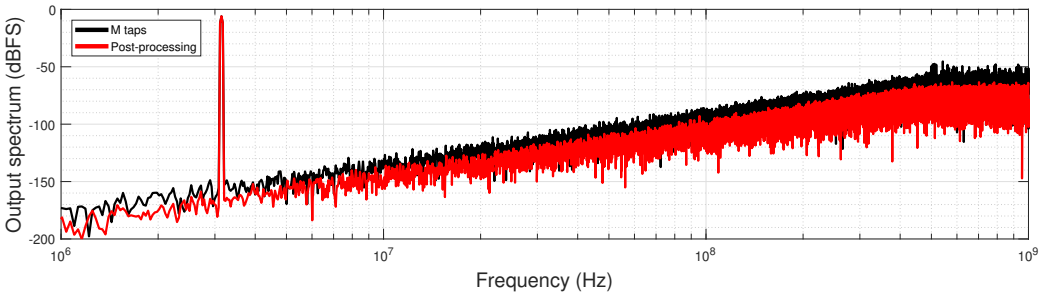


Fig. 5.15. Output spectrum when 91 taps are used in the feedback path for an input magnitude of −6 dBFS. SNDR = 76 dB

The previous example shows that the bit-split technique can be also applied successfully to certain ratios between N and M, no matter if the former is a multiple of the latter. For that matter, another case is simulated, but instead of 91 taps, a prime number, 89, is used. Given the nature of prime numbers it is not possible to apply perfectly the bit-split technique, however, as aforementioned, pseudo-equidistant phases achieve same practical results; the bigger is N, the better will be this approximation because the phases will be more indistinguishable ones from the others. A behavioral simulation for the case of 89 inverters is shown in figure 5.16 and it can be observed the are no visible sidebands and that the post-processing scheme works fine.



(a)



(b)

Fig. 5.16. Output spectrum for (a) all 89 taps the feedback path and (b) only 15 taps using pseudo-equidistant phases. SNDR for both cases is 76 dB.

Thus, working out the values of the rotating vectors and where the sidebands fall, it is possible to determine if a selected M will actually produce visible sidebands and so, leading to a system more prone to instability.

6. CONCLUSIONS

In this chapter, first, the conclusions based from the present document will be listed. Then, future lines of work will be presented.

6.1. Objectives met

This work has presented a novel technique to implement VCO-based ADCs, and it has studied its viability at system level. First, the state-of-art of $\Delta\Sigma$ ADC, specifically, VCO-based ADC was presented, and a brief overview on the theory was revised as well; it was shown that architectures using VCO are very promising. Later, on the next chapter, theoretical foundations on the VCO as PFM were reviewed and extended to cover the theoretical needs of the present work; the chapter concluded with a brief introduction to the bit-split technique. Chapter 4 presented and developed the theory behind the bit-split technique, the required linear models for the architectures selected were obtained based upon theory on chapter 3; to prove its validity simulations were performed. Finally, the last chapter presented a possible implementation for a selected case and studied different impairments on it.

Following is a list of the objectives met:

- A thorough study of the VCO as PFM was reviewed and presented. Moreover, applying such theory to study multiphase architectures was successfully presented for it is on what this Master's Thesis is built upon.
- Theoretical study of the bit-split technique was presented for two different architectures and verified by simulation. Linear models for the different architectures, first order frequency feedback, and first and second order phase feedback, were successfully developed. It was also shown that to build a system of *n*th order with such VCO architectures it is just an extension of the first and second order.
- A study of how a selected cases of impairments affect the technique was presented. The technique was shown to be robust against mismatch between analog and digital sides, and ELD because such impairments mostly affect the system at high frequencies, that is, out of the band of interest. It was also shown that an imperfect selection of phases was also possible without loss of SNDR or resulting in the sidebands affecting the output spectrum.
- Finally, main results of this work will be sent to the journal *IEEE Transactions on Circuit and Systems*. Moreover, through this academic year, the author has published and co-authored 2 different papers [50], [51] and has sent another one that is under revision [43]; all related to the VCO-based ADC.

6.2. Future lines of work

The focus on this work has been on the theoretical side of the implementation and has dealt with some impairments. However, the amount of impairments that are present in a system is high. Moreover, a circuit implementation to obtain measures from would be great. Following is a list of possible future lines of work that are related to the presented in this document:

- Study how the non-linearity of the VCO would affect the SNDR that is recovered from the system. Because the non-linearity can be modeled as a polynomial function placed just before the input of the VCO, it would generate harmonics that would degrade the performance whether all taps are used or not. Therefore, it shouldn't be the limiting factor; however, a study is mandatory to actually prove this.
- As stated before, more impairments can be added to the study, such as jitter in the DAC, metastability within the flip flops of the circuit, mismatch in the elements of the DAC, to use a real operational amplifier (non-infinite DC gain), mismatch between each set of VCOs (central frequency and gain), thermal noise, etc...
- A circuit implementation for both analog and digital part, following for the latter the simplification proposed in section 5. It would be interesting to study different architectures in the T2B converters as well as the latency or problems related to operate at frequencies of a few GHz.

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