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DESIGN AND CHARACTERIZATION OF A LOW VOLTAGE CMOS ASIC FOR MEDICAL INSTRUMENTATION

BACHELOR THESIS
BIOMEDICAL ENGINEERING

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ABSTRACT

The acquisition of biomedical signals requires analogue to digital converters of high resolution, low voltage of power and low consumption. The solution for this need is the use of new sigma delta conversion architectures such as the one tested in this Bachelor Thesis.

This work covers the design of the instrumentation necessary for the operation of Application-Specific Integrated Circuit Sigma Delta Analog-to-Digital Converter (ASIC ΣΔ ADC) that is already manufactured and its integration into a Printed Circuit Board (PCB). It also includes the development of the necessary software that facilitates the accomplishment of the necessary tests and the analysis of the data that will allow to characterize the operation of the fabricated prototype. Finally, the results and conclusions of the project will be described.

The ASIC to be tested in this Bachelor Thesis consists of a180-nm Complementary Metal-Oxide Semiconductor (CMOS) bandpass ΣΔ ADC developed to fulfil the specifications of a fully-integrated receiver for Magnetic Resonance Imaging (MRI). Integrating an integrated CMOS receiver into a single chip will help improve image quality by avoiding the use of many coaxial cables that are used to connect the Radio Frequency (RF) coils to the scanning hardware. The proposal made is a very simple Low-IF receiver characteristics in which a continuous time Low-IF bandpass ADC is the most efficient architecture. The circuit in continuous time replaces the classic filter only thus, an anti-alias filter would be necessary. In addition, the bandpass filter assists in the attenuation of the quantization noise in the bandwidth of interest, while at the same time the stability of the system is easily achieved due to the selected Low-IF.

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GLOSSARY OF TERMS

ADC	Analogic Digital Converter
ARDUINO	Open-source electronic prototyping platform
ASIC	Application-Specific Integrated Circuit
CMOS	Complementary Metal-Oxide Semiconductor
CT	Continuous Time
DAC	Digital to Analog Converter
DC	Direct Current
DR	Dynamic Range
DRC	Design Rules Checking
EMI	Electromagnetic Interference
ENOB	Effective Number Of Bits
ESD	Electrostatics Discharge
FFT	Fast Fourier Transform
HDD	Hard Disk Drive
Hw	Hardware
IF	Intermediate Frequency
IFSR	IF Sampling Frequency Ratio
IMD	Intermodulation Distortion
IMEC	Interuniversity Microelectronics Centre
IMEC	Interuniversity Microelectronics Centre

IQ	In Quadrature
LDO	Low dropout
LNA	Low Noise Amplifier
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signalling
LVS	Layout versus Schematic
MRI	Magnetic Resonance Imaging
NAS	Network Attached Storage
NTF	Noise Transfer Function
OSR	Oversampling Ratio
PCB	Printed Circuit Board
RF	Radio Frequency
SMD	Surface Mount Device
SNDR	Signal to Noise and Distortion ratio
SNR	Signal to Noise Ratio
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
Sw	Software
T	Tesla
VCM	Common Mode Voltage
VGA	Variable Gain Amplifier

1 INTRODUCTION

Magnetic Resonance Imaging (MRI) is one of the most widely used imaging techniques in medical diagnostics. MRI is a non-invasive technique to produce highly detailed images of tissue in the body. A great variety of anatomical and functional features, processes, and diseases can be visualized with this approach.

MRI employed a strong and static magnetic field which is applied to the patient using super-conducting magnets (submerged in liquid helium, -268.9 ºC), which aligns the nuclear spin of the abundant hydrogen atoms in water and fat of tissues in the same and opposite direction of the magnetic field. In MRI, a radio frequency wave, or a radio frequency pulse (RF), is transmitted into the patient. When this wave is sent with a very specific frequency, some spins will change their alignment as a result of this new magnetic field. After the RF pulse, they generate a signal as they return to their original alignment. This is the measured MR signal.

1.1 STATE OF ART

From the first MRI machine manufactured in 1977 by Dr. Raymond Damadian, see Figure 1.1, there have been many advances.

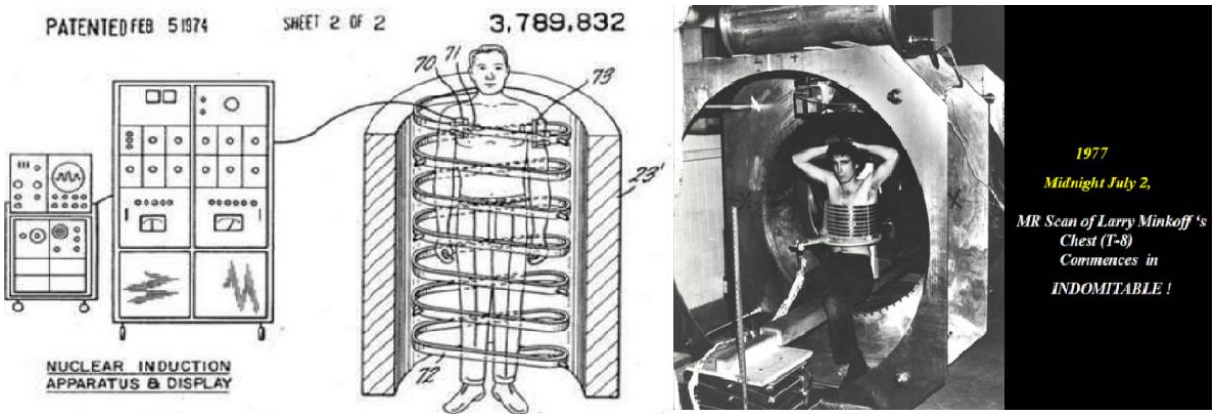

Figure 1.1 First MRI [1], [2]

MRI equipment has improved from devices where coils, signal transmitters and receivers were located in different rooms, which meant that in order to extract the signal from the magnetic fields and be able to process them, a lot of very long shielded

coaxial cables were needed. Currently, in magnetic resonance imaging equipment, the instrumentation of the receivers is made up by discrete commercial elements, but as technology has made such a progres it has been possible to make receiver PCBs increasingly smaller and immune to magnetic fields. This has allowed them to be placed within the magnetic field, which has made it possible to shorten the coaxial cables from tenths of meters in length to a few meters, see Figure 1.2

Figure 1.2 Actually MRI [3]

Surface coil arrays brought in proximity to the human body enhance the performance of an MRI measurement both in speed and signal-to-noise ratio. However, size and cabling of such arrays can deteriorate the performance of the imaging. Ultimately, the receiver must be placed directly on the coil to avoid bulky cable blocks and to receive the data directly in bore and send them digitally to the MRI scanner through the optical fiber. This implementation is the cheapest, most flexible and insensitive one to magnetic fields. In order to achieve this configuration, it is necessary for the PCB of the receiver to be as small as possible, and this can only be achieved if you have a receiver fully integrated into a single chip. The integration of the receiver into a single, small, nonmagnetic and very low power CMOS chip is the key to this evolution of MRI equipment. [4]

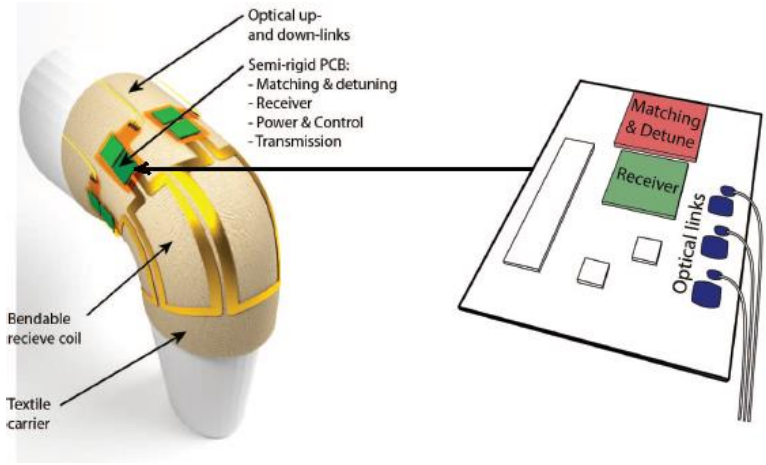

Figure 1.3 Prototype of wearable coil array and integrated electronics and Semi-rigid PCB [4]

The Department of Electronic Technology of the Carlos III University of Madrid, through the Mixed-Signal Circuits Laboratory and working with IMEC (Interuniversity Microelectronics Centre), have designed an Application-Specific Integrated Circuit (ASIC) for Biomedical Instrumentation, focused on MRI systems. The technology used in this ASIC is 1.8V 180nm CMOS.

The ASIC is suitable for the integration of a multichannel receiver of a MRI scanner. The use of this ASIC will simplify the receiver while also making it cheaper. Due to its low consumption it can be used in portable systems.

The ADC is targeted for receivers with operating carrier frequency between 64 and 128 MHz, which covers commercial 1,5 T and 3T scanners.

In this ASIC only the Analog-to-Digital Converter (ADC) is implemented. This is the first prototype that will be evaluated. It will be used to develop all the instrumentation needed for testing. In further steps, the rest of the blocks of the MRI receiver will be integrated into a second ASIC. The reason for this is that the ADC is the most demanding block, and has to be evaluated separately. In addition, all the instrumentation that will be developed for measuring this first ASIC, will be also used for the second ASIC.

This work will focus on the design and measuring of all the instrumentation needed for testing the ASIC, along with all the back-end digital calibration that will be used in the final system.

The chip ASIC consists of three main conceptions.

1. Firstly, the use of a Continuous- Time ΣΔ modulator is proposed to exploit its inherent anti-alias filter and remove or at least relax the filter front.
2. Secondly, a bandpass loop filter is used which is more efficient for a narrow bandwidth as 1 MHz. Moreover, a low IF (Intermediate Frequency) to Sampling Frequency Ratio (IFSR) allows the ADC to behave close to a low-pass ADC in terms of stability and block requirement.
3. Finally, IQ demodulation can be implemented in the digital decimation filter by choosing a proper IFSR.

In Figure 1.4 a) the diagram of a receiver which is the most frequently investigated so far can be seen.

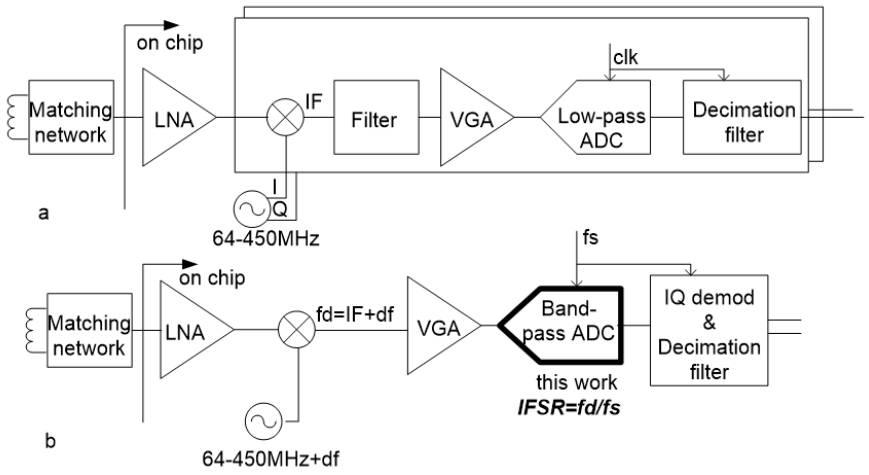

Figure 1.4 a)Block Diagram of integrated CMOS receiver [5] and b)Block Diagram of the proposed CMOS receiver.

In Figure 1.4 b) the proposed receiver diagram in which the input filter has been removed and the ADC is a bandpass instead of a low pass can be seen.

It is proposed to change the Low-pass ADC by the Band-pass ADC because it uses an increased IF up to few MHz. The main benefit of increasing IF is the freedom to design a frequency plan that accommodates enough bandwidth, avoid flicker noise and includes mixing of spurious tones which can simplify the Low Noise Amplifier (LNA) and the mixer. A bandpass ADC processes the narrowband signal without a penalty on oversampling. Moreover, a Low IF to sampling frequency Ratio (IFSR)

allows the ADC to behave close to a low-pass ADC in terms of stability and block requirements. This option will be more efficient.

1.2 OBJECTIVE

The goal of this Bachelor Thesis is to design all the instrumentation needed in order to evaluate the proposed ASIC. In addition, a close control loop will be also implemented in order to have real time measuring capabilities of the ASIC.

The main objectives of the Bachelor Thesis are:

1. Characterize the ASIC that **includes only the ADC**. This Bachelor Thesis is the first step in order to develop the complete MRI ASIC. In next steps this ADC will be integrated in another ASIC together with the sensor, LNA, mixer, ADC and digital filters (see Figure 1.4).
2. Develop all the instrumentation needed to measure the ASIC:
    a. The PCB to mount the ASIC
    b. The electronic to supply the ASIC
    c. The electronic to readout the digital Data of the ASIC
3. Develop a close control loop of the ASIC
4. Develop a software to post-process the data of the ASIC (digital back-end filters)
5. Validate the Design

The core of the Continous Time (CT) ΣΔ ADC implemented in this first version of the ASIC can be observed in Figure 1.5 . The details of the schematics of the resonators and the adder are shown in Figure 1.6.

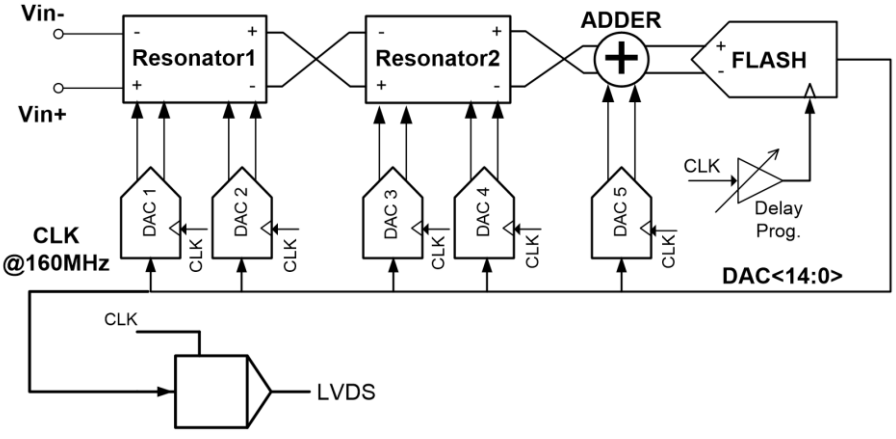

Figure 1.5 Block Diagram of Low-IF ΣΔ ADC

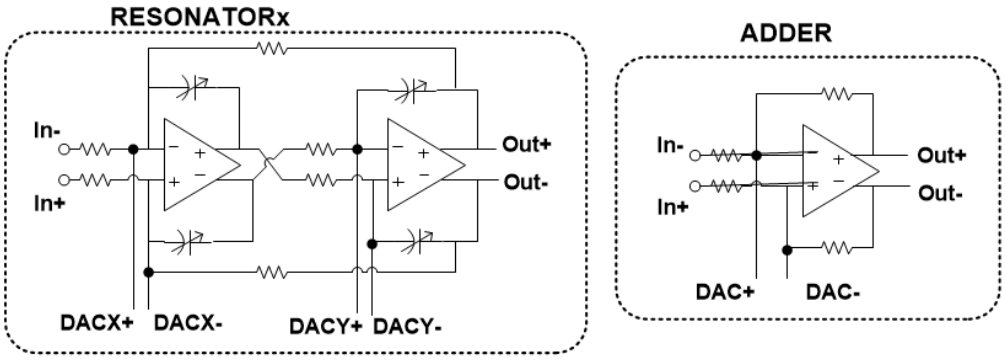

Figure 1.6 Detail of the components of Low-IF ΣΔ ADC

By definition an ASIC is a custom-made integrated circuit for a particular use. In order to be able to characterize it after its manufacturing it is necessary to have a controlled Hw-Sw (Hardware – Software) environment where the ASIC can be placed, simulating the expected inputs of previous subsystem and obtaining the outputs which must be delivered to the next subsystem. This is why it is essential to create a test platform where the measures to ensure that chip is correct are carried out. In order to guarantee that the tests have no problem outside the develop platform. Therefore, ASIC will be implemented in a printed circuit,thus it is necessary to generate a PCB.

Once the development platform has been manufactured and tested, ASIC testing is now made possible. The chip has internal elements which by external configuration can have a certain number of values (the measurements have to be done every configuration). Measurements of configurations which do not meet established requirements are discarded and measures meeting requirements are stored. After testing, a set of ASIC configurations are obtained with their measurements now meeting the requirements.

As our ASIC is a part of a larger circuit, we must provide the following subsystem with the values of the measurements of the configurations which meet the requirements, As well as the figures of merit of each configuration.

It is time to frame this Bachelor Thesis within the main project, see Figure 1.7.

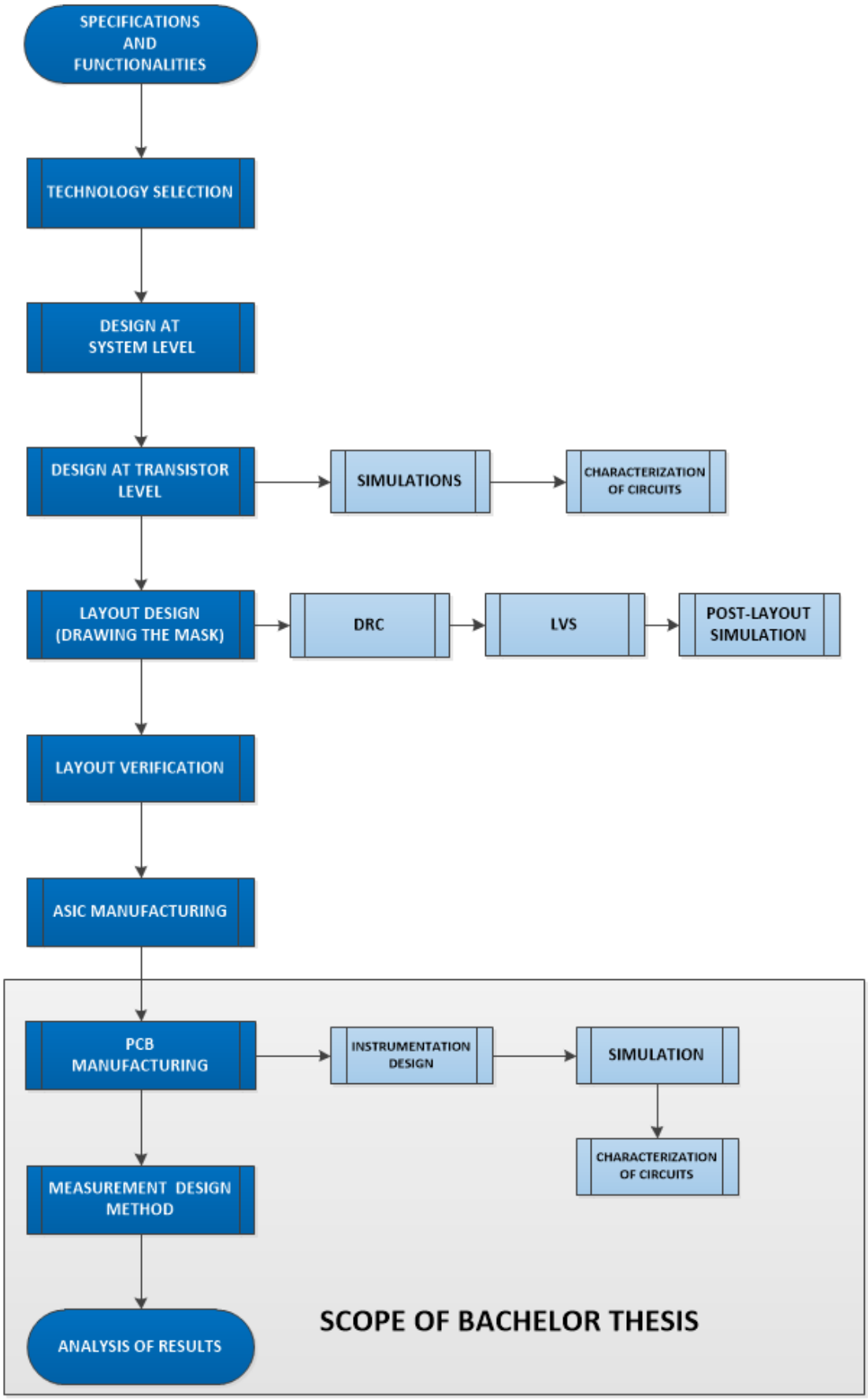

Figure 1.7 Flow of design integrated circuit. Scope of Bachelor Thesis.

The flow desing of an analog integrated circuit with a custom design (ASIC) is in Figure 1.7. The first stage of this flow is writing the specifications and requirements that must be met by the integrated circuit. In the second stage this technology is chosen, in this case the technology selected is the CMOS of 180nm. Next, the component subcircuits at high level are define. The designs are made at the transistor level, which once simulated and characterized the layout is performed. After carrying out all the necessary checks to ensure that the design corresponds to what has been specified, th ASIC is sent to manufacturing . With all ASIC specifications clear, all necessary instrumentation is prepared to be able to perform the tests. When all the instrumentation of PCB has been characterized, the PCB is made and sent to manufacture. At the end, a systematic method is developed that facilitates the accomplishment of the tests and finally the analysis of the data is done where it will be possible to say if the developed design is valid or not.

1.2.1 BLOCK DIAGRAM OF THE PROJECT

In Figure 1.8 is represented the closed-loop system schematic that controls the tests of the different configurations in "Real Time". Configuration tests have a long duration in time because the possible configurations are very high. The system operates autonomously and only needs a technician initializing it.

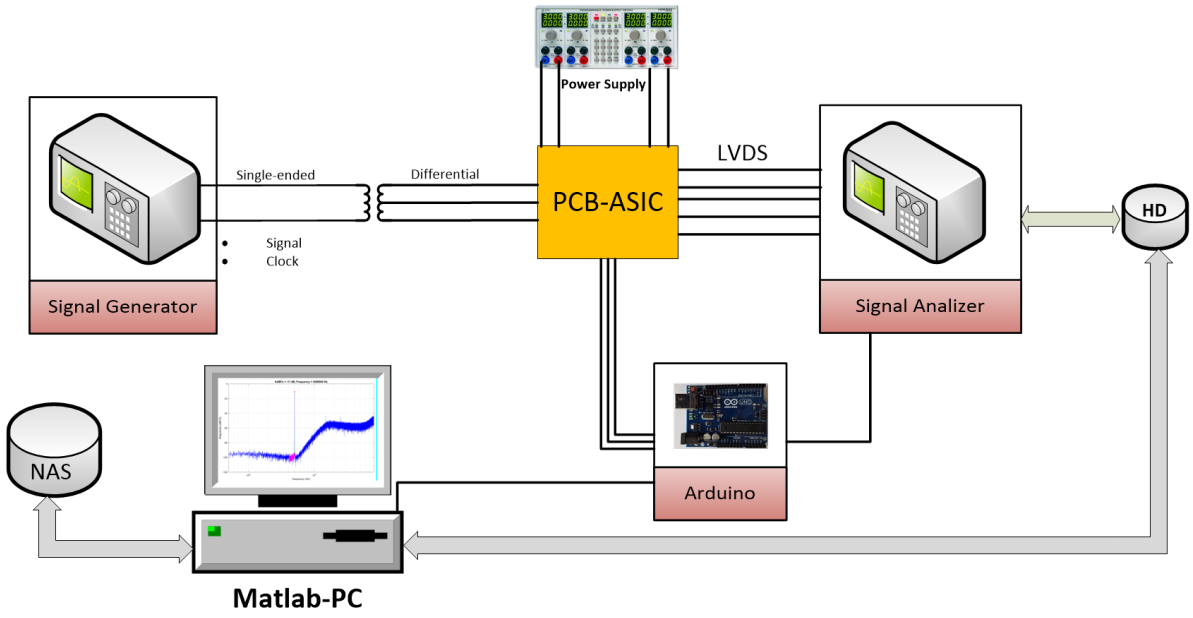

Figure 1.8 Configuration Loop of the ASIC

Now, the functional blocks of the ASIC test loop are described below.

1. **Instrumentation:** for the ASIC chip to perform its function it is necessary to develop the supporting circuitry (current sources, stabilized voltage sources, voltage references, control of digital inputs, etc). All this instrumentation will be integrated in a printed circuit, PCB. This will prevent all problems associated with standard test boards.
2. **Power of the system:** The system is powered by a DC (Direct Current) power supply that does not introduce power supply (50 Hz). In the trial it has been used a "**Programmable Power Supply HM7044**" by HAMEG.
3. **Input signal:** to test the different configurations a signal generator is used, performed with "**Programmable Synthesizer HM8134-2**" by HAMEG. The test signal used in the configuration process is a sinusoidal signal of 5 Mhz.
4. **The clock:** In CT ΣΔ ADC modulators, the sampling frequency is much higher than the Nyquist frequency, the sampling frequency is equal or higher than 160 MHz, so 16 times higher than the Nyquist frequency, a signal generator is used "**Vector Signal Generator SMV-03**" by Rohde & Schwarz. The ratio between the sampling frequency to the Nyquist frequency is known as OSR ("Oversampling Ratio").
5. **Output signal:** The ASIC provides an output that has to be processed, for this purpose a **Logic Analyzer** is used (**Agilent 16902A)**. The analyzer captures the digital output data of the CT ΣΔ ADC modulator, when indicated by the Matlab Script through the "Arduino" system, which is automatically saved in a text file with extension .csv, on a network hard drive**.**
6. **PC with Matlab Script:** A PC with Matlab and library is used to operate the "Arduino" microcontroller system. The Matlab Script performs the following functions:
    a. Handling the ASIC shift register using the Arduino to change the configuration parameters.
    b. Handling of the Logical Analyzer using the Arduino, this microcontroller system indicates to the Logical Analyzer the beginning and end of the capture of the test signal, the average duration of each capture is nine seconds.

c. Reading the text file that the logical analyzer has recorded in the Hard Disk Drive (HDD). The FFT (Fast Fourier Transform) is calculated (with the FFT, it is verified how good or bad is the output signal), the results of the data processing are saved.

7. "**Arduino" microcontroller system:** the "Arduino" is used to change the digital inputs of the ASIC, and also to handle the Logical Analyzer. ARDUINO is handled by the Matlab script.

A close loop is implemented, this controls:

1. The ASIC configuration data.
2. The acquisition and storage of the data provided by the ASIC.
3. Processing the data to determine which is the best result.
4. Storage of data processing.

The configuration of the ASIC will be done with an "Arduino" microcontroller, managed by a Matlab script that will also handle the processing of the data obtained from a logic analyzer.

1.3 PROJECT DEVELOPMENT STAGES

ID	TASK	WEEKS																									
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
1	Get used to ΣΔ ADC	3 weeks																											
2	Design: Instrumentation circuit				5 weeks																								
3	Layout: Integration Instrumentation circuit										4 weeks																		
4	Layout: PCB design											4 weeks																	
5	Send PCB to fabrication / Prototype reception															3 weeks													
6	Introduction of ASIC in PCB																		2 weeks										
7	Development of systematic measurement system																			5 weeks									
8	Complete characterization of ASIC																						4 weeks						
9	Result graphs																								3 weeks				
10	Memory development																				9 weeks								

Table 1.1 Timetable

The Table 1.1 timetable reunite the different phases of development of this Bachelor Thesis. The different stages took place at different times and with different dedication in terms of workin hours. For this reason, the timeline has been constructed without dates only weeks are counted without indicating the start with a certain date.

The project was separated into 10 stages, the first was to study the ΣΔ modulation to understand what is going to be tested, the second was to design and

simulate with the program Proteus the designed circuits. Once these circuits are validated, they were designed in the Altium program to integrate all the designs and perform the PCB. With the PCB in the laboratory, the ASIC was inserted and all discrete components (resistors, capacitors, connectors, etc.) were soldered.

The objective was to have the Sw prepared for when the PCB was fully ready. The nominal ASIC configuration data with which it was manufactured were calculated using a proprietary Matlab tool. The results obtained with the nominal configuration will be the basis for comparison with the real results. The simulated characterization will be the reference point for performing selective sweeps of tests in values near the nominal values. The best results of these tests are those that will be compared with the simulation values to determine the validity of the design.

1.4 REGULATION FRAMEWORK

Within the development of the project it is imperative to take into account certain safety parameters to maintain the good balance of the same. In order to do this, it is necessary to take into consideration both the correct working conditions that must be maintained in a laboratory to avoid damaging the measurement equipment and the electrostatic protection required when handling integrated circuits to avoid damaging them by electrical discharges. Neither should be forgotten the necessary protection of technician to those discharges. It is necessary to establish what steps have to be taken to fulfill the above conditions

In the specific case of this project based on the design and assembly of a PCB, the worker may be exposed to risks that may be related to the welding of different elements in printed circuit boards or the electrical risk involved in electronic operations. [6]

The welding used in electronics belongs to the type known as electric resistance welding with tin, but in this project welding paste has also been used. Although the risks involved in electrical welding with tin are minimal, it is necessary to take into account certain aspects that minimize the risks at work. Thus, it is recommended to check that the electrical equipment and the instruments are in perfect conditions of use. It is essential for the welder to be placed in a support orienting the electrode in the opposite direction of the operator. And finally avoid inhaling the fumes that occur

in the welding. This last point is closely related to the welder paste as this one has very toxic fumes so it is necessary a good ventilation of the room where it is being welded, in our case the laboratory, as well as an individual protection for each technician using masks. [7]

Since the main source of energy for this type of electronic devices is the electrical energy , this one must be also taken into account. For this reason, electrical risk (according to RD 614/2001) was defined as that originated by electric power, specifically including the risks of: [6]

- **Electrical shock** by contact with elements in tension or with masses put accidentally in tension. Because of this, the chip has protections so as not to be burnt. But it also implies that the technician can suffer from this electrical shock, as by touching the pads of the chip currents through the skin may be induced. In addition, these currents, though small may be, are high enough to cause internal damage to the chip. That is why the pads have "ESD (Electrostatic Discharge) protections" which consist of adding suitable circuits, with diodes to give a path to ground current avoiding electrostatic discharge. This would avoid damage to transistors or internal circuits of the chip.
- Electric shock or electric arc burns.
- Fires or explosions caused by electricity

One of the main electrical hazards is electrostatic discharges that can cause random failures in electronic components that are difficult to be controlled and pursued. So it is necessary to take protective measures against them.

These electrostatic discharges occur as a result of the static electricity that is generated due to following processes: [8]

- **By friction (or triboelectricity):** when two materials are rubbed against each other or separated from each other.
- **By load per contact**: because two conductors are one of them more charged than the other. Then the most charged conductor gives charge to the other one up to equally adquiere a potential difference in a value that may not be zero.

- **Load crown**: occurs when a very small surface is at a very high potential generating corona discharge.
- **Inductive load**: an object produces an electrostatic field which acts at a distance on nearby objects polarizing the charges. When the polarized object contacts another, one more loads are transferred or picked up, resulting in a loaded object.

Due to all these risks it is necessary to take into account prevention techniques such as: [6]

- **Procedural:** They try to establish safe operational methods of a general or specific nature for each activity or work operation.
- **Signaling**: They are based on the location of warning signs, caution, prohibition or information in workplaces with electrical risk.
- **Detection and identification**: They consist of identifying properly and checking the voltage in the electrical installations, before acting on them
- **Instructive:** These are intended to get the training and training of workers exposed to electrical risk, indicating the correct way of using equipment, tools, facilities, symbology and signaling

1.5 MEMORY STRUCTURE

This report is structured in eight chapters, according to Figure 1.9.

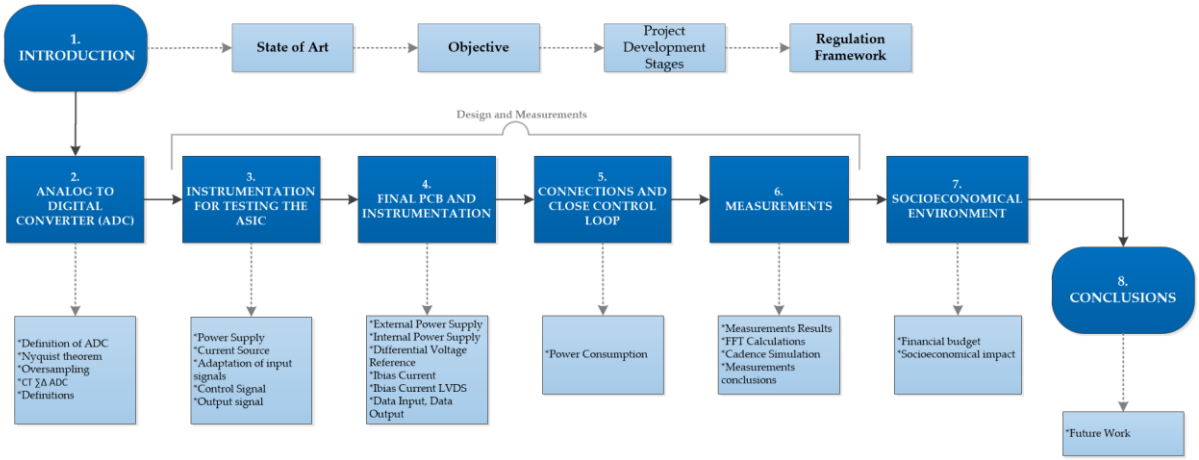

Figure 1.9 Flow of design integrated circuit. Scope of Bachelor Thesis

In the **Introduction** this Bachelor Thesis is contextualized within the technological development of the instrumentation of receivers of the MRI equipments. Moreover, the scope within the European project of constructing an integrated Receiver is defined. For this reason the **State of Art** of the MRI equipment, the **Objectives** to comply and the **Regulation Framework** are reflected. Also reflected is the **Project Development Stages.**

Chapter 2 describes what is an ADC and introduces the generalities of CT ΣΔ ADC and the main figures of merit.

In Chapters 3 and 4, and taking into account the electrical specifications of the ASIC prototype, all the necessary instrumentation is individually designed. Once this is validated through simulation these sepcifications will be used to design the PCB (**Objective 2**).

Chapter 5 shows the connections between the PCBs, the measurement equipment and the PC, which is the close control loop used to carry out the tests and obtain the data for later analysis. It is also show the power consumption of the ASIC for different configurations. Later on, the functionality of the Sw developed is clearly described (**Objective 4**).

In Chapter 6 the results of the ASIC characterization, ΣΔ ADC modulator, are analyzed. The results obtained from the simulation are compared to the best configurations obtained during the tests in order to decide whether the proposed design is valid or not (**Objective 5**). In the result analysis it is obtained that the ASIC works properly as expected and Its characterization has been possible (Objetive1).

Chapter 7 contains the budget and the socioeconomical impact of the project.

Chapter 8 sets out the scope achieved in each of the objectives, justifying if the principal of this Bachelor Thesis **Objective 1** has been satisfactorily achieved. The possible future works are going to be analyzed in order to improve the test.

2 ANALOG TO DIGITAL CONVERTER (ADC)

Within the goals of this Bachelor Thesis, it was indicated that an ASIC which is implemented as an CT ΣΔ ADC. This section will briefly describe the conversion of the analog signals to digital signal explaining the converter implemented in that ASIC.

2.1 DEFINITION OF ADC

There are many reasons for digitally processing an analog signal instead of processing the signal directly in the analog domain. Firstly, a digital programmable system allows flexibility in reconfiguring the digital processing operations simply by changing the program. Reconfiguration of an analog system usually implies hardware redesigning. Secondly, the tolerance in analog circuit make it extremely difficult for the system designer to control the accuracy of an analog signal processing system. Thirdly, it is more cheaper the digital hardware. [9]

In order to work in the digital world, it is necessary to have an interface that communicates the analog world with the digital world. This interface is the analog to digital converters. One practical limitation is the speed of operation of ADC.

The ADCs have implemented three function: sampling, quantification and coding, as can be seen in Figure 2.1.

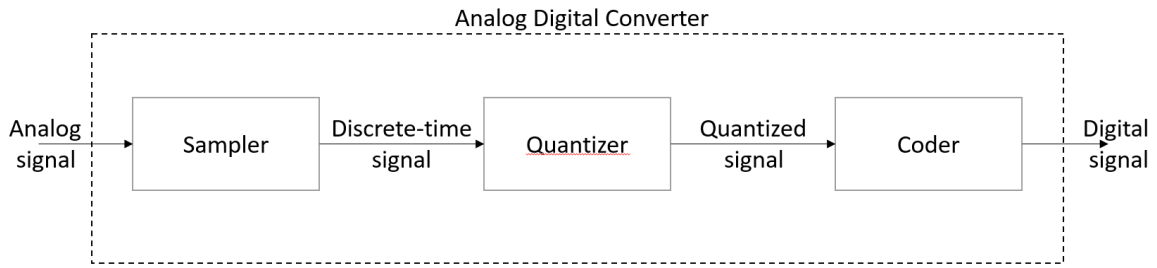

Figure 2.1 Analog Digital Converter

2.1.1 SAMPLING

This is the conversion of a continuous-time signal into discrete time signal obtained by taking "samples" of the continuous-time signal at discrete-time instant.

The temporal distance between taking one sample and the next one is called the sampling period and it is denoted as **T.** [9]

2.1.2 QUANTIZATION

This is the conversion of a discrete-time continuous-valued signal into a discrete-time discrete-valued signal. The value of each signal sample is represented by a value selected from a finite set of possible values. The difference between the unquantized sample and the quantized output is called quantization error. [9]

The figures of merit commonly used to characterize the quantization are defined below.

A range of an ADC is defined as the difference between the maximum value that can be measured and the minimum value.

$$R = (Vmax - Vmin) \tag{2.1}$$

It is defined as number of levels of the coding in the equation (2.2) where N is the number of bits of the ADC.

$$L = 2^N \tag{2.2}$$

The quantization step is the ratio between the range equation (2.1) and the number of levels equation (2.2).

$$\Delta = \frac{R}{L} = LSB \tag{2.3}$$

The quantization error follows the logic of Figure 2.2 where X(n) represents the sampled signal and X(q) is the quantized signal, the difference eq(n) is the quantization error, see equation (2.3)

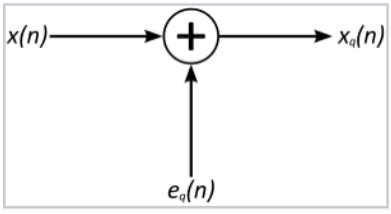

Figure 2.2 Quantization error model

$$e_q(n) = X_{q(n)} - X(n) \tag{2.4}$$

The quatization error will be between:

$$-\frac{\Delta}{2} < e_q(n) < \frac{\Delta}{2}. \tag{2.5}$$

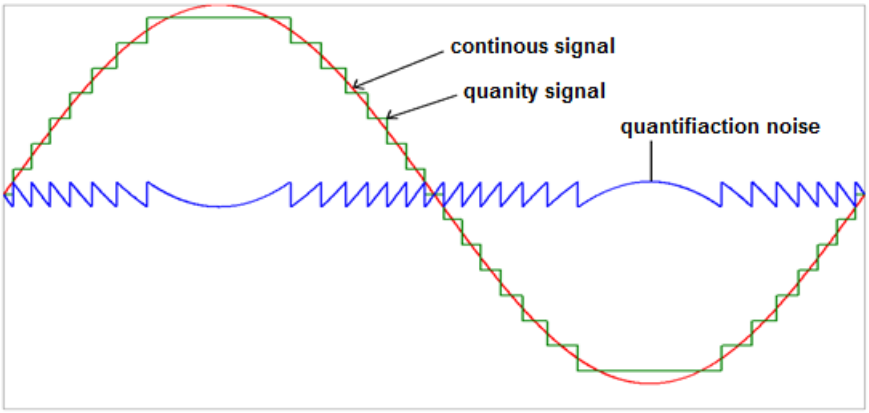

Figure 2.3 Signal representation, quantized signal and quantization error *[10]*

Although, as shown in Figure 2.3, the quantization error has a well-defined form, when treated with real signals, it can be considered as a White Gaussian noise signal. Also, the error is uniformly distributed across all frequencies, provided that the number of bits 'N' is large, that the input signal is within the quantization range and that the input signal is much larger than the Least Significant Bit (LSB).

It can be shown that for a sinusoidal signal with a peak to peak value equal to "R", the Signal to Quantization Noise Ratio (SQNR), is:

$$SQNR = 6.02 * N + 1.76 \text{ [dB]} \tag{2.6}$$

The SNQR gives information about the maximum theoretical efficiency of an ideal ADC converter. Performance will be lower due to others factors such as thermal noise, distortions, converter architecture, nonlinearities etc.

2.1.3 CODING

In the coding process, each discrete value that has come out of the quantization process is represented by a **b**-bit binary sequence.

2.2 NYQUIST THEOREM

If a signal is bandlimited and if the samples are taken sufficiently close together, in relation to the highest frequency present in the signal, then the samples uniquely specify the signal and it can be reconstructed perfectly. This result is called the sampling theorem and it can be expressed as follows:

Let X(t) be a bandlimited signal with $X(\omega)= 0$ for $|\omega| > \omega_M$. Then x(t) is uniquely determined by its samples x(nT), n= 0, ± 1, ± 2, ± 3 …. If

$$\omega_s > 2\,\omega_M \tag{2.7}$$

where

$$\omega_s = \frac{2\pi}{T} \tag{2.8}$$

Given these samples, it is possible to reconstruct x(t) by generating a periodic impulse train which successive impulses have amplitudes that are successive sample values. This impulse train is then processed through an ideal lowpass filter with gain T and cutoff frequency greater than ω_M and less than ($\omega s - 2\,\omega_M$). The resulting output signal will exactly equal x(t).

The sampling Frequency ωs, is also referred to as the Nyquist frequency. The frequency $2\omega_M$ under the sampling theorem, must be exceeded by the sampling frequency.

2.3 OVERSAMPLING

In signal processing, oversampling is the process of sampling a signal with a sampling frequency significantly higher than the Nyquist frequency. Oversampling improves resolution, reduces noise and helps avoiding aliasing and phase distortion by relaxing anti-aliasing filter performance requirements.

2.4 CONTINUOUS TIME SIGMA DELTA ADC

Miniaturization of electronic systems using nanoscale technologies allows to achieve greater speed in the devices. This miniaturization has made possible the development of ΣΔ modulators. [11]

Analog ADCs have many non-idealities that arise from random and systematic errors in circuit implementation processes, there are errors in the manufacturing process because the silicon is not homogeneous. These errors represent reliability problems; they can be compensated or calibrated after manufacture. On the other hand, these circuits undergo a time-dependent degradation due to the aging of the transistors, which means that the performance of the chip changes over time, which can cause circuits to change from fully functional to non-functional. Also different sources of disturbances such as electromagnetic interference (EMI) or substrate noise coupling can cause the chip to change, functionally correct circuit or failed circuit.

In addition to the above, ΣΔ ADCs offer a key advantage for their integration into the ASIC. Unlike the Nyquist ADCs, whose resolution depends heavily on the high precision of their component blocks, the oversampling and quantization noise shaping techniques used in the ΣΔ ADC allow speed to be exchanged for accuracy. Thus it can be obtained a circuit which is relatively insensitive to imperfections and aging of components. For these reasons, the ΣΔ modulation techniques are ideal for the implementation of high performance ADCs integrated in nanometric CMOS technologies, which are better suited to provide fast digital circuits than accurate analog circuits.

The ASIC chip to be configured is a ΣΔ modulator in continuous time, and the main features of these modulators will be described below.

Advantages of Modulators CT ΣΔ. [11]

- Faster operation with lower power consumption, driven by continuous operation time loop filter in which the dynamics of the circuits is not parasitic (as happens in switching capacitor circuits).
- Lower impact of errors caused by the sampling operation. This is a direct consequence of the fact that the sampling operation does not take place at

the input of the modulator, but within the loop. Sampling errors are filtered analogously to quantization noise.

- Lower thermal noise because, when not sampled, there is no folding effect "frequency folding" (which means less aliasing). In discrete-time modulators, high-frequency thermal noise signals collapse in the spectrum because the sampling rate is low, and in the signal recovery process the collapsed frequencies cause distortion and cannot be separated or distinguished of the original signal.
- Less impact of "digital noise" or "switching noise" switching noise is attenuated by the action of the loop filter, in the same way as the quantization noise.
- "Anti-aliasing", the loop filter can be employed for this purpose, relaxing the specifications or even eliminating the need for pre-filtering "anti-aliasing".

In quantization, an error called quantization error is generated. The error is a non-linear function of the input signal and produces a similar effect to a white noise source, because the error sequence is wrong with the signal and will be evenly distributed in the range [-Δ/2, +Δ/2], see equation (2.5.

The ΣΔ modulators are based on oversampling and noise shaping, which is responsible for minimizing the quantization noise in the desired band (Nyquist band).

OSR is the Oversampling Ratio:

$$OSR = \frac{fs}{fo} \tag{2.9}$$

Where fs is the sampling frequency and fo is the Nyquist frequency. The increase of the sampling frequency decreases the noise in the band of our signal.

In this modulator there is an H(s) filter whose function is to cause the quantization noise to decrease to low frequencies and increase to high.

Considering the quantizer as the only source of noise that is added to the filtered signal, a linear model equivalent to CT-ΣΔ can be obtained, as shown in Figure 2.4.

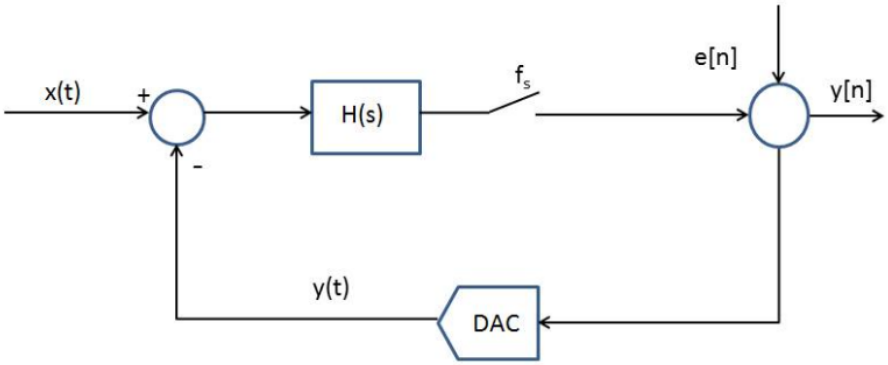

Figure 2.4 Lineal model of a CT - ∑Δ modulator

In this case, the modulator can be seen with two inputs **x, e** and one output **y**, in domain Z can be represented as:

$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z) \tag{2.10}$$

Where X(z) and E(z) are the Z transforms of the input signal and the error, Signal Transfer Function $S_{TF}(z)$ and Noise Transfer Function $N_{TF}(z)$ are respectively the transfer function of the input signal and the quantization noise.

$$S_{TF}(z) = \frac{H(z)}{1 + H(z)} \tag{2.11}$$

$$N_{TF}(z) = \frac{1}{1 + H(z)} \tag{2.12}$$

For the values where H(z)>>1, $N_{TF}(z)$ →0 y la Y(z) ≈ X(z). The spectral noise conformance will be performed by the H(s) filter, if we design it to take as large a value as possible within the bandwidth of our interest, the N_{TF} will be very close to zero and the S_{TF} very close to one, managing to take out most of the noise out the bandwidth of our interest. [12]

When implementing a CT-ΣΔ ADC it is very important to calculate the H (z), it will be the starting point to calculate the values of the discrete components. The calculation of this function becomes more complicated as the degree is increased, being extremely complicated above grade 3.

2.4.1 RESOLUTION

Today the CT- ΣΔ converters are a good choice for applications that require a digital signal processing with high speeds and good resolutions.

The resolution of these modulators depends on the order of the modulator filter, the higher the order of H(s), the higher the resolution however, the higher the order the worse the stability. The higher the filter order the more quantification noise is transferred to high frequencies with the consequent increase of the SNR and therefore of the dynamic range.

Then to increase the resolution of the modulator, an increase in the order of the filter can be performed as well as increasing the number of bits used in the quantification, or even increasing the OSR.

2.5 DEFINITIONS

At this point it is important to define the most important figures of merit that are used to characterize the oversampling converter.

2.5.1 SIGNAL-TO-NOISE RATIO (SNR)

It is the ratio of the output power at the frequency of an input sinusoid to the uncorrelated in-band error power. Ideally, only quantization noise is accounted to compute SNR, expressed as:

$$SNR = 10\ Log_{10}\left(\frac{\frac{A^2}{2}}{P_Q}\right) \tag{2.13}$$

Where:

A= Amplitude sinusoid input signal

PQ = Power noise quantification.

If errors due to noise and distortion are taken into account, the Signal-to-Noise Ratio (SNDR)is normaly used.

2.5.2 DYNAMIC RANGE (DR) AND EFFECTIVE RESOLUTION (ENOB)

The dynamic Range is defined as the ratio of the output power at the frequency of an input sinusoid with maximum amplitude to the output power for a small input for which SNR= 0 dB

Ideally, the dynamic range will correspond to the maximum SNR that can be obtained at the output of the CT ∑Δ modulator

$$DR = 10log_{10}\left[\frac{\left(\frac{A}{2}\right)^2}{2P_Q}\right] \tag{2.14}$$

Where:

A= Amplitude sinusoid input signal

PQ= Power noise quantification.

It can be shown that the dynamic range of a DAC of B-bit Nyquist can be calculated with the following formula:

$$DR = 10log_{10}\left[3 * 2^{(2B-1)}\right] \tag{2.15}$$

Relating the two previous formulas it can be defined the effective number of bits (ENOB) of the DAC as a function of DR as:

$$ENOB = \frac{DR(dB) - 1.76}{6.02} \tag{2.16}$$

3 INSTRUMENTATION FOR TESTING THE ASIC (SIGMA-DELTA ADC)

This chapter presents the circuits that make up the support instrumentation that will allow the realization of ASIC tests. The starting point for this project is the fully developed ASIC. Figure 3.1 shows the workflow followed to obtain the PCB (**objective 2**), which will allow to continue with the rest of the project objectives, until the objective 1, that is to characterize the ASIC, is achieved.

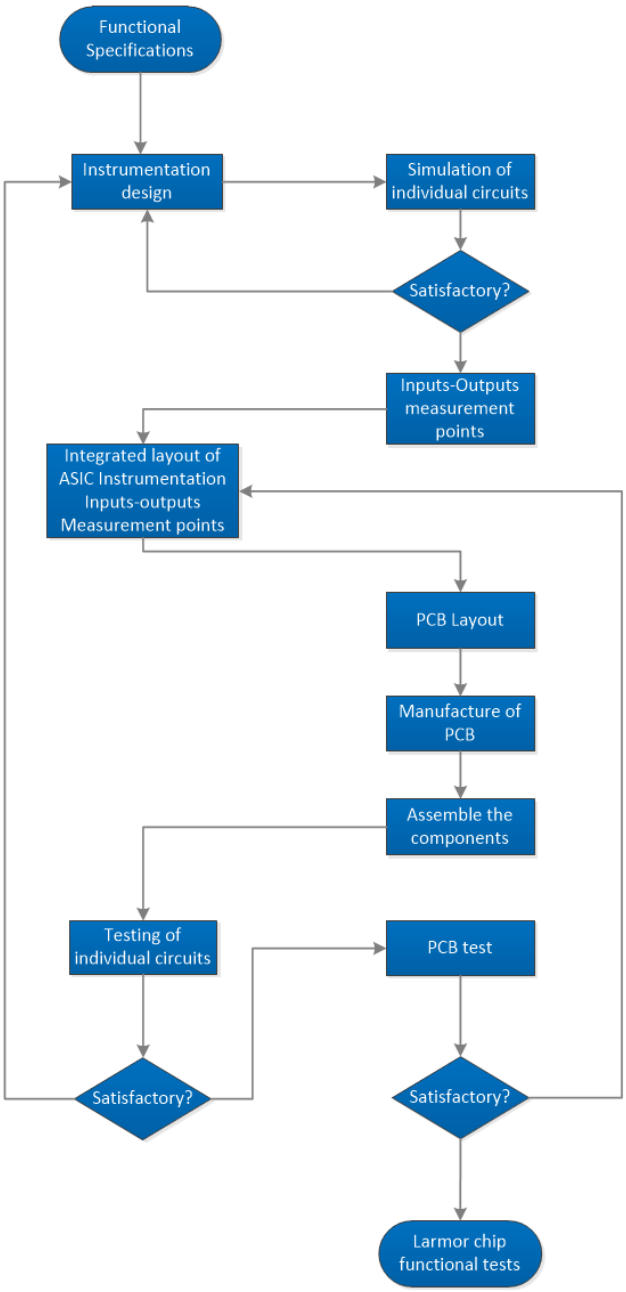

Figure 3.1 Flow chart PCB board development

The first step is to develop the PCB that will be used to test the ASIC. In this PCB the ASIC will be mounted together with all the circuits that are needed to supply the chip. For this is important to focus on different parts of the ASIC. These parts are the following:

a. The power supply
b. The Voltage references
c. The current references
d. Adaptation of the input signals.
e. Digital connection with the software that we will use to measure the output of the ASIC.

In this section will be explained the selection and design of all the circuits mentioned above. These circuits are intended to provide power, reference voltages, clock signal, configuration to ASIC. Figure 3.2 describe the pinout of the ASIC. As it can be observed the ASIC have 44 pins. In Table 3.1 each pin is described.

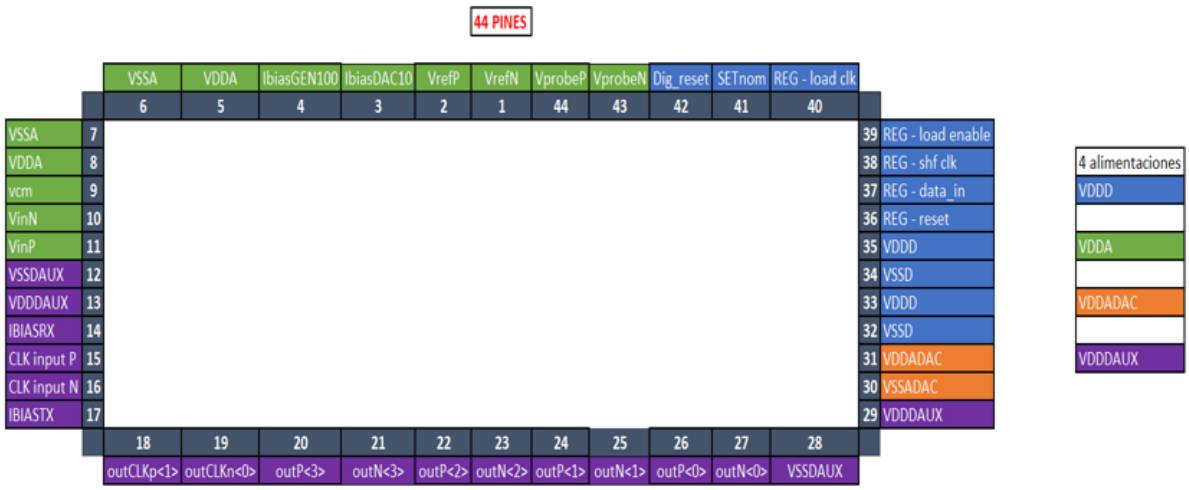

Figure 3.2 Pinout Chip LARMOR

Pin Number	Signal type and name	Alias	Value	Unit	Pin Value	Unit	Comments
1	VDC Reference for FLASH (N)	VrefN	0.275	V			V reference for FLASH
2	VDC Reference for FLASH (P)	VrefP	1.525	V			V reference for FLASH
3	Ibias current 10 uA	IbiasDAC10	10	µA	600	mV	Source current for DAC (1/5)
4	Ibias current 100 uA	IbiasGEN100	100	µA	650	mV	Source current for OAMP(1/5)
5	Analog Power Supply	VDDA	1.8	V			Power supply for the filter (OA1:5)
6	Ground	VSSA	0	V			Ground
7	Ground	VSSA	0	V			Ground
8	Analog Power Supply	VDDA	1.8	V			Power supply for the filter (OA1:5)
9	V. Common mode	Vcm	0.9	V			Voltage Common Mode for Resonator
10	Vinput N	VinN	(min 0.2)	V			Input differential signal
11	Vinput P	VinP	(max 1.6)	V			(1.6 VPP differential at full scale)
12	Ground	VSSDAUX	0	V			Ground
13	Auxiliary Power Supply	VDDDAUX	1.8	V			SPI and OA AUX (Probe)
14	Ibias current 100 uA	IBIASRX100	100	µA	900	mV	For LVDS RX pads bias (CLK input) -
15	Clock	CLK input P	160	MHz			Input Differential Clock
16	Clock	CLK input N	160	MHz			Input Differential Clock
17	Ibias current 500 uA	IBIASTX500	500	µA	720	mV	For LVDS TX pads bias (5 output pads)
18	Data_output LVDS_Clock_P	outCLKp<1>					LVDS Clock
19	Data_output LVDS_Clock_N	outCLKn<0>					LVDS Clock
20	Data_output LVDS_3_P	outP<3>					LVDS Data
21	Data_output LVDS_3_N	outN<3>					LVDS Data
22	Data_output LVDS_2_P	outP<2>					LVDS Data
23	Data_output LVDS_2_N	outN<2>					LVDS Data
24	Data_output LVDS_1_P	outP<1>					LVDS Data
25	Data_output LVDS_1_N	outN<1>					LVDS Data
26	Data_output LVDS_0_P	outP<0>					LVDS Data
27	Data_output LVDS_0_N	outN<0>					LVDS Data
28	Ground	VSSDAUX	0	V			Ground
29	Auxiliary Power Supply	VDDDAUX	1.8	V			SPI and OA AUX (Probe)
30	Ground	VSSADAC	0	V			Ground
31	IDAC Power Supply	VDDADAC	1.8	V			DAC1-5 current cells only
32	Ground	VSSD	0	V			Ground
33	Power supply for FLASH	VDDD	1.8	V			Power supply for FLASH (37 mA), Clock Delay, DAC1-5 Registers and Data output (register + binary encoder)
34	Ground	VSSD	0	V			Ground
35	Power supply for FLASH	VDDD	1.8	V			Power supply for FLASH (37 mA), Clock Delay, DAC1-5 Registers and Data output (register + binary encoder)
36	Shift register Reset	REG - reset	0/1.8	V			Reset signal for the shift register
37	Input data in the shift register	REG - data_in	0/1.8	V			Input data in the shift register
38	Shift register clock	REG - shf clk					Shift register clock
39	Load Enable	REG - load enable	0/1.8	V			Enable shift register
40	Clock	REG - load clk					Load CLOCK
41	Set all programable bits to its nominal value.	SETnom	0/1.8	V			Set all programable bits to its nominal value.
42	Allows reset of digital blocks.	Dig_reset	0/1.8	V			Allows reset of digital blocks.
43	Test signal	VprobeN	(min 0.2)	V			To test the individual integrators
44	Test signal	VprobeP	(max 1.6)	V			To test the individual integrators

Table 3.1 Interfaces all pins ASIC

For the validation of the circuits and subsequent creation of the PCB, the simulation programs Altium and Proteus have been used.

The PCB will be developed to operate with supply voltages of 3 V and 1.8 V, and with the possibility of further lowering these supply voltages to reduce

consumption. The tests performed on the system will eventually give the minimum supply voltage of the ASIC without loss of functionality.

3.1 POWER SUPPLY

The input voltage of the PCB will be a 3V. VDA voltage, which have been changed to power the PCB with a lower voltage. At first it was thought to feed with 3 V., but finally it was decided to feed with a maximum voltage of 1.8 V to reduce consumption. As the whole system is differential it is necessary the intermediate voltage so that the whole system works correctly. The necessary ones are:

- Four 1.8V voltage sources to be connected directly to the ASIC, see Table 3.1.
- An additional 1.8 V source used to generate the reference voltages required by Flash.
- A source that will generate the common mode voltage Vcm 0.9 V needed by the ASIC integrators, Table 3.1.
- Three 0.9 V sources for adapting single ended input signals to differentials.

In the Table 3.2. it is posible to see in detail the different sources.

Signal type and name	Alias	Value	Unit	Comments
V. Common mode	Vcm	0.9	V	Common Mode Voltage for Resonator
V. Common mode	VCM	0.9	V	Common Mode Voltage for input signal
Analog Power Supply	VDDA	1.8	V	Analog Power Supply
PCBAUX	VDDA_CS	1.8	V	To generate reference voltage for the Flash
Power supply for FLASH	VDDD	1.8	V	Power supply for FLASH (37 mA), Clock Delay, DAC1-5 Registers and Data output (register + binary encoder)
IDAC Power Supply	VDDADAC	1.8	V	DAC1-5 current cells only
Auxiliary Power Supply	VDDDAUX	1.8	V	SPI and OA AUX (Probe)

Table 3.2 Power supply on the PCB

3.1.1 POWER SUPPLY 1.8 V

After a thorough search among the component manufacturers, voltage regulators that met our requirements were Texas Instrument TPS79501DCQ [13]. The

TPS795 if from a family of low-dropout (LDO), ultralow noise, fast star-up, and excellent line and load transient responses in small outline, 6 pin SOT- 223. Each device in the family is stable with small 2.2-µF ceramic capacitor on the output. Values equal to or greater than 10 µF are recommended.

With this integrated, 1.8V voltage sources will be designed and simulated. Figure 3.3, shows the schematic designed.

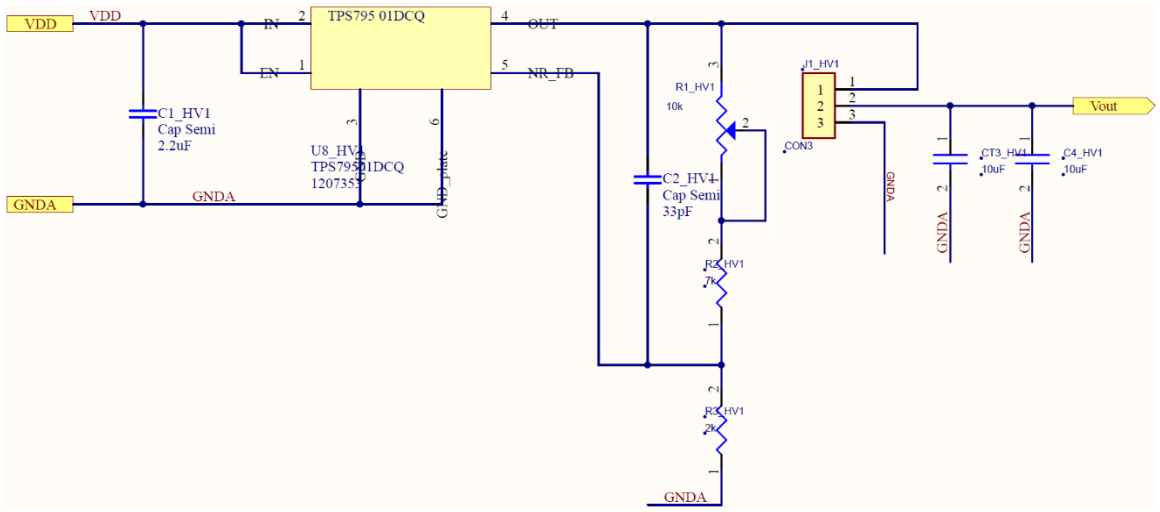

Figure 3.3 Power supply 1.8V

The output voltage of the TPS79501 adjustable regulator is programmed using external resistor divider (R_1 // R_2) as shown in Figure 3.4.

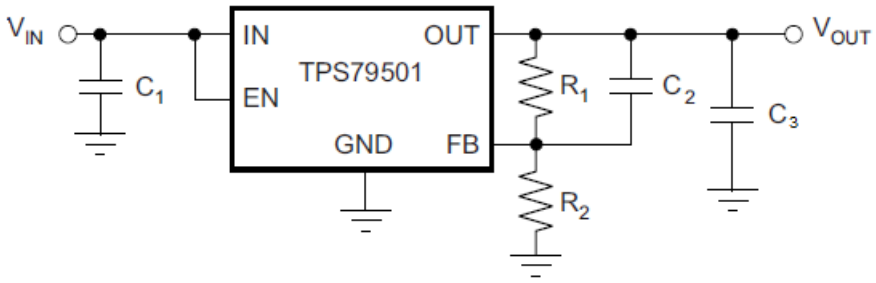

Figure 3.4 Typical Application, Adjustable Output [13]

The output voltage is calculated using equation (3.1).

$$V_{OUT} = V_{REF} * \left(1 + \frac{R_1}{R_2}\right) \quad (3.1)$$

Where

V_{REF}=1.2246 V. (internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 40 μA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided as increases the output voltage error.

The recommended design procedure when $V_{OUT} = 1.8V$ is choose $R_2 = 30.1\ K\Omega$. R_1 and R_2 is a set divider current of 40 μA, with C_2 =33 pF, and then calculate R_1 using equation (3.2).

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \qquad (3.2)$$

In this case, one capacitor of 10 μF has been used. The external supply VDD = 3V., will require that the source have V_{OUT} = 1.8 V. For this purpose R2 = 30K, and for R1 it have chosen a fixed resistance of 10K and an adjustable of 2K, this way it is possible to sweep the range from 3V to less than 1.8 V.

Test points are designed to allow the configuration of the subcircuit, isolating it from the set.

3.1.2 POWER SUPPLY 0.9 V

To form the reference Vcm of 0.9 V the chip LTC3026 [14] of the company Linear Technology was used. This voltage is used to make differential input signals. Four circuits are used, each source feeds one part of the circuit independently of the rest. This allows isolating the signals and thus to be able to detect possible errors in a simpler way.

- INPUT_VCM_TRAFO: It is connected to the output at the midpoint of the transformer of the input signal coming from the MRI sensors.
- CLKN_VCM_TRAFO: It is connected to the output at the midpoint of the transformer of the input signal clock signal which is the sampling frequency.

- OUTPUT_VCM_TRAFO: It is connected to the output at the intermediate point of the test signal transformer, which allows each of the amplifiers of the individual resonators to be tested.
- Vcm: Is the reference voltage that the ASIC needs to generate the internal differential signals is connected to pin 9.

The design of the circuit is the same for the explained four sources see Figure 3.5. At the output of the the manufacturer circuit it is recommended to be stable a small 2.2-µF ceramic capacitor on the output, values equal to or greater than 10 µF are recommended.

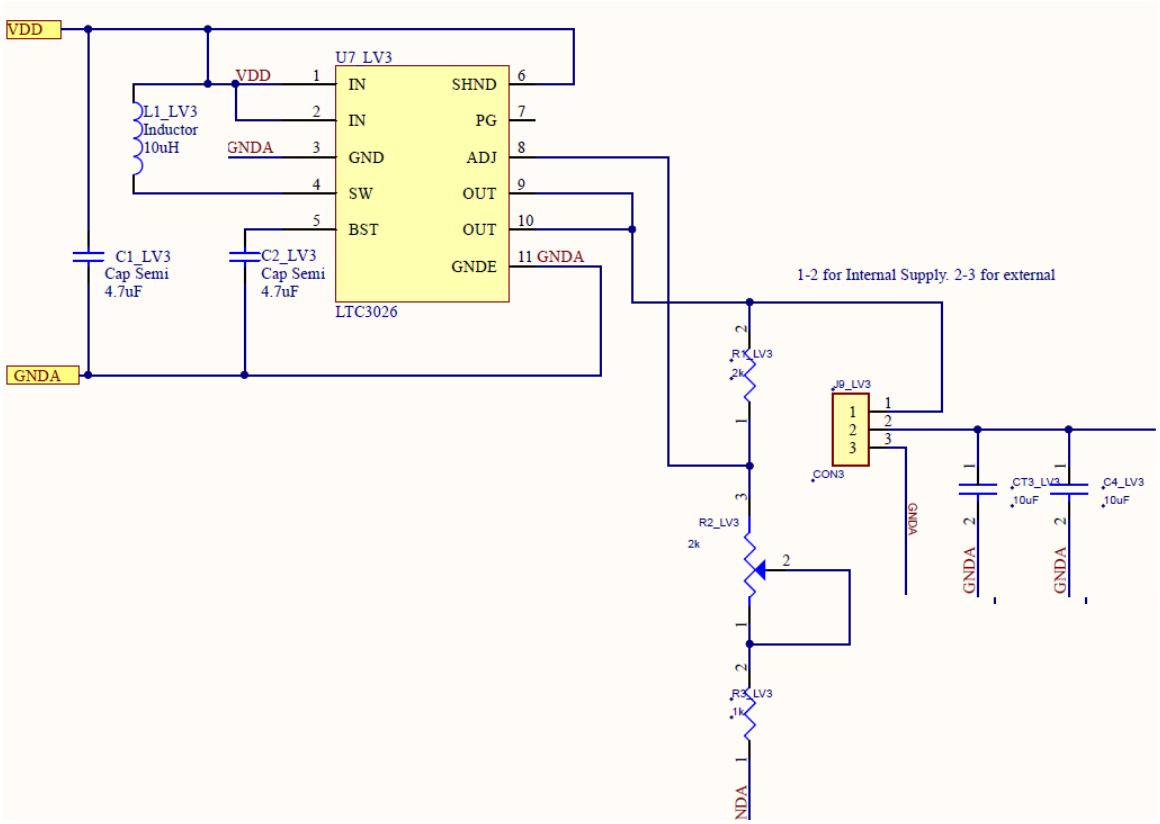

Figure 3.5 Voltage reference 0.9V

The indications of the datasheet are followed as regards the discrete elements that stabilize the chip, and as regards the resistances that allow obtaining the desired value of 0.9 V. corresponding to R_1, R_2 y R_3.

The following values are set:

- R_1= Fixed resistance of 2k
- R_2= Adjustable resistance of 2k

- R_3= Fixed resistance of 1K

The equation to be used as indicated by the manufacturer is the (3.3)

$$V_{OUT} = 0.4 * \left(1 + \frac{R_1}{(R_2 + R_3)}\right) \quad (3.3)$$

Test points are designed that allow the subcircuit to be configured, isolating it from the set.

3.1.3 VOLTAGE REFERENCE

In order to obtain the Flash references voltages of the Flash a 1.8 V source (generated in the PCB at "PCBAUX") was used.

Signal type and name	Alias	Value	Unit	Comments
VDC Reference for FLASH (P)	VrefP	1.525	V	V reference for FLASH
VDC Reference for FLASH (N)	VrefN	0.275	V	V reference for FLASH

Table 3.3 Reference Voltage Flash

The input pins of the references in the ASIC are of high impedance, therefore it was opted to obtain these voltages using two voltage dividers. They are composed with a fixed resistance and another adjustable.

3.2 CURRENT SOURCE

The ASIC has several pins that have to be connected with current sources, these pins offer a constant voltage that must be taken into account when designing the circuit. It is necessary to check the versatility of our chip therefore all the sources of intensity must operate with supply voltages from 3V to 1.8 V and even at lower voltage.

Pin Number	Signal type and name	Alias	Value	Unit	Pin Value	Unit	Comments
3	Ibias current 10 uA	IbiasDAC10	10	µA	600	mV	Source current for DAC (1/5)
4	Ibias current 100 uA	IbiasGEN100	100	µA	650	mV	Source current for OAMP(1/5)
14	Ibias current 100 uA	IBIASRX100	100	µA	900	mV	For LVDS RX pads bias (CLK input) -
17	Ibias current 500 uA	IBIASTX500	500	µA	720	mV	For LVDS TX pads bias (5 output pads)

Table 3.4 Ibias

Four sources of intensity are needed. These will connect to the different inputs of the chip. In the design of these intensity sources has taken into account the voltage of the terminal that they are going to feed.

1. **Ibias current 100uA**: The terminal of the chip (Ibias100) has a constant voltage of 650 mV (trimmed internally).
2. **Ibias current 10uA:** The chip terminal (Ibias 10) has a constant voltage of 600 mV (trimmed internally) is used in all five DACs.
3. **Ibias current 500uA**: The chip terminal (IbiasTX500u) has a constant voltage of 720 mV. It is used in the transmission of "low voltage differential signal" (LVDS).
4. **Ibias current 100uA**: The terminal of the chip (IbiasRX100u) has a constant voltage of 900 mV. It is used in the transmission of "low voltage differential signal" (LVDS).

The datasheet of commercial chip manufacturers was searched for the design of current sources, the chip chosen was an **LM334DT-CI** [15], Terminal Adjustable Current Sources, SOIC-8 from STMICROELECTRONICS.

The features are:

- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1 μA to 10 mA
- ±3% initial accuracy

According to the technical specifications, the area where the operating parameters are best in the LM334 is between 10 μA and 1 mA, which is within the working ranges of the specifications of interest. The minimum working voltage in this range is 1 V.

The internal heating can have a significant effect on current regulation for a I_{set} above 100 μA (in our case, only one source). The output current (I_{set}) has a temperature coefficient of about 0.33%/^{o}C . Thermal effects should be taken into account when the regulation is critical and I_{set} is higher than 100 μA.

The sense voltage is less than 100 mV. at this level, the thermocouple effects and the connection resistance should be reduced by locating the current setting resistor close to the device. Do not use sockets for this Integrated Circuit (IC).

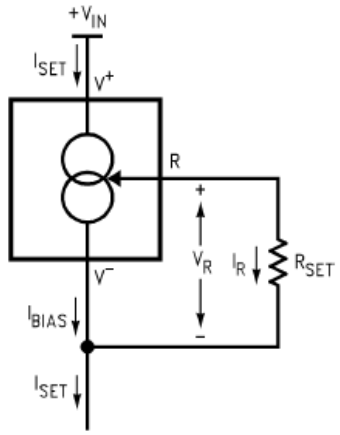

Figure 3.6 Current Source [15]

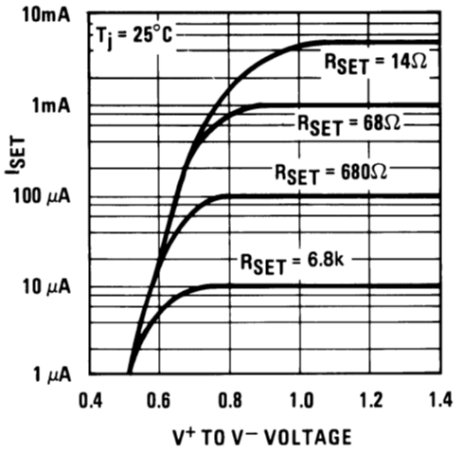

Figure 3.7 Turn on voltage [15]

Figure 3.7 shows the circuit to be used in all current sources. The R_{SET} in all of them will be adjustable resistors.

The purpose of the calculation is to obtain the value of the resistance for the supply voltage to 3 V and 1.8 V and with this value choose the adjustable resistance that is to be implemented in the PCB.

The datasheet gives us the equation (3.4) for the calculation of the intensity for a given temperature and resistance. The values will be calculated for a temperature of 298ºK.

$$I_{SET} = \frac{\left(\frac{227\mu V}{ºK}\right) * T}{R_{SET}} \tag{3.4}$$

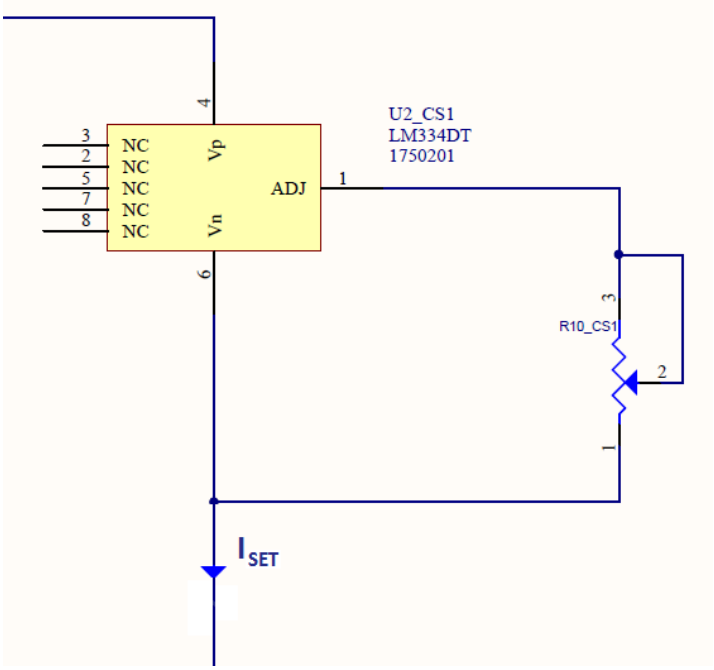

Figure 3.8 Schematic current source

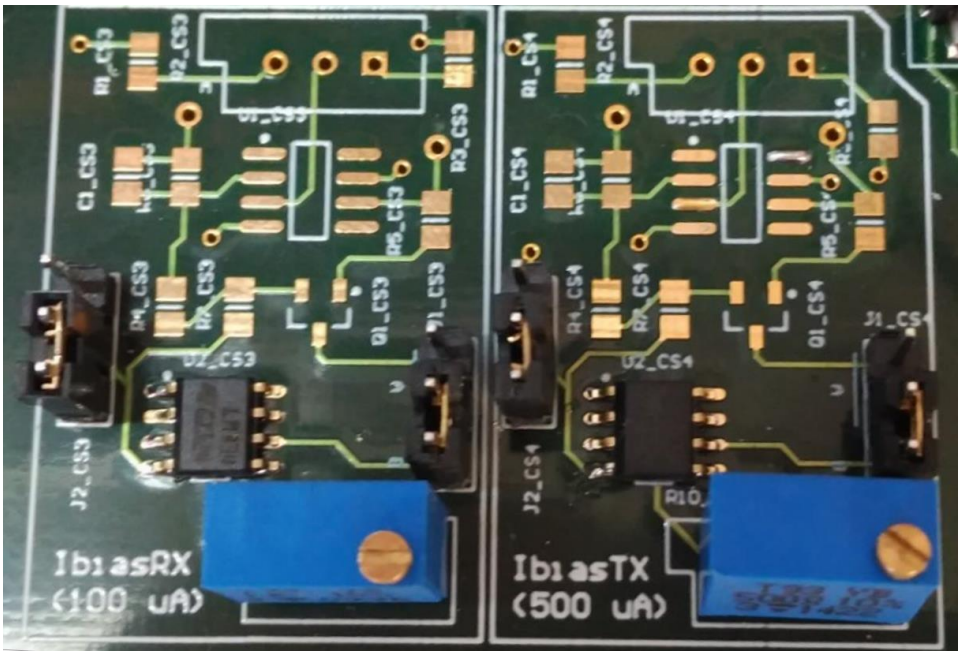

Figure 3.9 Picture of Current Source

As it is possible to see in Figure 3.9 in the area of current sources, is possible to see tracks without elements and without connecting.This is because initially two types of sources were designed in case the main design failed, without having to develop a second PCB, the first design worked correctly.

3.3 ADAPTATION OF INPUT SIGNALS. RF TRANSFORMERS

The ASIC is integrated into a signal receiving system within a magnetic resonance device. The signals to be processed will be those received from the sensors when operating in a real way. However, for testing purposes a pure input sinusoidal tone or tone signal is used.

The whole system is differential (not single-ended). Differential signals are used because more resolution is obtained, and also with these systems the noise can be eliminated. The laboratory signal generator used to generate both the signal and the clock signal produces signals single-ended. In order to generate a differential signal a RF transformer will be used. In Figure 3.10 is possible to see a representation of an RF transformer that converts a single-ended signal to differential.

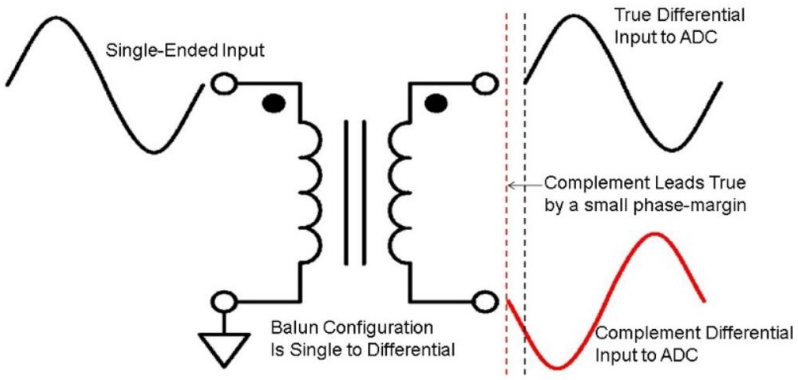

Figure 3.10 Transformer Single-ended to differential signal [16]

These RF transformers are also achieved by a differential signal. It was also possible to electrically isolate the system signal processing.

The midpoint of the secondary coil will be supplied with the VCM voltage of 0.9 V, which is the DC voltage over which the differential signals.

Three inputs are available for three input signals:

- Signal to process: 5 MHz
- Clock signal of the ADC: 160 MHz
- Test signal: This input will be used if there is a malfunction of the ASIC, in order to be able to test the different integrators of the ADC.

It was selected two different surface mount wideband RF transformers from Coilcraft enterprise.

Type	Part number[1]	Impedance ratio[2] pri:sec	Bandwidth (MHz)	Idc (mA)	Insertion loss max (dB)	Primary (pins 1-3) L min[3] (µH)	Primary (pins 1-3) DCR max (Ohms)	Secondary (pins 6-4) L min[3] (µH)	Secondary (pins 6-4) DCR max (Ohms)
 Type B	PWB-4-BL_	1:4	0.14 - 700	250	0.50	25	0.075	98	0.135
	PWB-16-BL_	1:16	0.075 - 90	250	0.30	75	0.260	1250	0.910

Table 3.5 Technical features [17]

PWB-16-BL will be used for the input signal as it allows to pass the frequencies up to 90 MHz. Thus, it will let pass the 5 MHz signal.PWL-4- allows to pass the frequencies up to 700 MHz, so the clock signal of 160 MHz will pass without problems the.

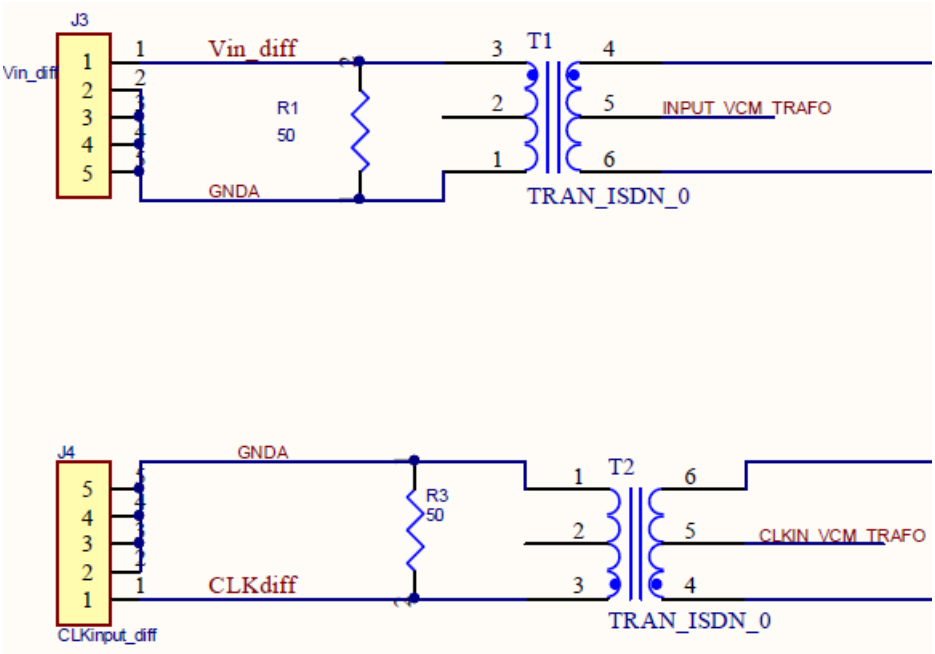

Figure 3.11 Circuit Single-ended to differential signal

3.4 CONTROL SIGNALS. ARDUINO CONNECTIONS

In order that the operation of the circuit is not influenced by the input or output signals, the signals coming from the Arduino system will be specially adapted using optical adapters. In this way it is guarantee that the operation of the system is not altered by these external signals.

The circuit that adapts these signals is shown in Figure 3.12.

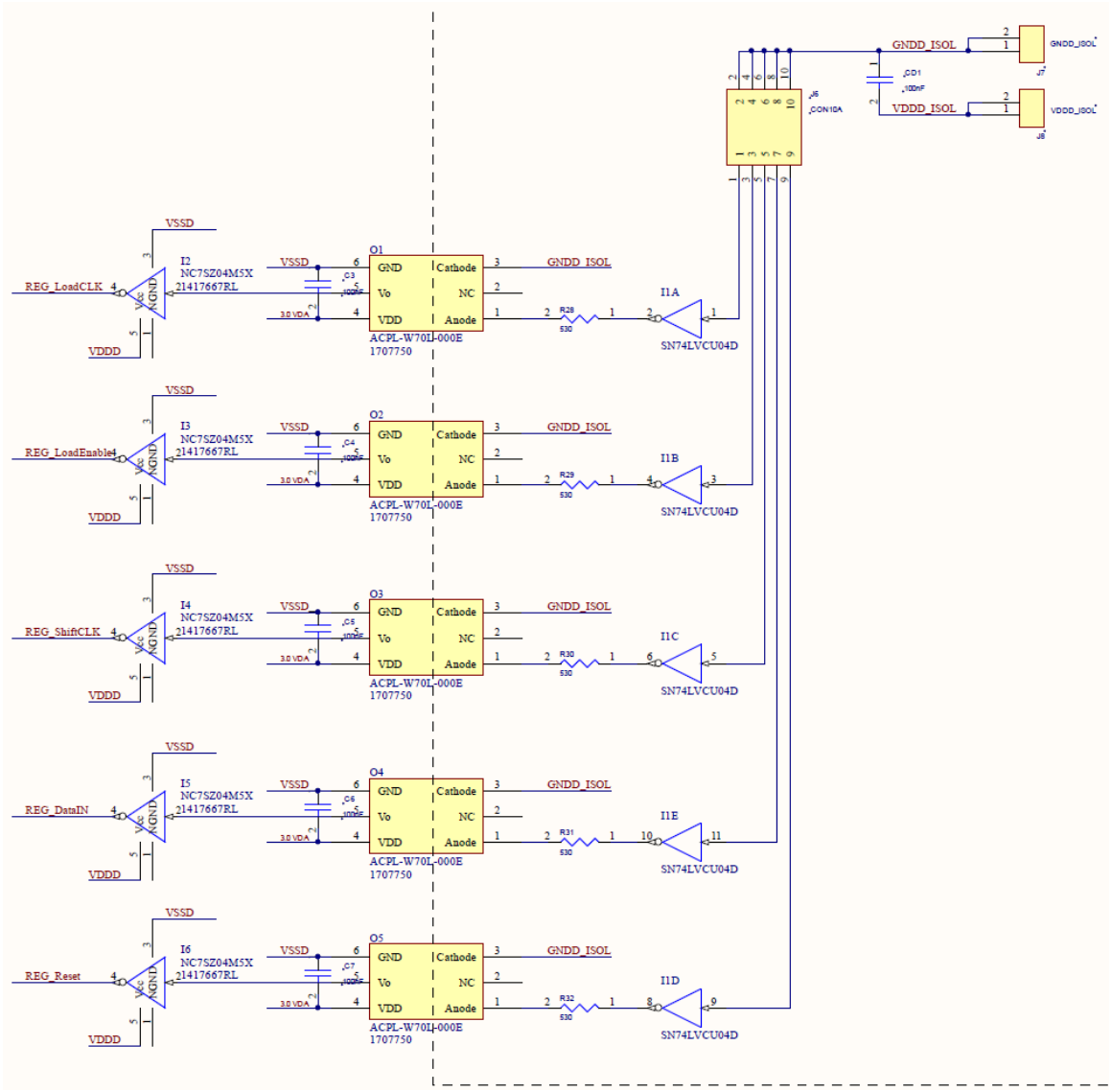

Figure 3.12 Isolated Arduino signals

There are five equal circuits that isolate the signals coming from the Arduino system. The circuit will be detailed below.

The system is powered from two independent sources. The part of the circuit that treats the signals of the Arduino system is powered by a source independent of the ASIC general power and the circuit area of the ASIC is powered by ASIC power supplies, which guarantees the isolation of the system.

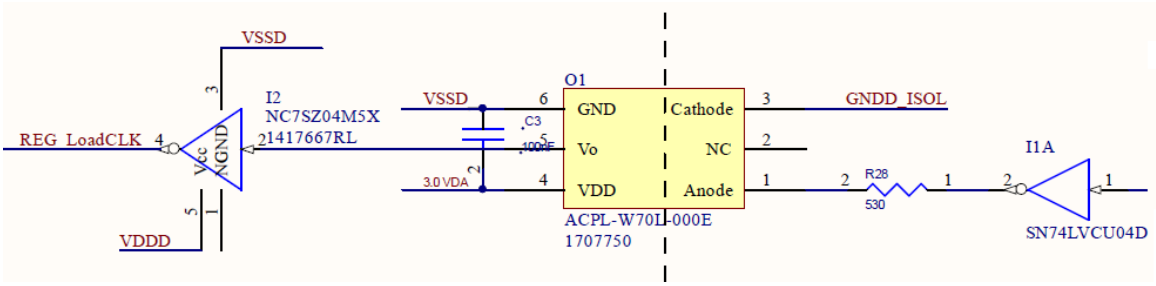

Figure 3.13 Individual Arduino signal circuit

For this circuit, three integrated circuits have been used:

- **SN74LVCU04D** [18]: Is a chip that integrates six inverters. The aim is to restore the tensions coming from the Arduino to the nominal values of feeding. In this way, the power delivery is not performed by the Arduino system, but by the inverter.
- **ACPL-W70L-000E** [19]: Is a chip that integrates an optocoupler.
- **NC7SZ04** [20]: Is an individual inverter that undoes the operation of the previous inverter.

The already isolated input signals will enter the SHIFT REGISTER implemented in the ASIC, which is used to program the internal parameters of the chip.

3.5 OUTPUT SIGNAL. LVDS SIGNAL TRANSMISSION

The input signal is processed by the ASIC generating an intermediate signal of 15 values (<0:14>) which once passed through the Thermometer becomes a 4-bit signal. This CMOS signal is converted in a post-thermometer step into a LVDS signal in addition to the clock signal within the ASIC. These signals are processed by a logic analyzer, Agilent 16902A The PCB will have 10 outputs, two clock signals and 8 from data (differential signals), with their respective connectors.

To transmit the signal the system that has been chosen is the **LVDS**, is a technical standard that specifies characteristic of a differential transmission. LVDS operates at low power and can run at very high speeds using twisted-pair copper cables.

In the following sections will be explained the differences between a System transmission single-ended and differential.

3.5.1 SINGLE-ENDED TRANSMISSION

Single-ended transmission is performed by using one signal line for each information channel and a common ground return path shared among numerous information channels. Figure 3.14 shows the electrical schematic diagram of a single-ended transmission system. Single-ended receivers interpret the logical state at their inputs based upon the voltage at the single input line with respect to ground. [21]

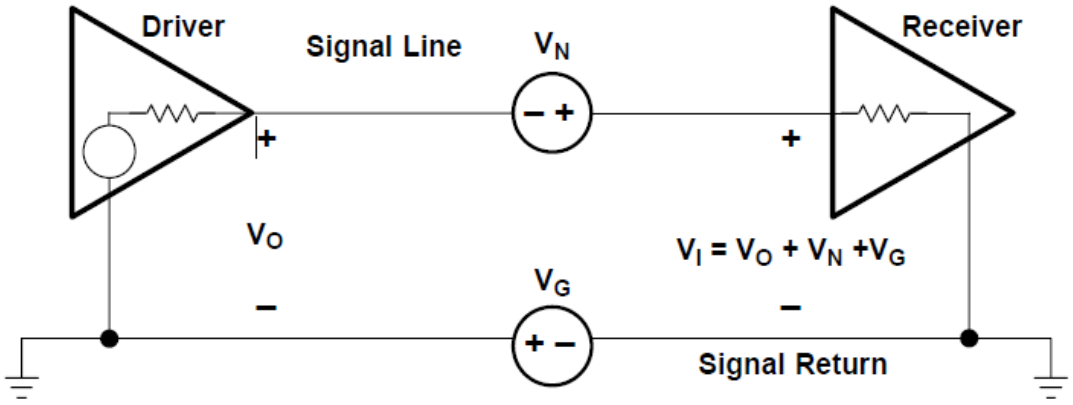

Figure 3.14 Single-Ending Interface Circuit Schematic Design [21]

The advantages of single-ended transmission are the simplicity and low-cost implementation. A single-ended system requires only one line per signal. It is therefore ideal when cabling connector costs are more important than the signalling rate or transmission distance.

The main disadvantages of the single-ended solution is its relatively poor noise performance at high signalling rates or long distance. Because the noise coupled to the circuit adds to the signal voltage, it is susceptible to data errors. The signal line of a single-ended circuits acts as an antenna to radiate and receive electric fields while the area formed around the circuit path is an antenna for magnetic fields. The voltage source V_N, as shown in Figure 3.14 represent this high-frequency electromagnetic coupling. Since single-ended interface circuits generally share the return path with other circuits, there is also a component of conducted susceptibility as changes in ground current create the ground noise voltage represented by V_G. This noise generally low in frequency (i.e. 50 Hz). [21]

3.5.2 DIFFERENTIAL TRANSMISSION (LVDS)

Differential transmission addresses many of the shortcomings of single-ended solutions by using a pair of signal lines for each information channels. Figure 3.15 shown an electrical schematic diagram of a differential transmission system. The differential driver uses a pair of complementary outputs to indicate the state transmitted. The differential receiver detects the voltage difference between the signal pair, rather than relative to ground, to determine its output state. [21]

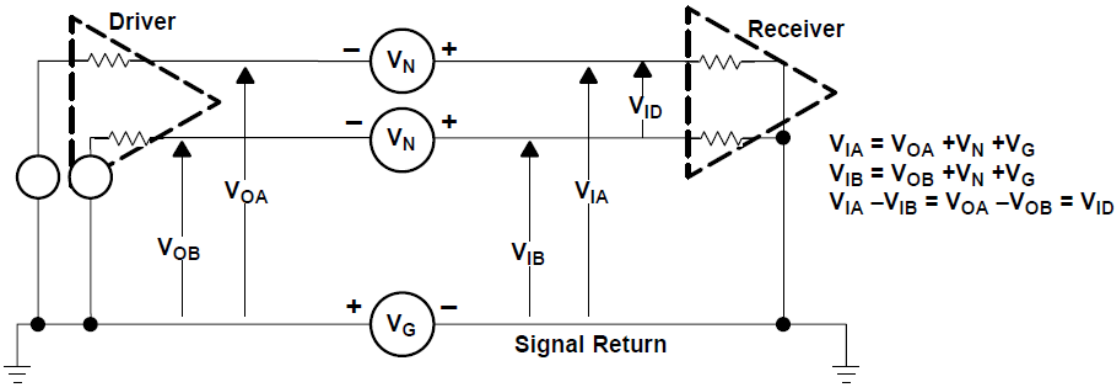

Figure 3.15 Differential Interface Circuit Schematic Diagram [21]

This mode of transmission has several important advantages over single-ended. You can see the fundamental advantage in the derivation of the differential input voltage $V_{D,}$ in Figure 3.15. The noise source V_N y V_G add to the inputs signal V_{IA} and V_{IB}, just as with single-ended circuit, but taking the difference between the two input voltages, the common noise terms are cancelled from the desired signal. The differential receiver accomplishes this and, with small differential input voltage thresholds, maintains high signal-to-noise ratios. [21]

There is a presumption that the V_N coupled to each signal are equal or nearly so. Differential signal pairs that are close together are generally expose to the same noise sources. Twisting the signal wires together adds to this advantage. This ensures similar exposure to electric fields and cancels differential electromotive force (emf) from magnetic field coupling by reversing the polarity in adjacent loops created by the twist. [21]

In addition to noise immunity, differential circuits radiate substantially less noise to the environment than single-ended circuits. This is primarily due to the complementary current in each line of the signal pair cancelling each other´s generated

fields. Conducted noise is also lower because there is little common-mode current to circulate through the signal return path. [21]

The logic of decoding the signal can be seen in Figure 3.16. When (VA- VB) is positive, the transmitted signal is "1" and when (VA-VB) is negative the transmitted signal is "0".

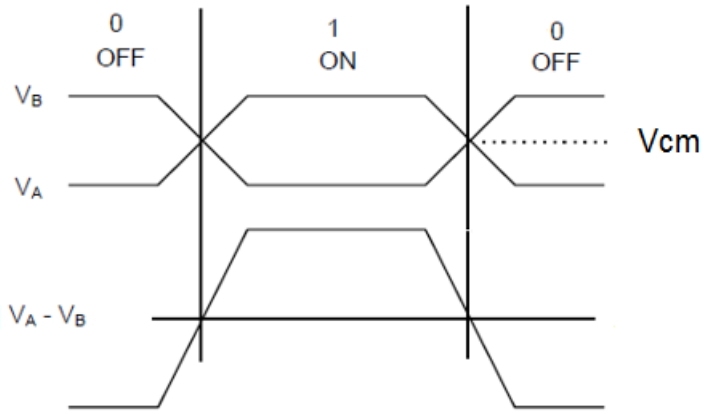

Figure 3.16 LVDS Signalling decoding

3.5.3 COMPARING SERIAL AND PARALLEL DATA TRANSMISSION

LVDS works in both parallel and serial data transmissions. In parallel transmission multiple data differential pairs carry several signals at once including a clock signal to synchronize the data. In our case four signal data and one clock in totally ten lines. In serial communications, multiple single-ended signals are serialized into a single differential pair with a data rate equal to that of all the combined single-ended channels.

Parallel data transmission achieves higher speeds than with serial transmission. As our Flash converter offers 15 levels of quantification <0:14>, Figure 3.17 .What has been done is to encode the signal with a thermometer to binary obtaining a signal of 4 bits. The next step is to treat these four bits plus the clock signal with a CMOS to LVDS converter obtaining 5 differential signals in parallel (10 pins of the ASIC). These can be transmitted in parallel which is simpler at the hardware level than serializing the data.

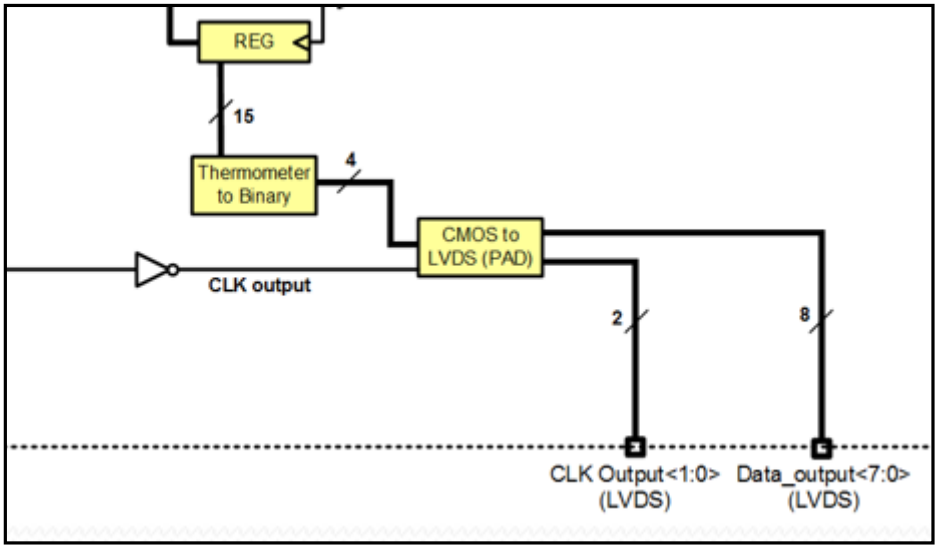

Figure 3.17 CMOS to LVDS

4 FINAL PCB AND INSTRUMENTATION

This chapter shows the photographs of all the circuits that make up the PCB as well as their layout on the final PCB, this section shows on a final PCB as Project **Objective 2** has been fulfilled.

All the necessary instrumentation for the ASIC was described in chapter 3 . The printed circuit object of this project is shown in Figure 4.1, on the board can be seen labelled the different elements of the instrumentation. It is possible to see in Figure 4.2 the schematic obtained from Altium. Here is shown the circuits the instrumentation required by the ASIC for the tests.

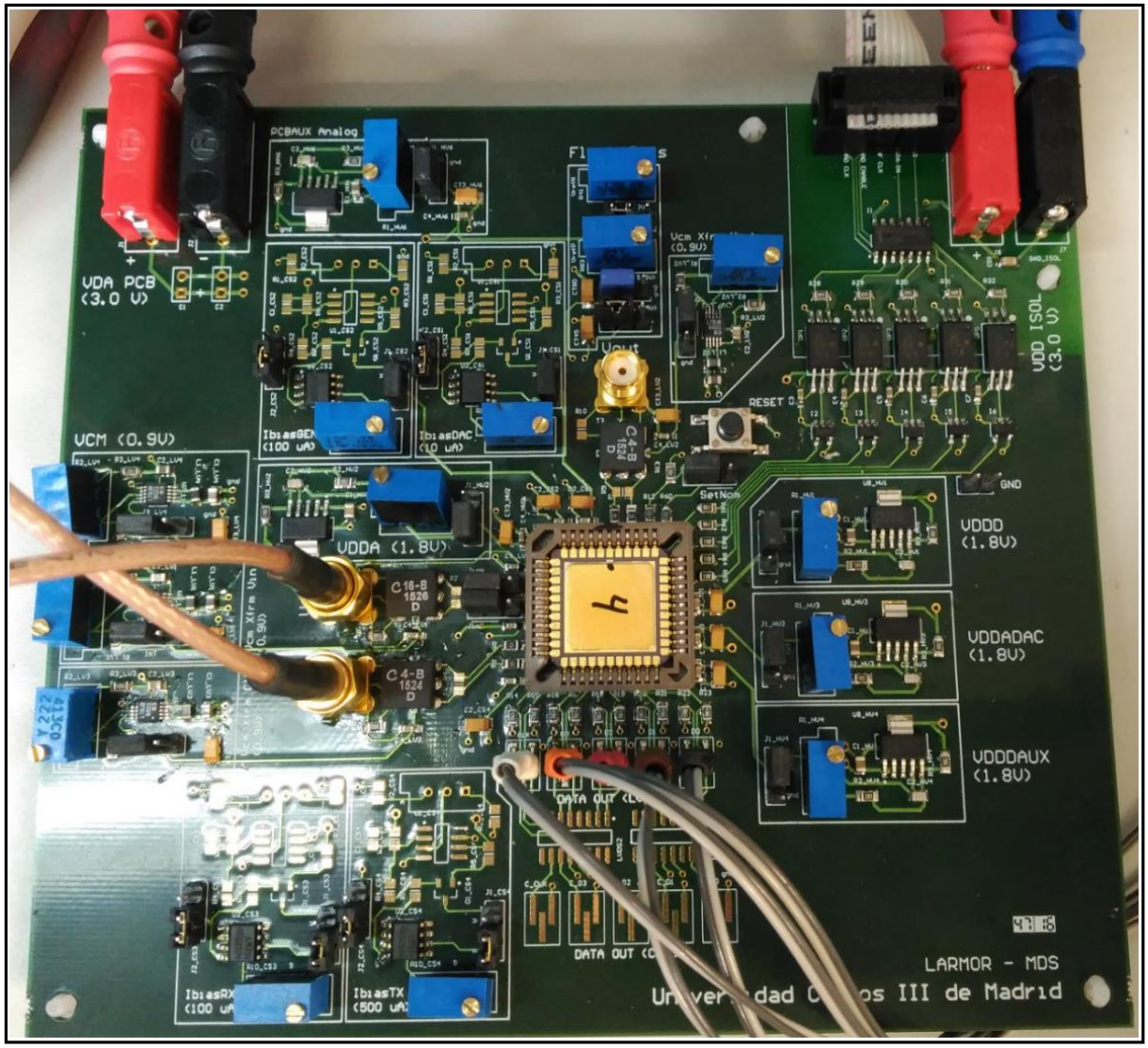

Figure 4.1 PCB for he ASIC characterization

Two templates generated by the Altium program, which have been used for the manufacture of the PCB can be consulted in ANNEX III PCB Layout .

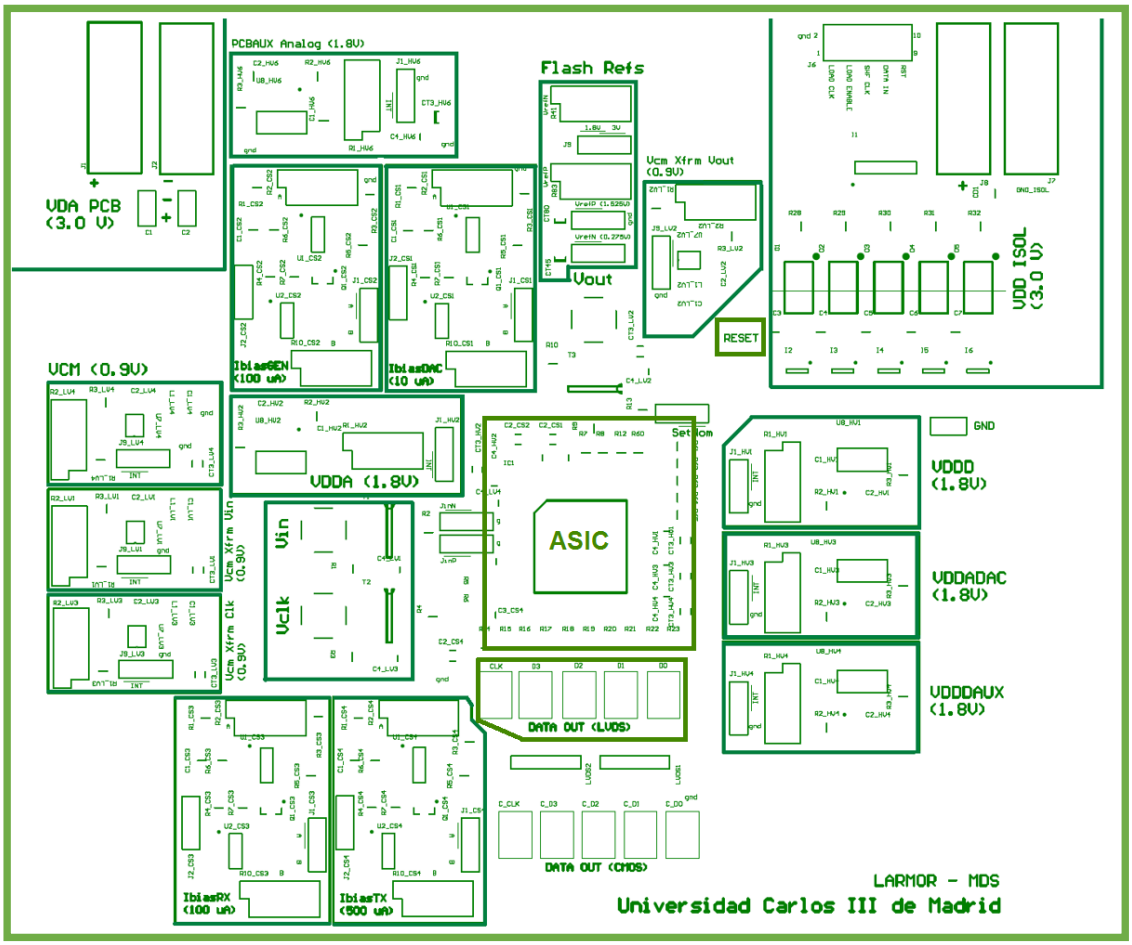

Figure 4.2 Schematic of the PCB with the restyled subsystems

The different feeds are shown in Figure 4.1 and Figure 4.2, as well as the inputs and outputs:

- Power supply: see section 4.1. and 4.2
- Current sources: see section 4.4 and 4.5.
- Input of the test signal with two coaxial cables: see section 4.6
- The outputs of the LVDS transmission with 5 pairs of cables: see section 4.6
- The control bus of the Arduino system: see section 4.6.

The following sections will show detailed photos of the different subsystems.

4.1 EXTERNAL POWER SUPPLY

The board is externally powered with 3V and the ASIC's Shift-Register programming input, which comes from the Arduino microcontroller system with another 3V source. The two feeds are from different sources to ensure the electrical insulation of the Arduino inputs. For these feeds has been used the power supply "**PROGRAMABLE POWER SUPPLY HM7044**" form enterprise HAMEG.

The interior of the ASIC is shown with the power domains in Figure 4.3. The different parts of the integrated circuit have been marked indicating that the voltage source feeds them and you can also see where the different Ibias.

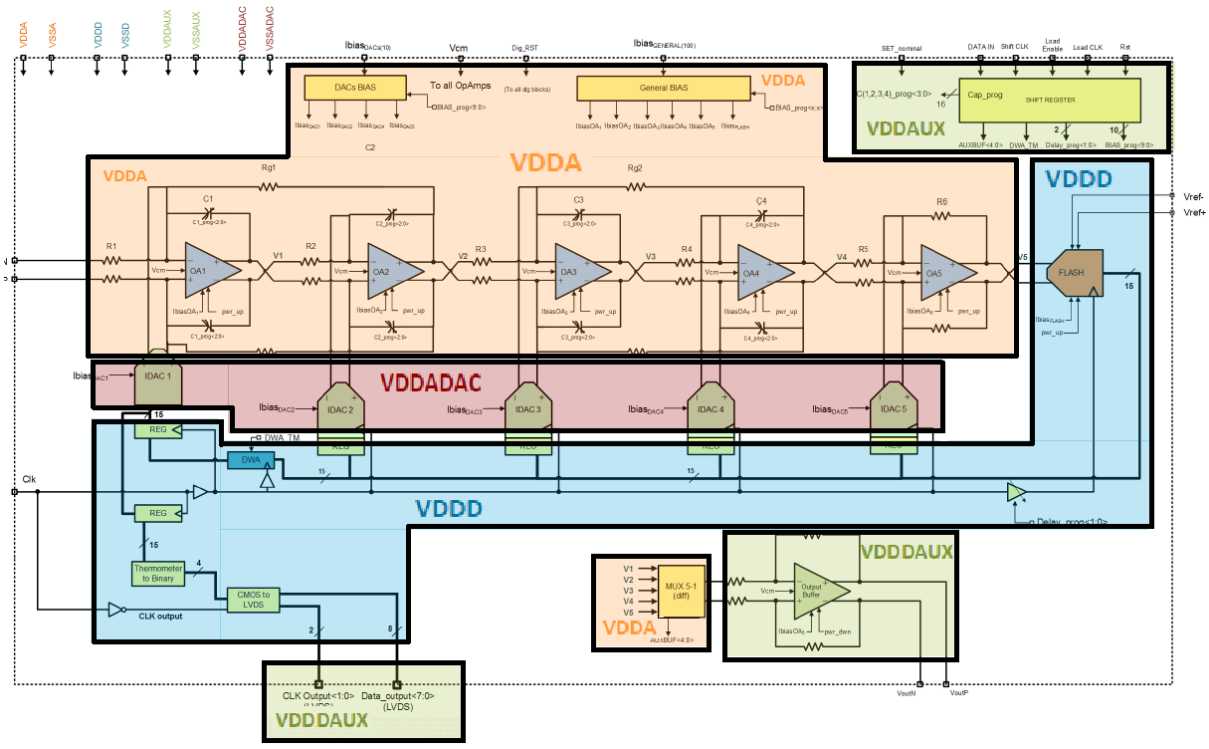

Figure 4.3 ASIC Power domain

The general power input of the PCB labeled as VDA PCB (3 V) and the input of the Shift-Register programming input circuit (which optically isolates the Arduino from the ASIC) are shown in Figure 4.4.

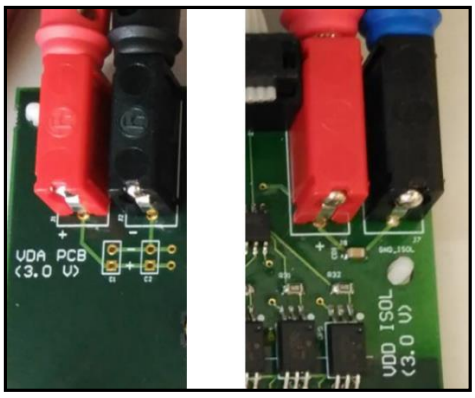

Figure 4.4 External PCB power supply VDA PCB and VDD Isol Arduino

4.2 INTERNAL POWER SUPPLY

1.8V power supply. As described in section 3.1.1 The FLASH-type decoder that has built in the ASIC, requires two reference voltages (1,525 V and 0.275 V) that are obtained from the power supply labeled as **PCBAUX Analog**.

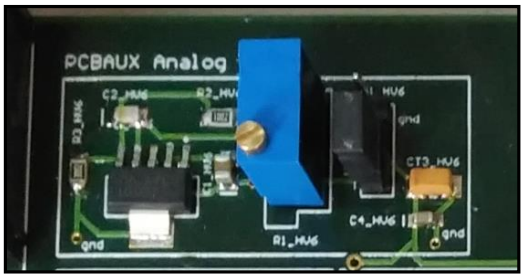

Figure 4.5 Internal PCB power supply 1.8 V to obtain reference voltages for FLASH

The references are obtained from two voltage dividers, see Figure 4.6

Figure 4.6 Circuit reference voltages for FLASH

The four adjustable sources of 1.8 V of nominal value that are in charge of feeding the different power domains of the ASIC (see Figure 4.3) are shown in Figure 4.7 . These power supply were described in section 3.1.1.

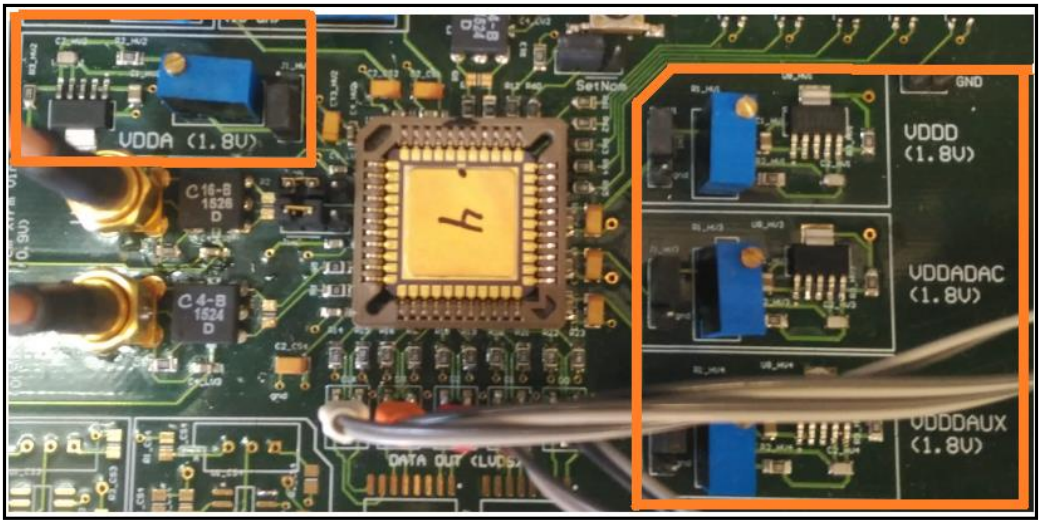

Figure 4.7 Internal PCB power supply 1.8 V

4.3 DIFFERENTIAL VOLTAGE REFERENCE

The whole system is differential, so it is necessary to generate the intermediate voltage of 0.9 V, labeled **VCM** in Figure 4.8. The three sources were described in section 3.1.2.

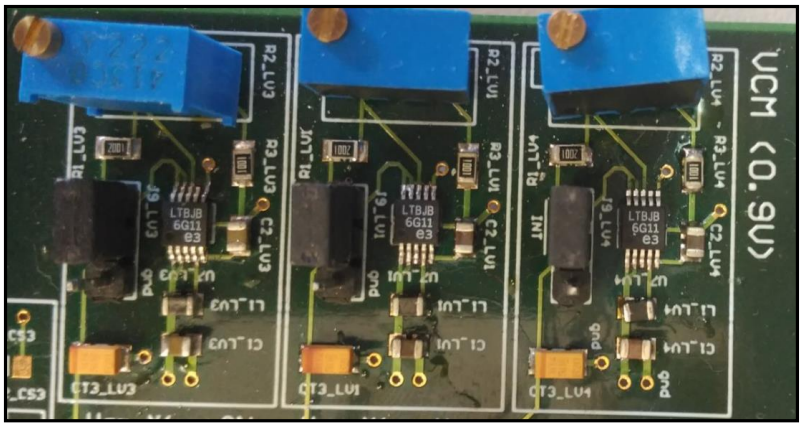

Figure 4.8 Internal PCB power supply 1.8 V

The above sources are required by the external instrumentation of the ASIC, but the ASIC also needs a reference of 0.9 V (which provides this reference is the circuit labeled Vcm) see Figure 4.9.

Figure 4.9 0.9 V differential ASIC Reference

4.4 IBIAS CURRENT

To compensate the Ibias currents of the internal circuits, in the integrators and the DAC are necessary sources of currents see Figure 4.10.

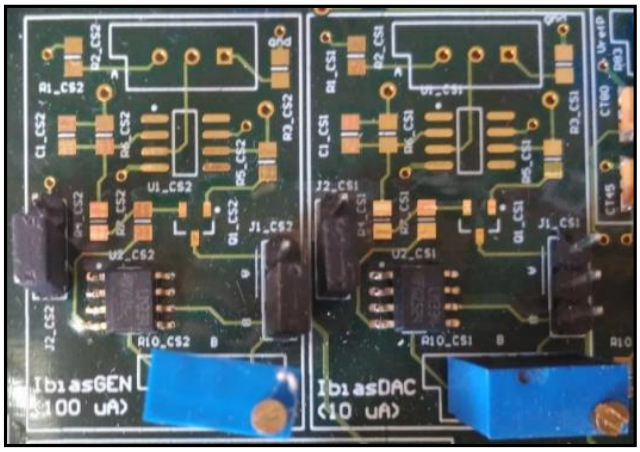

Figure 4.10 Ibias OpAmp and DAC

In Table 3.1, the IbiasGEN of 100 μA is the one that feeds the integrators and the IbiasDAC of 10 μA is the one that feeds to the DAC.

4.5 IBIAS CURRENT LVDS

In order to transmit the LVDS data, two sources of current:

- 100 μA IbiasRX for LVDS reception
- 500 μA IbiasTX for LVDS transmission

It is possible to see these two circuits in Figure 4.11 .

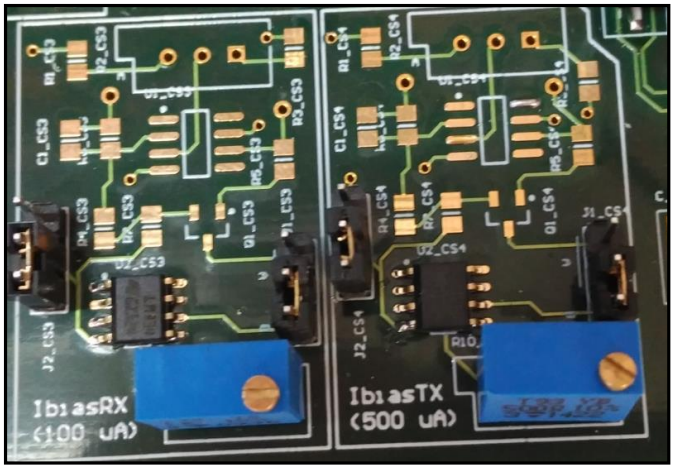

Figure 4.11 Ibias OpAmp and DAC

4.6 DATA INPUT / DATA OUTPUT

For the tests it has had to simulate the differential input signals to the System. As the generators that were used were single ended, it has been necessary to pass to differential. The coaxial cables of the input signal and the clock as well as the two RF Transformers that make the change are passed from single ended to differential. These are shown in Figure 4.12.

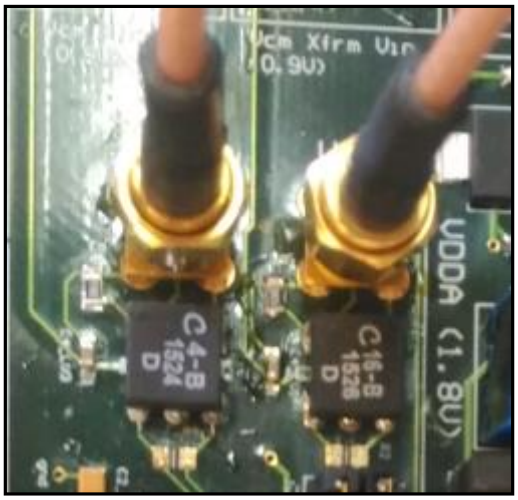

Figure 4.12 Input signal adaptation circuit

The internal parameters of the ASIC are programmed with the Matlab script using the Arduino System. Therefore, a system with optocouplers has been designed to electrically isolate the Arduino system from ASIC, see Figure 4.13.

Figure 4.13 also shows the connection of the PCB data bus with the Arduino System.

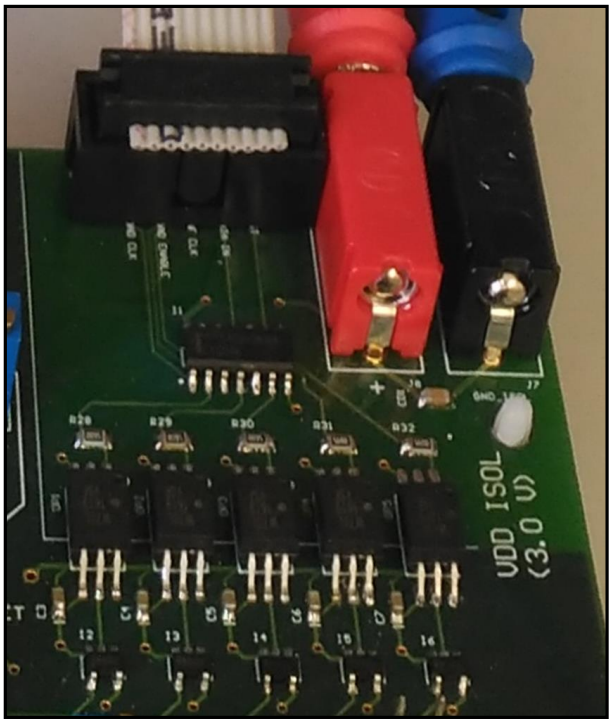

Figure 4.13 ISOL Arduino circuit.

Finally, the data are transmitted using LVDS. In Figure 4.14 are the five connectors with two pairs of cables for each transmitted bit, 4 bits plus the total clock 5 pairs of cables.

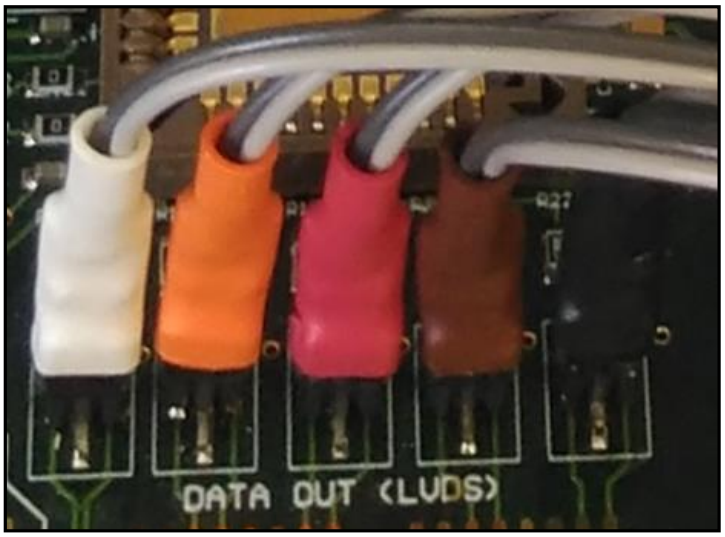

Figure 4.14 DATA OUT LVDS.

5 CONNECTIONS AND CLOSE CONTROL LOOP

This chapter presents the loop used to perform ASIC characterization tests. It shows the measuring devices used as well as the Sw that has been programmed in Matlab that allows the systematic realization of these tests (**objective 3).** Also on Matlab has been developed the Sw which calculates the figures of merit and graphs of the FFT of the modulator which allows the evaluation of the tested configuration (**objective 4**). The ultimate goal is to achieve optimal parameters that allow the ΣΔ ADC to achieve its best performance.

Once the Hw is designed, it is necessary to characterize the ASIC and process the data obtained from each of the obtained configurations.

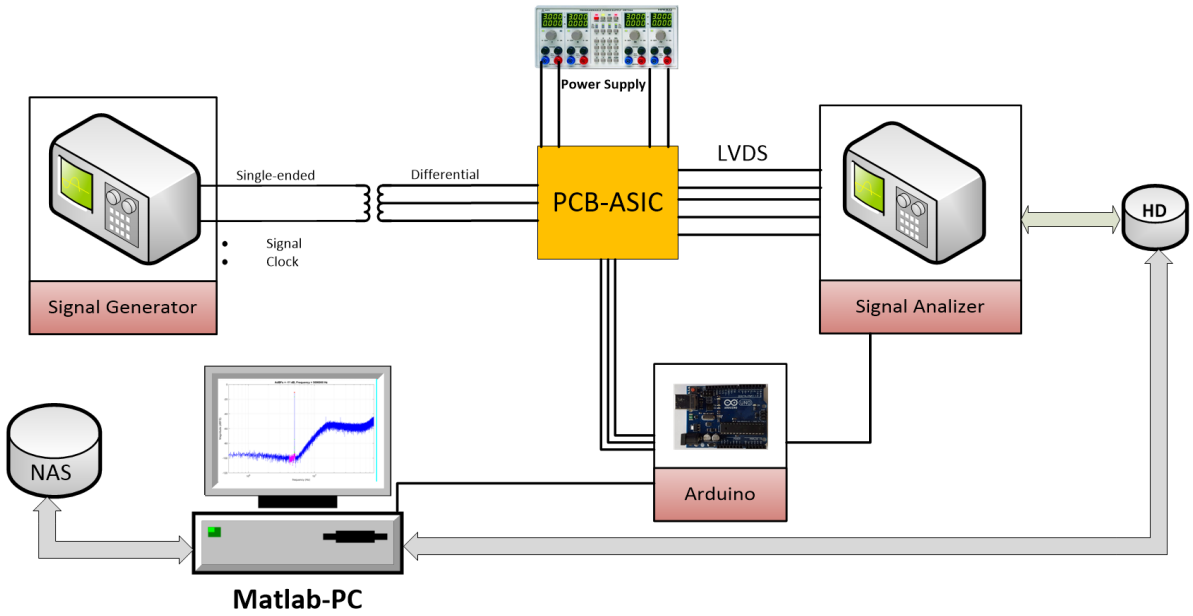

Figure 5.1 Connections

In Figure 5.1 it is possible to see all the connections needed to interconnect the PCB containing the ASIC with the laboratory measuring devices:

- **Power supply**: "**Programmable Power Supply HM7044**" by HAMEG, with this power supply it is possible to get the 3V power from the PCB.
- **Signal Generator_1**: "**Programmable Synthesizer HM8134-2**" by HAMEG with this generator it is possible to get the test signal.
- **Signal Generator_2**: "**Vector Signal Generator SMV-03**" by Rohde & Schwarz, with this generator it is possible to get the clock signal.

- **Signal Analizer**: **Logic Analyzer** is used, **Agilent 16902A, w**hich processes LVDS signals and generates a csv file.

The control and analysis of the data of the system is realized:

- **Pc**: A Pc with Matlab will be used with the control library of the "Arduino" microcontroller system. The Pc will govern the "Arduino" system and will have access to the HDD of the Logic Analyzer and the departmental Network Attached Storage (NAS).
- **Arduino**: Figure 5.2, will be connected via USB to the Pc-Matlab through a data bus to the PCB in order to transmit the configuration signals to the ASIC Shift Register. By means of a cable connect to the Logic Analyzer, it indicate the beginning of the data capture.

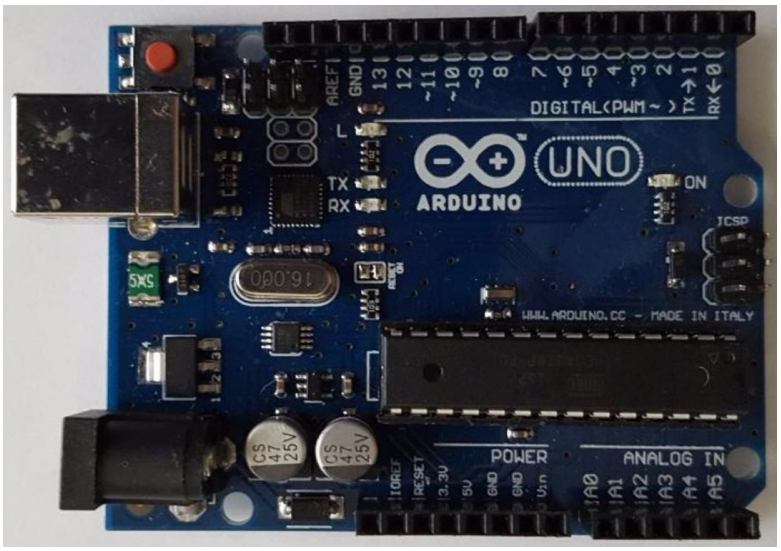

Figure 5.2 Arduino

Before starting the tests, it is necessary to configure the Logic Analizer to read LVDS signals. The start of the data capture is ordered by the Matlab script by means of a signal to the pin "D5" of the "Arduino" see Figure 5.2. The logical analyzer is programmed to capture the data and generate a file that stores in its HDD.

The control of the whole test is done from a Matlab script that has a main module and three functions:

1. **Main module:** ADC_Test_script. It establishes the communication with the Arduino and establishes the initial values of the Ibias of the DAC (DAC1,2,4,5) and the initial values of the capacitors C1: C4 of the integrators.
2. "**program_chip**" **function:** this function is in charge by the Arduino system to send the necessary data to the ASIC Shift-Register to configure the desired values.
3. Function "ADC_Analyzer_Automatic", this function is responsible for:
    a. Start the capture.
    b. Wait 9 seconds for the logical analyzer to capture the data and generate the csv file, saving it to the HDD.
    c. Calculate the parameters necessary for the calculation of FFT.
    d. Process the data obtained from the FFT.
4. **Function calcSNR1_v5:** this function is protected by copyright. It is the function that performs the calculations of the FFT.

Once the capture is done the ENOB is checked, if it is less than 12 the tested configuration is rejected and the data is saved. The ASIC is reconfigured with new parameters and the loop is repeated. In Table 5.2 a test sequence is shown where it can be seen that the maximum value reached in that test is 12.57 ENOB with a SNR of 64.5 dB.

The test parameters are as follows:

1. 5 MHz tone, with different input voltage values.
2. Dual tones in the range [4, 5] MHz, to test intermodulation (IMD).

Multiple tests have been performed for the optimal characterization of ASIC. The first objective of these tests is to find out what the values of the variables that obtain the best performance from the ADC. The main objective is to confirm that the ΣΔ ADC of 4^{th} order meets with the hypotheses and theories used in its development, as well as to detect the possible problems of the system.

It is desired to systematically find that capacitor and Ibias configuration in the DACs that provide the best SNR and SNDR.

The possible configurations are too high to test them all. The Department of Electronic Technology of the Carlos III University of Madrid has a proprietary tool developed in Matlab that allows to design and optimize an H (s) function, in this case the data were the ones being used:

- Clock=160 MHz
- IF= 4.5 MHz
- Quantizer and DAC size: 4 bits
- Delay between quantizer clock phase and DAC clock phase: 1/2 clock period

$$H(S) = \frac{0.5481\,s^4 + 1.6331\,s^3 + 0.9646\,s^2 + 0.4165\,s + 0.0938}{s^4 + 0.0771\,s^2 + 0.0015}$$

The input full-scale amplitude of de CT ΣΔ ADC is defined by the reference voltage of the 4-bit quantizer, has been set to 1.6 V. With all these data the best values for the capacitors C1 to C4 have been obtained as well as the currents of the DAC by means of simulation. The ASIC has been manufactured with the calculated values for these capacitors, these will be the nominal values, see ANNEX I Programming bits, These bit-encoded values are shown in Table 5.1. These will be the starting point for testing sweeps:

DAC1	DAC2	DAC4	DAC5	C1	C2	C3	C4
2	2	2	3	8	8	8	8

Table 5.1 Initial data for sweeping test

Before sending the ASIC to fabrication. It has been done multiples simulations with CADENCE program in order to validate the calculated values.

With these initial values is necessary to perform a systematic sweep of tests around the values where the best performance of the system is supposed to be.

There have been several sweeps tests. Table 5.2 shows the best results of one of these sweep with 4091 tests. In this table it is possible to see the values that can take the different variables.

The combination of values tested was as follows:

- DAC1, DAC2 and DAC4: values from 0 to 3
- DAC5: values from 0 to 7 (Only tested 1, 3, 5, 7)
- C1, C2, C3 and C4: values from 0 to 15 (Only tested 3, 7, 11 and 15).

				DACs, rank:					Rank caps:				
				Value 0 a 3			0 a 7		Value 0 a 15				Order
Proof	AdBFS	SNR	ENOB	DAC1	DAC2	DAC4	DAC5		C1	C2	C3	C4	
2610	-12.938	64.5	12.574	0	3	1	1		11	11	15	15	1
2594	-13.123	64	12.514	1	3	1	1		11	11	15	15	2
2674	-12.261	64.7	12.491	0	2	1	1		11	11	15	15	3
2611	-12.411	64.5	12.484	0	3	1	1		7	7	15	15	4
2578	-13.311	63.5	12.472	2	3	1	1		11	11	15	15	5
2562	-13.5	63.3	12.467	3	3	1	1		11	11	15	15	6
2738	-11.524	65.3	12.464	0	1	1	1		11	11	15	15	7
2642	-12.687	64.1	12.459	2	2	1	1		11	11	15	15	8
2691	-12.159	64.6	12.451	3	1	1	1		7	7	15	15	9
2626	-12.901	63.8	12.451	3	2	1	1		11	11	15	15	10
2615	-12.422	64.2	12.436	0	3	1	1		7	7	11	11	11
2597	-13.577	63	12.429	1	3	1	1		15	15	11	11	12
2614	-12.997	63.6	12.427	0	3	1	1		11	11	11	11	13
2690	-12.271	64.3	12.426	3	1	1	1		11	11	15	15	14
2566	-13.552	63	12.42	3	3	1	1		11	11	11	11	15
1589	-13.495	63	12.419	0	3	1	3		15	15	11	11	16
2658	-12.471	64	12.418	1	2	1	1		11	11	15	15	17
2582	-13.361	63.1	12.417	2	3	1	1		11	11	11	11	18
2726	-11.827	64.7	12.416	1	1	1	1		11	11	11	11	19
2646	-12.745	63.8	12.415	2	2	1	1		11	11	11	11	20
1590	-13.021	63.5	12.411	0	3	1	3		11	11	11	11	21
1334	-12.912	63.6	12.411	0	3	2	3		11	11	11	11	22
2678	-12.32	64.2	12.41	0	2	1	1		11	11	11	11	23
2739	-11.188	65.3	12.41	0	1	1	1		7	7	15	15	24
2707	-11.842	64.6	12.408	2	1	1	1		7	7	15	15	25
2598	-13.175	63.3	12.405	1	3	1	1		11	11	11	11	26
2722	-11.765	64.7	12.405	1	1	1	1		11	11	15	15	27
2659	-12.103	64.3	12.401	1	2	1	1		7	7	15	15	28
1578	-13.258	63.1	12.398	1	3	1	3		11	11	7	7	29
2310	-13.435	62.9	12.396	3	3	2	1		11	11	11	11	30
2482	-11.38	65	12.392	0	1	2	1		11	11	15	15	31
2723	-11.521	64.8	12.391	1	1	1	1		7	7	15	15	32
2755	-11.618	64.7	12.39	3	0	1	1		7	7	15	15	33
2599	-12.672	63.7	12.389	1	3	1	1		7	7	11	11	34
2803	-10.505	65.8	12.385	0	0	1	1		7	7	15	15	35
2613	-13.469	62.8	12.385	0	3	1	1		15	15	11	11	36
1641	-12.989	63.3	12.382	1	2	1	3		15	15	7	7	37

Table 5.2 ENOB, SNR. Datasheet configuration

5.1 POWER CONSUMPTION

During the tests, measurements of the consumption of the system were made, the data obtained can be seen in the Table 5.3. Measurements were made on the Filter, Flash and DACs to see how the consumption varied with the variations of the power supplies and currents.

Power consumption									
	Nominal Values @ 160 MHz			Optimized for power @ 160 MHz			Optimized for power @ 120 MHz		
	Voltage [V]	Current [mA]	Power [mW]	Voltage [V]	Current [mA]	Power [mW]	Voltage [V]	Current [mA]	Power [mW]
VDD Filter	1.80	32.2	57.96	1.65	22.5	37.13	1.65	16.7	27.6
VDD Flash	1.80	23.3	41.94	1.80	21.2	38.11	1.80	16.6	29.9
VDD DAC	1.80	4	7.20	1.65	3.2	5.25	1,65	3.9	7
Total	-	59.5	107.1	-	46.9	80.5	-	37.2	64.5

Table 5.3. Power Consumption

The measurement of power consumption in three scenarios.

1. Normal operating conditions (fs=160 MHz, V=1.8 V) and nominal values of the intensities that achieved an ENOB greater than 12. The total consumption was 107 mW, with a consumption intensity of 59.5 mA.
2. Low voltage power conditions 1.65 V, in this case the voltage of the Flash (1.8 V) and the fs = 160 MHz. The consumption drops to 80.5 mW, with an intensity consumed of 46.9 mA which supposes a decrease of 25%.
3. Low voltage power conditions 1.65V, in this case do not touch the voltage of the Flash (1.8 V) and decrease of the IbiasGEN from 100 µA to 85 µA, the fs = 120 MHz is reduced. In this case the low consumption To 37.2 mA which means a decrease of 38%.

The conclusion is that consumption can be improved without performance decrease.

6 MEASUREMENTS

In this chapter the results of the ASIC (ΣΔ ADC modulator) characterization are analyzed. The results obtained from the simulation are compared with the best configurations obtained during the tests in order to decide whether the proposed design is valid or not (**objective 5**). As can be seen in the development of this chapter, the data obtained from the tests, allows to know that the CT ΣΔ ADC can be used to remove the classic filter and an only an anti-alias filter is requiered. The bandpass loop filter atenuatted quantization noise over a narrow bandwidth.

The process followed in order to obtain the test data and its after processing is the following:

1. The test were based on the nominal values of the capacitors and the DAC Ibias. Taking into consideration that every test takes between 18 and 20 seconds it can be performed around 4300 and 4800 test every day. Finally, sweeping test of 4000 test has been performed every day to be able to daily analize them.
    a. Test around the nominal values.
    b. Beginning with the lower values and with steps of 1/2/3 in the capacitors values until reaching the maximun value. The same procedure has been carried out for the Ibias of the DAC.
2. The test performance is completely automatic. Once the Matlab program start it asked to introduce the minimun, maximun and the steps values of the parameters. After running the program, all the graphs has been stored and an Excel with the parameters, the ENOB and SNR of every configuration has been created as it can be seen Table 5.2.
3. From the CADENCE program have been obtained simulated data abaut ASIC schematic. These data were used to do a comparision between the real data and the simulated one. Few simulations were performed because the duration of the simulations were greater than 15 days.

After these test, the ones with ENOB higher of 12 bit were established as the good ones. The maxium ENOB reached is 12.6 bits.

6.1 MEASUREMENTS RESULTS

In the section the measured graphs obtained with the configuration of Table 6.1 are shown. The ENOB achieved were 12.6.

DAC1	DAC2	DAC4	DAC5	C1	C2	C3	C4
1	0	1	1	8	8	14	14

Table 6.1. Programming bits

On this same configuration the tests will be repeated with the signal input voltages shown in the Table 6.2 these are referred to full scale (1.6 V).

V1(dBFS)	V2(dBFS)	V3(dBFS)	Tone (MHz)
-41	-11	-3	5

Table 6.2. Input signal parameters

6.2 FFT CALCULATION

In this section it is going to be explained a comparison between one of the graphs obtained from the measurements with an equivalent simulation performed with the CADENCE program.

As stated in Chapter 5 the calculation of the FFT has been performed with a function that is copyrighted this is why it cannot be shown in this Bachelor Thesis, with the result provided by the function the following figures are obtained.

In Figure 6.1 the FFT is displayed when there is no signal at the input, and it is observed that it has the expected shape in a modulator ΣΔ ADC of 4^{th} order (the slope is approximate 80 dB). Over the graph, it is possible to see in pink the points in the [4,5] MHz interval, which correspond to a 1MHz of bandwith.

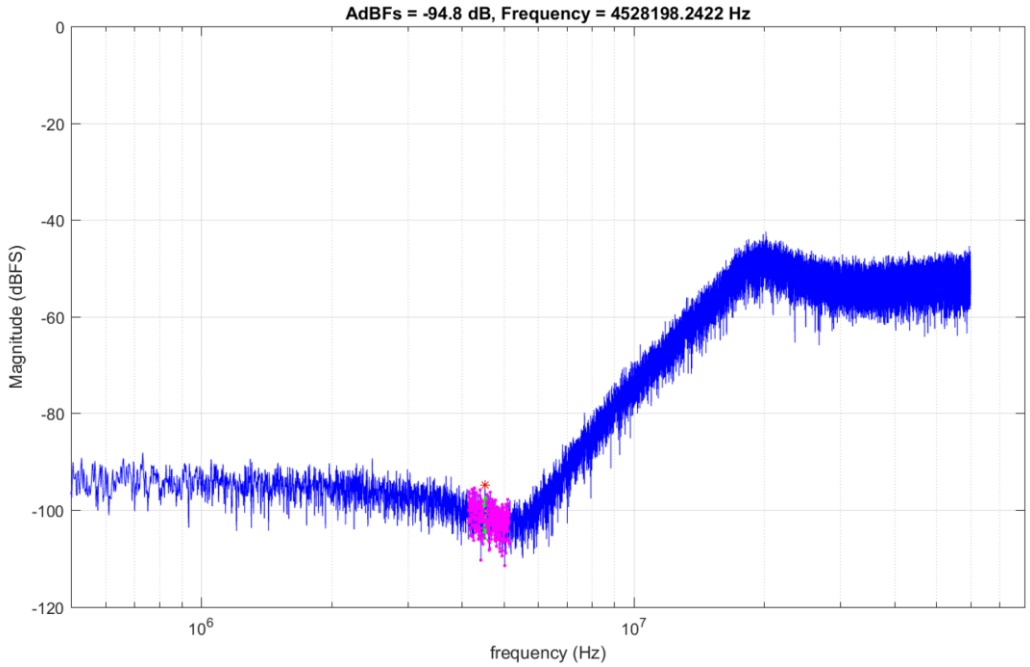

Figure 6.1 **Measured** FFT **Idle channel**

The following three figures represent the frequency response of the three test points in Table 6.2. In each graph is indicate the main values used to calculate the FFT.

In Figure 6.2 a 5 MHz tone was introduced with a full scale amplitude of -41 dBFS.

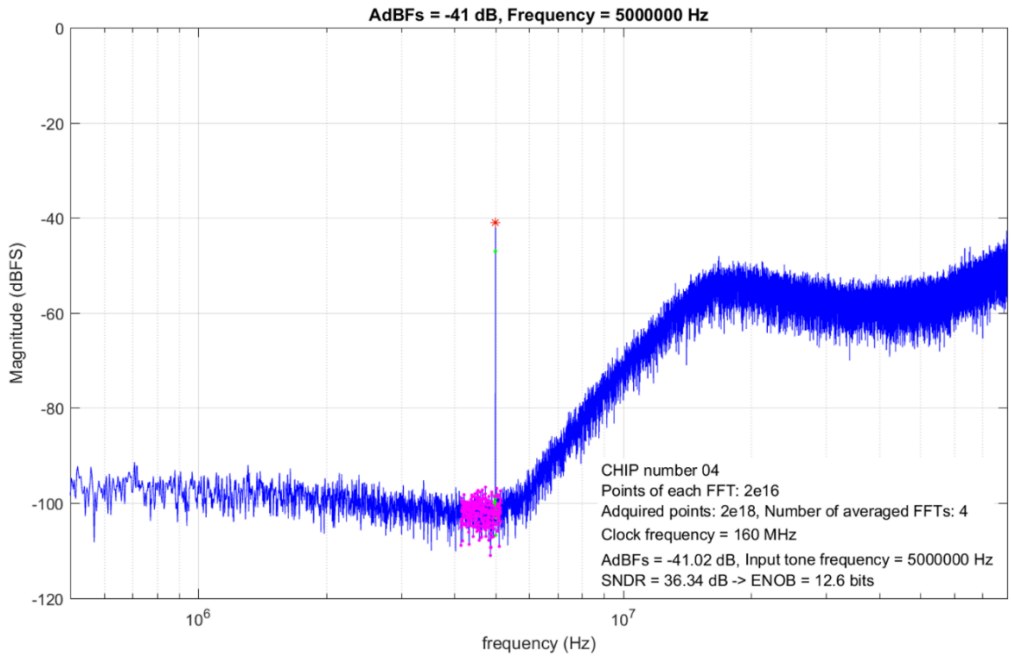

Figure 6.2 **Measured**. FFT 5MHz, -41 dBFS signal

As it can be seen in the graph of Figure 6.2, the pitch passes the filter without attenuation, a 12.6-bit ENOB with SNDR of 36.34 dB is achieved. The system is a

central frequency bandpass of 4.5 MHz with a bandwidth of 1 MHz, being this the expected result. A very high effective resolution is achieved. As can be observed in the graphs in Figure 6.2 and Figure 6.3, no unwanted frequencies appear.

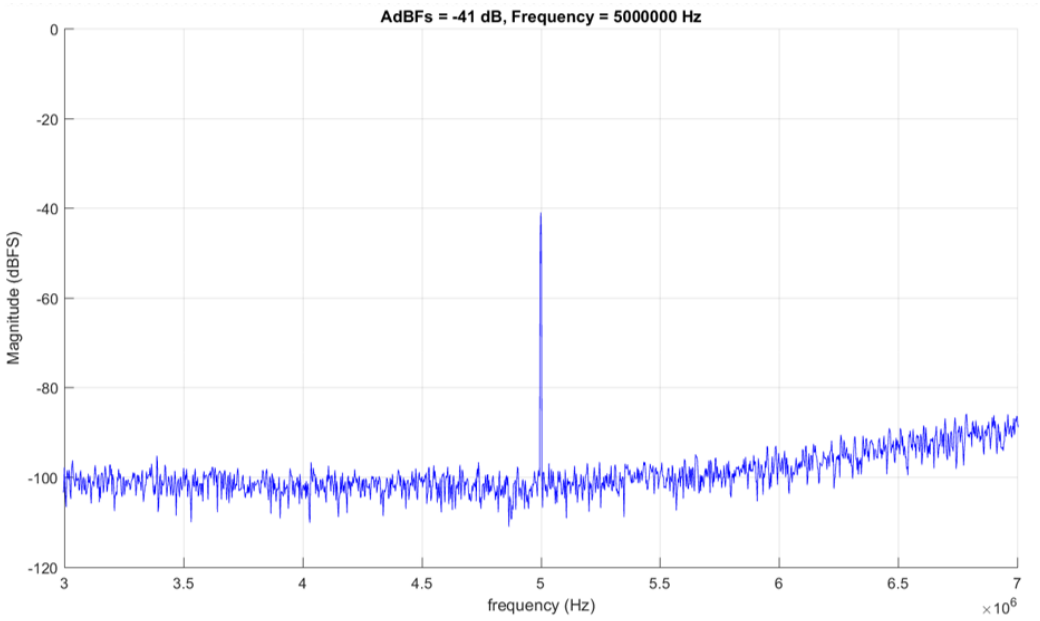

Figure 6.3 **Measured.** FFT 5MHz, -41 dBFS signal extension

In Figure 6.4 the same tone is introduced but changing the amplitude to -11 dBFS, the unwanted tones that appear are marked with red circles.

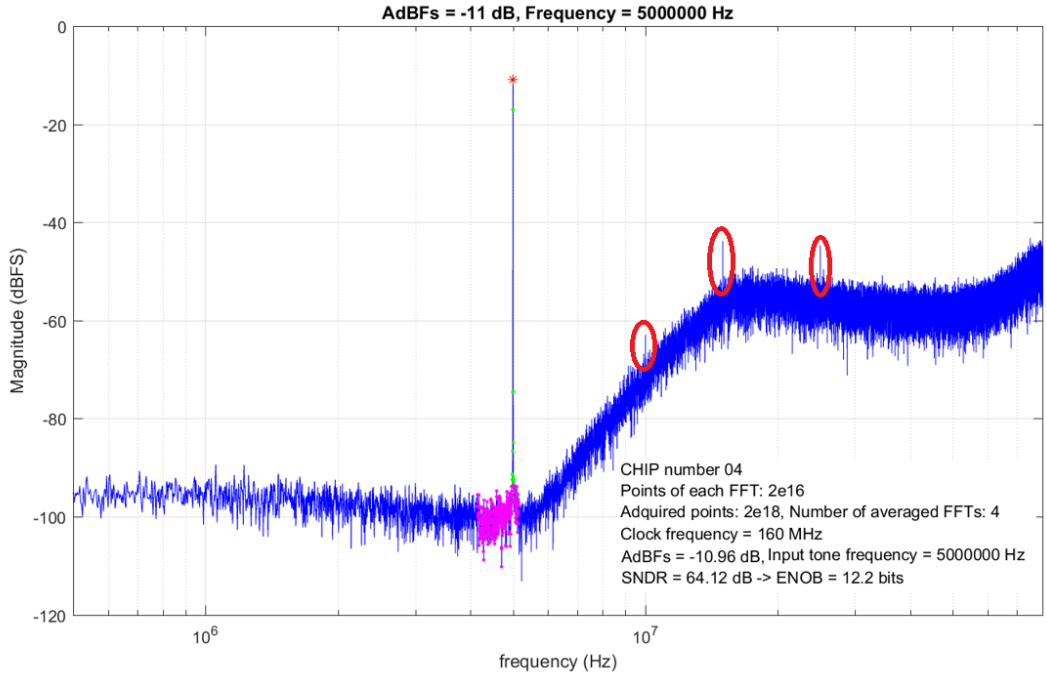

Figure 6.4 **Measured**. FFT 5MHz, -11 dBFS signal

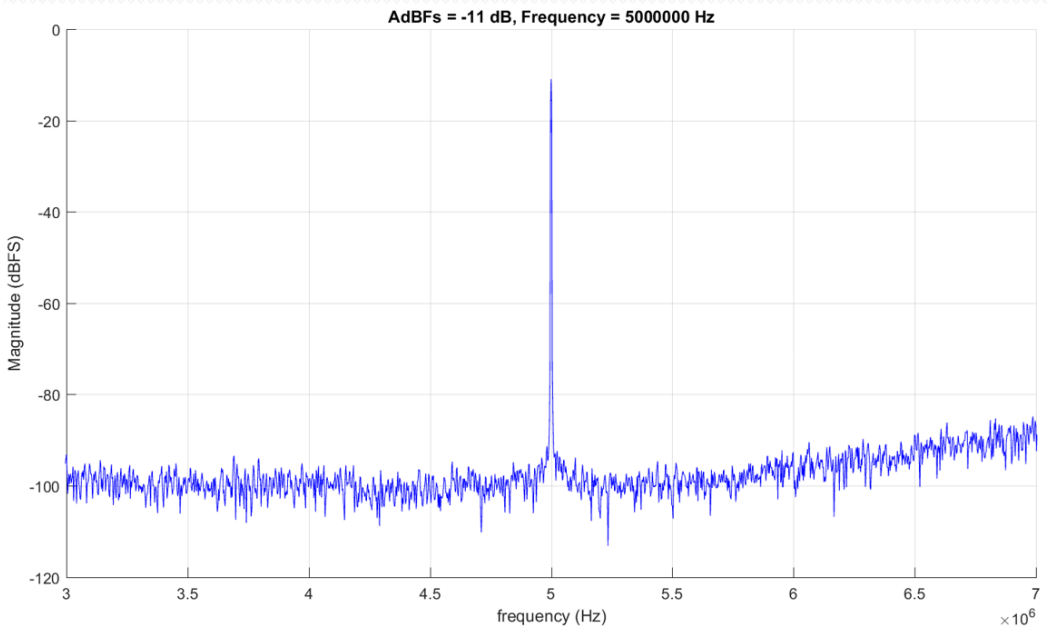

Figure 6.5 **Measured.** FFT 5MHz, -11 dBFS signal extension

As it can be seen in Figure 6.5 in which an amplification of the signal is shown, these distortions do not affect the bandwidth of interest, this being an optimal result for the input tone of 5MHz. Therefore, this significant amplitude increase does not cause a decrease in the effectiveness of Band-pass in terms of signal filtering.

Finally, the introduction of the same frequency tone but now at amplitude of -3dB is tested to analyze the frequency response.

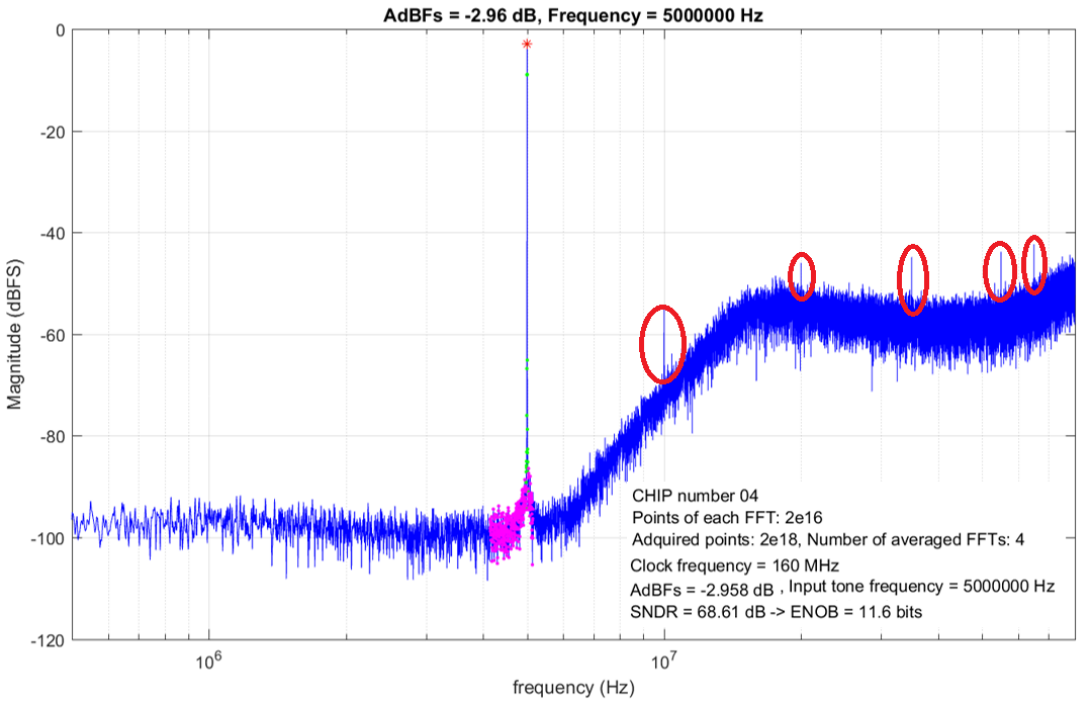

Figure 6.6 **Measured.** FFT 5MHz, -3 dBFS signal

As in the frequency response to the -11 dBFS signal, it is possible to detect unwanted tones, marked with red circles. In this amplitude of -3 dBFS more tones appear and with greater amplitude than in the previous tests. This is represented in Figure 6.6.

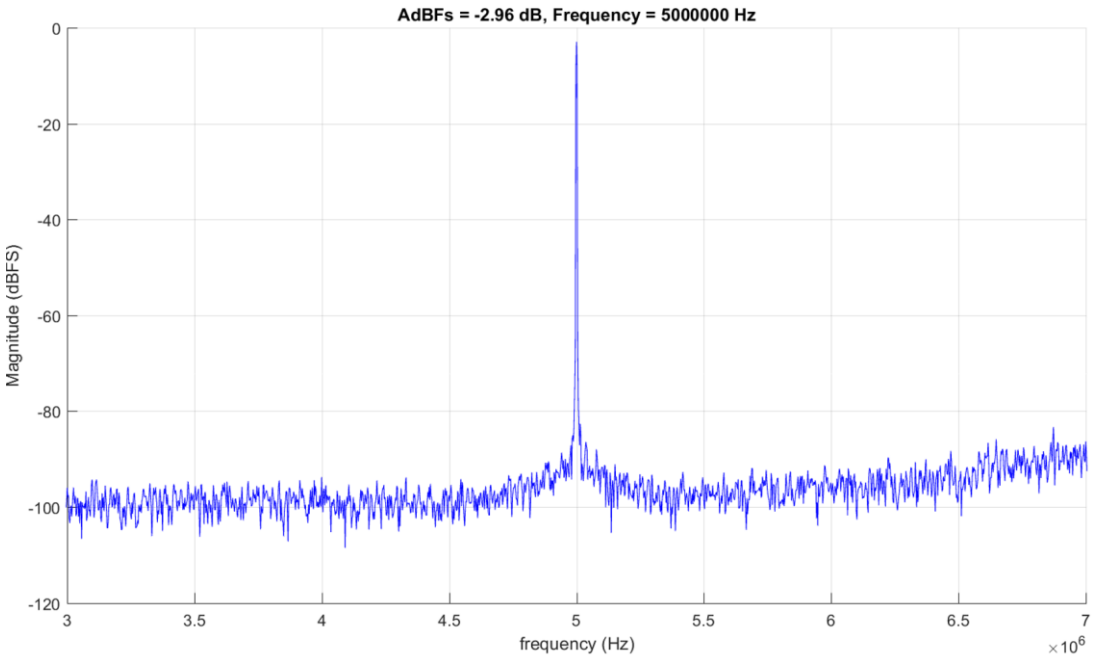

Figure 6.7 **Measured**. FFT 5MHz, -3 dBFS signal extension

In spite of the appearance of a greater number of unwanted tones, as can be seen in Figure 6.7, these are also not in the bandwidth of interest.

Therefore, it can be concluded that an increase in the amplitude of the input signal introduces small distortions in the frequency analysis. However, as can be verified the ENOB remains quite stable going from 12.6 to 11.6 which means a variation of 8%, being able to assert that the ASIC works correctly.

The next step is to obtain the dynamic range of this signal and compare it with another signal of 5 MHz, but sampled at 120 MHz and feed at 1.65 V instead of the nominal 1.8V to obtain an optimized signal for the power consumed. The result of this comparison is shown in Figure 6.8. As can be seen there is no distortion throughout the dynamic range which implies that there are no interfering noises in the signal which indicates that the design and manufacture of the ASIC is correct.

As can be seen in Figure 6.8 the dynamic range in both tests is 82 dB. The expected dynamic range was 90 dB, being in margins of the expected result.

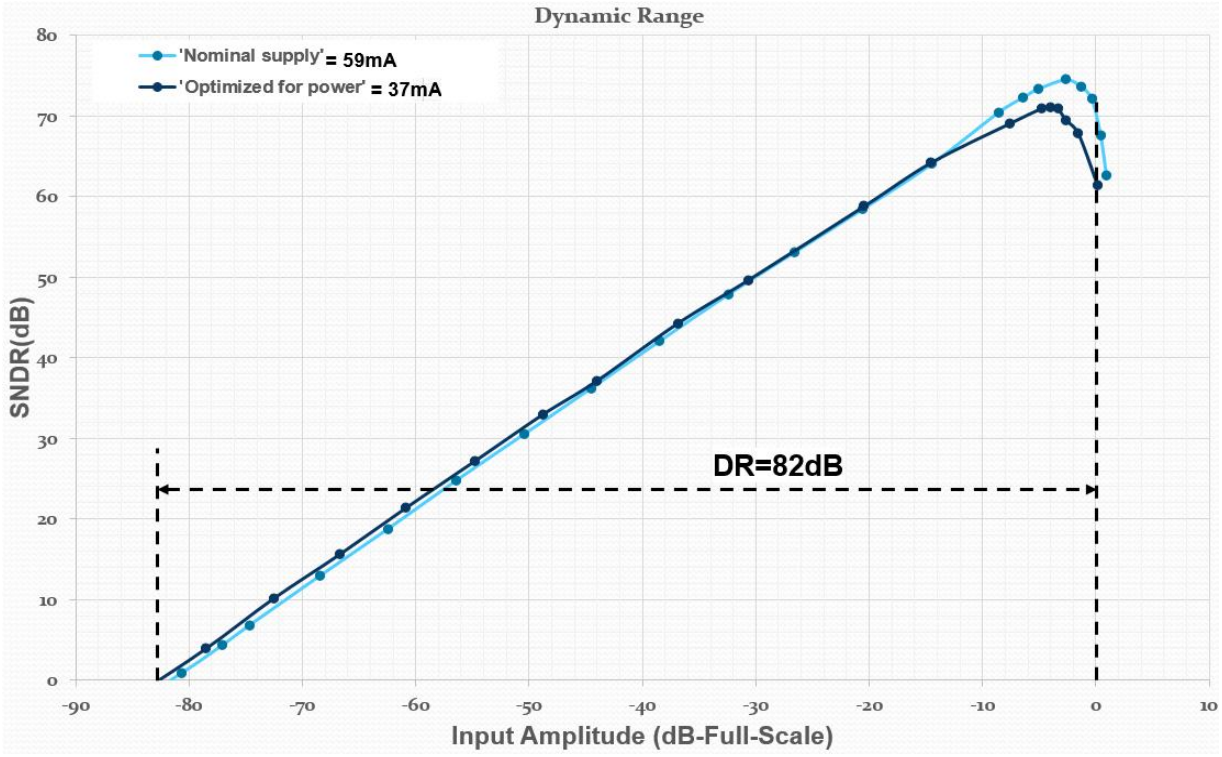

Figure 6.8 Dynamic Range

6.2.1 INTERMODULATION

The intermodulation product is one of the parameters to characterize the dynamic performance of an ADC converter. Although, it is widely used in radiofrequency devices. In its application to the converters, the IMD is calculated by applying two sinusoidal signals of two different near frequencies (f1 and f2) of the same amplitude, which must be large. In doing so, different distortion tones occur due to the interaction of the input signals in the modulator. These tones appear at certain frequencies as shown in Figure 6.9.

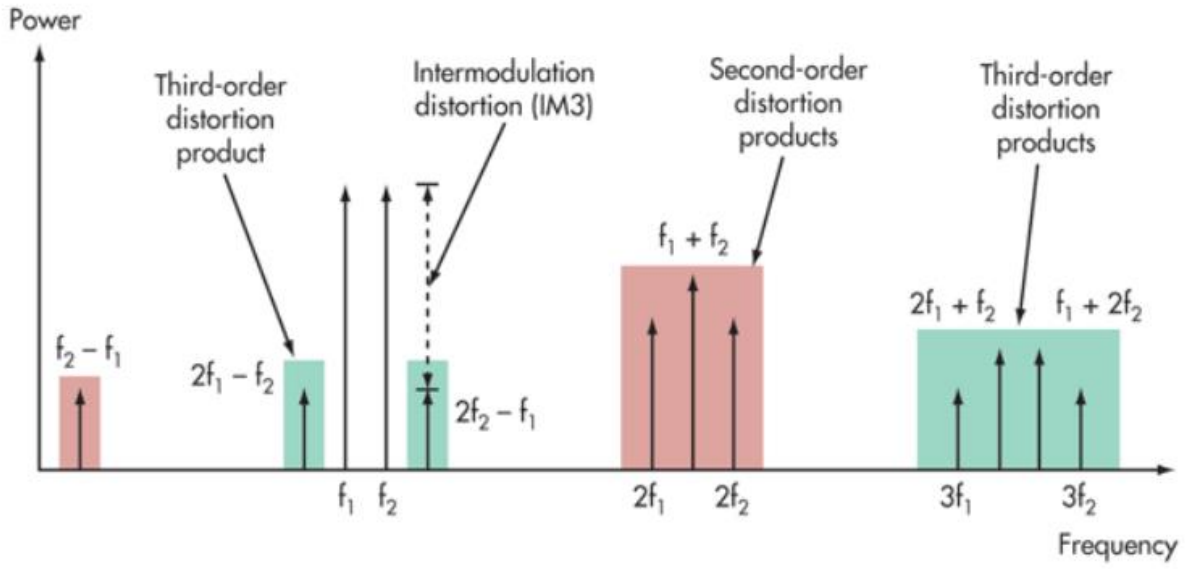

Figure 6.9 Intermodulation distortion [22]

The analysis of the intermodulation product allows to get an idea of how the system responds to multitoned signals, that is to say, complex or modulated signals, which are more realistic than a single sinusoidal signal of a single tone. That the value of the IMD is high which implies a good response.

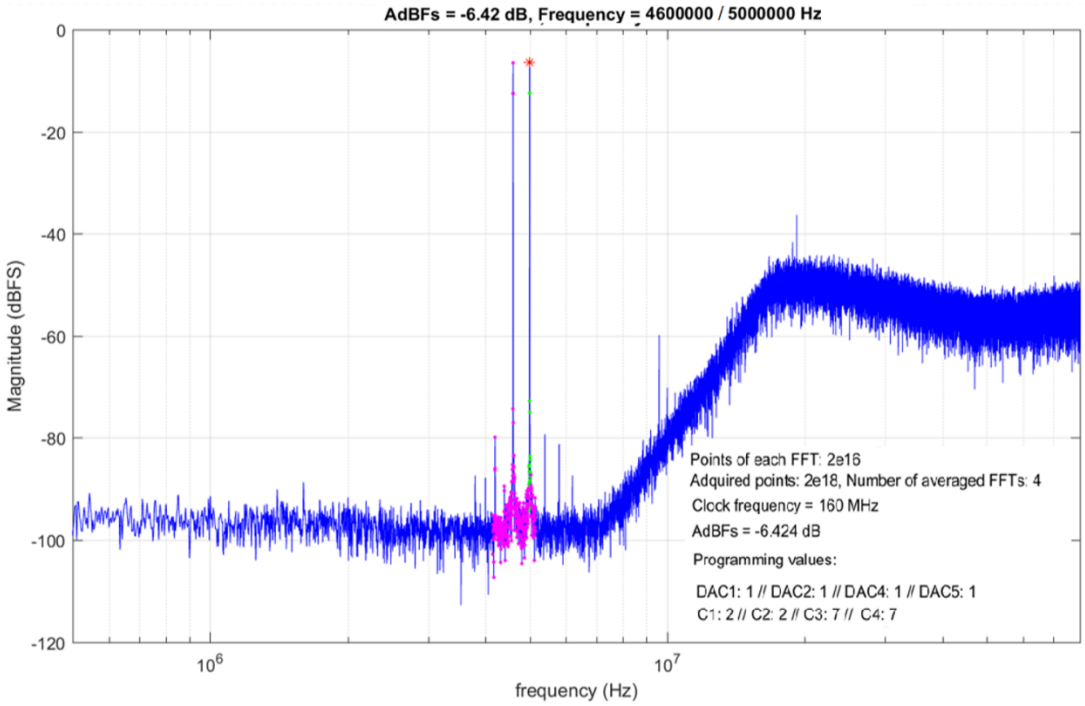

Figure 6.10 Intermodulation Test

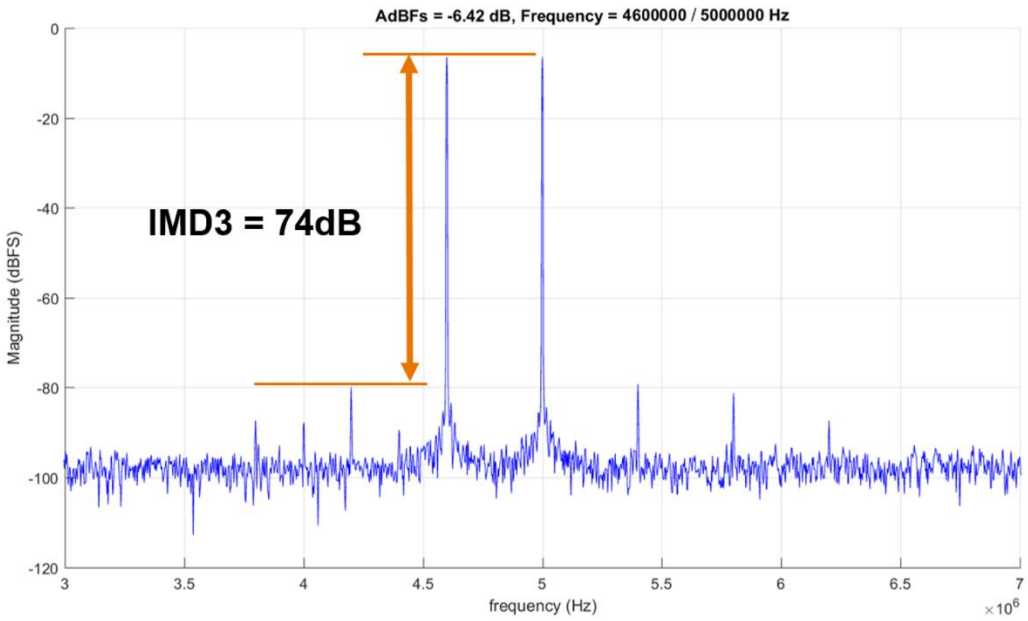

Figure 6.11 Intermodulation Test extension

It is observed that it has an IMD3 of 74 dB which is sufficient for the application of MRI.

6.3 CADENCE SIMULATION

There are simulations performed with the program "CADENCE". CADENCE simulations are in Figure 6.12. and Figure 6.13. When processing a signal of -3 dBFS and a frequency of 4.76 MHz the expected shape is obtained and the slope is approximately 80 dB per decade. The -3dB tone appear without attenuation as expected.

In terms of comparison between the simulated graphs and the measured graph at -3 dB of amplitude (Figure 6.6). It is possible to detect slight differences, the most important is the form of the noise-shaping at frequencies below the IF (4.5 MHz). In the graph obtained with the real measurements, this zone is much flatter than in the simulated one due to the thermal noise and the distortion. There are no unwanted tones in the simulated graph as in the real one, otherwise they are very similar, as expected.

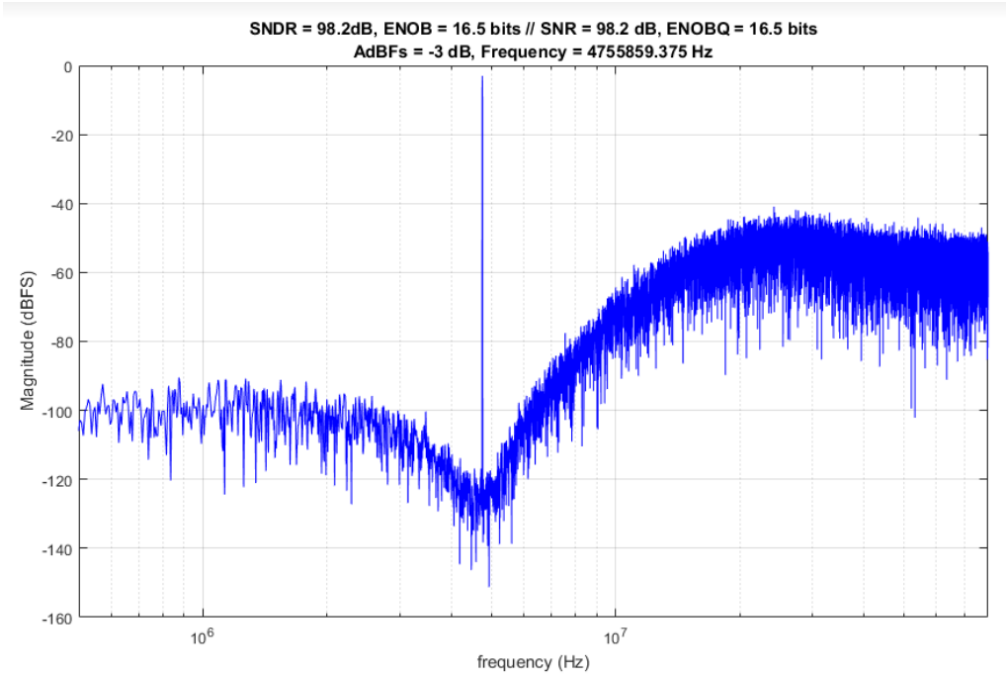

Figure 6.12 **Simulated**. FFT 4.76 MHz, -3 dBFS signal

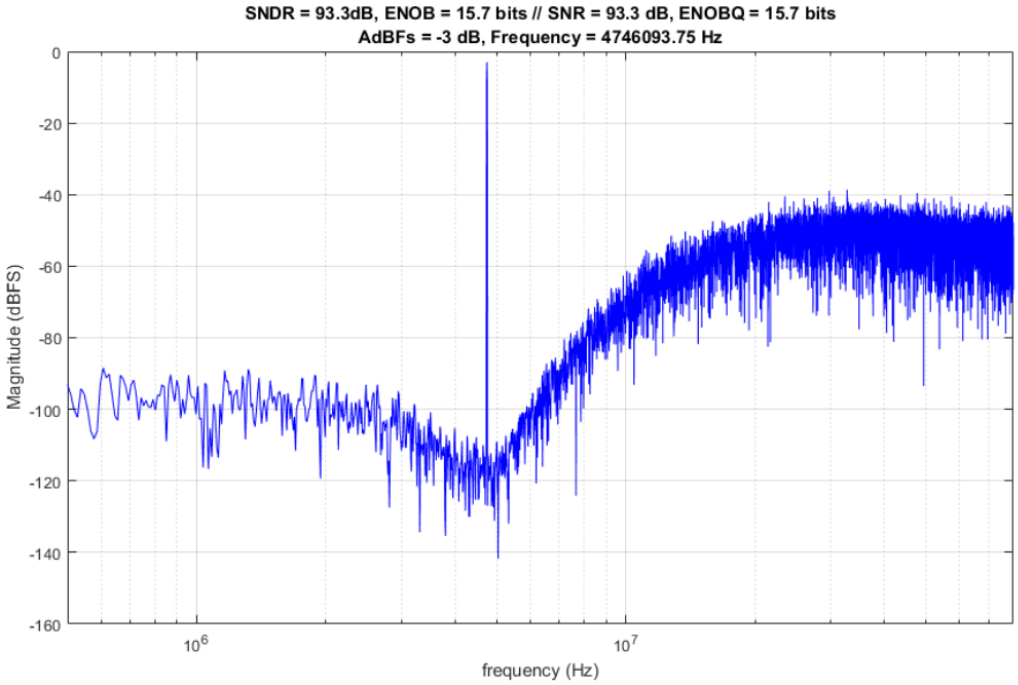

Figure 6.13 **Simulated**. FFT 4.76 MHz, -3 dBFS signal

6.4 MEASUREMENTS CONCLUSIONS

The measurements **show 82 dB dynamic range** (Figure 6.8) over a 1 MHz bandwidth with a limit tone of 5MHz in order to test the ADC in the limit of the bandwith , which **is good enough for this application**. The measured **IMD3 is 74 dB** (Figure 6.11).

The design is correct and meets the expectations. Therefore it can be said that the ASIC is valid being fulfilled the **objective 5**. The ASIC is completely characterized thereby fulfilling **objective 1**. **All the objectives fulfilled.**

7 SOCIOECONOMICAL ENVIRONMENT

7.1 FINANCIAL BUDGET

This section calculates the cost of the project, including material costs and engineering costs.

7.1.1 COST OF MATERIAL

Component	Description	Amount	Price(€/unit)	Total price
ASIC				
ASIC	ASIC	1	10000	10000.00
			SUBTOTAL	**10000.00**
PCB				
PCB	PRINTED CIRCUIT BOARD	3	124.3533	373.06
			SUBTOTAL	**373.06**
PCB COMPONENTS				
100nF	CAPACITOR	40	0.0257	1.03
0.1uF	TANTALO CAPACITOR	20	0.304	6.08
1uF	TANTALO CAPACITOR	20	0.227	4.54
100nF	CAPACITOR	50	0.0145	0.73
1uF	CAPACITOR	50	0.0257	1.29
1pF	CAPACITOR	50	0.0149	0.75
NC7SZ04M5X	SINGLE INVERTER	15	0.264	3.96
CQFJ48	CHIP SOCKET	5	0.4652	2.33
RED	BANANA CONECTOR	3	3.55	10.65
BLACK	BANANA CONECTOR	3	3.54	10.62
Pin strip	PIN STRIP	10	0.43	4.30
Vin_diff	SMA	6	5.35	32.10
ADN4668ARZ	LVDS RECEIVER	4	2.3	9.20
ACPL-W70L-000E	OPTOCOUPLER	5	3.54	17.70
Potenciometer 10K	POTENCIOMETER	5	1.57	7.85
Potenciometer 5K	POTENCIOMETER	5	1.6	8.00
Potenciometer 2K	POTENCIOMETER	5	1.87	9.35
5-1437565-0	RESET BUTTON	5	0.355	1.78
TRAFO Vin	Trafo RF	3	6.2	18.60
LF351D	OPAMP	8	0.764	6.11
LM334DT	SOURCE CURRENT	10	0.902	9.02
LTC3026	VLDO LINEAR REGULATOR	8	4.32	34.56
TPS79501DCQ	VLDO LINEAR REGULATOR	6	3.22	19.32
D01468 PCB Spacer Support	PCB SPACER SUPPORT	20	0.143	2.86
			SUBTOTAL:	**222.71**
			TOTAL MATERIALS	**10595.77**

Table 7.1 Cost of project materials

The materials have also included the cost of ASIC as it is the object of this Project.

The cost of material includes 21% IVA.

7.1.2 ENGINEERING COST

The engineering cost has been calculated on the basis that the average cost of an Engineer's hour taking into account all the concepts (salary, Social Security, etc.) is estimated to be **60 €/hour**. In the project a single engineer is computed, the duration of the project being 28 weeks, with a work from Monday to Friday for 8 hours a day. The project involves:

- Instrumentation design.
- PCB design.
- Assembly and testing of the PCB.
- ASIC complete system testing.
- Analysis and validation of results.
- Memory writing.

Task	Weeks	Days	Hour	€/ hour	Total €
Personnel : one engineer	28	140	1120	60	67200
				TOTAL	67200

Table 7.2 Cost of personnel

7.1.3 FINAL BUDGET

Summing up the concepts of cost of materials and engineering cost, the total cost of the project is in Table 7.3.

Type of cost	Cost
Cost of material	10595.77
Personnel cost	67200
TOTAL	77795.77

Table 7.3 Total Cost of the project

7.2 SOCIOECONOMICAL IMPACT

The socioeconomic impact of this project has to be evaluated taking into account several aspects.

In order to carry out the ASIC characterization, it has been necessary to develop a test environment. Specific instrumentation has been designed and a flexible Sw control loop has been developed to manage the test environment, which minimizes the time it takes to perform these. All this Hw-Sw knowledge has generated expertise in the group as for measurement techniques which is applicable to future ASICs. This will enable the capture of new projects which will mean more investment for the Research group. In particular all the work carriet out during the tests of this first prototype of the ASIC is reusable one hundred percent for the following versions, this will save time and money for the following characterizations.

The knowledge acquired during this project will be reused for the benefit of the realization of new types of measuresments, it may even involve the development of new specific instrumentation equipment. The development of new environments will be faster and the duration of the tests will be shorter. The laboratory in this way will gain in efficiency which will allow to carry out more projects. This improvement in the quality of the execution of tests may lead to the recruitment of new personnel.

Given that the project is in I+D category, as it is insiede an Europen interdisciplinary group,the knowledge acquired during the project can be transferred to companies in the microelectronics field. Thus resulting in a transfer of technology which translates into a benefit for the University, both economically and prestige.

These new ASICs, as indicated in the introduction, will lead to an improvement in current MRI receivers by eliminating coaxial cables and obtaining smaller and better resolution receivers. All this will have an impact on improving the quality of the image so the detection of diseases will be more accurate. There will be savings in production costs when building the MRI and also savings in treatment costs.

This progress made in the field of Biomedical Engineering will have a great social impact, as well as an economic impact since the improvement of the biomedical instrumentation helps the quality of life of people by improving the techniques of detection of diseases. But it is not only a social question as a saving in the costs of the MRI will restult in cheaper and more affordable MRIs for governments.

8 CONCLUSIONS

As a conclusion of this project we can consider both personal and technical conclusions.

For me this project represents a remarkable advance in its area of research, since it is something new and of great utility of which still can be much more useful in the implementation of new uses and variants adapted to the different situations in which it is required a system of these characteristics.

The accomplishment of this work has been a challenge, since it has been necessary to deepen the knowledge of the electronic branch acquired during the degree of Biomedical Engineering.

In the technical aspect, the results obtained have been as expected, however, it is still possible to improve the prototype tested. The five objectives of the project will be cited indicating in each of them the achieved scope.

Recalling the five basic objectives of this Bachelor Thesis:

- Objective 1: Characterize the ASIC.
- Objective 2: Develop the instrumentation need to measure the ASIC (PCB).
- Objective 3: Develop a close control loop of the ASIC.
- Objective 4: Develop a software post-process the data of the ASIC.
- Objective 5: Result analysis.

The main objective (objective 1) can only be met if the following four objectives have been satisfactorily fulfilled.

Objective 2 is clearly verifiable, the PCB has been developed with all its instrumentation and the most obvious proof is that the ASIC has been placed on it and satisfactory tests have been carried out.

Thanks to the automatization achieved in the generation of test patterns and the interconnection achieved between the Signal Analyzer, the Arduino system and the Matlab Sw, has allowed a high number of real-time tests that have managed to find the most optimal configurations. Therefore, **Objective 3** has also been met.

A Sw in Matlab has been developed, based on a copyrighted function that calculates the FFT. This Sw (which complements the Sw of the control loop) reads the file generated by the Signal Analyzer, and generates the FFT, calculates the merit figures as well as the graphs. It is therefore clear that **Objective 4** has also been met.

Objective 5 consist of performing the analysis of the results obtained. In order to decide if the ASIC chip worked according to specifications, there were simulations (carried out with the Cadence program) on the ASIC schematic. In these comparisons it was seen that the results were good enough, 82 dB DR over 1 MHz bandwidth, with a limit tone of 5 MHz. The measured IMD3 is 74 dB, which is good enough for its use in the receiver for MRI. **Objective 5** was met, there were measures and with them was possible to validate the design of the ASIC.

Objective 1 which was the characterization of the ASIC has been satisfactorily fulfilled.

The experience gained in these tests will be used both to improve the ASIC and test methods. Surely the next versions will get better merit figures than the current ones, even though they are good and totally valid for the defined project.

8.1 FUTURE WORK

With the accumulated experience, it has been seen that it is very interesting to be able to control and visualize in the Matlab program the actual values of the external feeds of the PCB (Automating the guarantee that at all times the sistems is fed with the desired voltage) as well as the values that are provided by the different sources of voltage, the sources of currents and the actual values of the different reference voltages.

These changes involve the design of sensors that measure voltages and currents and new circuits of adjustable voltage and current sources that can be configured externally (through Matlab). It is also necessary to develop a new PCB as well as a new Sw that incorporated these new functionalities.

The management of these data would lead to an improvement in the testing time , as the configuration time of these parameters in the PCB would be very fast and safe. It would also imply an improvement in the quality of the tests because it would

guarantee at all times that all the external parameters of the ASIC are with the desired values which would bring an extra reliability to the results of the same ones.

In addition to sporadic mistakes, its analysis would be easier because it would not be necessary to analyze if the failures are due to faults in the sources of voltage and currents.

ANNEX I PROGRAMMING BITS

The chip has a total of 34 bits that allow to vary the values of the capacitors of the filters, the values of the Ibias of the IDACs and the control of the transmission LVDS, as well as to perform the Reset of the ASIC, in the following table shows a Summary, to see the configuration tables of the capacitors of the integrators, see Annex 2.

These bits are controlled externally by the shift register that the ASIC has.

Programming bits (REGISTERED)				See Anex 2 and Anex 3
Signal type and name	**Alias**	**Value**	**Unit**	**Comments**
LVDS TX pad	IDSET_LVDS_TX<1>	1	bit	LVDS pad output current
AUX Buffer (Probe) multiplexer	AUXBUF<4:0>	5	bits	No probe output if all are '0'. Activate only one at a time to output the Vx (1-5) state signal.
IDAC5 programming . 3 bits	DAC5_prog<2:0>	3	bit	Trim of +/- 20% over nominal current value. 8 steps (3 bits)
IDAC4,2,1 programming. 2 bits each	DACx_prog<1:0>	6	bit	Trim of +/- 20% over nominal current value. 4 steps (2 bits). DAC3 is not programmable
DWA Transparent mode (no rotation)	DWA_TM	1	bit	
Programmable clock delay	delay_prog<1:0>	2	bits	
Capacitors programming - 4 bits for each 4 caps (C4:C1)	Cx_prog<3:0>	16	bits	Trim of +/- 30% over nominal value of each capacitor. 16 steps/cap (4 bits/cap)
TOTAL:		34	bits	

Table 1 Annex 1. Programming bits

The different configuration bits will then be described, following the order of the Table 1.

1. **LVDSTXpad**: **a bit (IDSET_LVDS_TX)**, Indicates whether or not there is LVDS data transmission.
    a. **IDSET_LVDS_TX** =1 → There is data transmission
    b. **IDSET_LVDS_TX**= 0 →There is not data transmission.

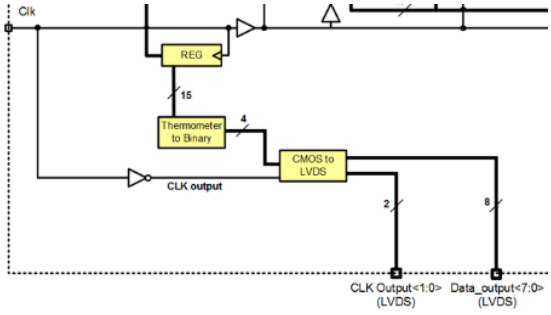

Figure 1 Annex 1. LVDS coding

The circuit that handles this bit is shown in Figure 1.

2. **AUX Buffer (Probe) multiplexer**: **five bits** (**AUXBUF<4:0>**). The ASIC has a Vprobe input that is only used if there is a malfunction of the chip, with the multiplexer of the Figure 2 it is possible to redirect the test input to any of the four integrators from which the ΣΔ ADC cascade is composed, and check if the cascade is working properly.

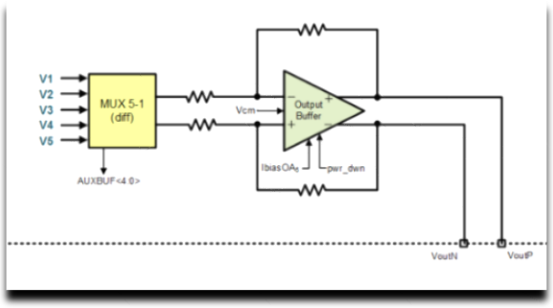

Figure 2 Annex 1 . Vprobe multiplexer

3. **IDAC5 programming**: **three bits (DAC5_prog<2:0>)**, The circuit that handles them is shown in Figure 3. It modifies the value of the nominal current by +-20%. There are 8 different values.

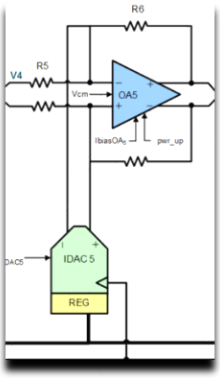

Figure 3 Annex 1 . IDAC5

4. **IDAC4,2,1 programming**: **two bits each** (**DACx_prog<1:0>**), The circuit that controls are shown in Figure 3. The DAC3 is not programmable. Modifies the value of the rated current by +20%, there are four different values, see Annex 3.

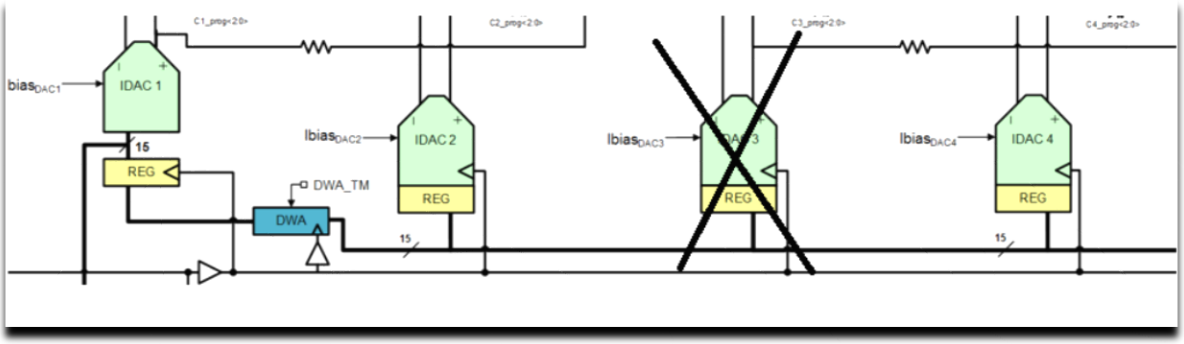

Figure 4 Annex 1. IDAC1/4

5. **DWA Transparent mode (no rotation): one bit (DWA_TM).** Enables or disables the DWA function.

6. **Programmable clock delay: two bits (clock_delay<0:1>).** Controls the Flash delay.

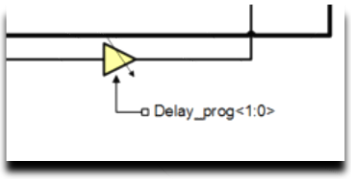

Figure 5 Annex 1 . Delay_prog Flash

7. **Capacitors programming - 4 bits for each 4 caps (C1:C4).** It modifies the values of the capacitors C1: C4 of the integrators in a + -30% with 16 levels of variation, See Annex 2.

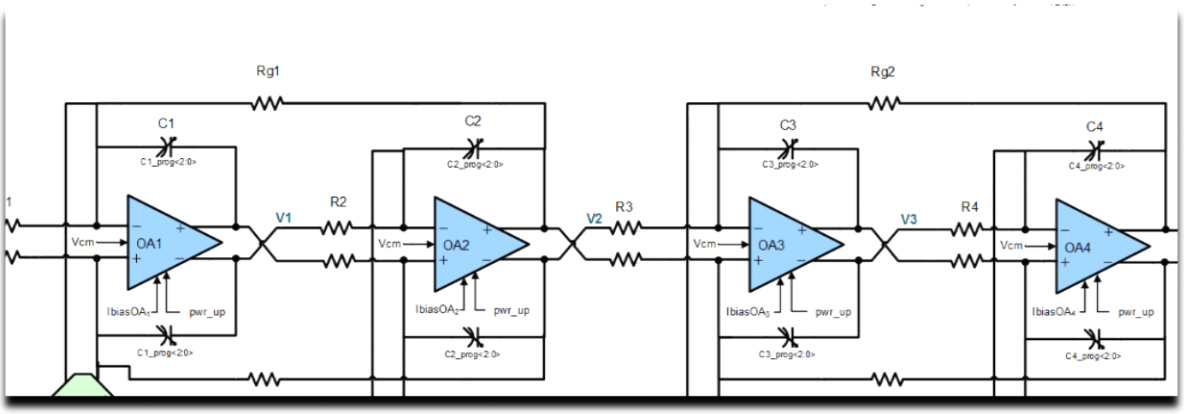

Figure 6 Annex 1 . Programming the C1:C4 of the integrators

The circuit that handles all these bits internally can be seen in the circuit of Figure 7.

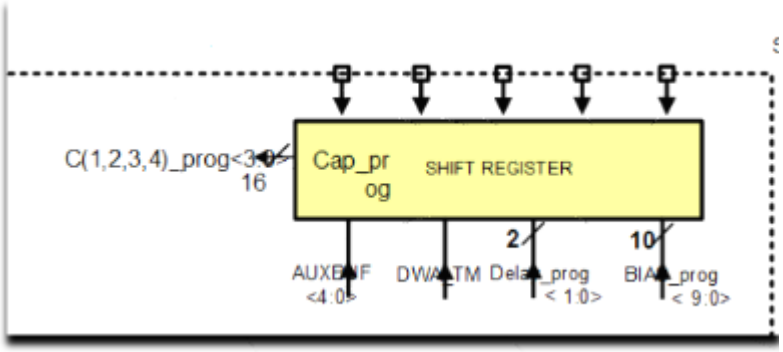

Figure 7 Annex 1. SHIFT REGISTER

There are also two bits to reset the board to factory settings.

Control Bits (dedicated PIN)				Comments
Signal type and name	Alias	Value	Unit	
Digital Reset (PIN)	Digital_Reset	1	bit	Allows reset of digital blocks.
Set Nominal (PIN)	SET_Nom	1	bit	Set all programable bits to its nominal value.

Table 2 Annex 1. Control bits, dedicated Pin

ANNEX II VALUES OF THE C1-C4 CAPACITORS OF THE OA1: OA4

The capacitance values in picofarads acquired by the capacitor C1 are shown in Table 1 depending on the values of the four bits controlling its capacity. Factory setting is 40pF

ADDED VALUE				Step	Possible values (pF)	% nominal value	Comment
C<3>	C<2>	C<1>	C<0>				
0	0	0	0	0	28	0.7	min
0	0	0	1	1	29.5		
0	0	1	0	2	31		
0	0	1	1	3	32.5		
0	1	0	0	4	34		
0	1	0	1	5	35.5		
0	1	1	0	6	37		
0	1	1	1	7	38.5		
1	0	0	0	8	40	1	Nominal
1	0	0	1	9	41.5		
1	0	1	0	10	43		
1	0	1	1	11	44.5		
1	1	0	0	12	46		
1	1	0	1	13	47.5		
1	1	1	0	14	49		
1	1	1	1	15	50.5	1.2625	max

Table 1 Annex 2. C1 possible values

The capacitance values in picofarads acquired by the capacitor C2 are shown Table 2 depending on the values of the four bits that control its capacity. Factory setting is 30pF.

ADDED VALUE				Step	Possible values (pF)	% nominal value	Comment
C<3>	C<2>	C<1>	C<0>				
0	0	0	0	0	20	0.66666667	min
0	0	0	1	1	21.25		
0	0	1	0	2	22.5		
0	0	1	1	3	23.75		
0	1	0	0	4	25		
0	1	0	1	5	26.25		
0	1	1	0	6	27.5		
0	1	1	1	7	28.75		
1	0	0	0	8	30	1	Nominal
1	0	0	1	9	31.25		
1	0	1	0	10	32.5		
1	0	1	1	11	33.75		
1	1	0	0	12	35		
1	1	0	1	13	36.25		
1	1	1	0	14	37.5		
1	1	1	1	15	38.75	1.29166667	max

Table 2 Annex 2. C2 possible values

The capacitance values in picofarads acquired by the capacitor C3 are shown Table 3 depending on the values of the four bits that control its capacity. Factory setting is 2.7 pF.

ADDED VALUE				Step	Possible values (pF)	% nominal value	Comment
C<3>	C<2>	C<1>	C<0>				
0	0	0	0	0	1.9	0.7037037	min
0	0	0	1	1	2		
0	0	1	0	2	2.1		
0	0	1	1	3	2.2		
0	1	0	0	4	2.3		
0	1	0	1	5	2.4		
0	1	1	0	6	2.5		
0	1	1	1	7	2.6		
1	0	0	0	8	2.7	1	Nominal
1	0	0	1	9	2.8		
1	0	1	0	10	2.9		
1	0	1	1	11	3		
1	1	0	0	12	3.1		
1	1	0	1	13	3.2		
1	1	1	0	14	3.3		
1	1	1	1	15	3.4	1.25925926	max

Table 3 Annex 2. C3 possible values

The capacitance values in picofarads acquired by the capacitor C4 are shown Table 4 depending on the values of the four bits that control its capacity. Factory setting is 2.3 pF.

ADDED VALUE				Step	Possible values (pF)	% nominal value	Comment
C<3>	C<2>	C<1>	C<0>				
0	0	0	0	0	1.5	0.65217391	min
0	0	0	1	1	1.6		
0	0	1	0	2	1.7		
0	0	1	1	3	1.8		
0	1	0	0	4	1.9		
0	1	0	1	5	2		
0	1	1	0	6	2.1		
0	1	1	1	7	2.2		
1	0	0	0	8	2.3	1	Nominal
1	0	0	1	9	2.4		
1	0	1	0	10	2.5		
1	0	1	1	11	2.6		
1	1	0	0	12	2.7		
1	1	0	1	13	2.8		
1	1	1	0	14	2.9		
1	1	1	1	15	3	1.30434783	max

Table 4 Annex 2. C4 possible values

ANNEX III PCB LAYOUT

This annex shows two templates generated by Altium for PCB printing.

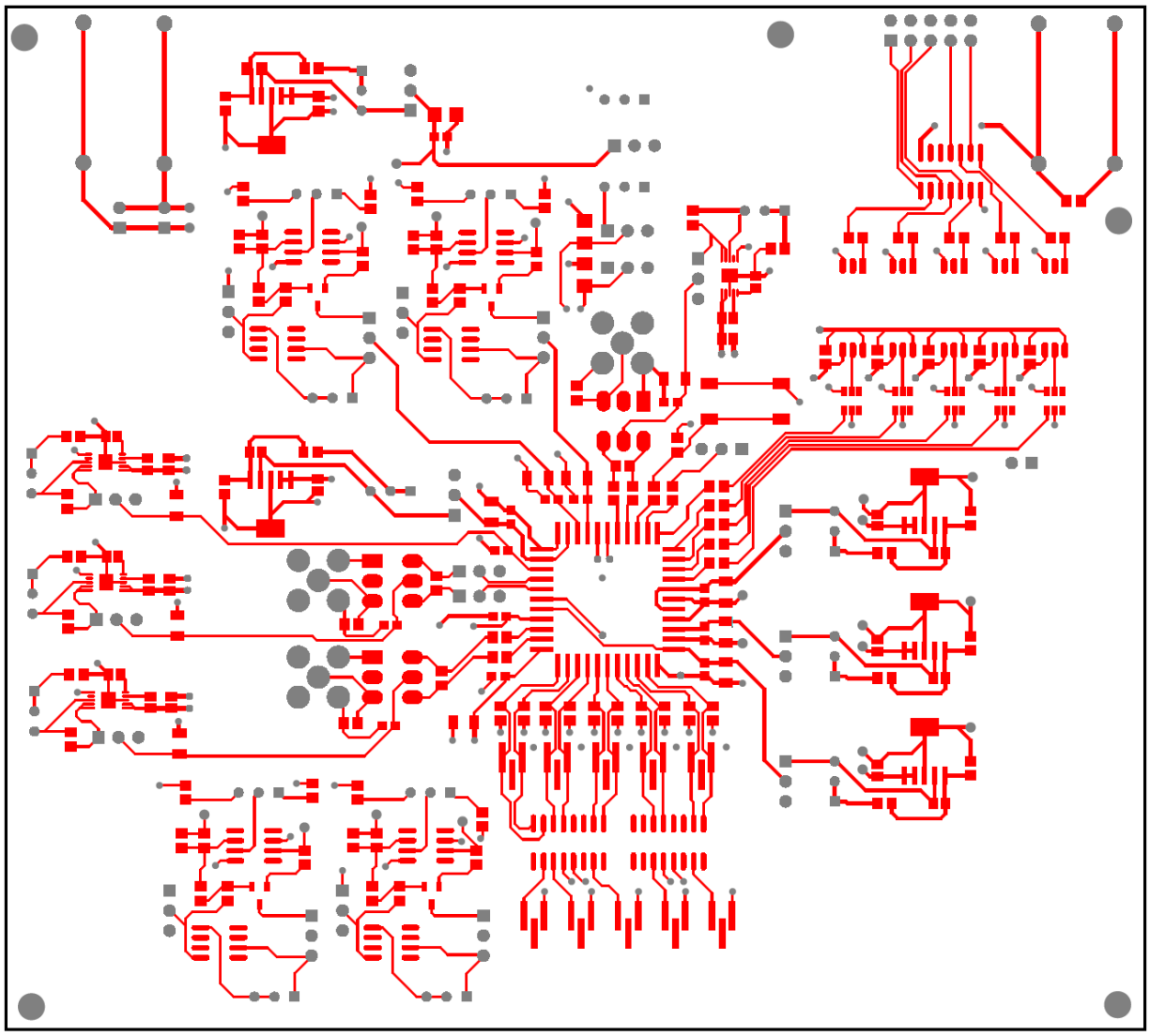

Figure 1 Annex 3 . Layout1.

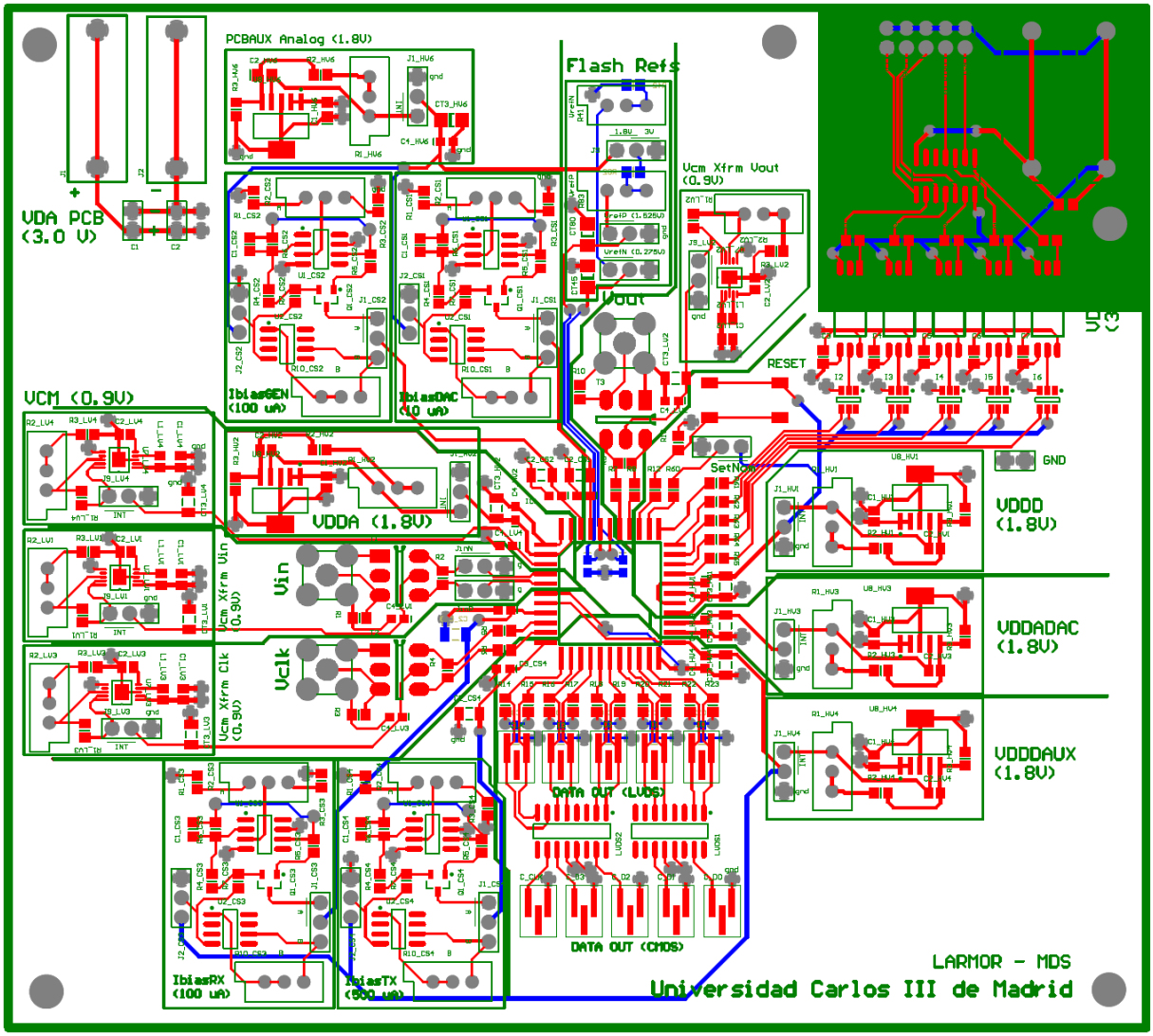

Figure 2 Annex 3 . Layout1

ANNEX IV MATLAB SOFTWARE

%ADC_Test_script

```
%Actualizado Marzo 2017
% 1. En este script se introducen los valores de las variables controlables
% por el registro de desplazamiento.
% 2. Posteriormente se llama a la función que programa el chip.
% 3. Finalmente se ejecuta la función que activa la captura y realiza la FFT
% de los datos de salida del chip.
clear all;
clc;
%a = arduino('com5', 'uno'); %% Ejecutar una vez antes de comenzar las capturas.
format long
%%% DATOS DE PROGRAMACIÓN %%%
% 1. Se introducen los valores de las variables controlables
% por el registro de desplazamiento.
IDSET  = [0 1];        %% IDSET LVDS TX
AUXBUF = [0 0 0 0 0];   %% AUXBUFFER<4:0> - V5, V4, V3, V2, V1.
DWA_TM = 1 ;           %% DWA_TM = 1 --> Modo transparente ON --> DWA APAGADO. DWA_TM = 0 --> DWA Encendido
DELAY  = [0 0];        %% Delay_prog
%Se piden las variables de los DAC y Condensadores por el online
%Esta entrada pide los valores mínimos de inicio de las pruebas de los DAC y Condensadores
prompt={'Introduce el valor DAC5 0 (min) a 7 (max).Nominal 4 ','Introduce el valor DAC4 0 (min) a 3 (max).Nominal 2',...
'Introduce el valor DAC2 0 (min) a 3 (max).Nominal 2','Introduce el valor DAC1 0 (min) a 3 (max).Nominal 2',...
'Introduce el valor C4 0 (min) a 15 (max).Nominal 8 ','Introduce el valor C3 0 (min) a 3 (max).Nominal 8',...
'Introduce el valor C3 0 (min) a 3 (max).Nominal 8','Introduce el valor C3 0 (min) a 3 (max).Nominal 8' };
   dlg_title='Entrada datos de valor minimo de inicio pruebas DAC y Condensadores';
   num_lines=1;
   default={'4','2','2','2','8','8','8','8'};
   resultado_min=str2double(inputdlg(prompt,dlg_title,num_lines,default));
%asignamos los valores a variables con nombre para que sea mas comprensible el codigo
DAC5_min = resultado_min(1);
DAC4_min = resultado_min(2);
DAC2_min = resultado_min(3);
DAC1_min = resultado_min(4);
C4_min   = resultado_min(5);
C3_min   = resultado_min(6);
C2_min   = resultado_min(7);
C1_min   = resultado_min(8);
%Esta entrada pide los valores máximos de final de las pruebas de los DAC y Condensadores
prompt={'Introduce el valor DAC5 0 (min) a 7 (max).Nominal 4 ', 'Introduce el valor DAC4 0 (min) a 3 (max).Nominal 2',...
'Introduce el valor DAC2 0 (min) a 3 (max).Nominal 2','Introduce el valor DAC1 0 (min) a 3 (max).Nominal 2',...
'Introduce el valor C4 0 (min) a 15 (max).Nominal 8 ','Introduce el valor C3 0 (min) a 3 (max).Nominal 8',...
'Introduce el valor C3 0 (min) a 3 (max).Nominal 8','Introduce el valor C3 0 (min) a 3 (max).Nominal 8' };
   dlg_title='Entrada datos de valor maximo de fin de  pruebas DAC y Condensadores';
   num_lines=1;
   default={'4','2','2','2','8','8','8','8'};
   resultado_max=str2double(inputdlg(prompt,dlg_title,num_lines,default));
%asignamos los valores a variables con nombre para que sea mas comprensible el codigo
DAC5_max = resultado_max(1);
DAC4_max = resultado_max(2);
DAC2_max = resultado_max(3);
DAC1_max = resultado_max(4);
C4_max   = resultado_max(5);
C3_max   = resultado_max(6);
C2_max   = resultado_max(7);
C1_max   = resultado_max(8);
%Esta entrada pide los valores de paso de cada uno de los DAC y Condensadores
prompt={'Introduce el valor DAC5 1 (min) a 7 (max).Nominal 4 ','Introduce el valor DAC4 1 (min) a 3 (max).Nominal 2',...
'Introduce el valor DAC2 0 (min) a 3 (max).Nominal 2','Introduce el valor DAC1 0 (min) a 3 (max).Nominal 2',...
'Introduce el valor C4 0 (min) a 15 (max).Nominal 8 ', 'Introduce el valor C3 0 (min) a 3 (max).Nominal 8',...
'Introduce el valor C2 0 (min) a 3 (max).Nominal 8','Introduce el valor C1 0 (min) a 3 (max).Nominal 8' };
```

```
   dlg_title='Entrada datos del valor de salto enn los bucles for';
   num_lines=1;
   default={'1','1','1','1','1','1','1','1','1'};
   resultado_paso=str2double(inputdlg(prompt,dlg_title,num_lines,default));
%asignamos los valores a variables con nombre para que sea mas comprensible
%el codigo
DAC5_paso = resultado_paso(1);
DAC4_paso = resultado_paso(2);
DAC2_paso = resultado_paso(3);
DAC1_paso = resultado_paso(4);
C4_paso   = resultado_paso(5);
C3_paso   = resultado_paso(6);
C2_paso   = resultado_paso(7);
C1_paso   = resultado_paso(8);
% Bucle anidado que genera todas las combinaciones posibles de los datos
% introducidos.
tic;
for DAC5 = DAC5_min:DAC5_paso:DAC5_max
for DAC4 = DAC4_min:DAC4_paso:DAC4_max
for DAC2 = DAC2_min:DAC2_paso:DAC2_max
for DAC1 = DAC1_min:DAC1_paso:DAC1_max
for C4 = C4_min:C4_paso:C4_max
for C3 = C3_min:C3_paso:C3_max
for C2 = C2_min:C2_paso:C2_max
for C1 = C1_min:C1_paso:C1_max
programar_chip(a,IDSET,AUXBUF,DAC5,DAC4,DAC2,DAC1,DWA_TM,DELAY,C4,C3,C2,C1);
   [SNDR,AdBFs,ENOBQ,y] =
ADC_Analyzer_Automatico(a,IDSET,AUXBUF,DAC5,DAC4,DAC2,DAC1,DWA_TM,DELAY,C4,C3,C2,C1); %% Se debe pasar
el handler de la comunicacion con arduino.
   if exist('Results') == 1
      [f c] = size(Results);
      k = f+1;
   elseif exist('Results') == 0
      Results = 0;
      k = 1;
   end
   Results(k,1) = k;
   Results(k,2) = AdBFs;
   Results(k,3) = SNDR;
   Results(k,4) = ENOBQ;
   Results(k,5) = DAC1;
   Results(k,6) = DAC2;
   Results(k,7) = DAC4;
   Results(k,8) = DAC5;
   Results(k,9) = C1;
   Results(k,10) = C2;
   Results(k,11) = C3;
   Results(k,12) = C4;
   Results;
ResultsTable = array2table(Results,...
  'VariableNames',{'k','AdBFS','SNR','ENOBQ','DAC1','DAC2','DAC4','DAC5','C1','C2','C3','C4'})
end
end
end
end
end
end
end
end
tiempo=toc;
 dir=['Y:\LOW IF\Medidas_DEC16_TO3\Capturas\TEST19\'];
save([dir 'Results.mat'],'ResultsTable');
writetable(ResultsTable,[dir 'Results.xls'])
```

% Programar_chip

```
% Actualizado Diciembre 2016

function programar_chip(a,IDSET,AUXBUF,DAC5,DAC4,DAC2,DAC1,DWA_TM,DELAY,C4,C3,C2,C1)

disp(['Enviando programación...']);
% SHIFT REGISTER WORD LENGHT = 35 BITS
DAC5   = de2bi(DAC5,3,'left-msb');      %% DAC5<2:0>
DAC4   = de2bi(DAC4,2,'left-msb');       %% DAC4<1:0>
DAC2   = de2bi(DAC2,2,'left-msb');       %% DAC2<1:0>
DAC1   = de2bi(DAC1,2,'left-msb');       %% DAC1<1:0>
C4     = de2bi(C4,4,'left-msb');     %% C4<3:0>
C3     = de2bi(C3,4,'left-msb');     %% C3<3:0>
C2     = de2bi(C2,4,'left-msb');     %% C2<3:0>
C1     = de2bi(C1,4,'left-msb');     %% C1<3:0>
DATA = [IDSET AUXBUF DAC5 DAC4 DAC2 DAC1 DWA_TM DELAY C4 C3 C2 C1];
DATA = fliplr(DATA); %% Invert DATA word order, so the first bit to write is the last register cell of the shift register.
% D13 - Load CLK
% D12 - Load Enable
% D11 - Shift CLK
% D10 - DATA INPUT
% D9  - Reset - OJO: Logica inversa
% Reset
writeDigitalPin(a, 'D9', 0); %D9  - Reset On (inverse logic)
writeDigitalPin(a, 'D9', 1); %D9  - Reset Off
% Data input
writeDigitalPin(a, 'D12', 1); %D12 = Load Enable
for i = 1:length(DATA)
   writeDigitalPin(a, 'D10', DATA(i)); % D10 = Data
   %disp(['DATO ',num2str(i),':',num2str(DATA(i))])
   pause(0.0001)
   writeDigitalPin(a, 'D11', 1); %D11 = SHIFT CLK. Avance
   pause(0.0001)
   writeDigitalPin(a, 'D11', 0); %D11 = SHIFT CLK. Avance
end
writeDigitalPin(a, 'D11', 1); %D11 = SHIFT CLK. Avance
writeDigitalPin(a, 'D11', 0); %D11 = SHIFT CLK. Avance
% Load data
writeDigitalPin(a, 'D13', 1); %D13 = Load CLK to Load the data into the memory register.
pause(0.0001)
writeDigitalPin(a, 'D13', 0); %D13 = Load CLK
writeDigitalPin(a, 'D12', 0); %D12 = Load Enable
pause(0.0001)
disp(['Programación enviada.']);
disp([' ']);
% All set to zero
writeDigitalPin(a, 'D13', 0);
writeDigitalPin(a, 'D12', 0);
writeDigitalPin(a, 'D11', 0);
writeDigitalPin(a, 'D10', 0);
writeDigitalPin(a, 'D9', 1);
end
```

%ADC_Analyzer_Automatico

```
%Función para analizar señal digital de salida. Chip LARMOR TO3
% Actualizado Febrero 2017
function [SNDR2,AdBFs,ENOBQ,y] =
ADC_Analyzer_Automatico(a,IDSET,AUXBUF,DAC5,DAC4,DAC2,DAC1,DWA_TM,DELAY,C4,C3,C2,C1)
% REALIZAR CAPTURA. Enviar señal al analizador lógico a través de placa arduino:
writeDigitalPin(a, 'D5', 1);
writeDigitalPin(a, 'D5', 0);
disp(['Esperando captura del analizador lógico...']);
pause(9) % Pausa para que el analizador lógico tenga tiempo de escribir los datos
%%%%%%%%%%%%%%%%%% PARÁMETROS DE ENTRADA %%%%%%%%%%%%%%%%%%%%%%%%
filename = ['X:\LARMOR_TO3\captura.csv'];    % FILE that contains captured data
Vfs=0.8;          % Fullscale voltage (Vp)
%dBinput=-10;        % Input power (dBFS)
maxBW=5e6;      % Upper bandwidth limit (Hz)
minBW=4e6;      % Lower bandwidth limit (Hz)
fs=160e6;         % Sampling freq (Hz)
exp_fft_points=16;  % Desired FFT points (exponent). Can be less or equal to captured data length.
                % Si exp_fft_points es menor que el num de datoscapturados, se hace la mediana de las FFT.
 %%%%%%%%%%%%%%%%%% LECTURA DE ARCHIVO DE DATOS %%%%%%%%%%%%%%%%%%
delimiter = ' ';
startRow=2;
endRow=inf;
formatSpec = '%d';
[fid,msg] = fopen(filename,'r');
dataArray = textscan(fid, formatSpec, endRow(1)-startRow(1)+1, 'Delimiter', delimiter, 'MultipleDelimsAsOne', true,
'EmptyValue' ,NaN,'HeaderLines', startRow(1)-1, 'ReturnOnError', false, 'EndOfLine', '\r\n');
closed = fclose(fid);
MyBus1 = dataArray{:, 1};
data = MyBus1(:,1);
%%%%%%%%%%%%%%%%%% CÁLCULO DE PARÁMETROS %%%%%%%%%%%%%%%%%%%%%%%%
ly=length(data);
exp_captured_data = floor(log(ly)/log(2));
y = data(length(data)-(2^(exp_captured_data))+1:end); %% Por si la captura no es de 2^(numero entero) ??
disp(' ')
disp(['Puntos capturados disponibles: 2^',num2str(exp_captured_data)])
disp(['Puntos utilizados para la FFT: 2^',num2str(exp_fft_points)])
fft_points=2^exp_fft_points;          % Número de puntos de la FFT
bin_size=fs/fft_points;               % Tamaño del bin
fbinmaxBW=round((maxBW/fs)*fft_points)*bin_size;
fbinminBW=round((minBW/fs)*fft_points)*bin_size;
fBW1=ceil(fbinminBW/bin_size)+1;       % Bin ancho de banda (inferior)
fBW2=ceil(fbinmaxBW/bin_size)+1;       % Bin ancho de banda (superior)
vfreq=(fs/fft_points:fs/fft_points:fs/2) - ((fs/fft_points));  % Creamos eje de frecuencias.
pieces = 2^exp_captured_data / 2^exp_fft_points;              % Vemos cuantas FFT se calcularán (en caso de promedio).
%%%%%%%%%%%%%%%% Data Calculation and display %%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%% FFT Calculation %%%%%%%%%%%%%%%%%%
[SNR2, SNDR2, y1_spec, toneBin, tone_pwr, dB_Tone, signalBins, Harmonics, noiseBinsHR] =
calcSNR1_v5(y,fBW1,fBW2,fft_points);
% Results calculation %
AdBFs=dB_Tone;
Atone=Vfs*10^(AdBFs/20);
ENOB = (SNDR2-AdBFs-1.76)/6.02;
ENOBQ = (SNR2-AdBFs-1.76)/6.02;
%Frecuencia de entrada. Hay que restar uno porque las frecuencias no calzan con el indice del bin
%de la matriz. Los incides de las matrices empiezan en 1. Las frecuencias en 0.
info_Freq = (toneBin-1)*bin_size;
% Graphical results generation %
figure1 = figure(1);
%figure1 = figure('PaperPosition', [0.63 0.63 27.2736 18.9312],'PaperSize',[20.98 29.68],'PaperOrientation','landscape');
clf;
% FFT LOGARITMICA
axes1 = axes('Position',[0.0613095238095239 0.44 0.413489523809524 0.5],'XMinorGrid','on','Parent',figure1);
% FFT completa
```

```
x1 = vfreq;
%AjusteTono=AdBFs-dbv(tone_pwr);
AjusteTono=0;
y1 = dbv(y1_spec(1:fft_points/2))+AjusteTono;
semilogx1 = semilogx(...
    x1,y1,...
    'Color',[0 0 1],...
    'Parent',axes1);
hold on
    x2 = vfreq(signalBins);
    y2 = dbv(y1_spec(signalBins))+AjusteTono;
    semilogx2 = semilogx(...
        x2,y2,...
        'Color',[0 1 0],...
        'LineStyle','none',...
        'Marker','.',...
        'Parent',axes1);
     xT = vfreq(toneBin);
    yT = dbv(tone_pwr)+AjusteTono;
        semilogxT = semilogx(...
        xT,yT,...
        'Color','red',...
        'LineStyle','none',...
        'Marker','*',...
        'Parent',axes1);
     x3 = vfreq(Harmonics);
    y3 = dbv(y1_spec(Harmonics))+AjusteTono;
    semilogx3 = semilogx(...
        x3,y3,...
        'Color',[0 1 0],...
        'LineStyle','none',...
        'Marker','.',...
        'Parent',axes1);
    x4 = vfreq(noiseBinsHR);
    y4 = dbv(y1_spec(noiseBinsHR))+AjusteTono;
    semilogx4 = semilogx(...
        x4,y4,...
        'Color',[1 0 1],...
        'LineStyle','none',...
        'Marker','.',...
        'Parent',axes1);
%%%%%axis(axes1,[500e3 80e6 -120 0]);
axis(axes1,[10e3 80e6 -120 0]);
txt={['SNDR = ' num2str(SNDR2,3) 'dB, ENOB = ' num2str(ENOB,3) ' bits'],['AdBFs = ' num2str(AdBFs,3) ' dB, Frequency = '
num2str(info_Freq) ' Hz']};
title(axes1,txt);
xlabel(axes1,'frequency (Hz)');
ylabel(axes1,'Magnitude (dBFS)');
grid(axes1,'on');
% FFT LINEAL
axes3 = axes('Position',[0.528571428571429 0.44 0.445028571428572 0.5],'Parent',figure1);
%axes3 = subplot(2,2,2)
%%axis(axes3,[3e6 7e6 -120 0]);
axis(axes3,[10e3 6e6 -120 0]);
title(axes3,txt);
xlabel(axes3,'frequency (Hz)');
ylabel(axes3,'Magnitude (dBFS)');
grid(axes3,'on');
hold(axes3,'all');
x5 = vfreq;
y5 = dbv(y1_spec(1:fft_points/2))+AjusteTono;
plot1 = plot(...
    x5,y5,...
    'Color',[0 0 1],...
```

```
    'Parent',axes3);
% HISTOGRAMA
axes4 = axes('CLim',[1 2],'Position',[0.132142857142857 0.08 0.249438095238098 0.280285824411135],...
    'XTick',[0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15],'Parent',figure1);
hist(axes4,y,[0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15])
histmax=max(hist(axes4,y,[0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15]));
axis(axes4,[0 15 0 histmax+(histmax*0.15)]);
xlabel(axes4,'Quantizer levels');
% INFORMACION DE PARAMETROS
% Create textbox
 parameters={[' '],...
     ['CHIP number 04'],...
     ['Points of each FFT: 2e' num2str(exp_fft_points)],...
     ['Adquired points: 2e' num2str(exp_captured_data) ', Number of averaged FFTs: ' num2str(pieces)],...
     [' '],...
     ['Vfs = ' num2str(Vfs) ],...
     ['Clock frequency = ' num2str(fs*10^-6) ' MHz'],...
     [' '],...
     ['AdBFs = ' num2str(AdBFs,4) ' dB, Atone (aprox.) = ' num2str(Atone,4) ' V, Input tone frequency = ' num2str(info_Freq) '
Hz'],...
     ['SNDR = ' num2str(SNDR2,4) ' dB -> ENOB = ' num2str(ENOB,3) ' bits'],...
     ['Programming values:'],...
     ['LVDSTX IDSET: [ ' num2str(IDSET) ' ]   //   AUXBUF: [ ' num2str(AUXBUF) ' ]'],...
     ['DWA Transparent Mode: ' num2str(DWA_TM) '   //   Clock delay: [ ' num2str(DELAY) ' ]'],...
     [' '],...
     ['DAC1: ' num2str(DAC1) ' // DAC2: ' num2str(DAC2) ' // DAC4: ' num2str(DAC4) ' // DAC5: ' num2str(DAC5)],...
     [' '],...
     ['C1: ' num2str(C1) ' // C2: ' num2str(C2) ' // C3: ' num2str(C3) ' //  C4: ' num2str(C4)],...
     };
annotation1 = annotation(...
  figure1,'textbox',...
  'Position',[0.526190476190477 0.08 0.599509523809525 0.278998758029981],...
  'FitHeightToText','off','LineStyle','none',...
  'String',parameters);
disp(['Bin Size: ',num2str(bin_size),' Hz'])
disp(['SNDR = ' num2str(SNDR2,5) ' dB --> ENOB(wD) = ' num2str((SNDR2-AdBFs-1.76)/6.02,5) ' bits'])
disp(['SNR = ' num2str(SNR2,5) ' dB --> ENOB(Quant) = ' num2str((SNR2-AdBFs-1.76)/6.02,5) ' bits'])
disp(' ')
disp(' ')
D = ['TEST19']; % Directorio para guardar figuras. Nombre del grupo de capturas.
fnamefig = ['Y:\LOW IF\Medidas_DEC16_TO3\Capturas\' D '\ Dataset_CHIP_04_' D '_ENOBQ_' num2str(ENOBQ,4)
'_SNDR_' num2str(SNDR2,4) '_AdBFs_' num2str(AdBFs,4) '_DWATM_' num2str(DWA_TM) '_C1_' ...
    num2str(C1) '_C2_' num2str(C2) '_C3_' num2str(C3) '_C4_' num2str(C4) '_DAC1_' num2str(DAC1) '_DAC2_' num2str(DAC2)
'_DAC4_' num2str(DAC4) '_DAC5_' num2str(DAC5) '.png'];
%saveas(figure1,fnamefig,'png')
fnamefig2 = ['Y:\LOW IF\Medidas_DEC16_TO3\Capturas\' D '\ Dataset_CHIP_04_' D '_ENOBQ_' num2str(ENOBQ,4)
'_SNDR_' num2str(SNDR2,4) '_AdBFs_' num2str(AdBFs,4) '_DWATM_' num2str(DWA_TM) '_C1_' ...
    num2str(C1) '_C2_' num2str(C2) '_C3_' num2str(C3) '_C4_' num2str(C4) '_DAC1_' num2str(DAC1) '_DAC2_' num2str(DAC2)
'_DAC4_' num2str(DAC4) '_DAC5_' num2str(DAC5) '.fig'];
%saveas(figure1,fnamefig2,'fig')
signalname = ['Y:\LOW IF\Medidas_DEC16_TO3\Capturas\' D '\ Dataset_CHIP_04_' D '_ENOBQ_' num2str(ENOBQ,4)
'_SNDR_' num2str(SNDR2,4) '_AdBFs_' num2str(AdBFs,4) '_DWATM_' num2str(DWA_TM) '_C1_' ...
    num2str(C1) '_C2_' num2str(C2) '_C3_' num2str(C3) '_C4_' num2str(C4) '_DAC1_' num2str(DAC1) '_DAC2_' num2str(DAC2)
'_DAC4_' num2str(DAC4) '_DAC5_' num2str(DAC5) '.mat'];
end
%save(signalname,'y');

%figure(2)
%plot(y)
%axis([1 1000 0 15]);
```

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