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DOCTORAL THESIS

Contribution to time domain readout circuits design for multi-standard sensing system for low voltage supply and high-resolution applications

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TESIS DOCTORAL

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To the crazy people in this world

Acknowledgment

All the work presented in this thesis come out as my research during several years. However, all the actions that I performed to achieve the results that I obtained couldn´t be possible without all the help that I received during this time from several people that I will try to summarize here. In first place I would like to thank all my researching team for been there every time as back up for some questions or motivation for pending actions. In special the director of the thesis, Enrique Prefasi. During my time in Austria I also received a lot of help to create the prototype with all the actions that I never done before, in the electrical design I would like to thank Cesare Buffa, Christopher Rogi and Richard Gaggl for their support. During my time in the laboratory doing the measurements I had the support from really good people that have make things much easier for me, thanks to Bernhard Kuttin, Andreas and Alex.

All the motivation to continue with this work has been crucial for me. I have to say thanks to all the people that have push me in the right direction. Eric, Marta, Marcos, David, Maxi and Luis. You have been always there making me believe that I was able to finish it.

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Mamá, nada tendría sentido sin todo lo que tú me has dado.

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List of Abbreviations

ADC	analog-to-digital converter
BW	bandwidth
CCD	charge-coupled device
CDC	capacitance-to-digital converter
CDS	correlated double sampling
CMOS	complementary metal-oxide-semiconductor
DAC	digital-to-analog converter
DS	dual slope
EMC	electromagnetic compatibility
ENOB	efficient number-of-bits
$\mathbf{f_{clk}}$	clock frequency
$\mathbf{f_s}$	sampling frequency
FFT	fast Fourier transform
IDC	incremental data converters
IoT	internet-of-things
LSB	least-significant bit

List of Abbreviations

MASH	multistage noise-shaping
MEMS	micro-electromechanical system
NTF	noise transfer function
OSR	oversampling ratio
PVT	process-voltage-temperature
SAR	successive approximation register
SC	switched capacitors
SNR	signal-to-noise ratio
STF	signal transfer function
VCO	voltage-controlled oscillator
$\mathbf{V_{FS}}$	full-scale voltage
ZCD	zero-crossing detector

List of Publications and Biography

This thesis is based on work already published during the course of the doctoral research period, and therefore coincides partially with the following contributions:

- J. Pérez Sanjurjo, E. Prefasi, C. Buffa, and R. Gaggl, “A Capacitance-To-Digital Converter for MEMS Sensors for Smart Applications,” Sensors, vol. 17, no. 6, p. 1312, Jun. 2017.
- Sanjurjo J.P., Prefasi E., Buffa C., Rogi C., Gaggl R. (2018) A High-Resolution Self-Oscillating Integrating Dual-Slope CDC for MEMS Sensors. In: Harpe P., Makinwa K., Baschirotto A. (eds) Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design. Springer, Cham

Papers in Journals

- J. Pérez Sanjurjo, E. Prefasi, C. Buffa, and R. Gaggl, “A Capacitance-To-Digital Converter for MEMS Sensors for Smart Applications,” Sensors, vol. 17, no. 6, p. 1312, Jun. 2017.

Papers in Conference Proceedings

- J. P. Sanjurjo, E. Prefasi, C. Buffa and R. Gaggl, "An energy-efficient 17-bit noise-shaping Dual-Slope Capacitance-to-Digital Converter for MEMS

sensors," ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Lausanne, 2016.

- J. P. Sanjurjo and E. Prefasi, "A high-sensitivity reconfigurable integrating dual-slope CDC for MEMS capacitive sensors," *2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Glasgow, 2015
- J. P. Sanjurjo, E. Prefasi and L. Hernandez, "A 1.2V low-power high-resolution noise-shaping ADC using multistage time encoding converters for biomedical applications," *2014 10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Grenoble, 2014

Chapters in Books

- Sanjurjo J.P., Prefasi E., Buffa C., Rogi C., Gaggl R. (2018) A High-Resolution Self-Oscillating Integrating Dual-Slope CDC for MEMS Sensors. In: Harpe P., Makinwa K., Baschirotto A. (eds) Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design. Springer, Cham

Patents

- Gaggl, Richard; Prefasi, Enrique; Perez Sanjurjo, Francisco Javier; Buffa, Cesare, "Self-oscillating dual-slope integrating quantizer for sigma delta modulators"

Other publications of the author

- J. P. Sanjurjo, E. Prefasi, L. Hernández, "Second-Order Noise-Shaping ADC using a Passive Integrating Quantizer for Biomedical Applications," DCIS Conference 2013: XXVIII edition of "Conference on Design of Circuits and Integrated Systems, Donosti, 2013.

Biography

Javier Pérez Sanjurjo was born in Madrid, Spain, in 1988. He obtained the B.S. degree in electrical engineering and the M.S. degree in Advanced Electronic Systems from Carlos III University of Madrid, Spain, in 2012 and 2014, respectively, where he is currently a student of the Ph.D. program in Electricity, Electronics and Automatic. He had worked for two years during his Ph.D. activity at Infineon Technologies in Villach, Austria. Nowadays, he is working as an analog designer for space applications in Video department at Airbus Defense & Space (ADS). His interest are readout circuits, sensors, environmental instrumentation systems and biomedical instrumentation systems.

Abstract

This research activity has the purpose of open new possibilities in the design of capacitance-to-digital converters (CDCs) by developing a solution based on time domain conversion. This can be applied to applications related with the Internet-of-Things (IoT). These applications are present in any electronic devices where sensing is needed. To be able to reduce the area of the whole system with the required performance, micro-electromechanical systems (MEMS) sensors are used in these applications. We propose a new family of sensor readout electronics to be integrated with MEMS sensors.

Within the time domain converters, Dual Slope (DS) topology is very interesting to explore a new compromise between performances, area and power consumption. DS topology has been extensively used in instrumentation. The simplicity and robustness of the blocks inside classical DS converters it is the main advantage. However, they are not efficient for applications where higher bandwidth is required. To extend the bandwidth, DS converters have been introduced into ΔΣ loops. This topology has been named as integrating converters. They increase the bandwidth compare to classical DS architecture but at the expense of higher complexity. In this work we propose the use of a new family of DS converters that keep the advantages of the classical architecture and introduce noise shaping. This way the bandwidth is increased without extra blocks. The Self-Compensated noise-shaped DS converter (the name given to the new topology) keeps the signal transfer function (STF) and the noise transfer function (NTF) of Integrating converters. However, we introduce a new arrangement in the core of the

converter to do noise shaping without extra circuitry. This way the simplicity of the architecture is preserved.

We propose to use the Self-Compensated DS converter as a CDC for MEMS sensors. This work makes a study of the best possible integration of the two blocks to keep the signal integrity considering the electromechanical behavior of the sensor.

The purpose of this front-end is to be connected to any kind of capacitive MEMS sensor. However, to prove the concepts developed in this thesis the architecture has been connected to a pressure MEMS sensor.

An experimental prototype was implemented in 130-nm CMOS process using the architecture mentioned before. A peak SNR of 103.9 dB (equivalent to 1Pa) has been achieved within a time measurement of 20 ms. The final prototype has a power consumption of 220 μW with an effective area of 0.317 mm^2. The designed architecture shows good performance having competitive numbers against high resolution topologies in amplitude domain.

Resumen

Esta actividad de investigación tiene el propósito de explorar nuevas posibilidades en el diseño de convertidores de capacitancia a digital (CDC) mediante el desarrollo de una solución basada en la conversión en el dominio del tiempo. Estos convertidores se pueden utilizar en aplicaciones relacionadas con el mercado del Internet-de-las-cosas (IoT). Hoy en día, estas aplicaciones están presentes en cualquier dispositivo electrónico donde se necesite sensar una magnitud. Para poder reducir el área de todo el sistema con el rendimiento requerido, se utilizan sensores de sistemas micro-electromecánicos (MEMS) en estas aplicaciones. Proponemos una nueva familia de electrónica de acondicionamiento para integrar con sensores MEMS.

Dentro de los convertidores de dominio de tiempo, la topología del doble-rampa (DS) es muy interesante para explorar un nuevo compromiso entre rendimiento, área y consumo de energía. La topología de DS se ha usado ampliamente en instrumentación. La simplicidad y la solidez de los bloques dentro de los convertidores DS clásicos es la principal ventaja. Sin embargo, no son eficientes para aplicaciones donde se requiere mayor ancho de banda. Para ampliar el ancho de banda, los convertidores DS se han introducido en bucles ΔΣ. Esta topología ha sido nombrada como *Integrating converters*. Esta topología aumenta el ancho de banda en comparación con la arquitectura clásica de DS, pero a expensas de una mayor complejidad. En este trabajo, proponemos el uso de una nueva familia de convertidores DS que mantienen las ventajas de la arquitectura clásica e introducen la configuración del ruido. De esta forma, el ancho de banda aumenta sin bloques adicionales. El convertidor *Self-Compensated noise-shaped DS* (el nombre dado a la nueva topología) mantiene la función de

transferencia de señal (STF) y la función de transferencia de ruido (NTF) de los *Integrating converters*. Sin embargo, presentamos una nueva topología en el núcleo del convertidor para conformar el ruido sin circuitos adicionales. De esta manera, se preserva la simplicidad de la arquitectura.

Proponemos utilizar el *Self-Compensated noise-shaped DS* como un CDC para sensores MEMS. Este trabajo hace un estudio de la mejor integración posible de los dos bloques para mantener la integridad de la señal considerando el comportamiento electromecánico del sensor.

El propósito de este circuito de acondicionamiento es conectarse a cualquier tipo de sensor MEMS capacitivo. Sin embargo, para demostrar los conceptos desarrollados en esta tesis, la arquitectura se ha conectado a un sensor MEMS de presión.

Se ha implementado dos prototipos experimentales en un proceso CMOS de 130-nm utilizando la arquitectura mencionada anteriormente. Se ha logrado una relación señal-ruido máxima de 103.9 dB (equivalente a 1 Pa) con un tiempo de medida de 20 ms. El prototipo final tiene un consumo de energía de 220 μW con un área efectiva de 0.317 mm2. La arquitectura diseñada muestra un buen rendimiento comparable con las arquitecturas en el dominio de la amplitud que muestran resoluciones equivalentes.

Chapter 1.

Introduction, motivation and objectives

1.1. Introduction

Sensing a physical property has been one of the main field of investigation since a long time, sensing temperature or pressure have been possible since XVIII century. However, the world has change a lot since then, different kinds of sensors and connections between them have been developed. In fact, precision, size and connectivity have been the main goals of improvement. Nowadays, a new family of sensors have been used and tested all over the world. They are called Smart Sensors [1]. It is because they are able to calibrate, compensate and transmit data with microprocessor circuits, opening the possibilities of use the sensing data. The evolution of this kind devices has helped in the growing of a new market called, Internet-of-Things (IoT) [2] [3] [4]. In the market of IoT, all the devices are connected through the network, sharing all the information. In the past decade, the applications related with the Internet-of-Things (IoT) have grown exponentially. In this field, smart sensors for environmental measurements (humidity, pressure, temperature and gas) are one of the most demanded

products. All the previous examples have in common the bandwidth that they share. Most of the variables to measure in IoT are in the low frequency domain. If the conversion is done with a high frequency converter, they can even be measured as DC (BW < 50 Hz). The main consequence is that most of the sensing activity will have similar readout outputs. This implies a big effort in developing new kinds of interfaces that are able to work with different type of sensors [5] [6] [7] [8]. To try to make as similar as possible the circuitry for different kind of sensors with a low-cost and energy efficient solution, Micro-Electro-Mechanical Systems (MEMS) sensors have arrived as the next generation of sensors for this purpose [9] [10] [11]. MEMS have the property of being very small in size keeping high performance. Also, they have a low cost per unit thanks to their process of manufacturing. For these reasons, MEMS are mainly used in IoT applications. Similar to a microelectronics component, MEMS are able to be produced in big. To try to make the output behavior similar between different sensing activities, capacitive MEMS are mostly used in IoT. This is one of the reasons why Capacitive-to-Digital Converters (CDC) are selected as one of the main readout topologies to be used in new sensors applications [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22] [23] [24] [25] [26]. They are able to digitize the signal of the MEMS with low power and high resolution which is the main interest in the market. A CDC is composed by an acconditioning signal circuit plus an analog-to-digital converter (ADC). Figure 1-1 shows the main blocks of interest:

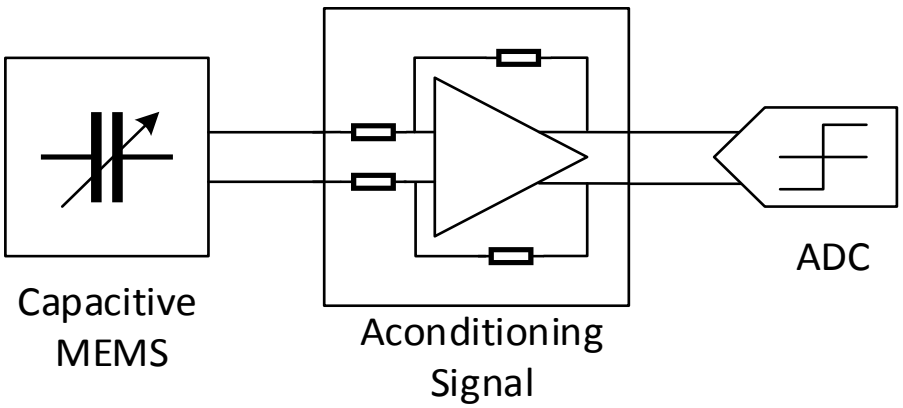

Figure 1-1 Block diagram of a CDC topology

In the open literature, different architectures have been tested as a possible solution for high-resolution CDCs. The typical approach is the use of charge transfer between capacitors to convert the sampled capacitance to voltage. Then this is used as an input for high order multi-bit switch-capacitor (SC) Sigma-Delta (ΔΣ) ADCs [16] [20] [25] [27] [28] [29] [30]. Its high resolution and linearity together with its intrinsic tolerance to analog non-ideal behavior make this option very popular for these applications. However, to reach the target resolution, large area and power demanding blocks are needed. In addition, when low voltage supplies are used, the performance of SC ΔΣ converters is reduced. Other types of solutions have been also proposed: successive approximation register (SAR) converters are good for scaling the CDC [31] [32] [33], IDCs are simple and can reduce the power consumption [34] [35]. Alternative solutions also show different approaches (like period modulation [36], delay-chain discharge [24], voltage-controlled oscillator (VCO) [37] [38] [39], and DS [19]) to reduce area and power consumption even further. Hybrid converters (like SAR + Incremental) takes the properties of the previous topologies [12] [17] [40] [41].

To save power and area keeping the same performance of high resolution CDCs, this thesis explains the development of a topology that is able to detect small capacitance changes while reducing ADC complexity, which is, typically, a critical block area and power wise in the CDC. To be area and energy efficient the proposed ADC is based on the single-bit noise-Shaping Integrating DS converter [42] [43] [44] that maps the amplitude information into the time domain. Compared to traditional Dual-Slope ADCs [45], it introduces quantization error noise-shaping as in standard ΔΣ ADCs. But it does not require multi-bit circuits (i.e.: flash quantizers or n-bit digital-to-analog converters (DACs)) to keep high resolution and performance; instead, it uses single-bit circuitry to exchange amplitude by time resolution allowing to use lower supplies voltages. In addition, this topology has an intrinsically small sensitivity to temperature and process variations. These properties were already shown in [42] [43] [44] [46].

1.2. Motivation of the thesis

The main motivation of this work is to contribute to the research and development of CDC architectures compatible with MEMS sensors to improve the quality and possibilities of the applications that surround the market of IoT.

Devices are becoming smaller and smaller, introducing two main issues, area and power consumption. To keep the performance in designs with a power supply below 1.8 V, new architectures need to be developed that can cope with the resolution given by classic architectures [47].

Time resolution topology is selected as a good candidate to deal with the main constrains mentioned before. In this way, high resolution, low area and power consumption is achievable by architectures that works with single bit circuitry, and therefore doesn't suffer from low voltage supply.

A high number of applications need a lot of different kind of sensors. Develop a single CDC for every of them does not seem an intelligent solution. Specially taking into account that most of the sensors used for this application share the same technology, they are MEMS sensors. A topology that is able to adapt from one application to another with the most possible efficiency seems to be an interesting solution.

Find a solution that can keep the same performances of ΔΣ converters but reducing the area and power consumption to adapt the CDC to new low power applications seems to be not efficient. To be able to deal with the characteristics of two different kind of converters, and hybrid solution that combine time resolution with noise shaping behavior from ΔΣ converters seem to be the perfect solution.

Create a standard package with the properties commented in the previous point can reduce the price and the time to market of many applications, making them useful and efficient.

1.3. Objectives of the thesis

To achieve all the goals that were commented in the motivation of this thesis the following objectives are defined.

- Study the electronic circuitry that has to be attached with the MEMS to create a proper readout topology. As said before, most of the MEMS used in these applications are capacitive MEMS, and therefore they have a measurable output in the capacitance domain. Because of that CDC seems to be the best candidate in readout circuits. In addition, the kind of variables that are going to be measured (gas, humidity, temperature or pressure), need a readout circuit that deals with low frequency source of noise must be selected.

- Taking into account the two outputs of the previous point (capacitance output and low frequency domain), it is not straight clear how to measure the output of the sensor. A study at system level is needed. To connect the sensor with the electronic of the CDC an AC modulation is needed. This modulation will make possible to take the info out of the capacitive sensor and give the data in the low frequency domain.

- Find a topology to use with AC modulation. How to optimize the whole design to make it robust and efficient. The different blocks of the CDC need to be design for the requirements that comes out of the previous study at system level. Making an acconditioning electronic block that is able to give a stable and precise analog signal and an ADC that can be connected with that.

- Develop the topology selected. Create a prototype that has connected the MEMS to the readout electronic, creating the whole CDC for measurement. Perform the research and activities needed to create a silicon solution that can be tested to compare with the State-of-the-Art (SoA) solutions. To achieve this goal, intermediate objectives need to be defined:

- Create a synchronous architecture that deals with the resolution and noise to give expected performances
- Design at circuit level the main components that are going to be needed to have a CDC with all the specifications defined at system level.
- Implement a layout design that deals with non-ideal behavior and EMC.
- Build a setup to make the characterization of the prototype in silicon to compare with the SoA.

• Make the comparation with the SoA. Make a fair study and discussion between the main solutions performed with the different architectures mentioned before. See if the solution performed is useful and if it opens a new field for further investigation, and therefore, what would be the future investigation to keep going with the improvements for the applications.

1.4. Document outline

We have split the work in three different parts. The first one intrudes all the theory of the previous works and the architecture proposed. The second part explain the building process of a prototype using the architecture proposed in the first. It includes the system, circuit, layout and packing considerations that have been considered for proper performances of the prototype. The third part presents the results obtained out of the measurements and compares the architecture with the other architectures used in similar applications and present the conclusions out of the work and a proposition of future activities.

Part I

Chapter 2 present and introduction to the topic. It includes a brief introduction to the market of IoT and smart sensors. The basic knowledge of a capacitance-to-digital-converter (CDC) is presented. To conclude a presentation of the State-of-the-Art of the main topologies of converters used in these kinds of applications is presented with a comparative between them in order to select the topology that we think that fits better for our purpose.

In **Chapter 3** the selected architecture is explained. It includes a selection for the front-end circuitry considering the constrains of the application and the desire performances. It also includes the theoretical explanation of the architecture proposed inf this work. The evolution from the classic DS to the architecture developed during this process is presented with empirical demonstration of the new features and its implication in the transfer function.

Part II

The whole CDC architecture is presented in **Chapter 4**. An explanation of MEMS behavior is included, with special mention the one used for this prototype. The architecture of the CDC is presented at system level with an explanation of every phase of the whole conversion. The design at circuit level is also included with the main parameters selected to minimize the non-ideal effects and optimize the performances. Also, this chapter presents the details that have been taken into account for the layout and packing of the prototype.

Part III

The measurements of the prototypes are presented in **Chapter 5**. It includes an explanation of the setup used during the measurements. The measurements included are the ones that characterize the resolution of the prototype in the whole range. Also, the behavior of the prototype against Temperature is presented.

Introduction, motivation and objectives

In **Chapter 6** a comparison with the State-of-the-Art is presented. The conclusions achieved during the whole research are commented respect to the objectives already presented. The future work that would have to be done to continue con this research is also mentioned.

Part I

Theoretical introduction to CDC for IoT applications and theory of the proposed architecture

Chapter 2.

Sensors and Converters

The purpose of this chapter is to give an introduction to the topic. Give a short introduction the environment, the market of IoT and how the sensors have evolved with that. Also, it will introduce the basic knowledge of a Capacitance to Digital Converter (CDC) and an overview of the state-of-the-art of readout circuits for smart sensors.

2.1. Applications

In the last years, the evolution of technology has changed our world completely. With the introduction of Internet of Thing and smart devices (IoT) a brand-new world for new applications have arrived. Nowadays there are many fields were new devices are required to satisfy new demands. For example, our homes are becoming more intelligent, they can give us information about the temperature outside, probability of rain, the status of the food inside the fridge, or the quality of the air in a certain room. However, this is not enough. With the idea of having all the information possible anytime, the market is evolving in the direction of solutions that are wearable. A watch, a pair of glasses, a smartphone, etc. All these examples have one thing in common, the small size. To be able to have a device that is providing all this information without affecting its size, new solutions need to be developed. The business under these

applications is growing exponentially, the main areas where is already taking a piece of the market are: IoT and Environmental Intelligence.

The concept of (IoT) comes out of the wireless interconnexion of items that surround us. Machines talking to each other and persons talking to machines. Within the last years sensors and networks (autonomous sensing systems) have gained new possibilities of control classical procedures in the human activity where it was not possible before due the spread of wireless networks and power consumption of the electronics. This is due the evolution of integrated circuits. The improvement in energy efficiency, performance and power consumption in the devices help to build an infrastructure much easier than before. There are many environmental parameters that need to be measured and controlled in different fields: home, automotive, energy management, industry, etc. [48]. An important new field needs to be mentioned, the quality in food and drinks. Avoid any possible contamination due a bad state of the food or detect products that have a carcinogenic effect is an important improvement hat will improve the quality of our health in the close future. The company Gartner says that 8.4 billion connected things will be used in 2017, a 31 % increase with the previous year. Also, it expected that by 2025 IoT nodes will connect most of the items in our day to day life [49]. To this goal will be achieved thanks to the development in smart sensors, nanotechnology and miniaturization of sensors. A common use of sensors is to use them to gather environmental information from different mediums. The importance of monitoring of the environmental can be reduced to two main topics, fresh water and fresh air, which are the main responsible of our health. There is the need of build sensors able to detect anything that mixes with the water and change it properties: organic matters, inorganic matters, radioactive waste. In special, plastic is considered major ocean pollutants, which causes severe harm in water properties. The same needs come from detecting the different toxic gases that contribute to air, like sulphur dioxide (SO2), or ozone (O3). The wide varieties of the sensors for the environment monitoring are

needed, namely, temperature, humidity, light intensity, wind speed, pressure, salinity, oxygen, toxic gases, and many more.

IoT puts together all this information with the inter-connection of sensors machines and persons to share the information in the whole world. Its main purpose is to access different items of our daily life and controlled them as good as possible. However, connect people through internet implies a big cost in infrastructure, in special in remote areas. The introduction of Low-cost smart sensors nodes is easy in the applications and reduce this issue.

2.2. Sensors and front-end solutions

As it was explained before, smart sensors are changing the intelligent systems. They provide new features that previously could not be performed by the common sensors, regarding economic or technical topics. Typical undesired characteristics of sensors like input offset, linearity, temperature effect can be automatically corrected by the digital part included in smart sensors. This feature helps to solve different technical and economic problems. As these operations are carried in software, no additional hardware is required. Therefore, it is possible to calibrate with digital control and there is no need to remove the sensor from its current environment or test fixture. For this reason, smart sensors are known for their standardized physical connection to enable the communication with the digital processor and therefore with the network. Also, smart sensors can perform different functions like sensing, self-calibration or ranging. These sensors can detect different parameters and change the programmability of the electronics in order to give precise data for different inputs.

Smart sensors open a new world of applications thanks to their properties. However, to go further in the integration of the sensor with the circuit there are physical constrains that are not possible to break. That is why a new generation of sensors have grown related with this market in the last years, the silicon-based sensors. Build sensors

in the same way of their Integrated Circuits front-ends helps to reduce the size, power consumption and price of the device. For example, complementary metal-oxide-semiconductor (CMOS) technology can be used. The CMOS charge-coupled device (CCD) [50] used in cameras are a good example of a mature sensor made in CMOS technology and it shows the possibility of integration and a high level of performance. However, there is a new kind of sensor that is becoming the more used of the integrated sensors. Its advantages of integration with the electronics plus the good performance are making MEMS (Micro-Electro-Mechanical Systems) sensors the new trend in front-end solutions.

2.3. Capacitance-to-Digital Converter

Capacitance-to-Digital Converter (CDC) [51] is the most used electrical circuitry with capacitance sensors. Any kind of sensor that has an output in the capacitance domain is a candidate to be used with this topology. However, the trend to create circuitry that is able to be connected with different interfaces (as can be seen in Figure 2-1) is the main reason of the upcoming interest in CDC topologies, specially inside the market of IoT. This is possible thanks to some constrains in the applications that were mentioned before. All the variables that are going to be measured of different applications have something in common. The bandwidth of all these signals is close to DC (BW < 50 Hz). It helps to target the bandwidth of interest to this value inside the CDC parameters of conversion and therefore to be able to measure all the different sources. To be able to work in an efficient way with multiple sensors, the CDC need to make some adjustments for every signal. To achieve this porpoise a configurable acconditioning step is included. Once the CDC is able to target different source of information, it needs to adapt the resolution specified for each application. This is one of the main advantages of use a CDC architecture with low BW input signals. Each sensing magnitude needs different level of precision in each application. Because of that the resolution in the CDC is given thanks to two different properties. The first one and

more obvious is the resolution of the ADC. The ADC is design to give certain resolution in a specific sample time.

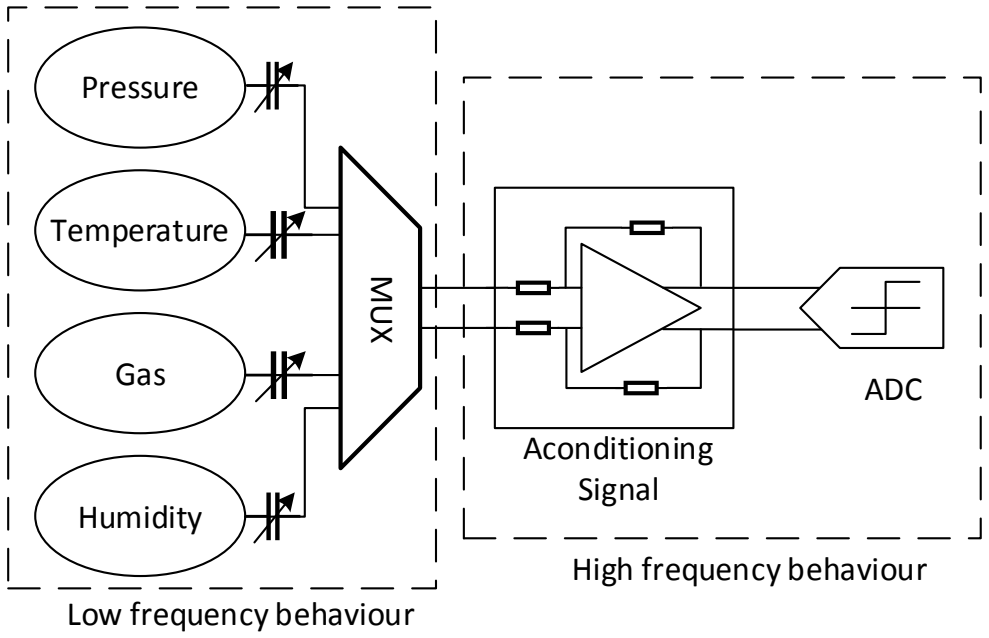

Figure 2-1 Block diagram of an IDC converter

However, the resolution can be extended in these applications increasing the measuring time. Considering that the signals to convert have a frequency below 50 Hz, the CDC can be connected to one input signal and acquire a lot of samples for decimation that will increase the precision to the DC value. As it is explained in Figure 2-2, when more samples are taken for one input signal, the BW where the noise is integrated is smaller and therefore the Signal to Noise Ratio (SNR) increases.

Taking this property into account, a CDC for low bandwidth sensors signals scale the minimum resolution required with the resolution of the ADC and the signals that required more resolution use decimation technic. The resolution that is possible to increase depends on the time constrains of the system and the initial resolution of the ADC. The time constrains can be due the total physical time per conversion of all the

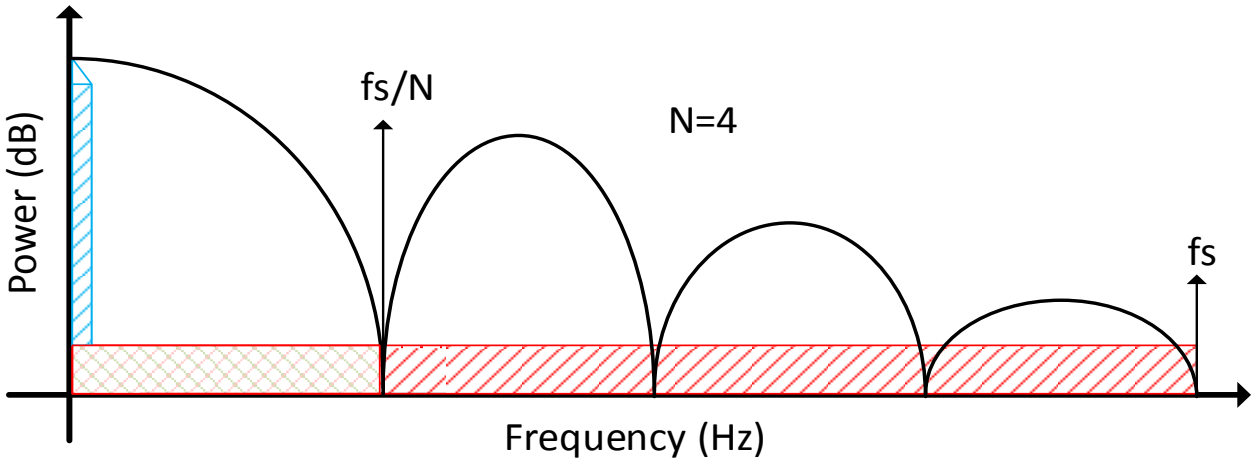

Figure 2-2 Relation between Signal and noise related with the sample frequency

inputs (normally the data need to be updated every 0.1-1 second) or the ADC topology. Depends on the ADC, the N factor of Figure 2-2 can be only an integer (for Nyquist ADC) or taking into account the oversampling-ratio (OSR) ADCs can be split in smaller resolution requirements. However, to save power, some solutions use discontinuous measurement. The CDC is only switched on for each measurement and extra time the

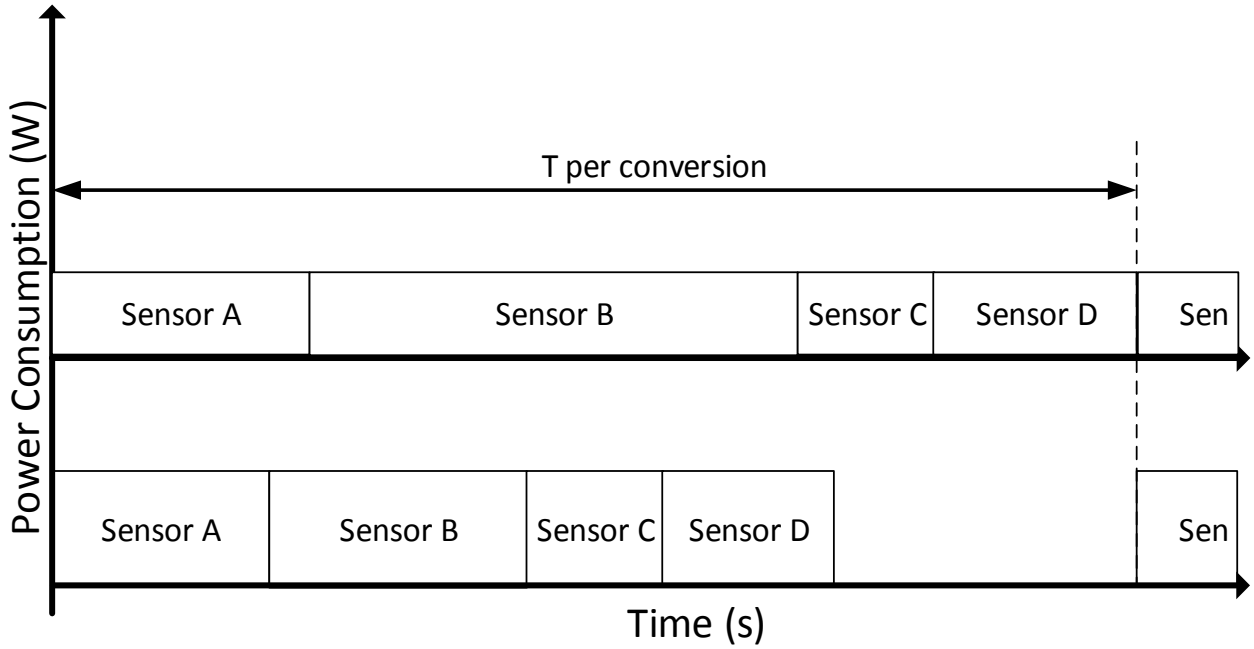

Figure 2-3 Comparison of conversion period between continuous and discontinuous converters

deltas (N/OSR). There are two different methods to make the measurement to use the flexible measuring time. Both are represented in Figure 2-3. The first one is continuous measurement. The CDC is always on and the ADC is converting the whole time, therefore the total time for conversion is split between all the inputs considering their

CDC goes into sleep mode to save power. Systems that use this method normally uses ADCs that give higher resolution in order to avoid extra time in the conversion.

In the State-of-the-Art there are many different possibilities that uses one of the previous methods of measurement. In the next section the main families of converters are presented.

2.4. State-of-the-Art of Converters

As mentioned in the previous section, there are a lot of different topologies of converters used in this type of applications. The amount of converter types is just a consequence of all the types of applications that demands different performances or with different level of relevance. The main constrains for IoT applications are: resolution, power consumption, area, flexibility, voltage power supply, complexity and robustness. Finding a solution that satisfy all of them with a high acceptance level is still out of the limits of the solutions developed. Nowadays, depending on the priority of each constrains, the designers choose a different topology to optimize their design. In this section the main topologies used are presented.

All the topologies can be organized inside two different groups. The ones that do the conversion continuously and the ones that do it discontinuous. It is important to mention that nowadays there is not a prove or understanding that one group or the other is better or worst. Each topology fit better in one of the groups due its architecture constrains.

2.4.1. Continuous Converters

The main idea of continuous converters is that the converter is working all the time. It is not dependant on any system level constrains to start to perform the conversion or to stop to do it. It just needs a sampling time to take the sample from the input. The output data is always available for post-processing giving more flexibility in the measuring time. Inside continuous converters there mainly to different architectures that are used. ΣΔ converters and Integration converters.

2.4.1.1. ΣΔ converters

ΣΔ converters is the favourite candidate in the SoA when that main constrain of the design is the required resolution. This family of converters is well known as the high-resolution converters in the whole range of input frequencies. The two keys of the popularity of ΣΔ are the effect of use an Over Sampling Ratio (OSR) and perform noise-shaping. As it is mentioned in [52] OSR is the ratio between the sampling frequency of the converter divided by two times the bandwidth of the input signal (fs/2*BW). It is proven in [52] that the transfer function of a ΣΔ, with OSR, doesn´t affect the power of the input signal but have an attenuation effect on the in-band-noise. Therefore, every time that the OSR is doubled, the power of in-band-noise is divided by half, or what is the same, by 3 dB. This relation is explained by the Signal to Noise Ratio (SNR) classic equation of an oversampling converter:

$$SNR=6.02*N+1.76+10*\log(OSR) \quad (1)$$

Where N is the number of bits in the quantizer. The noise shaping-behavior come out of the transfer function of the ΣΔ. [52] explains that the noise transfer function (NTF) inside a ΣΔ modulator is affected by a high-pass filter when the signal transfer function (STF) is a simple integrator, as it can be seen in Figure 2-4.

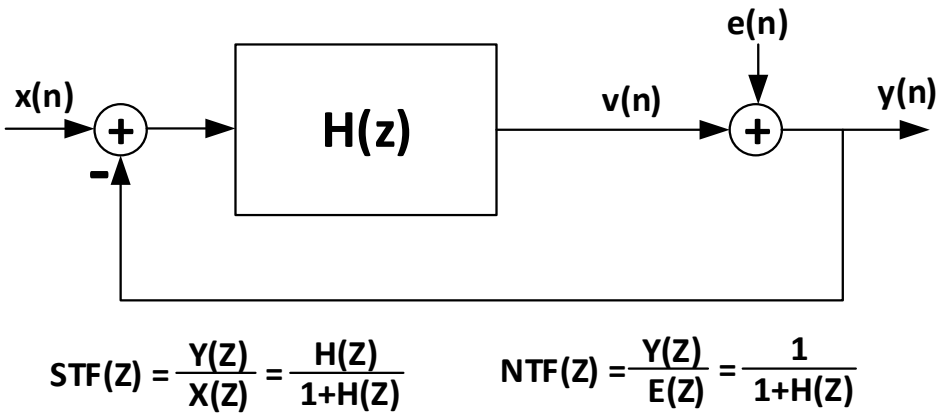

Figure 2-4 Block diagram and transfer function of a ΣΔ modulator

The properties that come out of the equations shows a big improvement of the previous SNR shown in equation (1). It is easy to understand the improvement of these two properties together. the combination of OSR (that moves to high frequencies the residual of the conversion) with the filter in the NTF thanks to the noise-shaping improves the SNR, as can be seen in equation (2), in the in-side-bandwidth of the converter as can be seen in Figure 2-5, where the fast Fourier transform (FFT) of a ΣΔ converter output is presented.

$$SNR=6.02*N+1.76-5.17+30*\log(OSR) \qquad (2)$$

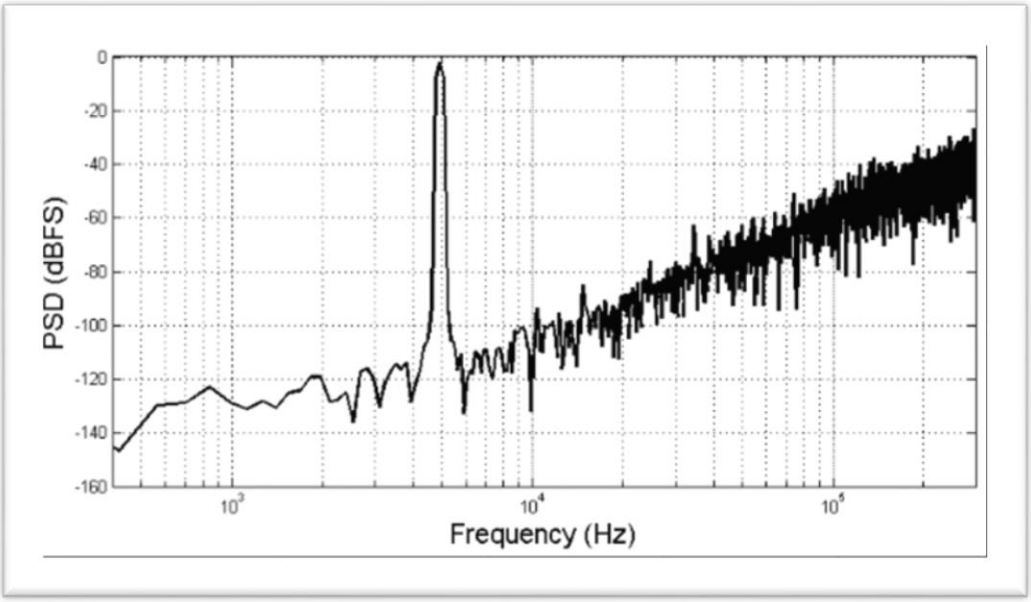

Figure 2-5 FFT of a ΣΔ modulator with noise shaping

The stability of these converters is the main drawback. Having a high order ΣΔ that can give the highest resolution of all the converter families, imply a design that needs to deal with the stability of a third, fourth or higher order loop, which is very sensitive to tolerances of the circuit. To deal with these issues, specific circuits that try to minimize the undesired effects in the loop are needed, making the ΣΔ converters more complex and with a bigger area and power consumption. In addition, classic ΣΔ normally use a Flash quantizer to maximize the resolution of the conversion, this type of quantizer is not possible to be used with low voltage supply. The same problem affects all the conversions that works in the amplitude domain. To fix the problem, single-bit ΣΔ converters have been developed in the last years to cope with a resolution equal to their old brothers. To give the same level of resolution, single-bit ΣΔ increase to loop order of the converter and the OSR. As mentioned before the loop order directly affects the stability of the conversion, and in combination with higher sampling frequency makes the design almost impossible to work under undesired effects. There is always a possibility to spend more power and area to stabilize the converter but then, the constrains of the IoT solutions push the design again. In addition to that, make all the extra circuitry to improve the stability of the converter only works for a specific

application, it means, the converter is focused on make the conversion of a specific sensors.

2.4.1.2. Integration converters

The integration converters family is well known in the SoA. It is considered a good candidate for low power converters in the low range of input bandwidth. Using simple circuitry, presented in Figure 2-6, the integration converters can cope with a good resolution. Inside the integration converters there are many different topologies. Period Modulation [36] or Current-Mode [18] are just some of the different way that this technic can be apply to converters. However, all of them have the same principle, the DS topology:

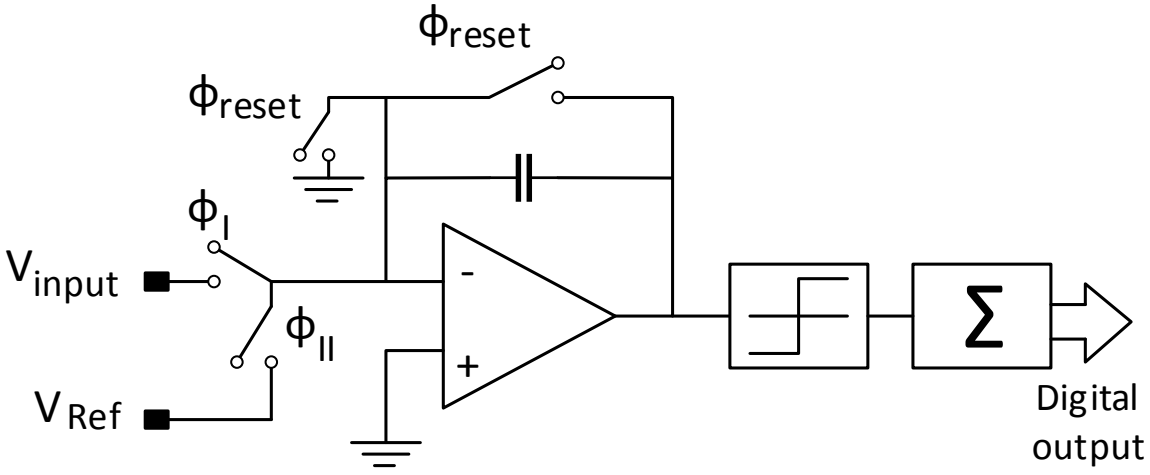

Figure 2-6 Block Diagram of Integration Converters

The behavior of this topology is simple. The conversion is based on charging a capacitor with a proportional voltage to the input value and then counts the time that takes to discharge the capacitor with a fixed current. It can be split in two phases and they are shown in Figure 2-7. In the first phase (T_I), the DS ADC integrates the input value. The voltage stored in the capacitor will be then proportional to slope $K_I = V_{IN}/(R_{in} \cdot C_{INT})$. This is only true if the input signal stays constant during T_I. To achieve this behavior the sampling frequency of the DS ADC ($Fs=1/Ts=1/(T_I + T_{II})$) is selected

much higher than the frequency of the input signal. In this way, the variation in the input signal during T_I will be negligible. This is one of the reasons why this topology fits good for low bandwidth applications. Use this solution for audio or video would lead to a clock in the DS ADC around GHz. In the second phase (T_{II}), the DS ADC is connected to the fixed current that discharges the capacitor with a constant slope ($K_2=I_{DAC}/C_{INT}$). When the capacitor is full-discharged (a zero crossing is detected), the conversion is achieved and the voltage in the integrating capacitor is reset. To obtain the digital output of the conversion the number of clock cycles of the second phase are counted. The resolution achieved in this method is proportional to the number of clock cycles needed to discharge the full-scale input signal. This feature makes the topology flexible to adapt for different resolution with the root cost of frequency speed and therefore power consumption. The resolution (LSB) and number of bits can be calculated as is shown in equation (1) and equation (2).

$$LSB = \frac{V_{FS}}{M} \tag{1}$$

$$N_{bits} = log_2(M) \tag{2}$$

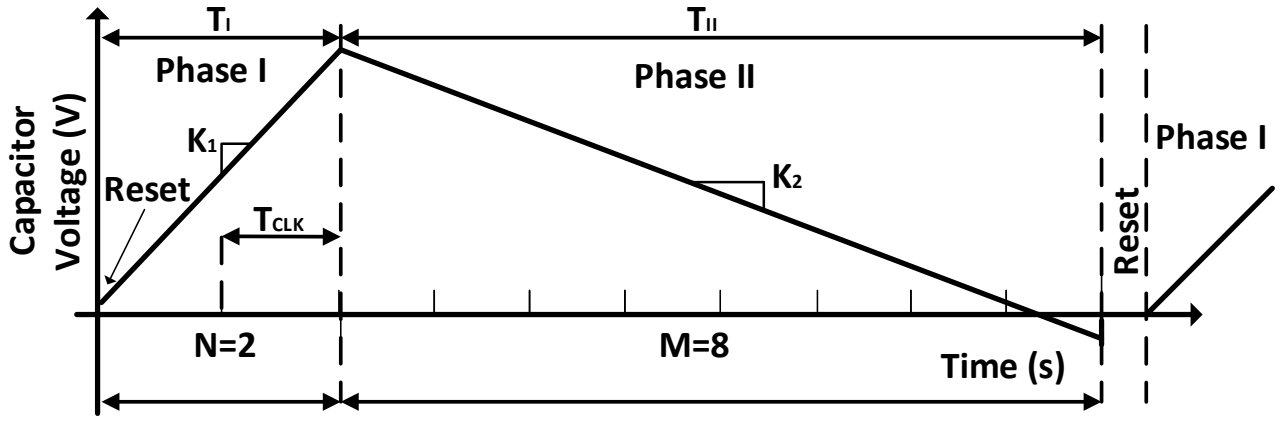

Figure 2-7 Time table of an Integration Converter (DS)

Where V_{FS} is the maximum input level and M the number of clock cycles needed for the conversion. In the example of Figure 2-7, M=8 which lead to a $N_{bits} = 3$. To increase the resolution the frequency of the clock or the measuring time have to increase.

This topology fits perfectly for the principle of continuous measurement mentioned before. The measuring time of the conversion can be escalated depending on the resolution required by adjusting K_2. However, the resolution will be limited by the measuring time constrain of the application.

2.4.2. Discontinuous Converters

In contrast with the previous converters, discontinuous converters switch off after the conversion in order to save power or just to make a reset in the design for future conversion. Making the conversion ins this way makes discontinuous converters ideal for multi input behavior. They use the switched off time of the converter to change the input to a new sensor without affecting the effective measuring time. Inside discontinuous converters there are three mainly types of architecture used in the SoA: Incremental Data Converters, SAR Converters and VCO Converters.

2.4.2.1. Incremental Data Converters (IDCs)

IDCs can be defined as the new generation for ΣΔ or at least inside the IoT world [53]. An ΣΔ IDCs is a ΣΔ ADC that is reset periodically. They use a decimation filter which is much simpler than in the classic solution, it gives the conversion result between two reset clock-edges. The intermittent operation improves the sample to sample accuracy, makes a direct impact on the efficiency of power consumption and enables a single ADC to be connected to multiple channels, eliminating the need for more ADCs for each sensor, and therefore reducing the area needed drastically. Also, the latency from the analog input to the digital output is smaller than in a classic ΣΔ converter, it is only a Nyquist conversion period. As it was mentioned before the power supply is one of the main constrains that affect the new topologies, that is why the IDCs normally use

a 1-bit comparator for the conversion. However, these converters suffer from having dead-zones around the thresholds of the quantizer, typically around zero, because of the two-level quantizer used in 1-bit circuitry due IoT constraints. In Figure 2-8 a diagram block of a typical ΣΔ IDCs is presented. The Digital Signal Processing (DSP) is used to correct the gain and offset error of the ΣΔ ADC. As explained before it is a ΣΔ converter with the modifications needed to be efficient in IoT applications.

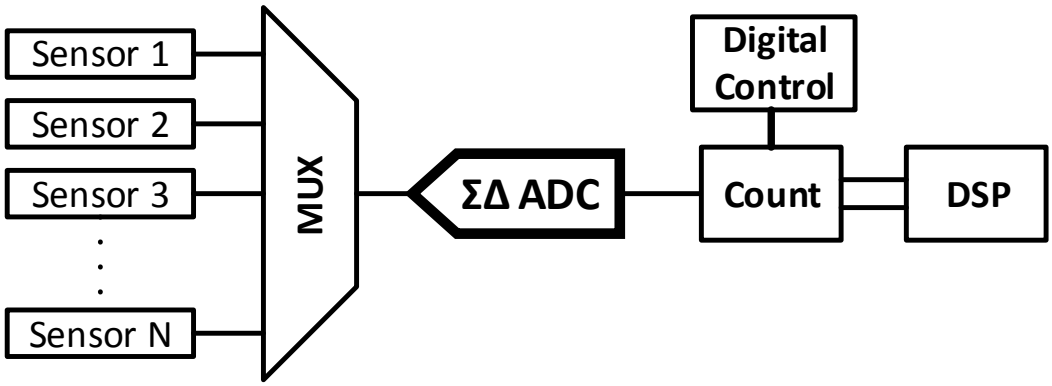

Figure 2-8 Block diagram of a ΣΔ IDC

The main improvements of these kind of converters are: the direct reduction of power compared with classic ΣΔ due uncontinuous conversions, the flexibility to deal with different sensor outputs, the reduction in area of the application thanks to the two previous characteristics. Only on ADC is needed in the solution.

However, these modifications have some drawbacks. Compared with classic ΣΔ converters there is a degradation of performance due to the ability to multiplex between different inputs. Normally, due the reset pulse of each conversion the length of the impulse respond is limited, and it affects the SQNR. In addition, ΣΔ IDCs still have some of the issues of classic ΣΔ converters. ΣΔ IDCs are implemented using 1-bit circuitry in the modulator to deal with source voltage issues. Because of that high frequencies and high loop orders are needed, increasing the risk of stability.

There are many different lines of investigation to trying to fix the issues mentioned before. One of the most used is the MASH IDCs [53]. MASH topologies are

a well-known architecture that has been used in ΣΔ ADCs for a long time. The MASH architecture, also called cascade ADC, uses different low order modulator loops (1st or 2nd order) in cascade to increase the order of noise-shaping without increase the order of the loop (and therefore the instability). Also, the use of the cascade topology improves the energy efficiency. This is because less peripheral circuits are needed (simpler DACs and quantizers). However, the use of MASH converters implies an increase complexity in the digital part of the converter due the cancelation filters needed. The cancelation filters are the responsible of increase the order of noise-shaping making the perfect cancelation of the NTF of the first loop. The complexity of these filters depends on the order of each loop. Also, the opamp of the first loop needs to have a high DC gains to avoid SQNR degradation Therefore to obtain a high SNR it requires opamp DC gain similar to the one used in a ΣΔ high order loop, which is difficult to achieve in a low-voltage design without any extra circuitry that kills the energy efficiency. On the other hand, MASH IDCs have much more relaxed requirements for the opamp gain and it has a much simpler filtering in the digital part, just implemented by decimation blocks [53].

2.4.2.2. Successive Approximation Register (SAR) Converters

Successive-approximation-register (SAR) converters are used in a wide number of applications. The applications that use this topology are frequently the ones that have medium-to-high-resolution up to the range of MHz of input signal. The resolution of SAR converters is inside the range from 8 to 12 bits. One of the most attractive characteristic is their low power consumption. No amplifier is needed as it can be seen in Figure 2-9 where the main blocks of a SAR converter are presented. The analog input goes to a track and hold block and it is compared with successive level of voltage from a reference with a multi bit DAC. The output of each comparison goes to a register. At the end of the conversion the output of all the register makes the digital vale of the input.

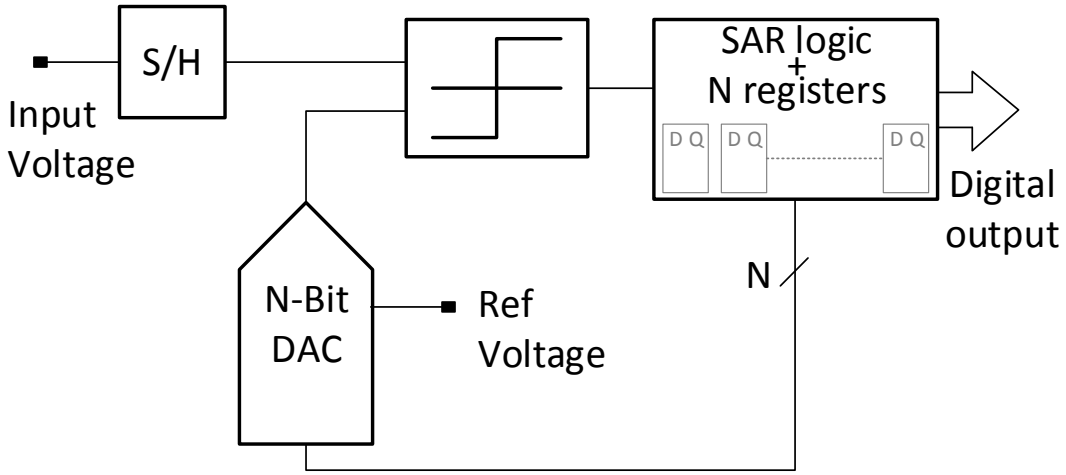

Figure 2-9 Block diagram of a SAR converter

The evolution of the conversion is presented in Figure 2-10. As it was said before, successive comparations are done between the tracked input and the levels of reference. The amount levels of reference voltage are directly related with the resolution of the conversion. For example, a 12 bits SAR converter will create 12 levels of reference with a 12 bits DAC. Therefore, the limitation of resolution is directly dependent on the CMOS technology and the voltage supply. In the market of IoT, where the applications work with low voltage technologies, SAR converters are a good candidate for applications that doesn´t need much resolution and need to have a fast conversion time or a very low power consumption.

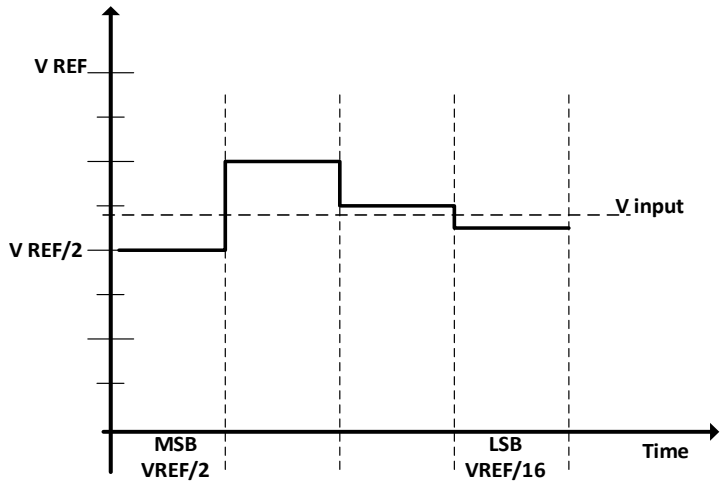

Figure 2-10 Time table of a SAR conversion with 4 bits

2.4.2.3. Voltage Controlled Oscillator Converters

VCO Converters base they behavior in taking an analog input and transform it into the phase domain with a frequency proportional to the amplitude level of the input. The block schematic of the converter is shown in FIG. The oscillator will produce X number of transitions in the inverters of the chain between two periods of the system clock. The number of transitions is measured with a phase detector per inverter output (N in the example of Figure 2-11) and after the decimation of all the samples the digital number is obtained. This architecture has the property of being able to perform noise-shaping in the output without any feedback loop in the topology. This is possible thanks to the digital logic that creates the digital output. The outputs of the inverters of the oscillator have no reset between different samples of the converter. This means that the phase of each output stays constant between the end of one sample and the beginning of the next one. In other words, the phase error of the output *n*, is present in the output *n+1*. This property plus the no need of analog circuitry in the converter, gives the VCOs a very good relation between resolution and power consumption and area. Because of that, VCOs ADCs have grown significantly in the last years. The evolution of the CMOS technology into low voltage supply is normally a problem for many architectures of converters. On the other hand, for VCOs, this change plays as an ally. With the new CMOS technologies, the transition speed of the transistors has increase and therefore the frequency of oscillation can reach higher levels before modulation problems [54].

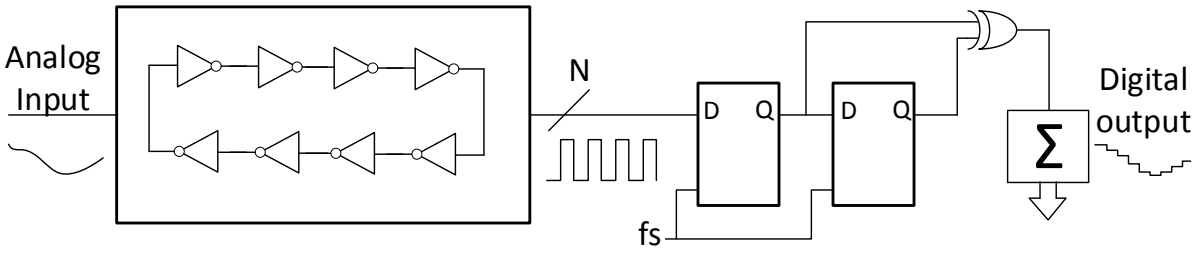

Figure 2-11 Block diagram of a VCO converter

However, there are some non-idealities that affect the VCOs:

- Sampling Clock jitter: VCO make the quantization in the time domain, therefor they use a fix amount of time as a reference, the sampling clock. Taking this into account, the jitter of this clock will produce a distortion in the results obtained. The sampling clock is not only used to start the conversion, it also gives the period of time of integration. Therefore, this non-ideality introduces two sources of error. The first one is the absolute jitter. It is produced because of the delta of time between the starting theoretical time and the rising edge of the system clock. This is common in any kind of ADCs and the effect doesn´t differ from them. However, the change of integration period of time has a direct impact in the output, it can be seen as a change in the full-scale reference of the system, introducing a big distortion in data. To reduce this effect, the free running frequency of the VCO should be reduced. In this way the relative time that is added or subtracted in each measurement by the jitter is reduced.
- VCO phase Noise: This effect comes a as consequence of the oscillation frequency of the VCO. Ideally, the spectrum of a VCO is like a sine wave. And ideal tone at the frequency of oscillation and white noise in the rest of the bandwidth. However, the non-ideal behavior of the electronics (thermal and flicker noise) produce a modification in the oscillation frequency. In the spectrum can be seen as two slopes around the tone. Due aliasing effect, these tones moves into low frequency domain, increasing the noise floor with a 10 dB/dec behavior. To deal with this effect, the designer needs to apply some techniques to reduce the thermal and flicker noise inside the oscillator, and therefore the effect due aliasing in the in-band-noise.
- Nonlinearity of VCO: VCO has nonlinearity in its tuning curve. Therefore, harmonic peaks will appear like in voltage-based ADC with nonlinearity problems. There is no much to do with these sources of noise. It is one of the main constrains that VCOs have.

Inside the IoT market, VCO converters can be a good candidate. They have good numbers in area and power consumption. Basically, thanks to the digital blocks used. No power-hungry blocks are needed like amplifiers. Also, the scalability of this architecture is excellent. Just by digital tune it can change input bandwidth or its resolution. However, it will have a limit in resolution due the non-idealities mentioned before, especially in low bandwidth applications, were the oscillation frequency will be smaller and therefore the phase noise will dominate.

2.4.3. SoA Analysis

The topologies presented in this section are the most used in applications for the market of IoT. The market is demanding solutions that can give high resolution data, normally, in the low-middle range of bandwidth. Also, the devices will try to measure all the possible environmental information. Therefore, IoT demand converters that can be connected to different kind of sensors. Also, the power consumption and area of the converter is an important constrain for application that will be inside small devices.

It is quite difficult to find a solution that works good in all the previous aspects. All the topologies described have their strength and weakness. Table I present a summary of all the main parameters need to be taken into account and all the topologies presented. ΣΔ converters are able to give the highest resolution of all the converters in a wide range of input bandwidth, but this is achievable by architectures that uses power hungry blocks working at high frequencies. Also, ΣΔ converters work in the amplitude domain. To give high resolution (N bits), a high voltage supply is needed in the quantizer to be able to create the N levels in the comparators. All these characteristics leads to a high area of silicon to perform the converter. Integration converters use one-bit circuitry and makes the conversion in the time domain, that is why they have a good power consumption that is scalable with low voltage technologies.

Table 1 Comparative between Converters topology and their properties

Properties / Converter	Resolution	Power Consumption	Voltage Supply	Area	Speed
ΣΔ	Very high	Very high	high	high	fast
Integration	medium	small	small	high	slow
IDC	high	medium	high	medium	fast
VCO	low	very small	very small	small	fast
SAR	medium	small	high	medium	medium

However, the resolution is limited to the measuring time for each application because of the low speed of the architecture, not being able to give as much resolution as other solutions. The area is not as big as in ΣΔ converters, but they also use some active components that are large in area compared with digital blocks. IDCs reduce the power consumption of ΣΔ by reducing also the resolution. In addition, thanks to the possibility to be attached different inputs by a multiplexer, the average area and power are improved. However, IDCs also make the conversion in analog domain, having the same kind of problem with the source of voltage. VCO have the lowest power consumption of all the architectures presented (working in the low range of input frequency). The digital blocks of the architecture have low power consumption, don´t need a high source of voltage (in fact they work better with low small technologies thanks to the increase in speed in the transitions of the transistors) and have a small area in silicon. Also, the can work with higher input signal frequency (by increasing also the power consumption). However, due the linearity issues the resolution is limited. SAR converters are very power efficient, avoiding any power-hungry block in the conversion and having a low duty time of conversion per period. As all the other converters that work in the amplitude domain they are directly affected with by the low supply voltage

technologies. Having also a limitation in resolution because of this problem. The area in silicon is also good compare with some architectures, but not as good as in VCOs. The same happens with the speed of conversion.

Considering the scenario presented, there is no a clear solution. All of them have their pros and cons. That is the reason why a new kind of converters is demanded. A topology that can put together the benefits of the different solution already presented will give the market of IoT a flexible solution that will be able to work in more types of applications at the same time. The name that they received is Hybrid Converters. Many different lines of investigation are trying to mix the benefits of low power solution mixed with high resolution (ΣΔ properties). Some of them are trying to replace the quantizer inside a ΣΔ or an IDC by a low power converter (in amplitude or time domain) and others are using techniques to obtain noise-shaping in Nyquist topologies.

As an example, [55] presents a topology where IDC and SAR architecture are mixed. A second order topology is achieved by an IDC using zero-crossing detectors (ZCD) instead of classic OTA to save power and an energy-efficient noise-shaping SAR as a quantizer inside the IDC. Results show a resolution of 16 bits with a power consumption of 0.24 μW.

Similar effect is also achievable in time domain. [41] presents an ADC of third order built just by digital blocks. It is just a combination of VCO and digital blocks. By the combination of them a continuous time sigma delta of third order is achieved. The problem of distortion inside the VCO is solved by digital calibration of the architecture. Pushing this effect below the noise level. The results show a very efficient in power ADC for an input frequency in the ranges of MHz. However, the application differs from the IoT. Theoretically, due its digital architecture; resolution, power and input bandwidth can be escalated to IoT requirements. It could be a good solution if the linearity problem and phase noise are still below quantization noise at low frequencies.

2.5. Conclusion

After all the topologies presented in the SoA and their characteristics, pros and cons there are some conclusions that come out to select a topology for our application.

- Conversion in the time domain. Working in the new CMOS technologies for low power consumption affects directly the level of the power supply. This change in the specifications directly affects all the topologies that makes the conversion in the amplitude domain. Therefore, conversion in the time domain is mandatory for us in order to keep the efficiency of the topology when the new technologies that have to come to the market of IoT.
- Perform Noise shaping. In Table 1, the converters that are able to achieve high resolutions with the requirements of the IoT applications are architectures that are able to perform noise-shaping. This property affects directly the resolution by reducing the power of noise in the input bandwidth. The architecture that we want to implement need to include this feature.
- Use one-bit circuitry. It is needed that the applications are robust. They need to be independent from process, voltage and temperature (PVT) variations as much as possible. One-bit circuitry is less sensitive to these tolerances. Also, the design need to be as small as possible. One-bit circuitry save a lot of space compared with multibit solutions.

Considering all these conclusions and looking at the table there are only two possible candidate topologies of converter that can satisfy the requirements. DS (Integration Converters) is selected as the topology that can be optimized in a hybrid topology thanks to low power consumption, robustness and room of improvement in the time of conversion.

Chapter 3.

CDC with a Self-Compensated Dual Slope

There are multiple possible approaches to create a front-end circuit that take the values out of the capacitors from the MEMS and give a stable signal as an input for the digital conversion. This is the first concern of the study, find a solution that is able to take the data out of the input capacitors with enough resolution and using the needed techniques to reduce the noise in the process. This chapter presents the main front-ends solutions for capacitive sensors that are used and a study to select the one that fits better for our application.

To complete the CDC a converter is needed after the processed input. As it was mentioned in the previous chapter, the study performed to analyse the State-of-the-Art (SoA) give the conclusions of what type of architecture we wanted to study and develop. Thinking into future applications, conversion in the time domain looks more feasible considering the supply voltage that new CMOS technologies are using. Make a design that base the performances in a technic that depends directly in this variable will reduce the room of use of our application. In addition, the use of one-bit circuitry goes in the

direction of the constrain already mentioned plus a reduction in power consumption and an improve in linearity. To conclude, he level of resolution, which is one of the main concerns in the applications that we target in this design is only achievable using techniques from ΣΔ converters as noise-shaping. Therefore, an evolution in Classic Dual Slope is needed. This is also presented in this chapter with the topology that has been developed for this application, the Self-Compensated DS.

3.1. Front-end topology

The main goal in the front-end design is to give an input to the ADC that has a Signal-to-Noise Ratio (SNR) high enough to doesn´t affect the conversion. The key challenge in the design of a buffer inside a front-end circuit for a capacitive MEMS is that it needs to be connected to a high impedance read-out node, and there for it is susceptible of EMC. The overall CDC performance is affected by the technology, the read-out topology and the packaging. Considering these variables and the possible constrains the main topologies are studied

3.1.1. Continuous time with AC-bridge and Voltage Amplifier

For an AC-Bridge configuration, a bridge with sensor and reference capacitor is formed, driven by two equal AC signals with 180 º phase difference. In Figure 3-1 a simplification of the circuitry in single ended is presented. The output voltage of the bridge will be proportional to the ΔC between C_s and C_r. The amplitude of the signal after the demodulator is given by (3).

$$V_{OUT} = V_{EX} \cdot \frac{C_s - C_r}{2 \cdot C_s + C_p} \cdot A_G \qquad (3)$$

Where A_G is the gain of the amplifier. There are some factors that need to be considered to increase the resolution of this method. The frequency of the digital signal will help to reduce the 1/f noise in this stage of the CDC. The frequency should be beyond the 1/f corner of the amplifier. The amplitude of the digital signal will help to

improve the minimum ΔC detectable. However, the power voltage is low for these applications, there is no a big room of improvement in this case. Finally, the parasitic capacitance will be the other factor that can improve the resolution. It is needed that this value is reduced as much as possible, taking into account all the variable that can affect it: design, layout and packaging. However, as it is mentioned in [56] the resolution of this approach is directly dependent on the thermal noise of the signal (V_{rms}). Considering that the sensor output bandwidth plus the modulation frequency is smaller than the GBW of the amplifier, the resolution can be determined by:

$$\Delta C_{min} = \frac{2 \cdot C_s + C_p}{V_{EX}} \cdot V_{rms} \cdot \sqrt{BW} \tag{4}$$

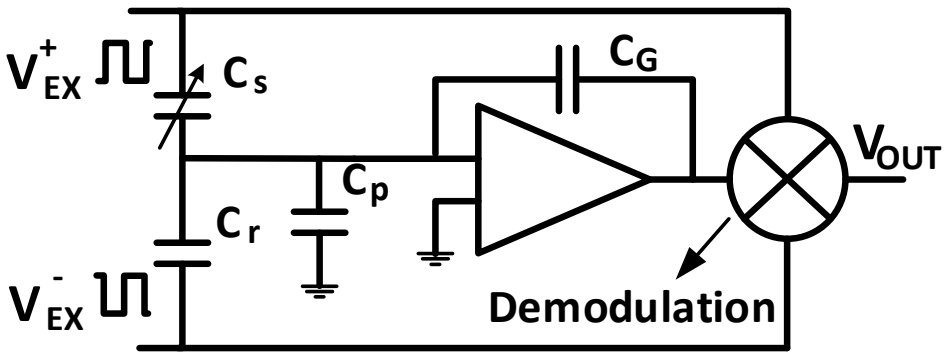

Figure 3-1 AC-Bridge Schematic

3.1.2. Continuous time Transimpedance Amplifier

For a transimpedance Amplifier configuration, a bridge with sensor and reference capacitor is formed, driven by two equal sinewave signals with 180 º phase difference. In Figure 3-2 a simplification of the circuitry in single ended is presented. In this case the bridge output current goes through a feedback resistance (R_{fb}). The driving signal have been selected sinusoidal to reduce the distortion. This will imply a reduction in the amplitude of the driving signals due to circuitry constrains in monolithic solutions [56]. However, the resolution will not be affected in topologies where the sensors have a different power supply than the front-end circuitry. In the case of a transimpedance

transfer function, the amplitude of the output will be dependent on the frequency of V_{EX} and the value of R_{fb}. Assuming that frequency of V_{EX} is smaller than the bandwidth of the front-end circuitry, the output would be considered like in equation (5):

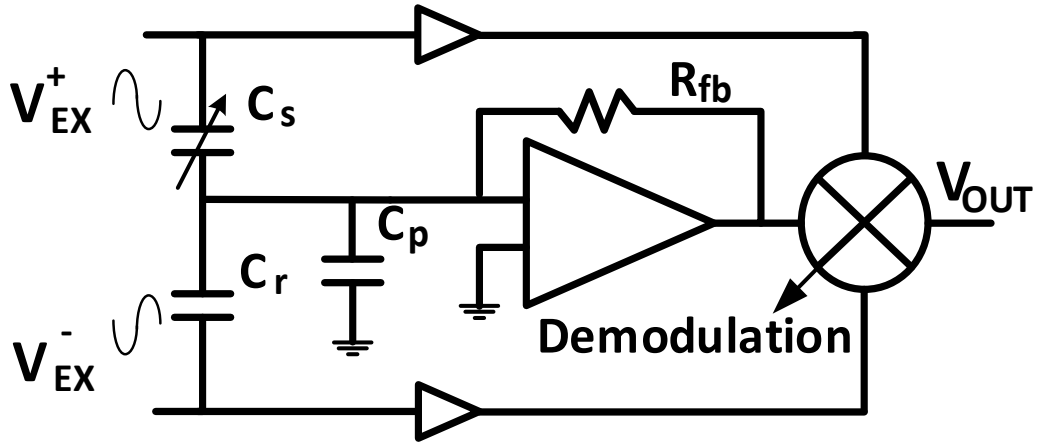

Figure 3-2 Transimpedance amplifier configuration Schematic

$$V_{OUT} = 2 \cdot \pi \cdot f_{V_{EX}} \cdot V_{EX_P} \cdot \Delta C \cdot R_{fb} \tag{5}$$

However, due transimpedance configuration, the pole associated with $R_{fb,}$ limits the bandwidth ($f_c=1/(2\pi CR_{fb})$), On the other hand, the dominant pole of the amplifier generates and inductive effect with a potential resonance that leads to a larger bandwidth. In transimpedance topologies, the output voltage is dependent on the frequency of the application. For this configuration, the resonance helps to increase the resolution of the topology, because the maximum output voltage is obtained at the resonance frequency, represented in equation (6):

$$f_{resonance} = \sqrt{\frac{GBW_{amp}}{2 \cdot \pi \cdot R_{fb} \cdot (2C_s + C_p)}} \tag{6}$$

With GBW_{amp} the gain bandwidth of the amplifier. In this kind of configuration, the noise floor is directly dependent on the thermal noise of R_{fb}. Normally the amplifier is designed with lower noise. However, in this case the noise floor, and therefore the minimum detectable capacitance, presented in equation (7), is independent of R_{fb}.

$$\Delta C_{min} = \sqrt{\frac{2 \cdot k_b T(2C_s + C_p)}{\pi GBW_{amp}}} \cdot \frac{\sqrt{BW}}{V_{EX}} \quad (7)$$

3.1.3. Correlated Double Sampling Switched-capacitor topology

In Switched-capacitor (SC) topologies for sensing, the bridge of capacitors is connected to two square signals generator with a delay in phase of 180 º (like in ac-bridge configuration). The schematic of this configuration can be seen in Figure 4.3. A proportional charge of the difference between the two capacitors is integrated in the feedback capacitor C_{fb}. As it can be seen in equation (8)

$$V_{OUT} = V_{EX} \cdot \frac{C_s - C_r}{C_{fb}} \quad (8)$$

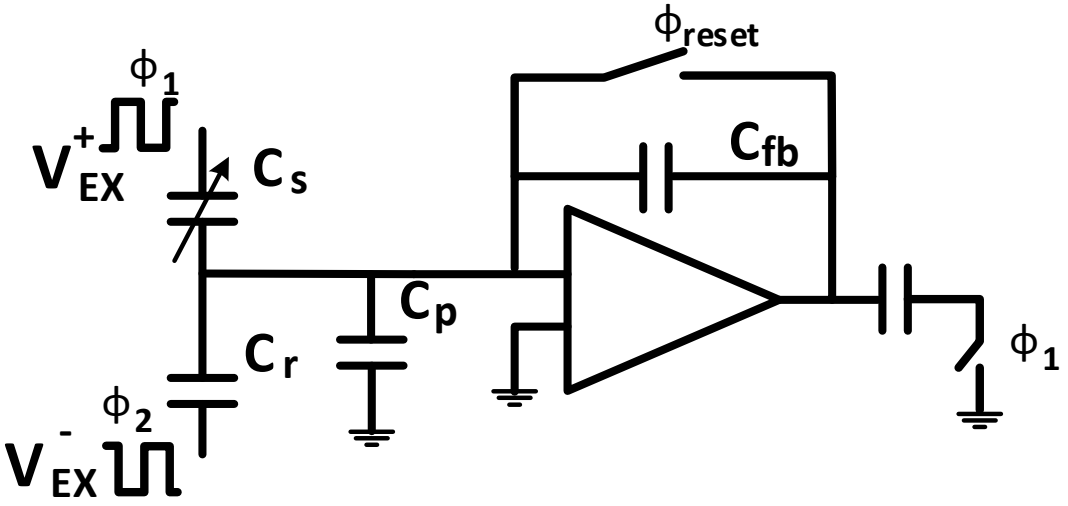

Figure 3-3 Correlated Double Sampling Switched-capacitor Schematic

The 1/f noise of the amplifier can be cancelled with Correlate Double Sampling (CDS). The thermal noise (kT/C) will be the dominant for this configuration, taken into account that C_{fb} is selected small to increase the output value. The noise contribution from the input stage can be cancelled with a proper topology, making the contribution of C_s and C_r equal. The kT/C_{fb} can be reduced by sampling and deducting it from the output [56].

Taking into account all the reduction of the noise contribution due the CDS topology, the minimum detectable capacitance of this configuration would be calculated by equation (9):

$$\Delta C_{min} = \sqrt{\frac{1}{f_s}} \cdot \sqrt{\frac{16 \cdot K_b T (2C_s + C_p) C_{fb}}{C_o}} \cdot \sqrt{BW} \qquad (9)$$

3.1.4. Comparison between topologies

To select a proper topology as a Front-end circuitry for the CDC, a comparison between the candidates have been implemented. The ΔC_{min} has been selected as the parameter to make the comparison. Some variables in the previous equations are fixed to their typical values for IoT applications.

V_{EX} is selected to maximum possible value (V_{EX} = 1.5 V). The bandwidth selected is the same for all the topologies because it is the same sensor, BW= 80 kHz. In the CDS topology C_{fb}= 500fF and C_o= 15 pF have been selected for this application Taking into account these previous equations, the resolution of all the topologies have a parameter in common, the parasitic capacitance (C_p). Also, different parameters depending on the architecture. V_{rms} in AC-Bridge, GBW_{Amp} in Transconductance and f_s in SC CDS solution. Figure 3-4 Comparison of resolution between different Front-end topologies depending on parasitic capacitance, Vrms, GBWAmp and fs. present a comparison for a range of C_p from 0 F to 9 pF. In AC-Bridge solution, two different values have been used as the V_{rms} of the signal. These values came out as the expected noise level in this stage. Considering the level of noise reached by the first topology, GBW_{Amp} and f_s have been selected to give the same level of performances. In the case of the Transconductance solution, a small improvement in the resolution is due a big increase on the GBW, making this topology inefficient in terms of power consumption. For SC CDS the resolution can be improved over the other topologies just by increasing

the f_s. However, like in Transconductance topology, the efficiency in terms of power of the CDC goes down when the clock of the system is increased dramatically.

Considering these results and the constrains in design of the CDC, the first topology has been selected for implementation. The level of resolution depends linearly on the parasitic in the output stage of the MEMS. It will be reduced as much as possible to keep the performance as good as possible

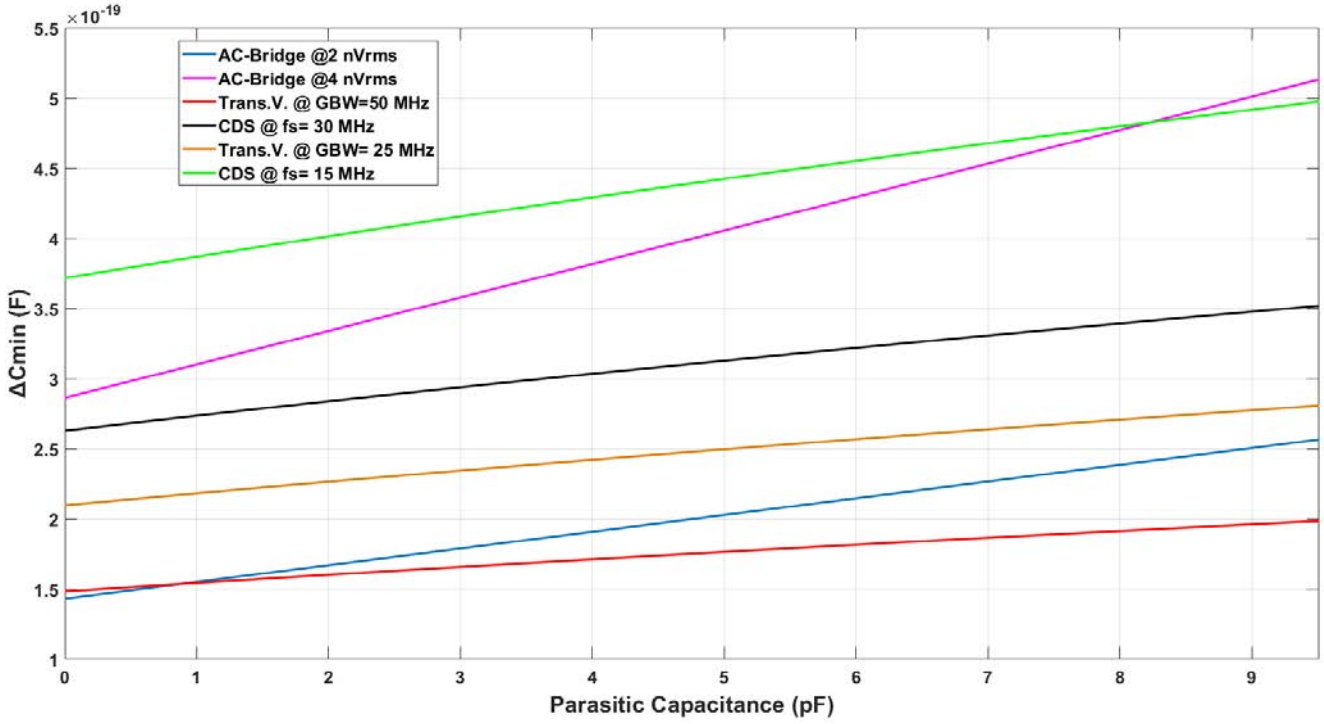

Figure 3-4 Comparison of resolution between different Front-end topologies depending on parasitic capacitance, Vrms, GBWAmp and fs.

3.2. Self-Compensated Dual Slope

As it was explained in the previous section, DS ADC is a good candidate for measuring low bandwidth input signals. A good resolution is achieved using a simple architecture based on one-bit circuitry, this feature also leads to a low power consumption. That is why the classic DS ADC has been used in instrumentation for many years. However, considering (2), to increase the resolution of the traditional DS ADC, variable M should increase exponentially. This implies that the latency of the

CDC with a Self-Compensated Dual Slope

ADC is large, or the clock for quantization is too high for high resolution as it was mentioned before. This fact makes classic DS converters not efficient enough compare with other techniques. To improve the performance, and hybrid topology has been used in the last years in [42], [43] and [44]. The topology is called noise-shaping Integrating DS. In these works, is shown that by modifying the classic DS ADC the performance for high resolution can be improved. This can be done by a slight modification of the traditional architecture. This modification is based on keeping the quantization error of each sample by the fact that the capacitor voltage at the end of each sampling period is not reset. This behavior is shown in Figure 3-5. This quantification error is kept for the next sampling period and it is integrated in the first phase of next conversion. In this way, the integration of the noise is performed, and the first order noise shaping is achieved.

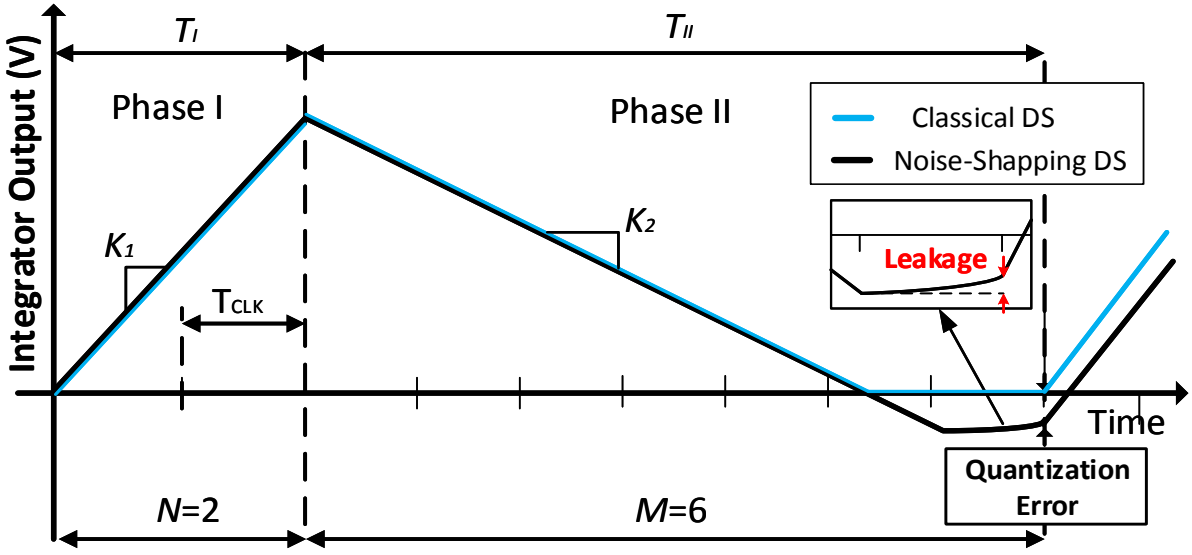

Figure 3-5 Time diagram of a Integrating DS ADC

Using this feature the high resolution can be achieved without increasing exponentially the master clock or the latency of the conversion. If the Noise-Shaping Dual-Slope converter is compared with standard ΔΣ modulators it does not require multi-bit circuits (i.e.: flash quantizers or n-bit DACs) to keep same resolution and performance, instead some single-bit analog blocks and digital logic is included in the

design to keep this residual value until the next conversion cycle. In [46] and [44] was demonstrated that the maximum Signal-to-Noise Ratio (SNR) that can be achieved using this architecture is like the one of a first order multi-bit ΔΣ modulator, presented in equation (10) :

$$SNR(dB) = 6.02 \cdot N_{bits} + 30 \cdot log(OSR) - 5.17 \qquad (10)$$

where N_{bits} is equal to (2) and OSR is the oversampling ratio between the sampling frequency and the signal bandwidth divided by 2: OSR=fs/(2·f_{BW}). According to (10), the resolution of the noise-shaping DS converter can be modified by these two variables. However, it is needed to have a fix and constant sampling frequency (f_s) to do it. To satisfy this requirement the variables of the converter must be selected in a way that the system is able to discharge completely the integrating capacitor in the second phase of the conversion (T_{II}) for all the input signal range, or what is the same, for the biggest value ($K_{1MAX}=V_{FS}/(R_{in}\cdot C_{INT})$). The relation that satisfy this condition is shown in (11), where K_2 is the ratio between the reference current and the capacitor of the integrator ($K_2= I_{ref}/C_{INT}$) and two main clocks must be defined: $f_{clk}=1/T_{clk}$ to count the discharge time, and $f_s=1/T_s$ as the frequency of the conversion.

$$K_{1\mathrm{MAX}} \cdot N \cdot T_{clk} + V_{LSB} = K_2 \cdot M \cdot T_{clk} \qquad (11)$$

According to the rate R= $f_{clk}/f_s=(M+N)$ and M=2^{Nbits}, (10) can be rewritten as in (12):

$$SNR(dB) = 6.02 \cdot \left(\frac{Log(R-N)}{Log(2)}\right) + 30 \cdot log\left(\frac{f_s}{2 \cdot f_{BW}}\right) - 5.17 \qquad (12)$$

where the resolution only depends on the frequency clocks that the system uses. However, this topology requires an extra digital block to control and keep the voltage after the zero-crossing constant until the end of the second phase, to keep the quantization error for the next sampling period. However, due to leakage in the integrator, this voltage is not always constant. In addition, the transfer function of this

topology is not linear, as it shown in Figure 3-6. The possible output digital values are in the range from -M to M. However, there are two different “0”, “0+” and “0-”. This implies a different weight for the middle value of the transfer function, and therefore a loose of linearity, which means that the Dynamic Range must be split by two to keep the linearity, it can be seen in Figure 3-6. To compensate this, an extra digital logic is needed (two different approaches has been already shown in [46] and [44]), increasing the area and power consumption of the converter. Taking in account this issue, to have a good performance in the conversion implies an extra effort in design, area and power consumption. To deal with these drawbacks of the Integrating DS ADC in a more efficient way a new topology is presented. This new proposal using a DS architecture is a contribution of this thesis. It is presented as a Self-Compensated DS architecture.

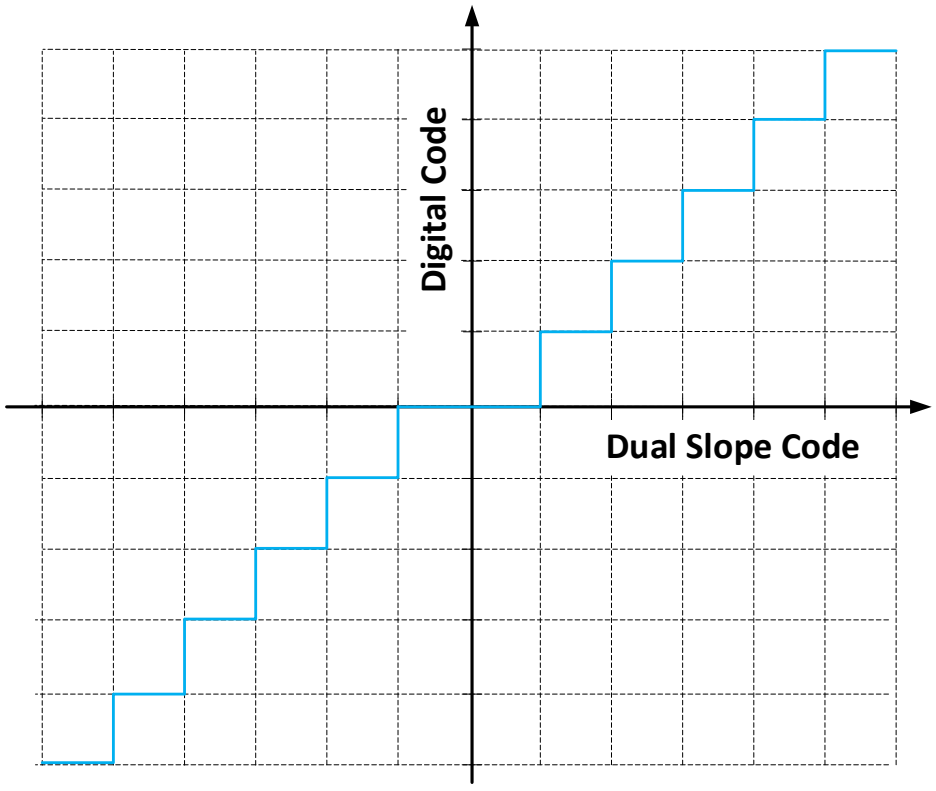

Figure 3-6 Transfer function of an Integrating DS

3.2.1. Self-Compensated implementation

The main motivation for this topology was to compensate the effect of leakage and reduce the digital control of the previous architecture. The main idea is to keep the residual value at the end of the conversion with other method that does not change the charge in the capacitor (which implies a big drop in resolution due a bad noise-shaping performance) and make the linearity compensation in a more efficient way. In this case, a solution that satisfy both problems are presented, the self-oscillation behavior. When the comparator in the DS detects a change of sign in the input (which means that the capacitor is full-discharged) the negative feedback changes the polarity in the next clock cycle to increase the charge in the capacitor again. The comparator will detect another change of sign in the capacitor and will change also the sign of the negative feedback, discharging the capacitor again. To explain this behavior, an example is presented in Figure 3-7. It is easy to demonstrate that the charge and discharge of the capacitor is equal. In this phase of the conversion the charge of the capacitor is given by a fixed current from the DAC. The value of this current is always the same, just the polarity of this current is changing. Taking in account these constraints, it can be said that after one period of oscillation (a negative and a positive charge in the capacitor), the value in the capacitor is the same as before. No leakage problem is presented, and no extra digital logic is needed to preserve the value, just an active iteration in the loop after the first discharge of the capacitor. The residual value of the capacitor is kept toggling after the zero crossing until the end of the second phase of the conversion. Some considerations need to be taken into account to prove that the performance is equal to the noise-shaping DS. As it can be seen in Figure 3-7 when the oscillations after zero-crossing give an odd number, the residual value is not equal to the one expected with the previous solution and therefore this could affect the performance of the noise-shaping modulator. The following equations shows that the residual value of the conversion is compensated in this situation and therefore the performance of this solution keeps the first order noise-shaping as the Integrating DS presented in [42], [43] [44]

CDC with a Self-Compensated Dual Slope

In equation (13) the voltage value of the capacitor after the integration (phase I) is calculated where the voltage of the input of the DS ADC is considered constant. As it was mentioned before, this can be assumed when the sampling frequency is much higher than the input frequency (f_s>>BW_{input}). The number of clock cycles need to discharge the capacitor (phase II) is calculated using equation (14). Equation (15) shows what will be the error at the end of phase II in a case where the zero-crossing gives an odd number, like in Figure 3-7. It can be seen that the quantification error is formed by the real quantification error (presented in equation (16)) and an extra component due the unbalanced oscillation (presented in equation (17)).

$$V_1[\mathrm{n}] = \frac{V_{IN}}{R_{IN} \cdot C_{INT}} \cdot N \cdot T_{clk} \; + \; \mathrm{q}[\mathrm{n}-1] \tag{13}$$

$$T_{\mathrm{DS}}[\mathrm{n}] = \mathrm{floor}\left[\frac{V_{IN} \cdot N \cdot T_{clk}}{R_{IN} \cdot I_{DAC}} + \frac{q(n-1) \cdot C_{INT}}{R_{IN} \cdot T_{clk}}\right] \; + \; 1 \tag{14}$$

$$\mathrm{q}[\mathrm{n}] = q'[\mathrm{n}] + LSB \tag{15}$$

$$q'[\mathrm{n}] = V_1[n] - \frac{I_{DAC} \cdot T_{DS}[n] \cdot T_{clk}}{C_{INT}} \tag{16}$$

:

$$LSB = \frac{I_{DAC}}{C_{INT}} \cdot \left(\frac{1 + (-1)^{M+1-T_{DS}[n]}}{2}\right) \tag{17}$$

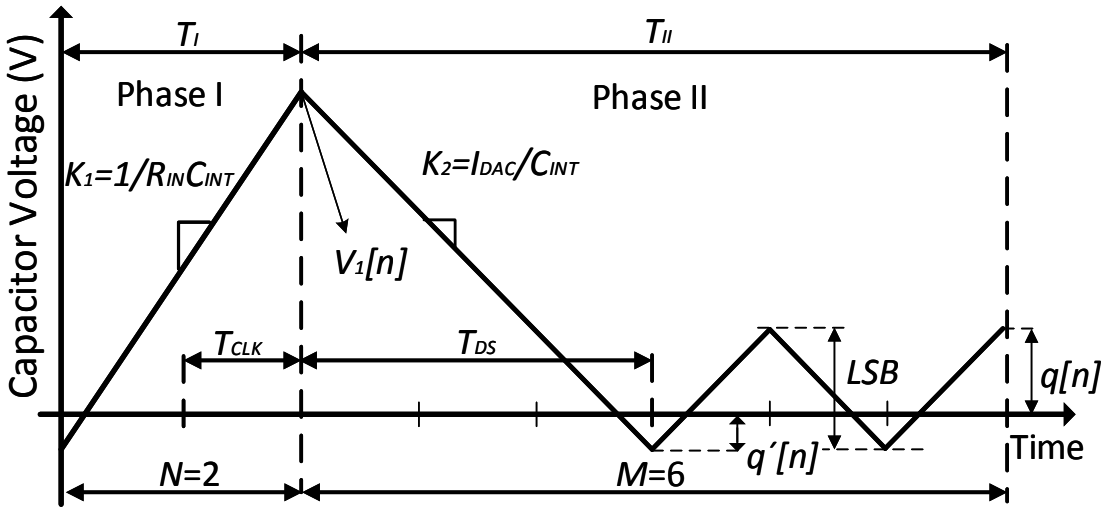

Figure 3-7 Time diagram of a Self-Compensated DS

However, it can be demonstrated that if equation (15) is used for one more iteration in (13), the system will be auto compensated and q[n+1] = q'[n+1] in (15). In addition, the digital output of this topology is between [-M, M] without any extra digital logic needed. For this topology, the digital output will be always an even number (or always an odd number) if M is an even number (or an odd number). This is because of the self-oscillation behavior. Because of that, the weight of the codes of the quantizer will be the same (two clock cycles) until the edges, and therefore the linearity problem that is presented in the middle of the transfer function in Integrating DS is solved, again, without any extra circuitry. There is one drawback that needs to be considered. Due the self-compensation effect, the weight of the number in the edges of the transfer function would divided by two as can be seen Figure 3-8. In a Self-Compensated DS, the input full-scale is taken ignoring the last period time. This feature will imply a higher gap of frequency in order to extend the number of bits in the quantization. However, having two period times for each output code improve the stability of the measurement against non-idealities of the architecture (comparator for example), relaxing the design requirements and therefore the power consumption.

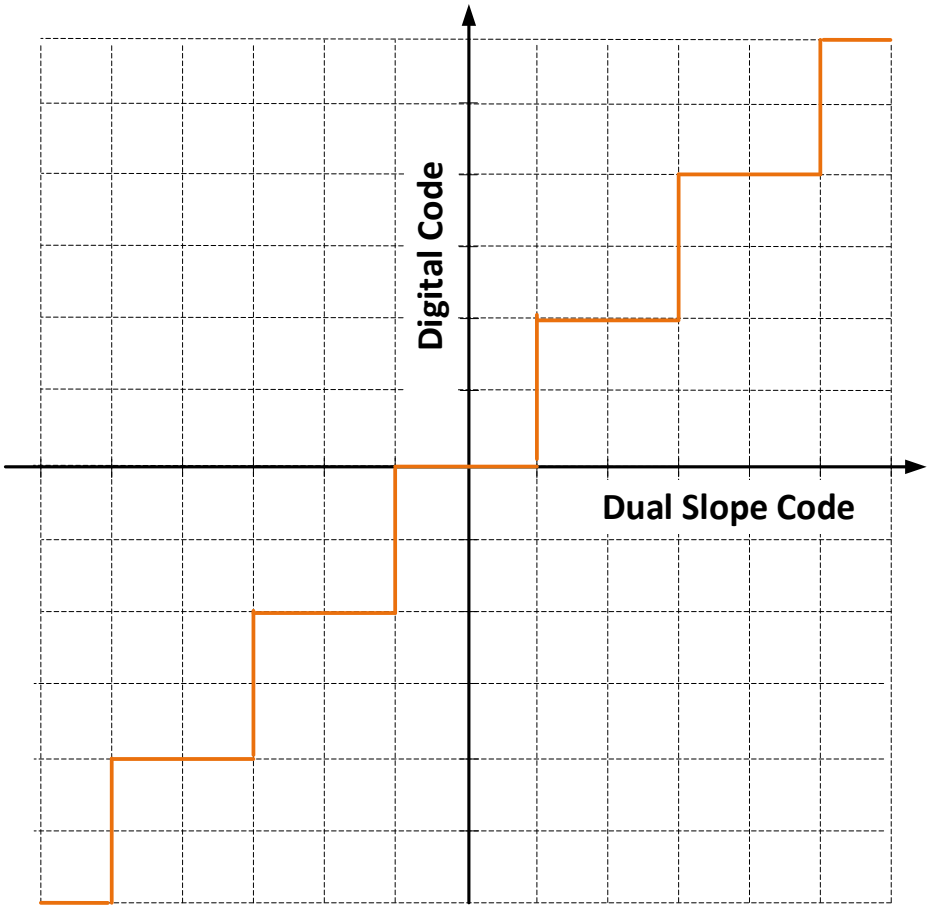

Figure 3-8 Transfer function of a Self-Compensated DS

3.3. Conclusion

The theoretical study included in this chapter has provide the information required to validate the Self-Compensated DS as a promising topology to be used inside a CDC using a continuous time AC-bridge as a front-end circuitry.

The study of the different possibilities in the acconditioning of the signal for the conversion has shown that the main contributor in the degradation of the resolution is the parasitic capacitance at the input of the circuit, or in this case, the connection between the MEMS sensor and the front-end stage. To minimize the effect and to be able to be efficient with an AC-bridge architecture, the packing of the prototype will need to be done as compact as possible. Making the distance of bonding between MEMS and CDC as short as possible.

Self-Compensated DS has proven the integrity of the signal in the previous equations. It is able to keep the noise-shaping of first order as a consequence of its transfer function with no extra digital blocks to deal with non-ideal behavior. Considering equation (12) a prototype that is able to cope with the required resolution to be competitive with the SoA will be designed.

Part II

CDC prototype using a Self-Compensated Dual Slope Converter

Chapter 4.

Continuous Time CDC for MEMS in 130-nm CMOS

In the previous chapters the concept to create a CDC using time domain with DS topology has been presented. In this chapter, the complete (CDC) topology is presented. An explanation of the type of sensor used in the topology is included with its main concerns for the integration in the CDC. The topology is explained at system level with a time table where all the signal used to control the CDC and the evolution of the conversion. After that, the details at circuit level are shown. The topologies used for the amplifiers, the programmability with passive components, the methods used to reduce the noise floor are explained in detail. Also, the architecture to keep the performances of the design, including the package of the chip, are explained in the layout section.

4.1. MEMS sensors

MEMS have a range in characteristic length from one millimetre down to one micron [57]. Is important to understand that MEMS are not machined. Instead, they are created using micro-fabrication technology similar to CMOS technology. This is

directly related with one of the advantages of this kind of sensors, the cost per unit. The way of production of this new kind of sensors is like integrated circuit industry, which means that batch fabrication can significantly reduce the costs of mass production. Also, compared with traditional sensors, the amount of material is much lower, which can further reduce cost of production. Other reason is that MEMS sensors are more applicable than the classic approach. Many new applications do not allow the use of classic sensors due the size, or power consumption. Apart of the improvement in price or viability compared with classical sensors, MEMS sensors introduce an advantage in integration. Because they are fabricated with similar process used in ASICS, MEMS sensors can be more integrated with the electronic. Even if truly monolithic solution has been proven to be difficult to achieve, many studies go in this direction, proving the efficiency of this approach

The emerging demand for high performance applications increase the interest of development of a variety of interface systems that cope the new requirements. The idea is that by combining sensory data we can compensate for the weaknesses and drawbacks of each individual sense organ and arrive at an understanding of the environment that is in some way superior. This feature is already used by some smartphone companies combining 3 axes accelerometers with 3-axes magnetometer, pressure sensor, 3-axis gyroscope, an ambient light sensor, and different combinations [58].

In the way that MEMS are made, they have mechanical moving parts and electronics. Mechanical structures represent the interface between physical world and electronics: they can sense a variation of a physical quantity or actuate. Regardless of transduction principle, a MEMS consists of a mass which is free to move in one or more direction in the 3D space with respect to the substrate, related with an alteration in the physical variable that is going to be measured. Different methods are commonly used to sense the displacement of the moving mass: capacitive, piezoresistive, optical, and resonant sensing. Capacitive readout MEMS are based on the measure of a capacitance variation due to the displacement of a suspended microscopic structure in presence of

an external applied force. Moving electrodes (also called rotors borrowing mechanical terminology) are mechanically anchored to the moving structure and fixed electrodes (as a consequence called stators) are anchored to the substrate. Figure 4-1 shows a differential capacitive sensing cell with a moving electrode anchored to a suspended shuttle (on the right) and forming a couple of capacitors with stators A and B.

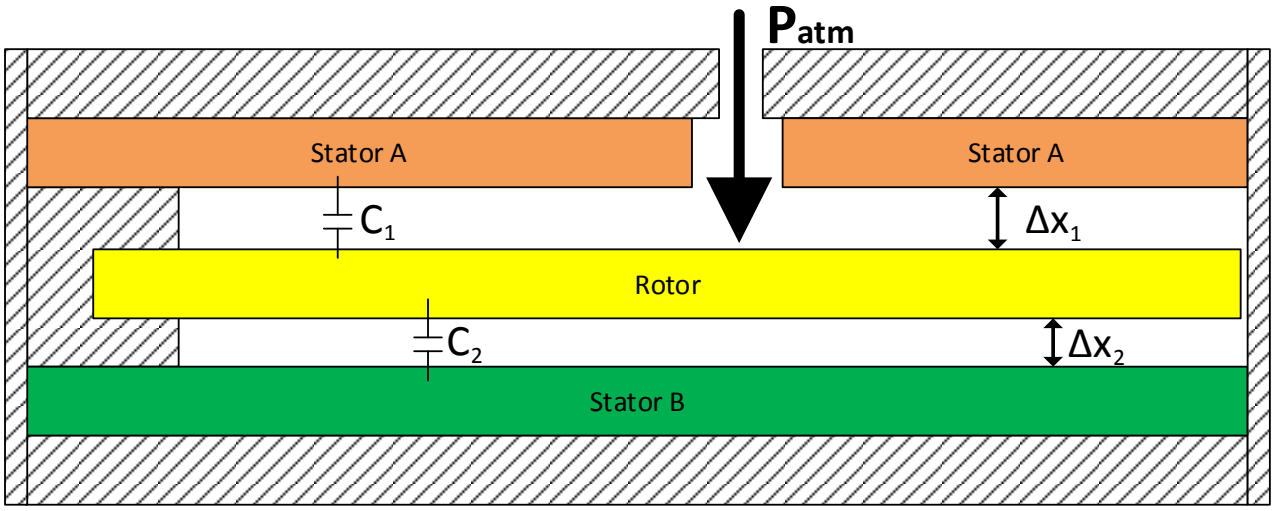

Figure 4-1 Sketch of a typical differential capacitive sensing cell for a MEMS structure. Stators A and B forcing acting on a suspended mass.

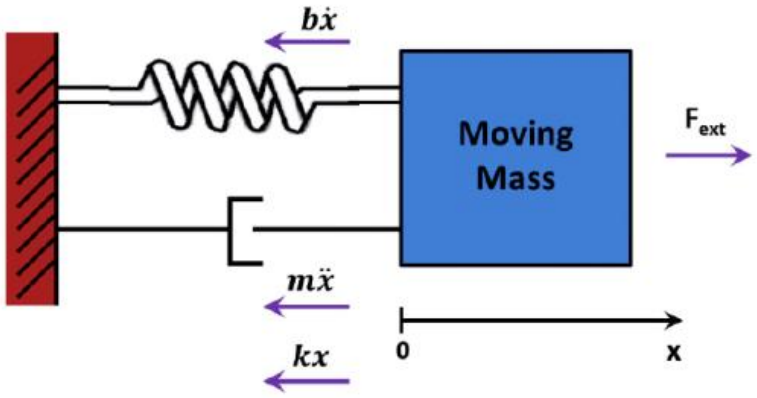

Figure 4-2 Diagram with forcing acting on a suspended mass.

A microelectromechanical system can be modelled as a lumped parameters spring-mass-damper system [59], as shown in Figure 4-2: a mass is connected via a spring to a fixed support, being pulled by an external force F_{ext}, pressure for example.

A dashpot is used to represent the mechanical damping behavior of the MEMS material. All these three elements share the same displacement x with respect to a rest position. For sake of simplicity, the example is done in one dimension, ignoring the secondary effects. Applying Newton's second law of motion, stating that the net force on a body is equal to the product of acceleration and mass of the body: F=m*a, the classical equation of motion describing the dynamics of a suspended micromachined structure can be derived:

$$m \cdot \ddot{x} + \mathrm{b} \cdot \dot{x} + \mathrm{k} \cdot \mathrm{x} = F_{\mathrm{ext}} \tag{18}$$

being the elastic force proportional to the displacement x, the viscous force to the velocity.

By applying Laplace transform to equation (18), the frequency behavior of MEMS can be studied with respect to frequency and two main parameters can be highlighted to describe the behavior of the mechanical element.

The resonance frequency is defined in equation (19):

$$F_r = m\frac{1}{2\pi} \cdot \sqrt{k/m} \tag{19}$$

A heavier moving mass resonates at lower frequency; the stiffer is the spring, the higher is the resonance frequency.

The quality factor Q, a dimensionless parameter useful to characterize how over- or under-damped a MEMS resonator is. Equivalently, for large values, Q also characterizes resonator bandwidth Δ_f relative to its center frequency f_r and it is related to MEMS parameters according to equation (20).

$$Q = \frac{1 f_r}{\Delta_f} = \frac{(\omega_r \cdot m)}{b} = \frac{\sqrt{k \cdot m}}{b} \tag{20}$$

Micromechanical devices are affected by thermal noise like all dissipative systems. In particular, dimensions scaling is attractive for a higher density integration, but small moving parts become more susceptible to mechanical noise due to molecular movement. Especially in sensors targeted for very low signals applications, mechanical noise may be a limiting factor. The power spectral density of the noise force can be written as in equation (21).

$$S_{\mathrm{Fn}} = 4 \cdot k_{\mathrm{B}} \cdot \mathrm{T} \cdot \mathrm{b} \tag{21}$$

T is the absolute temperature, k_B the Boltzmann constant and b damping coefficient previously introduced. It should not surprise that the resulting expression for mechanical noise is very similar to Johnson noise in resistors, $SVn = 4k_BTR$, as they both have the same physical origin, dissipation.

In gas damped systems, like MEMS working either at ambient pressure or in a package at a lower pressure, mechanical noise is mainly due to random paths of molecules which hit the suspended structure. The result of this statistic process is an unwanted random displacement of the moving mass which is nevertheless detected by position sense interface.

In this prototype a MEMS with two different kind of capacitors is used. The MEMS is presented in Figure 4-3. A Wheaton bridge configuration is used with the two kinds of capacitors. The capacitor called C_s has a dependency with pressure higher than the other capacitor used for reference (C_r). With a delta of pressure (and therefore in the F_{ext} mentioned before) the distance between the two plates of C_s will be reduce (the physical effect in the MEMS sensor) producing a change in the capacitance (electrical change of the MEMS sensor).

4.2. SYSTEM LEVEL

In the previous section the physical behavior of the MEMS used in the application has been explained. However, there are some effects that are going to affect the

performance of the prototype that need to be mentioned. Using a real MEMS introduce some non-idealities. One of the main ones that can affect the performance of the architecture is the resonance of the sensor. Due the physical properties of the sensor a

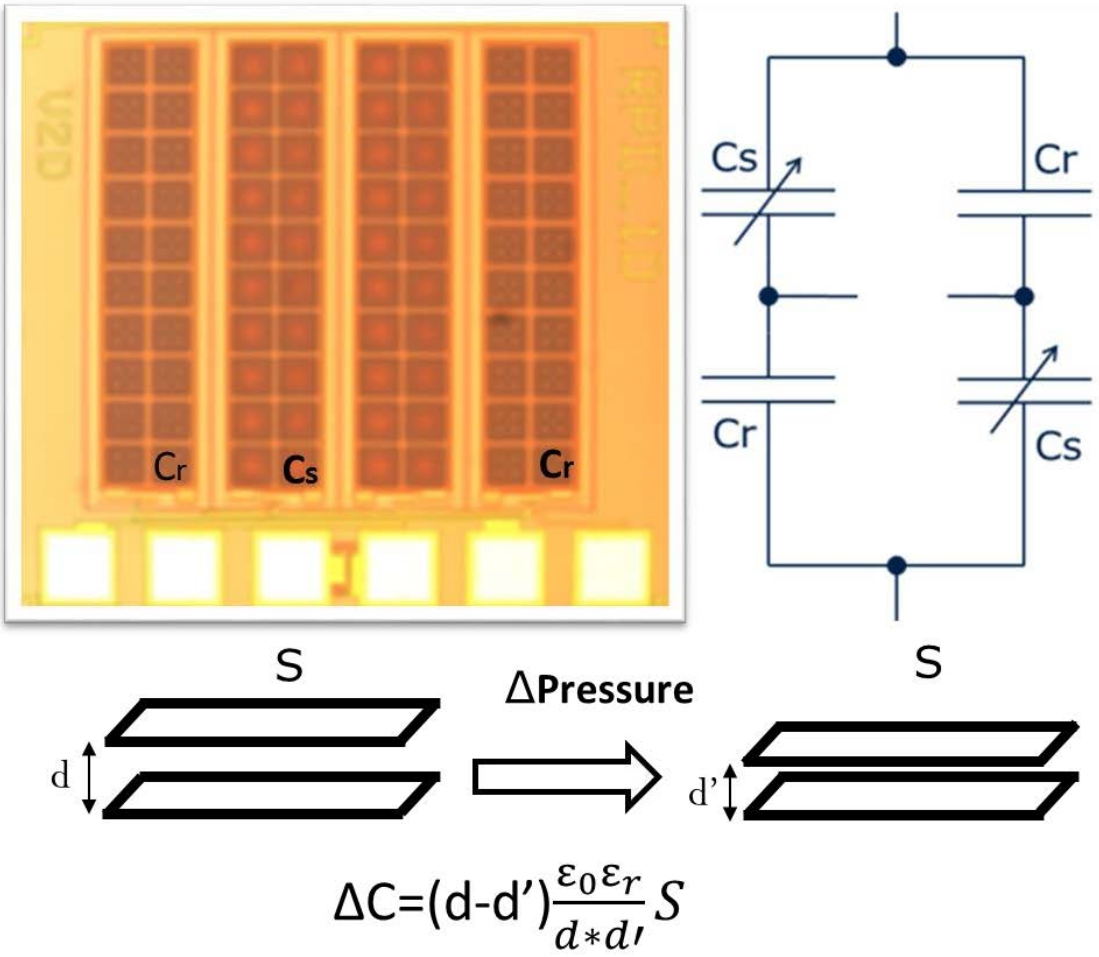

Figure 4-3 Pressure sensor MEMS used in the prototype

modulation signal is used to take the electrical information out of the capacitors. This modulation of the sensor implies a step at the input, and therefore a second order response. To obtain the desire information some adjustments are taken into account in the implementation.

The complete CDC can be seen in Figure 4-4. All the signals used in the conversion are presented. As it was mentioned before, the excitation signal of the MEMS is modulating its output to be able to use a capacitive bridge and also to remove the flicker noise out of the bandwidth of interest. Working in low frequency domain,

flicker noise will be one of the main contributors in the total noise of the application. The main technic to reduce its contribution is the modulation of the sensor to higher frequencies. In the demodulation step, the flicker noise will be translating to the high frequencies, improving the Signal-to-Noise Ratio. That is one of the main reason of using capacitive MEMS of IoT applications. V_{EX} represents the excitation signal of the MEMS bridge. Due to the response of second order of MEMS to a step input, it is shaped in a smooth square wave to reduce stimulation of high frequency of MEMS sensor and ringing in the output voltage of the bridge as it can be seen in Figure 4-6. This will lead to a signal (V_{Bridge}) at the input of the preamplifier with the same frequency of V_{EX} and an amplitude proportional to the difference between C_{sens} and C_{ref}, like it was explained in previous section. The preamplifier composed by OTA I, C_{offset} and C_{Gain} makes the reconditioning and scaling of the bridge output. After that the demodulation of the signal is implemented to have a signal that the low-bandwidth ADC is able to convert. The demodulation block is driven by V_{Ref}, which is V_{EX} after a digital buffer.

The modulation inside the MEMS and Front-end circuitry works as the chopping of the first part of the CDC, removing from the bandwidth of interest the contribution of offset error or, as it was mentioned before, flicker noise. The effect can be seen in Figure 4-5. However, the chopping frequency must be carefully chosen, it will be related with the second order response of the MEMS, therefore the frequency must be high enough to modulate flicker above the bandwidth of interest, far enough from resonance frequency from the sensor and low enough to allow the signal stabilizes after the ringing due second order system behavior.

The output of the demodulator is the input of the Self-Compensated noise-shaping DS converter (V_{IN}). As it was mentioned before, the signal is affected by the ringing of the MEMS. V_{IN} will have a stablishing time, considering the desired frequency of the chopping [60], the signal will have a stable value for a specified length of time every chopping semi-period. The connectivity between the two steps needs to be properly synchronized to have a good performance in the CDC. To meet this requirement, the

system is synchronized with signals Φ_I and Φ_{II}. These signals divide the sampling period into two phases. In Phase I the readout circuit will be connected to the ADC; this time

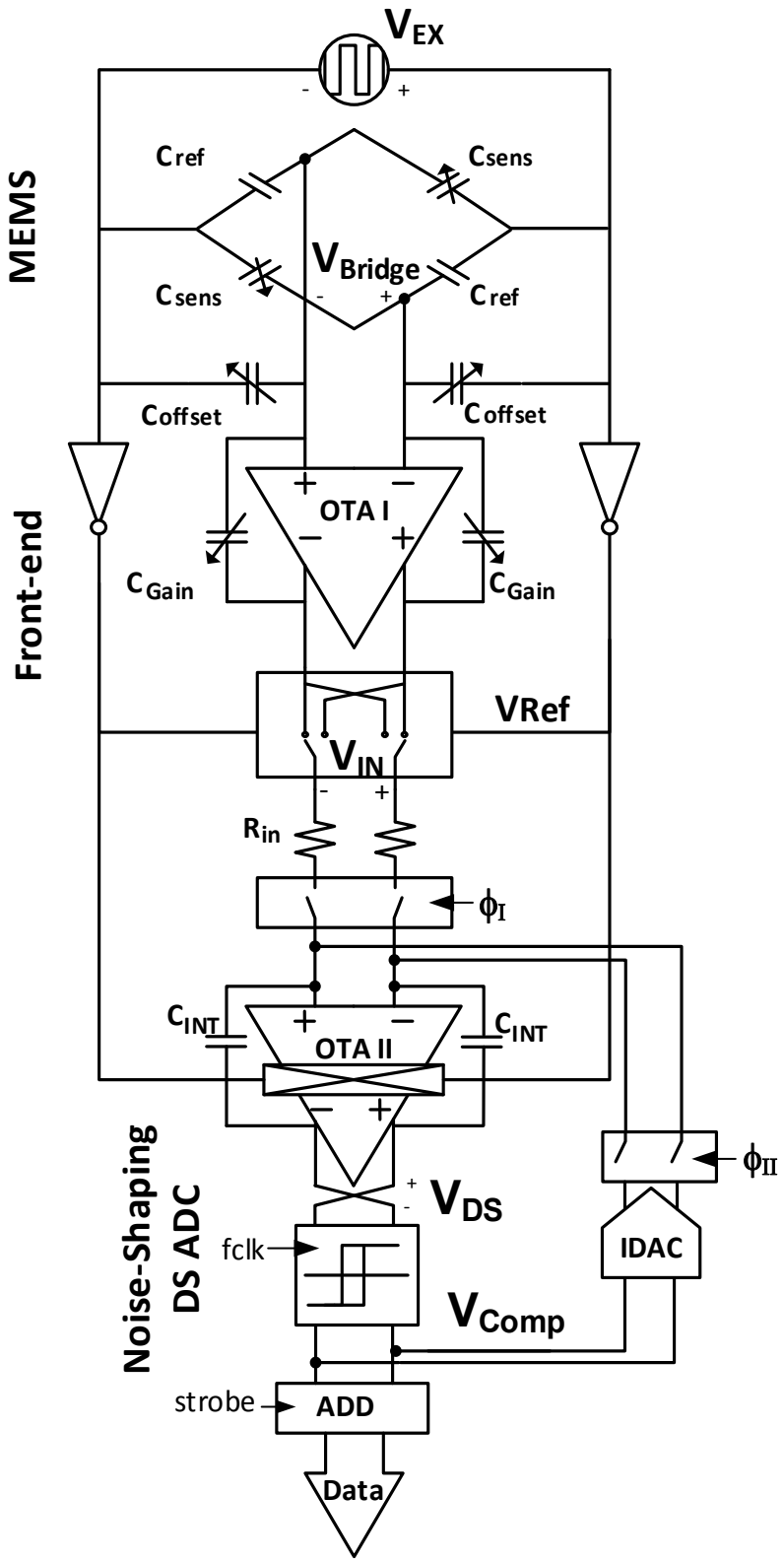

Figure 4-4 Block diagram of the proposed solution

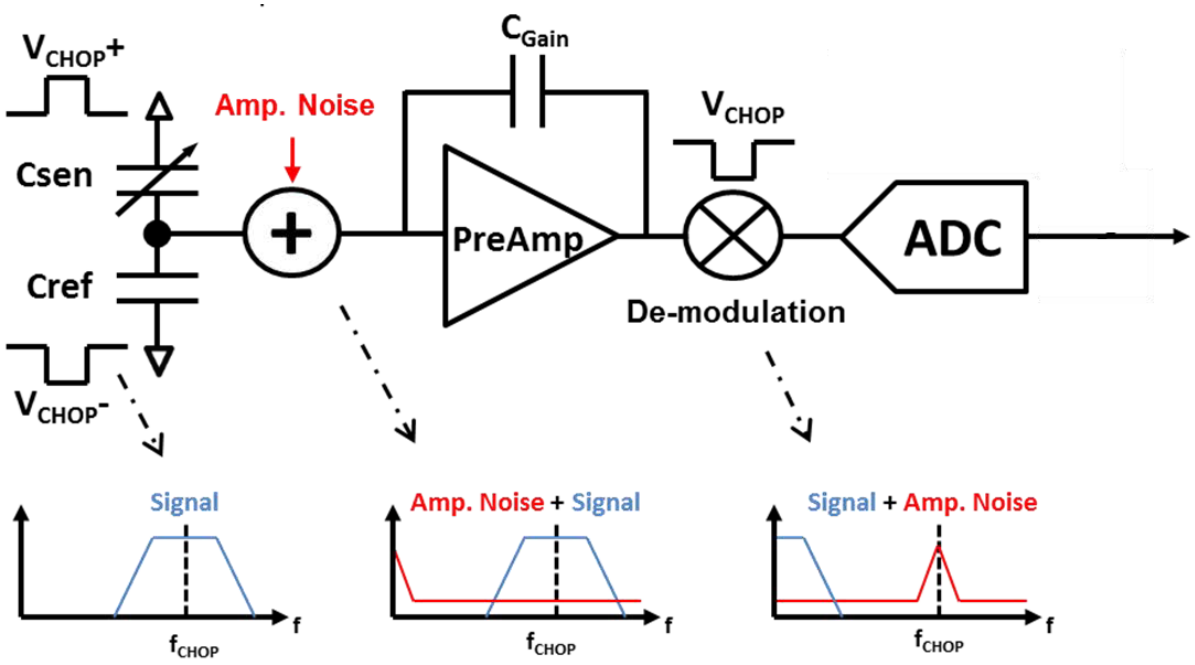

Figure 4-5 Chopping effect in front-end circuits

will be chosen when the output of the readout circuit is stable and doesn´t have a contribution from ringing noise. In this way, the Phase I of the Self-Compensated noise-shaping DS converter (Φ_I active) works as a track phase of a track and hold behavior. If the length of Phase I is larger than the length of time where VIN is stable, the ripple of the output of the Voltage amplifier will affect the output of the CDC reducing the resolution. The length of phases will be chosen taking into account simulation with the time response of the MEMS. Taking into account that the MEMS used is a product under development of a company, the detailed equations of its behavior are not shown.

The timing of phases signals Φ_I and Φ_{II} is done with non-overlapping architecture, as it can be seen in Figure 4-6 that the two signals are never at high level at the same time. This will help to avoid leak of currents and over voltage in ADC signals. Also, to achieve high resolution with the lowest clock frequencies (to reduce power consumption), these two phases of the conversion and therefore, N and M, are selected unequal. If Phase II (Φ_{II} active) is larger, M will be larger and therefore the number of bits inside the DS quantizer. N is selected equal to two clock periods, which is the minimum value for Phase I (Φ_I active) for a proper behavior of the system, giving

enough time to integrate the input signal without any ringing contribution. M is selected equal to 6. As it was mentioned before, V_{DS} is the output of the integrator of the Self-Compensated noise-shaping DS. The modulation signals and the phases of conversion are synchronized in a way that the chopping in OTA II is done at the start and end point of each conversion. With this configuration a possible distortion in the conversion due to DM rejection is minimized. Signal V_{COMP} represents the output of the clocked comparator. This signal will be used as the input of the DAC and to generate the multi-bit digital output of the CDC through the digital filter. The DAC is selected as simple as possible to minimize the circuitry. It is a 1-bit current DAC with no return to zero. The ADD block makes the logic addition of the output of the comparator generated during Phase II (high level adds a 1 and low level subtracts a 1) every falling edge of Phase II (Φ_{II}). Digital output is then proportional to the input amplitude of the Self-Compensated DS converter (V_{IN}), and therefore, to the input pressure of the CDC. In this system, the conversion rate is specified by the sampling period, which is defined as $Ts = T_I + T_{II}$, where $T_I = N \cdot Tclk$, $T_{II} = M \cdot Tclk$. and Tclk is the clock period of the comparator.

4.1. CIRCUIT LEVEL

After the explanation at system level of the CDC, the circuit levels details to achieve this performance are explained. Two main blocks are defined again for circuit design:

4.1.1. Analog front-end

The analog fronted is based on a closed loop capacitive voltage amplifier. It is composed by configurable capacitors C_{offset} and C_{Gain}, and an OTA (OTA I in Fig. 5.1) built with a Telescopic Gain-Boosted OTA to be power efficient. A simplify schematic at transistor level is shown in Figure 4-7. It can be seen that is a one stage topology with a special block for the control of the bias voltages of the cascode transistors. With a

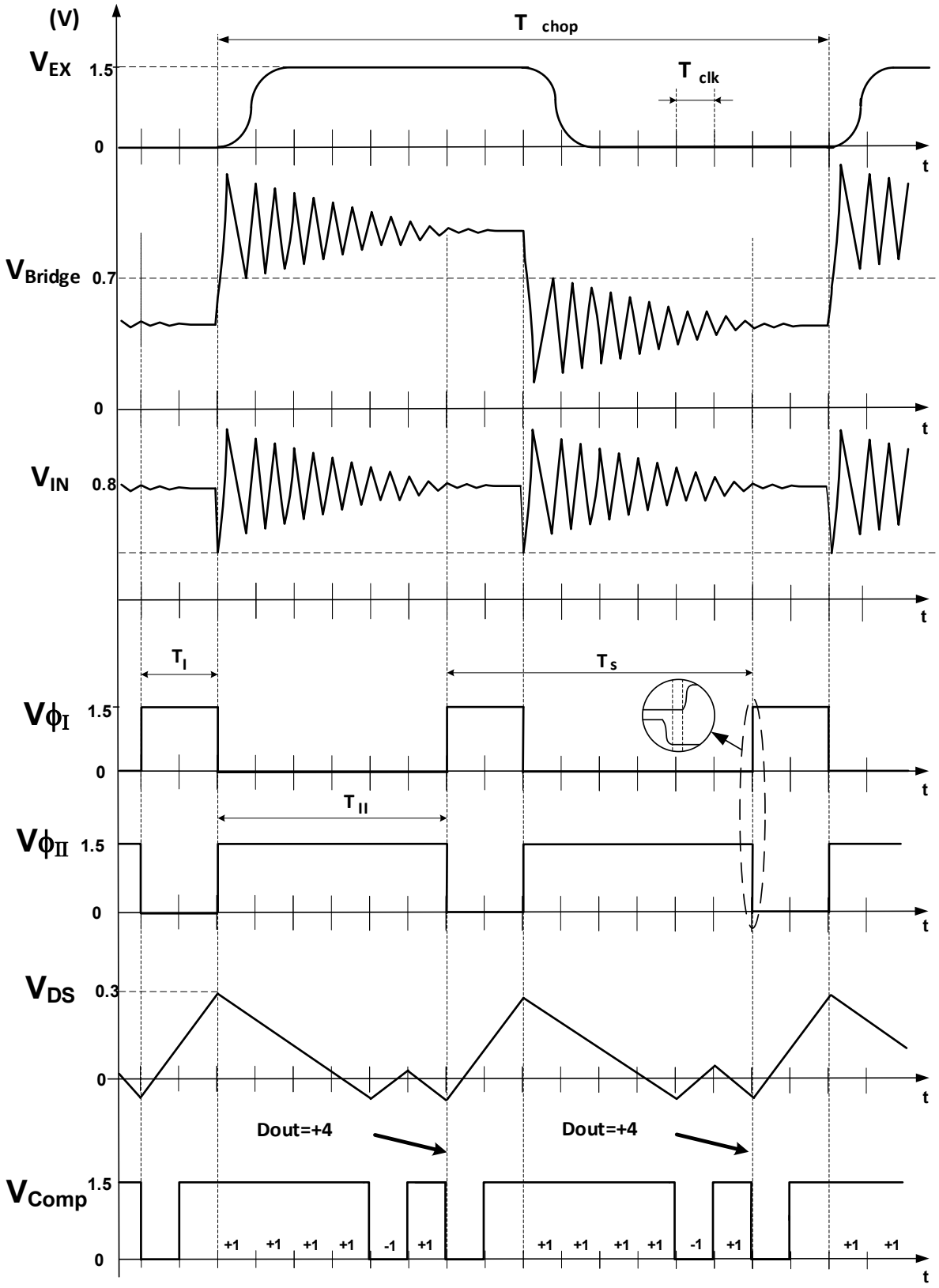

Figure 4-6 Time table of the proposed solution

precise control of bias voltages, the topology is able to give an output swing of 1 V differential. This means that the five transistors in cascade of the OTA are stacked within 1 V. The reason of using this one stage topology instead of another solution is to save power consumption. This topology saves almost half of power consumption compared with a Folded Cascode Architecture, where normally two-stage amplifier is needed. The power consumption of this OTA is 96 µA. The biasing is quite challenging due to the 1.5 V supply voltage, to keep the good performance a special biasing circuitry is designed to generate an input common-mode voltage that can track process and temperature. The output voltage is 0.5 Vpeak. This value is taken into account as the input voltage of the ADC. The OTA is designed with a DCGain= 132 dB and a GxBW = 3.46 MHz. These values were used to reduce the noise below 4 µVrms, keeping the resolution over 18 bits. This amplifier does not need any specific technique to reduce low-frequency noise as it is already chopped by the modulated/demodulated scheme proposed in this architecture.

To make a proper conversion in the whole range of the CDC is important to verify, and adjust if it is possible, the transfer function of the converter. There are some Process, Voltage and Temperature (PVT) variations that can affect the theoretical transfer function of the MEMS, and therefore the final resolution of the CDC. In addition, in sensors applications, the bonding between the sensor and the CDC always produces parasitic capacitances that affect the expected value of capacitance at the output of the bridge, and therefore, produces an offset in the transfer function. To compensate the effect of PVT variations and the parasitic capacitances the programmable capacitors C_{Gain} and C_{offset} (Figure 4-8) are included. The programmable capacitors have a unit cell of 25 fF. Figure 4-8a shows the effect of the offset compensation in the output voltage of the readout circuit. In this way, the difference between samples due to the bonding can be compensated. The range of its capacitance goes from -100 fF (the minus indicates that the capacitance is added in the other half of the bridge) to 675 fF. The other source of process variation that needs to be considered

is the gain of the system. The programmability of the CGain give a proper control of this magnitude (that affects directly the transfer function of the CDC) and its effect can be seen in Figure 4-8b. The range its capacitance goes from 275 fF to 1.525 pF.

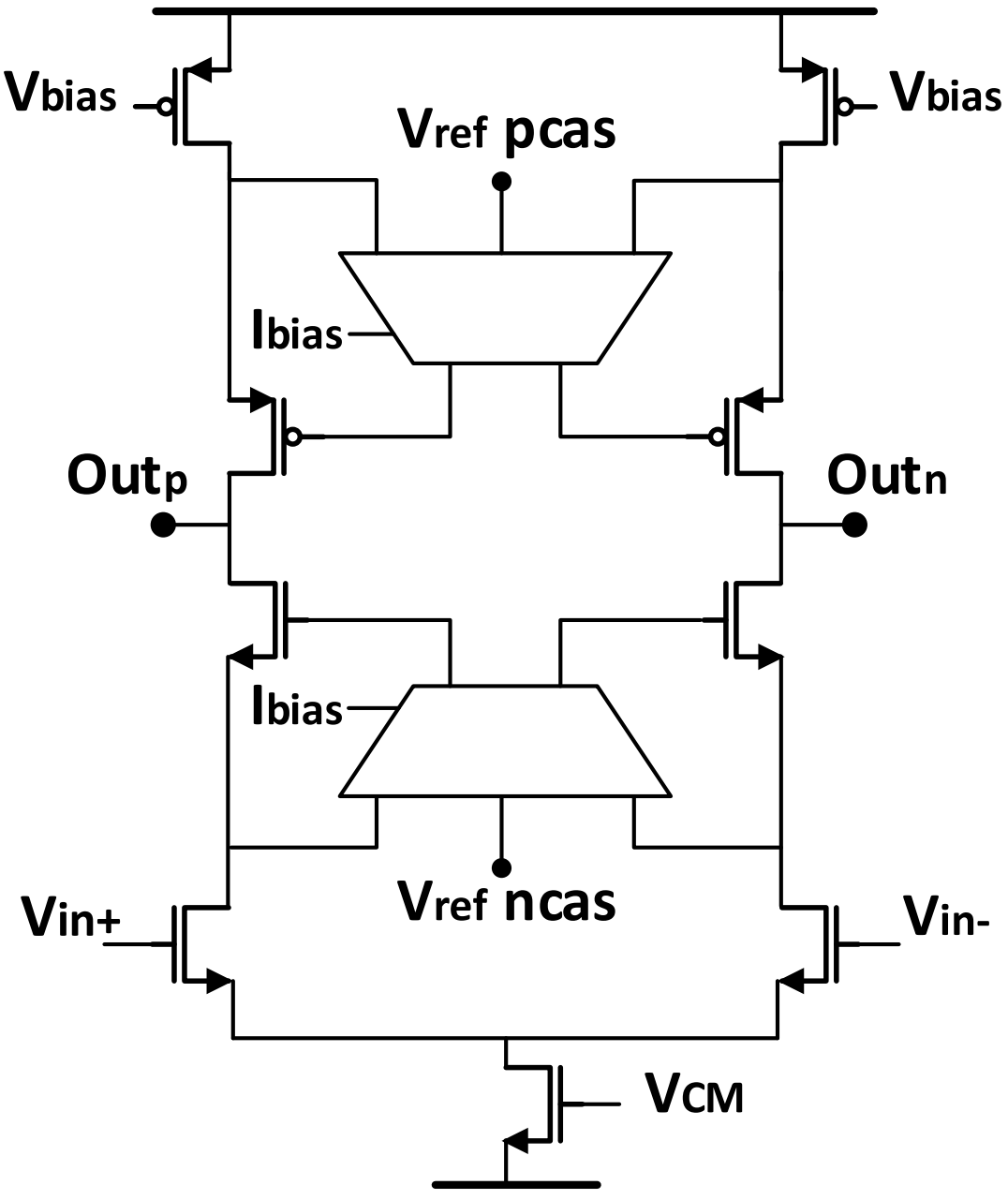

Figure 4-7 Simplified schematic of OTA I

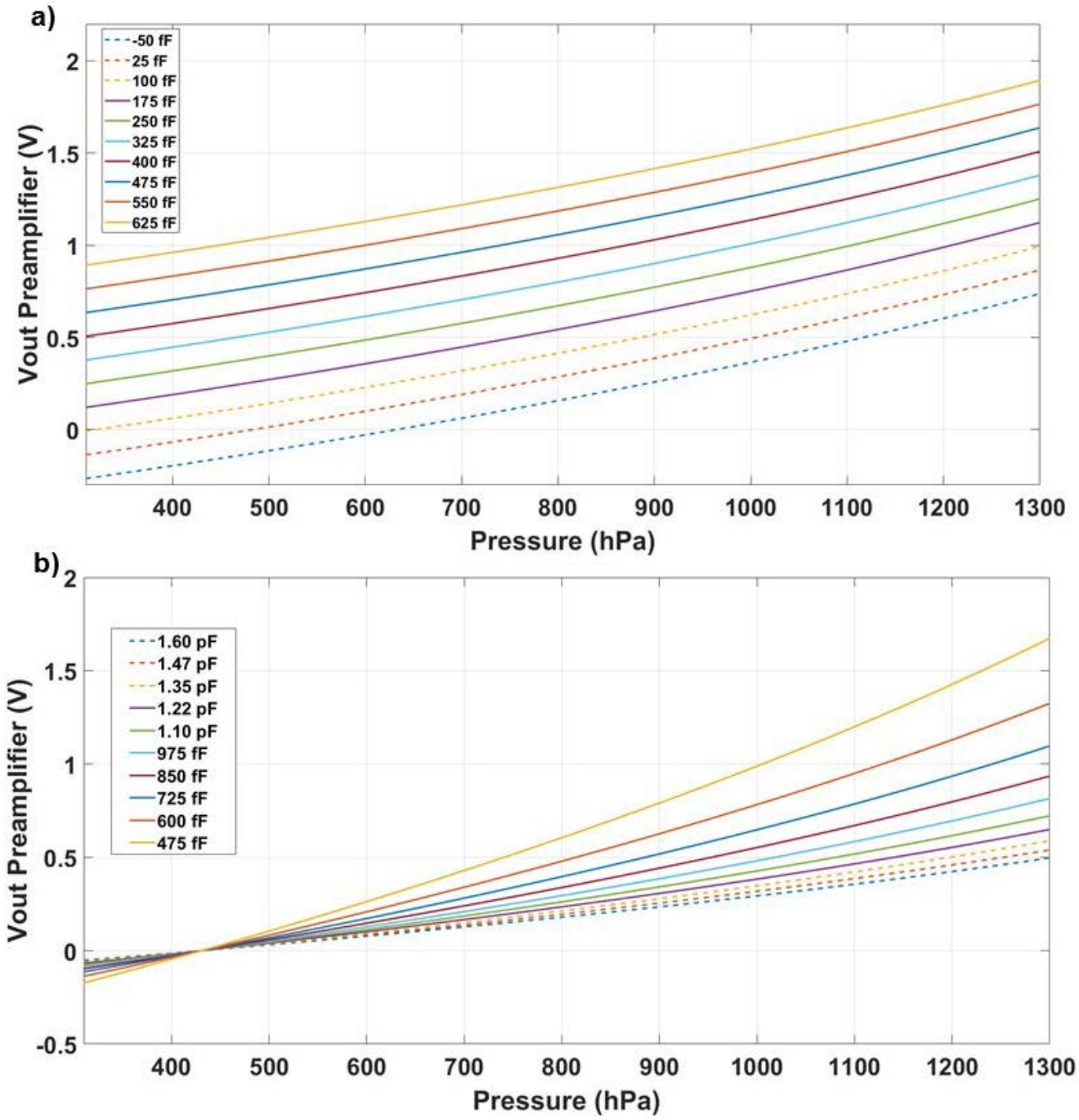

Figure 4-8 Preamplifier output voltage vs. pressure for different trimming of Coffset and CGain.

4.1.2. Self-Oscillating Noise-Shaping Dual-Slope

The power consumption of the DS ADC is given by the RC integrator formed with OTA II in Figure 4-4. The OTA used in the integrator is a two-stage class A/AB

pull-up-down topology and it is Miller-compensated. A simplified schematic is shown in Figure 4-9. This architecture allows a better power tradeoff with respect to folded Cascode and two stages class A topologies. However, in the class A/AB topology each gain stage requires a separate common mode feedback (CMFB) circuit. This is a consequence of using current mirrors in the second stage: the common mode output voltage of the first stage affects the bias condition of the second stage but does not affect the second stage output voltage. On the other hand, this kind of a second stage gives an output swing of 1 Vpp. This feature is mandatory in OTAs that are used inside a DS. Moreover, to cope with the 1/f noise introduced by the OTA input differential pair a chopping modulation technique has been adopted. The switch placed in before the differential pair (M1 and M2) modulates the amplifier´s input signal without any effect in the input offset. The demodulation switch is placed at a low impedance node before the dominant pole to perform the demodulation. In this way, the bandwidth of the amplifier does not limit the chopping frequency [60]. The signal used for this feature is the same that drives the demodulation stage of the Front-end circuitry; this way it is aligned with the timing of the system. The gain bandwidth product of this OTA has been set to 4 times the clock frequency GxBW=4·fclk (fclk=1/Tclk) to deal with the DAC pulses.

The switches that control the different phases in the DS ADC do not need to be done by a special circuit that increases the power consumption because their distortion is shaped by the noise-shaping behavior of the converter. Also, the nonoverlapping configuration helps to reduce the distortion. This OTA is working as an integrator of the DS. To be able to achieve high resolution the slew rate and the noise of this block need to be minimized. To deal with these specifications a DC_{Gain} = 116 dB has been selected, the Rout = 2 MΩ and Iout = 9 μA with a slew-rate smaller than 10 ns, which means the 0.1 % of the sampling time. The noise floor of this block is also under 4 μVrms as it was with the OTA in the preamplifier. This means that the dominant noise in introduced by the physical behavior of the MEMS due the excitation signal.

As it was mentioned before, the current DAC uses non-return-to-zero topology. To deal with the 1/f noise at the output of the IDAC, the current mirrors that drive the current cells are designed with large size PMOS (W = 9 µm / L = 94 µm) and NMOS (W = 9µm / L = 150µm) transistors. This solution in addition to the Self-Compensated DS behavior keeps the noise floor under the desired values. The oscillation in the feedback signal deals with the flicker noise, having the same effect as chopping but without any additional control. The effect of the oscillation has more weight in the Noise-to-Signal-Ratio (SNR) when the signal is small (because the time inside one period with oscillation is bigger).

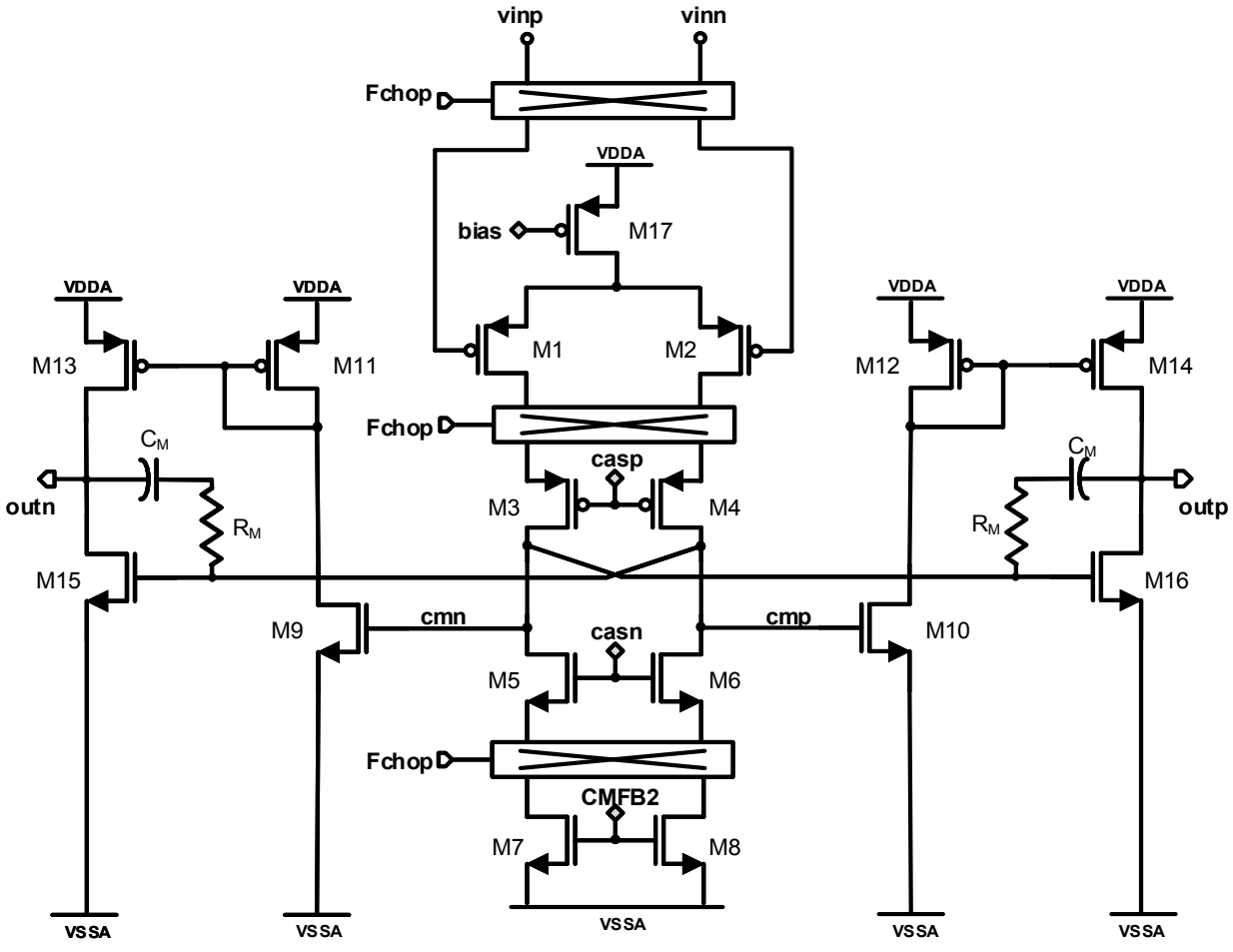

Figure 4-9 Simplified schematic of OTA II

A two-stage regenerative low power clocked comparator is used for the single-bit conversion. Its output is a PWM waveform that can be directly connected to the

IDAC and, with a stage of digital buffering, to the counter ADD to generate D_{OUT}. To capture the data in the desired time

a strobe signal is generated using the inverse cycle of the CLK and a window of Phase II of the DS. These two signals (D_{out} and Strobe) are captured and processed digitally. To measure DC input values with high resolution a reconfigurable digital filter (RDF) has been used. For this prototype, the RDF has been implemented in MATLAB. A diagram block of this filter is shown in Figure 4-10. The Data Generator can be configured for the resolution that is needed, using the Counter. The resolution depends on the measuring time, which is FL·Ts, where FL is the length of the filter. The data of this block is generated with low frequency (20 kHz) to save power. After the Data Generator, an interpolator is used to increase the frequency of this data to the sampling frequency. After integrating the data, the Tukey window is created. The output of the RDF multiplies the output of the ADC. The result goes through a configurable low pass filter to obtain a digital number adjusted to the resolution required. In our experiments, the configuration will be for high resolution, the RDF will be configured to give 20 bits.

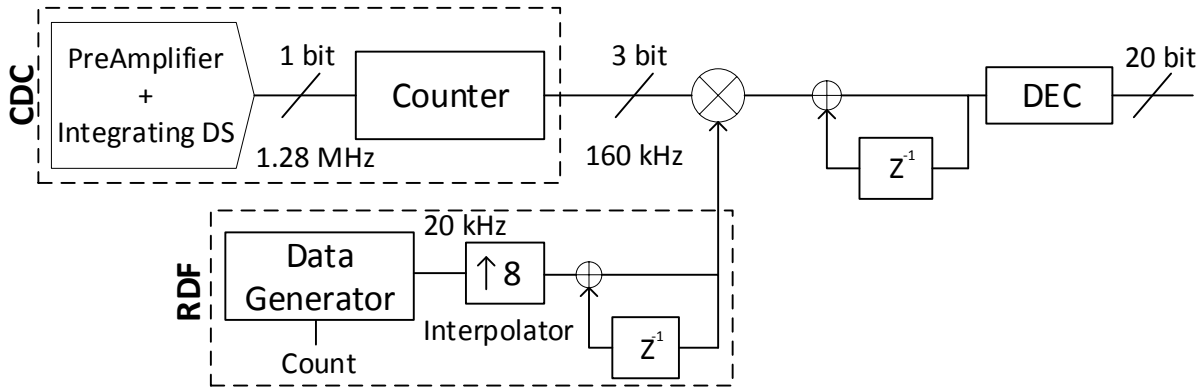

Figure 4-10 Block diagram of digital processing perform in MATLAB

4.2. LAYOUT DESIGN

In the design of microelectronics circuits, making a good design at transistor level does not always leads to a good behavior in silicon. There is an important step before production that needs to be considered. This step is the layout. Unlike digital circuits,

there are no tools that produces the layout of a design out of the schematic. The reason is quite simple. Every analog circuit need to be evaluated in a different way depending of the technology, architecture, application and special features that are considered. There is some research ongoing to try to achieve a software that can help with this [61], but until now, the outcome of this work is not flexible and efficient enough.

To design a good layout, basic physic principles are taken into account. The resistivity of a track or the capacitance between two layers of metal, can imply that the design behaves different from what is expected. There are some basics that every one that is going to make a layout needs to know:

4.2.1. Distance.

Even if it looks obvious, one of the main errors out of a layout design is the distance. The resistivity of the metal increase with the length of the tracks, which means that the tracks need to be as small as possible, making the design compact. This plays an additional role in differential circuits, were the signal goes through two different tracks. In this case, the layout design is done with a mirror topology, making each half of the circuit equal to the other. Using this technic, the mismatch of the signals is reduced. Also, the distance between tracks is selected carefully, as it is well known, the crosstalk and parasitic capacitance between tracks highly depends on this variable.

4.2.2. Size of transistors.

When the design is ongoing at transistor level, there is an extra fact that needs to be taken into account, the size of transistors. For a good packing of the components of the design and to reduce the mismatches of performance due manufacture issues, the size of transistors is selected proportional to a unity value. Doing the design in this way, it is possible to have just a few different sizes of transistors, making easier the placing and improving the design. A good selection of transistor size is shown in Figure 4-11 where the transistors between P69 are placed together in the layout even if they are not

close in the schematic. As it was mentioned a few lines before, design using this method helps to reduce the manufacture issues, the reason is the following: the manufacturing of silicon circuits is performed by lasers. The lasers are the ones that divide every layer of the circuit. In fact, one of the reasons that the microelectronics evolve in size is due better lasers. However, the cuts of this lasers are not perfect, having some tolerance. The tolerance of the cut can lead to differences between transistors that were meant to be equal, producing discrepancies with the theoretical behavior at schematic level. Using a unity cell as minimum transistor size and placing multiples of this cell to increase the size when is needed, helps to reduce the possible differences with the theoretical behavior. With this topology all the transistor will have a similar deviation from their nominal size, having less problem of mismach between transistors.

Distance plays an additional role if the third dimension is considered. As in PCB design, microelectronic circuits have different layers for tracks. It is important to consider the distance in this axe and avoid putting two different signals, one below the other. Normally to minimize distance of connections an increase the distance between tracks, the layers of metal that are closed are used in different axes, one for X dimension and the following for Y dimension.

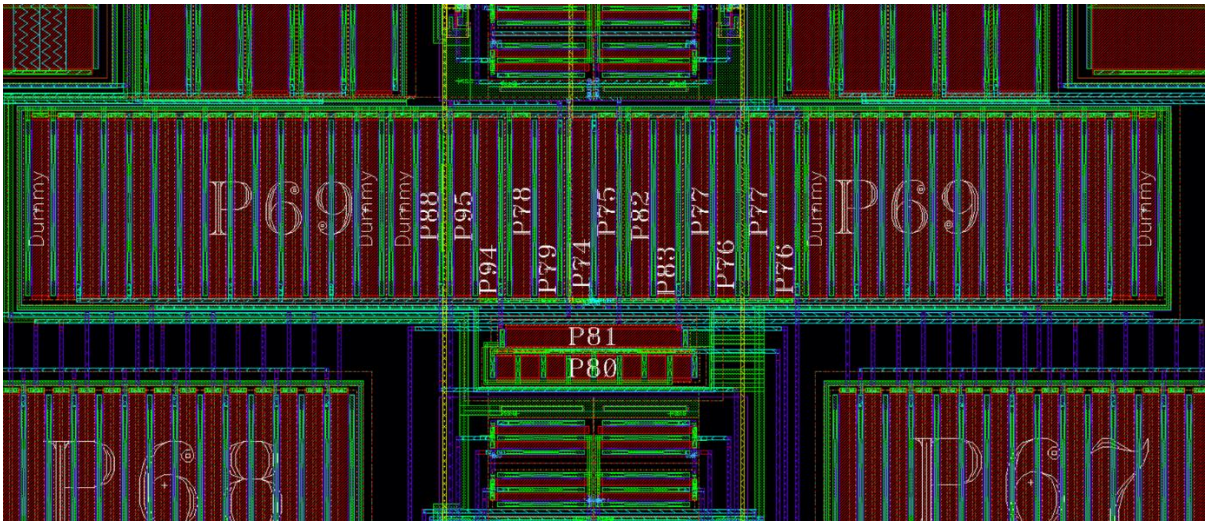

Figure 4-11 Layout view of PMOS transistors of the first stage in OTA II.

4.2.3. Dummy transistors.

The use of dummy transistors is related with the previous point. Even if all the transistors are selected with the same size, there will be a problem in the edges of transistor blocks. Normally the transistor that are placed in these positions have bigger tolerances that the others. To avoid this problem the dummy transistors are used. As the name says, the dummies transistors don´t have any electrical purpose. The only reason to include them is to improve the performance of the active ones. The use of this kind of transistors can be seen in Figure 4-12, dummies transistors are placed at the beginning and end of each block of transistor that share the connections. There are two types of transistor depending on the connection between them. If the family of transistor between the dummy transistors share the source and drain connection, the dummies will share them two, having the other connections short-cut to ground (in NMOS) or to VDD (in PMOS). These dummies are equivalent to diodes, making an influence in the output charge of the stage. This drawback need to be taken into account to avoid other problems. In Figure 4-12 they are marked with blue rectangles. The other type of dummies is used when the other transistors are placed close to each other, but they can´t It is clear that the second type of dummy transistor doesn't have any drawback in the electrical behavior of the design, however, the only use of this type will increase the

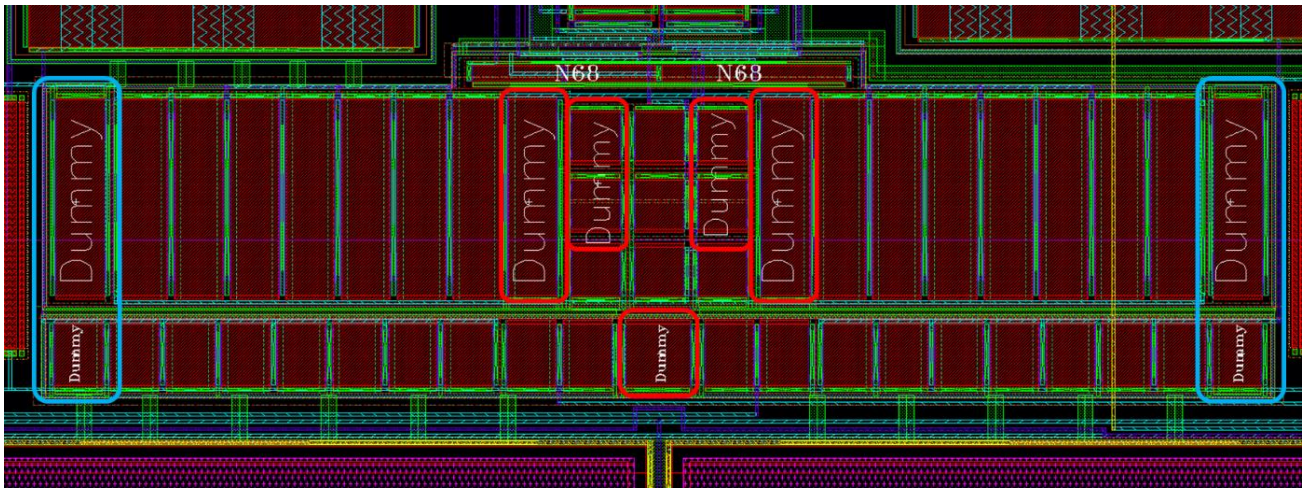

Figure 4-12 Layout view where different kind of dummy transistors are used

total area of the design (because the nominal transistor won´t share the drain and source connection) and the number of tracks will increase..

4.2.4. Guard-rings.

As mentioned in a previous point. The crosstalk is one of the mains sources of problems in a microelectronic circuit. Having very small distance between signals of one volt, can easily leads to crosstalk issues. To fix this problem the guard-rings are used. Figure 4-13 show one of the guard-rings used in the design. They are needed when the transistors have a different substrate from the ones that are closed or when a special care of the integrity of the signal is needed. Guard-ring surround a group of transistors making a connection between metal and the substrate of this transistors working as isolation. However, adding guard-rings to the layout design increases the area and the length of the tracks. Because of that, guard-rings are placed in the design when it is really necessary. A good example of the increase in area can be seen in Figure 4-13, where the transistor associated with the input differential pair are separated and isolated inside a guard ring. It can be seen that the empty space around these transistors is

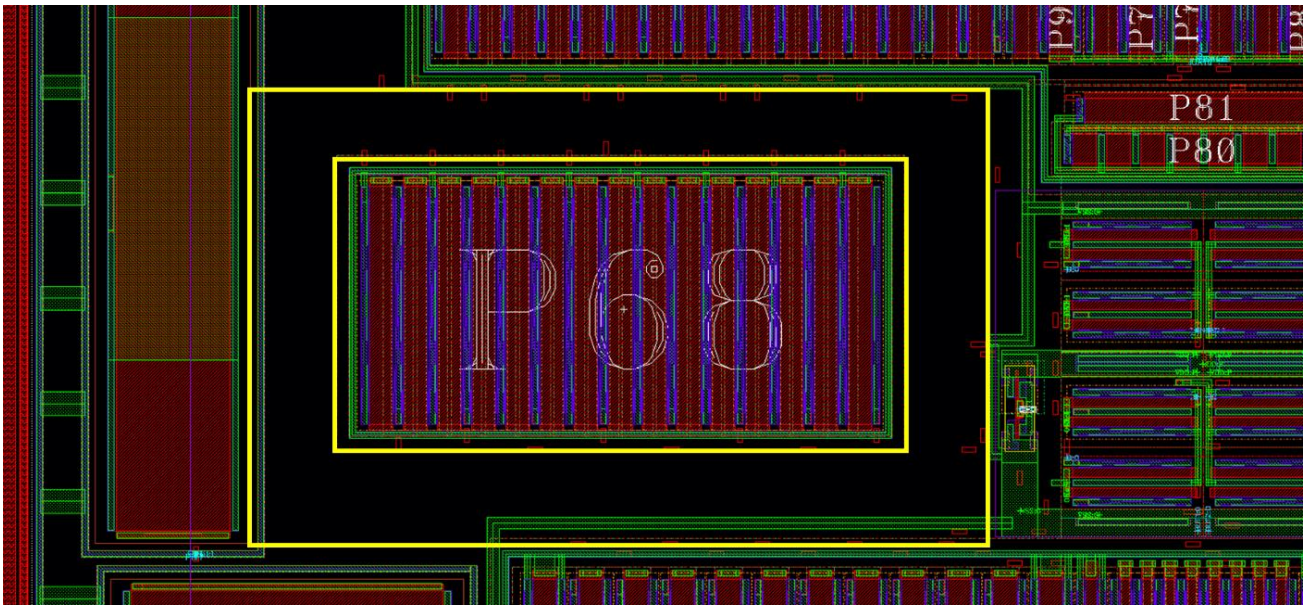

Figure 4-13 Layout view of a Guard-Ring surrounding P68 and its death zone due design constrains

considerable. However, the distance is chosen by the rule checker of the technology. It says that different bulk connections need to be 3mm away from each other.

4.3. Package & Bonding

After the design is on silicon, the bounding with the MEMS and with the package need to be done. This step of the design is the bigger contributor in non-ideal behavior of the design. Parasitic capacitance will be added due the distance of the wires from the pin in silicon to the MEMS and to the external connection of the chip. The bounding of the MEMS has been implemented as close as possible and the size of the package have been selected as small as possible taking in account the number of PINS needed (64).

Two different packages have been used. The first one is a flat package (IFK68F1-2722A). The area and parasitics of this package is too big for a good performance of the MEMS. However, the porpoise of the prototypes bonded in this kind of package is to characterize the ADC. That means that the CDC is bonded alone in the package. The chip is connected to the test board with a socket. Making the testability of a big number of samples much easier compared with soldering samples. However, the performances won't be taken as nominal results and therefore they won´t be presented in this document. The second package used is a CQFP64, a compact ceramic package with less area and parasitics than the previous one. For these models the MEMS sensors are included inside the chip. The bonding scheme can be seen in Figure 4-14.

To have an idea of the dimensions and the difference between them, we can compare the size of different package in Figure 4-15. On the left size of the figure, the CDC prototype without any package is presented. The two other packages are the ones used for the measurements. In the smaller one the bonding between the MEMS sensor and the CDC is done. That is the reason of the drill on top of the carrier, to be able to measure the ambient pressure. Like it was mentioned before the samples can be affected by non-idealities in this process, one of the main reasons is the parasitics introduce

between the MEMS and CDC. That is why in CQFP64 the distance of this bonding is minimized.

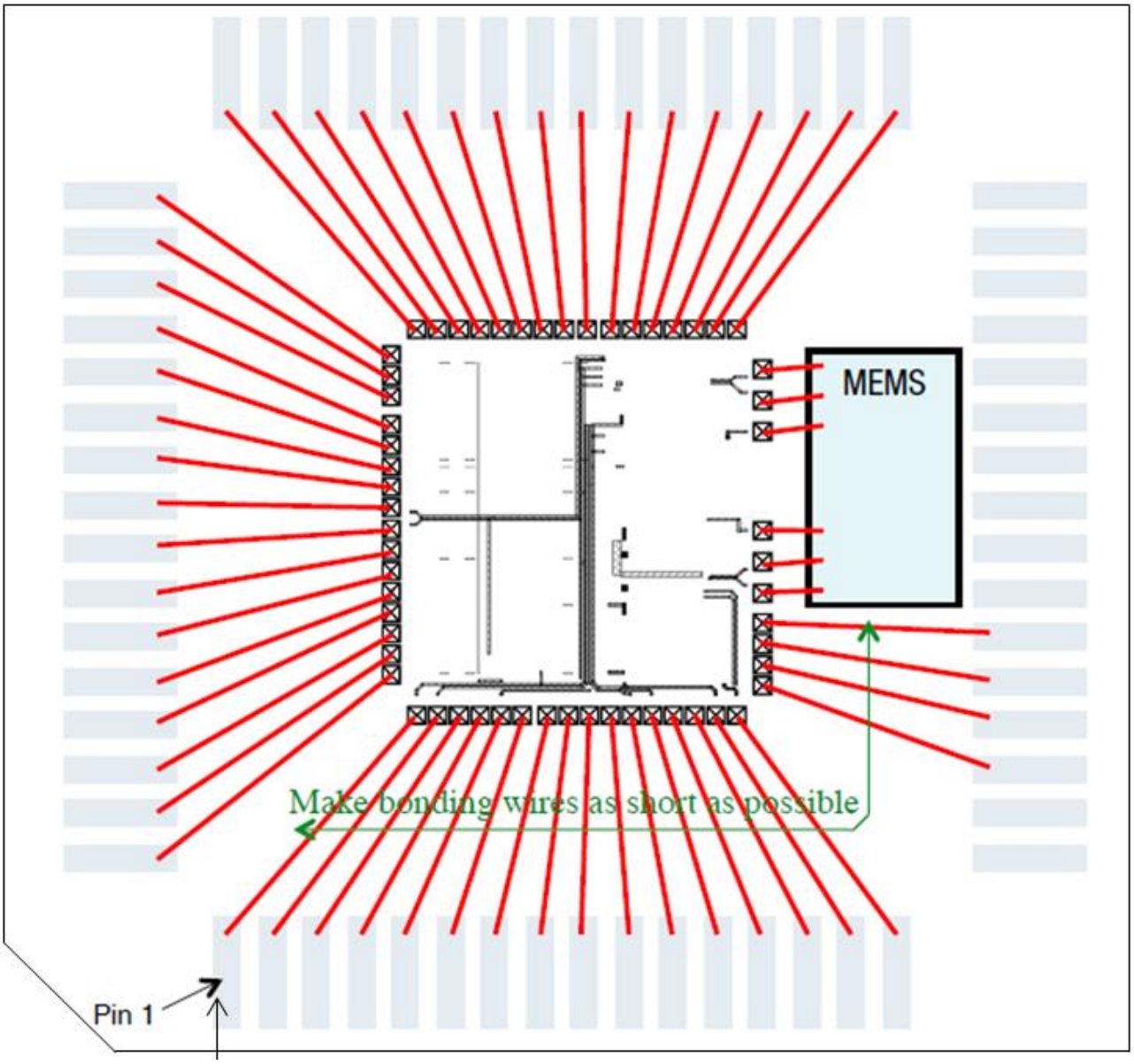

Figure 4-14 Bonding Scheme of the CDC in CQFP64 package

4.4. Conclusion

There are many different steps that are needed to full fill in order to complete the design of a prototype. To don´t affect the integrity of the design special care has been taken during all activities having an impact in the design.

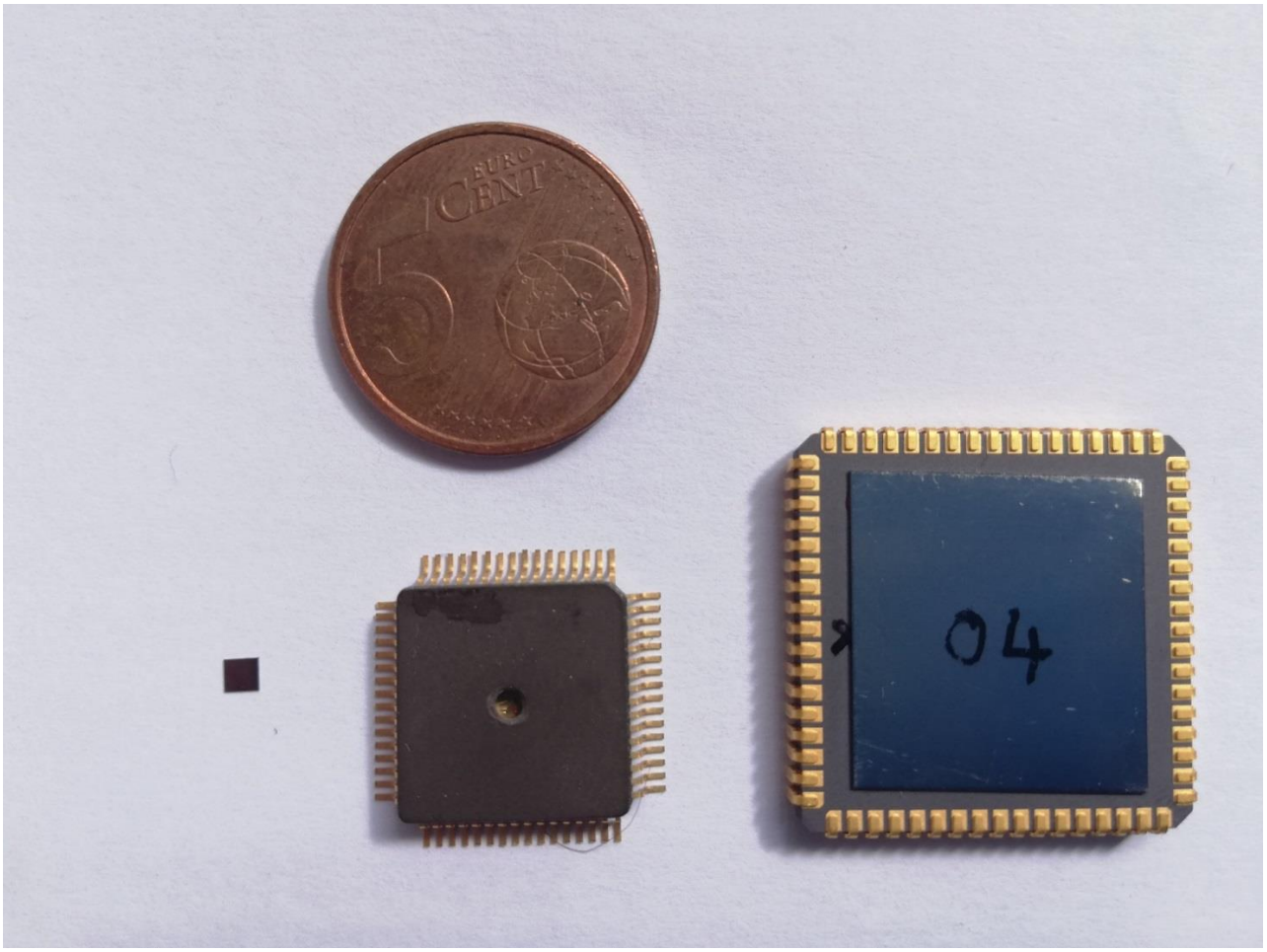

Figure 4-15 Comparison of size between silicon and different package

First of all, to have a proper connectivity between the different blocks, digital blocks have been designed to provide the synchronization signals needed. In this way every conversion of the DS starts after the stabilization of the output signal of the MEMS. If this is not guaranteed, the output of the CDC will be directly influenced by this effect losing a lot of resolution due oscillation behavior.

The system level has included different chopping parts to reduce the low noise contributors (offset and flicker mainly). All the chopping activity is synchronized to keep the signal integrity and it is related with the sample frequency in order to don´t affect any conversion period.

The circuit design has done to optimize as much as possible the power consumption keeping the performances. Blocks have been designed taking into account

a continuous time architecture, where less bandwidth is needed to keep integrity in the transfer function compared with SC circuits. This feature gives more room for efficiency in power consumption. Chopping feature inside the integrator of the DS has been done using nodes of low impedance, reducing the effect in the DC gain and the noise contribution. The flicker noise in the feedback loop is minimized by the size of the transistors used in the DAC plus a cancelation due the PWM behavior due the Self-Compensated behavior.

Layout was done taking in consideration all the techniques mentioned before obtaining a compact design with symmetric blocks that will reduce the mismach of the differential topology.

Part III

Experimental Results & Relevance of the proposed CDC

Chapter 5.

Experimental Measurements

To obtain experimental results, a prototype of the proposed CDC was fabricated in a standard digital 0.13 μm CMOS technology. The CDC was bonded together with a pressure sensor MEMS to minimizes the effect of parasitic capacitances between them. The bonding is done in a ceramic carrier of 64 pins. The cover of the package has a drill on top of it to give the possibility of controlling the air pressure inside this cavity. Figure 5-1 Die photo of the MEMS sensor and the CDC bonded together in a package with a drill for pressure control presents the proposed solution through the hole where the pressure controller will be connected. The CDC core has an area of 0.317 mm^2 and a mother clock of 1.28 MHz (which gives a sampling frequency of 160 kHz). The chip is connected to a 1.5 V power supply and it consumes 146 μA. This current includes analog blocks, digital blocks and excitation signal generator blocks. The V_{EX} that drives the bridge of the capacitor MEMS, which is also used to demodulate the input voltage of the pre-amplifier and to chop the integrator inside the DS, is set to 80 kHz.

5.1. Setup configuration

Each sample is welded to a small PCB that is connected into the socket of the mother PCB. This PCB is designed to control all the programmability of the digital

inputs (Offset and Gain of the pre-amplifier and different modes for test), do the readout of the output of the CDC and generate the necessary voltages needed in the chip and in the PCB.

The setup connected and working can be seen in Figure 5-2 Test-chip welded and working connected to the test PCB and pressure controller.. In this configuration the pressure controller that creates the isolated chamber inside the package is also connected. With this configuration the setup can feed a stable pressure to the CDC into the package with an accuracy of ± 0.1 Pa in the range from 500 hPa to 1200 hPa.

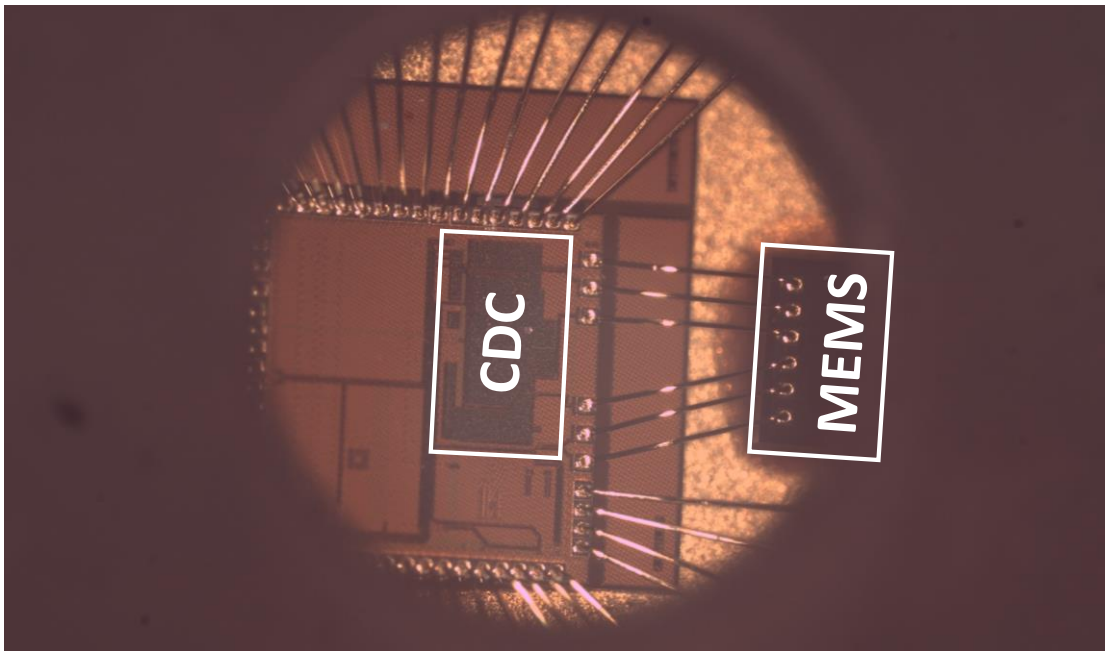

Figure 5-1 Die photo of the MEMS sensor and the CDC bonded together in a package with a drill for pressure control

To have a better knowledge of the experiments performed on the prototype and give the possibility to replicate them, the equipment used during this whole process is presented in Figure 5-3, it contains:

- Oscilloscope: *Tektronix DPO 5034* with BW=350 MHz and 3 GSamples/s.
- Clock generator: *Tektronix AFG 310.2*
- Power supply: *Agilent E3631A Triple Output DC Power Supply.*

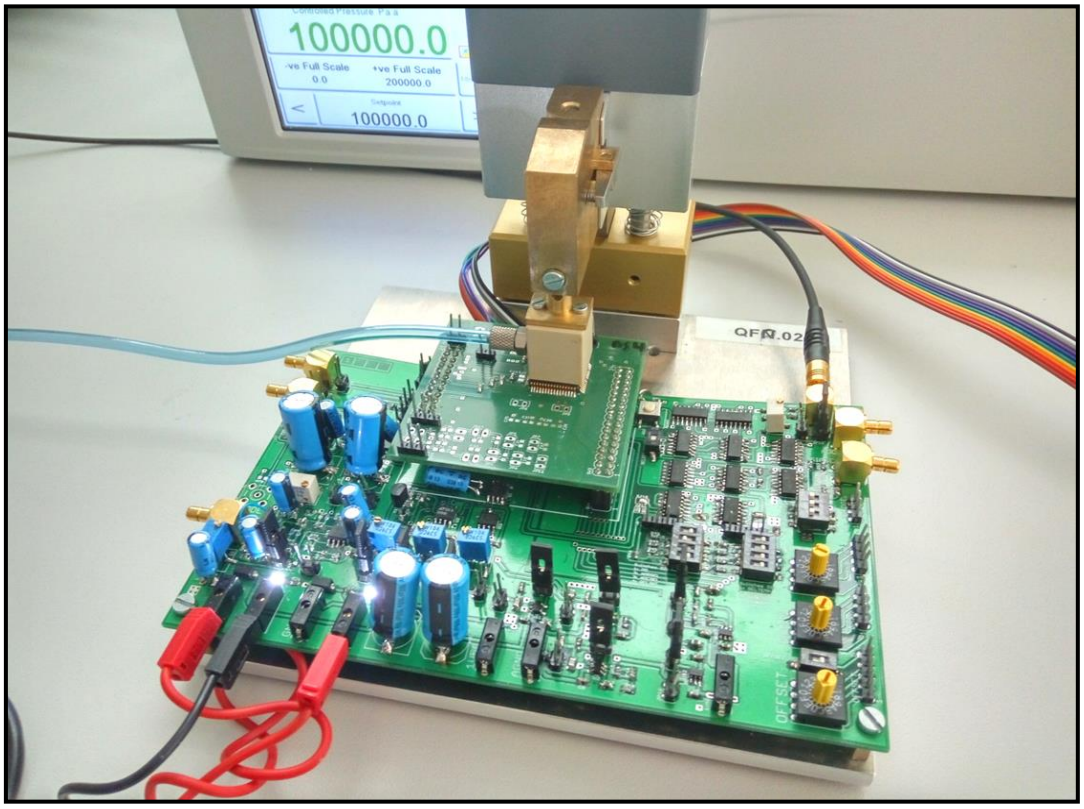

Figure 5-2 Test-chip welded and working connected to the test PCB and pressure controller.

Figure 5-3 Hardware used to make all the experiments of the test-chip.

- Pressure controller: *Druck pace 5000*
- Bitstream Analyzer: *GP_24132*
- Temperature test chamber: *Vötsch VT 7004.*

The master supply voltage and the master clock used in the PCB are ±5 V and 2.56 MHz respectively. The output data is captured using the official software of the Bitstream Analyzer. This software generates a text file that has a one-bit stream with the outputs of the CDC. The file is processed later with MATLAB.

5.2. Resolution measurements

To start with the measurements the readout circuit needs to be configured. AS it was mentioned before, to make a proper conversion in the whole range of the CDC is important to verify, and adjust if it is possible, the transfer function of the converter. If no calibration is done in this step, the DS integrating ADC will still work. The setup is design to align the range in capacitance of the input MEMS sensor with the input range of the DS.

After the initial configuration the system is ready to measure. Future calibration will not be needed unless the readout circuit is connected to a new MEMS sensor. To make quick check that the chip is behaving as expected and begin with measurements to characterize the performances of the chip, the signals available of the system can be checked with the oscilloscope Figure 5-4. These signals are equivalent to the ones explained in section 4.2 (Figure 4-6). It can be seen both figures (Theoretical behavior and experimental behavior) are showing the same behavior, as it was expected. “Clk” is the master clock of 1.28 MHz used to create all the phases and lower clocks. Strobe is the signal created to capture data from comparator output, the data out of the comparator will be registered only when there is a rising edge of Strobe signal, this happens only in Phase II of the conversion, where the disintegration time of the capacitor is measured. V_{EX} is the master source of all the modulation implemented in the chip. It is the signal

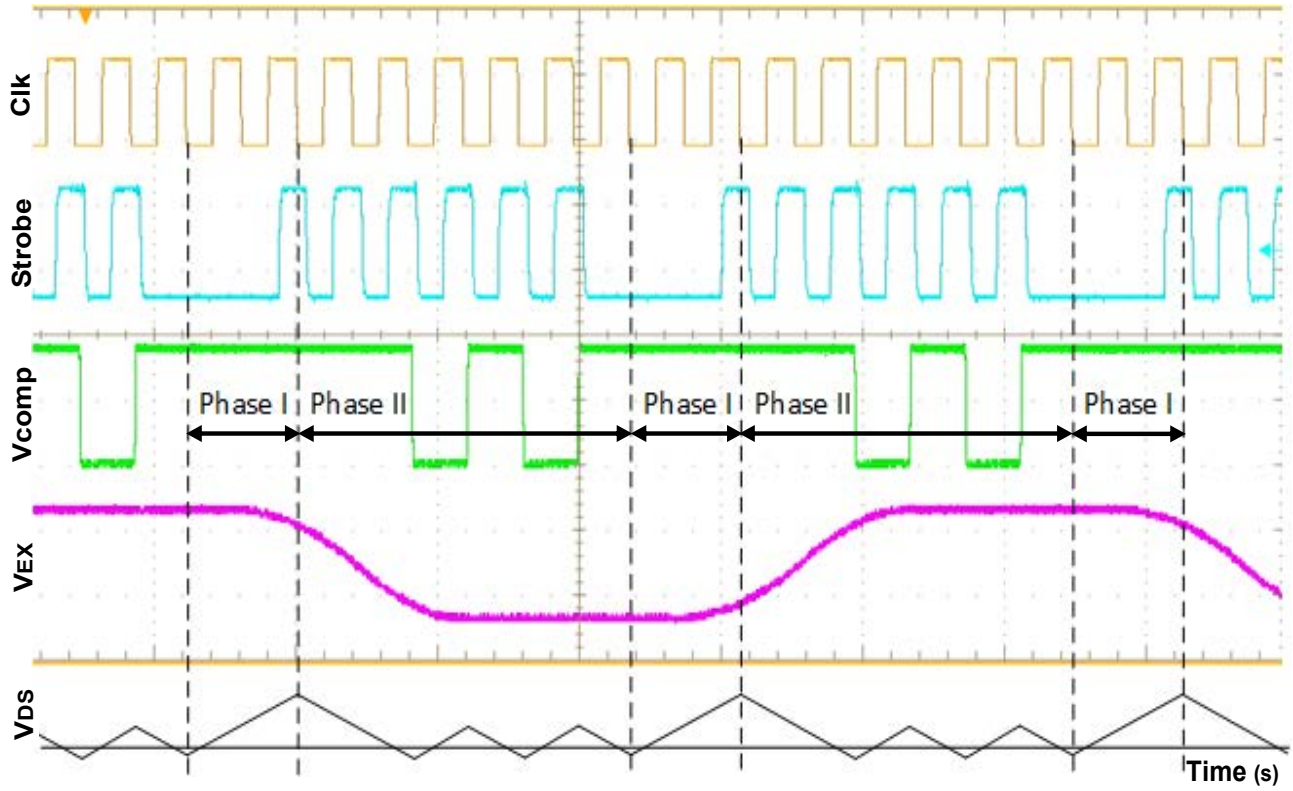

Figure 5-4 Time diagram of the signals that proves the behavior of the Integrating DS measured from the test-chip.

that drives the MEMS bridge. V_{comp} is the digital output obtained from the comparator and the one that is saved every rising edge of Strobe. V_{DS} is added to make easier to understand if the system is working as expected, like in Figure 4-6.

Ten different samples have been measured to study and verify the robustness of the design. To measure these samples the pressure controller was attached to the top of the package. A constant pressure with an error of ±0.1 Pa is set by Druk Pace 5000. The spectrum of the digital output of the CDC under these conditions is shown in Figure 5-5. It represents an input pressure of 1050 hPa, equivalent to a -16 dBFS at the input of the DS ADC, where the Full-Scale is VFS=1V. The measured equivalent integrated noise over a bandwidth of 10 Hz is 4.5 μV_{rms}. Using the main formula to calculate the SNR in CDCs, (22), the obtained integrated noise leads to an SNR of 103.9 dB or an equivalent ENOB ≈17 bits.

$$\mathrm{SNR} = 20 * log_{10}\left(\frac{V_{FS}/\sqrt{2}}{V_{rms}}\right) \tag{22}$$

Also, in Figure 5-5 the first order noise shaping from the Integrating DS converter can be observed. The modulation between the DC signal and the clock is present. This behavior is well known in first order noise shaping ADCs. The tones that can be seen at high frequencies are a consequence of the ratio between the sampling frequency and the length of the two different phases with the self-oscillating behavior. However, thanks to the modulation behavior they do not affect the in-band noise floor, and therefore, the resolution.

The purpose of this implementation is to reach high resolution for differential measurements. To achieve this, the chip needs to distinguish small changes of pressure from following measurements. For that, another experiment has been done. Keeping a constant pressure, different measurements have been done and processed. In an ideal design, the output of all of them (with the same input pressure) would be exactly the same. However due the noise and non-idealities of the circuits and implementation, some noise will affect the performance. Because of that, the different digital output values will be taken out of the CDC for the same input pressure. This data will follow a normal distribution with the average on the theoretical value of the transfer function and a deviation that will be related with the error of the CDC Taking in account that in this experiment the input data would be considered as a constant DC value through all the acquiring of data, an alternative way for measure the resolution of the chip can be used and contrast that the values obtained for static measurements (with the FFT) are valuable. For this reason, to measure the resolution of differential measurements, instead of using an FFT, the standard deviation of all the samples is used. Out of 100 of measurements, the results give a σ_{rms}= 4μV_{rms} which leads to a ΔC= 7 aF and ΔP= 1 Pa.

Experimental Measurements

Using the formula presented inside Figure 5-6, the value of ENOB=17.1 bits is achieved. This result is coherent with the spectral density shown in the FFT of Figure 5-5.

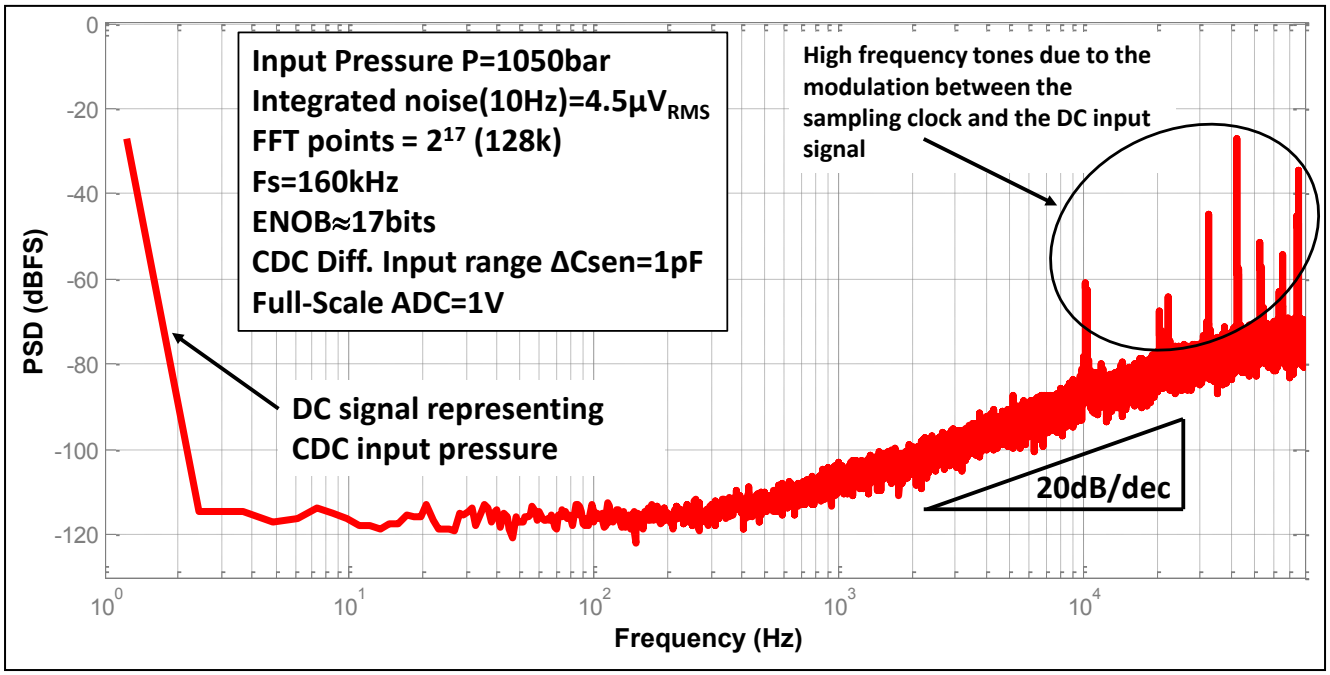

Figure 5-5 FFT of the CDC for an input pressure of 1050mbar

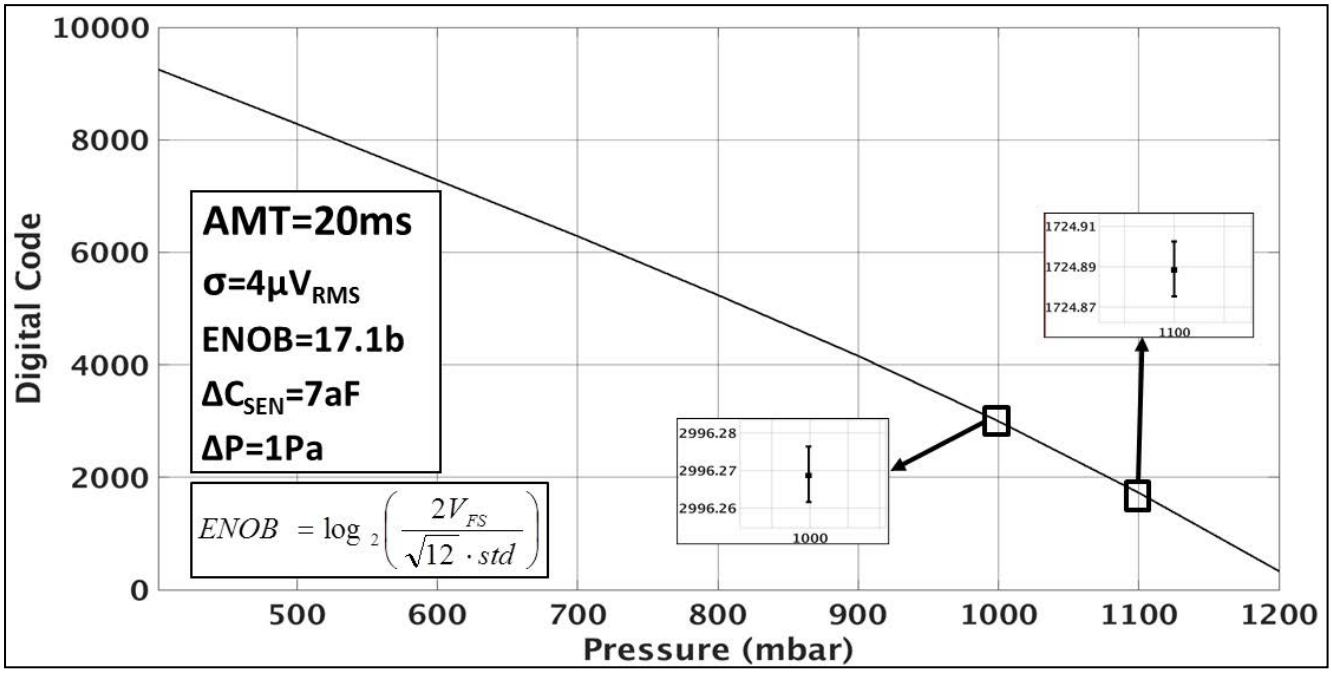

Figure 5-6 Digital output code of the CDC vs Input pressure in differential measurements analysis.

5.3. Temperature variation

After these experiments have been done, the resolution has been proved over different samples. Also, the distribution of the measurements for differential resolution proves that the solution is a good candidate to take in account for these kinds of applications. Taking in account that the direct application of the CDC present in this work is inside the IoT, a final experiment has been done to check the performance over the possible temperatures. For this experiment the prototype has been introduced inside of a temperature test chamber. A range from -40° to 80° has been covered. However, to be precise with the measurements and have a better control of

the temperature on chip a PTC 100 of four channels is attached on top of the package. In this way a measurement of temperature with a resolution of ±0.5°C is provided very close to the chip. For each temperature, the same kind of measurements used in differential analysis has been done. To perform this experiment to the temperatures were faced from 80 ºC to -40 ºC. The direction of temperatures is very important in order to avoid condensation due the change of temperature and therefore Relative Humidity (RH) close to condensation temperature. That is the reason why instead of measuring the behavior with 0 ºC, the measurement has been realized for -5ºC, avoiding any melted water on the surface of the setup. Also, to avoid frozen ice on PCB the placement inside the chamber was selected far from the gate that introduces the wiring. Even if this is close in an adiabatic way, a small flow of air produces the condensation of RH around this area.

The output of this analysis is a transfer function for each temperature point. This result is shown in Figure 5-7. The data presented is RAW data. No compensation or modification has been done. To merge all the transfer functions to a single one is important to take in account all the factors that contribute in each curve that are under control. The first one is the error related with the temperature dependency of the MEMS. The ΔC between the Csens and Cref is not only dependent on pressure. Different

temperatures introduce a different offset in the ΔC for each pressure point as it can be seen in Figure 5-8. Using for each temperature the curves presented in this figure, the correction factor is applied digitally. In our experiments, this correction was done directly in MATLAB. Once the temperature error is solved, a correction of offset and gain is applied. For this design a polynomial of order one (y = ax + b) is used. The final output after all the correction factors is presented in Figure 5-9. The resolution between different curves is, ENOB(T)= 11 bits. This number means an error resolution of ΔC= 44.5 aF and ΔP≈ 7 Pa between different temperatures. It is important to take in account that this value represents absolute resolution. It is not the same as the differential resolution explained before. It means that for every environment the system will follow and equivalent behavior for following measurements but in order to be consistent between different temperature regions, a bigger error needs to be taken into account. This will be taken into account for future works, a complex solution that includes more sensors, like temperature, in order to prove the flexibility of the solution and to calibrate itself.

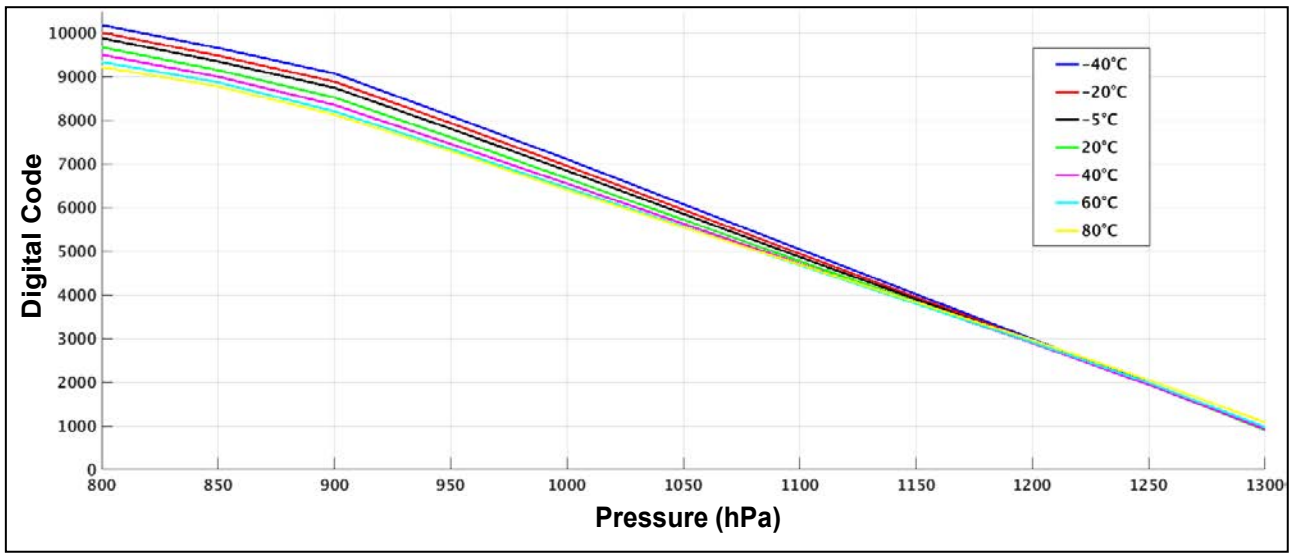

Figure 5-7 RAW data out of the transfer function measured in the prototype for different temperatures

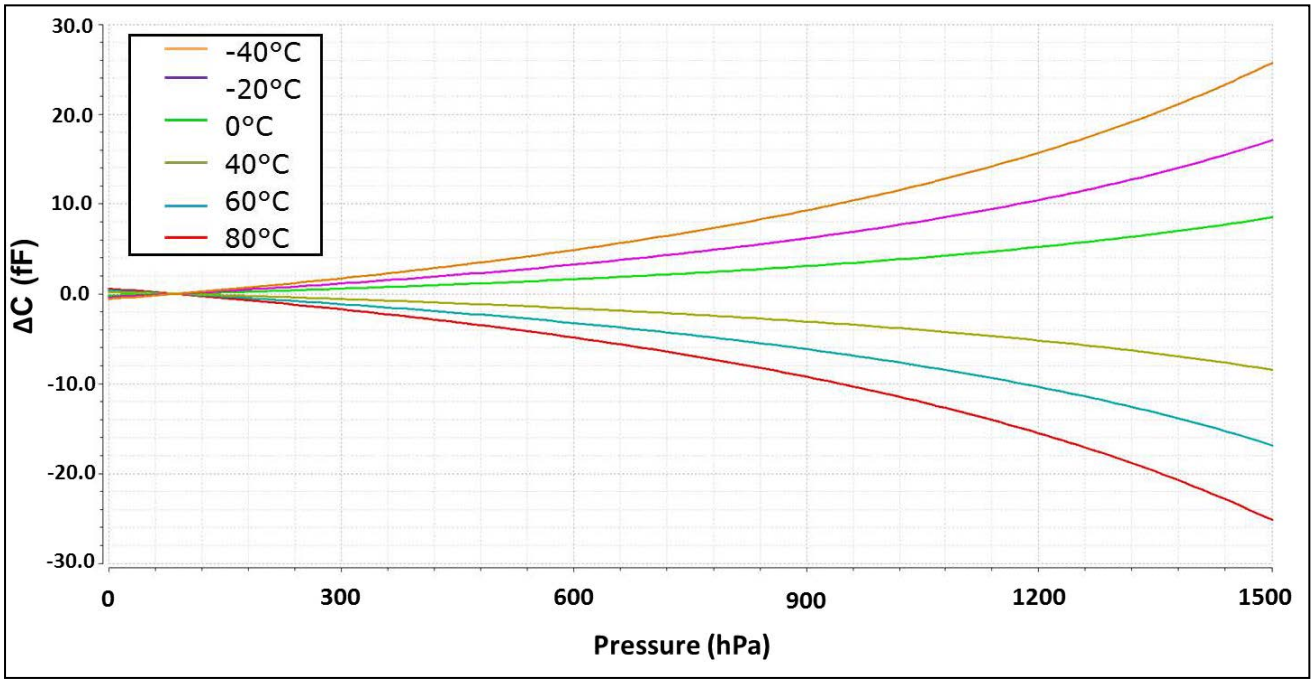

Figure 5-8 Error of resolution in the MEMS depending on the pressure for each Temperature

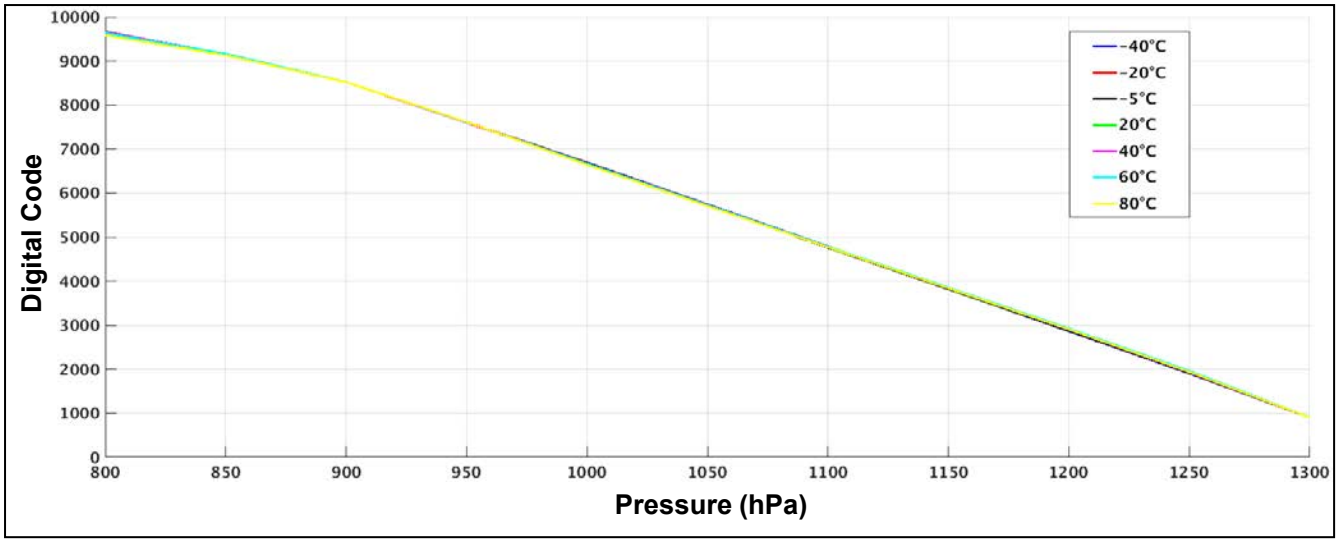

Figure 5-9 Compensated transfer functions after temperature, offset and gain error for different temperatures

5.4. COMPARE WITH THE SOA

In this work, an incipient new family of converters is presented. The proposed Self-Compensated noise-shaping DS device can achieve the same performance of the

topologies that use ΔΣ properties but using one-bit circuitry and time domain for the conversion. This fact gives also the benefit of low power architectures like SAR or classic DS. Also, in the previous chapter is demonstrated that the architecture presents a strong behavior against PVT variations.

Table I shows the main characteristics with the FoM of the state-of-the-art converters and this work. The FoM used to compare the different topologies takes into account is presented in equation (23). The table shows that the topology presented in this work has similar SNR_{Cap} (defined in equation (24)) to the topologies that use ΔΣ properties and FoM in the range of the other topologies of the state-of-the-art CDCs that target the same capacitance resolution. As mentioned before ΔΣ modulators can achieve higher resolution at the expense of higher power consumption. SARs converters are power efficient, but they are not able to achieve high resolution. Incremental converters are also power efficient, and they can achieve higher resolution, but as mentioned before, their power consumption is higher than other solution plus the conversion in amplitude domain will be affected by low voltage technologies.

$$FoM = \frac{Power \cdot Meas\ Time}{2^{(SNR_{Cap}-1.76)/6.02}} \tag{23}$$

$$SNR_{Cap}(dB) = 20 \cdot log \cdot \left[\frac{V_{full-scale}/2\sqrt{2}}{Resolution}\right] \tag{24}$$

VCO are very efficient but have a limitation in resolution due the non-linear behavior. Finally, classical DS is not efficient enough in resolution for these applications. Hybrid solution shows an improvement respect the architectures used alone. Weak points of each topology are minimized reaching a new level of performances with very efficient numbers in power consumption and area. With the information in Table 2, Figure 5-10 presents a graphic of the State-of-the-Art.

Table 2 CDC state-of-the-art

Reference	Type	Measure Time (ms)	Power (μW)	Sensor Range (pF)	ΔC_{min} (aF)	SNR_{cap} [1] (dB)	FoM [2] (pJ/conv)
[27]	ΔΣ	0.020	15000	10	65	94.71	6.75
[15]	ΔΣ	0.8	10	1	70	74	2
[12]	Hybrid	0.23	33.7	24	160	94.5	0.179
[24]	VCO	0.019	1.84	0.7	12,3	26.1	2.13
[36]	Integration	7.6	211	6.8	170	83	139
[19]	Integration	6.4	0.1	25.4	55,3	44.2	5.31
[20]	ΔΣ	1090	3750	8	4.2	116.6	742
[28]	ΔΣ	100	60000	4	1	123	5190
[16]	ΔΣ	13.3	6000	0.16	4	83	6,9
[29]	ΔΣ	10.5	760	16	42	102.59	74
[21]	ΔΣ	0.128	15	1	207	64.65	1.38
[35]	IDC	10.2	10	2	80	78,9	14.9
[30]	ΔΣ	100	7	0.4	1110	42.1	6730
[34]	IDC.	0.001	1440	1	490	57.2	2.44
[17]	Hybrid	0.001	7.5	5	1100	64.1	0.006
[23]	Integration	1	20	15	1140000	53.35	0.053
[32]	SAR	4	0.16	72.8	60	72.6	0.183
[31]	SAR	0.005	6.7	3.2	470	67.6	0.017
[14]	SAR	100	0.8	18.5	30,4	46.7	455
[37]	VCO	1	0.27	0.3	1200	38.9	3.74
[22]	Current	0.004	725	0.75	1130	47.4	13.2
[18]	Integration	0.02	15800	0.4	733	45.7	2010
[13]	SAR	250	0.22	78	122000	47.08	0.298
[62]	SAR	300	1000	2	1000	56.9	519
This work	Self-Comp. DS	20	220	1	5.4	96.3	82.2

There is a trade-off between the FoM and the resolution in all the converters. All of them use different measuring time or different power consumption to achieve different resolution, but somehow the change of these variables is just moving the solutions over an edge.

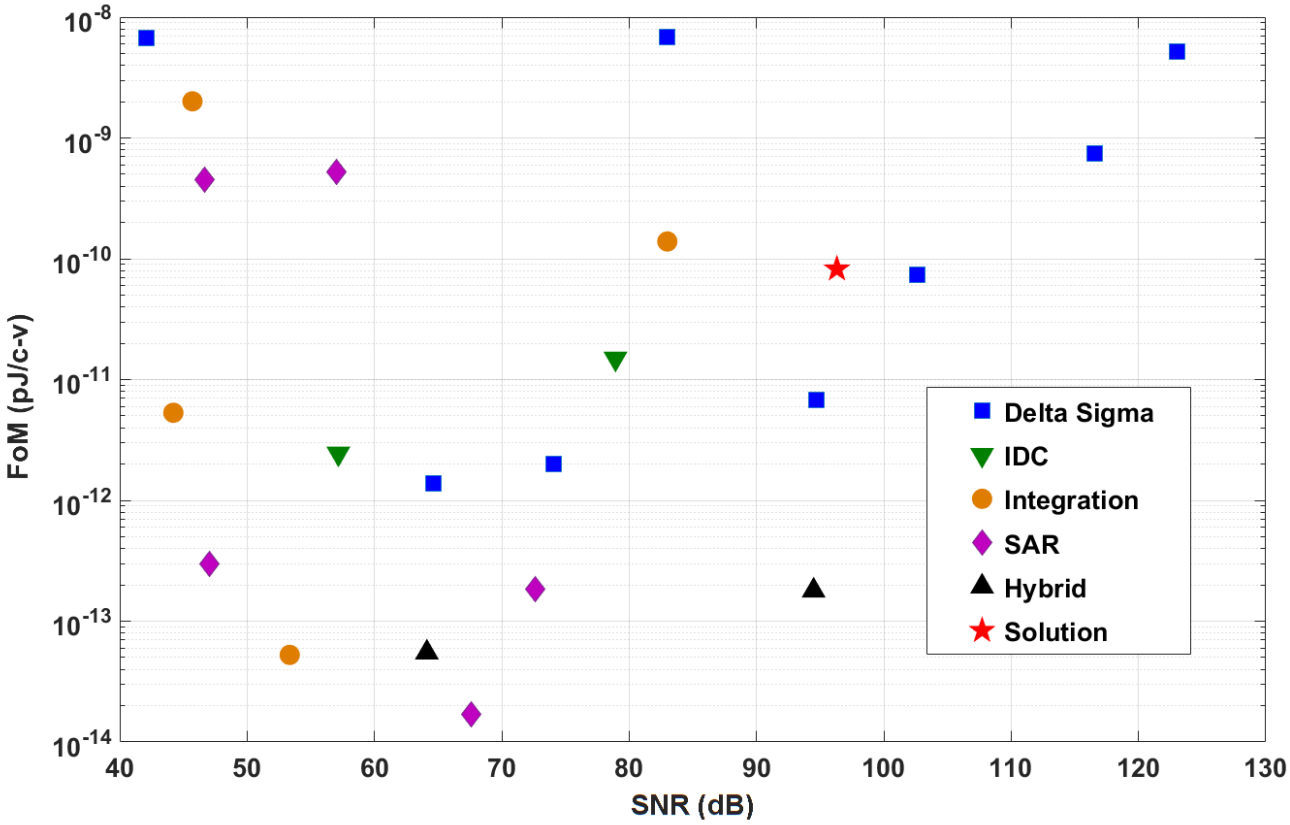

Figure 5-10 State-of-the-Art plot. Figure of Merit (FoM) vs Resolution

In this scenario, the proposed CDC that works in the time domain using a hybrid architecture offers a power efficient solution using very simple and robust implementation. In addition, its digital control gives an easy scalability and because of that, the solution can be adapted to different sensors just by a digital configuration. The topology presented is an efficient solution for the applications mentioned inside the IoT market. Thanks to the time domain conversion this topology doesn´t suffer from reduction of the voltage supply which is one of the new main constrains for IoT applications. This feature plus its robustness, make the prototype presented in this work a good solution for high resolution demanded CDCs in the low frequency domain.

5.5. Conclusion

The measurements presented in this chapter have proven the efficiency of the prototype and its possibilities to become a CDC used in many applications of IoT market.

Resolution measurements have proved that resolution obtained follows the resolution expected in equation (12). Only 2.5 dB is the difference between theory and experimental results. This is easy to explain taking into account the flat part of the FFT in the low frequency range. The noise floor due the non-idealities of the front-end circuit is present. However, the design has not much room of improvement, only 2.5 dB.

Measurements in the whole range of input capacitance have shown a good level of accuracy for differential measurements. To give a constant resolution in the whole range of the application was one of the main concerns of this application. Differential measurements in continuous time mode have make possible to detect minimum variations of pressure in different parts of the transfer function.

The analysis against temperature show that the architecture is able to deal with a wide range of temperature. The absolute resolution between different temperatures (and same input signal) is degraded to 11 bits. However differential resolution stays constant with temperature. This feature gives the possibility of digital calibration.

Environmental readout circuits will be directly affected by ambient temperature, end therefore is important to verify that the performances are the same in all the conditions. However, if a calibration can be done by an external temperature sensor, the resolution must be independent from temperature tolerances to keep the performances.

The solution presented has similar performance as classic ΔΣ modulators with the advantage of been more flexible and scalable to low voltage supply technologies.

Chapter 6.

Conclusions

In this final chapter we will present the conclusions and contributions of this research based on the objectives exposed at the beginning. Also, some inputs for future researching activity will be pointed out.

6.1. Conclusions

After all the research and development done on this work, this are the main conclusions that can be delivered:

- A new CDC architecture has been developed. The work done in this thesis proves that the CDC using a Self-Compensated DS is a candidate inside the hybrid topologies used for applications in the environmental sensing. The simplicity of the architecture, one-bit circuitry, robustness performance and power consumption are the main characteristics that proves the effectiveness of the architecture.
- The performances already mentioned can be achieved by a proper design and connection between the sensor and the front-end of the CDC. The synchronization of the modulation of the MEMS with the time conversion of

the DS was one of the sensitive issues. A proper configuration for modulation frequency and circuit topology has produced the desire results keeping the noise contribution under the desired values.

- Optimized design in 130-nm CMOS technology of analog blocks have been presented as the main responsible of the signal integrity. The topologies selected for the amplifiers and loop architecture are good candidates as results show. A good tradeoff between power consumption of the analog amplifiers and the resolution has been achieved.
- The solution performed in this work has been compared with the SoA. The conclusion out of this comparison is that the topology is a good candidate to be one of the main CDC topologies used in the future for IoT applications. The robustness, the power consumption and the scalability to low voltage technologies gives some advantages compare to the other topologies.
- Self-Compensated architecture have been proved to be a very good type of conversion for DS topologies. Its oscillation at the end of the conversion have been proved to deal with leakage problems of the previous solution (Integrating DS) reducing the digital logic needed for this issue. Also, because of the oscillation, the flicker contribution from the feedback circuitry is reduced. The oscillation at clock frequency of the feedback loop when the input signal is small, contributes to alleviate the contribution from flicker noise making the SNR higher than the Integrating DS in the same conditions. Also, the Self-Compensated architecture plus differential topology and chopping in the integration stage have been proving to be a good architecture to eliminate the offset error and therefore been a very good architecture for differential resolution giving in this application a precision of 1 Pa between two consecutive measurements.

6.2. Contributions

In the next section I will short the contributions that have been made related with their chapters.

The contributions in Chapter 3 are the following:

- Proposal of a front-end circuit based on AC-bridge and voltage amplifier for CDCs that work in the continuous time. Comparison with other candidate topologies have been presented showing the results defendant on parasitic capacitance and the key factor of each topology. Figure 3-4 proves that the performances of an AC-bridge topology can be as good as CDS circuitry for low parasitic capacitance.
- Proposal of a new topology of conversion using the DS principle that gives first order noise-shaping behavior with no extra circuitry for keeping the NTF of the transfer function. Based on the self-oscillated, behavior equations of the transfer function are presented. An explanation of the transfer function compensation for different possible residual values (odd and even number in the quantification process) is demonstrated. Also transfer function of the topology is presented. It presents a linear behavior with no issues in the weight of digital values around zero. Again, without any extra digital logic.

The contributions in Chapter 4 are the following

- Analysis of the physical behavior of a pressure MEMS for readout. Theoretical behavior of the sensor has been study and considered to create a proper architecture at system level for signal processing. We use signal modulation to take out the value from MEMS capacitors removing the offset error and dealing with the second order response of the sensor.

- Application of the CDC composed by AC-bridge front-end and Self-Compensated DS converter architectures. A new approach for sensing activity is provided.
- Proposal of synchronization between modulated front-end circuit and a Self-Compensated DS converter. Time table are presented to demonstrate the efficient timing for this conversion. Synchronized chopping in both blocks of the CDC is presented as an efficient technic for removing the low-bandwidth noise contributions.

The contributions of Chapter 5 are the following:

- The results of a CDC based on Self-Compensated DS converter implemented in 130-nm CMOS technology are presented. The measurements show a SNR of 103.9 dB (17 bits of ENOB) considering a 50 Hz of BW. Giving a constant resolution for differential measurements in the whole dynamic-range of the application. The power consumption is 220 μW with a 1.5 V supply.
- A temperature analysis indicates that the resolution of the same input value against a temperature range of 120 ˚C is degraded to 11 bits of resolution due the non-ideal behavior of the MEMS and CDC. However, the differential resolution keeps constant making possible the digital calibration with external temperature sensor.
- Considering the resolution obtained and compared with the other publications for same range of applications, our design shows a comparable performance with ΔΣ topologies. However, the solution is more flexible to be adapted to different MEMS interfaces. Also, regarding the evolution of the CMOS technologies used. The conversion in time domain of our architecture gives a principal advantage against classic ΔΣ.

6.3. Future work

After the work, there are some pending actions recommend to prove and to improve the Self-Compensated DS CDC for IoT applications:

- The topology presented in this work has been proved against one simple MEMS sensor. In order to confirm its flexibility to be connected to multi-sensor interfaces a prototype in these conditions need to be tested. To be able to deal with this modification more programmability in the time conversion will need to be done to be able to adapt to different full-scales.
- In order to improve the power consumption and be more competitive against other solutions, an architecture without the front-end amplification can be developed. This work is already the main topic of a new thesis that already has presented promising performances in [63].
- A monolithic solution can create a new step of resolution reducing the non-ideal effects that comes out from the parasitic capacitances and difference in mechanical or thermal stress of the devices. This feature plus the multi sensing interface will need a big amount of research activity that can lead with a new generation of sensing solution in one package.
- A MASH architecture can be study more in detail to improve the order in noise-shaping by adding another block that also works in the time domain and has a low power consumption (A VCO). A brief study of this architecture has been also done during this thesis, but its performances haven´t been tested on silicon.

Conclusiones

Para concluir, en este capítulo final presentaremos las conclusiones y contribuciones de esta investigación en función de los objetivos expuestos al principio. Además, se señalarán algunas propuestas para futuras actividades de investigación.

Conclusiones

Después de toda la investigación y el desarrollo realizado en este trabajo, estas son las principales conclusiones que se pueden sacar de este trabajo:

- Se ha desarrollado una nueva arquitectura de CDC para las aplicaciones en IoT. El trabajo realizado en esta tesis ha sido suficiente para demostrar que el CDC que utiliza una topología de doble-rampa *Self-Compensated* es un candidato dentro de las topologías híbridas utilizadas para aplicaciones de sensado ambiental. La simplicidad de la arquitectura, sus bloques de circuitos de un bit, la robustez y el bajo consumo de potencia son las principales características que demuestran la eficacia de la arquitectura.
- Las acciones ya mencionadas se pueden lograr mediante un diseño y una conexión adecuados entre el sensor y el circuito de sensado del CDC. La sincronización de la señal de modulación de los MEMS con la conversión en el domino del tiempo realizada por la topología de doble-rampa es uno de los temas más delicados a tener en cuenta a la hora de realizar este tipo de arquitecturas. Una buena sincronización entre la señal de modulación y

la que controla la topología del circuito ha producido los resultados deseados manteniendo el ruido por debajo de los valores deseados.

- Se ha presentado el diseño optimizado en 130-nm con tecnología CMOS de bloques analógicos como el principal responsable de la integridad de la señal. Las topologías seleccionadas para los amplificadores y la arquitectura de bucle han demostrado ser buenos candidatos debido a los resultados obtenidos. Se ha logrado un buen balance entre el consumo de potencia de los amplificadores analógicos y la resolución.
- Las prestaciones obtenidas en este trabajo se han comparado con el SoA. La conclusión de esta comparación es que la topología es un buen candidato para ser una de las principales topologías de CDC utilizadas en el futuro para aplicaciones de IoT. La robustez, el consumo de potencia y la escalabilidad de las tecnologías de baja tensión ofrecen algunas ventajas con las demás topologías expuestas.
- La arquitectura *Self-Compensated* ha demostrado ser un muy buen tipo de conversión para las topologías de doble-rampa. Se ha comprobado que su oscilación al final de la conversión es capaz de solucionar los problemas de corrientes de fugas detectados en topologías anteriores (*Integrating DS*) reduciendo la lógica digital necesaria para solucionar este problema. Además, como consecuencia de la oscilación, se reduce la contribución del ruido de baja frecuencia o ruido *flicker* del circuito de realimentación. La oscilación a la frecuencia del reloj del circuito de realimentación cuando la señal de entrada es pequeña, contribuye a aliviar la contribución del ruido *flicker* haciendo que la relación señal ruido sea más alta que la solución anterior en las mismas condiciones. Además, la arquitectura *Self-Compensated* además de una topología diferencial y el uso de *chopping* han demostrado ser una buena arquitectura para eliminar el error de *offset* y, siendo, por lo tanto, una muy buena arquitectura para resolución

diferencial, dando en esta aplicación una precisión de 1 Pa entre dos medidas consecutivas.

Contribuciones

En la siguiente sección voy a abreviar las contribuciones que se han hecho relacionadas con sus capítulos.

Las contribuciones en el Capítulo 3 son las siguientes:

- Propuesta de un circuito de sensado basado en puente de corriente alterna y un amplificador de voltaje para CDCs que funcionan en tiempo continuo. Se ha presentado una comparación con otras topologías candidatas y se muestran los resultados obtenidos en función de la capacidad parásita y el factor clave de cada topología. La Figure 3-4 demuestra que el rendimiento de una topología de puente de corriente alterna puede ser tan bueno como el de los circuitos de CDS para baja capacidad parásita.
- Propuesta de una nueva topología de conversión utilizando el principio doble-rampa que es capaz de dar un comportamiento de conformado del ruido de primer orden sin circuitos adicionales para mantener la NTF de la función de transferencia. En base a la topología *Self-Compensated,* se presentan las ecuaciones de comportamiento de la función de transferencia. Se demuestra una explicación de la compensación de la función de transferencia para diferentes valores residuales posibles (número impar y par en el proceso de cuantificación). También se presenta la función de transferencia de la topología. Presenta un comportamiento lineal sin problemas en el peso de los valores digitales alrededor de cero. De nuevo, sin ninguna lógica digital adicional.

Las contribuciones en el Capítulo 4 son las siguientes:

- Análisis del comportamiento físico de un sensor MEMS de presión. El comportamiento teórico del sensor se ha estudiado y tenido en cuenta para crear una arquitectura adecuada a nivel del sistema que permita un buen procesamiento de la señal. Usamos la modulación de la señal para extraer el valor de los condensadores MEMS eliminando el error de *offset* y minimizando el efecto de respuesta a una entrada escalón del sensor.
- Aplicación del CDC compuesto por arquitecturas de convertidor *Self-Compensated* y de puente de corriente alterna. Se proporciona una nueva topología para la actividad de sensado.
- Propuesta de sincronización entre el circuito de sensado modulado y un convertidor DS *Self-Compensated*. La tabla de tiempos se presenta para demostrar la sincronización eficiente para esta conversión. El *chopping* sincronizado en ambos bloques del CDC se presenta como una técnica eficiente para eliminar las contribuciones de ruido de bajo ancho de banda.

Las contribuciones del Capítulo 5 son las siguientes:

- Se presentan los resultados de un CDC basado en el convertidor *Self-Compensated* doble rampa implementado en la tecnología CMOS de 130-nm. Las mediciones muestran una SNR de 103.9 dB (17 bits de ENOB) considerando 50 Hz de BW. El prototipo es capaz de dar una resolución constante para mediciones diferenciales en todo el rango dinámico de la aplicación. El consumo de energía es de 220 μW con un suministro de 1.5 V.
- El análisis de temperatura indica que la resolución para el mismo valor de entrada frente a un rango de temperatura de 120 ˚C se degrada a 11 bits de resolución debido al comportamiento no ideal del MEMS y del CDC. Sin embargo, la resolución diferencial se mantiene constante haciendo posible la calibración digital con sensor de temperatura externo.

- Teniendo en cuenta la resolución obtenida y comparada con otras publicaciones para la misma gama de aplicaciones, nuestro diseño muestra un rendimiento similar con un FoM más pequeña.

Trabajo futuro

Después del trabajo, hay algunas acciones pendientes que se recomiendan para verificar y mejorar el CDC *Self-Compensated* doble-rampa para aplicaciones de IoT:

- La topología presentada en este trabajo ha sido probada contra un simple sensor MEMS. Para confirmar su flexibilidad para conectarse a interfaces multi-sensor, es necesario probar un prototipo en estas condiciones. Para poder hacer frente a esta modificación, se necesitará hacer más programabilidad en la conversión de tiempo para poder adaptarse a diferentes escalas de entrada.
- Para mejorar el consumo de energía y ser más eficiente aun en comparativa frente a otras soluciones, se puede desarrollar una arquitectura sin circuito de acondicionamiento. Este trabajo ya es el tema principal de una nueva tesis que ya ha presentado actuaciones prometedoras en [63].
- Una solución monolítica puede crear un nuevo paso de resolución que reduzca los efectos de las no-ideales que surgen de las capacidades parásitas y la diferencia en el estrés mecánico o térmico de los dispositivos. Esta característica más la interfaz de detección múltiple necesitarán una gran cantidad de actividad de investigación que puede conducir con una nueva generación de solución de detección en un solo chip.
- Se puede estudiar más detalladamente una arquitectura MASH para mejorar el orden en la configuración del ruido agregando otro bloque que también funcione en el dominio del tiempo y tenga un bajo consumo de energía (con un VCO). Un breve estudio de esta arquitectura también se ha

realizado durante esta tesis, pero sus actuaciones no han sido probadas en silicio.

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