TESIS DOCTORAL

Oversampled Analog-To-Digital Converter Architectures Based On Pulse Frequency Modulation

by

Eric Gutiérrez

PhD advisor: Luis Hernández

Electronics Technology Department
Carlos III University of Madrid
Leganés, December 2017

TESIS DOCTORAL

Oversampled Analog-To-Digital Converter Architectures Based On Pulse Frequency Modulation

PhD author: Eric Gutiérrez

PhD advisor: Luis Hernández

Firma del Tribunal Calificador: Firmas

Presidente:

Vocal:

Secretario:

Calificación:

Leganés, de de

To rock music

Acknowledgments

I would like to express my gratitude to all the people who contributed somehow to the research work described in this document.

Thanks to the members of the Electronics Technology Department at Carlos III University who helped me to carry out this work. Many special thanks to my PhD advisor Luis Hernández, who let me work within his research group and devote these years to the field of signal processing and microelectronics. Thanks for the careful review made of this document too.

Thanks to all the members of the Connected Home Division in Intel Austria GmbH in Villach, Austria. I felt very welcome within your group. It was a pleasure learning analog and digital electronics design from you. Big thanks also for the economic support provided during my research period.

Thanks to the partners at university, who made me feel fine during lunch times and pushed me from the beginning to the end of my research period. Thanks to Carlos and Marcos, whose suggestions made this work look better.

As a non-optional social convention, dankzij Pieter Rombouts en de andere leden van de ELIS-groep (circuits en systemen) van de Universiteit Gent. Ik heb veel geleerd tijdens de maanden van mijn verblijf daar.

The most special thank you to my family. Thanks to my parents, who always support me, even when the craziest ideas come to my mind. Thanks to Edgar, who also reviewed this work and provided me very useful comments. I hope we can interchange the roles in the future.

Finally, many many thanks to Martuca, my awake dreamer partner. This work is also yours. Thanks for making me smile at bad moments, encouraging me during the working weekends and taking care of me. Thanks not only for staying with me in Gent, but also in Brussels, Antwerpen, Villers, Mechelen, Leuven, Brugge, Oostende, Ieper and De Panne. I have finished this research work because you spent that time abroad with me. I hope to be able to return you the favor.

Eric Gutiérrez

November 2017

Contents

List of Figures

List of Tables

List of Abbreviations

ADC	analog-to-digital converter
BW	bandwidth
CMOS	complementary metal-oxide-semiconductor
DAC	digital-to-analog converter
DFT	discrete Fourier transform
$\mathbf{f_c}$	carrier frequency
$\mathbf{f_{osc}}$	output oscillation frequency
$\mathbf{f_o}$	rest oscillation frequency
$\mathbf{f_s}$	sampling frequency
FFT	fast Fourier transform
FIFO	first-in first-out
FIR	finite-impulse-response
FM	frequency modulation
GRO	gated-ring oscillator
HD3	third harmonic distortion
$\mathbf{K_{VCO}}$	VCO gain
LDO	low-dropout regulator
LSB	least-significant bit
MASH	multistage noise-shaping
MOSFET	metal-oxide-semiconductor field-effect transistor
NCF	noise cancellation filter
NMOS	N-type metal-oxide-semiconductor
NTF	noise transfer function
OFDM	orthogonal frequency-division multiplexing
OSR	oversampling ratio
PFM	pulse frequency modulation
PFMI	PFM-based integrator
PMOS	P-type metal-oxide-semiconductor
PVT	process-voltage-temperature
PWM	pulse width modulation
QAM	quadrature amplitude modulation
RAM	random access memory
RMS	root mean square

S&H	sample and hold
SNDR	signal-to-noise-and-distortion ratio
SNR	signal-to-noise ratio
SQNR	signal-to-quantization-noise ratio
STF	signal transfer function
$\mathbf{T_s}$	sampling period
VCO	voltage-controlled oscillator

List of Publications and Biography

Papers in Journals

- E. Gutierrez, L. Hernandez, F. Cardes, and P. Rombouts, "A Pulse Frequency Modulation Interpretation of VCOs Enabling VCO-ADC Architectures With Extended Noise Shaping," *IEEE Transactions on Circuits and Systems I: Regular Papers,* to be published. [Online]. Available: http://ieeexplore.ieee.org/document/8016429/

- E. Gutierrez, C. Perez, L. Hernandez, F. Cardes, V. Petrescu, S. Walter, and U. Gaier, "An Inherently Linear VCO-based ADC in 40-nm," submitted to *IEEE Transactions on Circuits and Systems II: Express Briefs.*

- E. Gutierrez, L. Hernandez, and F. Cardes, "VCO-based sturdy MASH ADC architecture," *Electronics Letters,* vol. 53, no. 1, pp. 14-16, 1 5 2017.

- L. Hernandez, and E. Gutierrez, "Analytical Evaluation of VCO-ADC Quantization Noise Spectrum Using Pulse Frequency Modulation," *IEEE Signal Processing Letters,* vol. 22, no. 2, pp. 249-253, Feb. 2015.

- L. Hernandez, and E. Gutierrez, "Oversampled ADC based on pulse frequency modulator and TDC," *Electronics Letters,* vol. 50, no. 7, pp. 498-499, March 27 2014.

Papers in Conference Proceedings

- E. Gutierrez, L. Hernandez, S. Paton, and P. Rombouts, "Optimal NTF zero placement in MASH VCO-ADCs with higher order noise shaping," submitted to *2018 IEEE International Symposium on Circuits and Systems (ISCAS),* to be held in Florence, 2018.

- L. Hernandez, E. Gutierrez, and F. Cardes, "Frequency-encoded integrators applied to filtering and sigma-delta modulation," *2016 IEEE International Symposium on Circuits and Systems (ISCAS),* Montreal, QC, 2016, pp. 478-481.

- E. Gutierrez, and L. Hernandez, "Spectral analysis of multibit VCO-ADCs and PFM-ADCs with sinusoidal inputs," *2015 IEEE International Symposium on Circuits and Systems (ISCAS),* Lisbon, 2015, pp. 1258-1261.

- E. Gutierrez, L. Hernandez, U. Gaier, S. Walter, and L. Zou, "A digitally corrected ADC using a passive pulse frequency modulator," *21st IEEE International Conference on Electronics, Circuits and Systems (ICECS),* Marseille, 2014, pp. 654-657.

- E. Prefasi, E. Gutierrez, L. Hernandez, S. Paton, S. Walter, and U. Gaier, "A 0.03mm^2, 40nm CMOS 1.5GS/s all-digital complementary PWM-GRO," *21st IEEE International Conference on Electronics, Circuits and Systems (ICECS),* Marseille, 2014, pp. 116-119.

- E. Gutierrez, L. Hernandez, U. Gaier, S. Walter, and L. Zou, "A low power and low distortion VCO based ADC using a pulse frequency modulator," *IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS),* College Station, TX, 2014, pp. 487-490.

- E. Gutierrez, L. Hernandez, L. Conesa-Peraleja, J. A. Torreño, S. Paton, "A MASH Oversampled ADC based on Gated Ring Oscillators," *2013 Conference on Design of Circuits and Integrated Systems (DCIS)*, Donostia, 2013.

Other publications of the author

- L. Hernandez, E. Prefasi, S. Paton, and E. Gutierrez, "VCO-ADC Resolution Enhancement Using Maximum Length Sequences," submitted to *2018 IEEE International Symposium on Circuits and Systems (ISCAS),* to be held in Florence, 2018.

- F. Cardes, E. Gutierrez, A. Quintero, C. Buffa, A. Wiesbauer, and L. Hernandez, "A 0.04 mm^2 103 dB-A Dynamic Range 2$^{\text{nd}}$ order VCO-based Audio $\Sigma\Delta$ ADC in 0.13 μm CMOS," submitted to *IEEE Journal of Solid State Circuits.*

- F. Cardes, A. Quintero, E. Gutierrez, C. Buffa, A. Wiesbauer, and L. Hernandez, "SNDR Limits of Oscillator-based Sensor Readout Circuits," submitted to *Sensors.*

- A. Quintero, C. Perez, E. Gutierrez, L. Hernandez, and S. Paton, "Noise-Shaping Time-Interleaved ADC based on a Single Ring Oscillator and a Sampling Array," *IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS),* Boston, MA, 2017.

- L. Conesa-Peraleja, J. A. Torreño, S. Paton, E. Gutierrez, and L. Hernandez, "An Empirical Analysis of PWM Based ADCs," *2013 Conference on Design of Circuits and Integrated Systems (DCIS)*, Donostia, 2013.

- E. Gutierrez-Fernandez, M. Portela-Garcia, C. Lopez-Ongil, and M. Garcia-Valderas, "FPGA-based implementation for steganalysis: A JPEG-compatibility algorithm," *Proceedings of SPIE - The International Society for Optical Engineering*, Grenoble, France, 2013.

Biography

Eric Gutiérrez was born in Móstoles, Spain, in 1989. He obtained the B.S degree in electrical engineering and the M.S. degree in advanced electronic systems from Carlos III University of Madrid, Spain, in 2012 and 2014, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering. He is also a teaching assistant in the Electronics Technology Department, at Carlos III University of Madrid, and an external consultant in Intel Austria GmbH, Villach, Austria. His interests are mixed-signal microelectronics, oversampled data converters and biomedical instrumentation systems.

Abstract

The purpose of this research work is providing new insights in the development of voltage-controlled oscillator based analog-to-digital converters (VCO-based ADCs). Time-encoding based ADCs have become of great interest to the designer community due to the possibility of implementing mostly digital circuits, which are well suited for current deep-submicron CMOS processes. Within this topic, VCO-based ADCs are one of the most promising candidates.

VCO-based ADCs have typically been analyzed considering the output phase of the oscillator as a state variable, similar to the state variables considered in $\Delta\Sigma$ modulation loops. Although this assumption might take us to functional designs (as verified by literature), it does not take into account neither the oscillation parameters of the VCO nor the deterministic nature of quantization noise. To overcome this issue, we propose an interpretation of these type of systems based on the pulse frequency modulation (PFM) theory. This permits us to analytically calculate the quantization noise, in terms of the working parameters of the system. We also propose a linear model that applies to VCO-based systems. Thanks to it, we can determine the different error processes involved in the digitization of the input data, and the performance limitations which these processes direct to. A generic model for any order open-loop VCO-based ADCs is made based on the PFM theory. However, we will see that only the first-order case and a second-order approximation can be implemented in practice. The PFM theory also allows us to propose novel approaches to both single-stage and multistage VCO-based architectures. We describe open-loop architectures such as VCO-based architectures with digital precoding, PFM-based architectures that can be used as efficient ADCs or MASH architectures with optimal noise-transfer-function (NTF) zeros. We also make a first approach to the proposal and analysis of closed-loop architectures. At the same time, we deal with one of the main limitations of VCOs (especially those built with ring oscillators), which is the non-linear voltage-to-frequency relation. In this document, we describe two techniques mitigate this phenomenon.

Firstly, we propose to use a pulse width modulator in front of the VCO. This way, there are only two possible oscillation states. Consequently, the oscillator works linearly. To validate the proposed technique, an experimental prototype was implemented in a 40-nm CMOS process. The chip showed noise problems that degraded the expected resolution, but allowed us to verify that the potential performance was close to the expected one. A potential signal-to-noise-distortion ratio (SNDR) equal to 56 dB was achieved in 20 MHz bandwidth, consuming 2.15 mW with an occupied area equal to 0.03 mm^2. In comparison to other

equivalent systems, the proposed architecture is simpler, while keeping similar power consumption and linearity properties.

Secondly, we used a pulse frequency modulator to implement a second ADC. The proposed architecture is intrinsically linear and uses a digital delay line to increase the resolution of the converter. One experimental prototype was implemented in a 40-nm CMOS process using one of these architectures. Proper results were measured from this prototype. These results allowed us to verify that the PFM-based architecture could be used as an efficient ADC. The measured peak SNDR was equal to 53 dB in 20 MHz bandwidth, consuming 3.5 mW with an occupied area equal to 0.08 mm^2. The architecture shows a great linearity, and in comparison to related work, it consumes less power and occupies similar area.

In general, the theoretical analyses and the architectures proposed in the document are not restricted to any application. Nevertheless, in the case of the experimental chips, the specifications required for these converters were linked to communication applications (e.g. VDSL, VDSL2, or even G.fast), which means medium resolution (9-10 bits), high bandwidth (20 MHz), low power and low area.

Resumen

El propósito del trabajo presentado en este documento es aportar una nueva perspectiva para el diseño de convertidores analógico-digitales basados en osciladores controlados por tensión. Los convertidores analógico-digitales con codificación temporal han llamado la atención durante los últimos años de la comunidad de diseñadores debido a la posibilidad de implementarlos en su gran mayoría con circuitos digitales, los cuales son muy apropiados para los procesos de diseño nanométricos. En este ámbito, los convertidores analógico-digitales basados en osciladores controlados por tensión son uno de los candidatos más prometedores.

Los convertidores analógico-digitales basados en osciladores controlados por tensión han sido típicamente analizados considerando que la fase del oscilador es una variable de estado similar a las que se observan en los moduladores $\Delta\Sigma$. Aunque esta consideración puede llevarnos a diseños funcionales (como se puede apreciar en muchos artículos de la literatura), en ella no se tiene en cuenta ni los parámetros de oscilación ni la naturaleza determinística del ruido de cuantificación. Para solventar esta cuestión, en este documento se propone una interpretación alternativa de este tipo de sistemas haciendo uso de la teoría de la modulación por frecuencia de pulsos. Esto nos permite calcular de forma analítica las ecuaciones que modelan el ruido de cuantificación en función de los parámetros de oscilación. Se propone también un modelo lineal para el análisis de convertidores analógico-digitales basados en osciladores controlados por tensión. Este modelo permite determinar las diferentes fuentes de error que se producen durante el proceso de digitalización de los datos de entrada y las limitaciones que suponen. Un modelo genérico de convertidor de cualquier orden se propone con la ayuda de este modelo. Sin embargo, solo los casos de primer orden y una aproximación al caso de segundo orden se pueden implementar en la práctica. La teoría de la modulación por frecuencia de pulsos también permite nuevas perspectivas para la propuesta y el análisis tanto de arquitecturas de una sola etapa como de arquitecturas de varias etapas construídas con osciladores controlados por tensión. Se proponen y se describen arquitecturas en lazo abierto como son las basadas en osciladores controlador por tensión con moduladores digitales en la etapa de entrada, moduladores por frecuencia de pulsos que se utilizan como convertidores analógico-digitales eficientes o arquitecturas en cascada en las que se optimizan la distribución de los ceros en la función de transferencia del ruido. También se realiza una aproximación a la propuesta y el análisis de arquitecturas en lazo cerrado. Al mismo tiempo, se aborda una de las problemáticas más importantes de los osciladores controlados por tensión (especialmente en aquellos implementados mediante osciladores en anillo): la relación tensión-frecuencia no

lineal que presentan este tipo de circuitos. En el documento, se describen dos técnicas cuyo objetivo es mitigar esta limitación.

La primera técnica de corrección se basa en el uso de un modulador por ancho de pulsos antes del oscilador controlado por tensión. De esta forma, solo existen dos estados de oscilación en el oscilador, se trabaja de forma lineal y no se genera distorsión en los datos de salida. La técnica se propone de forma teórica haciendo uso de la teoría desarrollada previamente. Para llevar a cabo la validación de la propuesta teórica se fabricó un prototipo experimental en un proceso CMOS de 40-nm. El chip mostró problemas de ruido que limitaban la resolución, sin embargo, nos permitió verificar que la resolución ideal que se podría haber obtenido estaba muy cercana a la resolución esperada. Se obtuvo una potencial relación señal-(ruido-distorsión) igual a 56 dB en 20 MHz de ancho de banda, un consumo de 2.15 mW y un área igual a 0.03 mm^2. En comparación con sistemas equivalentes, la arquitectura propuesta es más simple al mismo tiempo que se mantiene el consumo así como la linealidad.

A continuación, se propone la implementación de un convertidor analógico-digital mediante un modulador por frecuencia de pulsos. La arquitectura propuesta es intrínsicamente lineal y hace uso de una línea de retraso digital con el fin de mejorar la resolución del convertidor. Como parte del trabajo experimental, se fabricó otro chip en tecnología CMOS de 40 nm con dicha arquitectura, de la que se obtuvieron resultados notables. Estos resultados permitieron verificar que la arquitectura propuesta, en efecto, podía emplearse como convertidor analógico-digital eficiente. La arquitectura consigue una relación real señal-(ruido-distorsión) igual a 53 dB en 20 MHz de ancho de banda, un consumo de 3.5 mW y un área igual a 0.08 mm^2. Se obtiene una gran linealidad y, en comparación con arquitecturas equivalentes, el consumo es menor mientras que el área ocupada se mantiene similar.

En general, las aportaciones propuestas en este documento se pueden aplicar a cualquier tipo de aplicación, independientemente de los requisitos de resolución, ancho de banda, consumo u área. Sin embargo, en el caso de los prototipos fabricados, las especificaciones se relacionan con el ámbito de las comunicaciones (VDSL, VDSL2, o incluso G.fast), en donde se requiere una resolución media (9-10 bits), alto ancho de banda (20 MHz), manteniendo bajo consumo y baja área ocupada.

Chapter 1

Introduction

1.1 Context and motivation

Nowadays, we live in an interconnected world, characterized by fast communications that allows us to know about what is happening on the other side of the planet just in a second. Actions like taking our cell-phone and checking whether it will rain tomorrow in the town where we live, have become common actions that we usually perform many times during a day. This action, which might appear to be very simple, involves several actors that must work correctly to provide us a proper answer. Just to summarize, we need a weather station located at some point of the town to collect data from the environment; a mathematical model to foresee the upcoming weather, an online server to store the weather forecast data and make them available for the users, and a device to access the server and show the weather forecast to the user. If we distinguish between two type of data: analog data and digital data, there will be several conversions from one type to the other type, and vice versa. Firstly, the data collected from the environment are analog. Then, the data must be converted into digital data if we want them to be processed and stored on a computer. When processed and stored, these data must travel to the device of the user within an analog channel. Finally, it is in the user device where the last analog-to-digital conversion is made. As can be observed, in this simple action, analog-to-digital conversion is required, which makes analog-to-digital converters (ADCs) absolutely required devices in current society. This is only an example, however, analog-to-digital conversion emerges in many of the typical actions we perform in our routine, such as browsing on the Internet, taking a photo, checking our position in the GPS or going to the hospital for a chest X-ray [1]. Consequently, we require ADCs that work fine. Nevertheless, this is not the only requirement. Currently, new communication protocols [2–4] demand high speed communication links, which requires of high speed ADCs. We all know that, due to the complexity of the current cell-phones, battery life is low. Increasing battery life is essential to provide to the user longer autonomy. Then, we will also need of low-power ADCs. In addition, we also live in the world of "minituarization", which is featured by the requirement of manufacturing everything as small as possible [5] and by the very well-known Moore's law [6]. Taking all of these considerations into account, we can conclude that

current society needs high speed, low power and low area ADCs. The resolution will be determined by the application [7]. This requires of a continuous process of proposal, development and enhancement of ADCs in the context of the mixed signal microelectronics.

In the first decade of the current century, the manufacturing of ADCs was made over 0.35 μm and 0.12 μm CMOS processes. Due to the size of transistors and the high supply voltage (between 1.8 V and 3.3 V), the design of high speed and high gain opamps and transconductors was affordable, achieving suitable noise level for different applications [8–14]. Nevertheless, this changed with the development of new deep-submicron CMOS processes (below 65 nm). On the one side, these processes are supplied to voltages below 1.2 V, which reduces voltage headroom of transistors. As threshold voltage has not been reduced at the same ratio of supply voltage, the number of transistors that can be placed in stack configuration is more limited. On the other side, the gain of transistors is reduced and noise and mismatch issues get worse [15–17]. Consequently, analog design becomes more complicated and challenging. In contrast to analog design, digital design takes benefit from deep-submicron processes. The smaller the process we are dealing with, the higher the speed and the lower the area and the power consumption. This takes us to think that the implementation of "more digital" ADC designs is required to fit with the specifications of new CMOS processes. Typically, amplitude encoding was used to make the analog-to-digital conversion, as, for instance, in flash converters [18–20]. However, this technique is not a good choice when using low supply voltage and designing "more digital" architectures. One promising solution is the encoding of the input signal in time events, which is called time encoding [21, 22]. Time encoding is based on the encoding of the information of a signal into time parameters using the propagation delay of a digital inverter [23] or the oscillation frequency of an oscillator [24]. The maximum resolution achieved using this technique is defined by the minimum time delay of a CMOS gate. As the speed of a CMOS gate increases as the size of transistors decreases, time encoding takes benefit from the scaling process of CMOS design technologies. Within these topics, voltage-controlled oscillators (VCOs) are one of the options that might be exploited.

The research work described in this document is focused on the use of VCOs to implement time encoded ADCs. Firstly, we will provide our point of view about how the study of VCO-based systems can be tackled. Secondly, we will propose new implementation approaches derived from the analysis of them. Finally, we will describe some experimental results of the chips manufactured to prove the proposed theory. To be more specific, the implemented designs are specially oriented to accomplish with the requirements of new communication protocols.

1.2 Scope of the dissertation

The goal of the research is providing new insight in the development of VCO-based ADCs, both from a theoretical point of view and from a practical point of view.

From a theoretical point of view, the thesis proposes a new way of analyzing

VCO-based ADCs. The goal is understanding all the processes involved in the analog-to-digital conversion, proposing new VCO-based architectures, techniques to mitigate non-linear VCO's voltage-to-frequency conversion, providing an alternative vision of architectures already analyzed in the literature and obtaining analytical performance equations.

From a practical point of view, we implemented two chips in collaboration with the company Intel Austria GmbH in 40-nm CMOS processes. We worked along with this company in the development of ADCs for communication applications. The requirements for these devices were a medium resolution (around 9-10 bits) and high bandwidth (20 MHz) ADC with low power and low area, implemented with mostly digital architectures.

More specifically, the goals of this work are the following:

- Proposing a new approach to the study of VCO-based ADCs making use of the pulse frequency modulation theory. This will allow us to propose a generic order VCO-based system. All the error processes involved in the conversion will be known, being capable of establishing performance limits for these structures.
- Deriving new structures from this new approach and providing new insights to already known structures. At this point we will deal with a large amount of different structures: open-loop and closed-loop configurations or single stage and multistage structures.
- Obtaining performance equations of these systems.
- Dealing with the non-linearity of VCOs and, based on the theory described in the previous points, proposing new ways of mitigating (even correcting) it.
- Validating the new techniques with experimental prototypes implemented in 40-nm CMOS processes.
- Comparing the obtained results to equivalent published architectures in terms of power, resolution, bandwidth and area.

1.3 Document outline

We have divided the document into three different parts. The first part describes the theoretical analysis of VCO-based ADCs using a pulse frequency modulation interpretation. The second part corresponds to the application of the theory developed in the first part to the proposal and analysis of new VCO-based architectures. Finally, the third part describes the experimental results obtained from two fabricated chips.

Taking this into consideration, the outline of the document is the following:

Part I

Chapter 2 describes the basic notions required to get a good understanding of the topics of the document. We will go from the general to the specific: from the description of an ADC to the different types of ADCs and how a VCO can be used to make an analog-to-digital conversion. All of these descriptions will be supported by references to state-of-the-art chips that will help us to understand the original content provided later on.

Chapter 3 deals with the first block of the dissertation. We propose a pulse frequency modulation framework to analyze and design VCO-based ADCs. We describe a generic model to study VCO-based architectures, the nature of the errors involved in the digitization process and the equations that model these systems. We also point out the new insights provided by this approach, not provided by the conventional approaches.

Part II

In **Chapter 4**, we apply the pulse frequency modulation theory to the proposal and analysis of new single stage architectures. We specially focus on open-loop structures, but we also make a first approach to closed-loop ones. VCO-based architectures with digital precoding are described, along with pulse frequency modulators used as ADCs.

Chapter 5 concentrates on multistage noise shaping architectures. We apply the pulse frequency modulation interpretation to provide our particular vision of these systems. On the other hand, we propose a technique to optimize the noise-transfer-function zeros in low-pass architectures. Finally, a brief description of how multistage architectures can be built with digitally precoded VCOs is made.

Part III

Chapter 6 and **Chapter 7** describe the experimental results of the dissertation, with two prototypes implemented in 40-nm CMOS processes. Whereas the chip of Chapter 6 is a VCO-based ADC with a pulse width modulator in front of the oscillator, the chip of Chapter 7 is a multibit pulse frequency modulator with good linearity properties.

Part IV

Finally, **Chapter 8** concludes the document and provides some guidelines about how the work presented in this document may be extended in the future.

Part I

Theoretical modeling of VCO-based ADCs based on a PFM interpretation

Chapter 2

VCO-based ADCs: From the general to the specific

2.1 Analog-to-digital conversion

Electronics could be defined as the science dealing with the control of the flow of electrical charges in a "smart" way. Currently, electronics is present within our daily life. Listening to music, making the laundry or browsing on the Internet would become impossible activities without electronics. We can distinguish between two important branches in electronics: analog electronics and digital electronics. Whereas analog electronics deals with physical magnitudes measured and represented by continuous variables, digital electronics deals with binary magnitudes. These branches are not independent of each other. It is sometimes interesting to go from the analog domain to the digital domain, and vice versa. In this document, we are specially interested on the analog-to-digital sense of the flow.

The electronics device that makes the analog-to-digital conversion is named analog-to-digital converter (ADC). Although there are several types of ADCs, a first approach to understand the generic ADC architecture can be made if we consider the diagram block of Fig. 2.1. This diagram is composed of several blocks. Firstly, we have an anti-aliasing filter. The purpose of the anti-aliasing filter is removing any high-frequency component in the input signal $x(t)$ in order to avoid aliasing when sampling. It is typically a low-pass filter. Then, we have a sample and hold (S&H) circuit. Its purpose is holding the value of the analog signal to allow the quantization process when discrete time circuits are used. Hereafter, we have the quantizer block, whose goal is making the analog-to-digital conversion, i.e. assigning a binary value to the continuous value coming from the S&H. Quantization process usually involves sampling afterwards, with a certain sampling frequency (f_s). Finally, after the quantization process, the output data must be digitally processed to prepare them for their later use. If the ADC output data are oversampled, one of the digital operations to perform is the decimation. The decimation is needed to decrease the sampling rate of the output data to the Nyquist rate. The diagram of Fig.2.1 is generic and all the blocks do not have to be strictly present in all the possible ADC architectures.

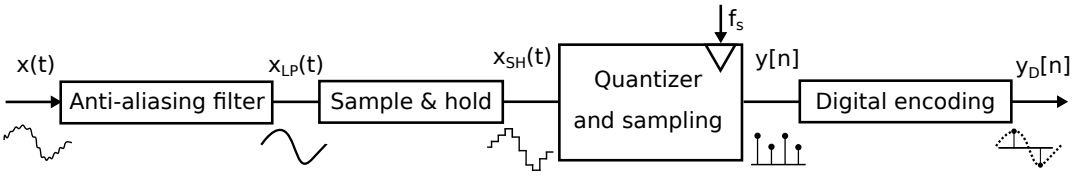


Figure 2.1: Generic ADC diagram block.

Nevertheless, it is a good way to understand all the processes involved in an analog-to-digital conversion.

Depending on the taken view, we can classify the ADCs in different ways. For instance, if we look at the nature of the input signal of the quantizer, this signal can be a continuous wave (with no S&H) or a discrete value hold for a period of time (with S&H). Accordingly, we will distinguish between continuous and discrete time ADCs, respectively. Furthermore, if we take into account the relationship between the bandwidth (BW), which is the band of interest of the converter, and the f_s, we will distinguish between two types of ADCs. Firstly, those in which the following expression will be accomplished:

$$f_s = 2 \cdot \mathrm{BW}. \tag{2.1}$$

They are called Nyquist converters. Examples of Nyquist converters are flash, pipeline or succesive approximation ADCs [25].

Secondly, there will be converters in which f_s is higher than twice the BW:

$$f_s > 2 \cdot \mathrm{BW} \tag{2.2}$$

These converters are called oversampled converters, such as $\Delta\Sigma$-modulation based ADCs [26]. The practical advantage of oversampled ADCs is that they are able to provide much higher resolution than Nyquist converters. To understand the fundamentals of this affirmation, we need to know basic foundations about quantization theory. These foundations are described below.

The quantization process can be defined as the correspondence of a real valued number (which is, in our case, the instantaneous value of an analog signal) to a set of discrete values (in our case, a digital signal). Fig. 2.2 shows an example of the transfer curve for a 3-bit quantizer. Considering a dimensionless input analog signal that takes values between -0.5 and 0.5, these values will be assigned to eight possible digital codes according to the transfer curve of Fig.2.2[1]. If we supposed an ideal analog-to-digital conversion with a set of infinite digital possible codes in the output, the transfer curve would follow the dashed line of Fig.2.2. However, the number of available digital values is limited in reality, so any analog-to-digital conversion always implies an error in the conversion. This error is named quantization error. In the particular case of Fig.2.2, the quantization error can be represented as a triangular wave with values between $-V_{\mathrm{LSB}}/2$ and $V_{\mathrm{LSB}}/2$, with

[1]Note that for values tending to 0.5, we will need an extra bit according to Fig. 2.2. For the moment, we will assume that we have that extra bit. In practice there is no extra bit and it is said that the quantizer is overloaded.

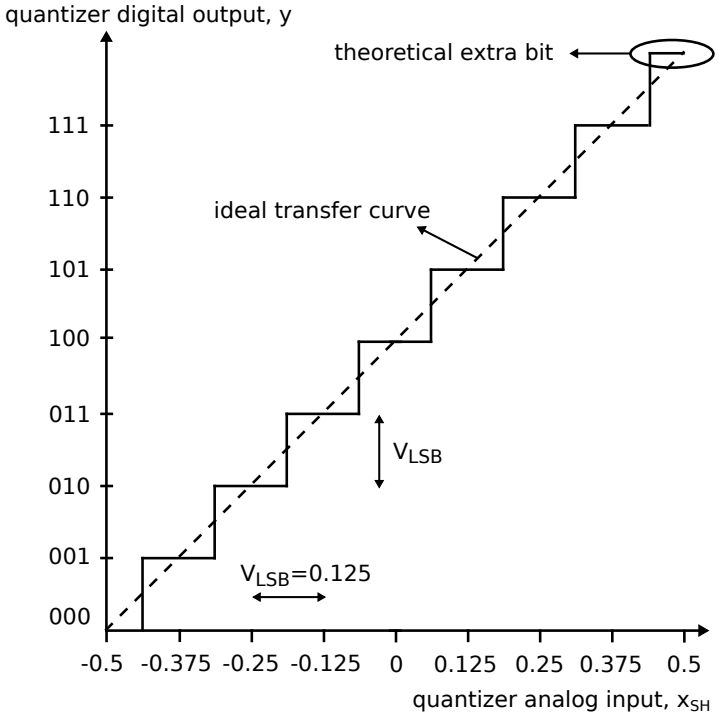


Figure 2.2: Transfer function of a 3-bit quantizer.

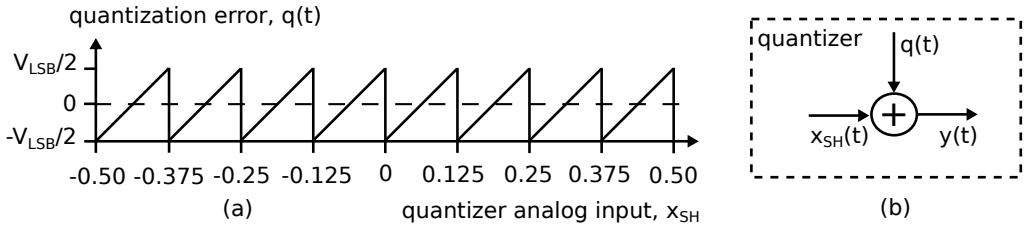


Figure 2.3: (a) Quantization error associated to the quantizer of Fig. 2.2, and (b) linear model of the quantization process.

V_{LSB} (least-significant bit (LSB)) being the equivalent analog voltage difference between one digital word and the next one. V_{LSB} follows:

$$V_{\mathrm{LSB}} = \frac{x_{\mathrm{SH,max}} - x_{\mathrm{SH,min}}}{2^N} = \frac{0.5 - (-0.5)}{2^N} = \frac{1}{2^N}, \tag{2.3}$$

where N is the number of bits of the quantizer. In our particular case, $N = 3$, so that $V_{\mathrm{LSB}} = 0.125$. The quantization error signal is plotted in Fig.2.3(a) in function of the analog input signal [27, 28]. The reader might have noticed that the quantization process can be considered a linear operation in which an analog error signal $q(t)$ is added to the input signal of the quantizer $x_{\mathrm{SH}}(t)$ to generate the quantized output signal $y(t)$. This equivalence is shown in Fig. 2.3(b).

If we could estimate the power of the quantization error $q(t)$, we would be able to calculate the signal-to-quantization-noise ratio (SQNR) and, as there is

no distortion, also the SNDR [2]. As was shown in Fig. 2.3(a), $q(t)$ depends on $x_{\mathrm{SH}}(t)$. Therefore, it is a deterministic signal and we can calculate its root mean square (RMS) voltage. This value will be defined as follows:

$$V_q^{\mathrm{rms}} = \frac{1}{\sqrt{12}} \cdot \frac{1}{2^N}. \tag{2.4}$$

Nevertheless, the waveform of $q(t)$ depicted in Fig. 2.3(a) will only show that shape if $x_{\mathrm{SH}}(t)$ is a ramp signal that goes from -0.5 to 0.5. In a general case, the input signal of the quantizer usually has no periodic pattern and the relationship between it and the quantization error is not always so clear than in Fig. 2.3. Consequently, to deal with a more generic case, it is typically assumed that the quantization error does not depend on the input quantizer signal and is a random signal with value range between $-V_{\mathrm{LSB}}/2$ and $V_{\mathrm{LSB}}/2$. If we suppose this, V_q^{rms} will remain as in (2.4) [25].

We also suppose that $x_{\mathrm{SH}}(t)$ is a sinusoidal wave with frequency f_{x}, as is usually done for ADCs analyses:

$$x_{\mathrm{SH}}(t) = 0.5 \sin(2\pi f_{\mathrm{x}} t), \tag{2.5}$$

where:

$$V_{x_{\mathrm{SH}}}^{\mathrm{rms}} = \frac{\sqrt{2}}{4}. \tag{2.6}$$

$$\tag{2.7}$$

Now, the SNDR can be calculated as:

$$\mathrm{SNDR} = 20 \log_{10} \frac{V_{x_{\mathrm{SH}}}^{\mathrm{rms}}}{V_q^{\mathrm{rms}}} = 6.02N + 1.76. \tag{2.8}$$

Equation (2.8) gives us the best possible SNDR for a certain ADC with an N-bit quantizer. It should be noted that (2.8) was calculated for an input signal with the highest amplitude possible. If we decrease the amplitude of the input signal, it is obvious that the power of the input signal will also decrease; however, the power of the quantization error will remain (remember that we had supposed that the quantization error did not depend on the input signal). Consequently, the SNDR will decrease too.

As $q(t)$ is assumed to be a random signal, the spectral power density will be uniformly distributed in the spectral range between -$\mathrm{f_s}/2$ and $\mathrm{f_s}/2$ when sampling in the ADC. As a result, the power of the quantization noise can be represented as in Fig. 2.4. The power of $q(t)$ (P_{q}) is calculated as follows:

[2] The SQNR is the ratio between the power of $x_{\mathrm{SH}}(t)$ and the power of $q(t)$. When making ADC performance measurements, we usually use the term SNDR, which is the ratio between the power of the input signal and the power of the quantization noise plus the distortion. With the goal of keeping always the same nomenclature (especially in the following chapters), we will use the term SNDR instead of the term SQNR. However, in this section, as there is no distortion, using the SNDR is similar to use the SQNR.

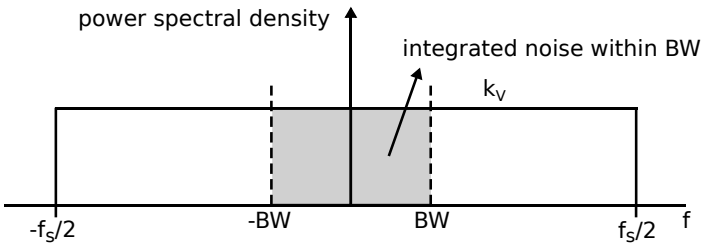


Figure 2.4: Quantization noise power spectral density between $-f_\mathrm{s}/2$ and $f_\mathrm{s}/2$.

$$P_\mathrm{q} = \int_{-\frac{f_\mathrm{s}}{2}}^{\frac{f_\mathrm{s}}{2}} k_\mathrm{V}^2 \cdot df = k_\mathrm{V}^2 \cdot f_\mathrm{s} = \frac{1}{12}\left(\frac{1}{2^\mathrm{N}}\right)^2,$$
$$k_\mathrm{V} = \frac{1}{\sqrt{12}} \cdot \frac{1}{2^\mathrm{N}} \cdot \frac{1}{\sqrt{f_\mathrm{s}}}, \tag{2.9}$$

where k_v is the power at each frequency of the spectrum. Note that, in the case of dealing with Nyquist converters, BW $= f_\mathrm{s}/2$ and all the power between $-f_\mathrm{s}/2$ and $f_\mathrm{s}/2$ is integrated when calculating P_q, leading to (2.8). Therefore, (2.8) only applies to Nyquist converters. The equivalent equation for oversampled converters is a little bit different.

If we observe Fig. 2.4, we might realize why oversampling converters are able to provide us higher SNDR than Nyquist converters for a certain N value. Whereas the BW is equal to $\mathrm{f_s}/2$ for a Nyquist converter as stated above, the BW is much lower than $\mathrm{f_s}/2$ in an oversampled converter, so that only a part of the quantization error power is integrated within the BW (as shown in Fig. 2.4). For an oversampled converter, the RMS voltage of the quantization error is now expressed as:

$$V_q^\mathrm{rms} = \frac{1}{\sqrt{12 \cdot \mathrm{OSR}}} \cdot \frac{1}{2^N}, \tag{2.10}$$

where the oversampling ratio (OSR) is defined as follows:

$$\mathrm{OSR} = \frac{f_\mathrm{s}}{2 \cdot \mathrm{BW}}. \tag{2.11}$$

The OSR establishes the ratio between the sampling frequency f_s and the BW. It is a very common parameter used when dealing with oversampled converters.

If we suppose the same input signal as in (2.5), the SNDR will be defined as:

$$\mathrm{SNDR} = 6.02N + 1.76 + 10\log_{10}\mathrm{OSR}, \tag{2.12}$$

where it is clearly visible the resolution improvement due to the oversampling.

This is the main difference between Nyquist and oversampled converters. However, oversampled converters do not take only advantage of oversampling. They often filter the quantization noise in an attempt to reduce the power of the noise that falls into the band of interest. This technique is named $\Delta\Sigma$ modulation and the converters which perform it are named $\Delta\Sigma$ modulators [26, 29–31]. They

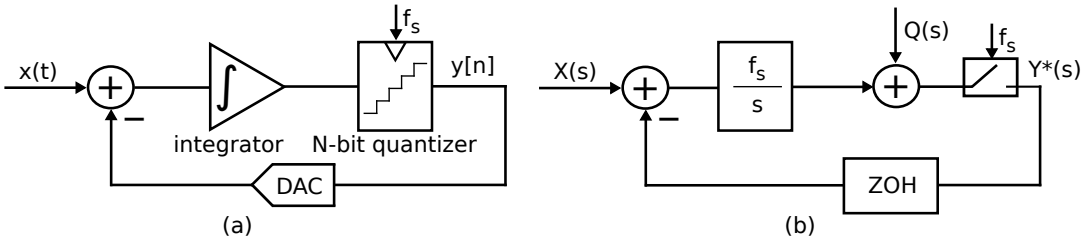


Figure 2.5: (a) The simplest way of building a continuous-time $\Delta\Sigma$ modulator, and (b) the equivalent linear model.

often shape the quantization noise by high-pass filtering, letting the resolution of the converter become even higher. As far as the ADCs we propose in this document make use of this technique, we will focus on the fundamentals of $\Delta\Sigma$ modulation in the next section.

2.2 $\Delta\Sigma$ modulation

In the previous section, we have seen that the sampling frequency in oversampled converters is higher than 2·BW in order to improve the resolution of the converter. Oversampled converters often perform a technique called $\Delta\Sigma$ modulation to enhance the resolution even more. $\Delta\Sigma$ modulation can be applied to either discrete or continuous systems. The work described in this document is focused on continuous-time systems, that's why we will explain $\Delta\Sigma$ modulation from a continuous-time point of view. However, if we dealt with discrete systems the explanations would remain valid and would be quite similar.

The simplest architecture for a continuous-time $\Delta\Sigma$ modulator is depicted in Fig 2.5(a). It is composed of an integrator, a N-bit quantizer and a negative feedback path that goes from the output of the quantizer $y[n]$ to the input signal $x(t)$ through a digital-to-analog converter (DAC). If we consider the Laplace representation of an integrator, a zero-order hold (ZOH) in the feedback path, and the linear model of a quantizer, shown in the previous section, Fig. 2.5(a) will turn into Fig. 2.5(b). If we calculate the expression for $Y^*(s)$ and make use of the properties of the starred operator (*) [32], $Y^*(s)$ will be defined as[3]:

$$Y^*(s) \approx \mathrm{STF}(z) \cdot X^*(s) + \mathrm{NTF}(z) \cdot Q^*(s) = \\ X^*(s) + \left(1 - z^{-1}\right) \cdot Q^*(s), \tag{2.13}$$

where $z = e^{sT_s}$, with the sampling period (T_s).

On the one hand, the signal transfer function (STF) is a unitary gain, this means that $X(s)$ will get through the system with no changes and it will appear in $Y^*(s)$ as it is. On the other hand, the noise transfer function (NTF) filters the quantization error with a high-pass filter. Considering $Q(s)$ as white noise, the

[3]The impulse-invariant discretization method was used to estimate this equation, that's the reason why (2.13) is an approximation. To keep a proper approximation, we always suppose that we are dealing with high OSR. Furthermore, all the gains were normalized to one.

power of the quantization error will be attenuated at low frequencies. If we deal with a low pass ADCs, as here, the resolution of the converter will be improved. To estimate a new expression for the SNDR, firstly, we take the NTF and go from the discrete domain to the continuous domain with the equivalence between z and s variables defined previously:

$$\mathrm{NTF}(s) = 2\sin\left(\pi\frac{f}{f_\mathrm{s}}\right), \quad f \in [0, f_\mathrm{s}/2]\,. \tag{2.14}$$

Secondly, we will calculate the power of the quantization noise in BW:

$$P_\mathrm{q} = \int_{-\mathrm{BW}}^{\mathrm{BW}} \frac{1}{12f_\mathrm{s}}\left(\frac{1}{2^N}\right)^2 \cdot 4\sin^2\left(\pi\frac{f}{f_\mathrm{s}}\right) df. \tag{2.15}$$

If $f_\mathrm{s} \gg \mathrm{BW}$, (2.15) can be approximated to:

$$P_\mathrm{q} = \frac{\pi^2}{36}\left(\frac{1}{2^N}\right)^2 \frac{1}{\mathrm{OSR}^3}. \tag{2.16}$$

Finally, keeping the similar power for the input signal as above, the SNDR will be defined as:

$$\mathrm{SNDR} = 6.02N + 1.76 - 5.17 + 30\log_{10}\mathrm{OSR}. \tag{2.17}$$

It can be checked that (2.17) takes us to higher SNDR than (2.8) for OSR$\gg$1.

The architecture of Fig. 2.5 depicts the conventional first-order continuous-time ΔΣ modulator, which is the simplest one. Nevertheless, this architecture can be turned into more complex architectures with improved resolution. For instance, the architecture of Fig. 2.6 is a second-order continuous-time ΔΣ modulator. The NTF for this architecture is a second-order high-pass filter, which implies that the in-band quantization noise is more attenuated than in the first-order architecture. Consequently, the resolution will be enhanced even more. Following the same approach as before, an equation for the SNDR can be also estimated for the second-order case:

$$\mathrm{SNDR} = 6.02N + 1.76 - 12.90 + 50\log_{10}\mathrm{OSR}. \tag{2.18}$$

One important advantage of continuous-time ΔΣ modulators over discrete-time ones is the inherent anti-aliasing filter they have. Fig. 2.7 shows the diagram for a first-order discrete-time ΔΣ modulator. The transfer functions of this system are exactly (not approximated) what is stated by (2.13). As can be observed, the sampler in this system is placed before the ΔΣ loop (actually, this sampler works as the S&H circuit of Fig. 2.1). Therefore, high frequency components of $X(s)$ must be filtered previously if we want them not to fall into the band of interest. Unlike in the discrete-time case, in the continuous-time case (Fig. 2.5(b)), we have a low-pass filter before the sampling. Consequently, high frequency components of $X(s)$ will be attenuated. This can be extended to all the continuous-time ΔΣ architectures. Due to this, it is typically said that

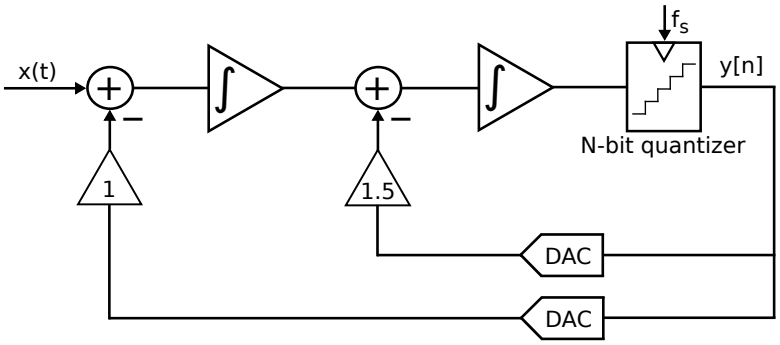


Figure 2.6: Second-order continuous-time $\Delta\Sigma$ modulator architecture.

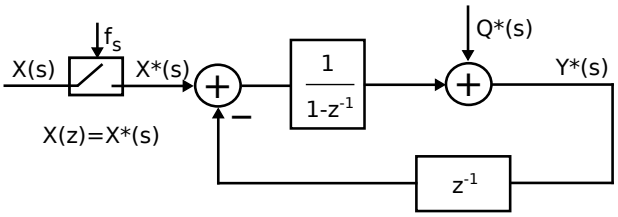


Figure 2.7: First-order discrete-time $\Delta\Sigma$ modulator.

continuous-time $\Delta\Sigma$ modulators have an inherent anti-aliasing filter that might make the anti-aliasing filter of Fig. 2.1 unnecessary.

The architectures proposed in this document have similar performance as $\Delta\Sigma$ modulators in terms of spectral shaping. However, we used VCOs to get that performance, instead of using conventional integrators included into a $\Delta\Sigma$ loop. Next, we will talk about the VCOs and how they can be used to build a noise-shaped oversampled analog-to-digital conversion.

2.3 VCO-based ADCs

The conventional structure of a $\Delta\Sigma$ modulator was presented in the previous section. Mainly, it was explained that the $\Delta\Sigma$ loop shapes the quantization noise to reduce the in-band power. A similar spectral performance can be achieved through the use of VCOs in several types of architectures.

A VCO is a circuit that generates an oscillating signal whose oscillation frequency depends linearly on the input voltage $x(t)$. In this document, we will focus on VCOs with digital output signal. This means that the output signal will be always a 50% duty cycle square signal. The output oscillation frequency (f_{osc}) can be expressed as:

$$f_{\text{osc}}(t) = f_{\text{o}} + K_{\text{VCO}} \cdot x(t), \quad K_{\text{VCO}} \leq f_{\text{o}}, \tag{2.19}$$

where we can distinguish between a rest oscillation frequency (f_o) term and a VCO gain (K_{VCO}) term. The input signal $x(t)$ is considered dimensionless and belonged to the range [-1,1].

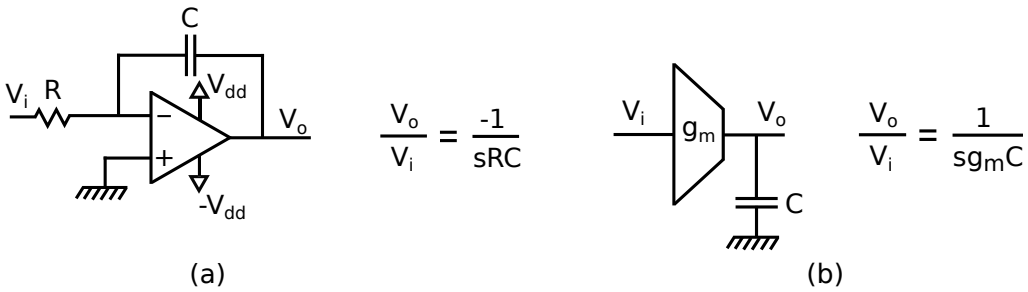


Figure 2.8: (a) Opamp-based integrator, and (b) transconductance-based integrator.

2.3.1 VCO-based integrator

One of the main components in every $\Delta\Sigma$ modulator architecture is the integrator (Fig. 2.6). There are many different ways to implement an integrator, however, not all of them are suitable for all the possible situations. Typically, an analog integrator can be implemented through two ways: using an opamp-based integrator (Fig. 2.8(a)) or a transconductance-based integrator (Fig. 2.8(b)) [33–35]. As can be observed, both of them require analog circuits. The recent development of nanometer CMOS processes has led to major challengues in analog design. On the one hand, narrow-length devices show a high amount of non-desired effects (i.e. hot carrier injection, leakage and mobility effects, etc.) [17]. On the other hand, the threshold voltage has not been reduced at the same rate as the supply voltage. Consequently, transistor voltage headroom is lower and the number of transistors that can be stuck in series is very limited. As a result, analog design becomes difficult. In the opposite situation, digital circuits benefit from this scaling process in terms of area, speed and power consumption. Digital designs are less sensitive to transistor non-desired effects, mismatch phenomena and temperature, which makes them suitable for nanometer architectures [36]. Against this background, the current trend is towards replacing analog architectures by digital ones as far as possible.

If we take this fact into consideration when designing $\Delta\Sigma$ modulators, we should look for a way of implementing digital versions of integrators. At this point, VCOs come into play. If we observe (2.19) and we keep in mind that the phase of a signal is the integral of its frequency, we will get:

$$\theta(t) = 2\pi \int_0^t f_{\text{osc}}(\tau)d\tau = \\ 2\pi f_o t + 2\pi K_{\text{VCO}} \int_0^t x(\tau)d\tau, \tag{2.20}$$

where θ(t) is the phase of the VCO output. We notice that, if we consider the output of the VCO as the phase of the output signal, we will deal with an integrator. In addition, we see that there are no limitations due to components requirements such as the gain of the operational amplifier in opamp-based integrators. Here, if the VCO accomplishes with (2.20), we will have an infinite gain

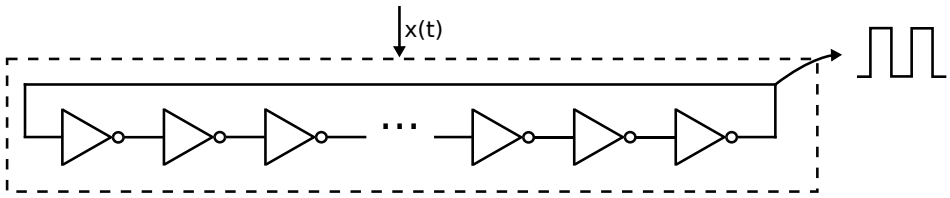


Figure 2.9: Conventional diagram of a ring oscillator.

integrator. Then, using VCOs as integrators looks a potential solution to replace conventional analog integrators.

2.3.2 A digital VCO: the ring oscillator

There are several ways of building VCOs [37–39]. However, we are interested on those that can be implemented with digital circuits to take benefit from the features of new deep-submicron CMOS processes. Due to its digital nature, ring oscillator based VCOs have attracted the interest of the designer community for the last years [24].

A ring oscillator is composed of an odd number of time delay taps connected in a ring configuration. The time delayed by each tap depends on the input of the ring oscillator, so that if we observe the output signal of any tap, we will see an oscillating signal whose oscillation frequency depends on the input signal. Fig. 2.9 shows the simplest circuit for a ring oscillator. The oscillation frequency of the ring oscillator is defined as follows:

$$f_{\text{osc,ring}}(t) = \frac{1}{2NT_{\text{d,tap}}(t)}, \tag{2.21}$$

where N is the number of taps and $T_{\text{d,tap}}(t)$ is the instantaneous delay of each tap. As $T_{\text{d,tap}}(t)$ directly depends on the input signal $x(t)$, $f_{\text{osc, ring}}(t)$ will depend on $x(t)$ as well.

The difference between the various ring oscillators relies on how the delay tap is implemented [39–41] and how the time delayed is controlled.

2.3.3 VCO-based configurations

On the one hand, we have seen that a VCO is able to work as a phase integrator, so that it could be incorporated into $\Delta\Sigma$ architectures that were previously built with the analog architectures shown in Fig. 2.8. On the other hand, we have described how a digital VCO, which are well-suited for current deep-submicron CMOS processes, can be implemented with ring oscillators. Our next step is describing how to build ADCs architectures with VCOs and, especially, with ring oscillators.

There are two kinds of VCO-based configurations: open-loop and closed-loop configurations. Both of these type of configurations will be described next.

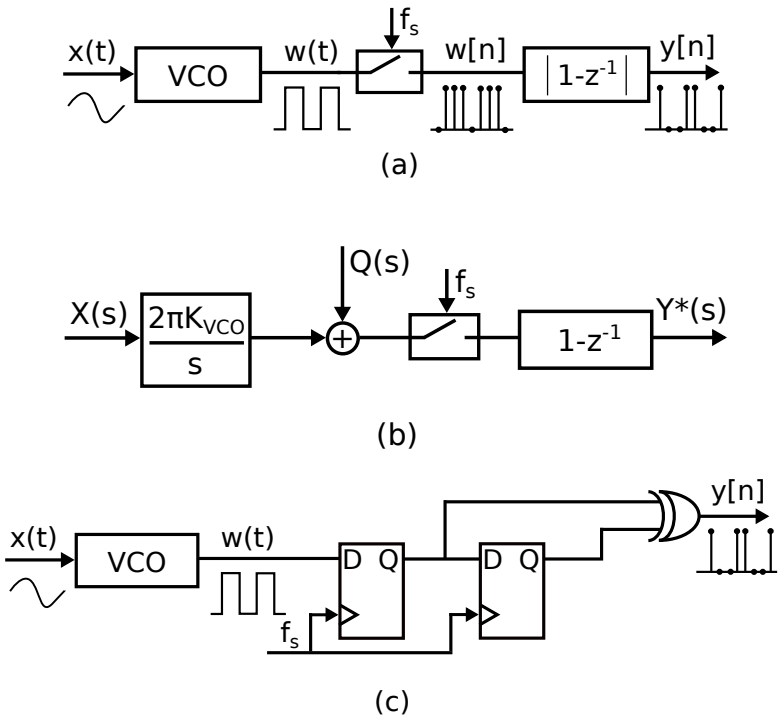


Figure 2.10: (a) Open-loop configuration VCO-based ADC, (b) linear model of the system, and (c) conventional architecture built with flip-flops and XOR gate.

2.3.3.1 Open-loop configuration

The simplest open-loop ADC that may be built with a VCO is depicted in Fig. 2.10(a). In this configuration, the input signal $x(t)$ is directly connected to the VCO. The VCO generates a square digital signal $w(t)$ with an oscillation frequency that follows (2.19). Then, $w(t)$ is sampled and finally is first differentiated to get the output data $y[n]$. If we take into consideration that a VCO is a phase integrator and we omit the term f_{o}, we can build the linear model of Fig. 2.10(b) for the architecture of Fig. 2.10(a)[4] Here, the VCO works both as an integrator and as a quantizer because the output of the VCO is already a digital signal. Signal $Y^*(s)$ can be expressed as follows:

$$Y^*(s) = 2\pi K_{\mathrm{VCO}} \left(\frac{1 - e^{-sT_{\mathrm{s}}}}{s} X(s) \right)^* + (1 - z^{-1}) Q^*(s), \tag{2.22}$$

where $Q^*(s)$ represents the quantization error of the analog-to-digital conversion that takes place in the VCO. Supposing that $f_{\mathrm{x}} << f_{\mathrm{s}}$:

$$Y^*(s) \approx 2\pi K_{\mathrm{VCO}} X^*(s) + (1 - z^{-1}) Q^*(s), \tag{2.23}$$

[4]In this equivalence we have omitted the term f_{o} in order to simplify the explanation and the used model. This term represents an offset term that does not modulate the input signal, so it can be removed from the explanation without any loss of generality.

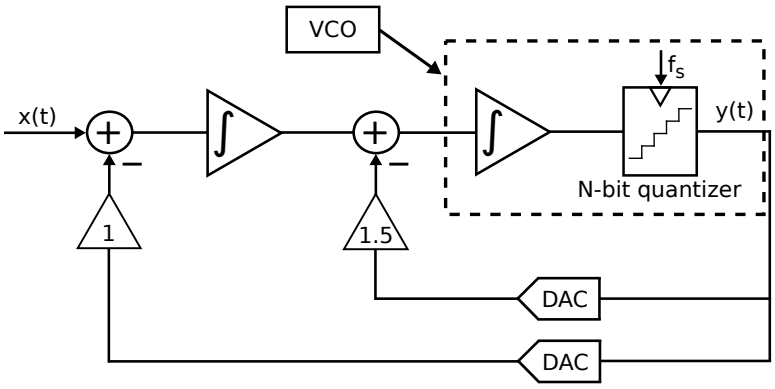


Figure 2.11: Second-order continuous-time $\Delta\Sigma$ modulator with a VCO working as the last integrator and the quantizer.

As can be observed, in terms of the noise, (2.23) is similar to (2.13). Consequently, from a spectral point of view, this architecture is equivalent to a first-order $\Delta\Sigma$ modulator [41–43].

In practice, this architecture is typically implemented as shown in Fig. 2.10(c), which is composed of the VCO and two flip-flops connected in cascade followed by a XOR gate, which makes the first difference [41].[5]

2.3.3.2 Closed-loop configuration

In the previous section, we used a VCO to build a first-order noise-shaped architecture equivalent to a $\Delta\Sigma$ modulator. Nevertheless, it has a different structure as conventional $\Delta\Sigma$ modulators. VCOs can be also used instead of conventional integrators in $\Delta\Sigma$ architectures in order to build high-order noise-shaped architectures. There are several examples of these type of architectures in the literature [44–50]. To illustrate how these architectures are implemented we could, for instance, replace the second integrator and the quantizer of Fig. 2.6 by a VCO as shown in Fig.2.11. This is what was done in [44]. However, not only the last integrator can be replaced. In [47], how to build generic order $\Delta\Sigma$ modulators with only VCO-based integrators was described.

2.3.4 VCO non-linearity

So far, we have seen that VCOs allows us to build architectures with the same performance as $\Delta\Sigma$ modulators. Due to the digital nature of ring oscillator based VCOs, it seems to be a good choice when implementing ADCs with deep-submicron processes. However, some VCO's limitations may degrade severely the

[5]Note that, when going from Fig. 2.10(a) to Fig. 2.10(b), we have omitted the absolute value operation in the first difference. This can be assumed if we only consider the rising edges of the VCO output signal to demodulate the output data. Then, a "strict" matching between Fig. 2.10(a) and Fig. 2.10(b) implies that the oscillation frequency of the equivalent VCO of Fig. 2.10 is twice the oscillation frequency of the VCO of Fig. 2.10(a). At the moment, we suppose that this phenomenon is included into the term K_{VCO} of Fig. 2.10(b).

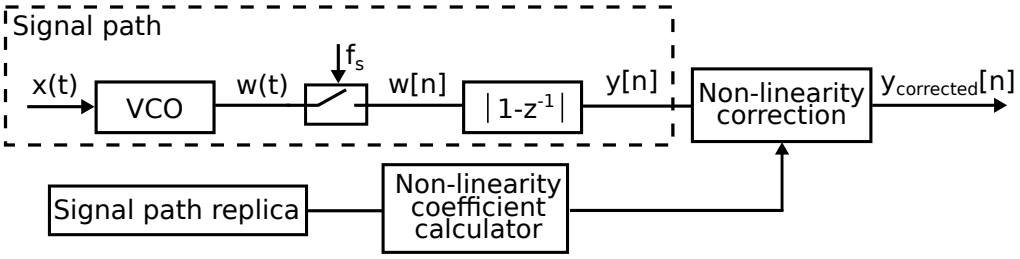


Figure 2.12: VCO linearity correction by means of digital post-processing.

performance of the converter.

The main limitation of VCOs is the non-linear voltage-to-frequency transfer function of the VCO. This phenomenon limits the resolution that can be obtained from a VCO-based ADC due to the distortion that will appear in-band. If we work with high-amplitude signals ($\geq$ 100 mV), for SNDRs higher than 45 dB it will be strictly necessary to add some kind of distortion compensation method. Otherwise, distortion will degrade completely the expected converter resolution.

Several attempts have been made to overcome this issue. Next, we will describe the most relevant methods:

2.3.4.1 Digital calibration

One of the most popular methods to compensate the linearity of a VCO is to place some digital logic in parallel to the ADC, with the purpose of digitally correcting the distortion coming from the VCO [43, 51–53].

In [43] we can find an example of this type of implementations. The architecture proposed in [43] follows the structure shown in Fig. 2.12. This idea is based on the assumption that the distortion that comes from the VCO can be estimated in a deterministic way. If the VCO distortion can be calculated and we know what is the shape of this distortion regardless of the input signal of the system, we will be able to remove it in the digital domain after sampling. To estimate the distortion of the VCO, the signal path through the converter is replicated. Then, the output of this replicated system is measured and the distortion components are estimated through digital circuits (non-linearity coefficient calculator). When they are calculated, they are subtracted from the digital output data $y[n]$ to correct the non-linearity (non-linearity correction block) and get the corrected output data $y_{\text{corrected}}[n]$.

The advantage of this technique is that it allows us to highly compensate the distortion of the VCO. For instance, in [43], the third harmonic distortion (HD3) is reduced from -48.5 dB to -80 dB. However, there are three disadvantages. Firstly, the system area is remarkably increased due to the compensation logic required. The compensation logic is composed of a signal path replica (as large as the converter signal path), and digital circuitry to calculate the distortion coefficients and correct the output of the system. This means that the area occupied might be doubled. Secondly, the required compensation logic supposes the design of complex circuits. Finally, these circuits may increase the power consumption of the system in an significant way.

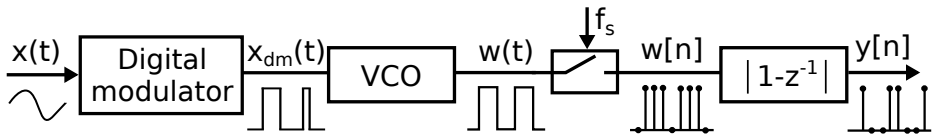


Figure 2.13: Using a digital modulator to linearize the VCO.

2.3.4.2 Digital precoding

Another way of correcting the VCO distortion is using a digital precoding block before the VCO. If a digital signal is connected to the VCO, it will oscillate at only two possible oscillation frequencies. Consequently, its performance will be inherently linear. Typically, a pulse width modulation (PWM) block has been used when this technique is considered to be implemented [54–57] but, in theory, any type of digital modulation could be used [58]. Fig. 2.13 shows how the VCO-based architecture looks when this technique is used.

The advantage of this solution is that it does not require large and complicate digital circuitry as in the digital calibration. Here, "only" a digital modulator is required. Nevertheless, the design of this modulator might become challenging if we are dealing with high-frequency oscillating systems (as will be our case later on) in terms of area, power and linearity. In addition, digital modulation is not free and adds modulation components within the spectrum of the input signal, which will degrade the performance of the converter if we do not deal with them properly.

2.3.4.3 Residue canceling

It is well-known that the distortion generated by a VCO depends on the amplitude of the VCO input signal. Therefore, we may think on reducing the amplitude of the VCO input signal. Some attempts to fix the VCO distortion based on this idea are [50, 59–61]. The architectures described on these papers usually split up the analog-to-digital conversion into two steps. Firstly, they make a first analog-to-digital conversion through a coarse ADC that is not a VCO-based one, and its output is subtracted from the input signal. Then, the result is introduced into a VCO-based ADC to make the second analog-to-digital conversion. As the output of the first ADC is a digitized version of the input signal, the result of the subtraction is a low-amplitude signal, low enough to make the VCO work in the linear region. Fig. 2.14 depicts the architecture proposed in [59], which is a multistage noise-shaping (MASH) architecture. We will deal with MASH architectures later on. As can be observed in the shaded area, a first quantization is made, the quantized signal is subtracted from the input signal and the result $V_{\text{res}}(t)$ is injected into the VCO.

The main disadvantage of this technique is that it requires a large amount of analog circuitry, which increases the complexity of the architecture, the power consumption and the occupied area.

Based on the residue cancelling idea, one of the last techniques developed to address the VCO non-linearity was published in [62]. In this paper, the coarse

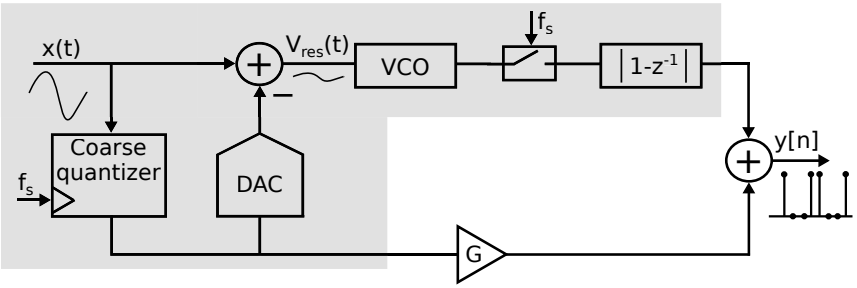


Figure 2.14: Feeding the VCO to a low voltage input signal.

quantizer of Fig. 2.14 is replaced by a VCO-based quantizer. The input of the coarse quantizer is high enough to generate distortion, however, if we regard the different signal paths of the architecture, we will notice that this distortion terms will be removed in the final sum that generates $y[n]$.

2.3.4.4 Circuit-based solutions

Finally, some efforts to overcome the VCO non-linearity have made through circuit-based proposals. If we focus on ring oscillators, the non-linearity comes from the non-linear variation delay suffered by each delay tap when either the supply voltage or the bias current changes. If this non-linear behavior is compensated somehow, the ring oscillator will work linearly. For example, in [63], the non-linearity is fixed through the tuning of the bias current of each CMOS inverter that compose the ring oscillator. Another example is [47], where a resistive divider is used to implement the inverse function of the voltage-to-frequency transfer function of the ring oscillator.

The main disadvantage of this type of solutions is that its performance highly depends on the manufacturing process (e.g. resistor variance) and the boundary conditions (e.g. supply voltage and temperature).

2.4 Conclusion

We have provided the foundations of the analog-to-digital conversion from the fundamental ideas to the specific ones, focused on oversampled ADCs implemented with VCOs. We have explained why VCO-based ADCs have attracted the interest of the designer community with the goal of replacing conventional $\Delta\Sigma$ modulators. The main reason for that is the possibility of implementing VCOs with mostly digital circuits, very suitable for deep-submicron CMOS processes. Finally, we have described one of the main drawbacks that limits the use of VCOs to build ADCs when high resolution is required, which is the non-linear voltage-to-frequency transfer function. The most significant ways to overcome this limitation have been described too.

The research work presented in this document deals with the proposal, study, design and implementation of VCO-based ADCs. This makes the knowledge of the content described in this chapter very important to understand the topics dealt in the following chapters.

Chapter 3

Spectral analysis of VCO-based ADCs based on pulse frequency modulation

In this chapter, we will provide new theoretical knowledge about VCO-based ADC spectral properties. The conventional analysis of VCO-based ADCs is based on similar assumptions to those made to analyze $\Delta\Sigma$ modulators. On the one hand, the VCO is seen as a phase integrator, which is somehow true. However, a VCO is also a signal encoder. This means that modulation components might appear at the output signal, making the integration "imperfect". The conventional approach does not consider the existence of these modulation components, which, in many cases, degrade the performance of the architecture. On the other hand, it is assumed that quantization noise does not depend on the input signal, which is not true [64, 65], and follows a white noise spectral distribution. Although it has been proven that these assumptions are good enough to build functional architectures for most of the cases, they are based on statistical assumptions that may not fit properly with some implemented architectures under certain conditions and may take us to unexpected results. Here, we will propose a new way to analyze VCO-based ADCs providing analytical equations and without making any statistical assumption.

We will show that a VCO can be analyzed using the equations that describe pulse frequency modulation (PFM) if some linear operations are taken into account. We will start with the equations of PFM and will adapt them to mathematically describe the output data of an open-loop VCO-based ADC. This methodology will allow us to get wider knowledge about the spectral properties of VCO-based ADCs and to know what is the effect of any of the working parameters in the performance of a converter (e.g. oscillation parameters). The PFM theory will apply to generic order open-loop VCO-based ADCs. Although we will see that only a few cases are implementable in practice, we will describe some new architectures derived from this theory. The starting point of the content of this dissertation was the equivalence between a first-order open-loop VCO-based ADC and a pulse frequency modulator we noticed at the beginning of the research period. Consequently, the amount of time we spent on studying the first order case is larger than for the other cases, leading to further results. In particular, for

the first order case, we also developed an algorithm to estimate the SNDR of this architecture without the need of simulating behavioral models. This algorithm applies to different architectures, both single phase and multiphase architectures that will be described too.

This chapter is specially focused on theoretical approaches that will suppose the key pillar of what will be presented among the whole document. In consequence, the understanding of this chapter is critical to get a proper perception of the content described in the following chapters. Although the content of this chapter is particularly theoretical, some significant extensions to practical circuits are also proposed. In addition, these new approaches allow us to analyze some limitations of potential practical implementations, as will be shown.

3.1 An introduction to the analysis of a VCO based on the pulse frequency modulation theory

The starting point here is the architecture of Fig. 2.10(c), which is the simplest way of implementing a first-order VCO-based ADC, and how this architecture performs, in a first approach, similarly to the architecture of Fig. 2.5(a).

The initial analyses of VCO-based ADCs tried to explain the operation of Fig. 2.10(c) with linear time-domain equations. In [41,66,67], to name a few, the circuit of Fig. 2.10(c) was shown to behave as the continuous-time first-order $\Delta\Sigma$ modulator shown in Fig. 2.5(a). The equivalence is based on considering the phase of the oscillator $\theta(t)$ as the state variable of the integrator of Fig. 2.5(a). This interpretation is restricted by the need to approximate the quantization error, which is typically assumed to be white noise. Based on this model, VCO-based ADCs were considered part of the $\Delta\Sigma$ ADC family and their description was as accurate as the conventional $\Delta\Sigma$ theory (and hence restricted by the model of the quantization error). Although the white noise model is useful to understand practical circuits, it is obviously an approximation and does not explain the true spectral structure of quantization noise or modulator stability. Several efforts have been made to refine the white noise model [64, 68], but most of them still use statistics. In [69, 70], an equivalence between a $\Delta\Sigma$ modulator and a FM modulator was first identified. Building forth on [69], exact analytical expressions for the output spectrum of a VCO-based ADC can be calculated. The key element of this analysis is to model the VCO-based system as a PFM combined with a sampler. This approach brings new insight, because the spectrum of a pulse frequency modulated signal can be described by a trigonometric series [71]. This gives us the opportunity to reformulate the description of VCO-based ADCs in an analytical way and answer the questions left aside by conventional $\Delta\Sigma$ modulation theory.

By the moment, our approach will be different from other works such as [45, 72–75], where the integrators in the loop filter of a continuous-time $\Delta\Sigma$ modulator are replaced by VCO-based equivalents and therefore require a feedback loop. Instead, we will concentrate on open loop architectures with no feedback around

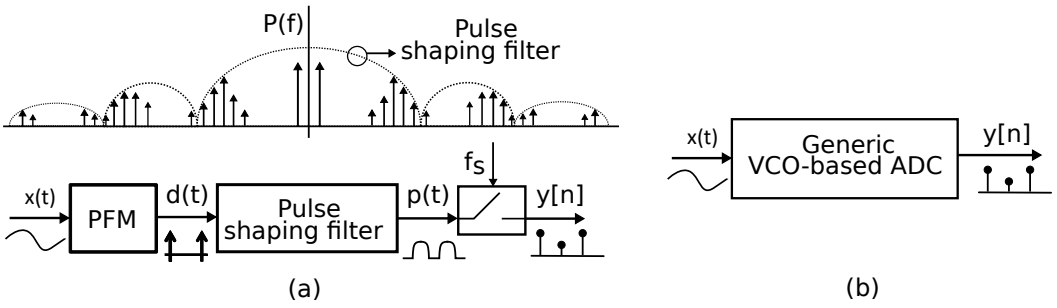


Figure 3.1: Approach followed: from the (a) PFM + pulse shaping filter + sampler architecture to a (b) generic order VCO-based ADC structure.

the VCOs [76] (later on, in Chapter 4, we will spend some time on making a first approach to closed-loop VCO-based systems using the theory proposed here).

The approach that we will follow is depicted in Fig. 3.1. Based on the PFM interpretation, we will propose a generic architecture of a VCO-based ADC which consists of a pulse frequency modulator followed by a pulse shaping filter and a sampler (Fig. 3.1(a)). The spectral characteristics of the pulse shaping filter will permit to tailor the noise shaping of the VCO-based ADC (Fig. 3.1(b)). The well known circuit of Fig. 2.10(c) will turn out to be a particular case of this generic architecture, implementing first-order noise-shaping.

3.2 Pulse frequency modulation: An alternative way to look at a VCO

In this section we will explain how a VCO can be used for the coding of a continuous-time analog signal. For this purpose, we will show that there is a strict equivalence between the VCO operation and pulse frequency modulation. This is a modulation technique that encodes band-limited signals into a train of Dirac delta impulses, where the information is encoded in the time position of the impulses [69].

3.2.1 VCO – PFM Equivalence

Fig. 3.2 shows a VCO and the associated pulse frequency modulated signals. Here, the input signal $x(t)$ drives a VCO and generates the VCO output signal $w(t)$. Without loss of generality, we will assume that the input signal $x(t)$ is bounded to the interval [-1,1], band-limited to a finite bandwidth BW and dimensionless. We will assume that the waveform $w(t)$ is a square wave. The actual instantaneous VCO frequency follows (2.19). When looking at the waveform $w(t)$, we see that all the information is contained in the edges of $w(t)$. In our treatment we will assume that only the rising edges are used[1]. We will also keep the same notations

[1]Note that the theory remains valid for circuits that use both the rising and the falling edges, but in that case it is more convenient to work with an $effective$ VCO frequency $f_{\text{osc,eff}}(t)$ which equals twice the actual VCO frequency $f_{\text{osc,eff}}(t) = 2f_{\text{osc}}(t)$. This is e.g. the case for the circuit

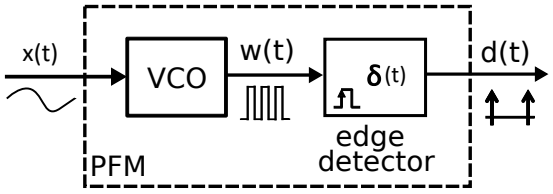


Figure 3.2: VCO – PFM equivalence.

already defined in (2.19) for the oscillation parameters and in (2.20) for the phase of the VCO. Note that the VCO gain (K_{VCO}) in this model is a design parameter. However, with our definition of the valid signal range, its value must be bounded as indicated in (2.19). We will restrict $x(t)$ to have zero mean for notational convenience. This requirement does not pose any practical limitation because if $x(t)$ has a DC component, we can always modify f_{o} to compensate the frequency offset produced by the DC shift. The rising edges of $w(t)$ represent the crossings of θ(t) (the phase of $w(t)$, equation (2.20)) over integer multiples of 2π. Now, we will generate the auxiliary signal $d(t)$ composed of Dirac delta functions coincident with the rising edges of $w(t)$. For this purpose, we have added the conceptual block "edge detector" to Fig. 3.2.Mathematically, this leads to:

$$d(t) = \sum_{k=0}^{\infty} \delta\left(t - t_{\mathrm{k}}\right), \quad \forall t_{\mathrm{k}} | \theta(t_{\mathrm{k}} = 2\pi k), \quad k = 0, 1, ... \tag{3.1}$$

The signal $d(t)$ is a pulse frequency modulated signal [77]. Clearly, $d(t)$ is a conceptual signal that cannot exist in reality. In practical applications, a pulse frequency modulated signal could be approximated by a train of narrow square pulses. Nevertheless, for our purposes, it is more convenient to build the argument on the (theoretical) Dirac delta pulsed signal $d(t)$.

For a sinusoidal input $x(t)$, the signal $d(t)$ can be expanded into a trigonometric series [71, 77]. It can be shown that $d(t)$ contains modulation sidebands at each multiple of the VCO rest frequency f_{o}, similarly to a frequency modulated signal. However, it also contains the actual signal $x(t)$ in the baseband, which is different from conventional frequency modulation (FM). If we consider a sinusoidal input signal $x(t)$:

$$x(t) = A \cdot \cos\left(2\pi f_{\mathrm{x}} t\right), \tag{3.2}$$

the signal $d(t)$ can be expanded into a trigonometric series as follows [77]:

$$d(t) = f_{\mathrm{o}} + K_{\mathrm{VCO}} \cdot x(t) + m(t),$$
$$m(t) = 2f_{\mathrm{o}} \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} J_{\mathrm{r}}\left(q \frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}}\right) \left(1 + \frac{rf_{\mathrm{x}}}{qf_{\mathrm{o}}}\right) \cos\left(2\pi\left(qf_{\mathrm{o}} + rf_{\mathrm{x}}\right)t\right), \tag{3.3}$$

where J_{r} is the r^{th} order Bessel function of the first kind. The expansion (3.3)

of Fig. 2.10(c)

can also be represented in the frequency domain by its Fourier transform $D(f)$:

$$D(f) = f_{\mathrm{o}}\delta(f) + \frac{AK_{\mathrm{VCO}}}{2}\left(\delta(f+f_{\mathrm{x}}) + \delta(f-f_{\mathrm{x}})\right) + M(f)$$
$$M(f) = f_{\mathrm{o}}\sum_{q=1}^{\infty}\sum_{r=-\infty}^{\infty} J_{\mathrm{r}}\left(q\frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}}\right)\left(1+\frac{rf_{\mathrm{x}}}{qf_{\mathrm{o}}}\right)$$
$$\left(\delta(f+(qf_{\mathrm{o}}+rf_{\mathrm{x}})) + \delta(f+(qf_{\mathrm{o}}-rf_{\mathrm{x}}))\right) \tag{3.4}$$

According to (3.3) and (3.4), $d(t)$ consists of a component which is linear with respect to the input signal as well as modulation sidebands components around each harmonic of the rest oscillation frequency f_{o}. These modulation sidebands components are denoted by the symbol $m(t)$ (or the associate spectrum $M(f)$).

3.2.2 Discussion of the Modulation Spectra

Unfortunately the expression for $m(t)$ (and $M(f)$) is not intuitive, because the modulation tones depend in a complex way on the signal parameters (input signal frequency as well as input amplitude). E.g. the sidebands are definitely not symmetrical around the central carrier and also they are not monotonically decaying. However, in general, each modulation sideband roughly consists of a pronounced central lobe and a tail that decays relatively rapidly. This is particularly the case when the input signal frequency is small relative to the VCO rest frequency. This situation is shown in Figs. 3.3(a) and (b), which show the calculated spectrum of the first six sidebands for the case of a low input signal frequency f_{x}=f_{o}/1024 and two different values of the input amplitude. Although according to (3.4) in principle, the sidebands around every harmonic of f_{o} stretch infinitely, it is clear from the figure that the bulk of every sideband's energy is contained in the central lobe which has a limited bandwidth. Moreover, if we denote the value of this limited bandwidth for the q^{th} as BW_{q}, we found that the following empiric relationship approximately holds:

$$BW_q \approx 2qAK_{\mathrm{VCO}} \tag{3.5}$$

The corresponding value of the calculated sideband bandwidth is also added to Fig. 3.3, and it is clear that it matches relatively well for this case of a low input signal frequency f_{x}=f_{o}/1024. As the equation indicates, the higher sidebands become wider, which has the consequence that the spectra of these higher order sidebands (e.g. for $q \geq 4$ in Fig. 3.3(b)) start to overlap. Due to this, the high frequency spectrum starts to look like white noise.

If we now keep the input amplitude the same as Fig. 3.3(b), i.e. AK_{VCO}=f_{o}= 8, but increase the input frequency to an intermediate value of f_{x}=f_{o}= 64, see Fig. 3.3(c), we can distinguish a central lobe with a bandwidth which still follows (3.5), but the tail of the modulation band decreases much less rapidly. If we from here further increase the input frequency to a relatively high input frequency of f_{x}=f_{o}= 16, see Fig. 3.3(d), the tail and the central lobe cannot really be distinguished anymore and the modulation band stretches well beyond the bounds of (3.5).

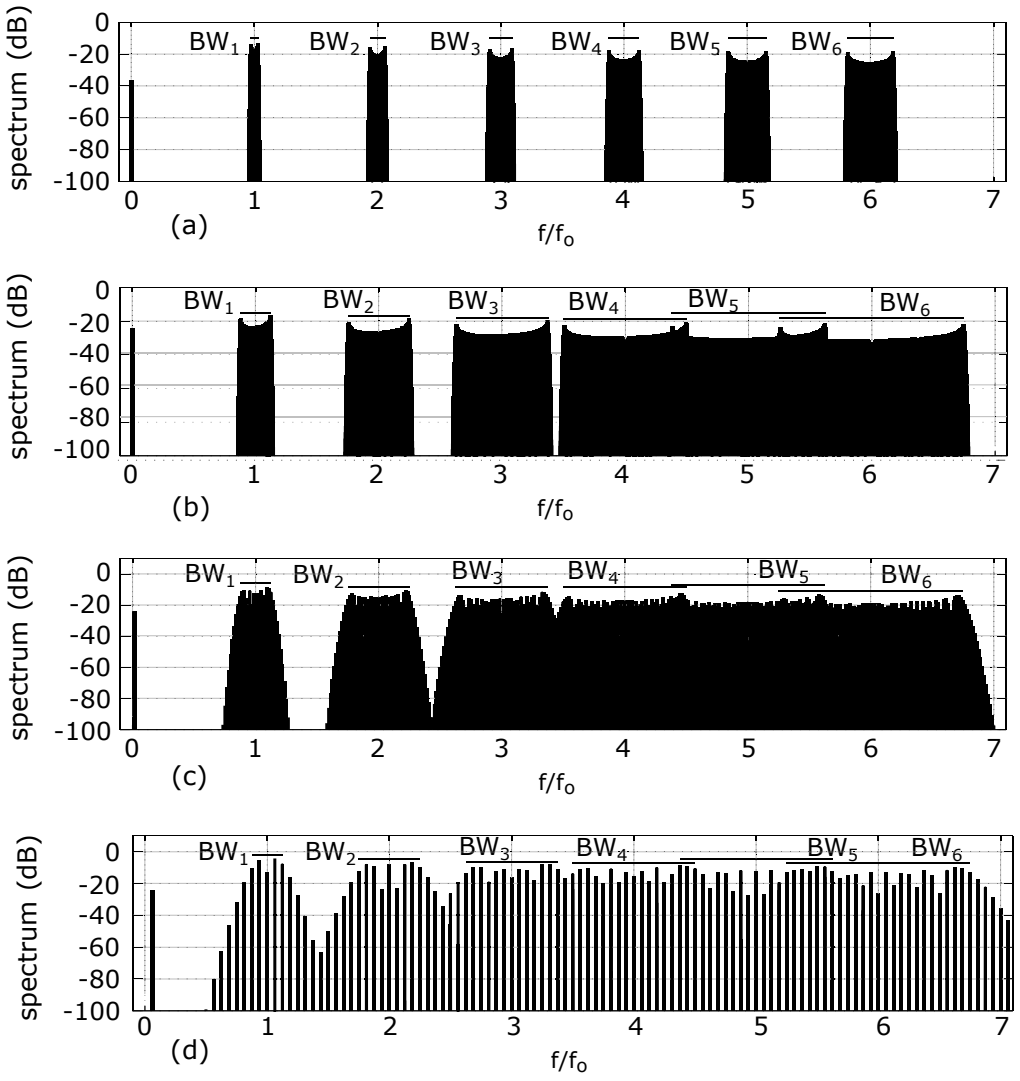


Figure 3.3: Calculated spectrum according to (3.4) of the first six sidebands for the case of an input signal with (a) a low input frequency $f_{\mathrm{x}} = f_{\mathrm{o}}/1024$ and a small input amplitude $AK_{\mathrm{VCO}} = f_o/32$, (b) again for a low input frequency $f_{\mathrm{x}} = f_{\mathrm{o}}/1024$ but a larger input amplitude $AK_{\mathrm{VCO}} = f_{\mathrm{o}}/8$, (c) for the same input amplitude $AK_{\mathrm{VCO}} = f_{\mathrm{o}}/8$ but now an intermediate input frequency $f_{\mathrm{x}} = f_{\mathrm{o}}/64$ and (d) for again the same input amplitude $AK_{\mathrm{VCO}} = f_{\mathrm{o}}/8$ but now a relatively high input frequency $f_{\mathrm{x}} = f_{\mathrm{o}}/16$.

3.2.3 Fundamental SNDR Limit of VCO-based coders

Regardless of the input signal, we can always say that globally, the sideband tones decrease in amplitude when they are further away from the corresponding harmonic of the VCO carrier. However, regardless of how rapidly the tail of each modulation sideband decays, it in reality stretches infinitely far, which means that there are always non-zero sideband tones from the first sideband (q= 1 in (3.3)) that will fall into the useful signal band. This phenomenon is sketched in Fig. 3.4. In theory, there are also contributions from the higher harmonic

sidebands, but in practice these are normally negligible compared to those from the first sideband.

The typical decimation filter applied to recover the output data from a VCO-based ADC architecture is a low-pass filter. Therefore, although the spectrum of $m(t)$ is deterministic, the in-band sideband tones of Fig. 3.4 degrade the signal integrity in a similar way as additive noise (or distortion). Then, for a given band of interest (BW), we can estimate the SNDR from (3.3) by summing the contributions of all the components falling into BW:

$$\mathrm{SNDR} = 10\log_{10}\frac{\left(\frac{AK_{\mathrm{VCO}}}{2f_{\mathrm{o}}}\right)^2}{\sum_{r=r_{\min}}^{r_{\max}}\left(J_r(\frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}})\left(1+r\frac{f_{\mathrm{x}}}{f_{\mathrm{o}}}\right)\right)^2}, \tag{3.6}$$
$$r_{\min} = \mathrm{ceil}\left(\frac{-\mathrm{BW}-f_{\mathrm{o}}}{f_{\mathrm{x}}}\right), r_{\max} = \mathrm{floor}\left(\frac{\mathrm{BW}-f_{\mathrm{o}}}{f_{\mathrm{x}}}\right)$$

Here $r_{\min}$ and $r_{\max}$ correspond to the index of the lowest and the highest component respectively that fall into BW. This equation can be considered as a fundamental encoding error, which is inherent in any VCO based scheme where the VCO encodes the information into the edge positions.

Unfortunately, (3.6) is again a non-intuitive function that depends on the effective amplitude $A \cdot K_{\mathrm{VCO}}$, f_{x}, BW and f_{o}. Upon investigation, this function was found to have a non-monotonic behavior in terms of these parameters. To illustrate this, the result for the case of a fixed f_{o}, a fixed $BW = f_{\mathrm{o}}/32$ and fixed $A \cdot K_{\mathrm{VCO}} = f_{\mathrm{o}}/\sqrt{2}$ corresponding to -3 dBFS, was evaluated for all in-band values of the input frequency f_{x} (i.e. f_{x} ranging from DC to the band edge). The resulting SNDR (corresponding to the VCO encoding error) is shown in Fig. 3.5. It is clearly a very strong function of the input frequency, which is consistent with Fig. 3.3, where we have already seen that the sideband tones decay much more rapidly for lower frequency input signals. Although for most of the input frequency values, the resulting SNDR corresponding to a fundamental encoding error is absurdly high, there are some values for the input frequency (located at the band edge), where the SNDR is much less good. The corresponding worst case here is 83 dB. Since, even in a bandwidth limited application, it is not known in advance what the input frequency will be, this worst case corresponds to a fundamental SNDR limit.

To further asses this a more detail study was performed, where f_{o} was kept fixed and BW was varied. For every value of BW, f_{x} was varied in steps of $BW/1000$. Then, (3.6) was evaluated and the value of the SNDR was collected (leading to a plot such as Fig. 3.5). Now, the worst case SNDR was defined as the fundamental SNDR limit corresponding to this normalized bandwidth value. This procedure was repeated for decreasing values of the input amplitude (starting from absolute full scale, i.e. A= 1 going down to -10 dBFS in steps of 1 dB). The results are shown in Fig. 3.6. The VCO-gain K_{VCO} was set to its maximal value, i.e. $K_{\mathrm{VCO}} = f_{\mathrm{o}}$, but it should be noted that the results shown in the figure can be mapped to other values of K_{VCO}, by adjusting the value of the input signal amplitude.

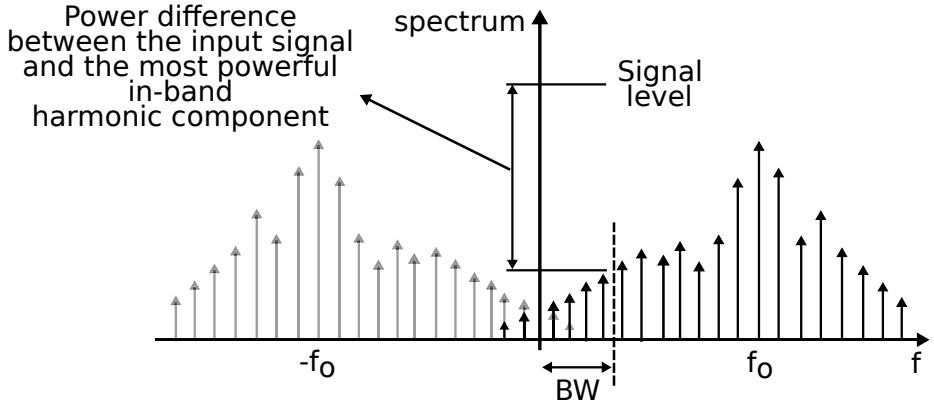


Figure 3.4: Sketch of the signal integrity degradation due to spurious tones of the first modulation sideband extending into the useful signal band.

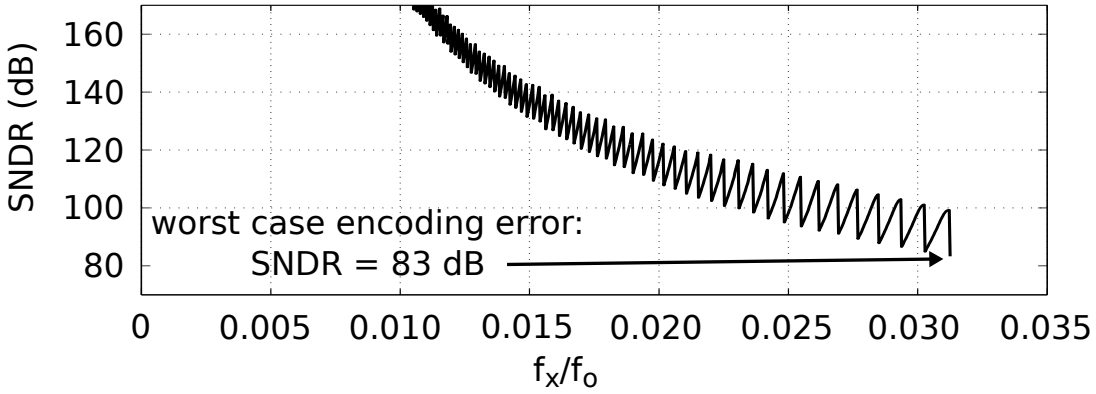


Figure 3.5: SNDR due to to the encoding error calculated according to Eq. (3.6) vs. the input signal frequency f_x for the case of an in input amplitude of -3 dB_{FS} for a fixed bandwidth equal to $f_o/32$.

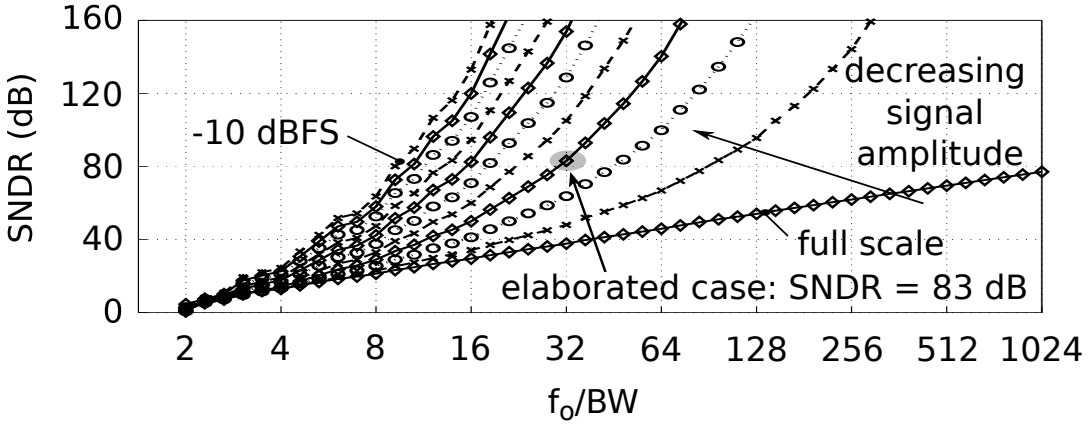


Figure 3.6: Limiting SNDR for the case of an in band input tone vs the ratio f_o/BW for different values of the input signal magnitude (ranging from full scale to -10 dBFS in steps of 1 dB).

The plot of Fig. 3.6 is a fundamental performance limit that occurs in all VCO-based coding schemes. As the plot indicates, the performance (set by this hard limit) rapidly increases when f_o increases. However, for signals that are really full-scale, the performance increases only very slowly. An important remark is, that this result was derived for a single-phase VCO that only uses the rising edge information. Later on, we will see that the result is also valid for multiphase VCOs (with M phases) that use both the rising and the falling edges, provided that we use the effective rest frequency $f_{o,\,\text{eff}} = 2 \cdot M \cdot f_o$. Most published VCO-based ADC designs until today are operated with $f_{o,\,\text{eff}}/BW$ values of well above 512 [41,52,56,61,78]. This means that the performance of these designs were never limited by fundamental limit. We will see that, when sampling is introduced, there will be additional noise/distortion components which, in many cases, will be larger than this fundamental limit.

3.3 Direct construction of a VCO-based ADC using the PFM representation

We will now start from the PFM representation described above and define a strategy to derive a family of theoretically possible VCO-based ADC structures. We will see that some of these structures do not translate to a circuit that can be implemented in a simple way. However, we will show that one of the derived solutions is equivalent to the conventional first-order VCO-based ADC depicted in Fig. 2.10(c). Our derivation will enable a much deeper insight in the spectral and tonal behavior of such ADCs that what can be understood from common explanations. Such first-order VCO-based ADCs are typically explained by linking the phase of the oscillator to the state variable of a $\Delta\Sigma$ modulator [41, 43, 67], which is then quantized and differentiated. Whereas this prior understanding has proven to be insightful, it is stuck at the white noise approximation of the quantization error and cannot explain the tonal behavior that occurs in reality. Our derivation will overcome this limitation and provide exact results.

3.3.1 Going from a PFM encoder to an ADC

Let us look again at the system of Fig. 3.2. To derive an ADC from this structure, somewhere *sampling* should be introduced. Clearly, signal $d(t)$ cannot be directly sampled because only the Dirac deltas in $d(t)$ coincident with a sampling instant would be detected. This can also be understood in the frequency domain, because sampling of $d(t)$ would introduce a multitude of uncontrolled aliases into the band of interest, due to the non band limited and non decaying spectrum of $d(t)$ (Fig. 3.3). This would make the recovery of the input signal impossible. Fig. 3.7 shows a generic VCO-based ADC structure that solves the aliasing problem. In the structure, a linear pulse shaping filter with impulse response $h(t)$ is added after the PFM (of Fig. 3.2). This filter generates an output signal $p(t)$ which can now be sampled with a uniform sampler with sampling frequency f_s to obtain the overall sampled output signal $y[n]$.

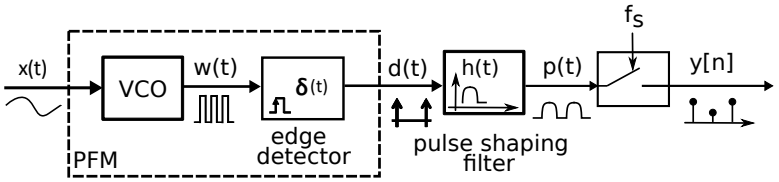


Figure 3.7: Generic structure for a potential VCO-based ADC.

The pulse shaping filter has two requirements. First, it must have a low-pass characteristic to allow the input signal components in $d(t)$ to pass through. Second, it should suppress the modulation sidebands located at frequencies that would alias to the low-pass signal band. This can be achieved by placing periodic zeroes in the frequency response at integer multiples of the sampling frequency (which will alias to the baseband). This way, all the baseband aliased components coming from the modulation sidebands will be spectrally shaped similarly to quantization noise in a conventional $\Delta\Sigma$ modulator. As a difference, such structure would be unconditionally stable. The aliasing process and how it is affected by the low-pass filter is represented in Fig. 3.8.

A good way to construct a suitable filter $h(t)$ is as a cascade of a low-pass function and a linear combination of delays of the sampling period $T_\mathrm{s} = 1/f_\mathrm{s}$. This linear combination of delays allows to implement the periodic zeroes. A potential solution for this is the $sinc_n$ filter:

$$H_n(s) = sinc_n = \frac{\left(1 - e^{-sT_s}\right)^n}{(sT_s)^n}. \tag{3.7}$$

In (3.7), the zeroes of n-th order at $s = 0$ are canceled by the poles of $1/(sT_\mathrm{s})^n$, resulting in a unity gain at DC and a periodic zero structure at integer multiples of the sampling frequency f_s. This filter would spectrally shape the aliases of the modulation sidebands by a n-th order zero, in a similar way as the NTF of an n-th order $\Delta\Sigma$ modulator. Fig. 3.9 shows the pulse shape and the frequency response for $n = 1$ (the case used also in Fig. 3.8) and $n = 2$.

3.3.2 Error analysis of the generic VCO-based ADC

Above, we have identified and quantified the first error in any VCO-based ADC (Fig. 3.5): i.e. the fundamental PFM encoding error. Now, we will quantify a second error that occurs in our generic VCO-based ADC structure of Fig. 3.7. For this, we will start with the model shown in Fig. 3.10(a).

Here $M(s)$ corresponds to the Laplace transform of the modulation terms introduced by the pulse frequency modulation process [e.g. according to (3.3)]. To simplify the model, the VCO gain K_VCO was normalized to unity and the offset contribution corresponding to the rest oscillation frequency f_o was omitted. Within these approximations, this model provides an exact description of the behavior of our generic VCO-based ADC. Then, in a next step, we use the property that a Z-domain factor of z^{-1} corresponds to a continuous-time delay

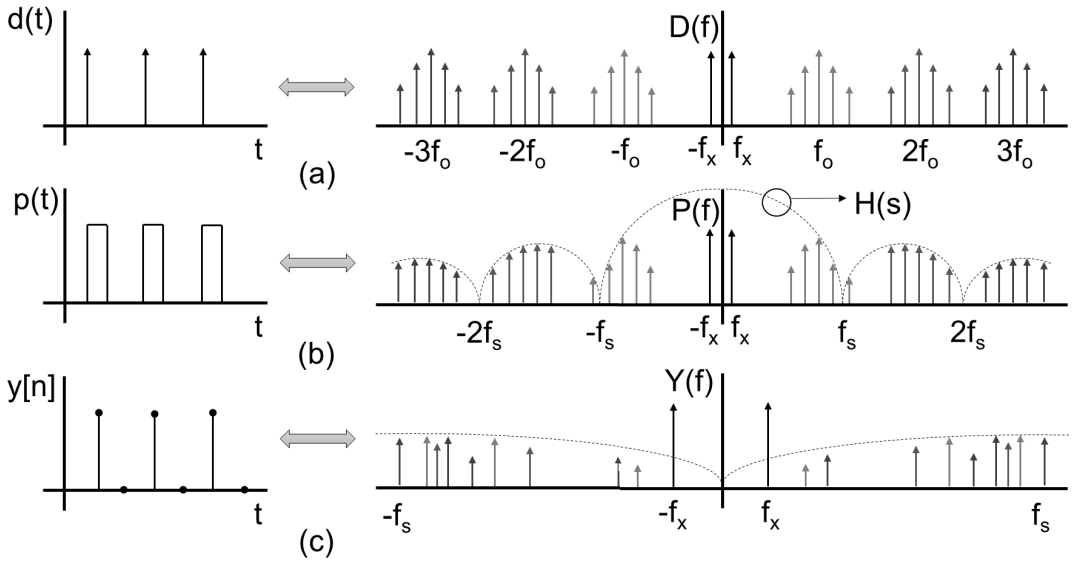


Figure 3.8: Illustration of the effect of the lowpass filter $H(s)$ on the aliasing of the modulation sidebands for the case of a single tone sinusoidal input signal, with a sketch of the time domain as well as the frequency domain signals for (a) the signal $d(t)$, (b) the filtered signal $p(t)$ and (c) the sampled overall output signal $y[n]$.

of one sampling period T_s followed by a sampler [32, 79]. This way, we obtain the model of Fig. 3.10(b), which is still strictly equivalent to the generic VCO-based ADC structure.

The second error in our generic ADC occurs due to the aliasing of high frequency components of the filtered modulation signal in the sampling process. In order to quantify this, we split the modulation signal $M(s)$ into two components: first we have the low frequency component M_LF, below $f_\mathrm{s}/2$. This low-frequency component gives rise to the fundamental PFM encoding error (see Fig. 3.6). The second component M_HF corresponds to the high frequency content in $M(s)$ above $f_\mathrm{s}/2$. This high frequency component passes through the continuous-time filter $1/(sT_\mathrm{s})^n$ and is then prone to aliasing. This process is illustrated in Fig. 3.10(c), where we reason on the output signal $U(s)$ of the block $1/(sT_\mathrm{s})^n$. Here the two effects of the aliasing phenomenon are modeled explicitly by a combination of two operations: on the one side, the high frequency components U_HF of the sampler's input signal U are removed but, on the other side, they re-enter the system again as aliased baseband components which we will denote as U_al and which is a discrete time signal. To stress that the aliasing happens in the sampling process we have introduced the special "sampling with aliasing" symbol. If we use the $[\cdot]^*$ operator to indicate sampling as defined in [32], the aliasing error U_al is defined as:

$$U_\mathrm{al} = \quad [U_\mathrm{HF}]^* \,. \tag{3.8}$$

If we assume that the input signal X is band-limited, then the high frequency component U_HF is entirely due to the filtered high frequency modulation compo-

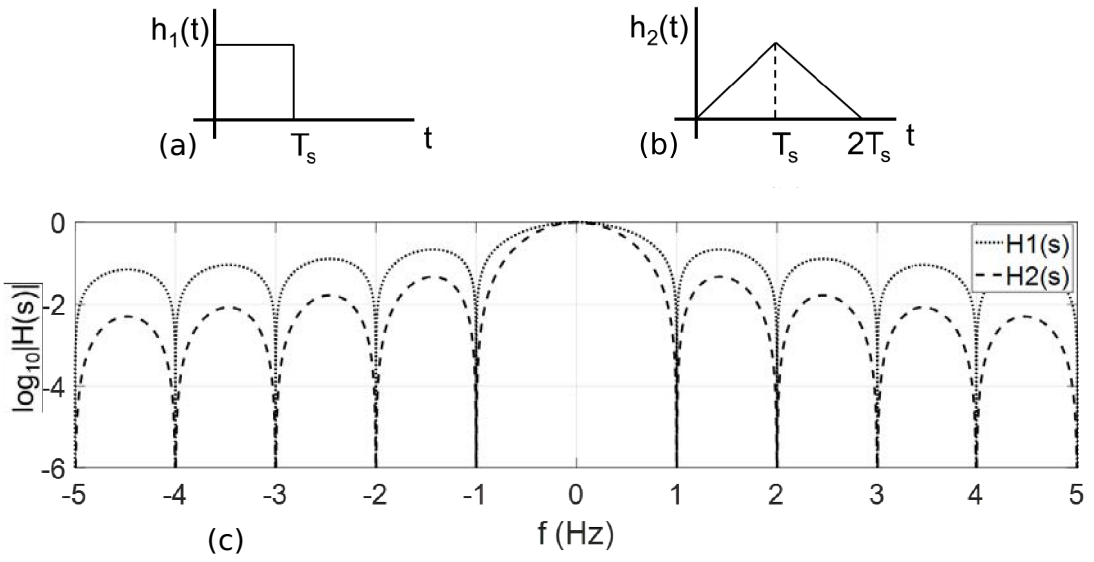


Figure 3.9: Time domain impulse response of (a) the first order shaping pulse and and (b) the second order shaping pulse with (c) their respective frequency response.

nents $M_{\mathrm{HF}}(s)$:

$$U_{\mathrm{HF}}(s) = \frac{M_{\mathrm{HF}}(s)}{(sT_s)^n}. \tag{3.9}$$

To emphasize that in this case the aliasing error is entirely due to the VCO's high frequency modulation components, we introduce the symbol M_{al} (read as: the aliased filtered modulation components of the VCO). A similar fact was identified in [80] where the link between quantization noise of a sine wave and frequency modulation was established. With these observations, finally our model can be simplified to the model of Fig. 3.10(d). Now, by inspection, the sampled output $Y(z)$ can be obtained as:

$$\begin{aligned} Y(z) = \left[\frac{X(s) + M_{LF}(s)}{(sT_s)^n}\right]^* (1 - z^{-1})^n + \\ M_{\mathrm{al}}(z)(1 - z^{-1})^n, \end{aligned} \tag{3.10}$$

where the $[\cdot]^*$ operator indicates sampling again. By introducing the signal transfer function $\mathrm{STF}(s)$ as:

$$\mathrm{STF}(s) = \frac{(1 - e^{-sT_s})^n}{(sT_s)^n}. \tag{3.11}$$

Equation (3.10) can be rewritten as:

$$\begin{aligned} Y(z) = &[\mathrm{STF}\ X(s)]^* + \\ &[\mathrm{STF}\ M_{LF}(s)]^* + \end{aligned}$$

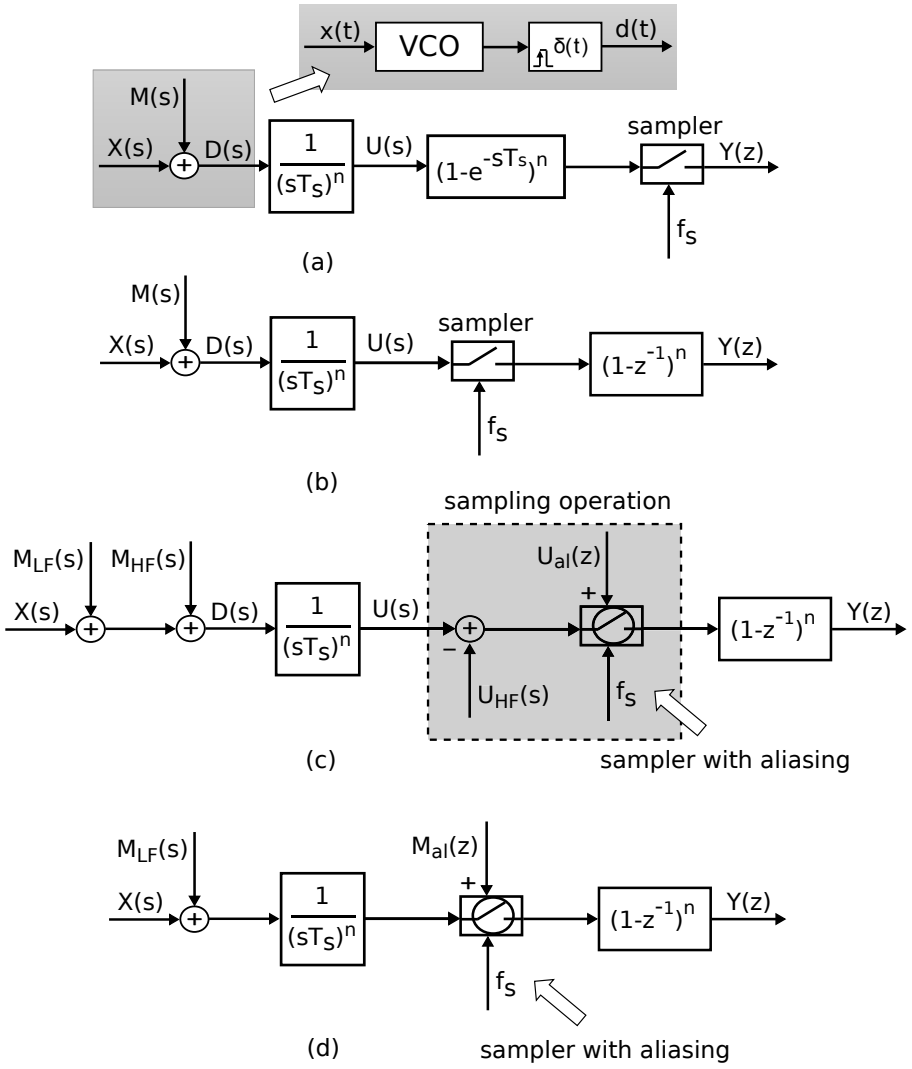


Figure 3.10: Explanation of the spectral shaping in our generic VCO-ADC (a) generic VCO-ADC, (b) equivalent structure of our generic VCO-ADC, (c) equivalent structure with explicit indication of the errors in the sampling process, (d) final equivalent model with the overall I/O behavior.

$$M_{\mathrm{al}}(z)(1-z^{-1})^n. \tag{3.12}$$

In the above equation, the first term corresponds to the desired signal component. The second term corresponds to the fundamental PFM encoding error. The third term corresponds to the aliasing error. As is evident from the equation, this aliasing error will be spectrally shaped according to the order of the pulse shaping filter. Hence, we expect a better signal-to-noise ratio (SNR) for increasing n, but unfortunately (as will be shown later on) it is not obvious to find a practical circuit for the pulse shaper apart from the case where $n = 1$ (first order case).

It should be noted that the aliasing error in this model replaces the quantization error of more conventional phase domain models [41]. However in this model, in principle, the spectra of all the signals in (3.10) can be calculated exactly.

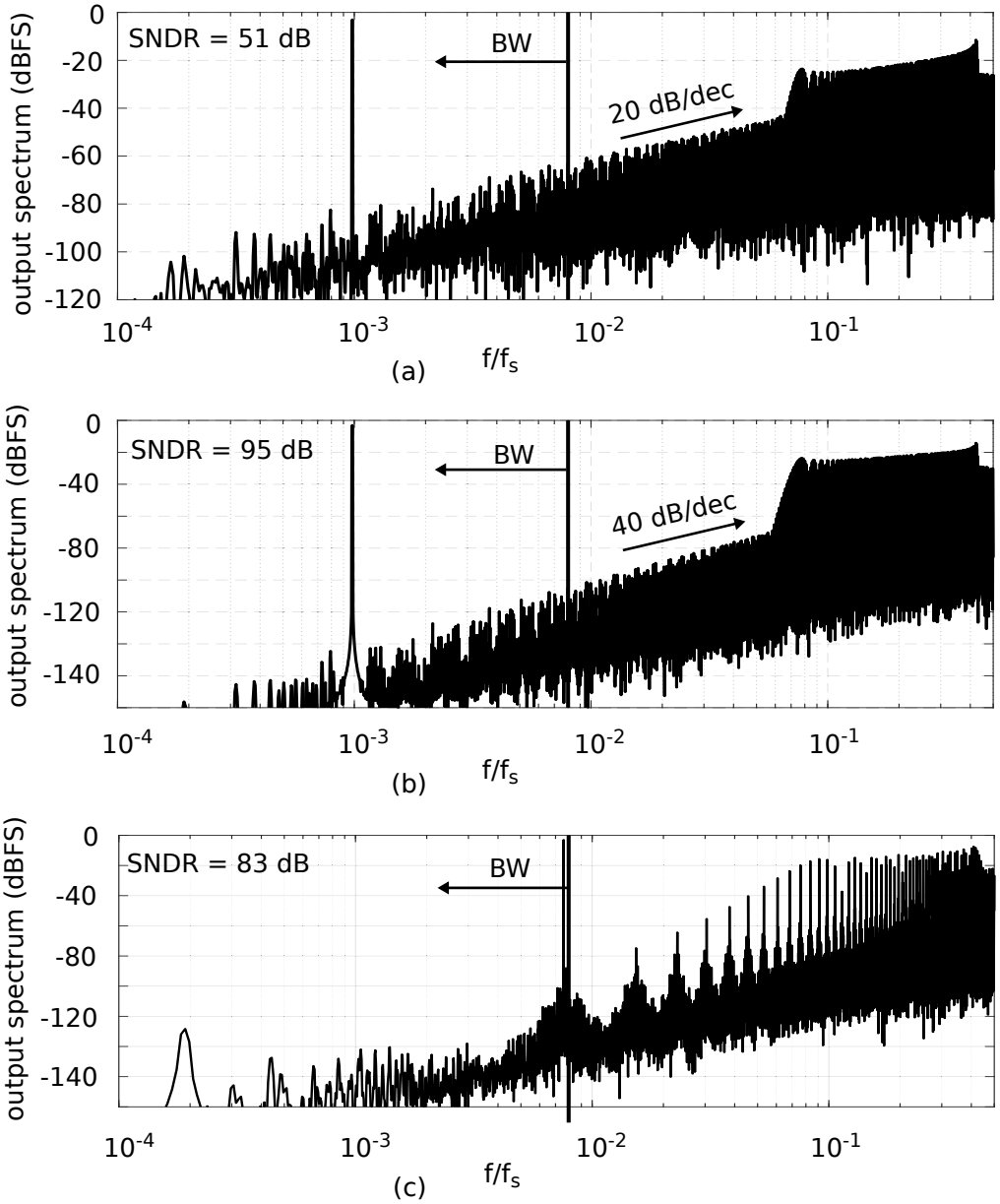


Figure 3.11: Output spectra of the generic VCO-ADC architecture illustrating the spectral shaping of the aliasing error for the case of: (a) a first-order sinc filter, (b) a second-order sinc filter,and (c) a second-order sinc filter where the input frequency f_{x} is chosen such that the SNDR is limited to 83 dB by the fundamental PFM encoding error (i.e. $f_{\mathrm{x}} \approx BW$).

E.g. the spectrum of the aliased signal (which is considered as an error in this system) can be obtained exactly by taking into account the filtering $1/(sT_{\mathrm{s}})^n$ and then summing over all the aliasing bands of the spectrum of $m(t)$. This closed expression allows the analytical calculation of resulting SNDR of $y[n]$ due to the aliases of the modulation sidebands. Whereas the theory provides closed analytical expressions for the spectra, the result is still an infinite sum over all the alias bands, which in practice must be numerically approximated with a computer.

As a result, these analytical expressions (although of theoretical interest) do not allow neither easy intuition nor hand calculations.

To illustrate the validity of the proposed generic VCO-based ADC, we have performed several behavioral simulations according to the conceptual block diagram of Fig. 3.7, where we have a VCO, an edge detector, a pulse shaping filter $H_{\mathrm{n}}(s)$ and a sampler. First, the case where the pulse shaping filters equals the first-order sinc filter $H_1(s)$ was considered. The results of a typical simulation are shown in Fig. 3.11(a). Here f_{s} was arbitrarily set to 1 Hz. The rest oscillation frequency f_{o} was set around $f_{\mathrm{s}}/4$: $f_{\mathrm{o}} \approx f_{\mathrm{s}}/4 = 0.25$ Hz. As before, we have assumed that the VCO input signal $x(t)$ is dimensionless and bounded to the interval [-1, 1]. The VCO gain was set to $K_{\mathrm{VCO}} = 0.25$ Hz/unit.

The resulting ADC is driven by a sinusoidal input signal with a frequency of $f_{\mathrm{s}}/1024$ and an amplitude of -3 dBFS. The plot clearly demonstrates a 20 dB/dec roll-off, confirming the analysis above. For an OSR of 64, we obtain an SNDR of 51 dB. For comparison, the result of the same experiment but now for the case where the pulse shaping filter equals the second-order sinc filter $H_2(s)$ is shown in Fig. 3.11(b). As expected, now the spectral roll-off has a slope of 40 dB/dec. The SNDR for an OSR of 64 is now equal to 95 dB. Clearly, in this case, due to the second-order sinc filter, the aliasing error exhibits second order spectral shaping and is greatly suppressed. However, it is important to realize that this spectral shaping only shapes the aliasing error and not the fundamental encoding error discussed in the previous section.

For this simulation, the value of the input amplitude, BW and f_{o} were chosen such that it corresponds to the case of Fig. 3.5. Looking back at that figure, we can see that for certain choices of f_{x} (i.e. near band edge), the fundamental encoding error limits the SNDR to only 83 dB regardless of the spectral shaping of the aliasing error. This is illustrated in Fig. 3.11(c), which shows the same simulation result as Fig. 3.11(b) but now for an input frequency f_{x} near band edge. Now the fundamental encoding error is larger than the spectrally shaped aliased error and restricts the performance to 83 dB, which exactly matches with the calculated result depicted in Fig. 3.5.

3.3.3 Implementation of a generic VCO-based ADC

Above we have derived a conceptual generic VCO-based ADC architecture (Fig. 3.7). However it is not immediately clear how the continuous-time analog pulse shaping filters should be implemented in practice. In order to investigate this, the time domain waveforms corresponding to the filter's input signal, $d(t)$, and output signal, $p(t)$, are shown in Fig. 3.12, for the case of the first and second order pulse shaping filters: $H(s) = H_1(s)$ and $H(s) = H_2(s)$, respectively.

In terms of practical implementation, the case with the first order filter is particularly useful. In this case, the impulse response $h_1(t)$ is the standard zero order hold pulse. This enables a hardware efficient realization, because, as shown in Fig. 3.12(b), $p_1(t)$ will always be composed of discrete amplitude levels due to the constant hold level of the shaping pulse. Then, the sampled signal $y[n]$ would become discrete both in time and in amplitude. A very interesting situation occurs when the delay between two consecutive pulses in $d(t)$ is larger than or

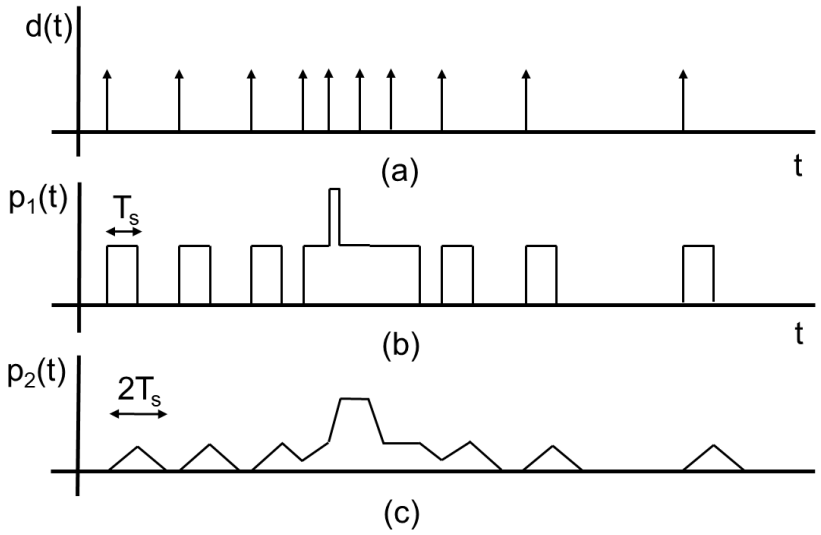


Figure 3.12: Time domain waveforms that can occur in the generic VCO structure of Fig. 3.7: (a) edge signal $d(t)$ (b) output signal $p_1(t)$ of the pulse shaping filter for the first order case and (c) output signal $p_2(t)$ of the pulse shaping filter for the second order case.

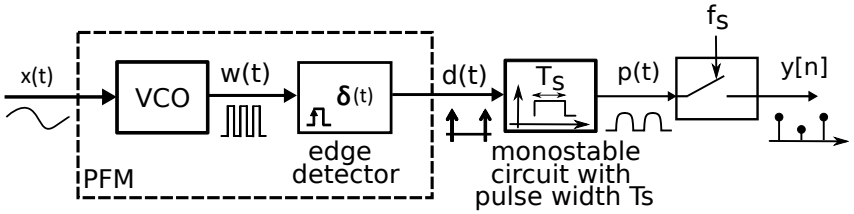


Figure 3.13: Conceptual realization of a first order VCO-ADC with a monostable.

equal to the sampling period $T_\mathrm{s} = 1/f_\mathrm{s}$. In this case, the filtered signal $p_1(t)$ can only take two possible values (logic zero or logic one). This enables the conceptual realization shown in Fig. 3.13, where the filter is implemented with a monostable which generates a pulse with a width of T_s on every rising edge of the VCO output waveform $w(t)$. Whereas this looks like a viable implementation, it should be noted that this realization is not advised in practice for the following reason: in order to make this circuit operate as desired, the pulse width should perfectly match with the sampling period T_s. In practice this cannot be achieved because mismatch effects that always occur in real circuits will make the pulse length different with respect to the ideal one. From a spectral point of view, this means that the zeroes of the corresponding filter are not exactly placed at integer multiples of the sampling frequency and, as a result, the suppression of the aliasing distortion is much less good than expected. Fig. 3.14 shows an example of this phenomenon. Here, the system of Fig. 3.13 was simulated with the same parameters as in Fig. 3.11, but a monostable whose pulses are only 1% longer in length than the nominal value was used. It can be observed that the performance is completely degraded by the aliasing components, which fall into the bandwidth

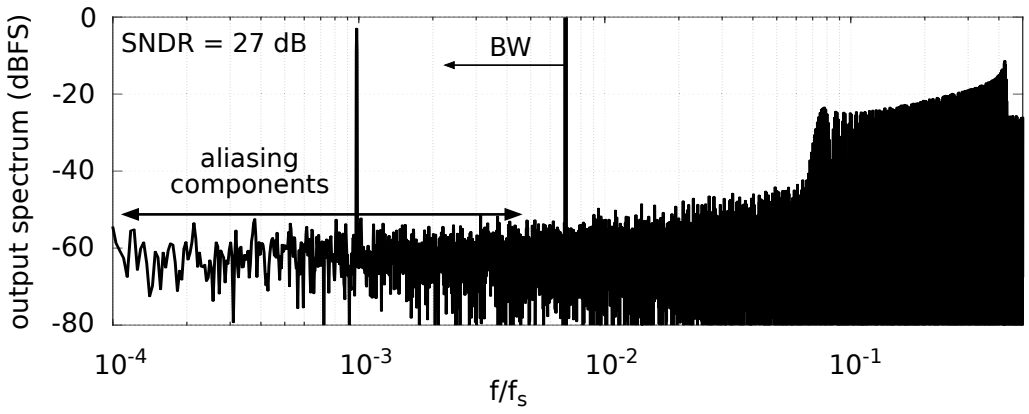


Figure 3.14: Performance degradation of the system of Fig. 3.13 when the length of the pulse in the monostable does not match exactly with T_s (1% deviation).

of the converter and make the SNDR be decreased to 27 dB.

As a difference with the circuit of Fig. 3.13, the circuit of Fig. 2.10(c) behaves similarly but automatically forces the sinc filter delay to be coincident with the sampling period. Therefore, it does not require any matching in the circuit and provides a robust implementation.

By observing Fig. 3.8 we can see that the model of Fig. 3.7 does not impose any restriction to the sampling frequency f_s. The spectral shaping of the modulation sidebands would happen regardless of the ratios between f_s, f_o and K_VCO. However, as explained above, the circuit of Fig. 2.10(c) only implements the generic first order VCO-based ADC of Fig. 3.7 if the minimum time distance T_min between two edges[2] in the VCO signal $w(t)$ is greater than or equal to the sampling period T_s. Considering a normalized VCO input signal $x(t)$ that is dimensionless and bounded to the interval [-1, 1], we can immediately conclude that the minimum sampling frequency $f_\mathrm{s,min}$ [41, 43]:

$$f_\mathrm{s,min} = (f_\mathrm{o} + K_\mathrm{VCO})_\mathrm{eff} = (f_\mathrm{max,osc})_\mathrm{eff} = \left(\frac{1}{T_\mathrm{min}}\right)_\mathrm{eff}, \tag{3.13}$$

where $f_\mathrm{max,osc}$ stands for the highest possible VCO output oscillation frequency.

This can be further understood if we consider the waveforms in the ideal first order case generic VCO-based ADC of Fig. 3.7 for the case where condition (3.13) is met or not. The situation where the condition is met is depicted in Fig. 3.15(a)-(b), where the VCO output $w(t)$ and the corresponding signal $p(t)$ are shown. Now we can see that condition (3.13) implies that the output signal $p(t)$ obtained from the generic first order VCO-based ADC is a single bit signal. This is evident from the observation that $p(t)$ has only two voltage levels. By contrast, if $f_\mathrm{max,osc}$ is higher than the sampling frequency, as in Fig. 3.15(c)-(d), the output signal $p(t)$ will become a multilevel signal. In this case, we still maintain discrete output signal levels, which can easily be represented by a digital representation, but now

[2]Remember that the circuit of Fig. 2.10(c) reacts both on the rising as well as on the falling edges, and hence should be analyzed with an effective oscillation frequency $f_\mathrm{osc,eff}(t)$ equal to twice the actual oscillation frequency.

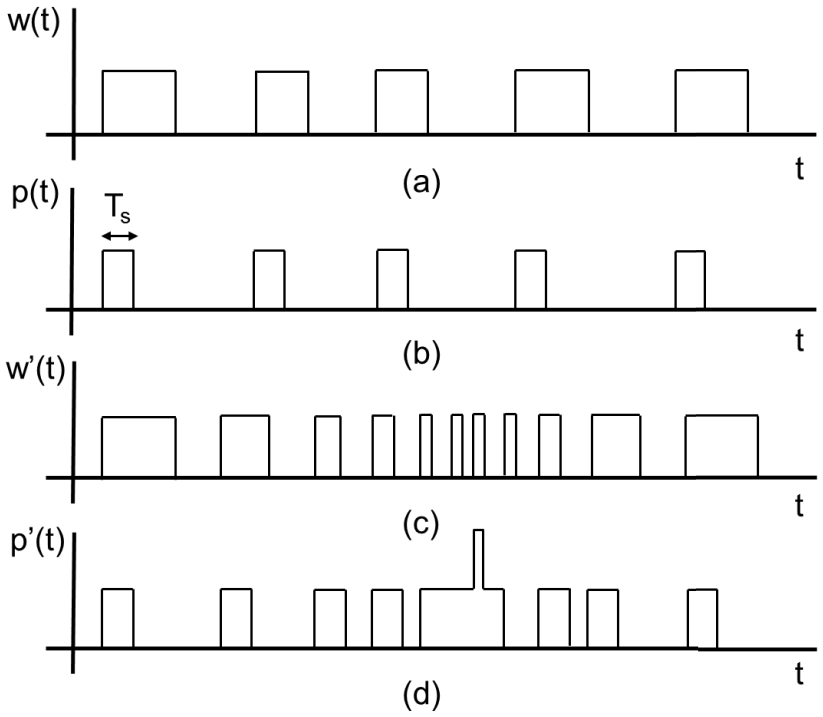


Figure 3.15: Effect of sampling frequency in generic first order VCO-ADC when: (3.13) is accomplished ((a) and (b)); (3.13) is not accomplished ((c) and (d)).

a multibit version. This situation in fact corresponds to the behavior of the well known multiphase ring oscillator VCO-based ADC of Fig. 3.16(a). In this system, the output signal $y[n]$ is a multilevel signal. This circuit can also be understood as an implementation of out generic first order VCO-based architecture with a high effective oscillation frequency f_{eff} given by [41, 43]:

$$f_{\text{osc,eff}} = 2 \cdot M \cdot (f_{\text{o}} + K_{\text{VCO}} \cdot x(t)). \tag{3.14}$$

In this case, the effective frequency does not comply with (3.13) and hence the overall behavior corresponds to Fig. 3.15(c)-(d).

Fig. 3.16(b) shows a system level block diagram that describes the behavior of Fig. 3.16(a). In Fig. 3.16(b), a single output PFM is connected to a multiplexer that casts the Dirac delta impulses in $d(t)$ into an array of identical pulse shaping filters. Each time a Dirac delta impulse enters the multiplexer, the switch advances to the next output in a cyclic way, sorting the Dirac delta impulses into M streams (see Fig. 3.16(c)). Every individual Dirac delta stream has a frequency M times lower than f_{eff} and then, (3.13) will hold. Therefore, each branch can use the circuit based on an XOR gate shown in Fig. 3.16(a) to implement the sampled pulse shaping filter with no restrictions. The system is exactly equivalent to Fig. 3.13.

Let us investigate Fig. 3.12 again, but now for the second order case, i.e. Fig. 3.12(c). Unfortunately, the pulse does not have a constant level moreover, the pulse values can vary continuously. As a result, at the sampling instants, we could sample a real valued quantity and such a real number cannot easily

be represented using digital signals. A similar argument can be made for all orders higher than one. The author has not found any other filter possessing the same properties as the zero order hold that could allow an exact implementation of a higher noise shaping order ADC. However, high order pulse shapes can be approximated by means of continuous time finite-impulse-response (FIR) filters defined by digital delays [81] as will be shown in the next section.

3.4 Approximation of second order pulse shaping filters with a continuous time FIR filter

The ideal triangular impulse response (represented by the filter $h_2(t)$, Fig. 3.9(b), is not easily implementable in practice. Nevertheless, we might still think of approximating its impulse response through the staircase shape $h_{2,\mathrm{M}}(t)$, shown in Fig. 3.17. Here, the staircase steps have a width of T_s/M and there are $2M-1$ steps.

A conceptual realization of this idea is shown in Fig. 3.17(b). Here, the signal $d(t)$ coming from the PFM is filtered by a filter with impulse response $h(t)$ consisting of a square pulse of length T_s/M (filter $h(t)$). The output $p(t)$ of this first filter is then applied to a second filter with impulse response $g_\mathrm{M}(t)$. Finally, the output $y(t)$ of this second filter is sampled to generate the final output data $y[n]$. The impulse response of the filter $h(t)$ can be written as:

$$h(t) = \frac{M}{T_s}\left(u(t) - u\left(t - \frac{T_s}{M}\right)\right). \tag{3.15}$$

The second filter is a continuous time FIR filter [81] and its impulse response equals:

$$g_M(t) = \sum_{k=1}^{M}\left(k \cdot \delta\left(t - \left(k + \frac{1}{2}\right)\frac{T_s}{M}\right)\right) + \sum_{k=1}^{M-1}\left((M-k) \cdot \delta\left(t - \left(M + k + \frac{1}{2}\right)\frac{T_s}{M}\right)\right). \tag{3.16}$$

Now our staircase pulse shaper $h_{2,\mathrm{M}}(t)$ of Fig. 3.17(a) can be written as:

$$h_{2,\mathrm{M}}(t) = g_\mathrm{M}(t) * h(t), \tag{3.17}$$

where $*$ stands for the convolution. In the Laplace domain this corresponds to:

$$H_{2,\mathrm{M}}(s) = \frac{M}{T_\mathrm{s}} \cdot \frac{1 - e^{-s\frac{T_\mathrm{s}}{M}}}{s} \cdot \sum_{k=1}^{M}\left(k \cdot e^{-s(k+\frac{1}{2})\frac{T_\mathrm{s}}{M}} + (M-k) \cdot e^{-s(M+k+\frac{1}{2})\frac{T_\mathrm{s}}{M}}\right). \tag{3.18}$$

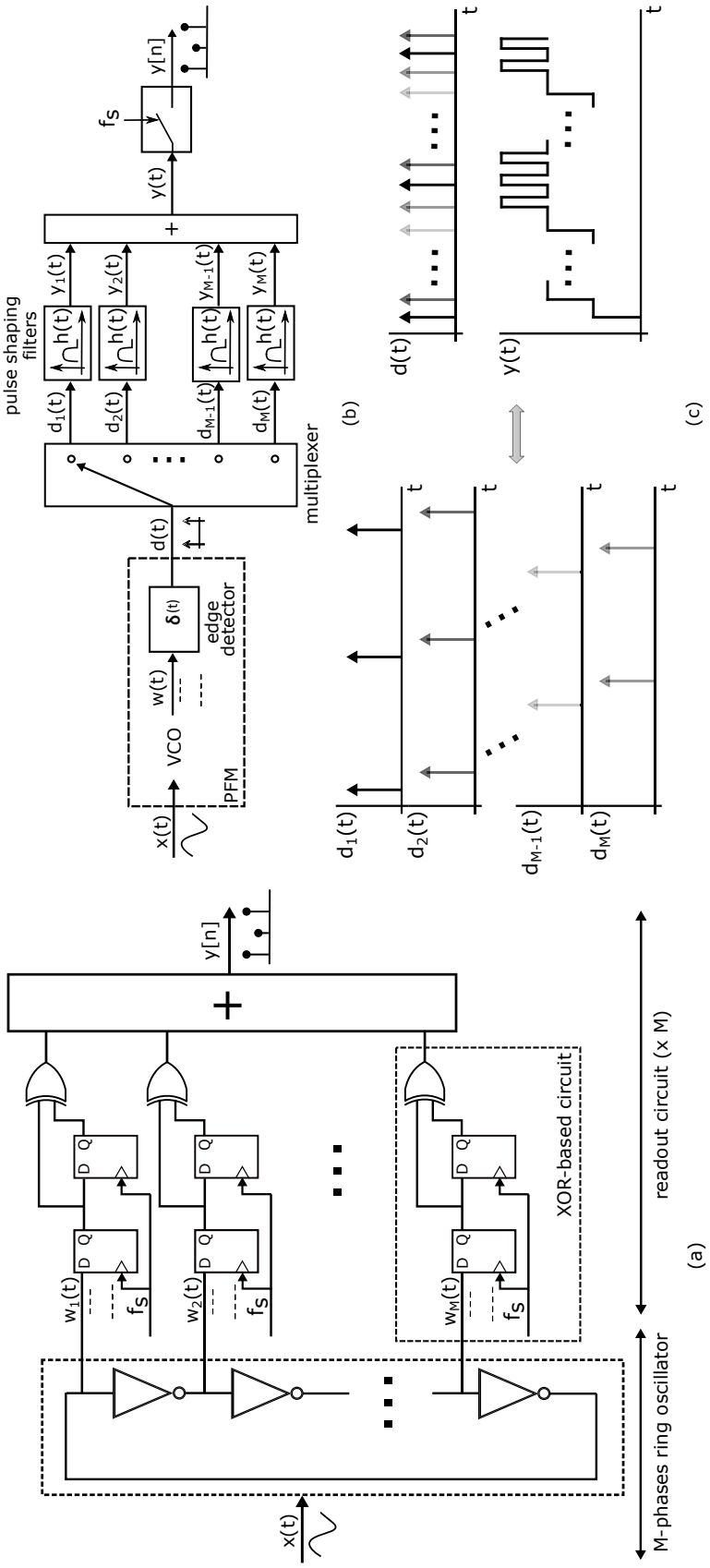


Figure 3.16: Ring oscillator based VCO-ADC concepts: (a) circuit, (b) conceptual diagram, and (c) time chronogram.

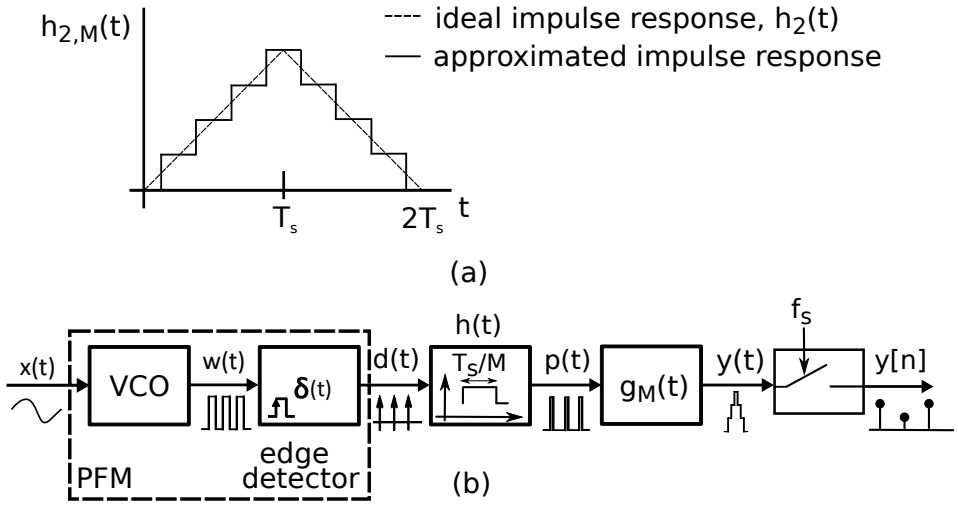


Figure 3.17: (a) Staircase approximation of the second order pulse shape and (b) a conceptual realization of the proposed idea which approximates second order spectral shaping.

If we calculate the limit when M approaches infinity, this becomes:

$$\lim_{M\to\infty} H_{2,\mathrm{M}}(s) = \frac{1}{T_\mathrm{s}^2} \cdot \frac{\left(1 - e^{-s\cdot T_\mathrm{s}}\right)^2}{s^2} = H_2(s). \tag{3.19}$$

Therefore, the $sinc^2(f)$ filter is asymptotically approximated for a sufficiently large value of M. Consequently, increasing the number of steps in the staircase filter $g_\mathrm{M}(t)$ will improve the performance of the system of Fig. 3.17(b) and bring it close to the ideal second order case.

For a practical realization of this idea, we can implement the analog FIR filter with a delay line composed of M delay elements [81], where each element introduces a delay of T_s/M. The proposed circuit is shown in Fig. 3.18(a). The implementation of such delay elements can be made with digital buffers that introduce a fixed continuous time delay in the digital signal.

To understand that this circuit indeed implements the system of Fig. 3.17(b), we need to apply some transformations. First, we have to interchange the order of the $g_\mathrm{M}(t)$ and $h(t)$ filters such that the FIR filter $g_\mathrm{M}(t)$ comes first. Second, the edge detection is also shifted to the back and is performed implicitly in the first (left) flip-flop of Fig. 3.18(a). The validity of this transformation can be understood by observing that the edges of the VCO signal $w(t)$ are the same as the edges of the (theoretical) Dirac delta train signal $d(t)$, and this is still true after passing through the delay line. The actual sampling is performed by the second (right) flip-flop in Fig. 3.18(b). Finally, the summation to implement the overall filter is implemented after the sampling of every tap in the delay line.

Fig. 3.18(b) shows a simulation result for the implementation of Fig. 3.18(a). The simulation was made with a delay line with 256 taps. For the rest, identical parameters were used as for the simulation of Fig. 3.11(b). Ideally this result should be very close to Fig. 3.11(b) and by comparison of the two figures, we

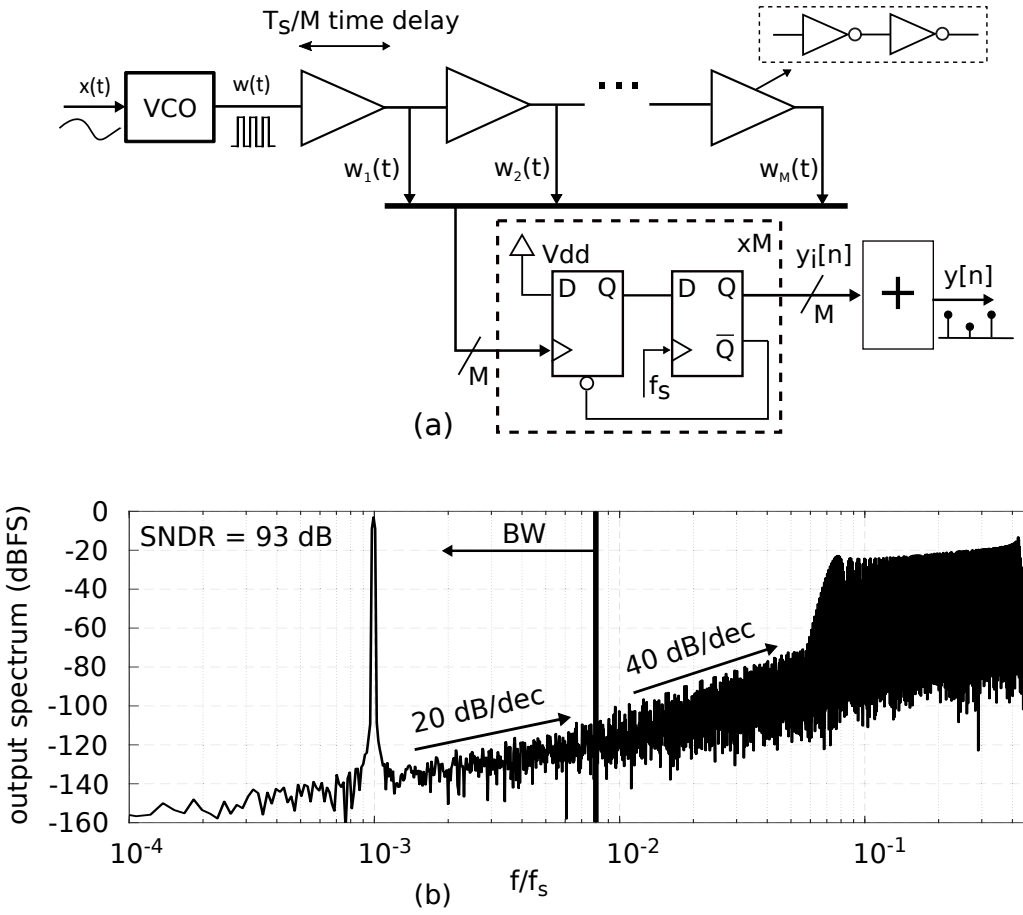


Figure 3.18: Practical implementation of the second order noise shaping approximation architecture: (a) circuit and (b) output spectrum for the case of a 256-tap approximation.

can see that this is true for a large part of the Nyquist band, where second-order noise shaping can clearly be observed. Also the corresponding SNDR of 93 dB at an OSR= 64 is very close to the ideal case. However, at very low frequencies, the limitation of the approximation becomes visible and only first-order spectral shaping can be observed in this frequency range. Note that in this case, 8 output bits are needed to represent the output signal $y[n]$.

Also for this case, simulations with mismatch in the delay line were performed. For a mismatch up to 1% in the delay of each tap of the delay line, no performance degradation is observed. However, for higher mismatch, the performance starts to degrade.

In Fig. 3.18(a), we used a single-phase VCO. However, the approximation to the second order case can also be applied to multiphase VCOs if the delay line is connected to each phase of the VCO (e.g. signals $w_i(t)$ in Fig. 3.16).

At this point we should note the difference between the architectures depicted in Fig. 3.18(a) and Fig. 3.16. Both of them are multibit architectures, but how the multibit output signal is constructed is very different from each other. Firstly, the filter that shapes the pulse frequency modulated signal $d(t)$ is not the same

for both cases (signal $d(t)$ in Fig. 3.18(a) would be the equivalent set of Dirac delta impulses obtained from signal $w(t)$). Whereas the pulse shaping filter for Fig. 3.18(a) is an approximation to a second-order sinc, the filter for Fig. 3.16 is a first-order sinc, regardless of the number of inverters in the ring oscillator. Consequently, we will not see second-order noise-shaping in the output spectrum of Fig. 3.16. Secondly, the delays of the inverters in the delay line of Fig. 3.18(a) are constant and signal independent as we want to implement a time invariant FIR filter. However, in a ring oscillator the inverter delays are modulated by the input signal $x(t)$, as described in the equivalent model of Fig.3.16(b) where the multiplexer advancement depends on the input signal $d(t)$. As depicted in Fig. 3.15(d), the high effective oscillation frequency makes the sampled output signal be multibit due to the overlapping between the pulses generated at the pulse shaping filters.

3.5 Detailed analysis of the first-order VCO-based ADC structure

After discussing the PFM-based interpretation of a generic order VCO-based ADC architecture and due to its importance, we will go one step further in the analysis and study of the first-order case.

A characterization of the quantization noise spectrum and the SNDR of first-order open-loop VCO-based ADC would represent a valuable design tool. VCO-based ADCs have been often described as first-order $\Delta\Sigma$ modulators [41, 43]. Based on these analyses, the SNDR of such converters has been defined for sinusoidal inputs using statistical models for quantization noise. In [64, 82] a formal analysis of a discrete-time first-order $\Delta\Sigma$ modulator showed that its quantization error displays a discrete spectrum. An analysis based on frequency modulation (FM) seems the natural way to model a VCO-based ADC. The spectrum of FM signals for sinusoidal inputs is well-known and was applied to VCO-based ADCs in [83]. However, direct application of FM spectral coefficients to VCO-based ADCs requires to demodulate the input signal, and this may not take us to intuitive mathematical calculations. In [69, 80] the link between quantization, first-order $\Delta\Sigma$ modulation and PFM was established.

In this section, we will use the PFM–VCO equivalence proposed previously to represent quantitatively the spectrum of an open-loop first-order VCO-based ADC. This brings two advantages. First, the discrete Fourier transform (DFT) of a finite sequence of a VCO-based ADC output can be calculated analytically considering all parameters, such as f_o and K_{VCO}. This result is not directly provided in [64]. The analytical calculation does not resort to statistical assumptions for quantization noise. Second, the proposed model does not require expressing the VCO-based ADC as a first-order $\Delta\Sigma$ modulator to prove first-order noise-shaping. Instead, the VCO-based ADC is modeled as a pulse frequency modulator whose spectral components produce first-order shaped aliases when sampled.

3.5.1 First-order open-loop VCO-based ADC architecture and PFM equivalence

From the previous sections we already know that the first-order VCO-based ADC architecture can be represented by the structure of Fig. 3.7, where the pulse shaping filter is the $sinc_1$ function. Keeping the same nomenclature and assumptions for the oscillation and the input signal parameters, the pulsed frequency modulated signal $d(t)$ follows (3.3). Then, signal $p(t)$ of Fig. 3.7 for the first order case will be defined as:

$$p(t) = h_1(t) * d(t) = \sum_{k=0}^{\infty} u\left(t - t_{\mathrm{k}}\right) - u\left(t - t_{\mathrm{k}} - T_{\mathrm{s}}\right), \quad \forall t_{\mathrm{k}} | \theta(t_{\mathrm{k}} = 2\pi k), \;\; k = 0, 1, ... \tag{3.20}$$

where $h_1(t)$ is the time-representation of $H_1(s)$ in (3.7).

Knowledge of the trigonometric series expansion of $p(t)$ permits us to calculate its Fourier transform, $P(\omega)$, which will be a sum of Dirac delta functions. Once $P(\omega)$ is known, we may calculate the DFT of $y[n]$ in Fig. 3.7, which allows us to predict the SNDR without running any simulation.

3.5.1.1 Oscillator spectrum before sampling

According to [71], (3.20) can be expanded into the following trigonometric series:

$$\begin{aligned} \omega_{\mathrm{o}} = 2\pi f_{\mathrm{o}}, \qquad \omega_{\mathrm{x}} = 2\pi f_{\mathrm{x}}, \\ p(t) = DC + BB \cdot \cos\left(\omega_{\mathrm{x}}\left(t - \frac{T_{\mathrm{s}}}{2}\right)\right) + \\ \sum_{q=1}^{\infty}\sum_{r=-\infty}^{\infty} CH\left(q, r\right) \cdot \cos\left(\left(q\omega_{\mathrm{o}} + r\omega_{\mathrm{x}}\right)\left(t - \frac{T_{\mathrm{s}}}{2}\right)\right), \\ DC = T_{\mathrm{s}} f_{\mathrm{o}}, \\ BB = \frac{AK_{\mathrm{VCO}}}{\pi f_{\mathrm{x}}}, \\ CH\left(q, r\right) = 2J_{\mathrm{r}}\left(q\frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}}\right)\frac{\sin\left(q\omega_{\mathrm{o}} + r\omega_{\mathrm{x}}\right)\frac{T_{\mathrm{s}}}{2}}{\pi q}. \end{aligned} \tag{3.21}$$

This series contains a constant component (DC) and a baseband component (BB) that represents the input signal $x(t)$. Coefficients $CH(q, r)$ represent the amplitude of the harmonics of the rest oscillation frequency f_{o} and the sideband tones around such harmonics. Integer q indexes the harmonics of f_{o} and integer r indexes the sideband tones around each harmonic at qf_{o}. The sinc transfer function corresponds to the pulse shaping filter $h_1(t)$. It is reflected into coefficient $CH(q, r)$, which is zero at integer multiplies of f_{s}, as opposite to the trigonometric expansion of $d(t)$ (3.3). The attenuation and phase shift of $x(t)$ due to $h_1(t)$ are also reflected in BB. The Fourier transform $P(\omega)$ will be a sum of Dirac deltas

weighted by the coefficients expressed in (3.21):

$$\begin{aligned} P(\omega) = 2\pi \cdot DC \cdot \delta(\omega) + \\ \pi \cdot BB \cdot \left(e^{j\omega_{\mathrm{x}} \frac{T_{\mathrm{s}}}{2}} \delta(\omega + \omega_{\mathrm{x}}) + e^{-j\omega_{\mathrm{x}} \frac{T_{\mathrm{s}}}{2}} \delta(\omega - \omega_{\mathrm{x}}) \right) + \\ \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} \pi \cdot CH(q,r) \cdot \left(e^{j(q\omega_{\mathrm{o}} + r\omega_{\mathrm{x}}) \frac{T_{\mathrm{s}}}{2}} \delta(\omega + (q\omega_{\mathrm{o}} + r\omega_{\mathrm{x}})) \right) + \\ \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} \pi \cdot CH(q,r) \cdot \left(e^{-j(q\omega_{\mathrm{o}} + r\omega_{\mathrm{x}}) \frac{T_{\mathrm{s}}}{2}} \delta(\omega - (q\omega_{\mathrm{o}} + r\omega_{\mathrm{x}})) \right). \end{aligned} \tag{3.22}$$

We have represented in Fig. 3.19(a) part of the modulus of $P(\omega)$ predicted by (3.22). The parameters used are the following: $f_{\mathrm{s}} = 1$, $f_{\mathrm{o}} = 1/4$, $K_{\mathrm{VCO}} = 1/16$. The input signal is a -6 dBFS sinusoidal wave at $f_{\mathrm{x}} = 1/8192$. The modulus of $H_1(\omega)$ is also represented in Fig. 3.19(a) as a dotted line. We have marked the tones weighted by $CH(q,r)$ corresponding to the sidebands of the first three harmonics of f_{o}. The harmonic sidebands represented by $CH(q,r)$ occupy a bandwidth that increases with q and whose average level decays with q. After some harmonics, the sidebands overlap resembling a noise shaped by $H(\omega)$. We may also observe in Fig. 3.19(a) the gap between the harmonic sidebands and DC, inside of which the sideband energy is small. If the input analog bandwidth of the ADC fits in this gap, the input signal will be encoded in $p(t)$ with nearly no error.

As a comparison, Fig. 3.19(b) represents the modulus of $P(\omega)$ plotted with the data obtained from a behavioral model similar to Fig. 3.13 (which is the ADC implementation of Fig. 3.7 when first-order in the pulse shaping filter is considered), and with the same parameters as in Fig. 3.19(a). In Fig. 3.19, we may observe the agreement between the simulated and the calculated values of $P(\omega)$ and also the nulls imposed by $H_1(\omega)$.

3.5.1.2 Sampled spectrum

Our interest is obtaining a sampled sequence of integer values that may represent the input signal $x(t)$ by means of pulse modulated signal $p(t)$. Therefore, we can predict the DFT of a finite set of N samples of $y[n]$, as is usually done to evaluate the performance of an ADC. This DFT can be easily calculated if the input tone at f_{x}, the sampling frequency f_{s}, the rest oscillation frequency f_{o} and the sequence length N are all linked by integer factors K_{s}, K_{o} and K_{x} as follows:

$$f_{\mathrm{s}} = 2K_{\mathrm{s}} \cdot f_{\mathrm{x}} \quad f_{\mathrm{o}} = K_{\mathrm{o}} \cdot f_{\mathrm{x}} \quad N = 2K_{\mathrm{x}}K_{\mathrm{s}}. \tag{3.23}$$

These definitions force all tones in the spectrum of $p(t)$ to fit into a bin of the DFT of $y[n]$. All DFT bins that are not an integer multiple of K_{x} will be zero. Therefore, the DFT of $y[n]$ may be indexed by an integer k (k = 0,1,2,) multiplied by K_{x}. In practice, $f_{\mathrm{x}} << f_{\mathrm{o}}$ and we may find an integer K_{o} that closely approximates the desired f_{o}. We may evaluate $Y[kK_{\mathrm{x}}]$, the DFT of $y[n]$, using the coefficients of $P(\omega)$. A delta located at frequency ω in $P(\omega)$ will alias to DFT

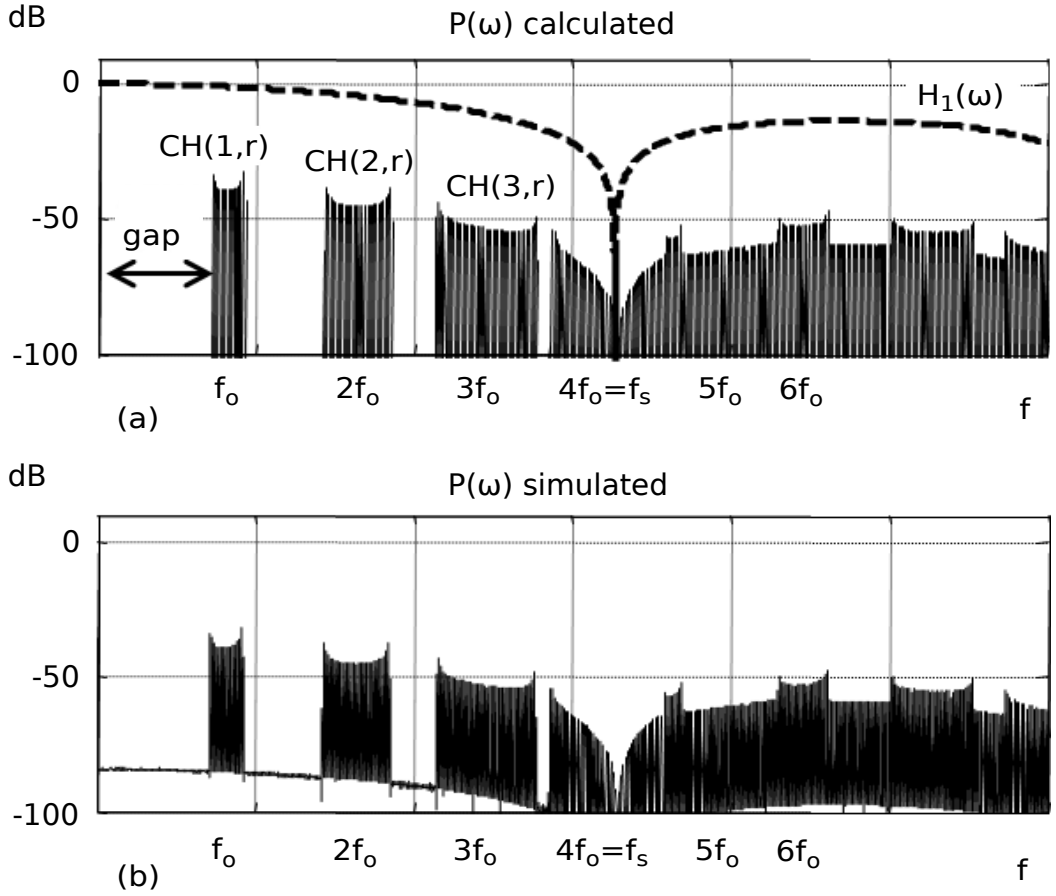


Figure 3.19: Modulus of $P(\omega)$: (a) calculated, and (b) simulated.

bin kK_{x} as follows:

$$\begin{aligned} \omega(q,r) &= q\omega_{\mathrm{o}} + r\omega_{\mathrm{x}} = q\omega_{\mathrm{x}}K_{\mathrm{o}} + r\omega_{\mathrm{x}} \\ k &= \mathrm{mod}\left(qK_{\mathrm{o}} + r, 2K_{\mathrm{s}}\right), \quad k = 0...2K_{\mathrm{s}} - 1. \end{aligned} \tag{3.24}$$

In (3.24), "mod" represents the reminder of the integer division by $2K_{\mathrm{s}}$. To calculate the DFT for the bin kK_{x}, it suffices to add all the complex coefficients of the Dirac deltas in $P(\omega)$ that alias to that particular index k. Let $R(k)$ be the set of all pairs (q,r) of integers complying with condition (3.24). The values of $Y[kK_{\mathrm{x}}]$ are calculated in (3.25). To calculate $Y[kK_{\mathrm{x}}]$, we have approximated the DFT bins of the DC component and input signal component BB neglecting the contributions of the rest frequency harmonic sideband aliases due to their proximity to the nulls of sinc function $H_1(\omega)$.

$$\begin{aligned} R(k) &= \left\{q \in \{1...\infty\}, r \in \{-\infty...\infty\} / k = \mathrm{mod}\left(qK_{\mathrm{o}} + r, 2K_{\mathrm{s}}\right)\right\} \\ Y[0] &\approx T_{\mathrm{s}} f_{\mathrm{o}} \quad BB = \frac{AK_{\mathrm{VCO}}}{\pi f_{\mathrm{x}}} \sin\left(\frac{\pi}{2K_{\mathrm{s}}}\right) \\ CH(q,r) &= \frac{2}{\pi q} J_{\mathrm{r}}\left(q\frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}}\right) \sin\left(\left(qK_{\mathrm{o}} + r\right)\frac{\pi}{2K_{\mathrm{s}}}\right) \end{aligned}$$

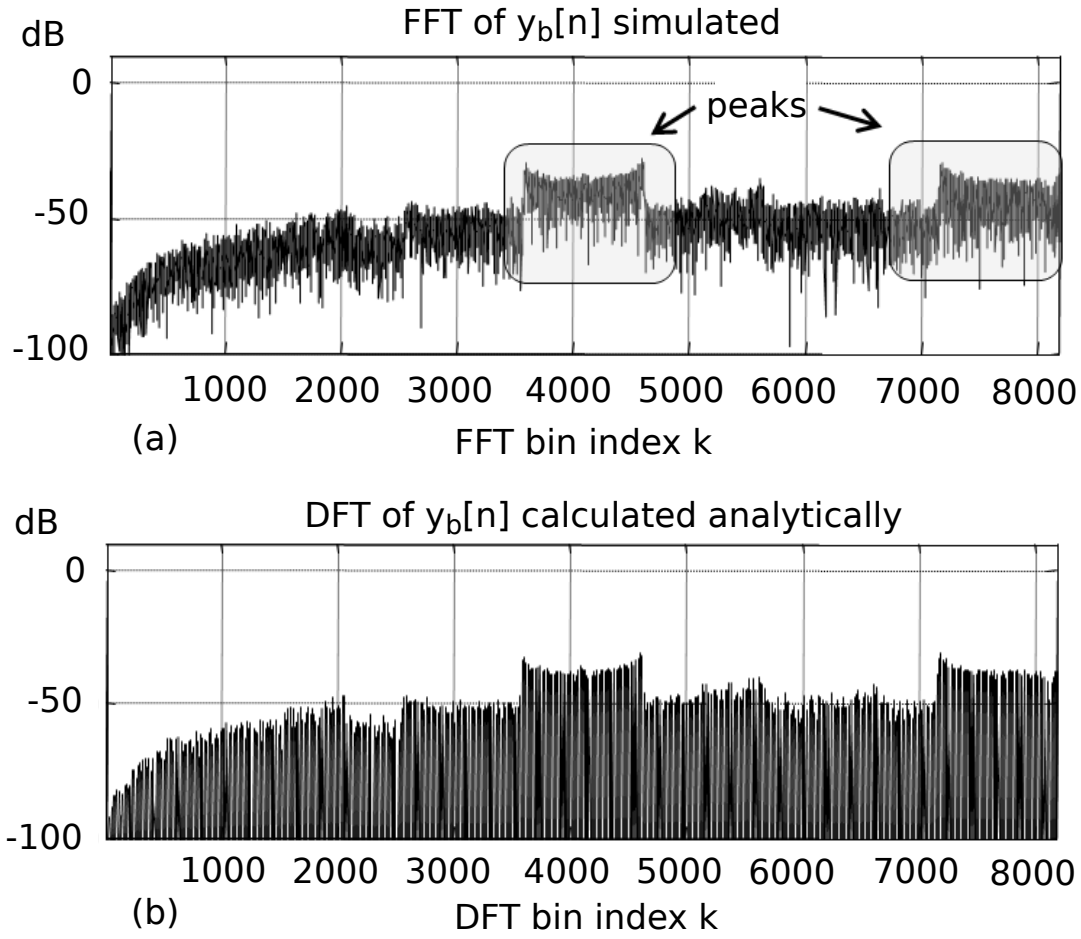


Figure 3.20: Simulated spectrum (a) and calculated spectrum (b) of $y[n]$.

$$
\begin{aligned}
Y[K_\mathrm{x}] \approx BB \cdot e^{-j\frac{\pi}{2K_\mathrm{s}}} \quad Y[N-K_\mathrm{x}] \approx BB \cdot e^{j\frac{\pi}{2K_\mathrm{s}}} \\
Y[kK_\mathrm{x}] = \sum_{R(k)} CH(q,r) e^{-j\frac{\pi}{2K_\mathrm{s}}(qK_\mathrm{o}+r)} / k = \mathrm{mod}\,(qK_\mathrm{o}+r, 2K_\mathrm{s}) \\
2 \le k \le K_\mathrm{s}-1 \\
Y[kK_\mathrm{x}] = \sum_{R(k)} CH(q,r) e^{j\frac{\pi}{2K_\mathrm{s}}(qK_\mathrm{o}+r)} / k = \mathrm{mod}\,(qK_\mathrm{o}+r, 2K_\mathrm{s}) \\
K_\mathrm{s} \le k \le 2K_\mathrm{s}-2. \qquad (3.25)
\end{aligned}
$$

Fig. 3.20(a) shows a 16K point fast Fourier transform (FFT) of $y[n]$ obtained by behavioral simulation, considering the same parameters as in Fig. 3.19. The peaks at high frequency are the modulation components around each multiple of the rest oscillation frequency. In addition, they reveal that considering a white noise model for the quantization noise is not a good approximation. We have applied (3.25) to reproduce the simulation of Fig. 3.20(a) by analytical calculation of Y[k]. The result is shown in Fig. 3.20(b), which replicates the peaks and shape of Fig. 3.20(a).

3.5.1.3 SNDR prediction

Equation (3.25) describes analytically the spectrum of $y[n]$. Hence, it is possible to predict the SNDR of the ADC from it. For this purpose, we only need to calculate the DFT bins of $Y[kK_\mathrm{x}]$ that lie inside the BW defined by $\mathrm{f_s}$ and OSR. We may define index k_BW as the closest DFT bin index corresponding to the edge of the BW. Then, the value of the SNDR will be:

$$k_\mathrm{BW} = \mathrm{int}\left(\frac{K_\mathrm{s}}{\mathrm{OSR}}\right)$$
$$\mathrm{SNDR}(dB) = 10\log_{10}\frac{|Y[K_\mathrm{x}]|^2}{\sum_{k=2}^{k\mathrm{BW}}|Y[K_\mathrm{x}]|^2} \tag{3.26}$$

If we observe (3.25), we will see that each set $R(k)$ contains an infinite number of values of q and r. However, $CH(q,r)$ quickly decreases away from the center frequency harmonics, as shown in Fig. 3.19. Therefore, to practically calculate (3.26), we may define some bounds for q and r to truncate the summation. A simple algorithm to calculate the SNDR is described next. Coefficients $Y[kK_\mathrm{x}]$ can be computed by adding all the tone complex coefficients (3.25) that alias into DFT bin kK_x. We will establish a noise floor Y_ref below in which a term $CH(q,r)$ in (3.21) can be discarded. As larger values of $CH(r,q)$ correspond to smaller values of q, we will start at $q=1$ and sweep index r. When Y_ref is reached in the computation of $CH(q,r)$, we no longer need to increase r and can jump to the next value of q. If the resulting index k (3.24) is above k_ABW, it can be discarded, which significantly speeds the computation of SNDR.

Fig. 3.21 shows a comparison between the dynamic ranges obtained by the behavioral simulation of Fig. 3.13 (simulated SNDR), and the proposed method (calculated SNDR), considering an $OSR = 64$ and $f_\mathrm{s} = 1$. In Fig. 3.21, two cases have been plotted ((a) and (b)) to evaluate different rest oscillation frequencies f_o, VCO gain constants K_VCO and input tone frequencies f_x. The SNDR calculations were performed with 32K point FFTs and Y_ref = -150 dBFS. The simulations deviate from the analytical calculations in less than 0.7 dB.

So far, our discussion has been limited to the first-order single-phase VCO-based structure, which produces a single-bit output data stream. However, the proposed approach to analytically calculate the spectrum can be easily extended to multiphase VCOs as will be shown next.

3.5.2 Extension to first-order noise shaping architectures with multiphase VCOs

In the previous sections, we discussed the analogy between a VCO-based ADC and a PFM. This analogy allows analytical calculation of the DFT of the output sequence and expected SNDR of the converter. The discussion was limited to the single-phase architecture. However, most of the practical VCO-based ADCs are constructed using multiphase architectures that produce multibit output data. Consequently, the analysis made before should be extended to multiphase VCO-based systems. Even more, most of the multiphase VCO-based ADCs are im-

plemented with ring oscillators, so we will focus our approach on the study of multiphase ring oscillators. In addition, a novel architecture will be proposed to implement a multiphase pulse frequency modulator with an architecture slightly different from the ring oscillator based one. The analytical calculation of the DFT will also be made for the case of the new architecture.

3.5.2.1 Multiphase ring oscillator based ADC

The spectral properties of a multiphase VCO-based ADC are retained in the single-phase case if an equivalent model is employed. This means that similar equations used to study the performance of single-phase systems can also apply to the multiphase case.

The conventional architecture of a ring oscillator based ADC is shown in Fig. 3.22(a). This VCO-based ADC is composed of a ring of M (odd) inverters whose delays are controlled by the amplitude of the input signal $x(t)$. The multiphase oscillator output is formed by sampling all the VCO phases $w_{\mathrm{i}}(t)$ at f_{s} and making the first difference (in this case with an XOR gate). The practical implementation of this circuit was shown in Fig. 3.16(a). Finally, individual outputs $y_{\mathrm{i}}[n]$ are added into a multibit signal to generate the multibit output data $y_{\mathrm{mb}}[n]$. Each VCO output can be individually seen as a single-phase architecture (similar to those architectures studied in the previous section), so that the VCO-PFM equivalence of Fig. 3.2 also applies here. Then, Fig. 3.22(a) turns into Fig. 3.22(b). To keep the same notation as in the single-phase case, we suppose that the edge detector only responds to the rising edges of the VCO. Accordingly, the ring oscillator of Fig. 3.22(b) must oscillate twice than the ring oscillator of Fig. 3.22(a). In Fig. 3.22(b) we can seize the linearity of filters $h(t)$ to swap them with the samplers and collapse all the signals into a single filter $h(t)$. We suppose that the ring oscillator follows (2.19). Provided that signal $d(t)$ is the sum of M signals with oscillation frequency f_{osc} and that each output is phase shifted by π/M, we will have in $d(t)$ a Dirac delta impulse stream of frequency $2M \cdot f_{\mathrm{osc}}$. Then, a multibit VCO-based ADC can be represented by an equivalent single-bit PFM but scaled in frequency by a factor of $2M$. If we apply this scaling to (3.21) and (3.25), the result will analytically describe the DFT of $y_{\mathrm{mb}}[n]$. Finally, we calculate the SNDR of the system by (3.26).

To validate the proposed equivalence, Fig. 3.23(a) depicts the FFT obtained by behavioral simulation of a 5-phases multibit VCO-based ADC example ($M = 5$). Fig. 3.23(b) shows the DFT calculated analytically through (3.25) and the equivalence proposed before. The parameters used in the system are the following: $f_{\mathrm{s}} = 1$ GHz, $OSR = 32$, $f_{\mathrm{osc}} = K_{\mathrm{VCO}} = 125$ MHz. A -8 dBFS sinusoidal waveform with $f_{\mathrm{x}} = 2$ MHz is used as input signal. The obtained SNDR is 50 dB in both cases.

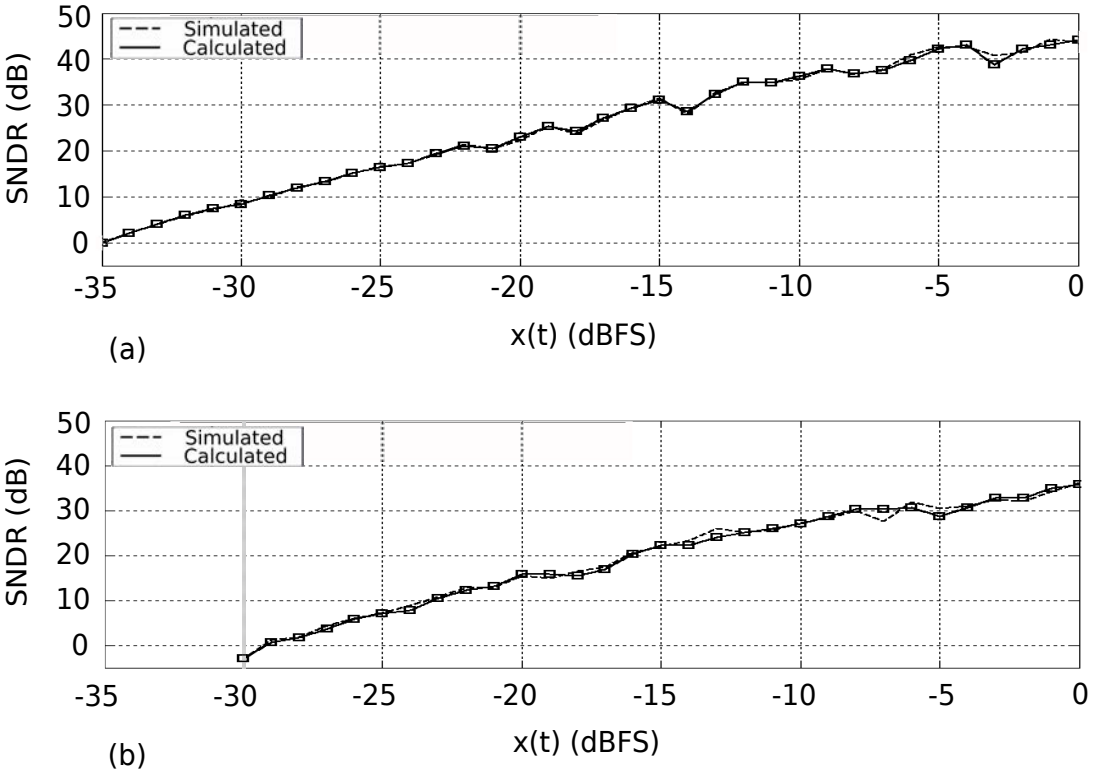


Figure 3.21: Dynamic range comparison: (a) $f_o = f_s/16$, $K_{VCO} = f_s/32$, $f_x = f_s/8192$; (b) $f_o = f_s/32$, $K_{VCO} = f_s/128$, $f_x = f_s/4096$.

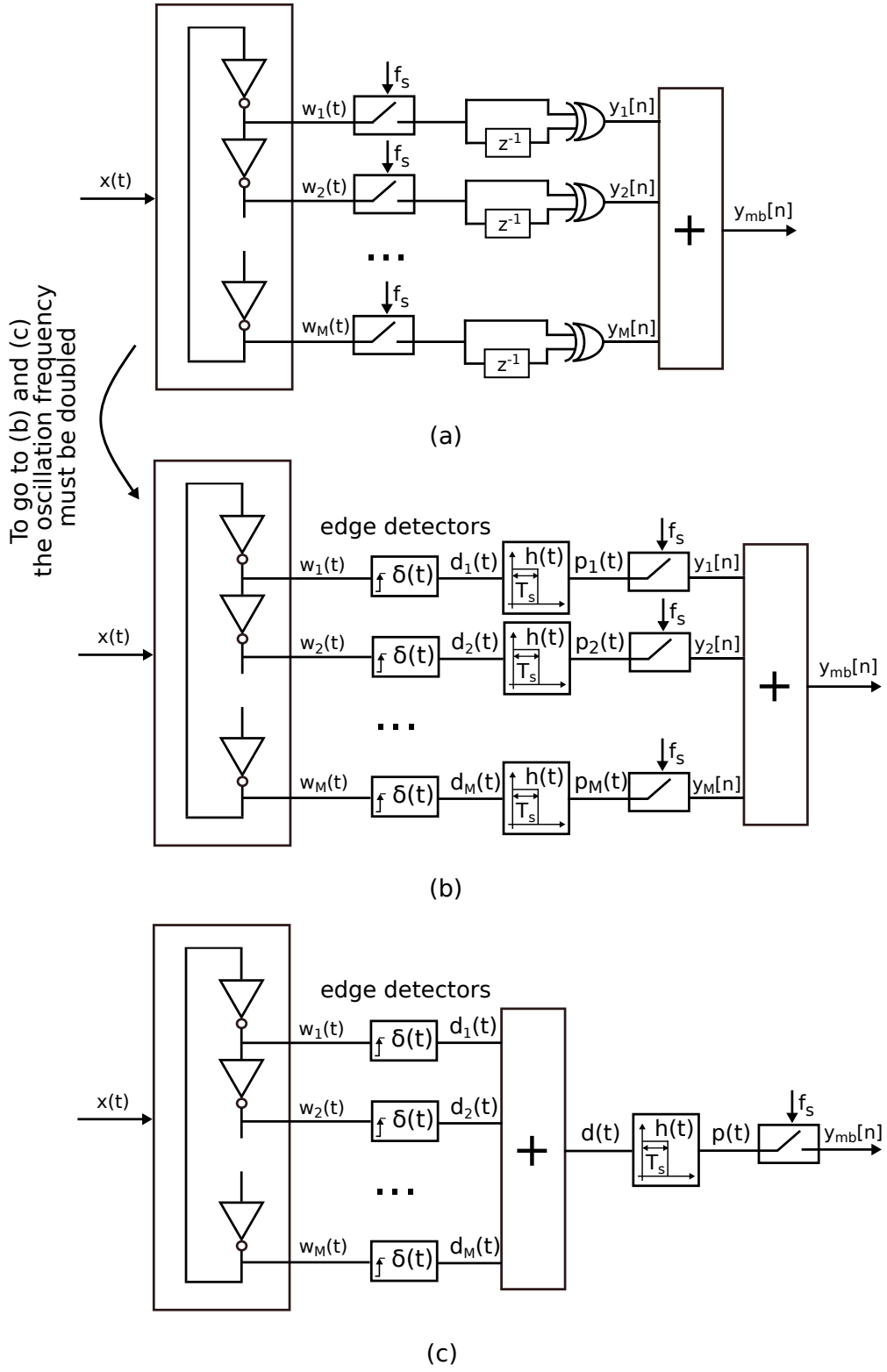


Figure 3.22: (a) Conventional ring oscillator based ADC, (b) replacing of the first difference by an edge detector and a filter, and (c) simplification to use one filter and one sampler.

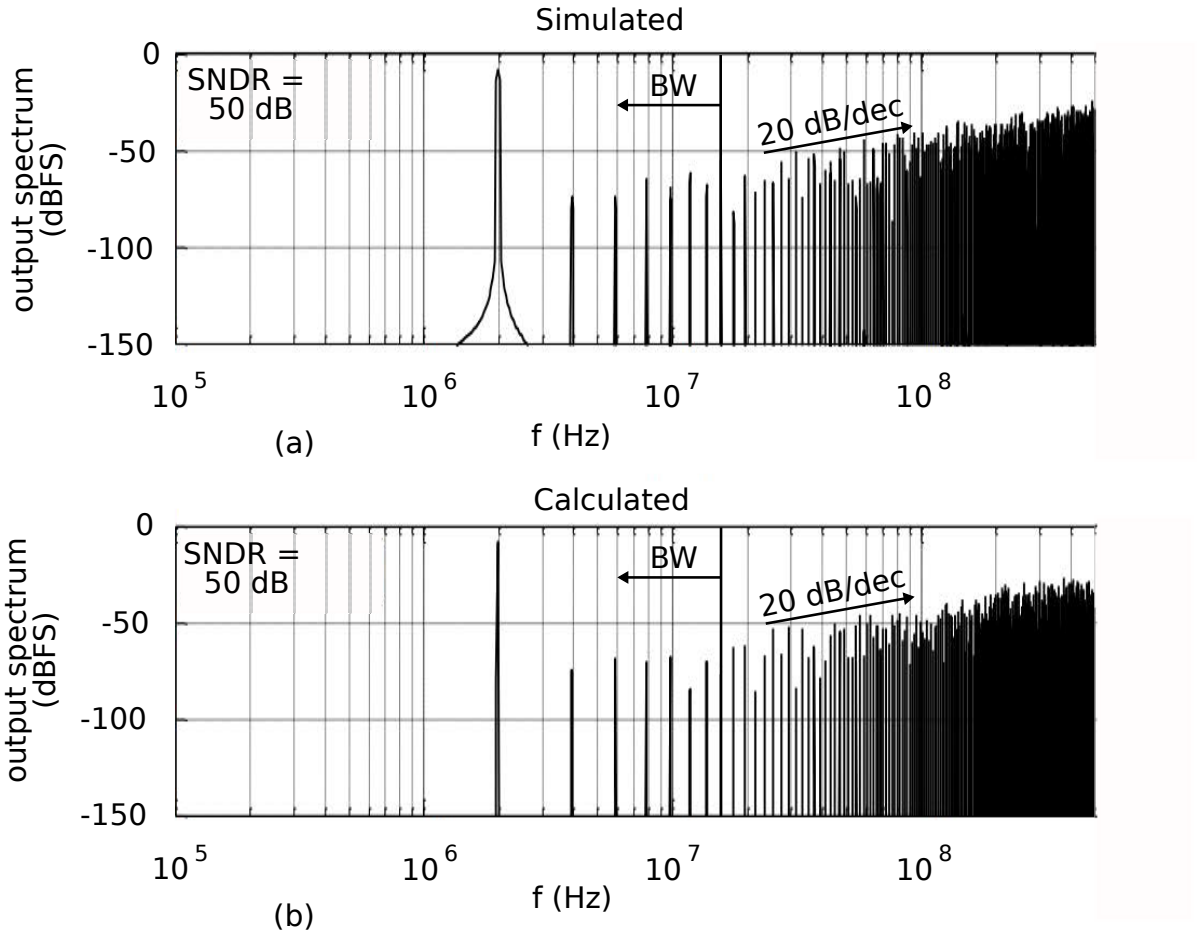


Figure 3.23: (a) Simulated spectrum, and (b) calculated spectrum for a multiphase VCO-based ADC.

In Fig. 3.23 the consistency of the proposed equivalency can be observed. Both spectra are similar and result in the same SNDR value, with slight differences due to estimation accuracy in (3.25). Additionally, it can be appreciated that no peaks are visible in the spectra, differently from Fig. 3.20. This occurs because the effective oscillation frequency is higher than the sampling frequency according to the multiphase architecture.

With the goal of making a complete checking of the proposed equivalence, Fig. 3.24 shows the dynamic range of the 5-phases VCO-based ADC in Fig. 3.23 obtained by behavioral simulation (dashed line). As a comparison, the solid line in Fig. 3.24 shows the dynamic range obtained from the estimation of 3.25. The parameters used are the same as in Fig. 3.23. In Fig. 3.24, similar results between the two ways of estimating the dynamic range can be observed. The largest difference is around 2 dB, due to accuracy limitations. Both methods predict a dynamic range value equal to 42 dB.

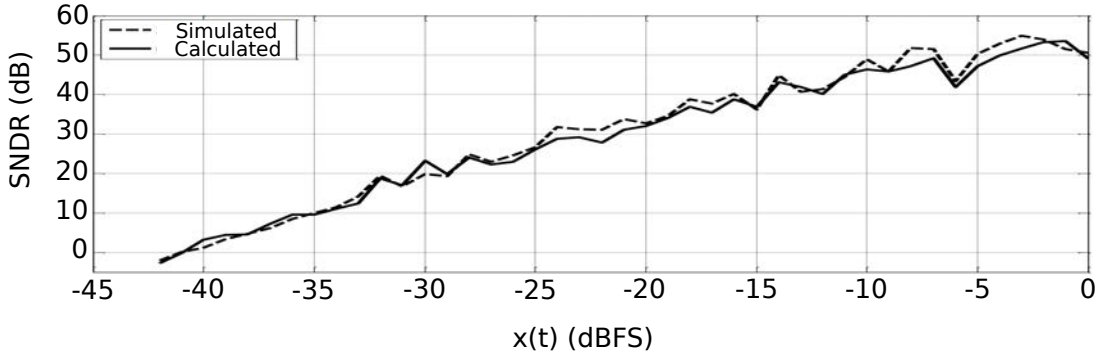


Figure 3.24: Simulated and estimated dynamic range of the same system of Fig. 3.23.

3.5.2.2 Multiphase PFM-based ADC

The PFM-based concepts are fundamental for the derivation of the theory applied to VCO-based ADCs made in this document. However a pulse frequency modulator can also be applied to build other noise-shaped ADCs. Similar approaches, as made for multiphase ring oscillators based ADCs, can be used to perform a theoretical analysis of the behavior of ADCs implemented with pulse frequency modulators. At present, we will not focus on the circuitry required to implement a multibit PFM based ADC yet, but will pay attention to a behavioral model of the system. This system will help us to support the explanations and the derivation of the theoretical equations.

We already know how to model a single-bit PFM-based ADC (Fig. 3.13). Extending this structure to a multibit one can be accomplished if we place a time delay chain composed of several taps after the filter $h(t)$. If we sample the outputs of the taps and sum all of them into a unique signal, the final signal will be a multibit one. Fig. 3.25(a) depicts a diagram scheme of the proposed system, where we can see the new delay line. The delay line is composed of N taps. Each tap has a nominal delay equal to T_s/N. Fig. 3.25(a) will be used later on because it is one of the architectures implemented in practice on silicon.

Fig. 3.25(b) shows how signals are distributed in time. It can be seen that the pulse frequency modulated signal $p(t)$ is connected to the delay line and the outputs of the taps are combined into a multibit signal $y_\mathrm{N}(t)$. Conversely to a multiphase ring oscillator, the delay introduced in the oscillator by each tap of the delay line is always the same. This means that the output data in both architectures are different.

Nevertheless, the multibit spectrum in the case of Fig.3.25(a) can also be calculated using the an equivalent approach as made in the previous section. We may apply (3.21) to each of the individual outputs $p_\mathrm{i}(t)$. Then, output signal $y_\mathrm{N}(t)$ could be expanded as a trigonometric series resulting from the addition of each series expansion of $p_\mathrm{i}(t)$ suitably shifted in time by T_s/N. For the i^{th} output $p_\mathrm{i}(t)$, we will make the following variable change in (3.21):

$$t' = t - \frac{T_\mathrm{s}}{N} \cdot i, \qquad i = 1...N. \tag{3.27}$$

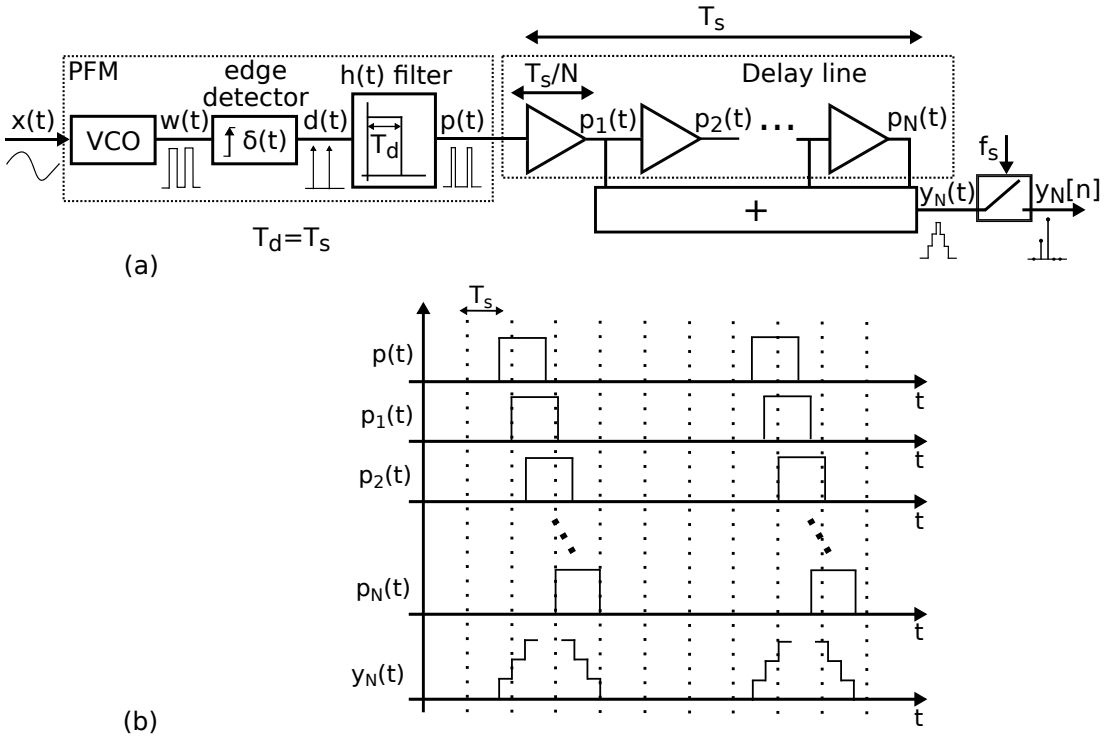


Figure 3.25: (a) Behavioral model of a multibit PFM-based architecture, and (b) chronogram of the pulse frequency modulated signals.

Coefficients DC, BB and CH remain the same as in (3.21). Accordingly, $y_{\mathrm{N}}(t)$ in Fig.3.25(a) can be calculated as follows:

$$y_{\mathrm{N}}(t) = N \cdot DC + BB \cdot \sum_{i=1}^{N} \cos\left(\omega_{\mathrm{x}}\left(t' - \frac{T_{\mathrm{s}}}{2}\right)\right) + \sum_{q=1}^{\infty}\sum_{r=-\infty}^{\infty} CH(q,r) \sum_{i=1}^{N} \cos\left((q\cdot\omega_{\mathrm{o}} + r\cdot\omega_{\mathrm{x}})\left(t' - \frac{T_{\mathrm{s}}}{2}\right)\right). \tag{3.28}$$

The proposed variable change can be analytically calculated by noting that:

$$\sum_{i=1}^{N} \cos\left(t - \frac{T_{\mathrm{s}}}{N}\cdot i\right) = I\cdot\sin(t) + Q\cdot\cos(t).$$
$$Q = 0.5\cdot\frac{1+\cos\left(\frac{N-1}{N}\cdot T_{\mathrm{s}}\right) - \cos(T_{\mathrm{s}}) - \cos\left(\frac{T_{\mathrm{s}}}{N}\right)}{1-\cos\left(\frac{T_{\mathrm{s}}}{N}\right)}.$$
$$I = 0.5\cdot\frac{1+\sin\left(\frac{N-1}{N}\cdot T_{\mathrm{s}}\right) - \sin(T_{\mathrm{s}}) - \sin\left(\frac{T_{\mathrm{s}}}{N}\right)}{1-\cos\left(\frac{T_{\mathrm{s}}}{N}\right)}. \tag{3.29}$$

We have replicated the simulations of the previous section to verify the applicability of the proposed method. Fig. 3.26 shows a dynamic range obtained from a behavioral model of the system of Fig. 3.25(a) in dashed line. The equivalent data was calculated analytically using (3.28) and (3.29), shown in solid line in

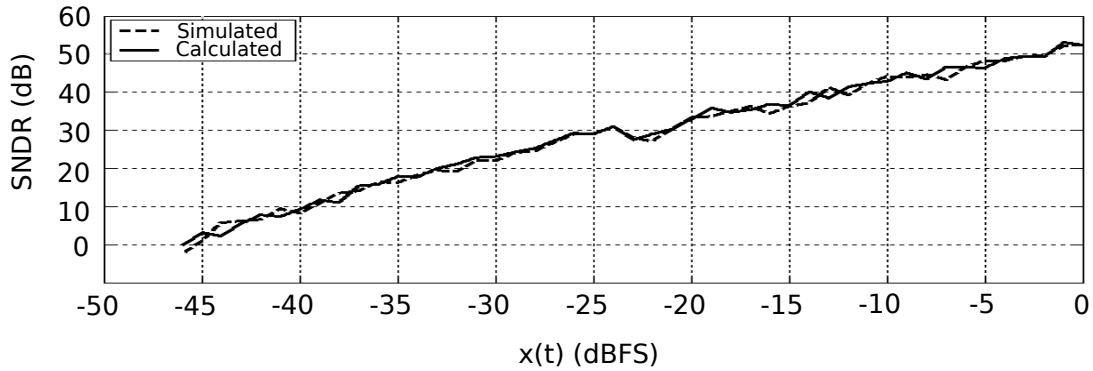


Figure 3.26: Simulated and estimated dynamic range the multibit PFM-based ADC architecture.

Fig. 3.26. The dynamic range refers to a multibit PFM-based ADC with eight taps in the delay line, $f_s = 1$ GHz, OSR= 32, $f_o = 250$ MHz, $K_{VCO} = 125$ MHz.

The similarity between both dynamic ranges can be appreciated, showing differences below 2 dB between them. The dynamic range obtained is equal to 46 dB in both cases.

3.6 Conclusion

We have shown a novel methodology to analyze and design VCO-based ADCs with extended noise shaping properties. The key element of the approach is that the VCO is considered as a signal encoder, instead of the typical interpretation where the VCO is viewed as a phase integrator. For this, an exact equivalence between a PFM and a VCO is established. This equivalence allows to reveal the fundamental PFM encoding error which forms an ultimate limitation of any VCO-based ADC and which was quantified in Fig. 3.6.

In a next step, we used the PFM interpretation for a direct construction of the generic VCO-based ADC of Fig. 3.7. We have shown that the noise shaping order of this VCO-based ADC architecture is determined by the filter that shapes the modulation components of the VCO. Ideally, if the correct filter was chosen, any noise shaping order architecture could be designed. Whereas the version with first order spectral turns out to be easy to implement, unfortunately, the ideal high order variants turn out to be complicated to implement in practice. As a partial solution for this limitation, we have proposed a practical technique to approximate the second order case through the use of a FIR filter composed of a delay line.

Finally, we went one step further for the first-order case, through the analytical calculation of the DFT of the output sequence and expected SNDR for single tone inputs. The mathematical derivations have been verified by evaluating the dynamic range of a VCO-based ADC example by calculations and by a behavioral simulation, achieving a 0.7 dB mismatch for the single-phase case. The approach was also extended to multiphase structures. To prove this extension, the equivalence between the single-phase case and the multiphase one

was established, which enables to apply the equations of the single-phase case to the multiphase case. Similar comparisons between mathematical derivations and simulations were made for this case, showing a maximum SNDR deviation of 2 dB between them. The analyzed multiphase architectures were the conventional multiphase ring oscillator based ADC and a novel PFM-based architecture that makes use of a digital delay line to generate a multibit output. This last architecture will be analyzed in depth in the following chapters.

Part II

New VCO-based ADC architectures based on pulse frequency modulation

Chapter 4

VCO-based single stage architectures

Once established the theory for the PFM–VCO equivalence, we will apply it to the proposal of new VCO-based architectures and also to the analysis of already known architectures. In this chapter, we will focus on single stage architectures. Firstly, we will deal with open-loop structures, and then we will make a first approach to closed-loop structures.

We will also talk about one of the most important and limiting drawbacks of VCO-based ADCs, which is the non-linear VCO voltage-to-frequency transfer function, particularly in ring oscillators. A non-linear voltage-to-frequency relation in the VCO will degrade the performance of open-loop VCO-based ADCs. Distortion will appear in the final output data and the SNDR will be strongly restricted. To provide an example to the reader, if we took the system shown in Fig. 2.10(c) (without any distortion compensation technique applied to the VCO) and supposed that the VCO is a ring oscillator, the expected SNDR would not be more than 45 dB for high amplitude input signals placed, for instance, at BW/8 (in order to make the distortion fall in-band). This limit is empirical, but can be observed by simulations. Note that we have considered a high amplitude input signal. Then, we may use a low amplitude input signal to decrease the distortion and achieve a good performance. Unfortunately, this is not always possible. For instance, in communication applications, high crest factor signals are common to many modulations such as orthogonal frequency-division multiplexing (OFDM) or quadrature amplitude modulation (QAM). Consequently, this is not a generic solution that applies to all the possible environments.

In the following sections we will describe two techniques to mitigate the non-linearity of the VCO that have been proposed and developed along the years of research. As a first approach, we will talk about a digital precoding technique to make the VCO oscillate only at two possible oscillation frequencies, so that it behaves in a linear way. Secondly, a PFM-based circuit that is inherently linear will be described. Both of them will be studied making use of the PFM interpretation.

In this chapter, we will limit the discussion of these techniques to the theoretical domain. However, in collaboration with the company Intel Austria GmbH, these two architectures were implemented on silicon using a 40-nm complementary

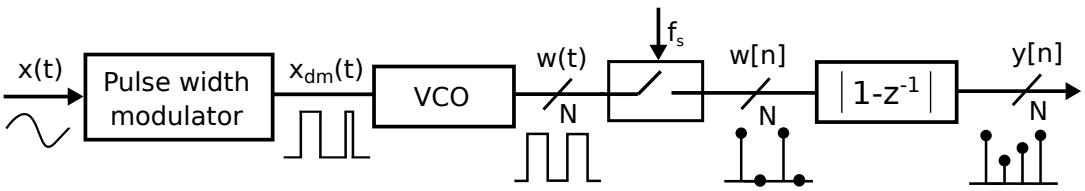


Figure 4.1: Open-loop VCO-based ADC with pulse width modulator.

metal-oxide-semiconductor (CMOS) process. This allowed us to experimentally check the performance obtained from a theoretical point of view. We will describe the circuits implemented on those chips, the measured performance and all the non-linear effects observed from the simulations and the measurements, later on, in Chapter 6 (digital precoded system) and in Chapter 7 (PFM-based system).

Finally, we will make a first approach to the implementation of continuous-time $\Delta\Sigma$ modulators with VCOs (closed-loop structures). We will use the equations derived from the PFM theory to explain the performance of these structures and to propose practical applications.

4.1 Digital precoding

As stated above, one of the main limitations of the VCO-based ADCs implemented with ring oscillators is the non-linear voltage-to-frequency conversion. One technique that can be applied to fix this issue involves employing some kind of digital modulation between the input signal and the VCO. This way, the VCO input signal is digital, so that the VCO will oscillate at only two possible oscillation frequencies. Therefore, the voltage-to-frequency relation will be inherently linear. In a generic way, the simplest architecture that can be designed with this technique will follow the scheme depicted in Fig. 2.13. There are several types of digital modulation that can be used [58]. Nevertheless, pulse width modulated signals have been the typical choice in practice [54–56,72,84]. The resulting system would look as in Fig. 4.1. This technique allows us to solve the VCO non-linearity, however we must pay attention to the non-linearity in the digital precoder and the modulation components associated to the modulator, which can completely destroy the performance of the converter.

Next, we will describe theoretically the proposed architecture and will show its performance.

4.1.1 A VCO-based ADC architecture with pulse width modulated precoding

We have already stated that the main goal of using a digital precoding is making the VCO work linearly. However, this technique also implies some disadvantages. One of the most important concerns is the modulation components associated to the modulation process. Here, we will use a pulse width modulator as the digital precoder. We can distinguish between synchronous and asynchronous pulse

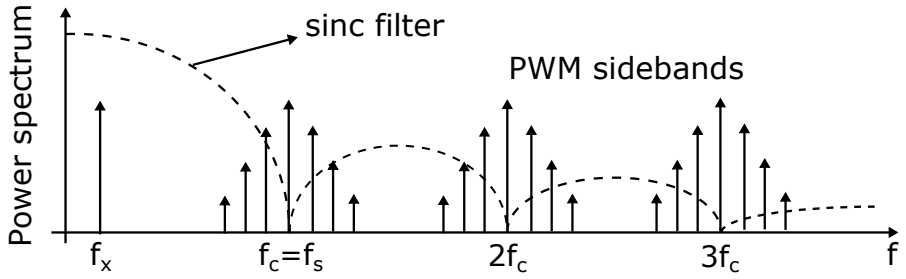


Figure 4.2: Spectrum of a natural pulse width modulated sinusoidal wave filtered by a sinc function.

width modulators. The spectrum of asynchronous pulse width modulated signals strongly depends on the input signal [55]. Therefore, we will focus on synchronous pulse width modulators. Within synchronous pulse width modulators, we distinguish between natural and uniform pulse width modulators. They show quite different spectra. These differences were analyzed in [55] and we will not go into details. In our case, we will use a natural PWM precoding with the purpose of avoiding the requirement of a sample and hold block in the front-end of the converter. This block would make the design more difficult and would occupy a large area. The spectrum generated by a natural PWM precoding was published in [85]. According to [85], it is composed of the input signal $x(t)$ and a set of sidebands components around every multiple of the carrier frequency (f_c). If this signal becomes the input of a VCO-based ADC (as in Fig. 4.1), it will get through the VCO and will be sampled afterwards. When the signal is sampled, these set of sideband components may alias into the band of interest and strongly degrade the performance of the converter. This phenomenon is similar to the aliasing of the pulse frequency modulated components observed when we theoretically analyzed the VCOs in Chapter 3 with the PFM interpretation. Accordingly, the relation between the f_c and f_s is required to be analyzed to achieve the best possible performance of the system.

Taken the PFM interpretation of a VCO, a generic order open-loop VCO-based ADC can be modeled as in Fig. 3.7. The pulse shaping filter is assumed to be a $sinc_n$ function, with nulls at each multiple of the sampling frequency f_s. This means that, if we connect a pulse width modulated signal to the VCO and f_c tends to f_s, mostly of the sideband components of the pulse width modulation should be attenuated at the output. This is illustrated in Fig. 4.2, where we can appreciate the shape of a pulse width modulated signal filtered by a sinc function.

Nevertheless, we should note that we deal with two modulation processes here: the pulse width modulation of the digital precoder and the pulse frequency modulation of the VCO. The modulation components of the VCO result from the "re-modulation" of the pulse width modulated signal, that is the input of the VCO, so that the generated spectrum is quite difficult to analyze in a simple way.

Now, the input signal of the VCO is not a band-limited signal (as can be observed in Fig. 4.2), which means that the analysis of the modulation components is not intuitive and might take us to very complicated equations. According to [86], if we connect a non-limited band signal to a pulse frequency modulator,

components at all the possible combinations of the input frequencies will appear in the output data. Equation (3.3) describes the spectrum of a pulse frequency modulated signal when the input signal of the VCO is a sinusoidal wave, and therefore band-limited. In the current case, we would need to apply (3.3) to all the components of the pulse width modulated spectrum (e.g. f_x, f_c, $f_c - f_x$, $f_c - 2f_x$, ...), which is no practical and useless. Unfortunately, in practice, it might be difficult to keep the sideband components out of the band of interest for all the possible situations. E.g. if we look at the sideband components around f_o, they will appear at $f_o - f_c - f_x, f_o - f_c - 2f_x$, etc; which means that the performance of our converter will depend not only on the f_c, but also on the f_x. The reader might notice that this phenomenon also occurs in Fig. 3.7. However, if we keep f_o much higher than f_x, we will be able to keep most of the sidebands out of the band of interest (the in-band sidebands will generate the fundamental encoding error described in Chapter 3). In the system built with the pulse width modulator, if f_c or some of its multiples tends to f_o, the intermodulated sidebands components might fall in-band easily, resulting in a system whose performance strongly depends on f_x, f_c and f_o.

In [55], a wide analysis of this type of architectures were made, stating that, indeed, the performance of them depends significantly on several parameters as the type of pulse width modulation, the ratio f_c/f_s or the input signal frequency f_x. Just to show the reader the high sensitivity of the system, we will provide two examples: one in which the sideband components do not fall into the band of interest, and another one in which we have the opposite situation and a very ugly situation.

In Fig. 4.3(a) we can observe an equivalent system to that shown in Fig. 4.1, but now without sampling and the equivalent first difference in the continuous time domain. This system is used to determine what is the power coming from the modulation processes that fall into the band of interest. Fig. 4.3(b) depicts one simulation of the system. This simulation was made with the nominal parameters that will be used later on to design the practical circuit. According to [54], we should not use integer relations between the carrier, the sampling and the VCO oscillation frequency (f_{osc}). In this case, we established that both f_c and f_{osc} equals approximately $f_s/2$ (but not exactly that relationship). The VCO is a 7-phases ring oscillator ($N = 7$) and the input signal is a sinusoidal wave of -6 dBFS. The sampling frequency is f_s= 1.5 GHz and BW= 20 MHz. In Fig. 4.3(b) the spectrum of the pulse width modulated signal $x_{dm}(t)$ is drawn in blue. The spectrum of signal $y(t)$ is drawn in red. In this case, there are several modulation components that fall into the band of interest and restrict the performance. The SNDR is limited to 59 dB. This value is the maximum value of the SNDR that we can achieve from the system with the selected parameters. Note that this limitation is equivalent to the limitation depicted in Fig. 3.6, and tends to worse when sampling. For the moment, it seems that we are dealing with a potential functional architecture. Now, we will increase f_o by only 0.4%. The resulting spectrum obtained from the VCO is shown in Fig. 4.3(c). It is clearly visible that the sidebands coming from the VCO fall in-band and completely destroys the performance of the converter. This is one of the main weaknesses of the VCO-based ADCs with digital precoding and something that must be seriously

taken into account when making a practical implementation as we made. In our case, as will be seen later on, we made a circuit design with several programmable options to tune the carrier frequency of the pulse width modulator and the VCO oscillation frequency.

This system can be also analyzed with the PFM-based models proposed in Chapter 3. In this case, we will start with the linear model depicted in Fig. 4.4(a). Here, the diagram is quite similar to Fig. 3.10 but adding the modulation components due to the pulse width modulator before the VCO (both the frequency components placed lower than $f_s/2$, $M_{\mathrm{PWM,LF}}(s)$, and the frequency components placed higher than $f_s/2$, $M_{\mathrm{PWM,HF}}(s)$). $M_{\mathrm{VCO,LF}}(s)$ and $M_{\mathrm{VCO,HF}}(s)$ represent the same components but due to the VCO modulation. The remaining terms represent the same as in Fig. 3.10.

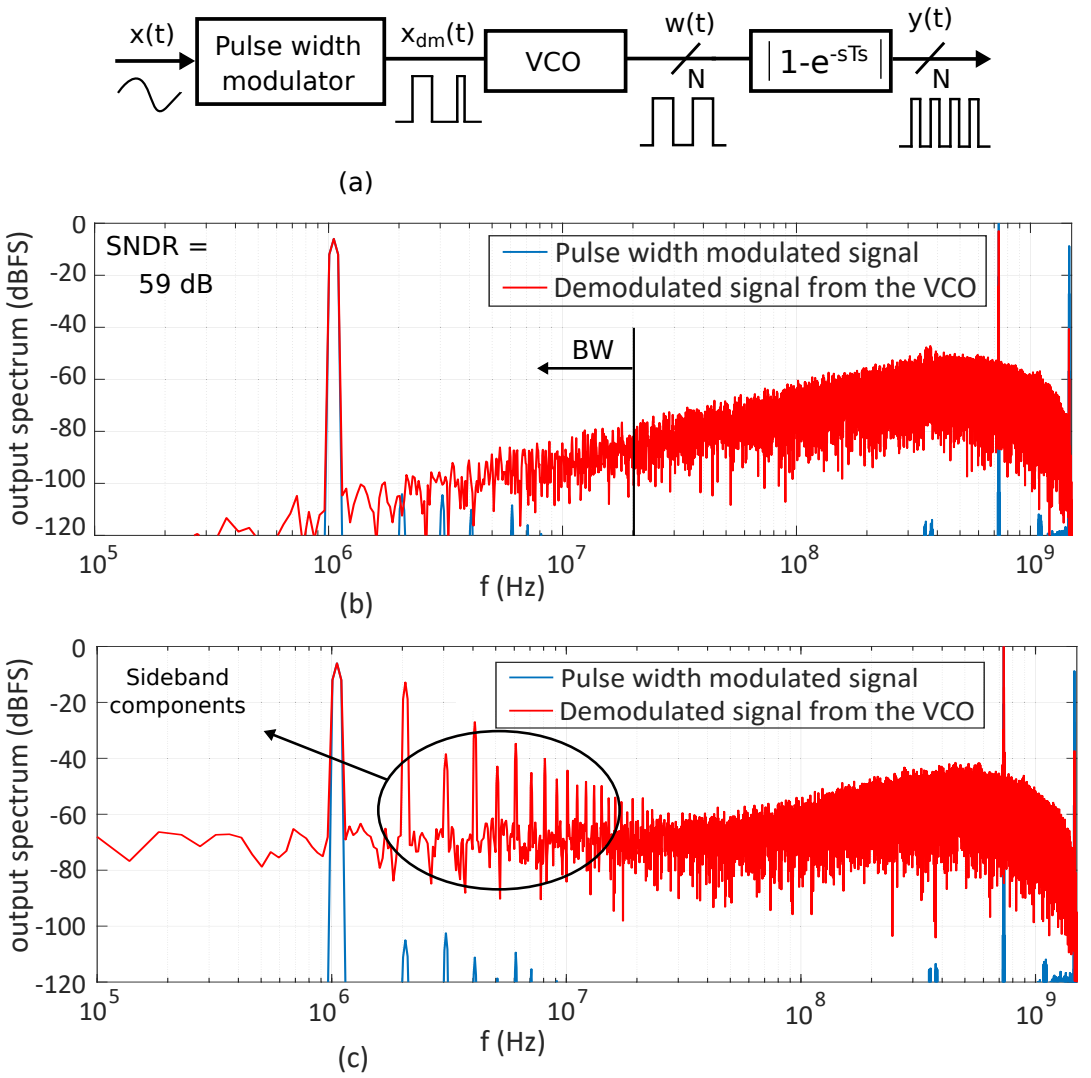


Figure 4.3: (a) Architecture used to study the encoding errors, (b) spectrum of the pulse modulated width signal and the demodulated signal coming from the VCO, and (c) the same spectrum as in (b) with a small variation in the rest oscillation frequency.

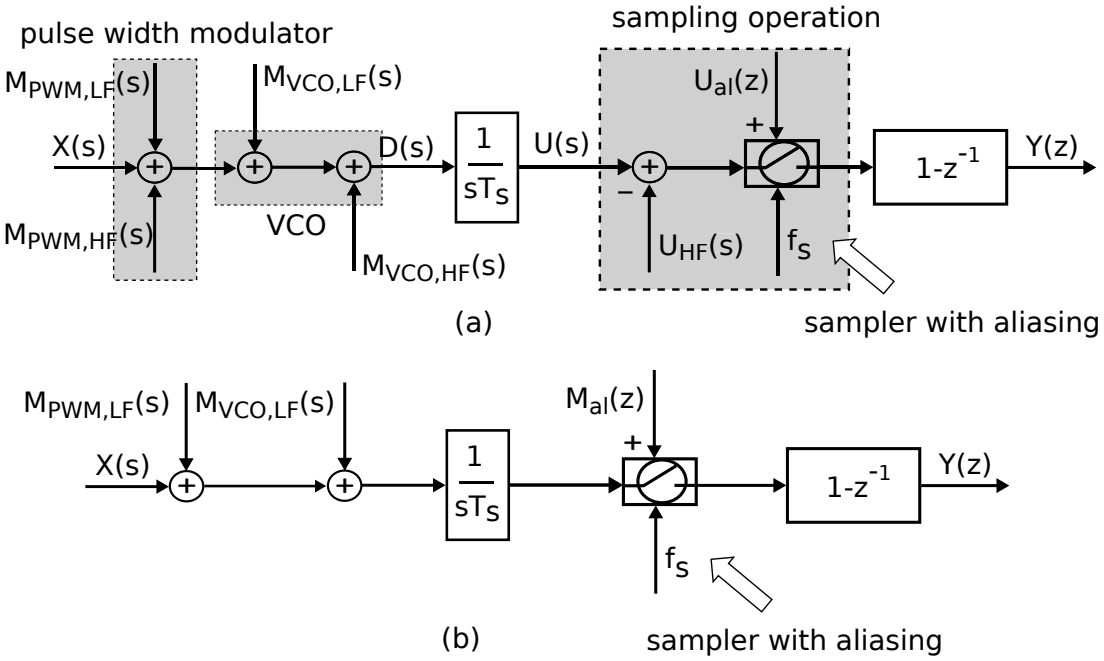


Figure 4.4: Explanation of the spectral shaping of the VCO-based architecture with digital precoding: (a) Expanded diagram, (b) Simplified diagram.

Similarly to Fig. 3.10, to go from Fig. 4.4(a) to Fig. 4.4(b), we take the high frequency modulation components (in this case coming from the VCO and the pulse width modulator), remove them, and add the appropriate aliased terms. This way, $M_{\mathrm{al}}(z)$ follows:

$$M_{\mathrm{al}}(z) = [U_{\mathrm{HF}}]^* = \left[\frac{M_{\mathrm{VCO,HF}}}{sT_{\mathrm{s}}} + \frac{M_{\mathrm{PWM,HF}}}{sT_{\mathrm{s}}}\right]^*, \tag{4.1}$$

and $Y(z)$ follows:

$$\begin{aligned} Y(z) = \\ \left[\frac{1-e^{-sT_{\mathrm{s}}}}{sT_{\mathrm{s}}}X(s) + \frac{1-e^{-sT_{\mathrm{s}}}}{sT_{\mathrm{s}}}M_{\mathrm{VCO,LF}}(s) + \frac{1-e^{-sT_{\mathrm{s}}}}{sT_{\mathrm{s}}}M_{\mathrm{PWM,LF}}(s)\right]^* + \\ M_{\mathrm{al}}(z)\left(1-z^{-1}\right) = \\ \approx X(s)^* + M_{\mathrm{VCO,LF}}(s)^* + M_{\mathrm{PWM,LF}}(s)^* + \\ M_{\mathrm{al}}(z)\left(1-z^{-1}\right). \end{aligned} \tag{4.2}$$

Note that the aliased terms are first-order noise-shaped as expected. If we compare (4.2) to (3.12), we will notice that in (4.2) we have the low frequency modulation components of the pulse width modulator $M_{\mathrm{PWM,LF}}(s)$. These components can be typically ignored. As stated before, f_{s} is recommended to be a value close to f_{s}, which supposes that there are no low frequency components coming from the pulse width modulator. On the other hand, the term $M_{\mathrm{VCO,LF}}(s)$ corresponds to the components analyzed in Fig. 4.3 (red drawn spectrum). From a practi-

cal point of view, we have to try that the power of the component $M_{\mathrm{VCO,LF}}(s)^*$ (which in this case is not negligible as shown in Fig. 4.3) is less that the power of the component $M_{\mathrm{al}}(z)\,(1-z^{-1})$. Otherwise, our architecture will be limited by the components coming from the pulse width modulator.

If we continue to describe the proposed architecture, we may notice that unlike conventional VCO-based structures, the VCO input signal is now a digital signal. This allows us to design the VCO as a gated-ring oscillator (GRO) [87–89]. A GRO is a type of VCO used when we have only two possible oscillation choices: oscillating at some frequency or not oscillating (keeping the oscillation phase). This requirement fits with our design, that's the reason why we will use it. In our case, the GRO is a multiphase oscillator that will oscillate between zero and $f_{\mathrm{s}}/2$. The number of phases in the oscillator equals seven.

After the GRO, we have the digital logic that, firstly, samples the signal and, secondly, computes the first difference. The seven phases in each oscillator are combined in seven similar digital paths working in parallel to generate the final output data. A multiphase oscillator is used to increase the resolution of the whole system. The details of the circuit will be described in Chapter 6.

Fig. 4.5(a) shows a diagram of the proposed architecture. Fig. 4.5(b) depicts a behavioral simulation of the proposed system. The oscillation parameters are equal to those used in Fig. 4.3(b). For a sinusoidal input wave of -6 dBFS, 20-MHz BW and $\mathrm{f_s}$= 1.5 GHz, the SNDR is 54 dB. In Fig. 4.5(b) we can appreciate the sideband components at high frequency. The position of these components depends on the relationship between $\mathrm{f_s}$, $\mathrm{f_c}$, $\mathrm{f_{osc}}$ and f_{x}. An incorrect relationship might suppose that these components fall into the band of interest and reduce the performance of the converter. According to the simulation made in Fig. 4.3(b), the resulting SNDR is lower than the value predicted by Fig. 4.3(b). Therefore, we lose 5 dB due to aliasing.

Later on, when we describe the architecture designed on silicon, we will provide more details about the architecture, the circuit and the obtained performance measurements.

4.1.2 Conclusion

A way of making a VCO-based ADC structure work linearly is proposed through the use of a digital encoder in front of the VCO. In this case, the selected digital modulator is a pulse width modulator, which encodes the input signal into a digital signal that is connected to the VCO. This way, the VCO oscillates only at two possible oscillation frequencies and does not generate distortion at the output signal. This technique has some important drawbacks. Firstly, we have to consider how the pulse width modulated components get through the VCO because they can limit the performance of our system significantly. This was analyzed with the PFM-based theory proposed previously. Behavioral simulations validate what is explained from a theoretical point of view, giving us an indication of the high sensitivity of the system and how its performance can be easily destroyed. Secondly, the linearity of the digital encoder might degrade the ADC performance similarly to the non-linearity of the VCO. As this system was implemented on silicon, this issue will be described later on.

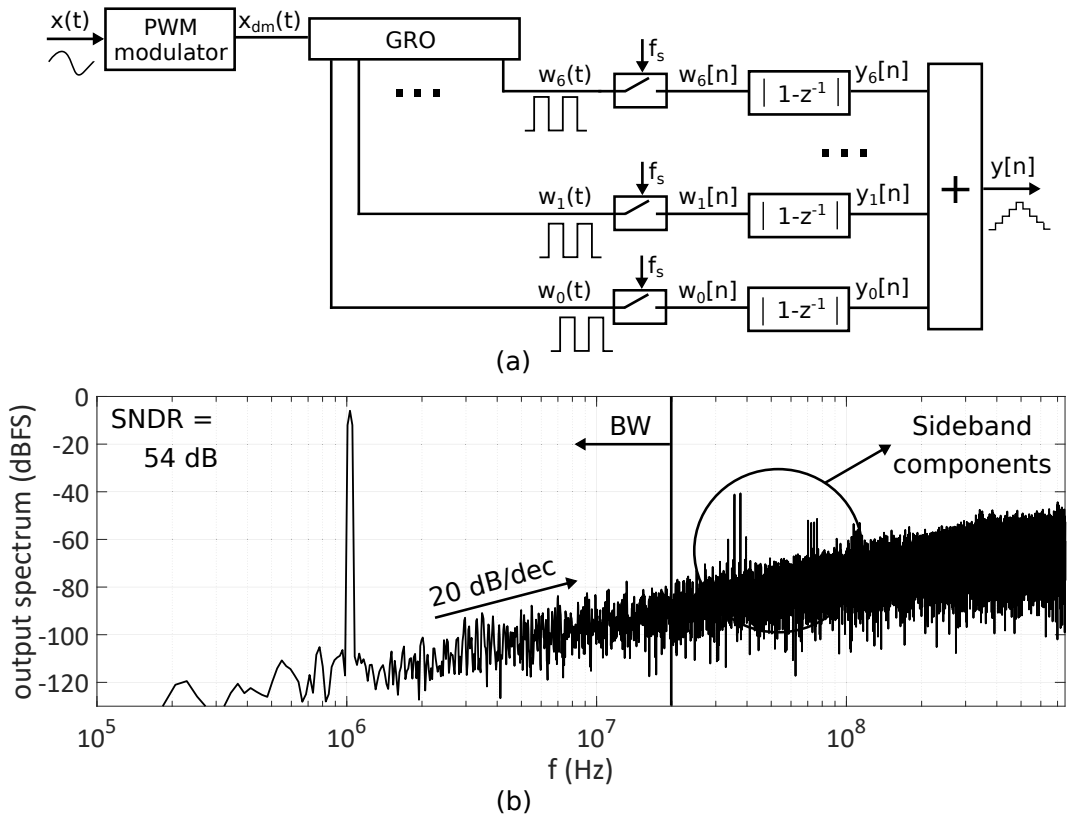


Figure 4.5: (a) Block diagram of the proposed architecture, and (b) behavioral simulation.

4.2 ADC circuits based on an analog pulse frequency modulator

The PFM interpretation of the VCO allowed us to get analytical equations for open-loop VCO-based ADC architectures, describe the different errors involved in the modulation and sampling processes, propose new theoretical architectures, and provide new approaches to analyze other already known architectures. However, a pulse frequency modulator is, in fact, a VCO-based ADC and can be used itself as a converter. In this section, we will describe how a pulse frequency modulator can be turned into an efficient ADC with similar performance to VCO-based ADCs implemented with ring oscillators. In addition, the architecture we will describe is not only an efficient ADC architecture, but we can take benefit from its proper linearity properties. We will describe the architecture of a PFM-based ADC theoretically and, in Chapter 7, we will talk about the designed circuit of a pulse frequency modulator prototype implemented in 40-nm.

The pulse frequency modulator architecture implemented on chip uses an active integrator. However, this architecture has some drawbacks that will be discussed later on. Simultaneously with the design of the chip, some new techniques were identified to fix these drawbacks. In particular, we found that architectures with similar performance could be made with a passive integrator. In this

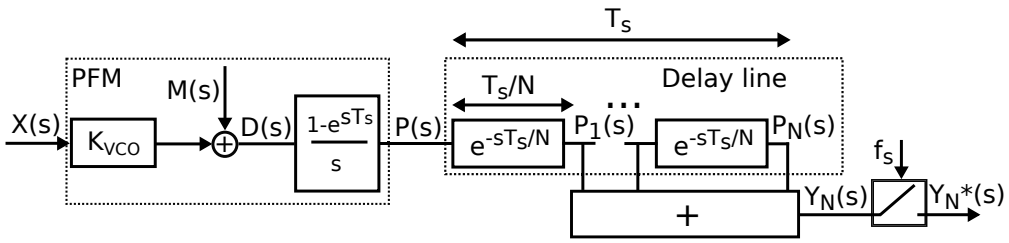


Figure 4.6: Laplace-based model of a pulse frequency modulator architecture followed by a delay line.

chapter, we will also describe theoretically how a pulse frequency modulator with active integration can be turned into a pulse frequency modulator with passive integration, which leads to a more linear, less power-consuming and simpler architecture.

4.2.1 An efficient ADC implemented with a pulse frequency modulator

The architecture of a pulse frequency modulator with multibit output was already shown in Fig. 3.25, where we used the PFM interpretation to analytically calculate the spectrum of the output signal $y_{\mathrm{n}}[N]$. Now, we will retake that architecture to talk more about it. For the moment, we will ignore the delay line of the figure and we will focus on the pulse frequency modulator block, which is already well-known for us. To match with the performance of a conventional VCO-based ADC, we must satisfy:

$$T_{\mathrm{d}} = \frac{1}{f_{\mathrm{s}}} = T_{\mathrm{s}}, \tag{4.3}$$

where f_{s} is the sampling frequency.

If signal $p(t)$ was sampled, the output spectrum would be first-order noise shaped. According to the PFM interpretation, we can define a linear model of the pulse frequency modulator (for simplicity, we do not take into account the DC component f_{o}). This model is shown in the left side of Fig. 4.6, expressed in terms of the Laplace 's' variable. Based on this model, the pulse frequency modulated output signal ($P(s)$) can be calculated. To identify a sampled signal in the equations, we use the star operator $(\cdot)^*$, as defined in [32]:

$$P^*(s) = \left(K_{\mathrm{VCO}} \cdot \frac{1 - e^{-sT_{\mathrm{s}}}}{s} X(s) + \frac{1 - e^{-sT_{\mathrm{s}}}}{s} M(s) \right)^* . \tag{4.4}$$

Supposing that $f_{\mathrm{x}} \ll f_{\mathrm{s}}$:

$$\frac{1 - e^{-sT_{\mathrm{s}}}}{s} X(s) \approx X(s), \tag{4.5}$$

we get:

$$P^*(s) \approx K_{\text{VCO}} \cdot X^*(s) + \left(1 - z^{-1}\right) \left(\frac{M(s)}{s}\right)^* . \tag{4.6}$$

Equation (4.6) shows that the system works similar to a first-order $\Delta\Sigma$ modulator, as expected. Whereas the input signal $X(s)$ is seen at the output as it is but multiplied by the VCO gain, the modulation components $M(s)$ are first-order noise shaped. Consequently, the pulse frequency modulator architecture could be used itself as an ADC. Unfortunately, $p(t)$ is a single bit signal, so that, if we consider it as our converter output signal, it will take us to an inefficient structure. We will explain next how this architecture can be transformed into an efficient ADC.

VCO-based ADCs implemented with ring oscillators are typically built with multiphase ring oscillators [41] that produce a multibit output. In the case of PFM-based ADCs, a multibit output can be implemented if the oscillating signal $p(t)$ is sampled after a continuous-time FIR filter [90] using, for example, the delay line configuration of Fig. 3.25(a). In the right side of Fig. 4.6(b) we can see the Laplace model of this delay line. Now, the output of the system is defined as follows:

$$Y_{\text{N}}^*(s) = \left(\sum_{n=1}^{N} e^{-s \cdot n \frac{T_{\text{S}}}{N}} \cdot P(s)\right)^* . \tag{4.7}$$

If we make the same assumptions as before, we get the following expression for $Y_{\text{N}}(s)^*$:

$$\begin{aligned} Y_{\text{N}}^*(s) \approx N \cdot K_{\text{VCO}} \cdot X^*(s) + \\ \left(1 - z^{-1}\right) \left(\sum_{i=1}^{N} e^{-s \cdot i \frac{T_{\text{S}}}{N}} \frac{M(s)}{s}\right)^* . \end{aligned} \tag{4.8}$$

Equation (4.8) shows that the modulation components are filtered by an additional low-pass FIR filter, at the same time that the input signal is multiplied by the term N. Let's now check whether the addition of the delay line to the system supposes a SNDR improvement. With that purpose in mind, we will study the differences between the equations that describe both the single-phase and the multiphase cases, i.e. (4.6) and (4.8) respectively.

On the one hand, regarding the STF derived from (4.6) and (4.8), we get the following ratio:

$$\frac{\text{STF}_{\text{multiphase}}}{\text{STF}_{\text{single-phase}}} = \frac{N \cdot K_{\text{VCO}}}{K_{\text{VCO}}} = N. \tag{4.9}$$

On the other hand, obtaining the same ratio for the NTF (here we suppose that our noise term is $M(s)/s$) is more difficult because the equations of the NTFs involve expressions that can not be easily simplified. This ratio is defined

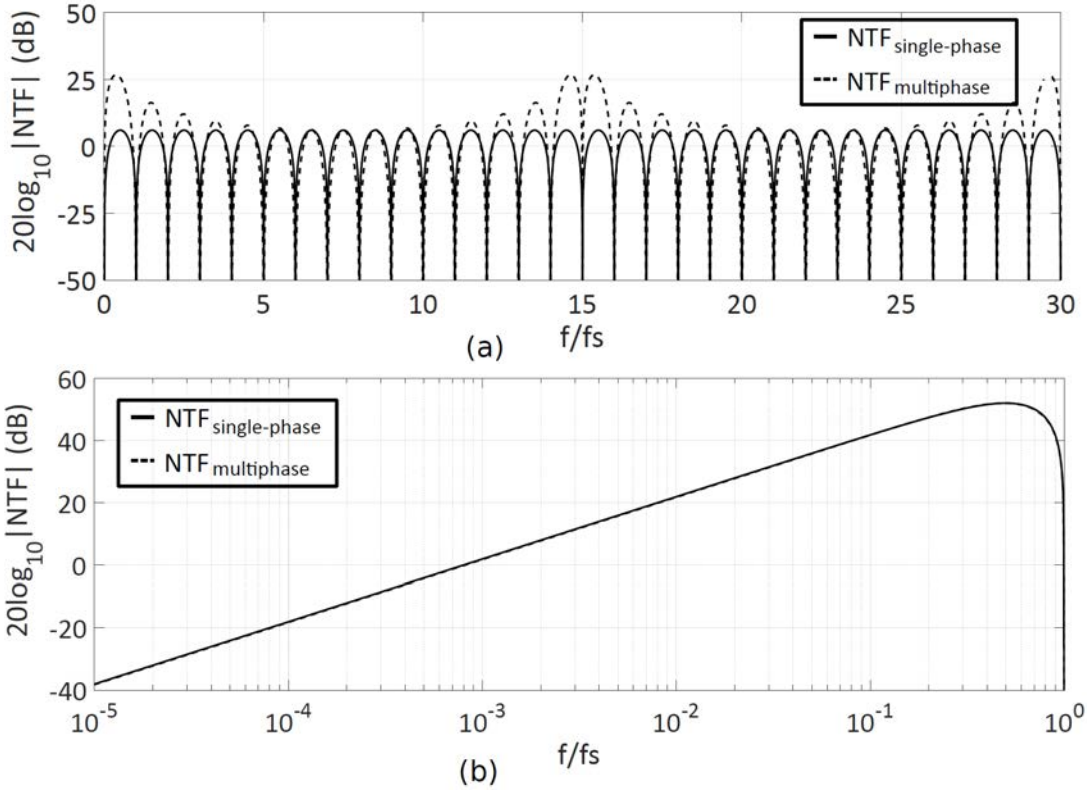


Figure 4.7: Spectral representation of the NTFs of both the single-phase and the multiphase pulse frequency modulator architectures: (a) in the continuous domain, and (b) in the discrete domain (after sampling).

as follows:

$$\frac{\mathrm{NTF}_{\mathrm{multiphase}}}{\mathrm{NTF}_{\mathrm{single\text{-}phase}}} = \frac{\left(1 - e^{-s \cdot T_\mathrm{s}}\right)\left(\sum_{n=1}^{N} e^{-s \cdot n \frac{T_\mathrm{s}}{N}}\right)}{\left(1 - e^{-s \cdot T_\mathrm{s}}\right)} = \sum_{n=1}^{N} e^{-s \cdot n \frac{T_\mathrm{s}}{N}}. \tag{4.10}$$

As can be observed, the relation is non-intuitive and no meaningful results can be concluded at a glance. However, empirical conclusions can be obtained from numerical estimations. Firstly, we have calculated the representation of both NTFs for a limited spectral gap. If we suppose, for instance, $T_\mathrm{s} = 1$ s and $N = 15$, the spectral representation looks as in Fig. 4.7(a). The shape of the NTFs is composed of a set of lobes with nulls in the multiples of f_s. When sampling, these lobes alias and generate the shapes shown in Fig. 4.7(b). It can be appreciated that both NTFs overlap and the difference between their values is negligible. From these numerical results, we can empirically establish that the ratio between the NTFs is equal to one. Although it is an empirical observation, it fits very well with the results obtained later on by simulation.

According to (4.9) and the results depicted in Fig. 4.7(b), we are able to deduce the following relationship between the SNDR for the single-phase case

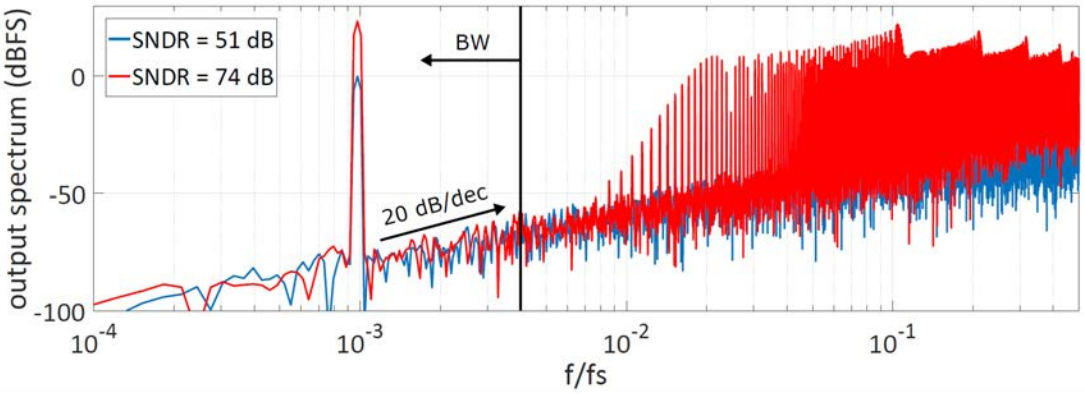


Figure 4.8: Behavioral simulations of both the single-phase and the multiphase pulse frequency modulator architectures (the output spectrum is normalized with respect to the output of the single-phase case).

and the SNDR for the multiphase case:

$$\mathrm{SNDR}_{\mathrm{multiphase}} = \mathrm{SNDR}_{\mathrm{single}} + 20\log_{10}(N). \tag{4.11}$$

To validate (4.11) we have used a behavioral model of the system shown in Fig. 4.6, both considering $p(t)$ and $y_{\mathrm{N}}(t)$ as the outputs of the system. Just to provide an example, Fig. 4.8 depicts the output spectra of both cases with a -3 dBFS sinusoidal input wave, OSR= 128, $f_{\mathrm{o}} = K_{\mathrm{VCO}} = f_{\mathrm{s}}/32$, and $N = 15$. Firstly, we can observe that the power level is similar in both cases according to the results of Fig. 4.7(b). Secondly, the difference between the SNDRs is equal to 23 dB. According to (4.11), we expect a difference approximately equal to 23.52 dB, therefore our prediction matches with the simulated results.

Then, the delay line of the Fig. 4.6(a) allows us to build a multibit pulse frequency modulator with improved SNDR. Now, we will propose a circuit to implement this multibit architecture.

4.2.2 PFM-based ADC with active integration

The first circuit which we came up with when designing the system of Fig. 4.6 is depicted in Fig. 4.9(a). The proposed circuit is composed of an integrator, an asynchronous comparator with a fixed threshold voltage V_{thr}, a rising-edge triggered monostable, and a feedback DAC with a gain K_{DAC} that closes the loop. In Fig. 4.9(b) we can see an example of the typical waveforms involved in the oscillation loop. As can be observed, the sign switching of $e(t)$ makes the integrated signal $e_{\mathrm{i}}(t)$ increase or decrease. If the monostable is idle and no pulse is being generated, $e(t)$ is positive and $e_{\mathrm{i}}(t)$ increases. When $e_{\mathrm{i}}(t)$ reaches V_{thr}, the comparator triggers the monostable and a constant-length pulse is generated. The pulse is fed back into the integrator. This forces $e(t)$ to be negative and $e_{\mathrm{i}}(t)$ is decreased. When the pulse finishes, $e_{\mathrm{i}}(t)$ increases again and the oscillation cycle is repeated. The lowest value reached by $e_{\mathrm{i}}(t)$ at the end of the monostable pulse depends on $x(t)$. Then, the time that $e_{\mathrm{i}}(t)$ takes to reach V_{thr} afterwards

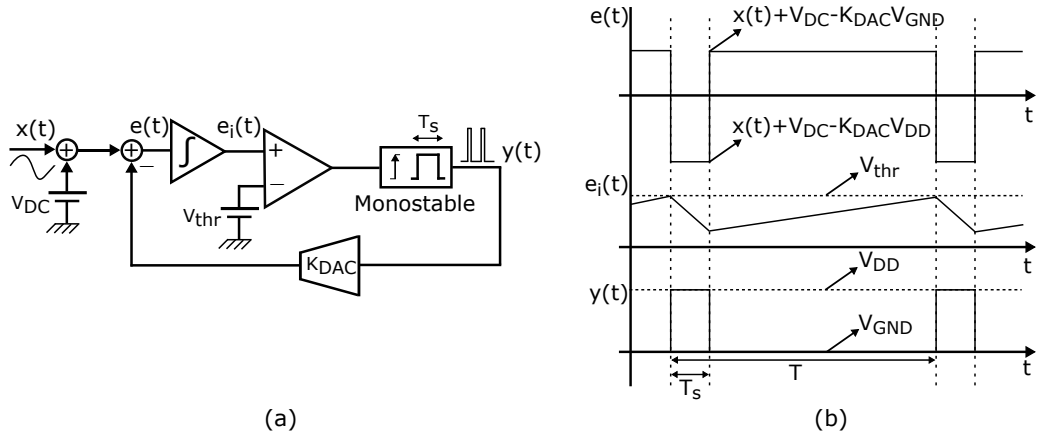


Figure 4.9: (a) Circuit for the implementation of the pulse frequency modulator, and (b) oscillating signals of the loop.

also depends on $x(t)$. If we keep the notation of Fig. 4.9, the oscillation frequency of the system ($f_{\mathrm{osc}}(t)$) can be calculated as follows:

$$f_{\mathrm{osc}}(t) = f_{\mathrm{o}} + K_{\mathrm{VCO}} \cdot x(t) = \frac{V_{\mathrm{DC}} - K_{\mathrm{DAC}} V_{\mathrm{GND}}}{K_{\mathrm{DAC}} T_{\mathrm{s}} \left(V_{\mathrm{DD}} - V_{\mathrm{GND}}\right)} + \frac{1}{K_{\mathrm{DAC}} T_{\mathrm{s}} \left(V_{\mathrm{DD}} - V_{\mathrm{GND}}\right)} x(t), \tag{4.12}$$

where V_{DD} is the supply voltage and V_{GND} is the ground supply.

As can be observed, $f_{\mathrm{osc}}(t)$ depends linearly on $x(t)$. As opposite to prior works, the linearity does not depend on the compensation of the nonlinear delay dependence of an inverter [47] or on digital calibration circuits [41]. Additionally, if we compare this architecture to conventional first-order continuous-time $\Delta\Sigma$ modulators, our output is multibit without requiring a multibit DAC (typically no linear) and a flash quantizer.

If we focus now on the integrator of Fig. 4.9(a), there are several ways to implement it. With the goal of making the design as simple as possible, we can split up the integrating path into two different paths. On the one side, we integrate the input signal with a transconductance that injects a current proportional to the input voltage into a capacitor. On the other side, the integration of the digital pulse is made by a digitally controlled current source. As the digital pulse remains always constant both in width and in amplitude, it is connected to a current source that injects a current into the capacitor or not depending on the logic state of the pulse. Fig. 4.10(a) shows the proposed circuit. As can be observed, we have now two different integrating paths: one made with the transconductance g_{m}, and the other one made with the digitally controlled current source I_{DAC}. We will also add a fixed current source I_{DC} to control the rest oscillation frequency, as will be seen later on. If we directly sample $y(t)$($y(t)$ is now equivalent to $p(t)$ in Fig. 3.25(a)), we will be dealing with a single-phase architecture. To extend the circuit to a multiphase architecture we can design the monostable in such a way that it works similarly to the delay line of Fig. 4.6. Fig. 4.10(b) shows how

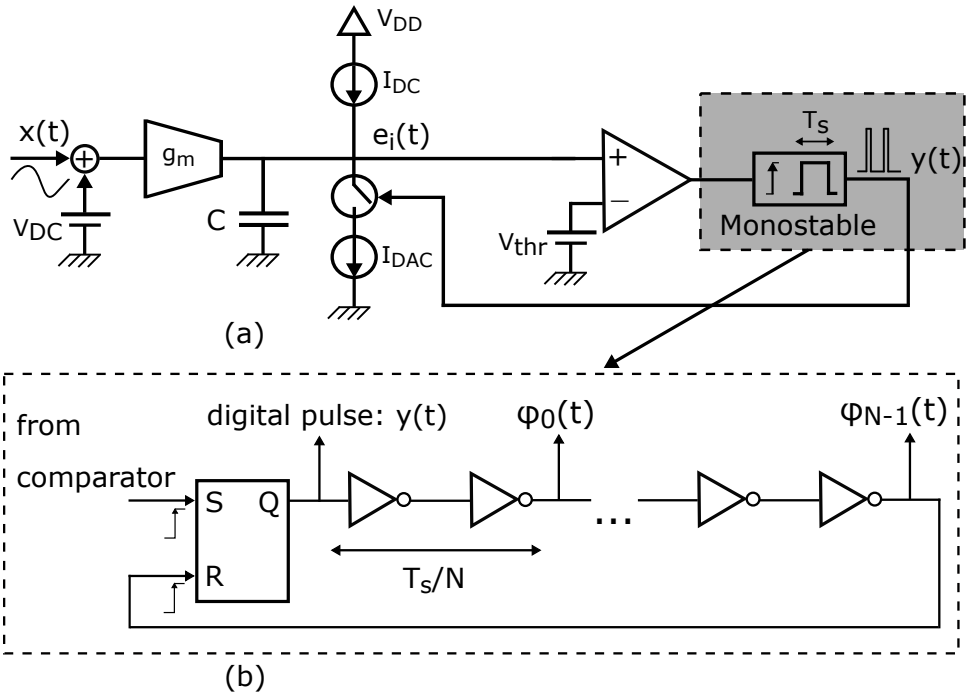


Figure 4.10: Pulse frequency modulator with active integration and separated integrating paths.

to build the monostable with CMOS inverters, making a delay line composed of N phase outputs. Here, the buffer composed of two CMOS inverters represents the taps of the delay line and delays T_s/N. Finally, if we want to build an ADC, each phase θ_i will be sampled and summed to produce a multibit output signal.

A behavioral model of this PFM-based ADC was simulated to check the performance of the system. Fig. 4.11 depicts the results of the simulation. The parameters used in the simulation are: f_s= 1 GHz, BW= 20 MHz, f_o=K_{VCO}= 250 MHz and N= 15. The input signal is a -3 dBFS sinusoidal waveform with frequency equal to 1 MHz. The resulting SNDR equals 58 dB. It can be appreciated that the spectrum is first-order noise-shaped.

The architecture of Fig. 4.10 corresponds to the circuit designed in the 40-nm chip. More details about the circuit implementation will be provided in Chapter 7, also with the measurements of the chip. The simulation of Fig. 4.11 was made with the nominal parameters of the chip.

According to (4.12), the proposed system shows a linear voltage-to-frequency conversion. However, taken into account the design of Fig. 4.10(a), we may notice that the transconductance is outside the oscillation loop. Therefore, potential non-linearity in the voltage-to-current conversion of the transconductance will not be compensated at any point, which means distortion in the output data and degradation of the converter resolution. This is the main drawback of the system of Fig. 4.10. In Chapter 7 we will see that the solution adopted to this problem requires designing a highly linear transconductance. Nevertheless, it is not the unique possible solution. Next, we will describe, from a theoretical point of view,

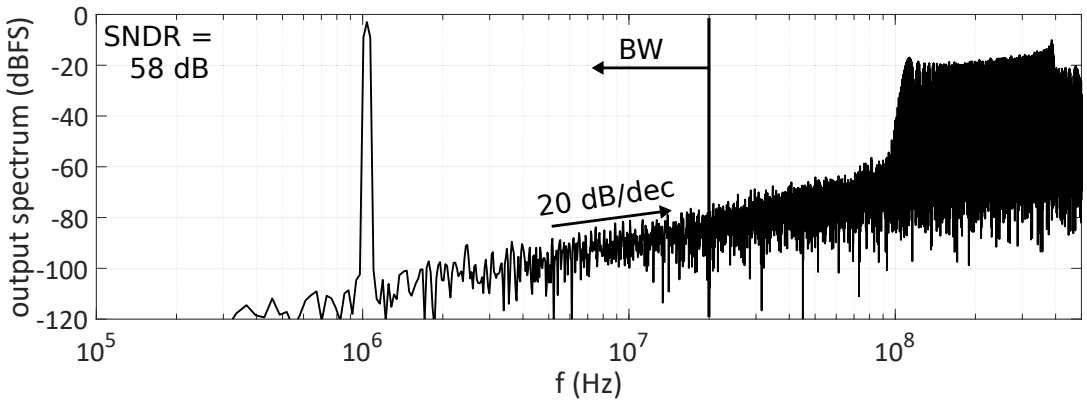


Figure 4.11: Behavioral simulation of the PFM-based ADC of Fig. 4.10.

two techniques to deal with this issue.

4.2.3 Pulse frequency modulator with resistive input and digital correction of non-linearity

In the previous section, we talked about the implementation of a PFM-based ADC with an active integration based on splitting up the integration into two different paths: the path of the input signal and the path of the digital pulse. The drawback is that, due to the open-loop transconductance, non-linearity in the integration of the input signal cannot be compensated and might degrade the final performance.

One way to deal with this issue may consist on a digital correction of the non-linearity once the data are collected. However, to make the appropriate corrections, we need to know the equations that model the non-linearity, which is difficult to infer because they depend on the behavior of the transistors that compose the transconductance.

A passive RC filter is a circuit that can be used to make a lossy integration. The problem is that the integration is based on an exponential behavior and it is quite non-linear. Nevertheless, it accomplishes with the requirement of having a well-known static non-linearity because the equations that model the performance of a RC filter can be easily estimated. Then, we propose to replace the transconductance of Fig. 4.10(a) by a RC filter and correct the non-linearity after sampling.

Fig. 4.12 shows the proposed PFM-based architecture. As can be observed, we use a RC filter to make the integration of the input signal $x(t)$. To show the performance of the system, we made the simulation depicted in Fig. 4.13. The simulation was made with N =15 taps in the monostable and all the parameters (R, C, I_{DAC}, etc) calculated in such a way that the oscillation parameters were in the same order as in Fig. 4.11. This way, we can compare both simulations. The sampling frequency, the OSR and the input signal parameters are the same as in Fig. 4.11. It can be observed that the resolution is strongly degraded by distortion. Whereas the ideal resulting SNDR is 58 dB (Fig. 4.11), here we get a

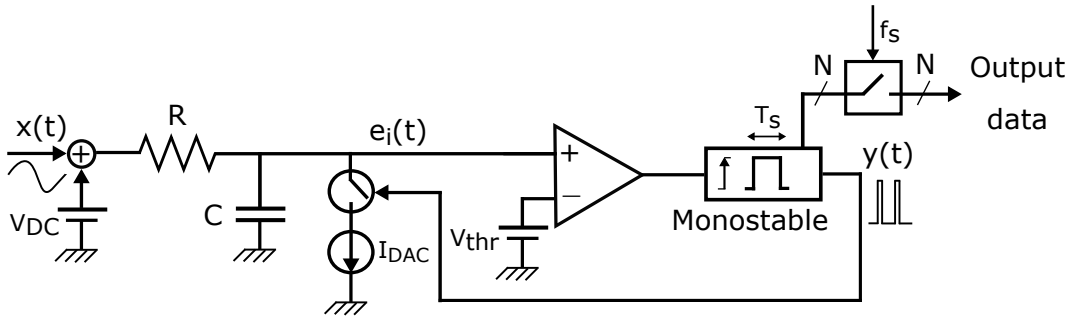


Figure 4.12: PFM-based architecture with front-end passive integration.

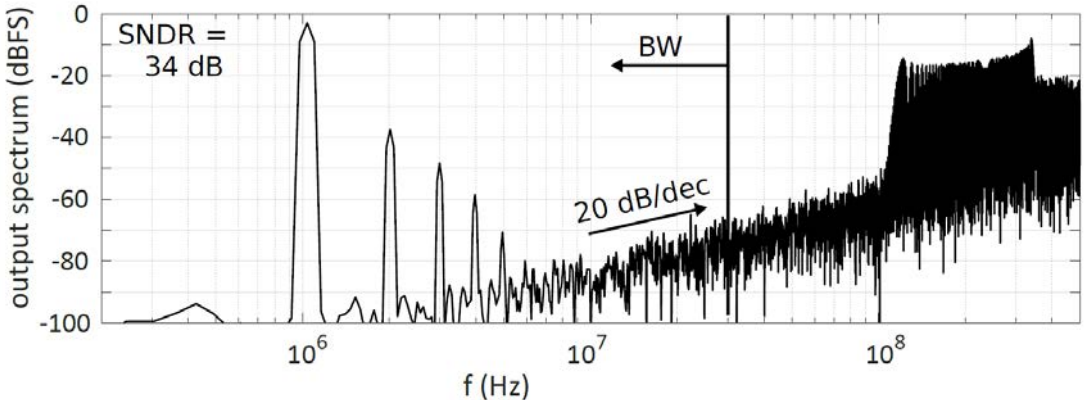


Figure 4.13: Behavioral simulation of the system of Fig. 4.12.

SNDR of 39 dB.

As stated above, the advantage of the system of Fig. 4.12 is the possibility of mathematically correcting the non-linearity by post-processing the output data. If the RC product is measured in an initial calibration phase and the circuit design parameters are known, non-linearity can be estimated. In addition, a RC time constant is less influenced by process-voltage-temperature (PVT) variations than the voltage-to-frequency dependence of a ring oscillator. Provided that the inverse function of the voltage-to-frequency conversion of the PFM-based system can be calculated, we will be able to recover digitally the input data with much less distortion.

The equation that defines the oscillation frequency $f_{\mathrm{osc}}(t)$ follows:

$$f_{\mathrm{osc}}(t) = \frac{1}{T_{\mathrm{s}} - RC \cdot \ln \frac{V_{\mathrm{thr}} - V_{\mathrm{DC}} - x(t)}{e^{-\frac{T_{\mathrm{s}}}{RC}} (I_{\mathrm{DAC}} R + V_{\mathrm{thr}} - V_{\mathrm{DC}} - x(t)) - I_{\mathrm{DAC}} R}}, \tag{4.13}$$

which is a non-linear expression with respect to the input signal $x(t)$. From (4.13) we can isolate the input signal $x(t)$:

$$x(t) = \frac{-1}{1 - e^{-\frac{T(t)}{RC}}} \left(e^{-\frac{T(t)}{RC}} \left(RI_{\mathrm{DAC}} + V_{\mathrm{thr}} - V_{\mathrm{DC}} \right) \right) +$$

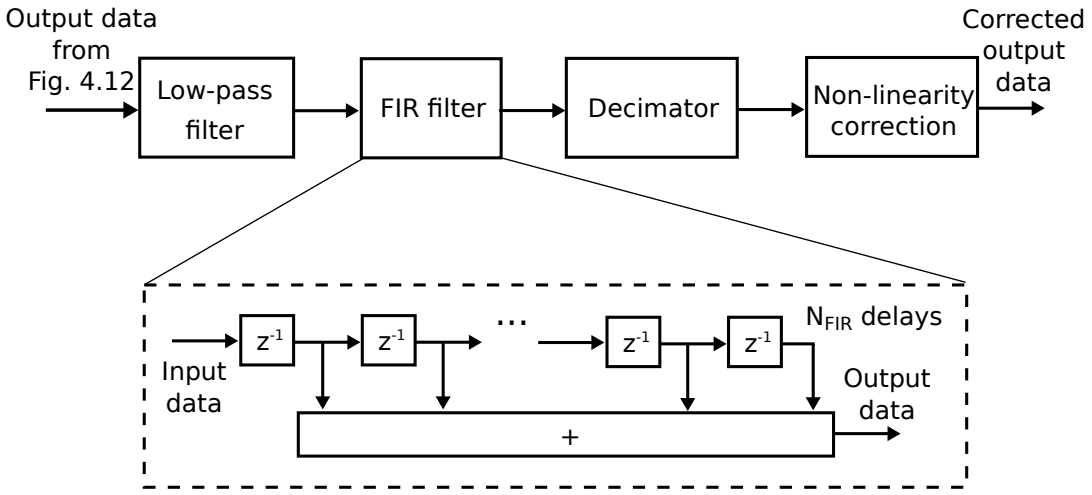


Figure 4.14: Digital post-processing of the ouput data.

$$\frac{-1}{1-e^{-\frac{T(t)}{RC}}}\left(-e^{-\frac{T(t)-T_{\mathrm{S}}}{RC}}RI_{\mathrm{DAC}}-V_{\mathrm{th}}+V_{\mathrm{DC}}\right), \tag{4.14}$$

where $T(t)=1/f_{\mathrm{osc}}(t)$.

Therefore, we have an expression that provides us the input voltage amplitude when the output oscillation frequency of the pulse frequency modulator is known. The oscillation frequency can be obtained by means of a moving average filter applied to the output data. This filter will be built as a FIR filter of N_{FIR} unity delays whose outputs are summed. However, before that, to better make the distortion correction, we will filter the output data with low pass digital filter, which is anyway required to implement a complete ADC in the post-processing stage. Then, we will estimate the oscillation frequency with a FIR filter, decimate the data and apply to them the inverse function of the non-linear voltage-to-frequency. Correction after the decimation eases the implementation of (4.14), as computations can be made at much lower sampling rate. The flow of the data in the post-processing stage is depicted in Fig. 4.14.

Fig. 4.15 shows a simulation of the proposed distortion correction method. The simulation parameters are the same as in Fig. 4.13. In the post-processing line, a 6^{th}-order low-pass Butterworth filter as the low-pass filter (cut-off frequency at 20 MHz) and a FIR filter as shown in Fig. 4.14 with $N_{\mathrm{FIR}}=16$ were used. The final corrected data were decimated to reach the Nyquist sampling rate. The blue-drawn spectrum represents the non-corrected output data once low-pass filtered. The SNDR for this case equals 34 dB (according to Fig. 4.13). The red-drawn spectrum represents the corrected output data at the end of the post-processing operations. The SNDR equals 57 dB, which supposes a SNDR improvement of 25 dB. As can be observed, the distortion is highly mitigated while keeping similar quantization noise power level.

The performance of this correction technique depends on the complexity of the post-processing digital chain. For instance, the higher the number of taps used in the FIR, the higher the SNDR improvement. However, if the level of

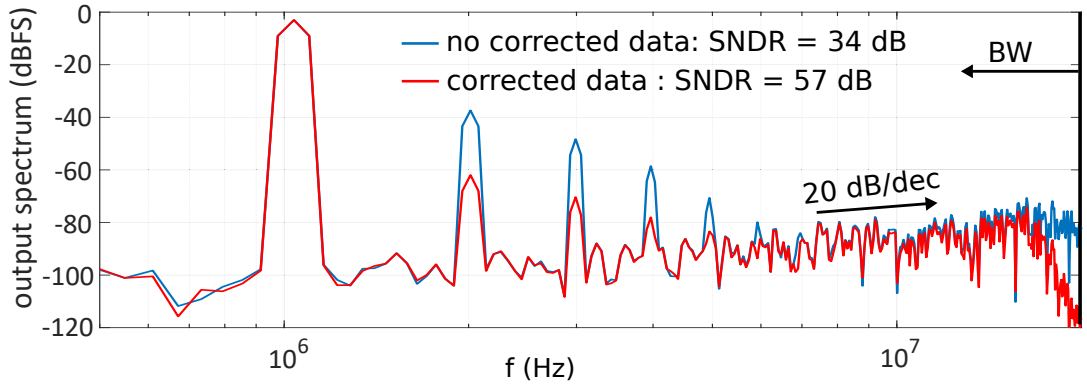


Figure 4.15: Post-processed output data with no correction (in blue) and with correction (in red).

taps is increased, the circuit complexity will also be increased and the number of bits required to represent the output data will be higher. An analysis on how to optimize the performance of this technique is out of the scope of this section.

The proposed technique allows us to correct the non-linearity of the PFM-based ADC shown in Fig. 4.12. Once corrected, the advantage of the system is the potential decrease of power consumption due to the removal of the front-end transconductance of Fig. 4.10(a). At the same time we are dealing with a simpler architecture, in which there is no need of a highly linear transconductance that might be challenging to design. In addition, the circuitry required to correct the linearity is not complex and the area occupied by the whose system is not significantly increased.

Next, we will go one step further in the process of making the PFM-based architecture as simple as possible. In this section, we have replaced the front-end active integrator by a passive integrator. Nevertheless, the digitally controlled current source of the feedback path remains and we need extra digital logic to mitigate the distortion. In the next section, we will replace the feedback current source by a resistor. This will take us to a very simple pulse frequency modulator architecture with a non-linear voltage-to-frequency relation that can be kept under control if some considerations are taken into account.

4.2.4 Pulse frequency modulator with passive RC loop filter

If we take the system of Fig. 4.12 and replace the feedback current source by a resistor, the resulting system will look as shown in Fig. 4.16. Similarly to (4.13), we can estimate the oscillation frequency of the system. According to the nomenclature of Fig. 4.16, $f_{\text{osc}}(t)$ follows:

$$f_{\mathrm{osc}}(t) = \frac{-(R_1+R_2)}{R_1R_2C\cdot\ln\left(\frac{-R_1V_{\mathrm{thr}}+R_2(x(t)+V_{\mathrm{DC}}-V_{\mathrm{thr}}))}{e^{-\frac{(R_1+R_2)T_{\mathrm{s}}}{R_1R_2C}}(R_1(V_{\mathrm{DD}}-V_{\mathrm{thr}})+R_2(x(t)+V_{\mathrm{DC}}-V_{\mathrm{thr}}))-R_1V_{\mathrm{DD}}}\right)-T_{\mathrm{s}}(R_1+R_2)} \tag{4.15}$$

where V_{DD} is the supply voltage of the system.

If we concentrate on the linearity, (4.15) is a complicated and non-intuitive equation. It is difficult to notice which parameters are really important when designing a linear system. To simplify the equation, we will make some assumptions. Firstly, we will suppose that $R_1 = R_2 = R$. Secondly, we will make $V_{\mathrm{thr}} = V_{\mathrm{DD}}/2$. With these considerations (4.15) becomes:

$$f_{\mathrm{osc}}(t) = -\frac{2}{RC\cdot\ln\left(\frac{x(t)+V_{\mathrm{DC}}-2V_{\mathrm{thr}}}{e^{-\frac{2T_{\mathrm{s}}}{RC}}(x(t)+V_{\mathrm{DC}})-2V_{\mathrm{thr}}}\right)-2T_{\mathrm{s}}}. \tag{4.16}$$

Now, if we make the length of the digital pulse (which here matches with the sampling period T_{s}) tend to zero and make the RC product tend to infinity, $f_{\mathrm{osc}}(t)$ will not depend on the input signal $x(t)$. Therefore, as a first approach, the lower the length of the digital pulse and the higher the RC product, the lower the gain applied to the input signal and the higher the linearity of (4.16). Another possible approach is taking (4.16) and estimate the Taylor series expansion. Once estimated, we will see that the power of the harmonics components is directly proportional to the RC product and inversely proportional to the length of the digital pulse. In ideal conditions, if the digital pulse matches exactly with T_{s}, it can be directly sampled with no problem. However, in real applications, we will deal with variations with respect to the nominal value and the length of the pulse will never equal exactly T_{s}. The consequences of this phenomenon were shown in Fig. 3.14. Consequently, although in Fig. 4.16 we sample directly the digital pulse, in practice, we need to isolate the digital pulse with respect to the sampled data. This can be done with the sampling circuit of Fig. 3.18(a). In addition, if we use this circuit, we can modify the length of the digital pulse to improve the linearity of the system.

Fig. 4.17 shows a behavioral simulation of the proposed system where the resulting SNDR almost equals the ideal one (Fig. 4.11). The oscillation parameters are the same as in Fig. 4.11 with an RC product equal to $5{\cdot}10^{-8}$ s, and digital pulses with length equal to 1 ns. As observed, the power of the distortion components are similar to the power of the distortion components of Fig. 4.15 when correction is applied, but without the need of digital correction.

The advantage of the proposed system is that it is the simplest PFM-based architecture that can be implemented in terms of the integration of both the input signal and the feedback pulse. The power consumption is also reduced because we do not need neither an active transconductor nor extra digital logic. In addition, the linearity of the system can be kept under control if correct design parameters are selected. The main drawback is that high-resolution architectures

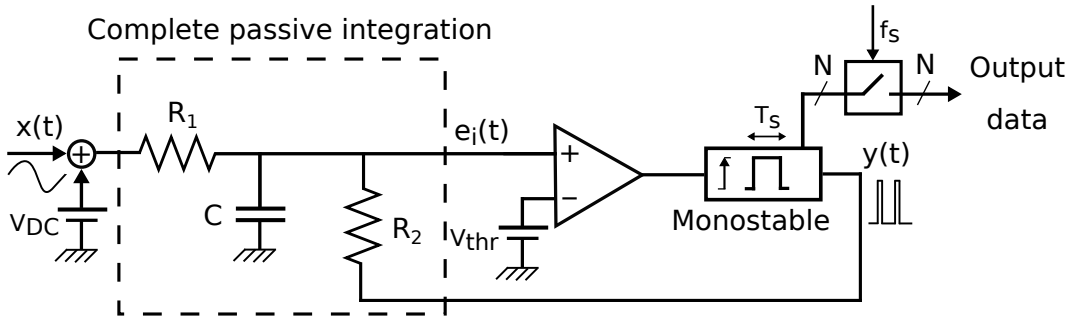


Figure 4.16: PFM-based architecture with complete passive integration.

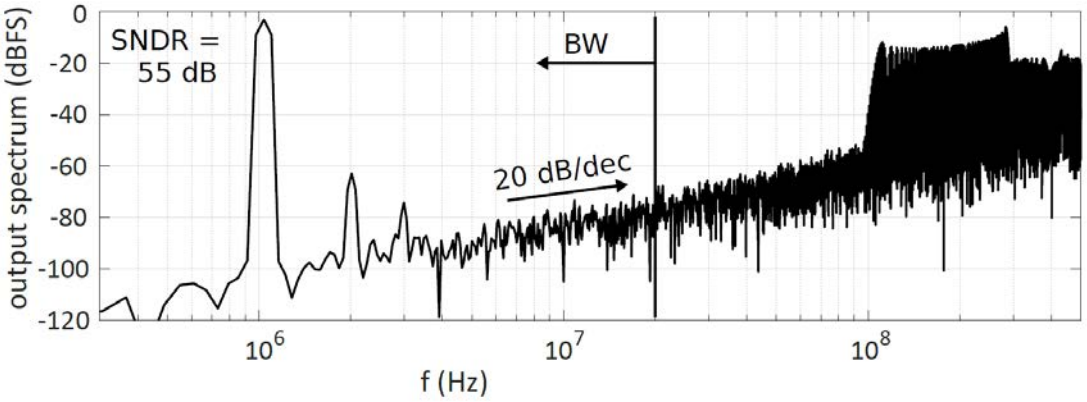


Figure 4.17: Behavioral simulation of the system of Fig. 4.16.

might require a high value of the RC product, which supposes large silicon area.

4.2.5 Conclusion

Along this section, we have been working on the development of a structure to implement in practice a PFM-based ADC. We explained how a pulse frequency modulator can be used as an efficient ADC, showing similar performance as ring oscillators based systems. The foundations of all the content described in this section are based on the PFM theory explained in Chapter 3. Once understood how a PFM-based ADC works, we proposed several circuits to make a practical implementation. Firstly, we proposed to use a PFM-based architecture in which a totally active integration was used. This architecture was intrinsically linear. Then, we split up the integration process into two different paths: the path of the input signal and the feedback path, which took us to an architecture whose implementation on silicon will be described later on. Secondly, we replaced the active integration of the input signal by a passive integrator and digitally correct the distortion after sampling. Finally, we proposed a PFM-based structure with complete passive integration in which the distortion can be kept under control if some design considerations are taken into account. This last system is a simple architecture that can be used to produce efficient ADCs.

4.3 A first approach to the implementation of VCO-based closed-loop architectures

So far, we have focused our research on open-loop VCO-based ADCs (although it is true that the proposed circuit to implement a pulse frequency modulator is a closed-loop circuit, at system level, it works similar to an open-loop architecture, Fig. 4.6). However, the PFM interpretation also provides us useful information that can be applied to the design of closed-loop VCO-based architectures. In this section, we will make a brief approach to summarize the main concepts derived from the PFM theory when implementing closed-loop structures. We will keep our attention on continuous-time $\Delta\Sigma$ modulators built with VCOs.

In principle, the implementation of continuous-time $\Delta\Sigma$ modulators with VCOs shares the benefits of other time-encoding techniques which map the amplitude of a signal into a pulsed waveform. Time-encoded signals are of digital nature. Therefore they are less sensitive to noise and supply limitations, and can be post-processed with digital circuits. However, these a priori advantages have shown to be efficient only when combined with other analogue techniques [44, 91–93]. Some of these limitations can be attributed to an incomplete understanding of VCO-based ADCs. The use of VCOs as analog integrators in continuous-time $\Delta\Sigma$ modulators is based on the assumption that a VCO is a phase integrator. This fact has been the pillar that supports all system level modeling of VCO-based continuous-time $\Delta\Sigma$ modulators so far. However, a closer look to how a VCO processes the input signal shows that some signal-dependent modulation components are also introduced (Fig. 3.3), making the integration "imperfect". Therefore, that system level modeling is based on an implicit approximation, namely the VCO output signal conveys the input signal in its low-pass spectrum once demodulated. With this integrator equivalence in mind, high order continuous-time $\Delta\Sigma$ modulators and even analog filters have been proposed used VCOs only [45, 48, 67, 94, 95]. Assuming that a VCO is a phase integrator, we may derive an easy rule to replace a conventional analog integrator by a VCO plus some digital logic (for instance, a counter). Using this easy rule, several working circuits have been successfully implemented. Nevertheless, some unclear questions arise. For example, what is the right choice for the rest oscillation frequency, what is the effect of connecting in cascade several VCO-based stages in terms of the modulation components or how the VCOs affect to the stability of the loop. These issues cannot be clearly answered with the integrator model.

The PFM theory can be also applied to the design of VCO-based continuous-time $\Delta\Sigma$ modulators and can be used to answer the previous queries that have not answered using the classical approaches yet. In this section, we will make a first approach to the application of PFM theory to the design of those systems, providing the mathematical foundations (equations that describe the output of a VCO-based integrator) and showing some application examples. This topic might be the starting point of an interesting and productive line of research for the future, but further investigations are out of the scope of this document.

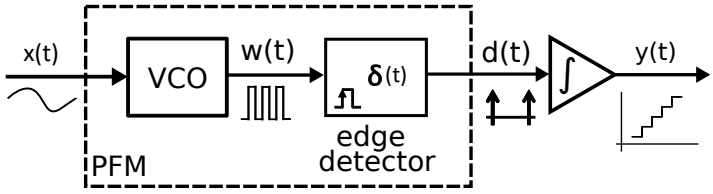


Figure 4.18: PFM followed by an integrator.

4.3.1 An "imperfect" integrator built with a VCO

As stated in the previous sections, a VCO can be analyzed as a signal encoder if the scheme depicted in Fig. 3.2 is considered. Making the same assumptions for the input signal $x(t)$ and the oscillation parameters of the VCO as in that figure, signal $d(t)$ will follow (3.3).

Now, we will place an integrator connected to $d(t)$ (Fig. 4.18). Then, the expression that describes $y(t)$ is:

$$\begin{aligned} y(t) &= \int_0^t d(\tau)d\tau = \\ & f_\mathrm{o}t + K_\mathrm{VCO}\int_0^t x(\tau)d\tau + \\ f_\mathrm{o}\sum_{q=1}^{\infty}\sum_{r=-\infty}^{\infty} & \frac{1}{\pi\left(q\cdot f_\mathrm{o}+r\cdot f_\mathrm{x}\right)} J_\mathrm{r}\left(q\cdot\frac{AK_\mathrm{VCO}}{f_\mathrm{x}}\right) \\ & \left(1+\frac{rf_\mathrm{x}}{q\cdot f_\mathrm{o}}\right)\sin\left(2\pi\left(q\cdot f_\mathrm{o}+r\cdot f_\mathrm{x}\right)t\right). \end{aligned} \tag{4.17}$$

As can be observed, the input signal $x(t)$ is integrated and multiplied by a gain term. Therefore, we are dealing with a structure that can be used to integrate signals. However, there are several high-frequency modulation components (we suppose that $f_\mathrm{o} >> f_\mathrm{x}$). These modulation components make the integration "imperfect". Finally, there is a growing term in time $f_\mathrm{o}t$. In a real implementation, this growing term must be compensated in some way. Due to the PFM-based nature of the system, hereinafter, we will refer to the structure of Fig 4.18 as a PFM-based integrator (PFMI).

The system of Fig. 4.18 can be used as a single ended integrator. To compensate the growing term in time, a similar PFM-based structure must be placed in parallel with the previous one, but this second PFMI will be connected to a constant input signal that make the VCO oscillate always at the rest frequency f_o (in our particular case $x(t) = 0$). The output $d(t)$ of the first PFMI (designated as $d_1(t)$) follows (3.3) and the output of the second PFMI ($d_2(t)$) follows:

$$d_2(t) = f_\mathrm{o} + \sum_{q=1}^{\infty} 2f_\mathrm{o}\cos\left(2\pi\cdot q\cdot f_\mathrm{o}t\right). \tag{4.18}$$

If we subtract both signals and calculate the integral of the subtraction, the

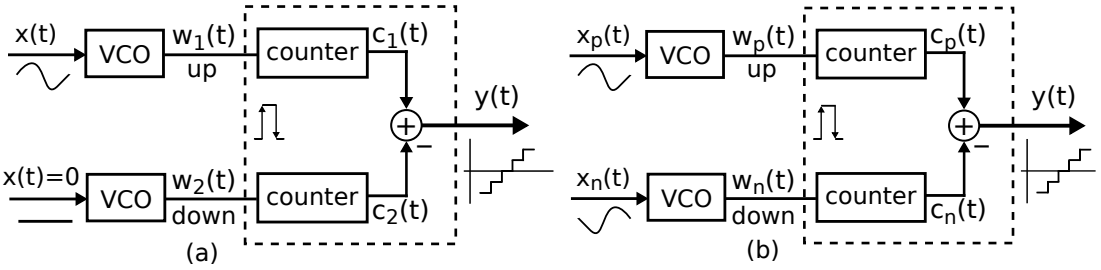


Figure 4.19: (a) Single ended PFMI, (b) Differential PFMI.

output signal $y(t)$ can be expressed as:

$$y(t) = K_{\mathrm{VCO}} \int_0^t x(\tau)d\tau + f_{\mathrm{o}} \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} \frac{1}{\pi\left(q \cdot f_{\mathrm{o}} + r \cdot f_{\mathrm{x}}\right)} J_{\mathrm{r}}\left(q \cdot \frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}}\right) \left(1 + \frac{r f_{\mathrm{x}}}{q \cdot f_{\mathrm{o}}}\right) \sin\left(2\pi\left(q \cdot f_{\mathrm{o}} + r \cdot f_{\mathrm{x}}\right) t\right) - f_{\mathrm{o}} \sum_{q=1}^{\infty} \frac{1}{\pi\left(q \cdot f_{\mathrm{o}}\right)} \sin\left(2\pi\left(q \cdot f_{\mathrm{o}}\right) t\right). \tag{4.19}$$

Now, the growing term in time does not appear anymore. This way the system output will remain bounded in time.

A practical single-ended architecture implemented with a PFMI can be built with the circuitry depicted in Fig. 4.19(a). Note that the integration of a Dirac delta impulse is a constant value, so that the integrator can be implemented with a counter that increments its count value at every Dirac delta impulse (making each value increment matches with the integrated "area" of a Dirac delta impulse). As every Dirac delta impulse matches in time with the rising edges of the VCO, we can directly connect the counter to the VCO. The counter will make the operations of both the edge detector and the integrator.

However, continuous-time $\Delta\Sigma$ modulators are typically implemented with differential integrators. The extension of the single ended PFMI to the differential PFMI can be easily made. In a differential architecture, the second VCO will be connected to the complementary input of the first VCO, instead of being connected to a constant value. This is shown in Fig. 4.19(b), where the input signal of the first VCO is $x_{\mathrm{p}}(t)$, and the input signal of the second VCO is $x_{\mathrm{n}}(t)$. These signals are defined as follows:

$$x_{\mathrm{p}}(t) = \frac{x(t)}{2}, \quad x_{\mathrm{n}}(t) = -\frac{x(t)}{2}. \tag{4.20}$$

So far, an input signal $x(t)$ with initial phase θ =0 was supposed for simplicity. If the initial phase $\theta \neq 0$, the expression for the modulation terms of (3.3) will

change according to [77]:

$$d(t) = f_{\mathrm{o}} + K_{\mathrm{VCO}} \cdot x(t) + 2f_{\mathrm{o}} \cdot \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} J_{\mathrm{r}} \left(q \cdot \frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}} \right) \left(1 + \frac{r f_{\mathrm{x}}}{q \cdot f_{\mathrm{o}}} \right) \cos \left(2\pi \left(q \cdot f_{\mathrm{o}} + r \cdot f_{\mathrm{x}} \right) t + r\theta - q \frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}} \sin \theta \right). \tag{4.21}$$

We will suppose that the initial phases are $\theta_p = 0$ and $\theta_n = \pi$ (for the P-side and the N-side of the differential structure respectively). If we apply these initial phases to (4.21), make the subtraction between (3.3) and (4.21) and integrate the result, we will get the following expression for $y(t)$:

$$y(t) = K_{\mathrm{VCO}} \int_0^t x_{\mathrm{p}}(\tau) d\tau + f_{\mathrm{o}} \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} \frac{1}{\pi \left(q \cdot f_{\mathrm{o}} + (2r+1) \cdot f_{\mathrm{x}} \right)} J_{2\mathrm{r}+1} \left(q \cdot \frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}} \right) \left(1 + \frac{(2r+1) f_{\mathrm{x}}}{q \cdot f_{\mathrm{o}}} \right) \sin \left(2\pi \left(q \cdot f_{\mathrm{o}} + (2r+1) \cdot f_{\mathrm{x}} \right) t \right). \tag{4.22}$$

All the even modulation components placed at the surroundings of each multiple of the rest oscillation frequency f_{o} are removed, just as in traditional differential structures.

Observing the mathematical foundations of the PFMI architecture, we notice that this architecture works as an "imperfect" integrator in which modulation components are added. If we want to build $\Delta\Sigma$ modulators with this structure, then we may think on replacing conventional opamp-based integrators by PFMIs. With this purpose in mind, we will firstly propose a linear model for the PFMI (for simplicity we will deal with the single ended architecture). According to (4.19), a PFMI follows the linear model depicted in Fig 4.20(a). If the integrator block is moved before the summation block, we will get the model of the left side of Fig. 4.20(b). This last model is similar to the conventional white noise model used in $\Delta\Sigma$ modulators when representing the process of integration and quantization (right side of Fig. 4.20(b)). However, there is one important difference, whereas the white noise model is a statistical model, we know the analytical equations that describe the modulation components. Note that for a complete equivalence the gains of both models must match, that's why we need to accomplish with the following condition:

$$K_{\mathrm{VCO}} = f_{\mathrm{s}}. \tag{4.23}$$

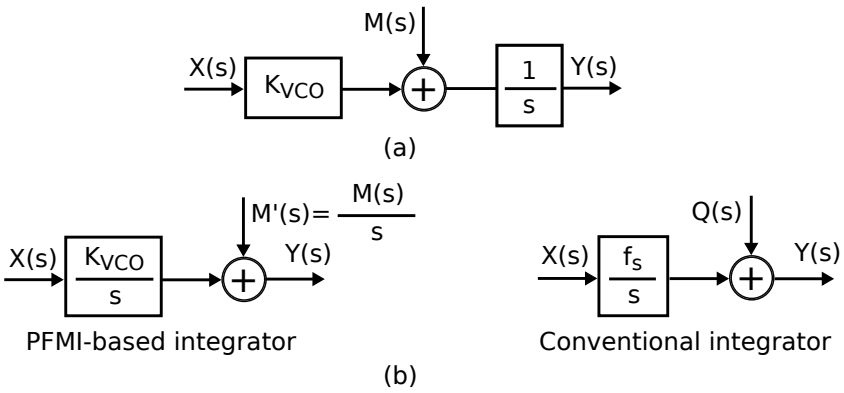


Figure 4.20: (a) Linear model for PFMI, (b) Equivalence between PFM-based and conventional integrator.

Therefore, by now, we have achieved a VCO-based linear model that can be used to design continuous-time $\Delta\Sigma$ modulators. Our model has the advantage of being based on well-known equations that may allow us to determine what is the effect of the modulation components regardless the position of the VCOs in the $\Delta\Sigma$ loop. This way we will be able to correctly choose the oscillation parameters of the VCOs and optimize the system performance. Stability analyses might also be made with this approach. Equations (4.19) and (4.22) are the starting point of further investigation that is out of the scope of this document. Our propose in this section is only providing the mathematical foundations based on the PFM theory to the design of continuous-time $\Delta\Sigma$ modulators (or even analog filters) with VCOs.

In closing, we will provide some examples of the PFMI-based model of Fig. 4.20(b) applied to the design of continuous-time $\Delta\Sigma$ modulators.

4.3.2 Application examples

Firstly, we will deal with the simplest continuous-time $\Delta\Sigma$ modulator, which is the first-order system. Fig. 4.21(a) shows the system built with the conventional integrator in the left side and the equivalent system with the PFMI in the right side. Fig. 4.22 shows the behavioral simulations for both of the systems depicted in Fig. 4.21(a). One-bit quantizer is used for the conventional case, and $f_o = K_{VCO} = f_s$ is used for the PFMI-based case. The OSR is 64 and we use a -3 dBFS sinusoidal input signal. The resulting SNDR equals 53 dB, is the same for both cases, and the spectra look similar. Although in practice this PFMI-based system is not an efficient implementation of an ADC, it permits us to validate the proposed equivalence.

For the behavioral simulation, the single-ended PFMI model shown in Fig. 4.19(a) was used. However, in practical designs, using a second VCO to compensate the growing term of (4.17) is not appropriate. This architecture can be easily simplified if we use the feedback path to compensate this term. The only thing we have to do is placing the sampler before the loop. Then the integration process is split up into two different paths. On the one hand, we have the integration of

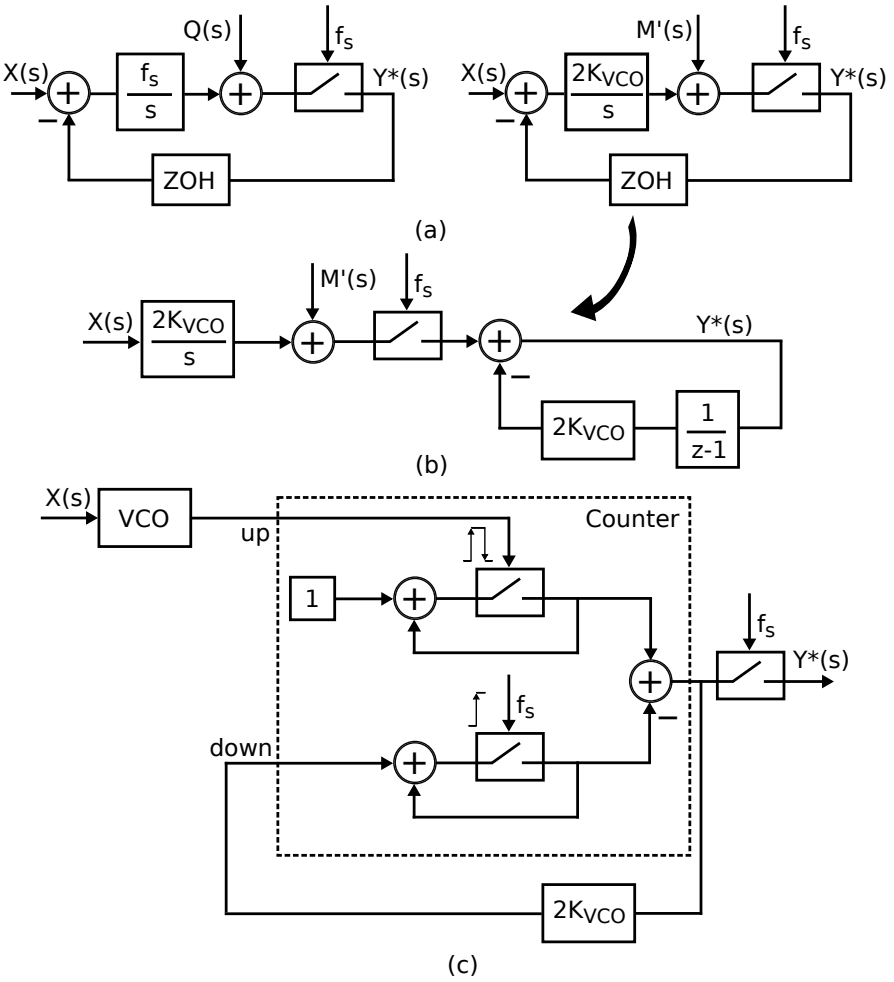


Figure 4.21: PFMI-based first-order noise-shaping architecture: (a) Linear models, (b) PFMI-based implementation with open-loop VCO, (c) Implementation with an up-down counter

the input signal that is made by the VCO and, on the other hand, we have the integration of the feedback loop that can be made in the discrete domain. These considerations take us to the model of Fig. 4.21(b), which is strictly equivalent to the models of Fig. 4.21(a). If analyzed, we notice that the feedback can be implemented in practice with a counter that decrements the count value with the rising edges of the clock signal, leading to the system of Fig. 4.21(c). This simplification was used in practice in [48].

Approaches to the design of higher order architectures were also made with the proposed equivalence, for instance, to design a third order noise shaped structure. We used [96] to design a third-order continuous-time $\Delta\Sigma$ modulator and, later on, design its PFMI-based equivalence. Fig. 4.23 shows both systems.

The main difference between both systems lies in the modulation components added in each integration stage for the model implemented with VCOs (called $M'_1(s)$, $M'_2(s)$, and $M'_3(s)$). These components are differently shaped depending on the stage they belong to (in our example $M'_1(s)$ is first-order shaped, $M'_2(s)$ is second-order shaped, and $M'_3(s)$ is third-order shaped). Consequently, we have

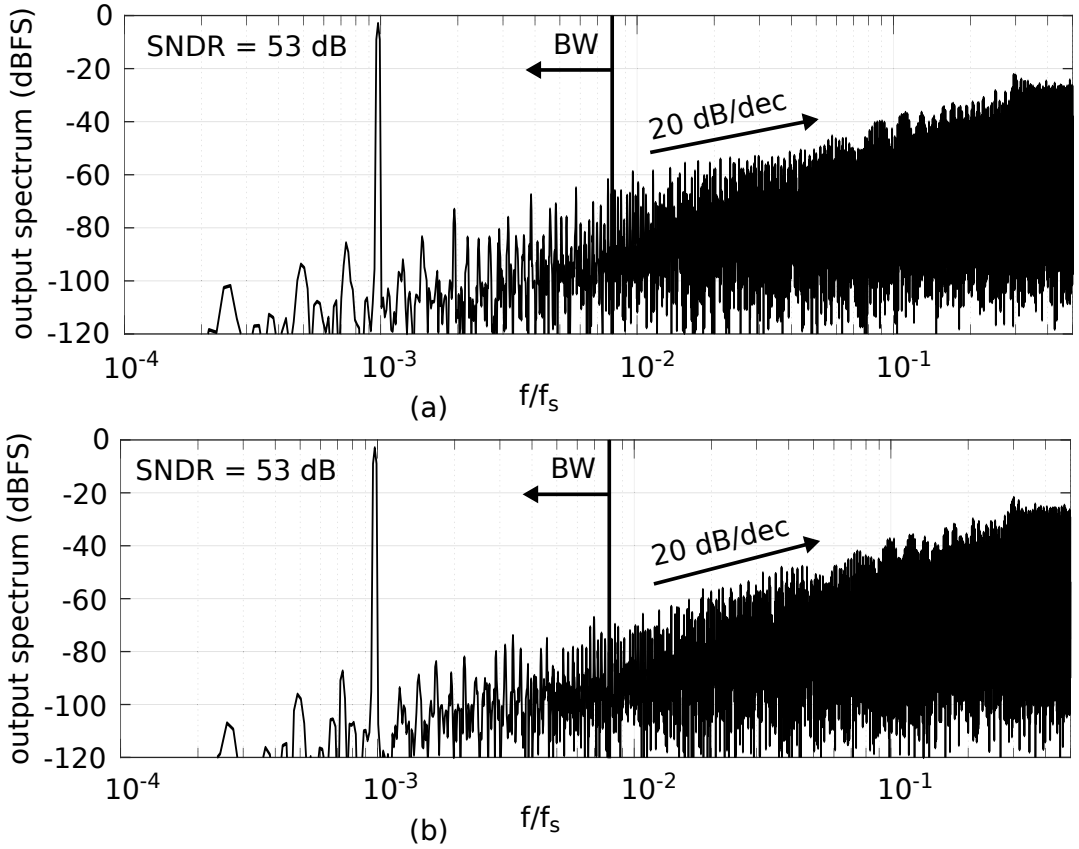


Figure 4.22: Behavioral simulations for the first-order continuous-time $\Delta\Sigma$ modulator implemented with a conventional integrator (a), and implemented with a PFMI (b).

to choose the rest oscillation frequencies of each stage very carefully with the goal of making them not limit the expected performance of the system. The easiest way to proceed is increasing the rest oscillation frequency as we go from the last VCO to the first one. This way, the modulation components that are less-order shaped are further away from the band of interest.

Fig. 4.24 shows a behavioral simulation of both systems. For Fig. 4.23(a), one-bit quantizer is used. For Fig. 4.23(b) $f_{o,1} \approx 6f_s$, $f_{o,2} \approx 2.5f_s$, $f_{o,3} \approx 2f_s$, and $K_{VCO,1} = K_{VCO,2} = K_{VCO,3} = f_s$. We use a OSR equal to 256 (in order to help us to get the oscillation components away from the band of interest) and a -12 dBFS sinusoidal input signal. Note that the difference between the rest oscillation frequencies of two successive VCOs is much higher than twice the bandwidth considered for the converter.

The resulting SNDR is 108 dB for both cases. Third-order noise shaping is clearly visible in both systems. The architecture implemented with VCOs shows intermodulation components due to the different oscillation frequencies of the VCOs. In this case, we followed the rule stated above by which the slowest VCO is the last one and we increase the rest oscillation frequency as we go from the last stage to the first stage.

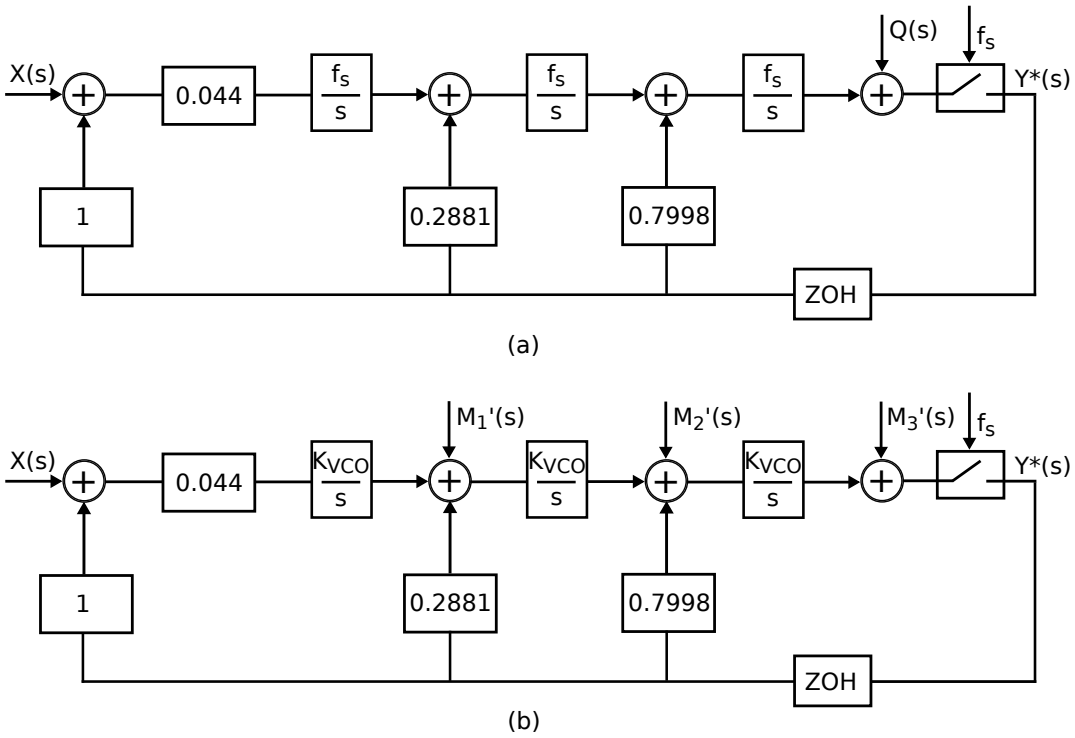


Figure 4.23: Linear model of a third-order continuous-time $\Delta\Sigma$ modulator implemented with conventional integrators (a), and implemented with VCOs (b).

4.3.3 Conclusion

In this section, we have shown the mathematical foundations that describe the integration process when VCOs are used to carry it out. This integration is associated with a modulation process that makes the integration "imperfect", and must be considered when implementing continuous-time $\Delta\Sigma$ modulators with VCOs. The equations we have provided may be the way of answering many of the queries unsolved when designing this type of system. We have also provided a linear way of introducing the VCO-based integration into the linear models typically used when designing $\Delta\Sigma$ modulators, showing the equivalence with a conventional analog integrator. Finally, we have provided two application examples that validate the proposed equivalence.

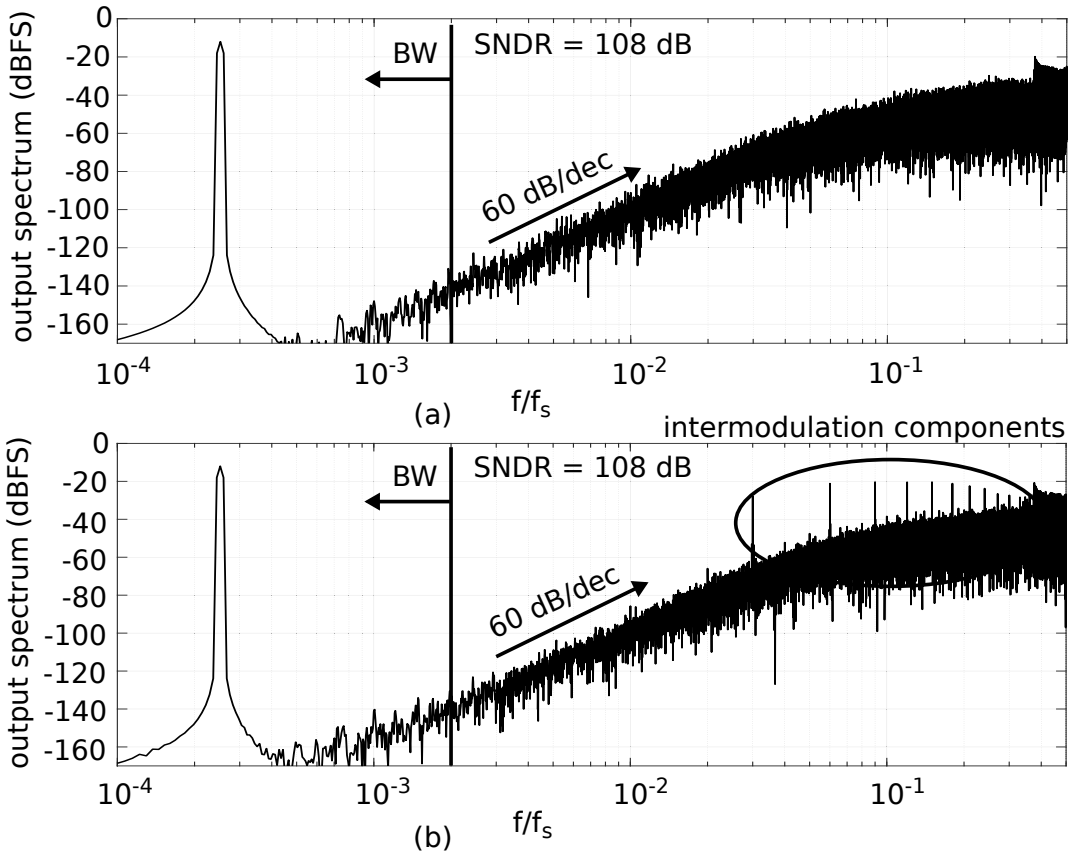


Figure 4.24: Behavioral simulations for the third-order continuous-time $\Delta\Sigma$ modulator implemented with conventional integrators (a), and implemented with PFMIs (b).

Chapter 5

VCO-based multistage noise shaping architectures

In Chapter 3 we proposed a new methodology for the analysis of open-loop VCO-based ADCs. We showed that, ideally, in Fig. 3.7 any noise shaping order can be achieved if the proper filter $H_{\mathrm{n}}(s)$ is selected. However, in practice, only the first-order case or an approximation to the second-order one can be implemented. This supposes one of the limitations of open-loop VCO-based structures. To overcome this issue, an increase of the noise-shaping order is usually accomplished by incorporating analogue integrators into a $\Delta\Sigma$ loop combined with VCO-based quantization [44]. However, the performance of these systems is restricted by the power consumption of the analog integrators. Alternatively, continuous-time $\Delta\Sigma$ modulators implemented only with VCOs were proposed in [45, 74].

One potential solution to increment the order of the converter is to build VCO-based multistage noise shaping architectures (MASH) [97], where each stage is a first-order VCO-based architecture. In this chapter, we will explain how the generic VCO-based architecture can be placed in cascade configurations to form MASH structures. In principle, the approach can be done for any order of the generic VCO-based ADC. Nevertheless, we will limit the discussion to the case where the generic VCO-based ADC is first-order noise-shaped because this is the structure that can be implemented in practice. We will describe a MASH architecture built with two VCO-based stages, so that the resulting structure exhibits second-order noise shaping [98, 99]. A brief extension to structures with more than two stages will also be proposed. We will see that the PFM interpretation of the VCO-based architectures will allow us to get a major understanding of the spectral processes involved in MASH architectures. Furthermore, we will be able to analyze practical limitations of these structures, such as the finite interconnection bandwidth and gain mismatch between stages.

Then, a novel technique to optimize the NTF zeros of MASH configurations will be proposed. This technique will be applied to VCO-based MASH architectures and it will be validated through behavioral simulations.

Finally, how to build MASH architectures with a digital precoded VCO-based first stage will be also described.

5.1 Analysis of MASH VCO-based ADC architectures using the PFM theory

The operating principle of our proposed MASH architecture can be understood from the model shown in Fig. 5.1. It consists of a first VCO-based ADC, an error estimator block and a second VCO-based ADC. In the figure, each VCO-based ADC is modeled according to the previously derived model of Fig. 3.10. As before, to simplify the discussion, the VCO gains were normalized to unity and the offset contributions corresponding to the VCO rest oscillation f_o were omitted. On the top level, the architecture is similar to typical continuous-time MASH $\Delta\Sigma$ modulators [100, 101], which also consist of a first ADC, an error estimator and a second ADC. However, in our case, no conventional analog blocks (such as opamps, comparators, ...) are used, only VCOs and digital circuitry. The first VCO-based ADC is driven by the overall input signal $X(s)$ and produces a digital, discrete time output signal $Y_1(z)$. From the analysis above, we know that:

$$Y_1(z) = [\text{STF } (X(s) + M_{1,\text{LF}}(s))]^* + U_{1,\text{al}}(z)(1 - z^{-1}), \tag{5.1}$$

where the aliased modulation component $U_{1,\text{al}}(z)$ is given by:

$$U_{1,\text{al}}(z) = \left[\frac{M_{1,\text{HF}}}{sT_s}\right]^*. \tag{5.2}$$

In practice the performance is limited by the first order differentiated contribution of $U_{1,\text{al}}(z)$.

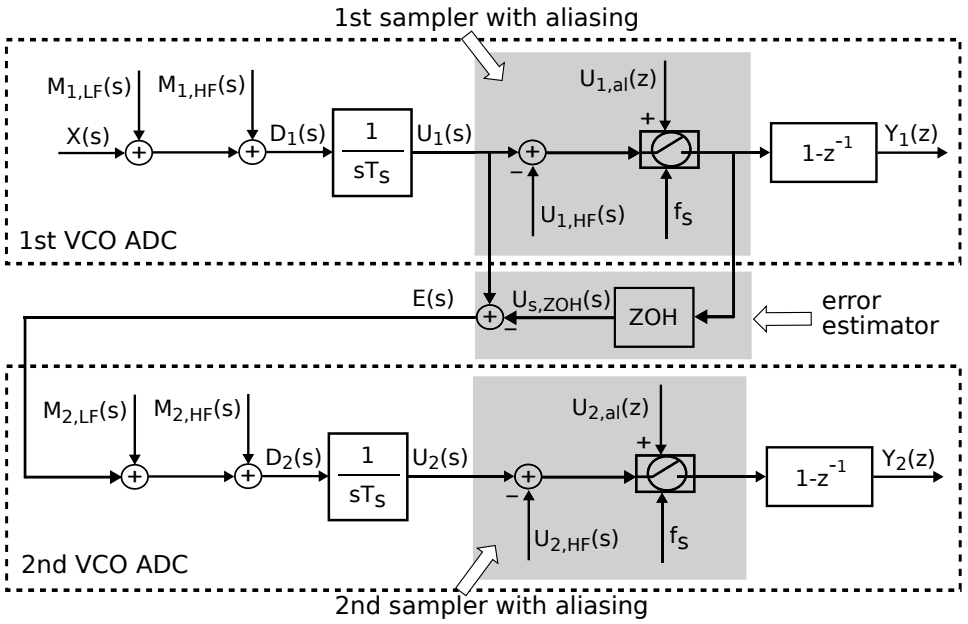


Figure 5.1: Model describing the proposed 1-1 VCO-based MASH.

The key enabling element in our proposed structure is the error estimator block, which generates a continuous-time signal $e(t)$. Signal $e(t)$ is an estimation of the dominant first stage's error. Since this error is the aliasing error $U_{1,\mathrm{al}}(z)$ that occurs in the sampler, the error signal can be obtained by taking the difference between the sampler's input and its output, as shown in Fig. 5.1. To be more precise, we can write E as:

$$E = U_{1,\mathrm{LF}} + U_{1,HF} - [U_{1,\mathrm{LF}}]^* H_{\mathrm{ZOH}} - U_{1,\mathrm{al}}(z) H_{\mathrm{ZOH}}, \tag{5.3}$$

where $U_{1,\mathrm{LF}}$ and $U_{1,\mathrm{HF}}$ are defined as follows:

$$U_1 = U_{1,\mathrm{LF}} + U_{1,\mathrm{HF}}, \tag{5.4}$$

with

$$U_{1,\mathrm{LF}} = \frac{X + M_{1,\mathrm{LF}}}{sT_s}, \tag{5.5}$$

$$U_{1,\mathrm{HF}} = \frac{M_{1,\mathrm{HF}}}{sT_s}. \tag{5.6}$$

Here, abstraction is made from the transform domain (either frequency domain or s-domain), and we are implicitly assuming that the s-domain representation of the 'z'-variable is e^{sT_s}. As before the subscript $_{\mathrm{LF}}$ denotes low frequency components that are not prone to aliasing. The transfer function H_{ZOH} corresponds to the zero order hold pulse and equals $(1 - e^{-sT_\mathrm{s}})/(sT_\mathrm{s})$. Clearly when taking into account that for low frequencies $H_{\mathrm{ZOH}} \approx 1$, we immediately see that the low frequency component E_{LF} of our error estimation E corresponds to the aliasing error:

$$E_{LF} \approx -U_{1,\mathrm{al}},$$

which is the desired behavior. This error signal E drives the second VCO and hence, in a similar way as for (5.1), we can write:

$$Y_2(z) = [\mathrm{STF}\ (E(s) + M_{2,\mathrm{LF}}(s))]^* + U_{2,\mathrm{al}}(z)(1 - z^{-1}). \tag{5.7}$$

Now, the core idea of a MASH structure is to pass each stage's output through proper noise cancellation filter (NCF) and combining them into the overall output signal $Y(z)$. If done appropriately , the error from the first stage is removed and overall higher noise shaping order is achieved. The most obvious choice for the noise cancellation filters NCF_1 and NCF_2 is[1]:

$$NCF_1 = 1, \qquad NCF_2 = 1 - z^{-1}. \tag{5.8}$$

Then the overall output signal $Y(z)$ is obtained as:

$$\begin{aligned} Y(z) &= NCF_1 \cdot Y_1(z) + NCF_2 \cdot Y_2(z) \\ &= Y_1(z) + (1 - z^{-1}) \cdot Y_2(z). \end{aligned} \tag{5.9}$$

[1]If we work with non unity values of K_{VCO} appropriate gain factors should be added to the noise cancellation filters.

If we now make the approximation that the filter effect of the zero order hold pulse is negligible we can write the overall output as:

$$\begin{aligned} Y(z) \approx & [\mathrm{STF} \cdot X(s)]^* + \\ & [\mathrm{STF} \cdot M_{1,\mathrm{LF}}(s)]^* + \\ & \left(1 - z^{-1}\right) \cdot [1 - \mathrm{STF}]^* \cdot U_{1,\mathrm{al}}(z) + \\ & \left(1 - z^{-1}\right) \cdot [\mathrm{STF} \cdot M_{2,\mathrm{LF}}(s)]^* + \\ & \left(1 - z^{-1}\right)^2 \cdot U_{2,\mathrm{al}}(z). \end{aligned} \tag{5.10}$$

In the above expression, we can make the further approximation that in the signal band the signal transfer function STF is approximately unity. Then the expression can be further simplified into:

$$\begin{aligned} Y(z) \approx & [X(s)]^* + [M_{1,\mathrm{LF}}(s)]^* + \\ & \left(1 - z^{-1}\right) \cdot [M_{2,\mathrm{LF}}(s)]^* + \\ & \left(1 - z^{-1}\right)^2 \cdot U_{2,\mathrm{al}}(z). \end{aligned} \tag{5.11}$$

From this expression we see that there are three terms that can degrade the performance. First, there is the contribution from $M_{1,\mathrm{LF}}$, the fundamental PFM encoding error of the first stage (see Fig. 3.6). The way to keep this error contribution under control is to limit the input signal amplitude and to operate the first VCO at a sufficiently high effective oscillation frequency. Second, there is a contribution from $M_{2,\mathrm{LF}}$, the fundamental PFM encoding error of the second stage. This contribution is first order differentiated, and hence should not limit the performance. However, the input of the second VCO is the error signal whose amplitude is large, which is not a favorable situation for this error contribution (see Fig. 3.6). Hence, to keep this error contribution under control the second VCO should be operated at a sufficiently high effective oscillation frequency. Finally, there is the second stage aliasing error. If the appropriate measures are taken to control the fundamental PFM encoding error terms, (5.11) can be further simplified into:

$$Y(z) \approx [X(s)]^* + \left(1 - z^{-1}\right)^2 \cdot U_{2,\mathrm{al}}(z). \tag{5.12}$$

In this expression we see that the limiting factor is formed by the second stage aliasing error, but this error exhibits a second-order spectral shaping.

5.1.1 Practical implementation

The key element in the practical implementation is the error estimator block. In order to better understand its operation, Fig. 5.2 shows the relevant time domain waveforms: i.e. $d_1(t)$, $u_1(t)$, the sampled and held version of $u(t)$ ($u_{\mathrm{s,ZOH}}(t)$) and the error signal $e(t)$ for the case of a single-phase VCO. From the figure it is clear that the error signal $e(t)$ is always discrete in amplitude, and hence can be implemented with digital circuitry. The error estimator circuit can be combined with the efficient (and almost standard practice) circuit of Fig. 2.10(c). In this

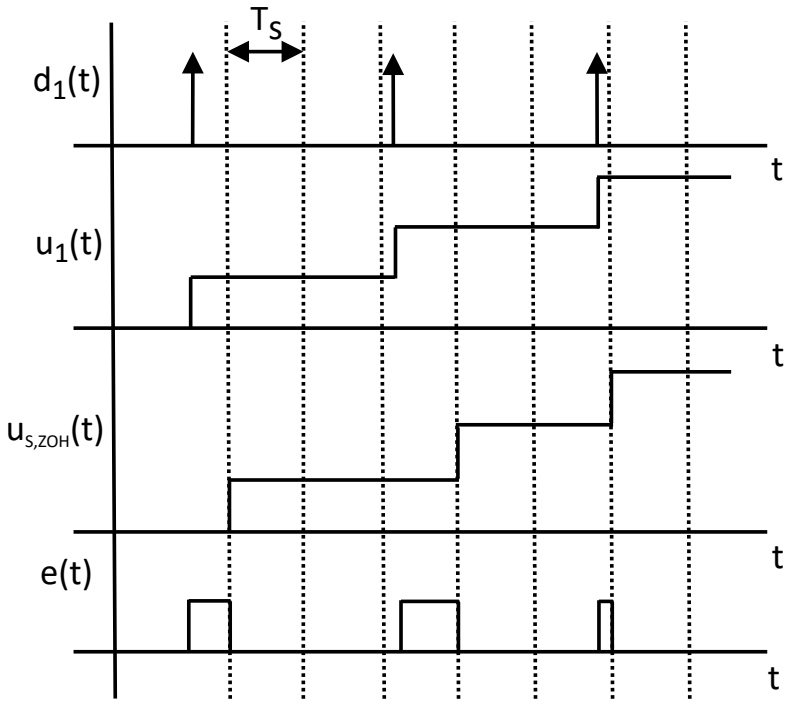


Figure 5.2: Time domain waveforms of the relevant signals to obtain the error estimation $e(t)$ in a VCO-based stage.

case, if the following condition relative to the maximum oscillation frequency in the first VCO is accomplished:

$$f_{1,\max} \leq \frac{f_s}{2}, \tag{5.13}$$

the signal $e(t)$ is even a two-level (single-bit) signal.

The proposed implementation is shown in Fig. 5.3 for the generic case of a M-phases VCO in the first stage. At the moment, we will focus on the case in which M =1. By drawing the waveforms for this circuit under condition (5.13), it is immediately verified that signal $e(t)$ is identical to the desired waveform of Fig. 5.2, which confirms the correct operation of the circuit. This configuration has an additional advantage: the second VCO is driven by a single-bit signal and hence will always operate linearly at two possible oscillation frequencies [102]. To confirm the performance of this structure, several behavioral simulations were performed. Fig. 5.4 shows a typical resulting output spectrum. The following parameters were used in the simulation:

$$f_{\text{osc},1}(t) = f_{\text{o},1} + K_{\text{VCO},1} \cdot x(t) = \frac{f_s}{4} + \frac{f_s}{4} \cdot x(t), \tag{5.14}$$

$$f_{\text{osc},2}(t) = f_{\text{o},2} + K_{\text{VCO},2} \cdot e(t) = \frac{f_s}{4} + \frac{f_s}{4} \cdot e(t), \tag{5.15}$$

where the sub-index '1' is referred to the first stage VCO and '2' is referred to the second stage VCO. Here, the two digital levels of $e(t)$ correspond to the

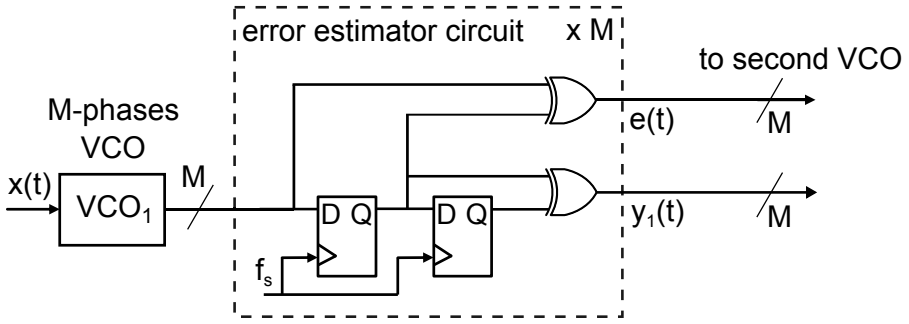


Figure 5.3: Practical implementation of the error estimator circuit with a M-phases VCO.

signal values e= -1 and e= 1 and, as before, the input signal $x(t)$ is scaled such that it is in the interval [-1, 1]. The input signal was a -3 dBFS sinusoid with a signal frequency $f_x = f_s/1024$. The plot clearly demonstrates second-order spectral shaping. For an OSR= 64, the SNDR is 72 dB. This performance seems modest compared to the performance demonstrated in the second-order case of Fig. 3.11(b) and the (approximately) second-order case of Fig. 3.18, where the SNDR was respectively 95 dB and 93 dB for the same OSR. However, it is important to note that both y_1 and y_2 are single-bit signals, whereas the output signal for the theoretical case of Fig. 3.11(b) was a real number that cannot be represented with a finite number of bits, and the output signal for the case of Fig. 3.18 was an 8-bit signal.

The extension to the multiphase case can be built by replicating the error estimator circuit for each of the phases in the first VCO (as shown in Fig. 5.3) and combining all the error signals into a multibit signal. Then, the second VCO works a digital controlled oscillator [103–105]. Fig. 5.4(b) shows a simulation of the MASH architecture implemented with 15-phases VCOs, both in the first and the second stage. With similar parameters to Fig. 5.4(a) the SNDR is 93 dB, approximately the same as in Fig. 3.11(b).

5.1.2 Finite interconnection bandwidth and gain mismatch

There are two important performance limiting factors in the practical implementation described above: i.e. interconnection bandwidth and VCO gain mismatch in the second VCO. Both are illustrated in Fig. 5.5. Hereinafter, we will deal with single-phase VCOs in the depicted simulations, but the analyzed limiting factors could be similarly extended to the multiphase case.

The interconnection bandwidth is associated to the XOR-gate that generates the error signal $e(t)$ (see Fig. 5.3). This gate has to drive the load formed by the input impedance of the second VCO. However, it cannot produce infinitely steep edges, which were implicitly assumed in the discussion above (see the waveforms in Fig. 5.2). To model this effect, the bandwidth limiting low-pass filter $LP(s)$ is inserted in Fig. 5.5. In addition to the finite coupling bandwidth, the gain of the second VCO ($K_{\mathrm{VCO},2}$) cannot be controlled with an infinite accuracy. Due to this, the gain of the second VCO will always deviate from the desired value.

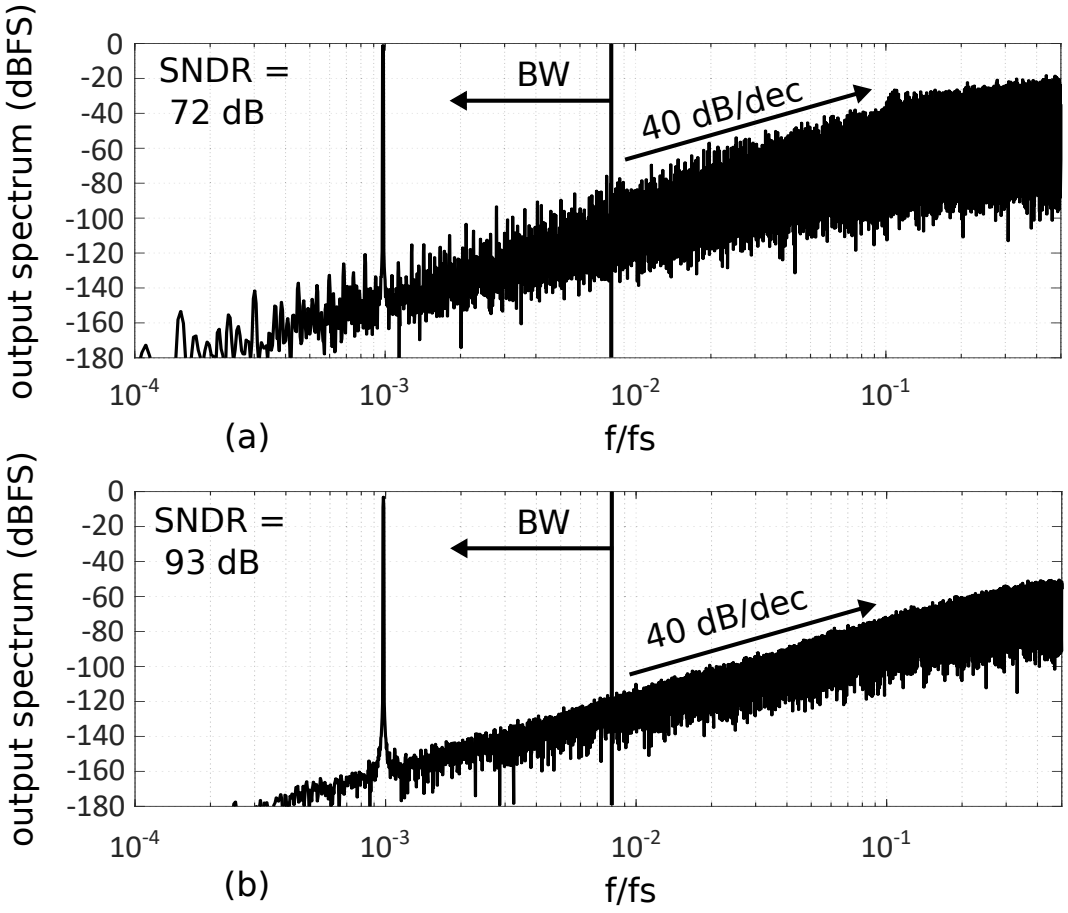


Figure 5.4: VCO-based MASH output spectrum with: (a) single-phase VCOs, and (b) multiphase VCOs (M =15).

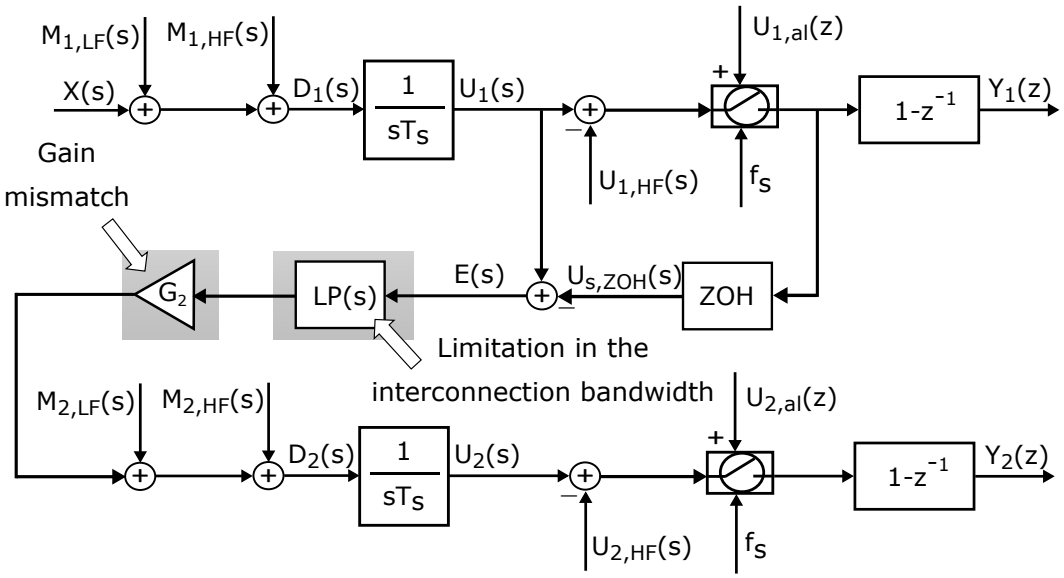


Figure 5.5: Linear model for the proposed 1-1 VCO-based-MASH incorporating finite coupling bandwidth and gain mismatch in the second VCO.

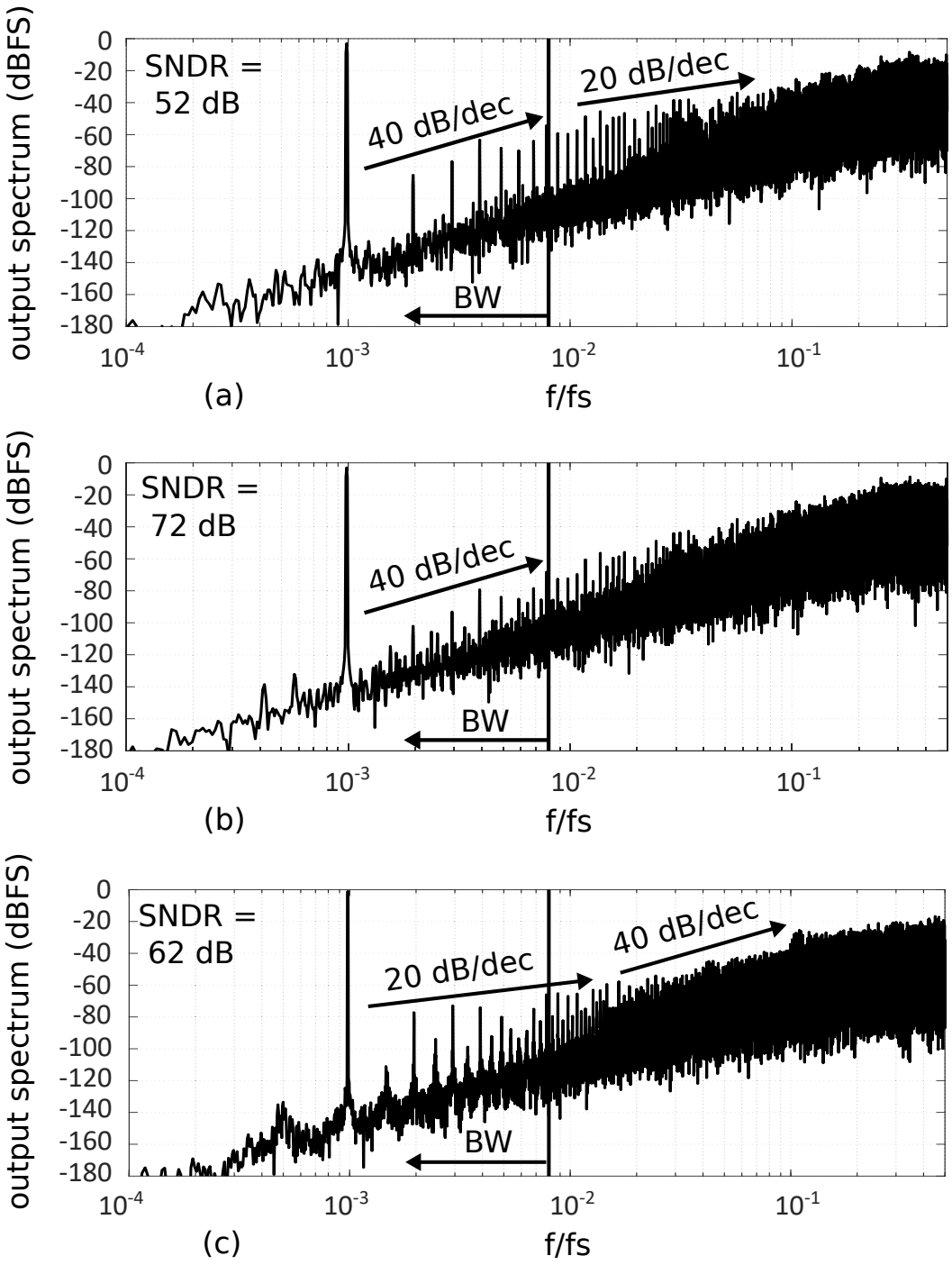


Figure 5.6: 1-1 VCO-based-MASH output spectrum with limited bandwidth in the interconnection path, (a) $f_c = BW$ and (b) $f_c = 10 \cdot BW$, and (c) with a gain mismatch of 20%

To take this effect into account a gain mismatch coefficient G_2 was added to the model. When we analyze these effect and make the same approximations as in the derivation of (5.11), we come to the conclusion that the actual conversion result $Y'(z)$ is now:

$$Y'(z) = Y(z) + U_{1,\text{leak}}, \tag{5.16}$$

where $Y(z)$ stands for the ideal conversion result of (5.11) and $U_{1,\text{leak}}$ corresponds to a leakage term which, within the approximations that were used to obtain (5.11), can be found as:

$$U_{1,\text{leak}} = [1 - G_2 \cdot LP(s) \cdot STF]^* \cdot \left(1 - z^{-1}\right) U_{1,\text{al}}(z). \tag{5.17}$$

Note that such a leakage effect is very similar to what occurs in other types of MASH converters [106, 107]. To study the effect of the finite interconnection bandwidth, let us now, for the moment assume that there is no gain mismatch (i.e. $G_2 = 1$). Clearly, the noise leakage term will be nonzero if $LP \neq 1$. In this case we retain an error term which only has first order spectral shaping. Note that also a nonzero phase shift will cause the noise leakage. To illustrate this, we have performed the same simulation as the one of Fig. 5.4, but now with finite interconnection bandwidth. This is modeled by setting LP to a first order low-pass filter with a cut-off frequency f_c equal to the desired signal bandwidth ($BW = f_s/128$), which from a naive point of view seems adequate. The result is shown in Fig. 5.6(a). It is clear that the spectral shaping is severely affected. As expected the degradation in considerably worse at high frequency (where LP is not at all close to unity). The resulting SNDR is severely degraded and is only 52 dB. In order to restore the original performance, the interconnection bandwidth must be increased to a value much higher than the intended signal bandwidth. In our simulation experiments (with varying OSRs) we found that it is a good strategy to aim for an interconnection bandwidth that is, at least, ten times higher than the intended signal bandwidth. This is illustrated in Fig. 5.6(b), where it can be observed that the original performance is restored.

The effect of a gain mismatch is illustrated in Fig. 5.6(c), which shows the result for the case of a mismatch of 20%. Clearly also here, the spectral shaping is affected, with a first-order shaped error contribution which dominates in the signal band. The SNDR is degraded to 62 dB. Also this mismatch effect is identical to mismatch effects as they occur in other types of MASH modulators. If the exact gain of the second VCO is known (e.g. through some type of adaptive estimation or factory calibration [107]), it can be incorporated in the noise cancellation filter NCF_2, which should then be modified into $(1 - z^{-1})/G_2$. If this is done for the case of Fig. 5.6(c), the original spectrum of Fig. 5.4 is again restored and the SNDR is again equal to 72 dB.

5.1.3 Extension to higher order MASH architectures

The model proposed in Fig. 5.1 can be extended to the implementation of higher order MASH architectures. These structures will be built by replicating the error estimator block between the stages (similarly to Fig. 5.1) and combining the outputs through proper NCFs. Just to provide an example, a behavioral

simulation of a third-order noise-shaping MASH architecture is shown in Fig. 5.7. In this case, the parameters used for the simulation are the same as in Fig. 5.4(b) with 15-phases VCOs. The NCFs used are the following:

$$NCF_1 = 1, \quad NCF_2 = 1 - z^{-1}, \quad NCF_3 = \left(1 - z^{-1}\right)^2. \tag{5.18}$$

As can be appreciated, third-order noise-shaping is clearly visible.

Nevertheless, whereas implementing in practice the second order architecture could take us to an average difficulty circuit design, higher order structures might suppose very complicated circuits due to the effects studied in the previous section. For instance, as an indicator to the reader, the simulation shown in Fig. 5.7 is very sensitive to the variations of the gains in each stage. A very small variation in the VCO gain of the second or the third stage (less than the 1%) makes the low frequency spectrum become second-order noise shaped, instead of third-order noise shaped. Consequently, the SNDR gets lower and we lose the advantage of the third stage. A way of dealing with this issue may be the design of adaptive NCFs that compensate the gain deviation.

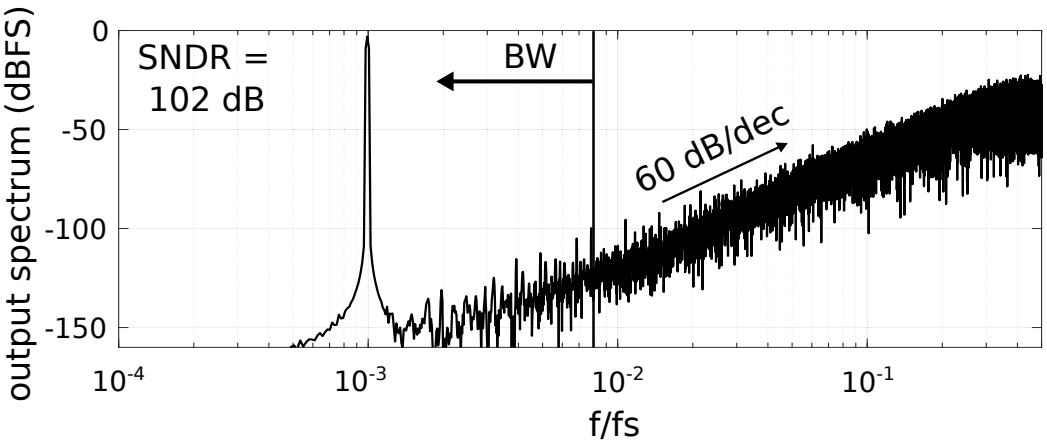


Figure 5.7: Third-order MASH behavioral simulation with 15-phases VCOs.

5.1.4 Conclusion

We have described a novel methodology to analyze and design VCO-based MASH architectures based on the PFM theory proposed previously. This approach allowed us to know how all the errors involved in the conversion affect to the performance of the system.

We have limited the discussion to the case in which each stage of the system is a first-order structure because it is the architecture that can be implemented in practice. We have used the linear models of Chapter 3 to get the equations that describe the performance of a 1-1 VCO-based MASH architecture, and we have validated them through behavioral simulations.

The performance of MASH architectures can be degraded by several phenomena. Here, we dealt with two of them, the finite interconnection bandwidth and the gain mismatch between stages. To study these issues, we have also used the

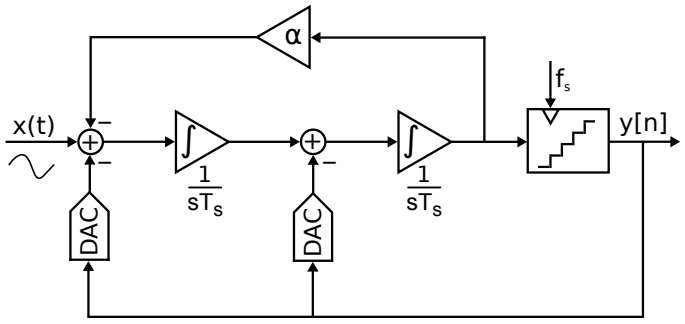


Figure 5.8: Second-order continuous-time modulator with control of the NTF zeros.

PFM theory, getting results through simulations that match with what was expected from equations. On the one hand, to overcome the finite interconnection issue, we found that we need an interconnection bandwidth that is, at least, ten times higher than the intended bandwidth of the converter. On the other hand, to overcome the gain mismatch between stages, factory calibration or adaptive filters can be used.

Finally, we have extended the same approach to build higher order systems. The implementation of a third-order VCO-based MASH architecture was provided as an example.

5.2 Optimal NTF zero placement in MASH VCO-based ADCs with higher order noise shaping

Until now, all the published MASH VCO-based ADC structures (the same for those proposed in this document) have the limitation that all the noise-transfer-function (NTF) zeros are at DC. However, it has long been known that improved performance can be obtained if the NTF zeros are placed at optimized positions over the signal band [108]. In this section, we will present a technique to achieve this making use of the PFM interpretation of VCO-based ADCs.

5.2.1 1-1 continuous-time MASH modulator with optimized NTF zeros

In order to construct our MASH VCO-ADC architecture we will work in two steps: we will start from a conventional single-loop continuous-time $\Delta\Sigma$ modulator with optimized zeros and transform it into a MASH structure. Then, in a second step, we will replace the analog integrators by VCO-based circuits.

Hence, we start from the single-loop continuous-time prototype shown in Fig. 5.8. As the figure shows, there is a local feedback path (α) coupled around the two integrators. Due to this, the two open-loop poles at DC (due to the integrators) are shifted away from DC and create two resonant complex conjugate

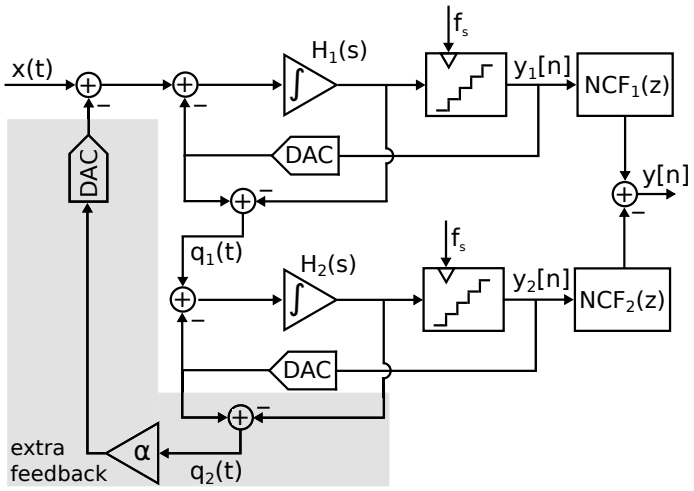


Figure 5.9: 1-1 continuous-time MASH modulator with control of the NTF zeros.

poles at a frequency (f_{N}) that is defined by the value of the factor α:

$$f_{\mathrm{N}} = \frac{f_s}{2\pi}\sqrt{\alpha}, \tag{5.19}$$

where $f_s = 1/T_s$ corresponds to the sample frequency. These resonant loop gain poles will lead to zeros in the closed loop NTF. The position of these zeros can be controlled by selecting an appropriate value of α.

An architecture for a MASH $\Delta\Sigma$ modulator with optimized zeros is shown in Fig. 5.9. It consists of a first stage, which is a first-order modulator, built around the integrator $H_1(s)$. This first stage has a discrete time output signal $y_1[n]$. The quantization error $q_1(t)$ of this first stage is fed into the second stage, which is also a first-order modulator (built around the integrator $H_2(s)$). The output signal of this second stage is $y_2[n]$. Then, the overall output $y[n]$ is obtained by combining the signals $y_1[n]$ and $y_2[n]$ through noise cancellation filters (NCF_1 and NCF_2). To control the NTF zeros, we have to add an extra feedback branch α over the two different stages. This is inspired by the single loop structure of Fig. 5.8 and has some similarity to the technique of [109]. Let us now analyze this in more detail. First, we have the integrator transfers $\mathrm{H}_1(s)$ and $\mathrm{H}_2(s)$:

$$\mathrm{H}_1(s) = \mathrm{H}_2(s) = \frac{1}{s \cdot T_{\mathrm{s}}}, \tag{5.20}$$

where T_{s} is the sampling period. Then, the output signals of both stages can we written as:

$$\begin{aligned} Y_1(z) &\approx X^*(s) + \left(1 - z^{-1}\right) Q_1^*(s) - \alpha Q_2^*(s), \\ Y_2(z) &\approx Q_1^*(s) + \left(1 - z^{-1}\right) Q_2^*(s), \end{aligned} \tag{5.21}$$

where $(\cdot)^*$ indicates sampling as defined in [32]. The equation is only an approximation because, the signal transfer filtering is neglected, which is a reasonable approximation if the oversampling factor is sufficiently high. If we select proper

NCFs, we will be able to remove the quantization error from the first stage and shape the quantization error from the second stage with zeros at arbitrary frequencies. A good choice of the NCFs is:

$$\mathrm{NCF}_1 = 1 \qquad \mathrm{NCF}_2 = 1 - z^{-1}. \tag{5.22}$$

With this choice of the NCFs, the output signal $y[n]$ can be written as:

$$\begin{aligned} Y(z) = \mathrm{NCF}_1 \cdot Y_1(z) - \mathrm{NCF}_2 \cdot Y_2(z) = \\ X(z) - Q_2(z) \underbrace{\left[(1+\alpha) - 2z^{-1} + z^{-2}\right]}_{\mathrm{NTF}} \end{aligned} \tag{5.23}$$

Note that in this expression the sampled signals, such as e.g. $X^*(s)$, are transferred to the Z-domain and hence written as e.g. $X(z)$.

According to (5.23), the final output signal Y is composed of a (desired) contribution of the input signal X and a contribution of the second stage quantization noise Q_2, which is filtered by the overall NTF. However the zeros of the NTF are not at DC, instead they are at a frequency that is controlled by the value of α, see (5.19). Hence this freedom can be exploited to achieve improved noise shaping. A side comment here is that the zero is not exactly on the unit circle. However if the oversampling ratio is sufficiently large (i.e. $\alpha \ll 1$), this is not a significant disadvantage.

5.2.2 VCO-based 1-1 MASH with optimized NTF zeros

The architecture described in the previous section has the interesting property that both stages are first-order. As will become clear below, this enables a relatively simple transformation toward a VCO-based structure. Let us now construct an equivalent VCO-based structure of the MASH shown in Fig. 5.9. For this, the VCO will follow (2.19) and the input signal will be dimensionless and will belong to the range [-1,1].

According to the PFM interpretation, the output signal y of a first-order VCO-based ADC stage with an input signal x can be written as:

$$Y(z) \approx [X(s)]^* + \left(1 - z^{-1}\right) \cdot E_{\mathrm{al}}(z), \tag{5.24}$$

where $E_{\mathrm{al}}(z)$ corresponds to the aliasing error. It was shown that the output signal $e(t)$ of the error estimator circuit (top box of Fig. 5.3) provides a good estimation of the baseband component of the sampling error $e_{\mathrm{al}}(t)$. This way, this signal can be used as the input of a second stage to construct the MASH VCO-based ADC already described in the previous section. Note that the proposed technique can be applied to VCO-based ADCs with multiple VCO phases (as is the case for ring oscillators based VCOs). This is also the case for the improved solution described below.

The proposed solution is shown in Fig. 5.10. It consists of adding the overall feedback coefficient α to the MASH concept proposed before. If we use the same

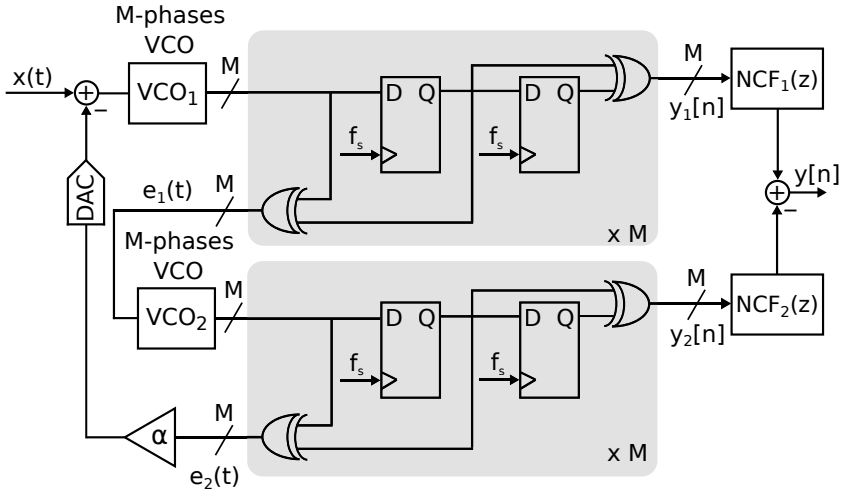


Figure 5.10: 1-1 MASH VCO-based ADC with control over the NTF zeros.

noise cancellation filters as (5.22), we will obtain:

$$Y(z) \approx [X(s)]^* + \left(1 + \alpha - 2z^{-1} + z^{-2}\right) \cdot E_{2,\mathrm{al}}(z), \tag{5.25}$$

where $E_{2,\mathrm{al}}(z)$ represents the aliasing error from the second stage. Clearly this is very similar to (5.23), and hence this structure is expected to have similar behavior.

A behavioral model of the architecture of Fig. 5.10 was simulated to verify the performance predicted by the previous equations. Fig. 5.11 shows a typical simulation result. For the simulation the number of VCO phases (M) is equal to 15, the OSR is 64 and the input signal is a -6 dBFS input sinusoidal at $f_s/1000$. The oscillation parameters of the VCOs are $f_{\mathrm{o},1} = f_{\mathrm{o},2} = f_{\mathrm{s}}/8$ and $K_{\mathrm{VCO},1} = K_{\mathrm{VCO},2} = f_{\mathrm{s}}/8$. The coefficients of the NCFs are set for these gain coefficients. Clearly, the spectrum is second-order noise-shaped with two conjugate zeros placed at $f_{\mathrm{N}}/BW = 1/\sqrt{3}$, which is the optimal location according to [108]. The corresponding SNDR equals 88 dB. From the plot we can also see that the notch does not really go infinitely deep (due to the fact that the NTF zero is not exactly on the unit circle), but this does not significantly affect the performance. The same simulation was also performed without the extra feedback path (i.e. the conventional MASH structure) and with the same parameters. The obtained SNDR was 84.6 dB, which matches the theoretically expected SNDR difference [108], resulting in a SNDR improvement of 3.4 dB.

5.2.3 1-1-1 continuous-time MASH modulator with optimized NTF zeros

Now we will extend the approach to the third order case. Just as before we will first propose a conventional continuous-time modulator and then transform it into a VCO-ADC.

As in Fig. 5.8, we will use a feedback branch over two stages to shift the NTF

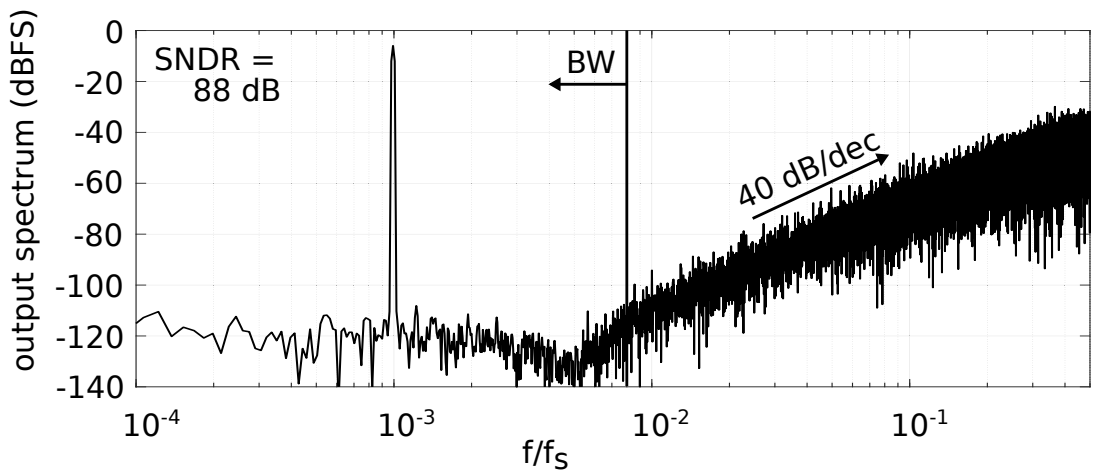


Figure 5.11: Behavioral simulation of the 1-1 MASH VCO-ADC with optimized NTF zeros.

zeros to a desired frequency. For the third order case, we need a zero at DC and a pair of conjugate zeros at a controllable frequency. The proposed architecture for this is shown in Fig. 5.12. Similarly to the architecture of Fig. 5.9, the input signal $x(t)$ is connected to the first stage and the rest of the stages are fed by the quantization error signal from the previous stage. In addition, there is an extra branch that feeds the quantization error from the first stage $q_1(t)$ into the third stage with a gain G. According to [110], this is required to get a continuous-time system that matches exactly with the equivalent discrete-time system which the continuous one derives from. The shift of the zeros, is achieved by a local feedback around the second and the third stage through the coupling coefficient α. The final output signal $y[n]$ is obtained by combining the output signals from all the stages through the appropriate NCFs. For integrator coefficients according to (5.20), the appropriate NCFs are the following:

$$\mathrm{NCF}_1 = 1 \quad \mathrm{NCF}_2 = 1 - z^{-1} \quad \mathrm{NCF}_3 = \left(1 - z^{-1}\right)^2. \tag{5.26}$$

Then, the overall output signal can be written as:

$$\begin{aligned} Y(z) &= \mathrm{NCF}_1 \cdot Y_1(z) - \mathrm{NCF}_2 \cdot Y_2(z) + \mathrm{NCF}_3 \cdot Y_3(z) \\ &\approx X(z) + \\ &\quad Q_3(z)\left(1 - z^{-1}\right)\left(1 + \alpha - 2z^{-1} + z^{-2}\right). \end{aligned} \tag{5.27}$$

The quantization errors from the first and the second stage are canceled, and the quantization error from the third stage is high-pass filtered with one zero at DC and a conjugate pair of zeros at a frequency controlled by the value of α.

5.2.4 VCO-based 1-1-1 MASH with optimized NTF zeros

Now, we will again transform the 1-1-1 continuous-time MASH architecture into a structure with only VCOs. In this section, we will keep the same nomenclature and considerations for the input signal and the VCO oscillation parameters as

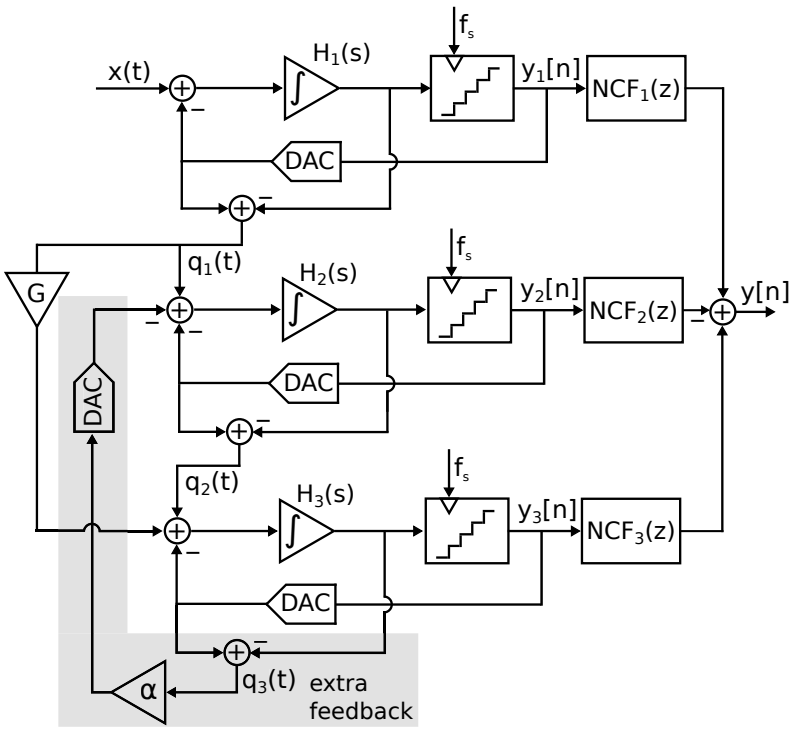


Figure 5.12: 1-1-1 continuous-time MASH modulator with control of the NTF zeros.

before.

The result of the transformation is shown in Fig. 5.13. If we use the NCFs proposed in (5.26), the output data will be expressed as follows:

$$Y(z) \approx [X(s)]^* + E_{3,\mathrm{al}}(z)\left(1-z^{-1}\right)\left(1+\alpha-2z^{-1}+z^{-2}\right), \tag{5.28}$$

where $E_{3,\mathrm{al}}(z)$ represents the aliasing error from the third stage. Similarly to the continuous-time case, only the quantization error from the third stage appears at the output with one zero at DC and a conjugate pair of zeros at an arbitrary frequency.

Again a behavioral model of the architecture of Fig. 5.13 was built and simulated. Fig. 5.14 shows a typical simulation result. Here the value of α was set to obtain an NTF notch at $f_\mathrm{N}/BW = \sqrt{3/5}$ according to [108] with the purpose of optimizing the resulting SNDR. All the simulation parameters remain as in Fig. 5.11. The oscillation parameters of the VCOs are $f_{\mathrm{o},1} = f_{\mathrm{o},2} = f_{\mathrm{o},3} = f_\mathrm{s}/8$, and $K_{\mathrm{VCO},1} = K_{\mathrm{VCO},2} = K_{\mathrm{VCO},3} = f_\mathrm{s}/8$. The resulting SNDR equals 107.5 dB.

The figure clearly exhibits the desired notch in the spectrum. Also the correct out-of band roll off of 60 dB/decade can be observed. The architecture was also simulated without the extra feedback. In this case, we have a third-order noise shaped structure whose NTF has three zeros at DC. The resulting SNDR was 100 dB. Hence, the optimization of the zeros takes us to a SNDR enhancement of 7.5 dB, which approximately corresponds to the prediction of [108].

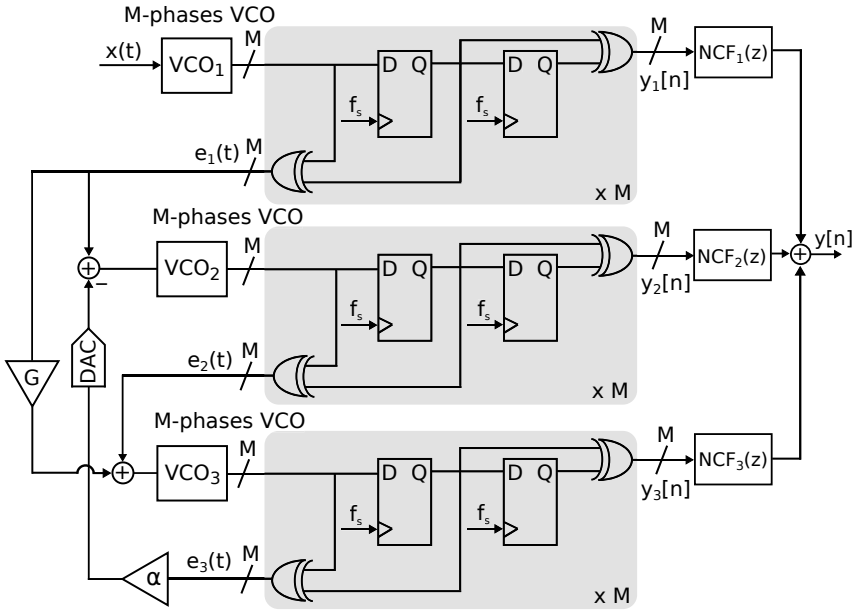


Figure 5.13: 1-1-1 MASH VCO-based ADC with control over the NTF zeros.

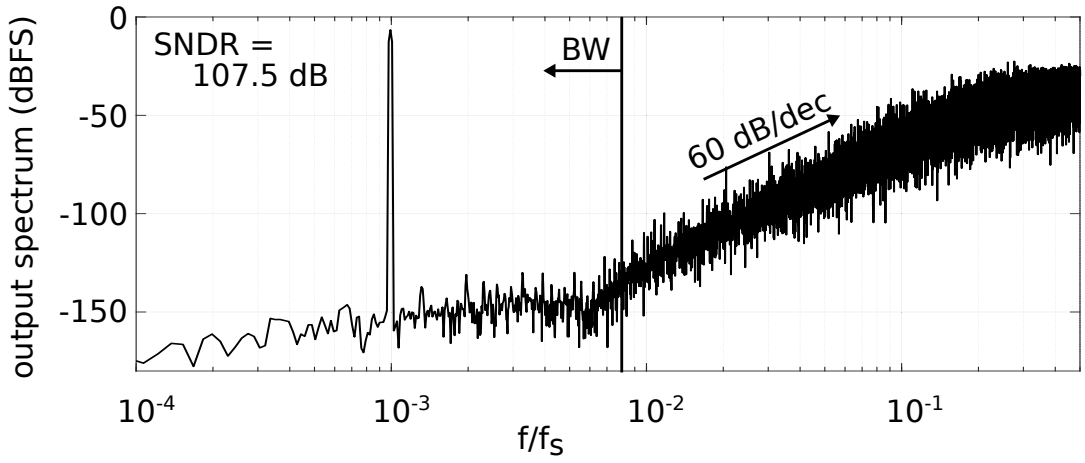


Figure 5.14: Behavioral simulation of the 3rd-order MASH VCO-ADC.

5.2.5 Conclusion

We have proposed a new approach to control the position of the NTF zeros in continuous-time cascaded (MASH) $\Delta\Sigma$ modulators. This enables placement of the zeros at optimal locations in the signal band, which allows to achieve improved performance. An important aspect of this approach is that every stage in the cascade is first order only. This enabling element allowed us to make the important extension of our technique to MASH VCO-ADCs, making use of the PFM interpretation. The technique was elaborated both for the case of a second-order as well as a third-order MASH VCO-ADC. Simulation results are presented and confirm the validity of the technique.

5.3 Extension of the VCO-based structure with digital precoder to a MASH architecture

The digital precoding technique proposed in the previous chapter (Fig. 4.5(a)) can be also extended to the implementation of VCO-based MASH architectures. The way of making the connection between stages was deeply explained in [97] using the model of a VCO as a phase integrator. Just to provide an example to the reader about how our digital-precoded system can be used to implement MASH architectures, we will build a second order MASH structure with the system of Fig. 4.5(a).

Fig. 5.15(a) depicts the diagram of a MASH architecture where the first stage is digital precoded. As can be observed, the connection between the stages is different from the VCO-based MASH architectures proposed in this chapter. This is due to the front-end digital modulator, which requires a different way of estimating the quantization error [97]. Note that, whereas we fix the linearity of the first oscillator with the help of the pulse width modulator, the input of the second oscillator is digital too, so that it also works linearly. Similarly to Fig. 5.1, the outputs $y_1[n]$ and $y_2[n]$ must combined through NCFs, which in this case correspond to (5.8).

To validate the approach, Fig. 5.15(b) shows a behavioral simulation of the system of Fig. 5.15(a). Both GROs oscillate at $f_s/2$, $f_c = f_s/2$ with f_s =1.5 GHz. We used a -6 dBFS sinusoidal input signal with 20 MHz BW. The resulting SNDR equals 80 dB and second-order noise-shaping is clearly visible.

This MASH structure has not been analyzed with the PFM-based theory developed in Chapter 3. Consequently, we are not able to provide more details about the challenges that might imply its implementation. The goal of this section is only providing a first approach of how the first order system of Fig. 4.5(a) could be extended to a second order MASH architecture based on the theory proposed in [97].

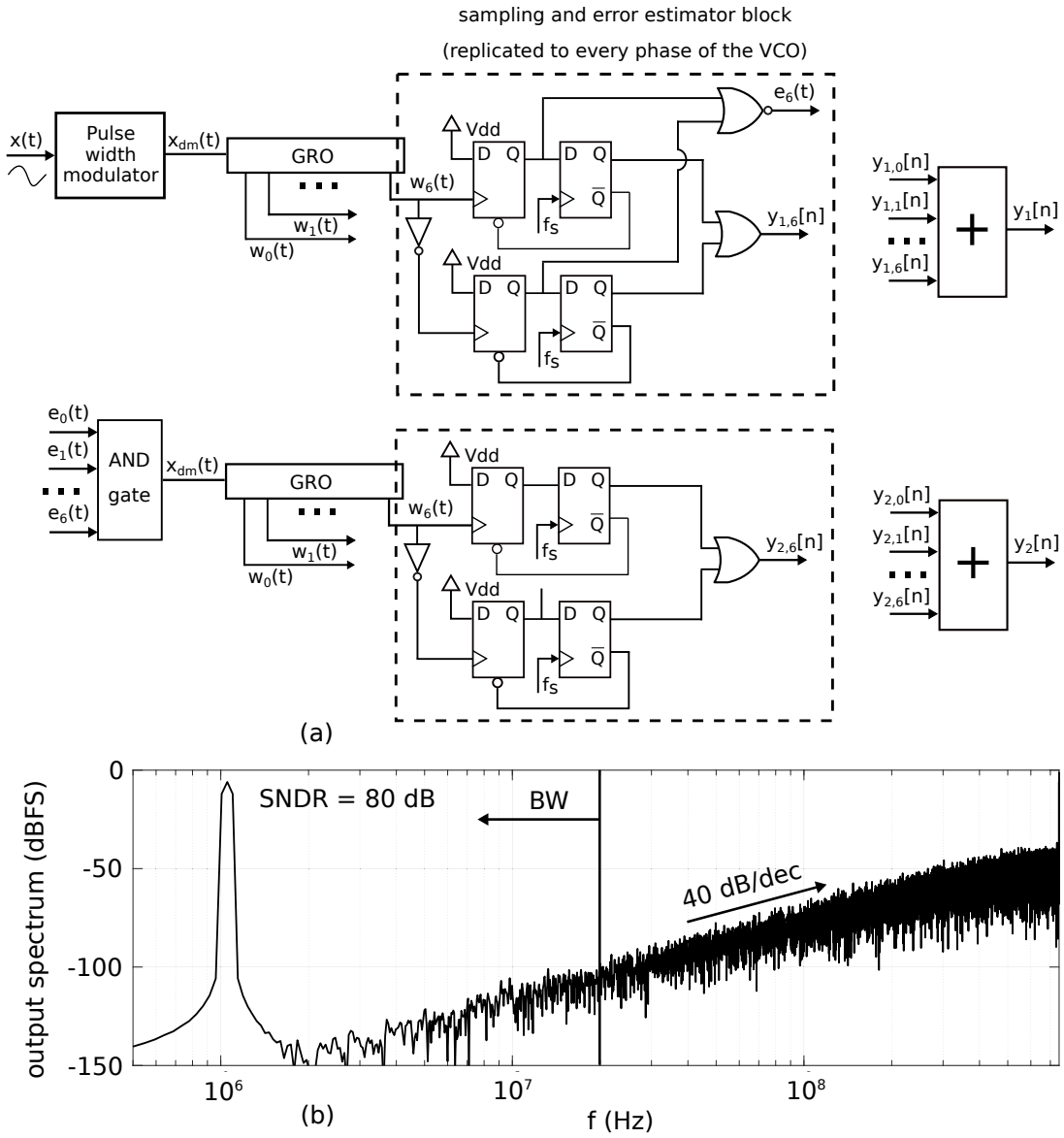


Figure 5.15: (a) Block diagram of the proposed architecture, and (b) behavioral simulation.

Part III

Experimental results

Chapter 6

Chip I: VCO-based ADC with digital precoding

One of the experimental prototypes implemented in collaboration with Intel Austria GmbH corresponds to the architecture described in Section 4.1, which is a VCO-based ADC with a front-end pulse width modulator. The architecture was implemented in a 40-nm CMOS process with 1.1 V supply voltage. We will describe the circuitry of the system and will show the measured performance from the experimental chip. As the chip arises from a collaboration with Intel Austria GmbH, there are some parts of the circuit that were designed within this company. Due to intellectual property issues, we will not describe them in detail.

In summary, the prototype shows a measured performance of a potential 20 MHz BW SNDR peak equal to 56 dB. However, we will show that the practical SNDR is highly limited due to noise issues that should be solved in potential future redesigns. The power consumption is 2.15 mW and the occupied area is 0.03 mm^2. The designed architecture is well-suited for medium-resolution and high-bandwidth applications.

6.1 Implementation details

The implemented architecture follows the diagram depicted in Fig. 4.5(a), but in a pseudo-differential architecture, which means that the whole system is composed of two identical branches of Fig. 4.5(a). These branches work in parallel, as depicted in Fig. 6.1(a), where $x_{\mathrm{p}}(t)$ and $x_{\mathrm{n}}(t)$ are the complementary input signals of the P-side and the N-side respectively. Just to remember the architecture, we use a synchronous naturally sampled pulse width modulator that we connect to a GRO composed of seven phases. Then, each phase is sampled and firstly differentiated to demodulate the data. Finally, the signals from the phases are combined into a multibit signal that represents the output data. It is important to remember that we use a synchronous and natural pulse width modulator to mitigate the degradation of the performance due to the sideband modulation components that might fall into the band of interest. Even so, we showed that the system is still very sensitive to this phenomenon.

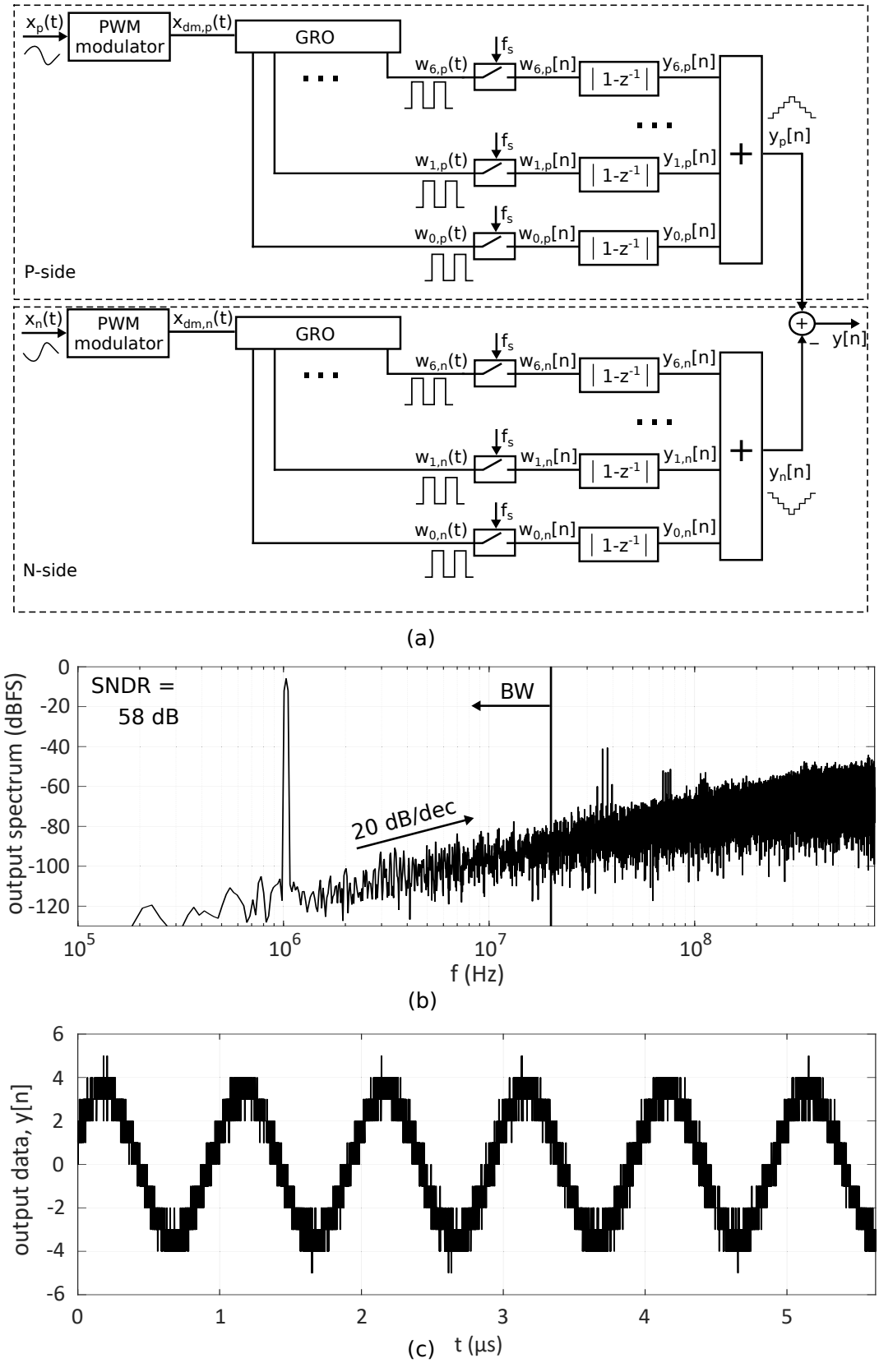


Figure 6.1: (a) Pseudo-differential architecture of the implemented VCO-based ADC with pulse width modulation precoder, (b) reference behavioral simulation, and (c) output data versus time.

Fig. 6.1(b) shows the ideal behavioral simulation that we take as the reference for the practical prototype. The resulting SNDR is 58 dB for the pseudo-differential architecture considering a bandwidth of 20 MHz. The sampling frequency is 1.5 GHz and the input signal is a sinusoidal wave of -6 dBFS at 1 MHz. Fig. 6.1(c) shows the output data resulted in the simulation of Fig. 6.1(b).

The implementation of the circuit is depicted in Fig. 6.2, where the pseudo-differential architecture is clearly visible. In the following subsections, we will describe each of the circuit blocks that compose the architecture.

6.1.1 Pulse width modulator

The schematic of the overall complementary pulse width modulator is depicted in Fig. 6.2. It is composed of a ramp generator and two asynchronous comparators. The input of the ramp generator is the signal clock (with an oscillation frequency that depends on the digital frequency divider). Previously to the ramp generator, we placed a programmable digital frequency divider in order to be able to choose between different carrier frequencies. The ramp generator integrates the clock signal, injecting current into the capacitor C_{L} when the clock signal is a logic '1' and subtracting current from it when the clock signal is a logic '0'. This way, the output signal $w(t)$ is a triangular wave with the same oscillation frequency as the input signal. $V_{\mathrm{bias,p}}$, $V_{\mathrm{bias,n}}$ and C_{L} control the amplitude of the triangular wave, which must match with the full-scale amplitude of the converter input signal. The output of the ramp generator is connected to two identical asynchronous comparators which make the comparison between the triangular wave and the two complementary input signals: $x_{\mathrm{p}}(t)$ and $x_{\mathrm{n}}(t)$. The differential output of both comparators are pulse width modulated signals that are connected to the GROs.

The pulse width modulator circuit was totally designed and provided by Intel Austria GmbH. That's the reason why we will not go into more details about the circuit implementation.

A very important specification required in the pulse width modulator is the linearity of the circuit. As we are dealing with an open-loop architecture, non-linearity in the pulse width modulator is not compensated and might degrade the performance of the converter (similar to the VCO non-linearity of Fig. 2.10(a)). Accordingly, digital precoding is a proper way to fix VCO non-linearity, as long as we are able to design a digital precoder with good linearity properties, which might be challenging. In order to check this, the distortion of the pulse width modulator was measured by simulation. The results are shown in Fig. 6.3. It can be seen that the HD3 equals 46 dB for a -6 dBFS sinusoidal input wave, which strongly restricts the converter performance if we take into account the behavioral simulation of Fig. 6.1(b). In Fig. 6.3 the carrier frequency equals 1 GHz. However, in the chip, the carrier frequency was set to 750 MHz, therefore we might expect a slight linearity improvement in the experimental measurements.

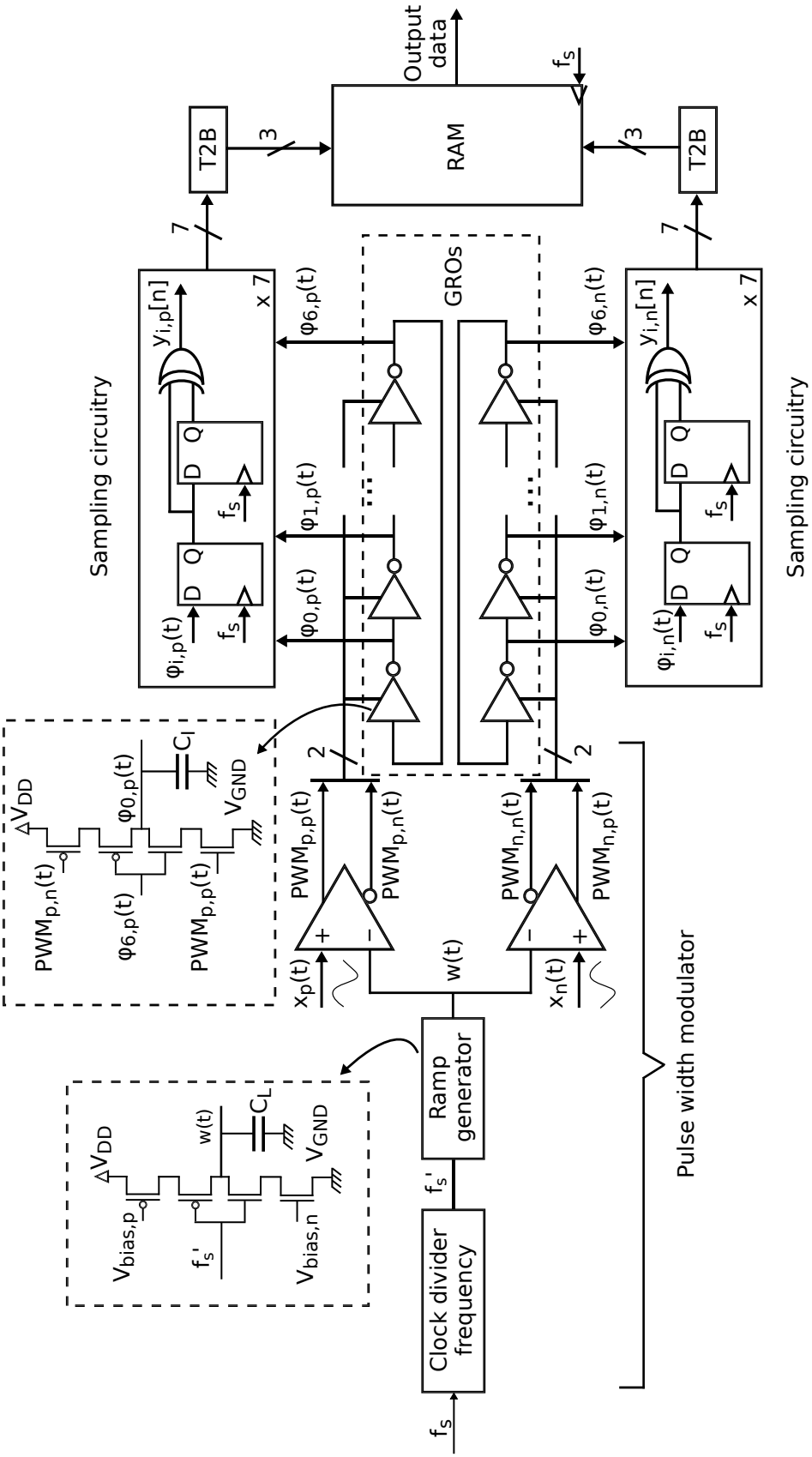


Figure 6.2: VCO-based ADC with digital precoding implemented in the chip.

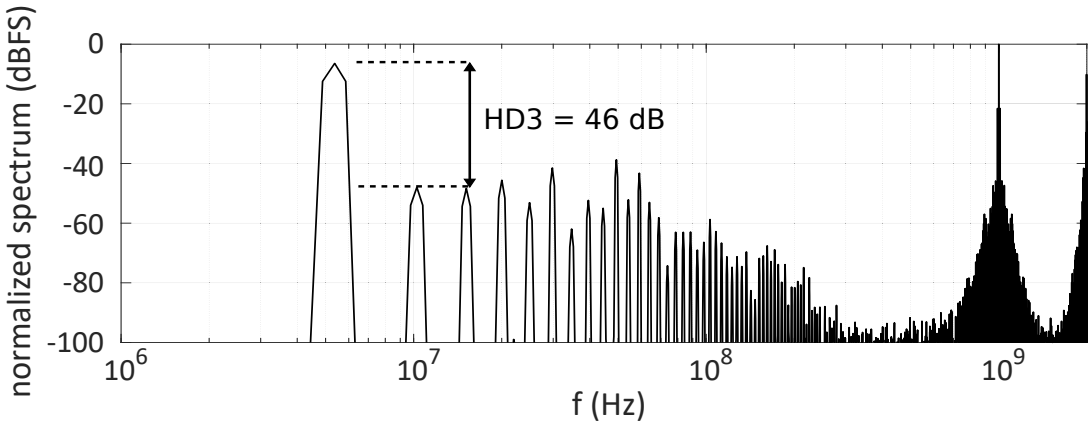


Figure 6.3: Pulse width modulator distortion measured by simulation.

6.1.2 GRO

Each GRO is composed of seven inverters connected in a ring configuration. Fig. 6.2 shows the structure of each inverter. The inverters show the conventional structure of a CMOS inverter [27], but adding two complementary switches between V_{DD} and the P-type metal-oxide-semiconductor (PMOS) transistor, and between V_{GND} and the N-type metal-oxide-semiconductor (NMOS) transistor (this configuration is called starved inverter). The pulse width modulated signal that comes from the comparator is connected to these switches. If the switches are closed, oscillation will be enabled. Conversely, if the switches are opened, the inverter will not be able to charge or discharge the output capacitor C_{I}, so that the output voltage (that represents the phase of the oscillator) will remain. The oscillation frequency depends on how fast we are able to charge and discharge the output capacitor, which directly depends on the current provided by the inverter and the output capacitor. With the goal of tuning the oscillation frequency, a set of programmable capacitors were placed at the output of the inverters. The nominal oscillation frequency of the GRO is approximately 750 MHz.

6.1.3 Digital logic

The sampling circuitry (Fig. 6.2) implemented in the chip is the conventional XOR-based circuit used to demodulate and sample the VCO output signal [41]. Once sampled, the data are encoded in thermometric code. These data are turned into binary code through a conventional thermometer-to-binary encoder (T2B) with the goal of minimizing the number of output bits. Both the sampling circuitry and the T2B are built with the standard CMOS 40-nm digital library. Then, the binary data are stored on an first-in first-out (FIFO) random access memory (RAM) that allows us to access them at a lower rate through a serial interface. Finally, they are processed on a computer.

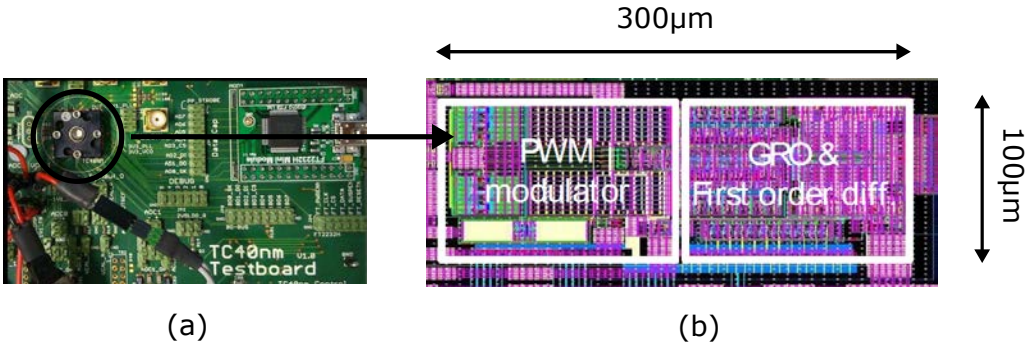


Figure 6.4: Test fixture: (a) PCB, and (b) layout of the circuit.

6.2 Experimental results

The proposed architecture was manufactured and its performance was measured. The PCB and layout photo are shown in Fig. 6.4 (die photo is not shown due to intellectual property restriction issues). The core area is only 0.03 mm^2, including the programmable capacitors and frequency divider of the ramp generator. Apart from the serial interface from we read the data, an output port where the oscillation frequency of both GROs can be observed was also available. As the oscillation frequency was programmable, we were able to tune it thanks to this output port.

As can be appreciated, in this chip, we added circuits to tune the carrier frequency of the pulse width modulator and the oscillation frequency of the GRO. These circuits were added with the goal of mitigating the effects of the sideband components that fall in-band and avoid effects similar to those shown in Fig. 4.3(c).

Fig. 6.5 shows the most representative performance measurements. The system was tested using a sampling frequency $f_s = 1.52$ GHz and a carrier frequency equal to 751 MHz ($f_s/2$). The oscillation frequency of the GROs had been tuned until the best performance was found. Fig. 6.5(a) shows the idle channel of the output data when there is input (only the DC component). If we considered the power of a full-scale input signal, we would get a 20 MHz BW SNDR peak equal to 56 dB, which is consistent with the SNDR value predicted in Fig. 6.1(b). We can also see that the floor noise level is around -80 dBFS. In Fig. 6.5(b), a 3 MHz -20 dBFS sinusoidal wave is used as the input signal. The resulting SNDR is 34.4 dB. Similar measurement was made in Fig. 6.5(c), but now with a 18 MHz sinusoidal input signal (close to the edge of the band of interest). The SNDR is 35.6 dB, very similar to the SNDR of Fig. 6.5(b). Finally, Fig. 6.5(d) shows the output spectrum with a 3 MHz -8 dBFS sinusoidal input signal, with a SNDR equal to 42.5 dB. If we compare Fig.6.5(d) to Fig.6.5(b), we may notice one of the main problems of the architecture. To go from Fig.6.5(b) to Fig.6.5(d), we increased the input power 10 dB. It can be appreciated the the power of the floor noise has been increased. If we keep increasing the input amplitude, this noise will keep going up and the resolution will be strongly degraded. The reason why we observe this behavior is mainly attributed to the GRO. When dealing with

high amplitude signals, the pulse width modulated signal will contain narrow digital pulses if the input signal is close the full-scale amplitude. If the GRO is not fast enough to react properly to this pulses, the phase coherence will be lost, resulting in noise increase. Finally, in Fig. 6.5(d) we can appreciate the third harmonic component of the input signal, as expected from the simulations made in Fig. 6.3.

Despite we have shown that the performance is degraded by some design problems, we will suppose that the virtual SNDR peak we might have measured with a proper design equals 56 dB (Fig.6.5(a)). Then, the equivalent resolution for a 20 MHz BW equals 9 bits with a power consumption of 2.15 mW with 1.1 V supply voltage. This leads to a Figure of Merit equal to 105 fJ/conversion-step. The performance of the architecture is summarized and compared to other similar architectures in Table 6.1. Whereas our architecture keeps similar power consumption and area in comparison to other equivalent architectures, our design is much simpler. In addition, the design uses a pulse width modulator with a carrier frequency higher than other published designs, which makes it fit well with high bandwidth applications.

6.3 Conclusion

We have described a 40-nm prototype of a VCO-based ADC architecture with digital precoding. The proposed open-loop architecture shows first-order noise shaping in the output spectrum and alleviates the VCO non-linearity issue. We have shown that our design is limited by some design constraints that degrades the final performance. Nevertheless, with a sampling frequency of 1.52 GHz, it consumes only 2.15 mW to potentially get 9 ENOB in 20 MHz BW. Due to the open-loop and mostly digital structure, the proposed architecture could be used as the input stage of an all-digital multistage converter (Fig. 5.15) in high bandwidth and low power applications. Compared to other equivalent ADCs, the solution presented is less complex while keeping similar power, area and linearity properties. Neither digital calibration circuits nor feedback structures are used to increase the linearity of the VCO, which makes the architecture simple.

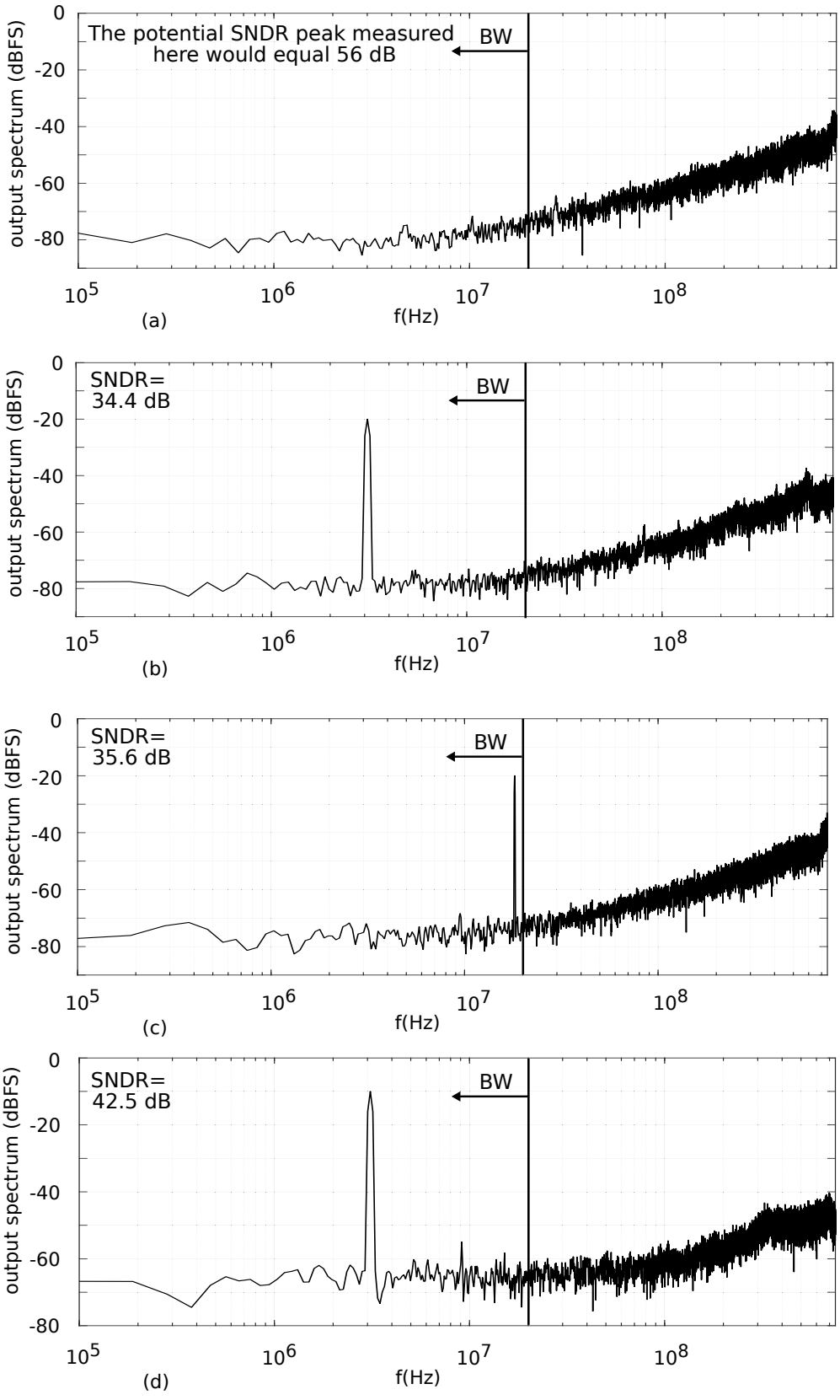


Figure 6.5: Measured output spectra: (a) idle channel, (b) -20 dBFS input signal at 3 MHz, (c) -20 dBFS input signal at 18 MHz, and (d) -10 dBFS input signal at 3 MHz.

Table 6.1: Comparison with related work: VCO-based ADC with digital precoding

	Process (nm)	**BW (MHz)**	**$SNDR_{peak}$ (dB)**	**f_s (MHz)**	**Supply voltage(V)**	**Area (mm^2)**	**Power (mW)**	**FoM (fJ/step)**[a]	**FoM (dB)**[b]
[41]	130	10	63.1	500	1.2	0.078	12.6	-	-
[56]	90	8	59.1	640	-	0.1	4.3	366	-
[61]	65	20	68	1000	1	0.6	8.2	99	162
[62]	40	40	59.5	1600	0.9	0.017	2.57[c]	42	-
[111]	65	30	64	200	1.0	0.023	12.2	154	-
This work	**40**	**20**	**56**	**1520**	**1.1**	**0.03**	**2.15**	**105**	**156**

[a] FoM (fJ/step) = Power/(2·BW·$2^{\frac{SNDR_{peak}-1.76}{6.02}}$).
[b] FoM (dB) = $SNDR_{peak}$ + $10\log_{10}$(BW/Power).
[c] The power of the driving buffer is not included.

Chapter 7

Chip II: PFM-based ADC with active integration

In Chapter 4, we explained why a pulse frequency modulator can be used itself as an ADC and how to extend the single-phase architecture to an efficient multiphase architecture. One of the advantages of this architecture is its inherent linearity, without depending on the delay of an inverter as occurs in ring oscillators. The architecture of Fig. 4.10 with active integration was implemented in a 40-nm CMOS prototype in collaboration with the company Intel Austria GmbH.

In this chapter, we will describe how each of the blocks that compose the architecture were designed and will provide the performance measurements of the chip. To sum up, the prototype shows a measured performance of SNDR peak equal to 53 dB within 20 MHz BW. The power consumption is 3.5 mW and the occupied area is 0.08 mm^2. We will also describe the observed problems of the system that might degrade the ideal performance. Finally, we will compare our architecture to equivalent systems already published in the literature.

7.1 Implementation details

The architecture we propose is a pseudo-differential architecture, where each branch has the structure shown in Fig. 4.10(a). The resulting architecture is shown in Fig. 7.1(a). We described the performance of this structure previously. It is composed, mainly, of a pulse frequency modulator with active integration, and makes use of a delay line to generate several phases that are combined into a multibit output signal. Fig. 7.1(b) depicts the ideal behavioral simulation that we will take as the reference for the measurements. This simulation is the same already shown in Fig. 4.11, but with a pseudo-differential configuration. The sampling frequency is 1 GHz. The input signal is a -3 dBFS sinusoidal waveform at 1 MHz. The SNDR equals 61 dB in 20 MHz BW. Finally, Fig. 7.1(c) shows the time representation of the output data of the simulation depicted in Fig. 7.1(b).

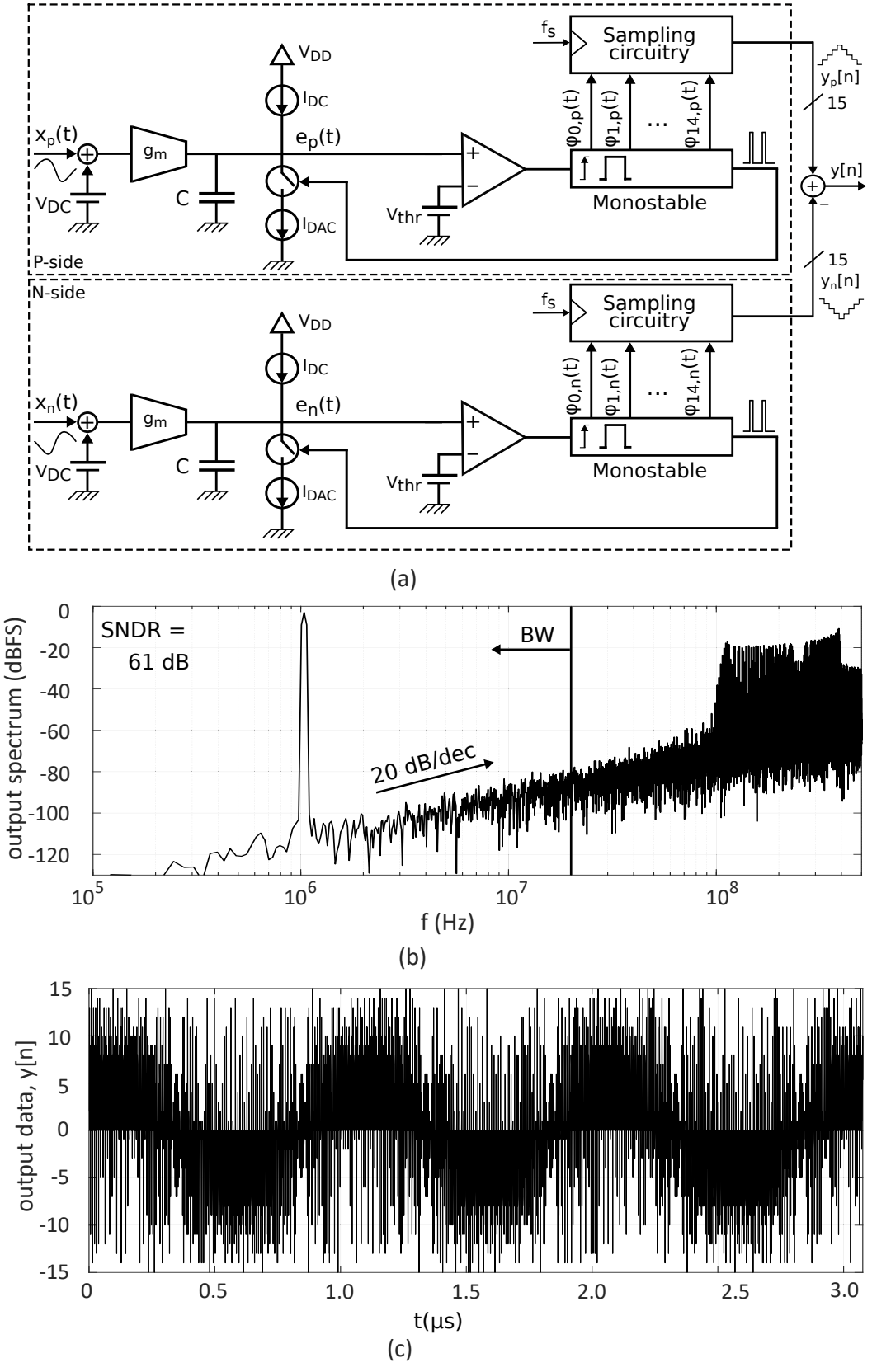


Figure 7.1: (a) Proposed architecture to be implemented on silicon, (b) behavioral simulation of the proposed architecture, and (c) output data versus time.

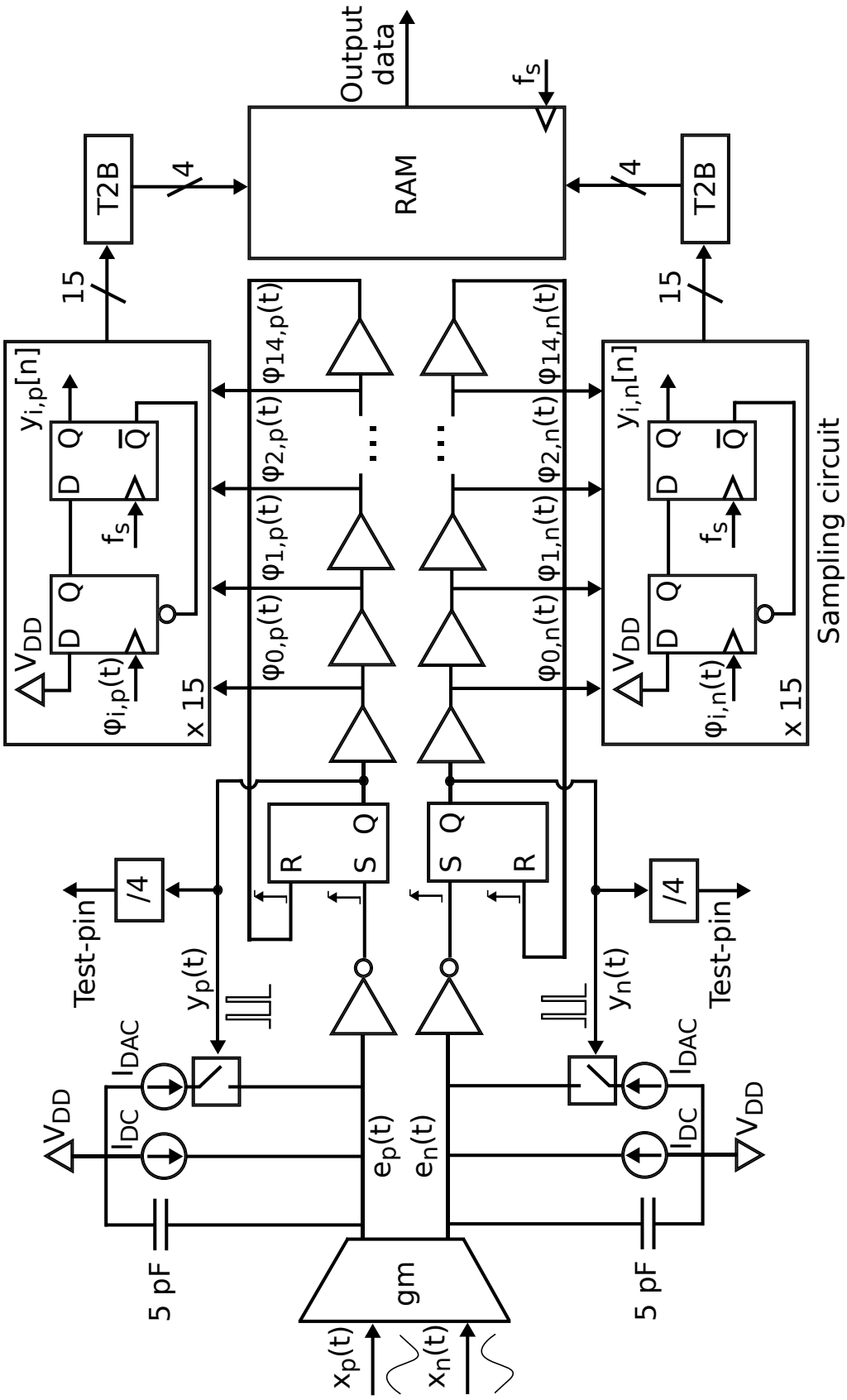


Figure 7.2: PFM-based ADC circuit implemented in the chip.

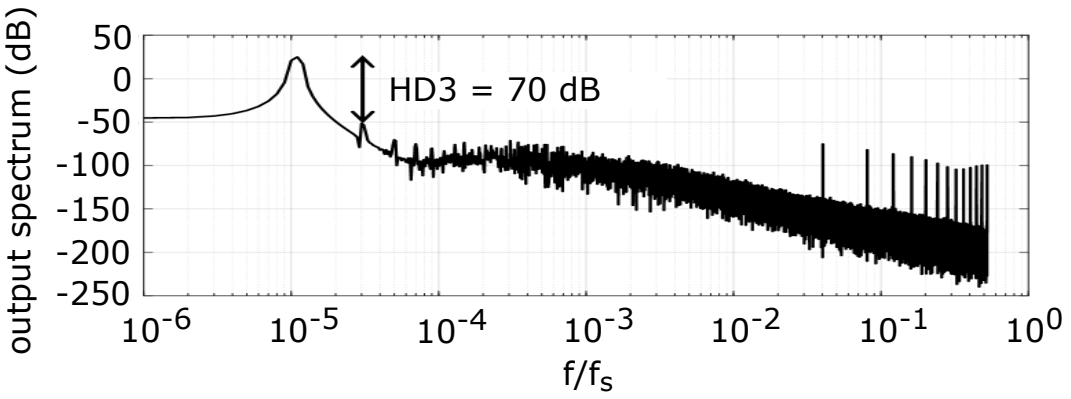


Figure 7.3: Transconductance distortion measured by simulation.

The circuit implemented in the chip is depicted in Fig. 7.2. The block diagram uses a fully differential input stage that drives two oscillators encoding the input signal. These two oscillators correspond to both sides of the pseudo-differential structure, the P-side and the N-side. Two 5-pF capacitors are used to perform a current integration. The current integration is split up into two paths: the input signal and the feedback pulse (as in Fig. 4.10). On the one hand, the differential input voltage is converted into a differential current by means of a transconductance g_{m}. On the other hand, the integration of the feedback pulse is implemented by means of a single-bit current DAC. The comparator output triggers a monostable composed of a rising-edge triggered set-reset flip-flop and a chain of 15 digital buffers. Finally, each output of the digital buffers is sampled and post-processed. The supply voltage equals 1.1 V.

In the following subsections, we will describe in detail each of the circuit blocks that compose the architecture.

7.1.1 Bulk-driven transconductance

The circuit employed for the transconductance is a bulk-driven degenerated differential pair structure. As can be observed in Fig. 7.2, the transconductor is placed in an open-loop configuration. Consequently, the associated distortion will not be compensated by any loop and might degrade the final SNDR. Therefore, a highly linear architecture is required to keep the distortion components below the in-band quantization noise level. It is known that bulk-driven circuits are especially suitable for low voltage designs [112–114]. First of all, the threshold voltage requirements are removed. In addition, the transconductance of a bulk-driven metal-oxide-semiconductor field-effect transistor (MOSFET) is lower than its gate-driven equivalent. Our design benefits from these two facts because they enable a full swing of the input signal without degrading the linearity. The simplified transconductance circuit is shown on Fig. 7.4(a), together with the sizes of transistors. It is based on the conventional degenerated differential-pair, but connecting the differential input signal to the bulk terminals of the front-end MOSFETs. The gate terminals of the differential pair are connected to a suitable common mode voltage to maintain the desired bias current.

According to circuit simulations, the transconductance shows 70 dB HD3 with a resistor R_{gm} of only 600 Ω and a full scale differential input of 0.6 V_{pp}. This harmonic distortion level is good enough to accomplish with the system level requirements established in accordance with behavioral simulations. This simulation is depicted in Fig. 7.3, where a low-pass filter is applied to the differential output current of the transconductance to measure the distortion and avoid aliasing when sampling.

7.1.2 Bias current source and current DAC

In parallel with the capacitor, a bias current source (I_{DC}) and a single-bit asynchronous current DAC (I_{DAC}) are placed in each side of the pseudo-differential structure. Whereas the purpose of the bias current source is controlling the rest oscillation frequency, the purpose of the current DAC is injecting a current pulse into the capacitor to integrate the monostable output signal. The monostable output is always a return-to-zero pulse with constant duration. Therefore, the current injected into the capacitor depends only on the pulse width and not on its actual shape, which attenuates the influence of unequal rise and fall times. This feature eases the design of this part of the circuit because the current DAC can be implemented with a current source followed by a switch, which is enabled or disabled by the monostable output. A synchronization clock is not required. In Fig. 7.4(b) we can observe the circuit of the bias current source and in Fig. 7.4(c) the circuit of the DAC, together with the sizes of the transistors.

With regard to the bias current source, it follows the conventional current source structure with a branch that mirrors the current from a reference circuit [27] and injects it continuously into the capacitor. Similarly, in the case of the current DAC, we have also a current mirror to copy the current from a current reference circuit. Nevertheless, the circuit for the current DAC is more complex. Here, we use a digital switch to make the current flow into the capacitor or not. When the current is not flowing through the capacitor, it flows through a dummy resistor R_{DAC}. This way, we keep transistors M_7 and M_8 always biased and we mitigate ringing phenomena in the output current.

7.1.3 Comparator

The circuit for the asynchronous comparator is composed of a cascade of digital inverters. As the rest oscillation frequency of the loop is on the order of hundreds of MHz, the comparator delay must be very low. The maximum capacitor voltage is of 30 mV only. Consequently, a high-gain and high-speed inverter architecture is required, at least for the first inverter. The comparator is therefore implemented with a first current-controlled NMOS-based inverter followed by two standard CMOS inverters. V_{thr} is the switching voltage of the first inverter. The output of this structure is already a digital signal that triggers the monostable. The circuit of the comparator is shown in Fig. 7.5(a).

The specifications of this comparator are extremely important to get a good performance in the architecture. The voltage swing at the input of the comparator is very low, so we can consider that the first inverter of the comparator works as an

amplifier. The features of this inverter will determine the best performance that can be achieved in the converter. Nominally, the highest oscillation frequency in the loop is about 500 MHz, so we need to keep high gain within this range of frequency. High speed inverters are built with high current bias flowing through the inverters, which increases the power consumption. We will see later on that, in terms of power consumption, the comparator is the main contributor and the main element to be enhanced in future designs.

7.1.4 Monostable and digital logic

The design of the monostable and the digital logic (in the digital logic we include the sampling and the post-processing circuitry) is based on the standard 40-nm CMOS digital library.

The monostable is composed of a rising-edge triggered set-reset flip-flop followed by a chain of buffers implemented with inverters. This chain of buffers is used to generate the digital pulse that is fed back into the integrating capacitor. At the same time, we use the connection between one buffer and the next one to sample the signal and generate a multibit output data. Fig. 7.5(b) depicts the schematic of the monostable.

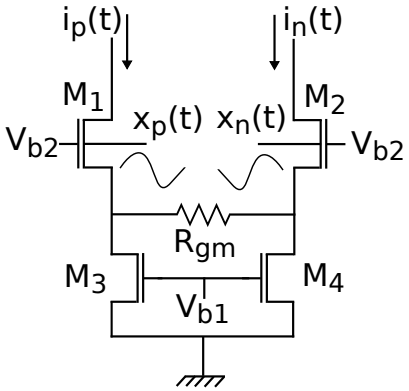
With respect to the sampling circuit, we may notice that it is not the conventional sampling architecture used for VCO-based ADCs implemented with XOR gates [41]. We require the sampled pulse to be equal to the sampling period, regardless of the actual length of the square pulse generated by the monostable. The proposed sampling circuit of Fig. 7.2 is a 1-bit counter with asynchronous reset, that counts up with the rising edges of the phases of the monostable $\varphi_{\mathrm{i}}(\mathrm{t})$ and is cleared each rising edge of the clock signal. This way, we make sure that every pulse is translated to each output with only one sample at logic '1' avoiding data replication.

The sampled data are encoded in thermometric code. Then, these data are introduced into a conventional thermometer to binary encoder (T2B) to minimize the number of output bits. Finally, the output data stream is stored on an FIFO RAM, from where data can be read at lower rate through a serial interface.

7.1.5 LDO and circuit references

Above we have described the elements that compose the PFM-based ADC we have implemented in the chip. However, we have also some extra circuitry that does not belong to the ADC core but is required to make the circuit work.

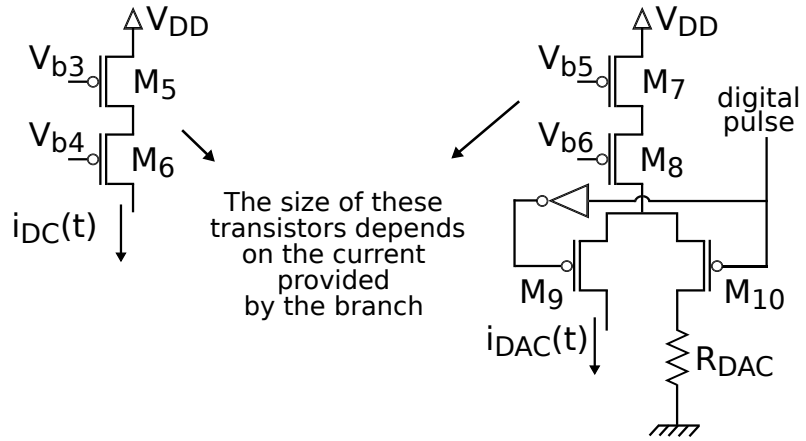
The chip was implemented in a multi-project test-chip sharing the silicon with another projects of Intel Austria GmbH. Consequently, there was a central core used to provide all the voltage and current references to the different circuits implemented in the chip. In our case, only current references were required. This central core was completely designed by our partners and we did not take part on it.



(a)

	W / L
M_1 , M_2	27.5µm / 400nm
M_3 , M_4	134.4µm / 3µm

$R_{gm} = 600\ \Omega$



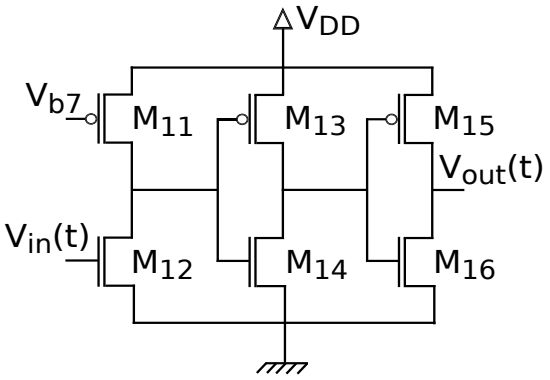
(b)

	W / L
M_9 , M_{10}	3.34µm / 40nm

$R_{DAC} = 1.7k\Omega$

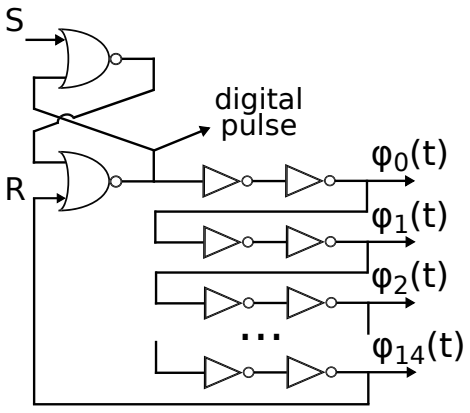
(c)

Figure 7.4: Circuit blocks of the PFM-based ADC: (a) Transconductance, (b) Bias current source, (c) current DAC, (d) comparator, and (e) monostable.



(a)

	W / L
M_{11}	100µm / 80nm
M_{12}	24µm / 80nm
M_{13}	450nm / 40nm
M_{14}	360nm / 40nm
M_{15}	900nm / 40nm
M_{16}	720nm / 40nm



(b)

Figure 7.5: Circuit blocks of the PFM-based ADC: (a) Comparator, (b) monostable.

Furthermore, we used a low-dropout regulator (LDO) placed between the supply voltage and the circuit of the monostable. The purpose of this LDO is filtering the low-frequency noise that comes from the supply sources outside the chip. This LDO was also provided by our partners. We used two LDOs, each of them connected to each side of the pseudo-differential architecture.

7.1.6 Calculation of oscillation parameters

If we calculate f_{osc} in Fig. 7.2, we will get:

$$f_{\mathrm{osc}}(t) = \frac{i_{\mathrm{DC,gm}} - i_{\mathrm{DC}}}{i_{\mathrm{DAC}} \cdot T_{\mathrm{d}}} + \frac{g_{\mathrm{m}}}{i_{\mathrm{DAC}} \cdot T_{\mathrm{d}}} x(t), \tag{7.1}$$

where $i_{\mathrm{DC,gm}}$ is the DC current of the transconductance g_{m}. As can be observed, we have several parameters that can be trimmed to achieve the desired oscillation parameters. With that purpose in mind, we have added some programming logic to both the bias current sources and the current DAC elements, which can be tailored to program f_{o} and K_{VCO}. These elements are composed of several parallel branches (identical to the structures of Fig. 7.4(b) and (c)) that provide different current values and have digital switches with the goal of enabling or disabling them. That's the reason why in Fig. 7.4 we do not provide the size of transistors M_5, M_6, M_7, M_8. The size of these transistors will depend on the current provided in each branch. The supply voltage provided by the LDO is also programmable. This allows us to change the monostable supply voltage to modify the delays of the buffers and the length of the generated pulse T_{d}.

7.2 Experimental results

As stated before, the proposed PFM-based ADC was fabricated using a 40-nm CMOS process in a multi-project test chip in collaboration with Intel Austria GmbH. The 40-nm CMOS technology is featured by a nominal supply voltage equal to 1.1 V and transistors with a nominal threshold voltage equal to 400 mV. Fig. 7.6 shows the die photo of the chip. The PCB used for the text fixture is the same used for the first chip (Fig. 6.4(a)).

The layout is arranged symmetrically along the horizontal axis for the two sides of the pseudo-differential architecture. The occupied area is equal to 550 μm x 290 μm. If we take into consideration only the ADC circuit core without the test interface, the LDO and reference circuits, the occupied area is 0.08 mm^2.

To measure the performance of the chip, we have two possible interface choices. As a first choice, we have a test-pin from where we can observe the oscillation of each PFM-based oscillator. To allow the use of a standard CMOS pad, the pulsed output from the monostable is divided by a factor of four and turned into a 50% duty-cycle square signal. The down-divided signal is captured at high speed using a sampling oscilloscope and stored for post-processing on a computer. As a second test choice, we have the digital output interface measured from the RAM and displayed in Fig. 7.1(c). This output represents the output that would

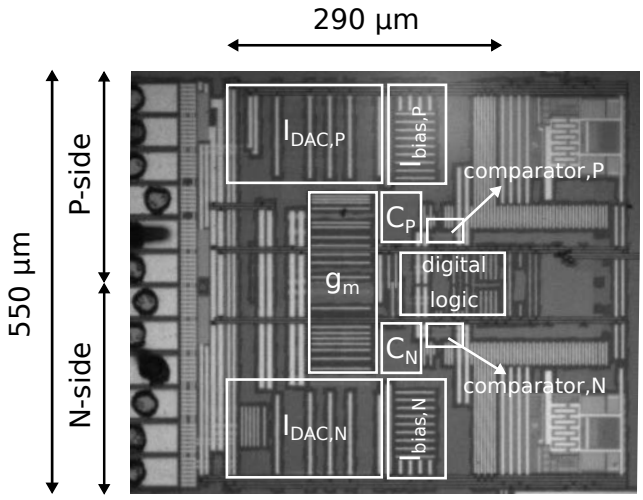


Figure 7.6: Die photo.

be used in practical applications and from where we would expect to observe a similar performance to Fig. 7.1(b).

The circuit was not designed for a specific sampling frequency. Due to the programmable oscillation parameters, we can tune the oscillation frequency to be in accordance with different sampling frequencies and observe the ADC performance when several bandwidths in the input signal are considered.

Firstly, we will start with the results obtained through the test-pin interface. The digital signal from this port is a square signal whose edges (both rising and falling edges) match with the rising edges of the pulsed signal of the monostable ($y_{\mathrm{p}}(t)$ or $y_{\mathrm{n}}(t)$ in Fig. 7.2). If we apply an absolute first difference to the sampled signal, we will demodulate it and we will be able to measure the performance. These operations are made on a computer. Through this test-pin we can select both sides of the pseudo-differential architecture, but only one is visible at a certain instant. Accordingly, the measurements depicted below are single-ended. Fig. 7.7 depicts the output spectra measured by the test-pin for two cases. Data are collected through an oscilloscope using a sampling frequency equal to 5 GHz. In Fig. 7.7(a), the input signal is a 1-MHz -6 dBFS 0.3 $\mathrm{V_{p\text{-}p}}$ sinusoidal wave. This spectrum is limited by flicker noise at low frequencies and quantization noise at high frequencies. The distortion that comes from the transconductance is higher than the distortion expected from simulations. However, a proper HD3 is still achieved and it will not degrade the expected SNDR. In Fig. 7.7(b) the performance of the ADC with no input signal is measured. A tone can be observed at 100 MHz, corresponding to the idle oscillation frequency programmed at 400 MHz. The in-band noise floor is limited by flicker noise.

Secondly, we will show the measurements obtained from the FIFO RAM in a differential configuration. In this case, the data are already demodulated. Therefore, no post-processing is required on a computer. Independent tuning is applied to each side of the pseudo-differential architecture in order to match the oscillator gains and attenuate the even harmonic components.

Fig. 7.10 shows the data measured from the FIFO for the P-side (a), the N-side

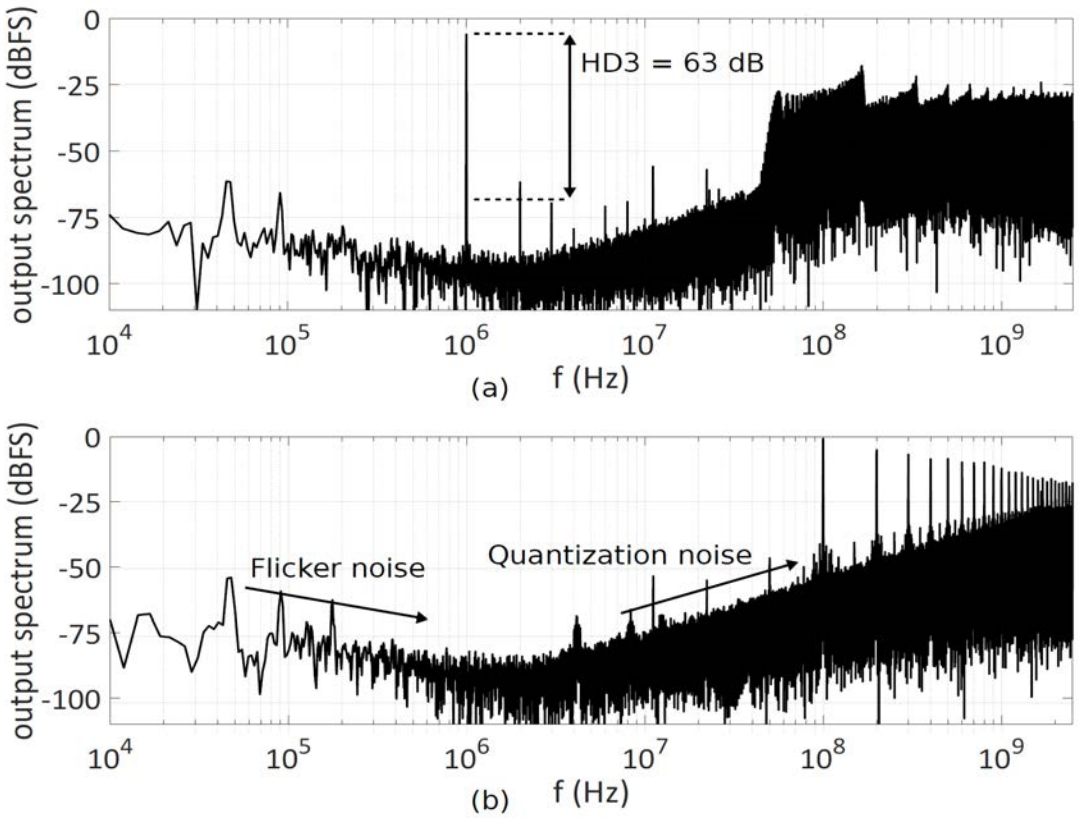


Figure 7.7: Output spectra measured through the test-pin: (a) with input tone, (b) idle state.

(b) and the subtraction between both of them (c). The input signal is a sinusoidal wave with 1-MHz -6 dBFS 0.3 $V_{p\text{-}p}$. The SNDR equals 53 dB for BW= 20 MHz. First-order noise-shaped quantization noise is appreciated at high frequencies and flat noise at low frequencies, which limits the SNDR from the expected design value. Analyzing the data from the digital port, the excess noise captured by the digital interface is attributed to metastability in the sampling circuitry in view of the idle phase noise measured in the laboratory.

Finally, Fig. 7.8 depicts a dynamic range with the same input and oscillation parameters of Fig. 7.10. Here, the measured dynamic range equals 58 dB. The SNDR peaks is measured with a -6 dBFS input signal and it corresponds to the spectrum shown in Fig. 7.10. For input signal amplitudes higher than -6 dBFS the distortion that comes from the transconductance restricts the performance of the converter and, consequently, the SNDR does not get higher.

The total power consumption is 3.5 mW excluding the post-processing digital logic (T2B and RAM) for the pseudo-differential architecture. In Fig. 7.9 we can see the percentage of the power consumed by each block of the ADC core. As can be observed, almost half of the total power consumption corresponds to the comparator, which supposes the bottleneck when trying to reduce the power consumed by the chip. If we split up the power consumption into the analog power and the digital power, the first one supposes 72% and the second one 28% of the total power. This shows us the importance of implementing ADCs

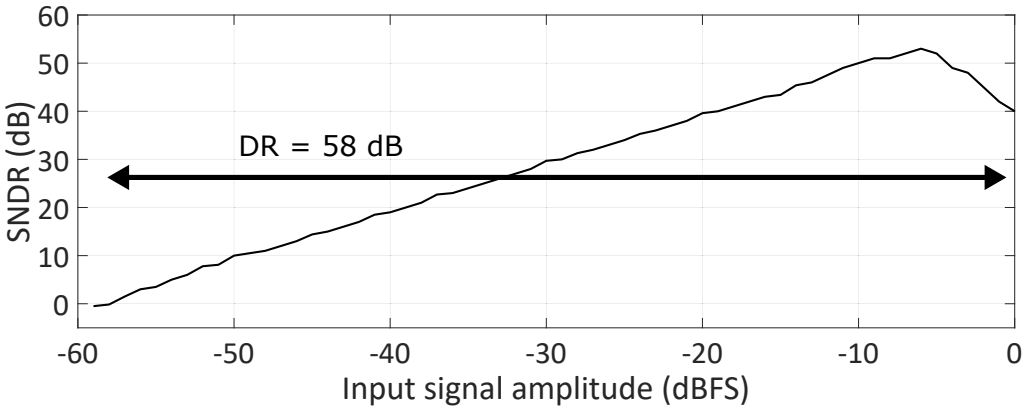


Figure 7.8: Measured dynamic range with a 1-MHz input sinusoidal wave.

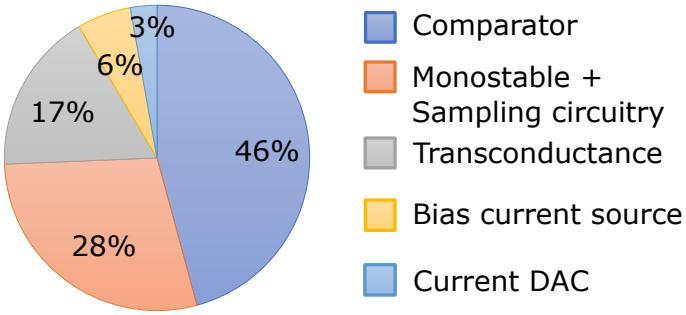


Figure 7.9: Distribution of the power consumption in the chip.

completely digital in order to highly reduce the power consumption.

Table 7.1 shows a comparison between our work and other similar architectures. It can be noticed that our design consumes less power than most of the selected architectures and occupies similar area.

7.3 Conclusion

We have proposed a novel architecture of a VCO-based ADC implemented through a pulse frequency modulator. This new approximation allows us to achieve linear, low-power and low-area ADC architectures. It is implemented with mostly digital circuitry, what makes it very suitable for current deep-submicron processes. The linearity of the architecture depends mainly on the linearity of the front-end transconductor. A new highly-linear bulk-driven transconductor was described and practically tested. Measurements taken from the chip shows a peak SNDR= 53 dB for 20 MHz BW with power consumption of only 3.5 mW and occupied area of 0.08 mm^2. Comparing to other equivalent architectures, our design is efficient in power at the same time that occupies similar area. In addition, this chip supposes the first ADC architecture based on a pulse frequency modulator proposed in the literature at the moment.

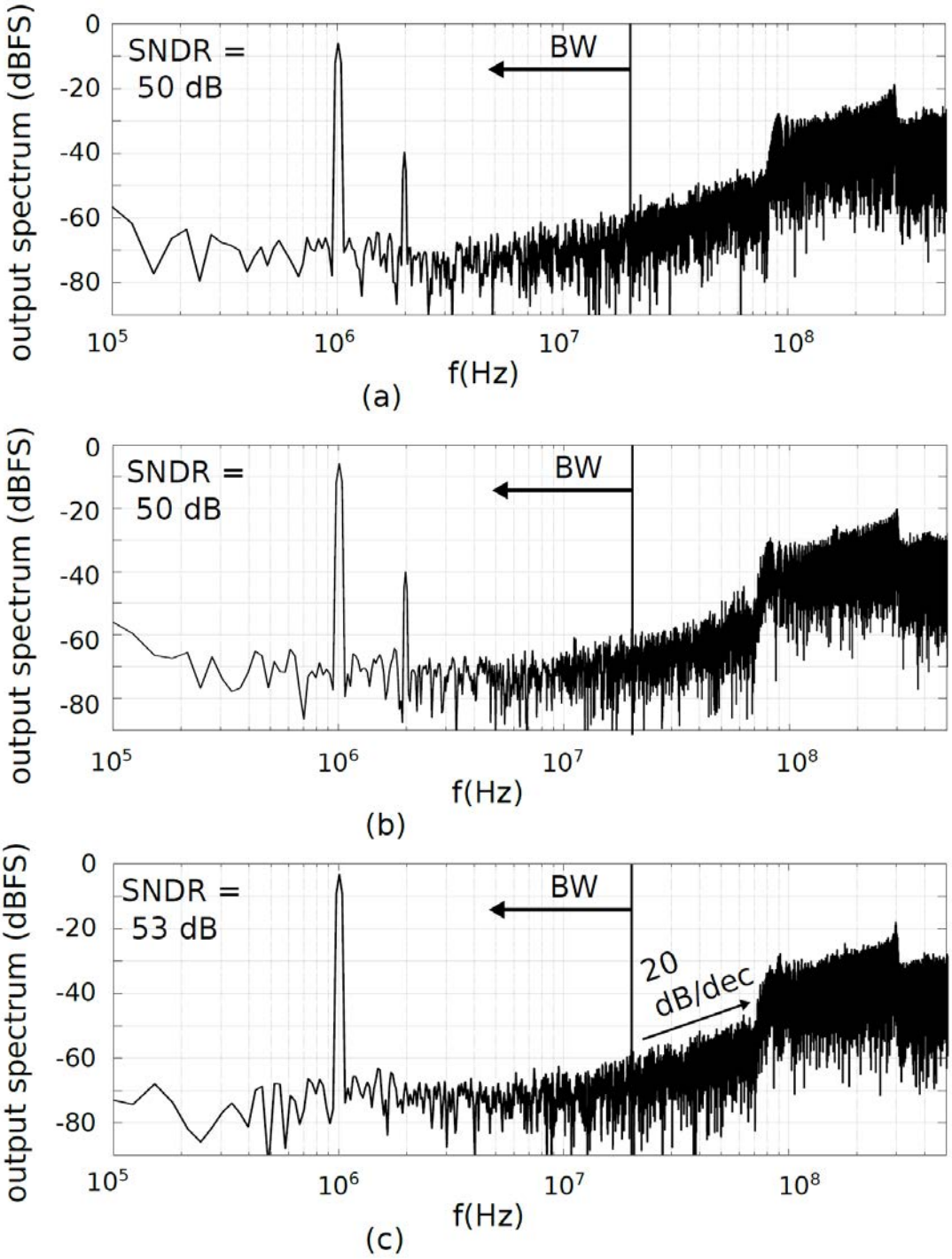


Figure 7.10: Output spectra measured through the digital interface: (a) P-side output, (b) N-side output, and (c) differential output.

Table 7.1: Comparison with related work: PFM-based ADC with active integration

	Process (nm)	**BW (MHz)**	**$SNDR_{peak}$ (dB) | DR (dB)**	**f_s (MHz)**	**Supply voltage(V)**	**Area (mm^2)**	**Power (mW)**	**FoM (fJ/step)**[a]	**FoM (dB)**[b]
[41]	130	10	63.1 | -	500	1.2	0.078	12.6	-	-
[48]	65	10	55.1 | 63	1000	0.8/1.1[d]	0.01	0.71/0.77[d]	-	153.5
[56]	90	8	59.1 | 65.6	640	-	0.1	4.3	366	-
[59]	180	2.5	73.4 | -	51.2	1.8	0.22[e]	4.8	244	161
[61]	65	20	68 | -	1000	1	0.6	8.2	99	162
[62]	40	40	59.5 | -	1600	0.9	0.017	2.57[c]	42	-
[111]	65	30	64 | -	200	1.0	0.023	12.2	154	-
[115]	16	125	71.9 | 74.8	2150	1.35/1.5/1[f]	0.217	54	67.2	165.5
This work	**40**	**20**	**53 | 58**	**1000**	**1.1**	**0.08**	**3.5**	**242**	**150.6**

[a] FoM (fJ/step) = Power/$(2 \cdot BW \cdot 2^{\frac{SNDR_{peak}-1.76}{6.02}})$.
[b] FoM (dB) = $SNDR_{peak}$ + $10\log_{10}$(BW/Power).
[c] The power of the driving buffer is not included.
[d] Analog/digital.
[e] Excludes area of the off-chip digital back-end and calibration unit.
[f] VCO/DAC/others.

Part IV

Conclusion

Chapter 8

Conclusion

In this final chapter, we will summarize the contributions of the PhD research based on the goals proposed at the beginning of the research period. We will also provide some guidelines on possible topics to study in the future. These guidelines come from the last months of investigation and may suppose the starting point of new research projects.

The first topic of the research was providing new insights about how VCO-based systems can be analyzed. We started from the assumption that the analysis of a VCO as a phase integrator leads us to proper designs, but important spectral properties are lost throughout the analysis. In addition, there are no equations that exactly describe the quantization noise in VCO-based systems. We thought that a mathematical description of VCO-based systems was fundamental to design and optimize these systems. Accordingly, at first, we established the equivalence between a VCO and a PFM, which allowed us to propose a model for a generic order VCO-based ADC. This approach provided us the possibility of proposing noise shaping architectures with extended order. We seized the fact that the equations that model a pulse frequency modulated signal were known. These equations could be extended to the output of a VCO-based system to get a mathematical description of it, leading to a better understanding of the different error processes that occur in a VCO-based structure. We also could calculate the performance of this kind of systems in terms of the oscillation parameters of the VCO, without any statistical assumption.

Then, the PFM theory was applied to the proposal and analysis of new VCO-based systems. Firstly, we dealt with single stage architectures. At this point, a second topic emerged, which was how to fix the non-linear voltage-to-frequency relation of the VCO in open-loop configurations, particularly when dealing with ring oscillators. Several approaches had been made in the literature about this issue. In this document, we provided our particular point of view about the issue, proposing two linear correction techniques. The first one focused on the use of a digital modulator in front of the VCO to make it work linearly. This approach was not completely new and had already been proposed by other authors. Nevertheless, we described its performance based on the PFM theory and we supported the theoretical explanations with an experimental chip. The second linear correction technique is based on using a pulse frequency modulator as an ADC. We showed that a PFM-based system might have some linearity advantages with respect to

ring oscillators based ADC. Several PFM-based ADCs were proposed. One of them was implemented on silicon to experimentally check its performance. We also made a first approach to the application of the PFM theory to the design of VCO-based closed-loop configurations, specially focused on continuous-time $\Delta\Sigma$ modulators. Secondly, we studied multistage architectures. We provided a novel approach of VCO-based MASH architectures, which included the modeling of these architectures using the PFM interpretation, how to make a NTF zeros optimization and how MASH structures could be implemented in digital precoded VCO-based architectures.

Finally, the last topic of the document is the description of the experimental results of the previous theoretical content. Two chips were manufactured in 40-nm CMOS processes and were described in Chapter 6 and Chapter 7. In the first chip, we implemented a first order VCO-based ADC with a pulse width modulator as the input stage. The performance measurements were deviated from the theoretical ones due to some design issues, but they allowed us to notice that this type of system might work correctly and lead to low power and low area systems. The second chip is a PFM-based ADC with active integration. We showed that the non-linearity of the system can be kept under control and that a PFM can be used as an ADC as had been predicted previously, leading to efficient low power systems.

8.1 Contributions

To be more precise, we will sort the contributions in function of the chapter in which they are made.

The contributions in Chapter 3 are the following:

- Proposal of the equivalence between a VCO and a pulse frequency modulator. Development of a linear model of a VCO-based system using the PFM theory. Proposal of new open-loop VCO-based architectures. Linear models (similar to those used to design $\Delta\Sigma$ modulators) are proposed with all the errors involved in the analog-to-digital conversion. We show how to ideally extend the noise-shaping order of the architecture, although in practice it does not lead to practical circuits. We demonstrate how a VCO followed by a FIR filter can be approximated to a second-order noise shaping structure.

- Description of the encoding and alias errors in VCO-based ADCs. Based on the oscillation parameters and the bandwidth of the converter, we provide the maximum SNDR possible to be achieved.

- Application of the equations of the PFM to mathematically model the output spectrum of VCO-based systems. We show that estimations based on the equations match properly with the simulations results.

- Definition of the equivalence between a multiphase VCO and a single-phase VCO with higher oscillation frequency.

The contributions in Chapter 4 are the following:

- Analysis of the digital precoding technique to make the VCO work linearly. We use the PFM theory to analyze how the modulation components may affect to the ADC performance.

- Proposal of an efficient PFM-based ADC. Analysis of the performance, the extension to a multibit architecture and inherent linearity. We propose a first circuit of the PFM based on an active integration.

- We extend, step by step, the previous PFM-based architecture to get the simplest possible circuit. Firstly, we propose to use a passive integration only for the input signal, which requires digital correction after sampling. Secondly, we extend the passive integration to the feedback path too. We show that, if some design considerations are taken into account, linearity correction is not required.

- A first approach to the design of continuous-time $\Delta\Sigma$ modulators with VCOs using the PFM theory is made. We propose the equations of an analog integrator built with VCOs, both for the single-ended and the differential case. These equations allow us to study the effect of the modulation components in the loop. We establish the equivalence between the conventional integrators and the VCO-based integrators, and apply the equivalence to some examples.

The contributions in Chapter 5 are the following:

- Application of the PFM theory to MASH architectures. We provide a new approach to this type of systems based on the models developed previously. Based on this approach, we also analyze the practical limiting factors.

- Proposal of a technique to optimize the NTF zeros in generic order MASH architectures. Behavioral simulations are used to validate the approach.

- Extension of the VCO-based ADC structure with a pulse width modulator to a MASH architecture. We show how the interconnection stage is made and what is the performance based on a behavioral simulation.

The contributions in Chapter 6 are the following:

- A VCO-based ADC with pulse width modulator in the front-end is implemented in a 40-nm CMOS process. The measurements show a SNDR of 35.6 dB for a -20 dBFS sinusoidal input wave considering 20 MHz BW. This supposes a theoretical dynamic range equal to 56 dB. The power consumption equals 2.15 mW with 1.1 V supply voltage.

- The performance is degraded due to the GRO, which is not able to keep the phase coherence and oscillate properly when the digital input signal is composed of narrow pulses. This happens when the input amplitude is close to the full scale value.

- If we suppose a potential SNDR peak of 56 dB and compare our architecture to other published systems, our design is much simpler and occupies less area, while keeping the same power consumption.

Finally, the contributions in Chapter 7 are the following:

- A multibit PFM-based ADC is implemented in a 40-nm CMOS process. The measurements show a peak SNDR of 53 dB for a -6 dBFS sinusoidal input wave considering 20 MHz BW. The dynamic range equals 58 dB. The power consumption is 3.5 mW with 1.1 V supply voltage.
- A novel high linear bulk-driven transconductance is implemented in the front-end of the converter. The measurements shows good linearity properties for high amplitude input signals.
- The performance of the converter is degraded due to digital metastability.
- If we compare our architecture to other published systems, our design consumes less power than most of them and occupies similar area.

8.2 Future work

The author would like to provide some suggestions for future research:

- A model for a generic order open-loop VCO-based ADC is provided in Chapter 3. The drawback of this system is that for noise shaping orders higher than one there is no practical design that can be implemented. Some research could be made to investigate novel ways of implementing the generic filter with digital output.
- In the case of the approximation of the second order case through a FIR filter, we use a FIR filter composed of several identical taps with the same time delay. A filter composed of taps with different time delays might take us to new architectures provided that the frequency response of the FIR filter would not be periodic.
- Implementation of band-pass NTFs using the appropriate pulse shaping function.
- The VCO-based MASH is robust against gain variations in the first VCO. However, it is very sensitive to gain variations in the second VCO. It would be very interesting to implement a VCO-based sturdy MASH architecture immune to gain variations in the second VCO.
- Extension of the PFM theory and its application to the design of continuous-time $\Delta\Sigma$ modulators with VCOs. Using the PFM-based equations might allow us to study several phenomena that cannot be studied with the conventional phase integrator model, such as the relation of the intermodulation components at the output, the stability of the system and how to optimize the oscillation parameters of the VCOs.
- Experimental chips with the new architectures proposed in Chapter 3 would help to validate the conclusions we got from a theoretical point of view.

- The VCO-based ADC with digital precoding should be redesigned paying attention to the input stage of the GRO. This stage requires higher speed circuits, which react properly to narrow digital pulses coming from the pulse width modulator.
- A PFM with completely passive integration was proposed theoretically. A chip with this architecture would be interesting to check the performance and the linearity of the system.
- The 40-nm pulse frequency modulator based chip is limited by metastability in the digital circuits. A redesign applying techniques to mitigate metastability is highly recommended. In addition, the comparator supposes almost the 50% of the power consumption. A new comparator design with lower power consumption would result in a more efficient architecture.

Conclusiones

En este capítulo, resumiremos las contribuciones del trabajo de investigación basándonos en las ideas que se propusieron al comienzo del periodo de investigación. Además, se propondrán nuevas líneas de investigación a tener en cuenta en el futuro. Estas líneas derivan de los últimos meses de trabajo y pueden suponer el comienzo de nuevos proyectos.

El punto de inicio de la investigación realizada fue la propuesta de una nueva forma de analizar los sistemas basados en osciladores controlados por tensión. Comenzamos asumiendo que la consideración de que un oscilador controlado por tensión es un integrador de fase puede llevarnos a diseños funcionales. Sin embargo, las características espectrales del oscilador no se tienen en cuenta a lo largo del análisis. Además, desde ese punto de vista, no disponemos de ecuaciones que describan de forma precisa el ruido de cuantificación. Todo lo que se suele afirmar acerca del ruido de cuantificación se basa en modelos estadísticos. En vista de este hecho, se pensó que una descripción matemática de los sistemas basados en osciladores controlados por tensión era fundamental para diseñar y optimizar este tipo de sistemas. Como consecuencia, en primer lugar establecimos la equivalencia entre un oscilador controlado por tensión y un modulador por frecuencia de pulsos, lo que nos permitió proponer un modelo de convertidor analógico-digital basado en oscilador controlado por tensión de orden genérico. Este punto de vista nos facilitó proponer arquitecturas sobremuestreadas con orden extendido. Además, nos beneficiamos del hecho de que las ecuaciones que modelaban la señal de salida de un modulador por frecuencia de pulsos ya eran conocidas. Estas ecuaciones podían ser extendidas para ser aplicadas a la salida de sistemas basados en osciladores controlados por tensión y obtener una descripción matemática de la misma. Esto supuso un mejor entendimiento de los diferentes errores que se producen cuando una señal se digitaliza con un oscilador controlado por tensión. También se pudo calcular y analizar el funcionamiento de estos sistemas en función de los parámetros de oscilación del oscilador controlado por tensión, sin ningún tipo de consideración estadística.

A continuación, la teoría de la modulación por frecuencia de pulsos se aplicó a la propuesta y el análisis de nuevos sistemas basados en osciladores controlados por tensión. En primer lugar, estudiamos las arquitecturas con una única etapa. En este punto, surgió un nuevo fenómeno a considerar, que consiste en cómo tratar con la relación no lineal tensión-frecuencia en osciladores controlados por tensión en lazo abierto, especialmente en osciladores en anillo. Varias formas de tratar con este asunto habían sido publicadas ya con anterioridad. En este documento, ofrecemos nuestro particular punto de vista proponiendo dos métodos

de corrección. El primero se centra en el uso de un modulador digital previo al oscilador controlado por tensión, que hace que el oscilador controlado por tensión oscile de forma lineal. Este método no fue completamente nuevo, ya que había sido propuesto por otros autores previamente. Sin embargo, como novedad, se describió la arquitectura desde el punto de vista de la modulación por frecuencia de pulsos y se validó la teoría gracias a un chip experimental. La segunda técnica de corrección que se propuso se basa en el uso de un modulador por frecuencia de pulsos como convertidor analógico-digital. Mostramos que un modulador por frecuencia de pulsos, desde el punto de vista de la linealidad, puede tener ventajas respecto a convertidores analógico-digitales implementados con osciladores en anillo. Se propusieron varias arquitecturas de convertidores analógico-digitales basadas en moduladores por frecuencia de pulsos. Uno de ellos se implementó en chip con el objetivo de comprobar y analizar su funcionamiento. También se realizó una primera aproximación a la aplicación de la teoría de la modulación por frecuencia de pulsos para el diseño de sistemas en lazo cerrado basados en osciladores controlados por tensión, poniendo especial énfasis en los moduladores $\Delta\Sigma$ en tiempo continuo. A continuación, centramos la atención en las arquitecturas multietapa. Se propuso una nueva forma de estudiar las arquitecturas en cascada de tipo MASH, que incluía el modelado de las mismas haciendo uso de la teoría de la modulación por frecuencia de pulsos, la optimización de los ceros de la función de transferencia del ruido y la descripción de arquitecturas en cascada con osciladores controlados por tensión con codificación digital previa.

Finalmente, el último punto a tratar del documento es la descripción de los resultados experimentales, que se basan en los resultados teóricos propuestos anteriormente. Se fabricaron dos chips experimentales en procesos CMOS de 40 nm. Estos chips se describieron en los Capítulos 6 y 7. En el primer chip, se implementó un convertidor analógico-digital basado en oscilador controlado por tensión de primer orden con un modulador por ancho de pulsos en la etapa de entrada. Las medidas realizadas difieren de las ideales debido a algunos problemas de diseño. No obstante, nos permitieron constatar que este tipo de sistemas pueden usarse como convertidores funcionales eficientes en potencia y área. El segundo chip es un convertidor analógico-digital basado en un modulador por frecuencia de pulsos con integración activa. Se mostró que la no linealidad del sistema puede mantenerse bajo control, si se toman ciertas consideraciones al respecto, y que un modulador por frecuencia de pulsos puede emplearse como convertidor analógico-digital, como había sido predicho con anterioridad. Este tipo de arquitecturas derivan en sistemas eficientes en potencia.

Contribuciones

Para ser más específicos, a continuación se nombran las contribuciones del trabajo de investigación atendiendo al capítulo en donde se encuentran.

Las contribuciones del Capítulo 3 son las siguientes:

- Equivalencia entre un oscilador controlado por tensión y un modulador por frecuencia de pulsos. Modelo lineal de un sistema basado en oscilador controlado por tensión haciendo uso de la teoría de la modulación por frecuen-

cia de pulsos. Propuesta de nuevas arquitecturas en lazo abierto basadas en oscilador controlado por tensión. Modelos lineales (similares a aquellos usados en el diseño de moduladores $\Delta\Sigma$) en donde se aprecian todos los errores involucrados en la conversión analógica-digital. Se muestra también cómo se realiza la extensión del orden del conformado espectral de ruido a un orden genérico, aunque en la práctica no se puedan alcanzar circuitos funcionales. Finalmente, se demuestra cómo un oscilador controlado por tensión seguido de un filtro FIR se puede aproximar a una arquitectura de segundo orden.

- Descripción de los errores asociados a la codificación y al muestreo en los convertidores analógico-digitales basados en osciladores controlados por tensión. Basándonos en los parámetros de oscilación del oscilador y en el ancho de banda considerado, se aporta la máxima relación señal-(ruido-distorsión) que se puede conseguir.

- Aplicación de las ecuaciones de la modulación por frecuencia de pulsos para describir matemáticamente el espectro de salida de sistemas basados en osciladores controlados por tensión. Se muestra la concordancia existente entre los resultados obtenidos y las simulaciones de comportamiento.

- Definición de la equivalencia entre un oscilador controlado por tensión con varias fases y un oscilador controlado por tensión con una única fase pero con una mayor frecuencia de oscilación.

Las contribuciones del Capítulo 4 son las siguientes:

- Análisis de la codificación digital previa al oscilador controlado por tensión con el objetivo de hacer que este último oscile en régimen lineal. Se usa la teoría de la modulación por frecuencia de pulsos para analizar cómo las componentes de la modulación pueden afectar al rendimiento del convertidor analógico-digital.

- Propuesta de un convertidor analógico-digital eficiente basado en un modulador por frecuencia de pulsos. Análisis de su rendimiento, de la extensión a una arquitectura de varios bits y la linealidad inherente. Se propone un primer circuito para el modulador por frecuencia de pulsos basado en una integración activa.

- Extensión, paso por paso, de la arquitectura previa a una que sea lo más simple posible. En primer lugar, se propone usar un integrador pasivo solo para la señal de entrada, lo que implica la necesidad de corregir digitalmente la distorsión tras el muestreo. En segundo lugar, se extiende la integración pasiva también la realimentación. Se muestra que, si ciertas consideraciones de diseño se tienen en cuenta, no es necesario corregir la distorsión.

- Se aportan las primeras nociones para el diseño de moduladores $\Delta\Sigma$ en tiempo continuo con osciladores controlados por tensión haciendo uso de la teoría de la modulación por frecuencia de pulsos. Se proponen las ecuaciones que modelan un integrador analógico implementado con osciladores

controlados por tensión, tanto para el caso "single-ended" como para el caso diferencial. Estas ecuaciones nos permiten estudiar el efecto de las componentes de modulación en el lazo. Se establece la equivalencia entre los integradores convencionales y los implementados con osciladores controlados por tensión. Finalmente, se aplica dicha equivalencia para proponer algunos ejemplos de aplicación.

Las contribuciones del Capítulo 5 son las siguientes:

- Aplicación de la teoría por frecuencia de pulsos a arquitecturas en cascada de tipo MASH. Se aporta una nueva perspectiva de estos sistemas basándonos en los modelos propuestos con anterioridad. Con esta perspectiva también se analizan los factores limitantes que surgen en la práctica.

- Propuesta de una técnica para optimizar los ceros de la función de transferencia del ruido en una arquitectura de tipo MASH. La técnica se valida a través de simulaciones de comportamiento.

- Extensión de la arquitectura de convertidor analógico-digital basado en oscilador controlado por tensión con modulación previa por ancho de pulsos a arquitecturas de tipo MASH. Se muestra cómo se implementa la etapa de conexión entre etapas y cuál es el rendimiento esperado con simulaciones de comportamiento.

Las contribuciones del Capítulo 6 son las siguientes:

- Un convertidor analógico-digital basado en oscilador controlado por tensión con modulación previa por ancho de pulsos se implementa en un proceso CMOS de 40 nm. Las medidas realizadas muestran una relación señal-(ruido-distorsión) de 35.6 dB para una señal sinusoidal de entrada de -20 dBFS considerando un ancho de banda de 20 MHz. Esto supone un rango dinámico teórico de 56 dB. La potencia consumida es 2.15 mW con una tensión de alimentación igual a 1.1 V.

- La resolución medida es menor a la que se esperaba desde un punto de vista ideal debido al oscilador controlado por tensión, ya que no es capaz de oscilar correctamente y mantener la coherencia de fase ante señales con pulsos digitales estrechos. Esto ocurre cuando la señal de entrada del convertidor está próxima a valores del fondo de escala.

- Suponiendo una señal-(ruido-distorsión) pico virtual equivalente a 56 dB y comparando nuestra arquitectura con otros sistemas publicados, nuestro diseño es más simple, ocupa menos área y consume una potencia equivalente.

Finalmente, las contribuciones del Capítulo 7 son las siguientes:

- Un convertidor analógico-digital basado en un modulador por frecuencia de pulsos de varios bits se implementa en un proceso CMOS de 40 nm. Las medidas realizadas muestran una relación señal-(ruido-distorsión) pico de

53 dB para una señal sinusoidal de entrada de -6 dBFS considerando un ancho de banda de 20 MHz. El rango dinámico es igual a 58 dB. La potencia consumida es 3.5 mW con una tensión de alimentación igual a 1.1 V.

- Una nueva arquitectura lineal de transconductor con la señal de entrada a través del sustrato de los transistores se implementa en la etapa de entrada del convertidor. Las medidas realizadas muestran buenas propiedades de linealidad para señales con gran amplitud.

- La resolución del convertidor se reduce con respecto a la esperada debido a fenómenos de metaestabilidad en los circuitos digitales.

- Comparando la arquitectura con otros sistemas publicados, nuestro diseño consume menos potencia que la mayor parte de los diseños publicados y ocupa un área similar.

Líneas de investigación futuras

A continuación se muestran algunas sugerencias para la continuación del trabajo presentado en este documento:

- Un modelo de orden genérico de un convertidor analógico-digital basado en oscilador controlado por tensión en lazo abierto se propone en el Capítulo 3. El problema de este sistema es que para diseños con orden mayor que uno, el filtro resultante no es implementable en un convertidor. Una línea de investigación futura consistiría en la propuesta de los filtros digitales necesarios para alcanzar sistemas de orden mayor que uno que pudieran incluirse en la estructura de un convertidor analógico-digital.

- En el caso de la aproximación al caso de segundo orden a través de un filtro FIR, se utiliza un filtro FIR compuesto de varias etapas idénticas que retrasan el mismo tiempo. Un filtro FIR compuesto con etapas distintas con respecto al tiempo retrasado puede derivar en nuevas arquitecturas dado que la respuesta en frecuencia del filtro no sería periódica.

- Implementación de arquitecturas paso-banda haciendo uso del filtro apropiado.

- La arquitectura de tipo MASH basada en osciladores controlados por tensión es robusta frente a las variaciones de ganancia del oscilador de la primera etapa. Sin embargo, es muy sensible a las variaciones de ganancia del oscilador de la segunda etapa. Sería muy interesante implementar una arquitectura de tipo MASH immune frente a variaciones de ganancia en la segunda etapa.

- Extensión de la teoría de la modulación por frecuencia de pulsos y su aplicación al diseño de moduladores $\Delta\Sigma$ en tiempo continuo con osciladores controlados por tensión. Usar la teoría de la modulación por frecuencia de

pulsos nos permitiría estudiar varios fenómenos que no podrían ser estudiados con el modelo convencional de integrador de fase, como es la relación entre los productos de intermodulación a la salida del sistema, la estabilidad del sistema o la optimización de los parámetros de oscilación.

- La implementación de chips experimentales con las nuevas arquitecturas propuestas en el Capítulo 3 ayudarían a validar las conclusiones que se obtuvieron desde un punto de vista teórico.

- El convertidor analógico-digital basado en oscilador controlado por tensión con modulación digital en la etapa de entrada debería ser rediseñado poniendo atención a la etapa de entrada de los osciladores controlados por tensión. Esta etapa requiere de circuitos más rápidos que reaccionen correctamente a pulsos digitales estrechos.

- Un modulador por frecuencia de pulsos con integración pasiva tanto en la entrada como en la realimentación se propuso desde un punto de vista teórico. La implementación de un chip experimental con esta arquitectura sería interesante para comprobar su funcionamiento y medir la linealidad del mismo.

- La resolución del modulador por frecuencia de pulsos implementado en 40 nm está limitada por fenómenos de metaestabilidad en los circuitos digitales. Se recomienda un rediseño de la arquitectura aplicando técnicas para mitigar este fenómeno. Además, el comparador de la arquitectura consume casi el 50% de la potencia total, por lo que un nuevo diseño de comparador con menor consumo de potencia es altamente recomendable.

Appendix

In this appendix we will summarize the mathematical derivation of the equations that describe the pulse frequency modulated signals $p(t)$ of Fig. 3.13 and $d(t)$ of Fig. 3.2. The derivation of signal $p(t)$ was firstly published in [71] and, later on, it was expanded to signal $d(t)$ in [77]. Here, we will follow the same procedure, but applying it to the output of a VCO.

Signal $p(t)$ is a train of fixed-length pulses (we will suppose that the amplitude of the pulses is equal to 1), with length equal to T_{d} and rising edges placed at time instants t_{k}:

$$h(t) = \sum_{k=-\infty}^{\infty} u(t - t_{\mathrm{k}}) - u(t - t_{\mathrm{k}} - T_{\mathrm{d}}), \tag{1}$$

where time instants t_{k} correspond to the instants at which the phase of the VCO ($\varphi(t)$) is multiple of 2π (we only consider the rising edges).

The oscillation frequency of the VCO is defined as follows:

$$f_{\mathrm{osc}}(t) = f_{\mathrm{o}} + K_{\mathrm{VCO}} \cdot x(t). \tag{2}$$

If we suppose that the input signal is a sinusoidal wave of the form:

$$x(t) = A \cdot \cos\left(\omega_{\mathrm{x}} t\right), \tag{3}$$

the output phase of the VCO will be represented as:

$$\varphi(t) = \int_0^t (f_{\mathrm{o}} + K_{\mathrm{VCO}} x(\tau)) d\tau = f_{\mathrm{o}} t + \frac{A \cdot K_{\mathrm{VCO}}}{\omega_{\mathrm{x}}} \sin(\omega_{\mathrm{x}} t). \tag{4}$$

Then, we will be able to calculate the instants t_{k} if we solve the following equation:

$$f_{\mathrm{o}} t_{\mathrm{k}} + \frac{A \cdot K_{\mathrm{VCO}}}{\omega_{\mathrm{x}}} \sin(\omega_{\mathrm{x}} t_{\mathrm{k}})) = 2\pi n \qquad n = 0, 1, 2... \tag{5}$$

Unfortunately, (5) is not an equation with intuitive solution.

We will define a new variable time called t':

$$t' = t + \frac{A \cdot K_{\mathrm{VCO}}}{\omega_{\mathrm{x}} f_{\mathrm{o}}} \sin(\omega_{\mathrm{x}} t)). \tag{6}$$

This new variable will be substituted in (1). Then, using Parseval relation [116],

we will get:

$$p(t) = \frac{1}{2\pi j} \sum_{q=-\infty}^{\infty} \frac{1}{q} (e^{jq\omega_o t'} - e^{jq\omega_o (t'-T_d)}). \tag{7}$$

If we combine (6) and (7), the resulting expression will be the following:

$$p(t) = \frac{1}{2\pi j} \sum_{q=-\infty}^{\infty} \frac{1}{q} e^{jq\omega_o t} (e^{jq\frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}}\sin(\omega_{\mathrm{x}} t)} - e^{jq\frac{AK_{\mathrm{VCO}}}{f_{\mathrm{x}}}\sin(\omega_{\mathrm{x}}(t-T_{\mathrm{d}}))} \cdot e^{-jq\omega_{\mathrm{o}} T_{\mathrm{d}}}), \tag{8}$$

where $j = \sqrt{-1}$. If we make use of the property of Bessel functions shown in (9), apply it to (8) and operate, the result will be (3.21).

$$e^{jZsin\theta} = \sum_{r=-\infty}^{\infty} J_r(Z) e^{jr\theta} \tag{9}$$

Finally, $d(t)$ will be the limit of $p(t)$ when T_{d} tends to zero and the amplitude of the pulses tends to infinity (with the goal of keeping the power of the pulses). If we calculate properly this limit, we will get (3.3).

Bibliography

[1] R. Malladi and D. Agrawal, "Current and Future Applications of Mobile and Wireless Networks," *Commun. ACM*, vol. 45, pp. 144–146, 10 2002.

[2] [Online]. Available: https://www.postscapes.com/internet-of-things-protocols/

[3] J. Wannstrom. (2013). [Online]. Available: http://www.3gpp.org/technologies/keywords-acronyms/97-lte-advanced

[4] J. Hauptmann, D. Giotta, and U. Gaier, "Analog design trends in communication systems," in *Proceedings of the 2013 9th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, June 2013, pp. 3–6.

[5] [Online]. Available: http://www.figaro.co.jp/en/technicalinfo/miniaturization.html

[6] Advancing moore's law the road to 14 nm. [Online]. Available: https://www.intel.com/content/www/us/en/silicon-innovations/advancing-moores-law-in-2014-presentation.html

[7] [Online]. Available: http://www.analog.com/en/analog-dialogue/articles/the-right-adc-architecture.html

[8] S. Paton, A. D. Giandomenico, L. Hernandez, A. Wiesbauer, T. Potscher, and M. Clara, "A 70-mW 300-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 15-MHz bandwidth and 11 bits of resolution," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1063, July 2004.

[9] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz CMOS Continuous-Time $\Sigma\Delta$ ADC With 20-MHz Signal Bandwidth, 80-dB Dynamic Range and 12-bit ENOB," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, Dec 2006.

[10] S. Yan and E. Sanchez-Sinencio, "A continuous-time sigma-delta modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 75–86, Jan 2004.

[11] L. J. Breems, R. Rutten, and G. Wetzker, "A cascaded continuous-time $\Sigma\Delta$ Modulator with 67-dB dynamic range in 10-MHz bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2152–2160, Dec 2004.

[12] A. Morgado, R. del Ro, J. M. de la Rosa, L. Bos, J. Ryckaert, and G. V. der Plas, "A 100khz-10mhz bw, 78-to-52db dr, 4.6-to-11mw flexible sc $\sigma\delta$ modulator in 1.2-v 90-nm cmos," in *2010 Proceedings of ESSCIRC*, Sept 2010, pp. 418–421.

[13] O. Rajaee, T. Musah, N. Maghari, S. Takeuchi, M. Aniya, K. Hamashita, and U. K. Moon, "Design of a 79 dB 80 MHz 8X-OSR Hybrid Delta-Sigma/Pipelined ADC," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 719–730, April 2010.

[14] C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, April 2010.

[15] M. Steyaert, V. Peluso, J. Bastos, P. Kinget, and W. Sansen, "Custom analog low power design: the problem of low voltage and mismatch," in *Proceedings of CICC 97 - Custom Integrated Circuits Conference*, May 1997, pp. 285–292.

[16] K. Bult, "Analog design in deep sub-micron CMOS," in *Proceedings of the 26th European Solid-State Circuits Conference*, Sept 2000, pp. 126–132.

[17] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog Circuit Design in Nanoscale CMOS Technologies," *Proceedings of the IEEE*, vol. 97, no. 10, pp. 1687–1714, Oct 2009.

[18] M. Choi and A. A. Abidi, "A 6-b 1.3-Gsample/s A/D converter in 0.35- μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1847–1858, Dec 2001.

[19] K. Uyttenhove and M. S. J. Steyaert, "A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25- μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1115–1122, July 2003.

[20] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner, "A 6-bit 1.2-GS/s low-power flash-ADC in 0.13- μm digital CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 7, pp. 1499–1505, July 2005.

[21] L. Hernandez and E. Prefasi, "Analog-to-digital conversion using noise shaping and time encoding," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 7, pp. 2026–2037, Aug 2008.

[22] E. Prefasi, S. Paton, L. Hernandez, R. Gaggl, A. Wiesbauer, and J. Hauptmann, "A 0.08 mm^2, 7 mW Time-Encoding Oversampling Converter with 10 bits and 20MHz BW in 65nm CMOS," in *2010 Proceedings of ESSCIRC*, Sept 2010, pp. 430–433.

[23] J. P. Jansson, A. Mantyniemi, and J. Kostamovaara, "A CMOS time-to-digital converter with better than 10 ps single-shot precision," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1286–1296, June 2006.

[24] J. Jalil, M. B. I. Reaz, and M. A. M. Ali, "CMOS Differential Ring Oscillators: Review of the Performance of CMOS ROs in Communication Systems," *IEEE Microwave Magazine*, vol. 14, no. 5, pp. 97–109, July 2013.

[25] T. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design*, ser. Analog Integrated Circuit Design. Wiley, 2011.

[26] R. Schreier and G. C. Temes, *Understanding delta-sigma data converters*. New York, NY: Wiley, 2005.

[27] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd ed. Wiley-IEEE Press, 2010.

[28] C. Analog Devices, Inc., *Analog-digital Conversion Handbook; 3rd Ed.* Upper Saddle River, NJ, USA: Prentice-Hall, Inc., 1986.

[29] J. C. Candy and G. C. Temes, *Oversampled SigmaDelta Modulation*. Wiley-IEEE Press, 1992, pp. 73–80. [Online]. Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=5312250

[30] J. M. de la Rosa, "Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 1–21, Jan 2011.

[31] J. M. de la Rosa, R. Schreier, K. P. Pun, and S. Pavan, "Next-Generation Delta-Sigma Converters: Trends and Perspectives," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 484–499, Dec 2015.

[32] J. G. Tuxal, *Automatic Feedback Control System Synthesis*. McGraw-Hill Book Company, Inc., 1955.

[33] T. Georgantas, Y. Papananos, and Y. Tsvidis, "A comparative study of five integrator structures for monolithic continuous-time filters: a tutorial," in *1993 IEEE International Symposium on Circuits and Systems*, May 1993, pp. 1259–1262 vol.2.

[34] E. Sanchez-Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial," *IEE Proceedings - Circuits, Devices and Systems*, vol. 147, no. 1, pp. 3–12, Feb 2000.

[35] M. Kachare, A. J. Lopez-Martin, J. Ramirez-Angulo, and R. G. Carvajal, "A compact tunable CMOS transconductor with high linearity," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 2, pp. 82–84, Feb 2005.

[36] A. J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 132–143, Jan 2005.

[37] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, Mar 1996.

[38] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun 1999.

[39] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 896–909, Jun 2001.

[40] A. Elshazly, S. Rao, B. Young, and P. K. Hanumolu, "A 13b 315fsrms 2mW 500MS/s 1MHz bandwidth highly digital time-to-digital converter using switched ring oscillators," in *2012 IEEE International Solid-State Circuits Conference*, Feb 2012, pp. 464–466.

[41] J. Kim, T. K. Jang, Y. G. Yoon, and S. Cho, "Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 1, pp. 18–30, Jan 2010.

[42] J. Daniels, W. Dehaene, M. S. J. Steyaert, and A. Wiesbauer, "A/D Conversion Using Asynchronous Delta-Sigma Modulation and Time-to-Digital Conversion," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 9, pp. 2404–2412, Sept 2010.

[43] G. Taylor and I. Galton, "A Mostly-Digital Variable-Rate Continuous-Time Delta-Sigma Modulator ADC," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2634–2646, Dec 2010.

[44] M. Z. Straayer and M. H. Perrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time *SigmaDelta* ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, April 2008.

[45] A. Wiesbauer, D. Straussnigg, L. Hernandez, and F. Cardes, "System and Method for an Oversampled Data Converter," United States Patent 20 140 270 261, Sept. 18, 2014.

[46] Y. Du, T. He, Y. Jiang, S. W. Sin, U. Seng-Pan, and R. P. Martins, "A continuous-time VCO-assisted VCO-based $\Sigma\Delta$ modulator with 76.6dB SNDR and 10MHz BW," in *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, May 2013, pp. 373–376.

[47] A. Babaie-Fishani and P. Rombouts, "Highly linear VCO for use in VCO-ADCs," *Electronics Letters*, vol. 52, no. 4, pp. 268–270, 2016.

[48] ——, "A Mostly Digital VCO-Based CT-SDM With Third-Order Noise Shaping," *IEEE Journal of Solid-State Circuits*, vol. PP, no. 99, pp. 1–13, 2017.

[49] B. Young, K. Reddy, S. Rao, A. Elshazly, T. Anand, and P. K. Hanumolu, "A 75dB DR 50MHz BW 3rd order CT- ΔΣ modulator using VCO-based integrators," in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, June 2014, pp. 1–2.

[50] K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, and P. K. Hanumolu, "A 16mW 78dB-SNDR 10MHz-BW CT- ΔΣ ADC using residue-cancelling VCO-based quantizer," in *2012 IEEE International Solid-State Circuits Conference*, Feb 2012, pp. 152–154.

[51] N. Narasimman and T. T. Kim, "An ultra-low voltage, VCO-based ADC with digital background calibration," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 1458–1461.

[52] S. Rao, K. Reddy, B. Young, and P. K. Hanumolu, "A Deterministic Digital Background Calibration Technique for VCO-Based ADCs," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 950–960, April 2014.

[53] T. K. Jang, J. Kim, Y. G. Yoon, and S. Cho, "A Highly-Digital VCO-Based Analog-to-Digital Converter Using Phase Interpolator and Digital Calibration," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 8, pp. 1368–1372, Aug 2012.

[54] L. Hernandez, S. Paton, and E. Prefasi, "VCO-based sigma delta modulator with PWM precoding," *Electronics Letters*, vol. 47, no. 10, pp. 588–589, May 2011.

[55] L. Hernandez, E. Prefasi, S. Paton, and P. Rombouts, "Analysis of VCO based noise shaping ADCs linearized by PWM modulation," in *2012 19th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2012)*, Dec 2012, pp. 352–355.

[56] S. Rao, B. Young, A. Elshazly, W. Yin, N. Sasidhar, and P. K. Hanumolu, "A 71dB SFDR open loop VCO-based ADC using 2-level PWM modulation," in *2011 Symposium on VLSI Circuits - Digest of Technical Papers*, June 2011, pp. 270–271.

[57] A. Babaie-Fishani and P. Rombouts, "Design of a low-voltage op-amp-less ASDM to linearise VCO-ADC," *Electronics Letters*, vol. 52, no. 11, pp. 911–913, 2016.

[58] E. Roza, "Analog-to-digital conversion via duty-cycle modulation," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 11, pp. 907–914, Nov 1997.

[59] K. Ragab and N. Sun, "A 12-b ENOB 2.5-MHz BW VCO-Based 0-1 MASH ADC With Direct Digital Background Calibration," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 433–447, Feb 2017.

[60] S. Li and N. Sun, "A 174.3dB FoM VCO-based CT ΔΣ modulator with a fully digital phase extended quantizer and tri-level resistor DAC in 130nm CMOS," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Sept 2016, pp. 241–244.

[61] A. Ghosh and S. Pamarti, "Linearization Through Dithering: A 50 MHz Bandwidth, 10-b ENOB, 8.2 mW VCO-Based ADC," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 9, pp. 2012–2024, Sept 2015.

[62] X. Xing and G. G. E. Gielen, "A 42 fJ/Step-FoM Two-Step VCO-Based Delta-Sigma ADC in 40 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 3, pp. 714–723, March 2015.

[63] M. Voelker, S. Pashmineh, J. Hauer, and M. Ortmanns, "Current feedback linearization applied to oscillator based adcs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 11, pp. 3066–3074, Nov 2014.

[64] R. M. Gray, W. Chou, and P. W. Wong, "Quantization noise in single-loop sigma-delta modulation with sinusoidal inputs," *IEEE Transactions on Communications*, vol. 37, no. 9, pp. 956–968, Sep 1989.

[65] R. M. Gray, "Spectral analysis of quantization noise in a single-loop sigma-delta modulator with DC input," *IEEE Transactions on Communications*, vol. 37, no. 6, pp. 588–599, Jun 1989.

[66] M. Park and M. H. Perrott, "A VCO-based analog-to-digital converter with second-order Sigma-Delta noise shaping," in *2009 IEEE International Symposium on Circuits and Systems*, May 2009, pp. 3130–3133.

[67] U. Sönmez, F. Sebastiano, and K. A. A. Makinwa, "Analysis and Design of VCO-Based Phase-Domain ΣΔ Modulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 5, pp. 1075–1084, May 2017.

[68] S. Ardalan and J. Paulos, "An analysis of nonlinear behavior in delta - sigma modulators," *IEEE Transactions on Circuits and Systems*, vol. 34, no. 6, pp. 593–603, Jun 1987.

[69] C. M. Zierhofer, "Frequency Modulation and First-Order Delta Sigma Modulation: Signal Representation With Unity Weight Dirac Impulses," *IEEE Signal Processing Letters*, vol. 15, pp. 825–828, 2008.

[70] M. Hovin, D. Wisland, Y. Berg, J. T. Marienborg, and T. S. Lande, "Delta-sigma modulation in single neurons," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, vol. 5, 2002, pp. V–617–V–620 vol.5.

[71] E. Fitch, "The spectrum of modulated pulses," *Electrical Engineers - Part IIIA: Radiocommunication, Journal of the Institution of*, vol. 94, no. 13, pp. 556–564, March 1947.

[72] W. Yu, J. Kim, K. Kim, and S. Cho, "A Time-Domain High-Order MASH $\Delta\Sigma$ ADC Using Voltage-Controlled Gated-Ring Oscillator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 4, pp. 856–866, April 2013.

[73] Y. Yoon, K. Lee, P. Wang, and N. Sun, "A purely-VCO-based single-loop high-order continuous-time $\Delta\Sigma$ ADC," in *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, June 2014, pp. 926–929.

[74] A. Babaie-Fishani and P. Rombouts, "True high-order VCO-based ADC," *Electronics Letters*, vol. 51, no. 1, pp. 23–25, 2015.

[75] A. Sanyal and N. Sun, "Second-order VCO-based $\Delta\Sigma$ ADC using a modified DPLL," *Electronics Letters*, vol. 52, no. 14, pp. 1204–1205, 2016.

[76] C. Wulff and T. Ytterdal, "Resonators in open-loop sigma delta modulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 10, pp. 2159–2172, Oct 2009.

[77] E. J. Bayly, "Spectral Analysis of Pulse Frequency Modulation in the Nervous Systems," *IEEE Transactions on Biomedical Engineering*, vol. BME-15, no. 4, pp. 257–265, Oct 1968.

[78] J. Daniels, W. Dehaene, M. Steyaert, and A. Wiesbauer, "A 0.02mm^2 65nm CMOS 30MHz BW all-digital differential VCO-based ADC with 64dB SNDR," in *2010 Symposium on VLSI Circuits*, June 2010, pp. 155–156.

[79] R. Schreier and G. C. Temes, *Understanding delta-sigma data converters*. New York, NY: Wiley, 2005. [Online]. Available: https://cds.cern.ch/record/733538

[80] C. M. Zierhofer, "Quantization Noise as Superposition of Frequency-Modulated Sinusoids," *IEEE Signal Processing Letters*, vol. 16, no. 11, pp. 933–936, Nov 2009.

[81] Y. Tsividis, "Mixing domains in signal processing," in *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, vol. 1, May 2004, pp. I–157–I–160 Vol.1.

[82] N. T. Thao, "Formal Spectral Theory for Ideal Sigma-Delta Quantization with Stationary Time-Varying Inputs," in *2007 IEEE International Conference on Acoustics, Speech and Signal Processing - ICASSP '07*, vol. 3, April 2007, pp. III–1481–III–1484.

[83] T. Redant, P. A. J. Nuyts, P. Reynaert, and W. Dehaene, "Presilicon Circuit-Aware Linear Least Squares Spectral Analysis for Time-Based Data Converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 11, pp. 751–755, Nov 2013.

[84] W. Yu, K. Kim, and S. Cho, "A 148fs$_{rms}$ Integrated Noise 4 MHz Bandwidth Second-Order $\Delta\Sigma$ Time-to-Digital Converter With Gated Switched-Ring Oscillator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, pp. 2281–2289, Aug 2014.

[85] Z. Song and D. V. Sarwate, "The Frequency Spectrum of Pulse Width Modulated Signals," *Signal Process.*, vol. 83, no. 10, pp. 2227–2258, Oct. 2003. [Online]. Available: http://dx.doi.org/10.1016/S0165-1684(03)00164-6

[86] M. Nakao, M. Norimatsu, Y. Mizutani, and M. Yamamoto, "Spectral distortion properties of the integral pulse frequency modulation model," *IEEE Transactions on Biomedical Engineering*, vol. 44, no. 5, pp. 419–426, May 1997.

[87] M. Z. Straayer and M. H. Perrott, "A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, April 2009.

[88] B. M. Helal, M. Z. Straayer, G. Y. Wei, and M. H. Perrott, "A Low Jitter 1.6 GHz Multiplying DLL Utilizing a Scrambling Time-to-Digital Converter and Digital Correlation," in *2007 IEEE Symposium on VLSI Circuits*, June 2007, pp. 166–167.

[89] C. M. Hsu, M. Z. Straayer, and M. H. Perrott, "A Low-Noise Wide-BW 3.6-GHz Digital $\Delta\Sigma$ Fractional-N Frequency Synthesizer With a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, Dec 2008.

[90] Y. Tsividis, "Mixed-Domain Systems and Signal Processing Based on Input Decomposition," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 10, pp. 2145–2156, Oct 2006.

[91] K. Reddy, S. Dey, S. Rao, B. Young, P. Prabha, and P. K. Hanumolu, "A 54mW 1.2GS/s 71.5dB SNDR 50MHz BW VCO-based CT $\Delta\Sigma$ ADC using dual phase/frequency feedback in 65nm CMOS," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*, June 2015, pp. C256–C257.

[92] A. Iwata, N. Sakimura, M. Nagata, and T. Morie, "The architecture of delta sigma analog-to-digital converters using a voltage-controlled oscillator as a multibit quantizer," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 7, pp. 941–945, Jul 1999.

[93] S. Li and N. Sun, "A 0.028mm^2 19.8fJ/step 2nd-order VCO-based CT $\Delta\Sigma$ modulator using an inherent passive integrator and capacitive feedback in 40nm CMOS," in *2017 Symposium on VLSI Circuits*, June 2017, pp. C36–C37.

[94] B. Drost, M. Talegaonkar, and P. K. Hanumolu, "Analog Filter Design Using Ring Oscillator Integrators," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3120–3129, Dec 2012.

[95] ——, "A 0.55V 61dB-SNR 67dB-SFDR 7MHz 4th-order Butterworth filter using ring-oscillator-based integrators in 90nm CMOS," in *2012 IEEE International Solid-State Circuits Conference*, Feb 2012, pp. 360–362.

[96] R. Schreier, "The delta-sigma toolbox for Matlab," 01 2000.

[97] L. Hernandez, "VCO based multi-stage noise shaping ADC," *Electronics Letters*, vol. 48, no. 4, pp. 206–208, February 2012.

[98] M. Hovin, A. Olsen, T. S. Lande, and C. Toumazou, "Delta-sigma modulators using frequency-modulated intermediate values," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 1, pp. 13–22, Jan 1997.

[99] M. Finsrud, M. Hovin, and T. S. Lande, "Adaptive correction of errors in second-order MASH Delta Sigma FDM solution," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 11, pp. 1005–1013, Nov 2001.

[100] D. Y. Yoon, S. Ho, and H. S. Lee, "An 85dB-DR 74.6dB-SNDR 50MHZ-BW CT MASH $\Delta\Sigma$ modulator in 28nm CMOS," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3.

[101] L. J. Breems, R. Rutten, and G. Wetzker, "A cascaded continuous-time Sigma Delta Modulator with 67-dB dynamic range in 10-MHz bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2152–2160, Dec 2004.

[102] A. Elshazly, S. Rao, B. Young, and P. K. Hanumolu, "A Noise-Shaping Time-to-Digital Converter Using Switched-Ring Oscillators - Analysis, Design, and Measurement Techniques," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 5, pp. 1184–1197, May 2014.

[103] L.-K. Leung, C.-F. Chan, and O. C.-S. Choy, "A giga-hertz CMOS digital controlled oscillator," in *ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196)*, vol. 4, May 2001, pp. 610–613 vol. 4.

[104] G. Donzellini, D. D. Caviglia, G. Parodi, D. Ponta, and P. Repetto, "A digital controlled oscillator based on controlled phase shifting," *IEEE Transactions on Circuits and Systems*, vol. 36, no. 8, pp. 1101–1105, Aug 1989.

[105] W. Grollitsch, R. Nonis, and N. D. Dalt, "A 1.4ps rms-period-jitter TDC-less fractional-N digital PLL with digitally controlled ring oscillator in 65nm CMOS," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, Feb 2010, pp. 478–479.

[106] A. Edward, Q. Liu, C. Briseno-Vidrios, M. Kinyua, E. G. Soenen, A. I. Karlayan, and J. Silva-Martinez, "A 43-mW MASH 2-2 CT ΣΔ Modulator Attaining 74.4/75.8/76.8 dB of SNDR/SNR/DR and 50 MHz of BW in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 448–459, Feb 2017.

[107] C. Zhang, L. J. Breems, G. Radulov, M. Bolatkale, H. Hegt, and A. van Roermund, "A digital calibration technique for wide-band CT MASH ΣΔ ADCs with relaxed filter requirements," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 1486–1489.

[108] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulators," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 40, no. 8, pp. 461–466, Aug 1993.

[109] M. Sanchez-Renedo and S. Paton, "A cascaded CT ΣΔ modulator with NTF zero and simple mismatch tuning method using interstage feedback," in *2007 Ph.D Research in Microelectronics and Electronics Conference*, July 2007, pp. 77–80.

[110] M. Ortmanns, F. Gerfers, and Y. Manoli, "A Case Study on a 2-1-1 Cascaded Continuous-Time Sigma-Delta Modulator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 8, pp. 1515–1525, Aug 2005.

[111] J. Daniels, W. Dehaene, and M. Steyaert, "All-digital differential VCO-based A/D conversion," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, May 2010, pp. 1085–1088.

[112] S. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques," *IEEE Circuits and Systems Magazine*, vol. 2, no. 1, pp. 24–42, First 2002.

[113] R. Fried and C. C. Enz, "Bulk driven MOST transconductor with extended linear range," *Electronics Letters*, vol. 32, no. 7, pp. 638–640, Mar 1996.

[114] T. Kulej and F. Khateb, "Bulk-driven adaptively biased OTA in 0.18 μm CMOS," *Electronics Letters*, vol. 51, no. 6, pp. 458–460, 2015.

[115] S. J. Huang, N. Egan, D. Kesharwani, F. Opteynde, and M. Ashburn, "28.3 A 125MHz-BW 71.9dB-SNDR VCO-based CT ΔΣ ADC with segmented phase-domain ELD compensation in 16nm CMOS," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 470–471.

[116] A. Papoulis, *The Fourier Integral and Its Applications*. McGraw-Hill, 1962.