

Aalto University  
School of Electrical Engineering

Anni Parkkila

# Development of metal contacts for black silicon

Master's Thesis  
Espoo, January 28, 2020

Supervisor: Professor Hele Savin  
Advisor: Iris Mack, PhD



<b>Author:</b>	Anni Parkkila	
<b>Title:</b>	Development of metal contacts for black silicon	
<b>Date:</b>	January 28, 2020	<b>Pages:</b> ix + 58
Department of Electronics and Nanoengineering		
<b>Professorship:</b>	Micro and Nanoelectronics	
<b>Supervisor:</b>	Professor Hele Savin	
<b>Advisor:</b>	Iris Mack, PhD	
<p>Black silicon (b-Si) surfaces have exceptionally good optical properties for applications like solar cells with their reflectivities as low as only <math>\sim 1\%</math>. Conventional contact fabrication methods developed originally for flat silicon surfaces have been shown to result in nonconformal contacts and high contact resistance values on b-Si surfaces, which has led to increased total resistance and decreased solar cell efficiency.</p> <p>This thesis aimed to find optimized sputtering parameters for Ti/Pt/Ag stack to fabricate conformal and good ohmic contacts on b-Si surface, without holes and with contact and line resistance as low as possible. Two different patterning methods, a simple steel shadow mask and lift-off process, were used to produce the desired front metal contacts. Two sputtering parameters, time and power, were varied and the results characterized by Scanning Electron Microscope and Transfer Length Method. The hypothesis was that with lower sputtering power and thus lower sputtering yield, the resulting metal layer would be more conformal on the b-Si structure.</p> <p>The measured values for contact resistance <math>R_c</math> (<math>\sim 450\text{--}620\text{ m}\Omega</math>) and specific contact resistivity <math>\rho_c</math> (<math>\sim 1.27\text{--}2.48\text{ m}\Omega\cdot\text{cm}^2</math>) were in range as compared to planar surfaces reported in literature, which is promising for the b-Si samples that have much higher aspect ratio. Line resistance values were higher as compared to planar surfaces reported in the literature due to the much lower thickness of contacts. By further optimizing the sputtering parameters and thickening the finger structures, it could be possible to achieve conformal, good ohmic contacts and thus, to increase the efficiency of b-Si solar cells.</p>		
<b>Keywords:</b>	black silicon, metallization, solar cell, semiconductor	
<b>Language:</b>	English	

<b>Tekijä:</b>	Anni Parkkila	
<b>Työn nimi:</b>	Metallikontaktien kehitys mustalle piille	
<b>Päiväys:</b>	28. tammikuuta 2020	<b>Sivumäärä:</b> ix + 58
	Elektroniikan ja nanotekniikan laitos	
<b>Professori:</b>	Mikro- ja nanoelektroniikka	
<b>Valvoja:</b>	Professori Hele Savin	
<b>Ohjaaja:</b>	Iris Mack, PhD	
	<p>Mustan piin hyvät optiset ominaisuudet ja alhainen, jopa <math>\sim 1\%</math> heijastuvuus, ovat erityisen hyviä erilaisia sovelluksia kuten aurinkokennoja varten. Tavanomaiset tasaiselle piille tarkoitetut metallointimenetelmät aiheuttavat mustan piin pinnalle epätasaisia metallikontakteja, joilla on korkea kontaktiresistanssi ja sen myötä korkea kokonaisresistanssi, joka johtaa heikompaan aurinkokennon tehokkuuteen.</p> <p>Diplomityön tarkoitus oli löytää optimoidut sputterointiparametrit Ti/Pt/Ag-metalloinnille tasaisen ja hyvän ohmisen kontaktin valmistukseen mustan piin pinnalle niin, että kontakti- ja johdinresistanssi ovat mahdollisimman alhaiset. Mustan piin rakenteet muodostettiin ICP-RIE-kuivaetsauksella. Metallikontaktien muodostukseen käytettiin kahta eri menetelmää, teräksistä shadow maskia sekä optista litografiaa. Sputteroinnissa muokattiin kahta eri parametria, aikaa ja tehoa. Tulokset mitattiin pyyhkäisyelektronimikroskoopilla ja Transfer Length Method -mittauksella. Hypoteesin mukaan matala sputterointiteho johtaisi tasaisempaan metallikerrokseen mustan piin pinnalle.</p> <p>Mitatut arvot kontaktiresistanssille <math>R_c</math> (<math>\sim 450\text{--}620\text{ m}\Omega</math>) ja kontaktiresistiivisyydelle <math>\rho_c</math> (<math>\sim 1.27\text{--}2.48\text{ m}\Omega\cdot\text{cm}^2</math>) olivat linjassa kirjallisuuden kanssa, mikä on lupaavaa mustapiinäytteille, joiden pinta on voimakkaasti kuvioitu verrattuna tasaiseen piihin. Johdinresistanssitulokset olivat korkeampia pienemmän johdinpaksuuden takia. Optimoimalla sputterointiparametreja enemmän ja paksuntamalla metallikontakteja on mahdollista saavuttaa tasaiset, hyvät metallikontaktit ja siten kasvattaa mustapiiaurinkokennojen tehokkuutta.</p>	
<b>Asiasanat:</b>	musta pii, metallisointi, aurinkokenno, puolijohde	
<b>Kieli:</b>	Englanti	

# Preface

This Master's Thesis was the final piece of my studies. I thank my supervisor, Prof. Hele Savin, for giving me the opportunity to work in her research group, for offering me this interesting thesis topic, and for all the guidance and inspiration during the process. I also thank my advisor, Dr. Iris Mack, for always helping me with the experiments and analyzing the results, for great discussions, and for constant interest in guiding my work. I also thank the rest of the Electron Physics Group for their support. The research for the thesis was undertaken at the Micronova Nanofabrication Centre of Aalto University, and I thank everyone who helped me with my research there.

My years as a student at Aalto University have so far been the best in my life. I had the honor to meet many talented and passionate individuals during classes, parties and events, and especially during volunteering activities in the Guild of Electrical Engineering and the Aalto University's Student Union. I will always cherish every laughter, tear, hug and love shared with the amazing people in the Aalto community. During my exchange studies in 2018 at the Tokyo Institute of Technology, Japan, I learned that even while living alone on the other side of the world, things will always eventually work out. I miss my time in Japan dearly and all the people I befriended there, and I cannot wait to get back there again!

There is no way I could express enough gratitude for everyone I have met and everything that has happened during these years. I wholeheartedly thank Miika and Erna for being such invaluable friends and for all the crazy things we got to experience. I sincerely thank all the groups I have been part of, HTMK'013, JTMK'14, Polyteekkarimuseo, SIKH'16, FTMK'16, and TPTMK'17. Special thanks go to Joutomiehet for not ruining my studies but instead for being the best roommates one can hope for; The Guild of



Electrical Engineering and all its members for making me feel at home and introducing me to the Teekkari life; TPTMK'19 for being the most awesome committee I could ever have hoped for; TJ'19 for being the best kind of support and diversion with all the fun events and activities during the writing process of this thesis, and simply for giving me the opportunity to have the most satisfying "end" for my life as a student.

I would also like to thank my family, my mother Anne and brothers Taneli, Tommi and Aleksi for always supporting me. My final thanks go to Joni, for being my biggest supporter in life for many years, for helping me through all the moments I struggled with L<sup>A</sup>T<sub>E</sub>X, for coping with me when I barely had time to be at home in my busiest moments, and for constant love and help with everything I could ask for.

May all the future students have as "full blast" amount of fun as I did during my studies and life as a Teekkari. Jappadaida and Iuvenis in Aeternum!

Tekniikan kehhdossa, 28.1.2020

Anni Parkkila

"Suomessa kaikki hullut saavat valkoisen lakin.  
Kaheleimmat heistä merkitään tupsulla."

# Abbreviations and symbols

## Abbreviations

Al	Aluminum
Ag	Silver
b-Si	Black silicon
DI-water	Deionized water
FF	Fill Factor
HF	Hydrofluoric acid
ICP-RIE	Inductively Coupled Plasma - Reactive Ion Etching
MACE	Metal-Assisted Chemical Etching
MEMS	Microelectromechanical systems
N <sub>2</sub>	Nitrogen
Ni	Nickel
O <sub>2</sub>	Oxygen
Pd	Palladium
PIII	Plasma Immersion Ion Implantation
PLD	Pulsed Laser Deposition
POCl <sub>3</sub>	Phosphorus Trichloride
Pt	Platinum
PVD	Physical Vapor Deposition
SEM	Scanning Electron Microscope
SF <sub>6</sub>	Sulfurhexafluoride
Ti	Titanium
TLM	Transfer Length Method

## Symbols

$d$	Contact spacing
$I_{IN}$	Input current
$I_{MP}$	Current at the maximum power point
$I_{OUT}$	Output current
$I_{SC}$	Short-circuit current
$L_T$	Transfer length
$P_{max}$	Maximum output power
$P_{MP}$	Maximum power point
$R$	Resistance
$R_c$	Contact resistance
$R_m$	Metallic conductor resistance
$R_{semi}, R_{sh}$	Semiconductor sheet resistance
$R_T$	Total resistance, series resistance
$V$	Voltage
$V_{MP}$	Voltage at the maximum power point
$V_{OC}$	Open-circuit voltage
$Z$	Contact width
$\eta$	Efficiency
$\rho_c$	Specific contact resistivity

# Contents

Preface	iv
Abbreviations and symbols	vi
<b>1 Introduction</b>	<b>1</b>
<b>2 Theory and background</b>	<b>4</b>
2.1 Solar cell structure . . . . .	4
2.2 Total resistance losses of the front metal contacts . . . . .	6
2.2.1 Contact resistance $R_c$ losses at the metal-semiconductor interface . . . . .	8
2.2.2 Metallic conductor resistance $R_m$ . . . . .	9
2.3 Black silicon . . . . .	10
2.4 Black silicon metallization methods in literature . . . . .	12
2.4.1 Screen-printing . . . . .	13
2.4.2 Evaporation . . . . .	16
2.4.3 Sputtering . . . . .	18
<b>3 Experimental</b>	<b>22</b>
3.1 Sample fabrication and process flow . . . . .	22
3.1.1 RCA cleaning . . . . .	24
3.1.2 Inductively coupled plasma reactive-ion etching (ICP- RIE) . . . . .	24
3.1.3 Emitter implantation . . . . .	25
3.1.4 Shadow mask . . . . .	26

3.1.5	Lift-off . . . . .	28
3.1.6	Sputtering Ti/Pt/Ag . . . . .	30
3.2	Characterization methods . . . . .	32
3.2.1	Scanning Electron Microscope (SEM) . . . . .	32
3.2.2	Transfer Length Method (TLM) . . . . .	33
<b>4</b>	<b>Results &amp; discussion</b>	<b>36</b>
4.1	Scanning Electron Microscope results . . . . .	36
4.2	Resistance measurements . . . . .	44
4.2.1	Contact resistance . . . . .	45
4.2.2	Finger line resistance . . . . .	48
<b>5</b>	<b>Conclusions</b>	<b>52</b>
	<b>References</b>	<b>58</b>

# Chapter 1

## Introduction

More than 80% of commercial solar cells utilize silicon as their base material.[1] Unfortunately, bare silicon has a very high reflection rate of over 30%, causing optical losses in solar cells.[2] These optical losses heavily affect the power received from the solar cell because of the lowered short-circuit current. As light is reflected from the surface, it does not generate electron-hole pairs, which are essential for creating the current and thus power of the solar cell. One of the most used ways to reduce these optical losses is to use anti-reflection coatings, which are thin layers of dielectric material.[2] Most common anti-reflection coating is silicon nitride.[1] Another way to reduce reflection is to modify the surface of the silicon by etching, for example, to create micro- and nanoscale patterns that reduce the reflective effects.[1, 2] The most common and also industrially used method is to create microstructures on silicon by chemical etching, which leads to pyramid-like structures.[2]

Black silicon (b-Si) is a more recently developed method to reduce reflection losses. It consists of nanostructured silicon material with high aspect ratio and needle-like structures.[3] B-Si has been given a lot of attention in research and has already been industrialized, and it is an advantageous material for solar cell fabrication for its low reflectance properties.[3] Reflectivities as low as only  $\sim 1\%$  over a wide range of visible light have been observed with black silicon surfaces.[1] In recent years black silicon has been studied for solar cell applications to find a highly efficient way of produc-

## CHAPTER 1. INTRODUCTION

ing power from solar cells. Other applications like silicon microreactors for chemical and biological applications [4] and photodiodes [5] can also benefit from nanostructured b-Si surfaces.

However, black silicon has some issues that are all related to the black silicon surface structure. Firstly, the enlarged surface area results in increased surface recombination.[3] Secondly, doping tends to be heavier or non-uniform at the b-Si surface, which leads to Auger recombination and shunts.[3] Lastly, it's hard to form uniform metal contacts on black silicon surface, as the metal is usually mostly deposited only on top of the nanostructure and does not reach the valleys of the structures, leaving air pockets in the structure.[6] These poor contacts lead to higher resistivities.[3]

In this thesis ways to develop better metal contacts by sputter deposition are investigated. Sputtering is a widely used method of metallization and there has been some research done before to use it on black silicon also. However, results so far have been similar to other methods, like screen-printing, meaning that the bottoms of the black silicon valleys are not reached by the metal.[4] However, many of the previous research papers have not reported the sputtering parameters that have been used nor did they report any optimization of the parameters and therefore the contacts. In this master's thesis, the goal was to change some of the sputtering parameters, like sputtering time and power, to find the optimal way to also fill the bottoms of the valleys. The hypothesis was that with lower power, which is equal to reduced sputtering rate, and longer sputtering time, the b-Si nanostructures will not get blocked as quickly at the top and the material has more time to reach the bottom of the valleys as well. Both a shadow mask and a lift-off method were used to create the metal contact patterns. The sputtering results were studied both by taking high magnification SEM images of the contacts as well as by electrical measurements. Reaching a low contact resistance  $R_c$  and thus better contact between the metal and the black silicon was the main goal of this thesis. An additional aim was to thoroughly investigate literature for previous research done in black silicon metallization.

Finally, the structure of the thesis is introduced. Chapter 2 describes theory of solar cells, black silicon and electrical losses caused by the front

## *CHAPTER 1. INTRODUCTION*

metal contacts, as well as summarises previous research done in the field of black silicon metallization and contact fabrication. The chapter is divided by the methods that have been used before. Each section briefly explains each method and presents the results from previous studies. Standard and also industrial relevant methods like screen-printing, evaporation, and sputtering are investigated. Chapter 3 explains the process flow and sample fabrication methods used for this thesis. Methods include substrate cleaning, black silicon etching and sputtering of the metal contacts. After this, the utilized characterization methods, Scanning Electron Microscope and Transfer Length Methods, are explained shortly. In Chapter 4 the contact resistance results and SEM images are analyzed and discussed. Chapter 5 summarizes the thesis and thoughts for further research are provided.



## Chapter 2

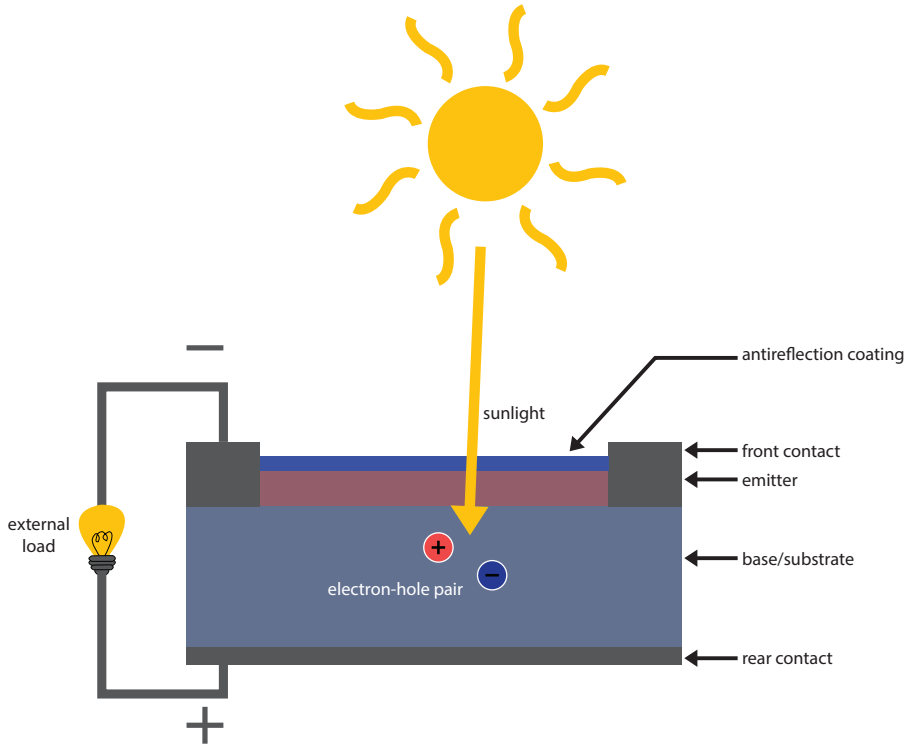
# Theory and background

### 2.1 Solar cell structure

A solar cell is an electronic device that converts sunlight into electricity. The incoming photons are absorbed by the solar cell and raise electrons in the material to a higher energy state. These electrons with higher energy move to an external circuit to dissipate their energy, creating current and voltage, and return back to the solar cell.[2] Figure 2.1 depicts a very basic cross-sectional structure of a conventional solar cell with grid-like front contacts and larger rear contact, as well as an antireflection coating on top of the emitter to prevent the sunlight from reflecting from the solar cell surface and therefore to enhance absorption. An alternative to using an antireflection coating is nanostructuring of silicon, like black silicon, which is introduced in Section 2.3 Black silicon.

Efficiency is the most commonly used parameter to compare the performance of solar cells with each other. Efficiency  $\eta$  is defined as the ratio of energy output from the solar cell to input energy from the sun. Efficiency depends on the spectrum and intensity of the incident sunlight and the temperature of the solar cell. In addition to these, efficiency is highly dependant on the performance of the solar cell itself.[2] The quality of the front metal contacts plays a crucial role as all metal contacts have resistance, consisting of contact resistance between the metal-semiconductor interface and the

## CHAPTER 2. THEORY AND BACKGROUND



**Figure 2.1:** *Cross-sectional illustration of a basic solar cell. The basic structure utilizes an antireflection coating on flat silicon substrate with doped emitter in between the base and the antireflection coating. Solar cells have contacts both on the front and rear side.*

resistance along the finger structures. Thus, the quality of the front metal contacts and their resistance values also affect the efficiency.[7] In principle, solar cells require both rear and front contacts. The rear contacts often cover the whole backside of the cell, but the front contacts are structured in a grid-like shape to minimize shadowing. The size and the space of the grid needs to be optimized to maximize the solar cell absorption and at the same time to maximize the collection of free electrons.[2] As mentioned, the resistance properties affect the efficiency of the whole device so it's important to optimize the contacts so that the total resistance is as low as possible.[7]

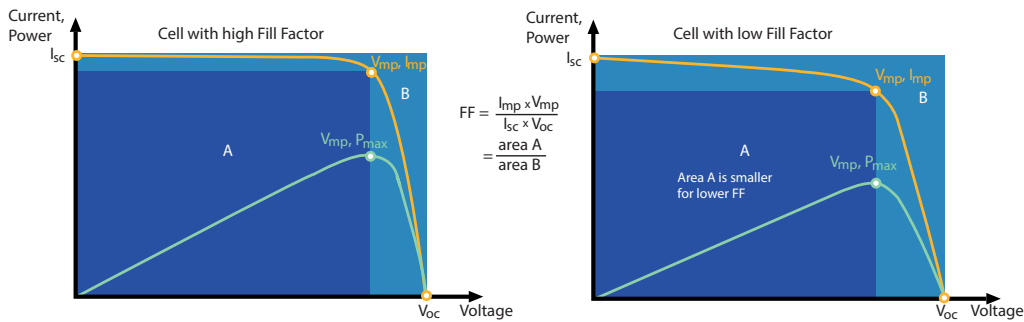
Another parameter that can be measured from solar cells is the Fill Factor (FF).[2] It is defined as the ratio of the maximum power  $P_{MP}$  from a solar

## CHAPTER 2. THEORY AND BACKGROUND

cell to the product of open-circuit voltage  $V_{OC}$  and short-circuit current  $I_{SC}$  so that

$$FF = \frac{P_{MP}}{V_{OC} \times I_{SC}} \quad (2.1)$$

At one sun, for a typical silicon commercial solar cell the maximum FF is around 0.83. The FF values differ for different materials, for example, a GaAs solar cell may have a FF approaching 0.89. Both shunt and series resistance losses decrease the Fill Factor and efficiency of a solar cell. Graphically, the FF is a measure of the "squareness" of the solar cell and is also the area of the largest rectangle that will fit in the IV-curve. A theoretical example of FF and IV-curve is shown in Figure 2.2.[2]



**Figure 2.2:** Graph of cell output current (orange line) and power (green line) as a function of voltage. Also shown are the cell short-circuit current ( $I_{sc}$ ) and open-circuit voltage ( $V_{oc}$ ) points, as well as the maximum power point ( $V_{mp}, I_{mp}$ ). On the left is an example of a cell with high FF and on the right is with low FF.[2]

## 2.2 Total resistance losses of the front metal contacts

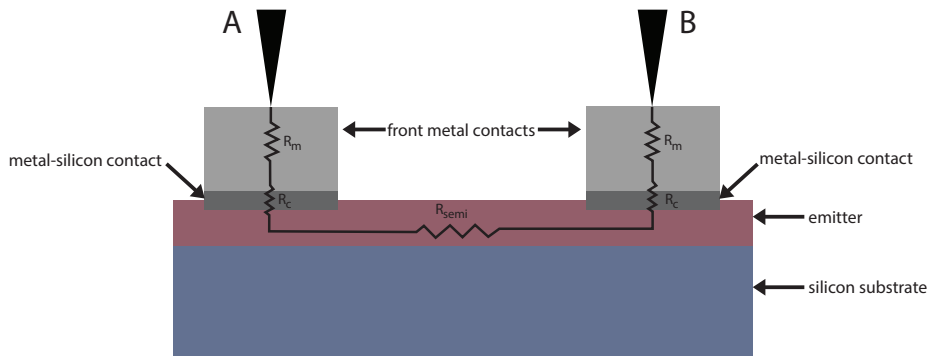
All semiconductor devices have contacts and in general, the contacts are mostly metal-semiconductor contacts. All contacts have contact resistance  $R_c$  and thus measuring and characterizing the contact resistance is important as it also affects the total resistance, also known as the series resistance,

## CHAPTER 2. THEORY AND BACKGROUND

and thus the efficiency and performance of the whole device.[7] The metal contacts also have their own resistance  $R_m$  which affects the total resistance and the conductivity along the finger lines of the front contacts.[2, 7] The main impact of series resistance is to reduce the Fill Factor. Thus, both the contact resistance  $R_c$  and the metal conductor resistance  $R_m$  decrease the Fill Factor.[2] Because of that, the Fill Factor is a good reference value when comparing different kinds of front metal contacts on solar cells.

Ohmic contacts have either linear or quasi-linear current-voltage characteristics. The basic principle is that the contacts must be able to supply the necessary device current. Also, the voltage drop across the contacts must be small compared to the voltage drops across the active device regions. In addition to this, the contacts should not degrade the device significantly, for example by decreasing the output power.[7, 8]

The current flows either vertically or horizontally into the contact and thus the effective contact area may differ from the true contact area. The total resistance between two points A and B having metal contacts can be divided into three components, which are the resistance of the metallic conductor  $R_m$ , the contact resistances  $R_c$  and the semiconductor sheet resistance  $R_{semi}$ , as depicted in Figure 2.3. The sheet resistance of the semiconductor for solar cells typically range from 30 to 100  $\Omega/\square$ .[8]



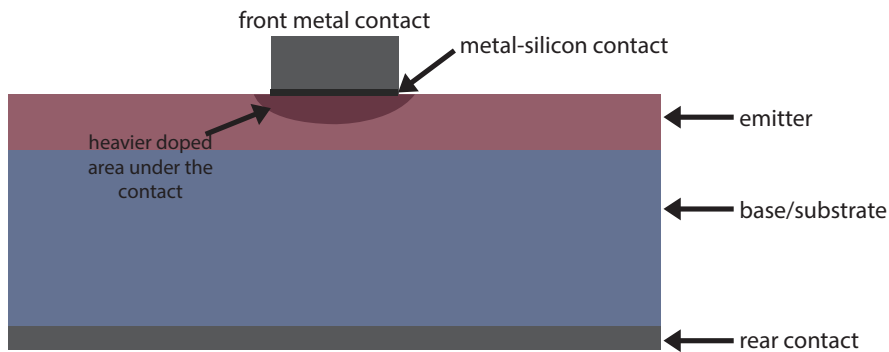
**Figure 2.3:** A schematic of two contacts to a diffused semiconductor layer, with the metal conductor resistances, the contact resistances and the semiconductor resistance indicated.

Thus, the total resistance  $R_T$  between A and B is

$$R_T = 2R_m + 2R_c + R_{semi} \quad (2.2)$$

### 2.2.1 Contact resistance $R_c$ losses at the metal-semiconductor interface

In this section, the basics of contact resistance characteristics are explained. The method to measure contact resistance is introduced later in Section 3.2.2 Transfer Length Method (TLM). Contact resistance losses occur at the interface between the semiconductor substrate (usually silicon) and the metal contact. One way to lower the contact resistance is by heavier doping under the contacts, as seen in Figure 2.4. Doping is a technique used to vary the number of electrons and holes in semiconductor to increase the conductivity of the material.[2]



**Figure 2.4:** Lower contact resistance can be achieved by heavier doping under the front metal contacts. Contact resistance losses occur at the interface of the metal contacts and the semiconductor.

However, it is necessary to note that the contact resistance is not very clearly defined. It is characterized by two quantities, which are the contact resistance  $R_c$  ( $\Omega$ ) and the specific contact resistivity  $\rho_c$  ( $\Omega\cdot\text{cm}^2$ ). Portions of the metal immediately above and the semiconductor below the metal-semiconductor interface, as well as any current crowding effects or any in-

## CHAPTER 2. THEORY AND BACKGROUND

terfacial oxide layer between the metal and semiconductor, are also part of the contact resistance.[7] The contact between the metal contacts and the semiconductor may also depend on the type of the emitter doping on the wafer and thus should be taken into account when analyzing the measurement results.[9]

Contact resistance values are often not reported in research regarding black silicon metallization. Despite this, contact resistance, along with the metal layer conformality, was chosen as the most important characteristic to measure the quality of the ohmic contacts. By measuring the contact resistance it was possible to determine how well the chosen deposition method and parameters worked for creating good metallic contacts on the nanostructured silicon surface and how promising the contacts are for operating the device.

### 2.2.2 Metallic conductor resistance $R_m$

The front metal contacts themselves also have their own resistance,  $R_m$ , which affects the total resistance. It also has an effect on line resistance along the fingers and grid resistance of the front contact finger pattern.[2, 7] Thus, it also affects the Fill Factor.[2] The front contact resistance depends on the metal used, its deposition method and geometry.[8] When discussing finger line resistance, it's often presented in the form of resistance divided by the finger length,  $\Omega/\text{cm}$ .

Table 2.1 presents reference values of front contact metallization measured on flat silicon solar cells.[10] Even though these values are from non-texturized silicon surfaces, they still provide a good reference and target values for contacts formed on black silicon samples. In this thesis, however, especially the contact resistance  $R_c$ ,  $\rho_c$  and line resistance values are of interest.

Schroder et al. defined in their study that for solar cells in general, the specific contact resistivity  $\rho_c$  should be  $\leq 2 \text{ m}\Omega\cdot\text{cm}^2$ . [8] Even if the contact resistance or the line resistance is good, the overall performance can still be

bad. This is because the contact resistance takes only the vertical resistance into account, and the line resistance takes only the horizontal as long as there is a continuous film. Therefore, in order to get good FF and efficiency values, it is necessary to have both contact resistance and line resistance as small as possible.

**Table 2.1:** Reference values of front contact metallization measured on flat silicon.  $\rho_c$  means the specific contact resistivity. [10]

Parameter	Screen-printed	Photolithography
finger thickness ( $\mu\text{m}$ )	14	8
finger width ( $\mu\text{m}$ )	80	20
$\rho_c$ ( $m\Omega\cdot\text{cm}^2$ )	0.3–3	0.01
metal resistivity ( $\mu\Omega/\text{cm}$ )	3	1.7
Fill Factor	0.74–0.77	0.81–0.82

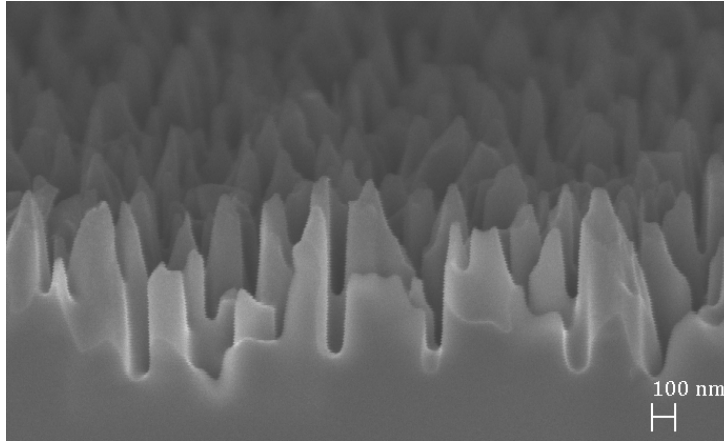
## 2.3 Black silicon

Black silicon is defined as nanostructured silicon such that the surface appears completely black. This nanostructuring is formed through etching, appearing as nano-scale needle-like structures [3], as shown in Figure 2.5.

Black silicon is an attractive material for solar cell applications as it has superior low reflectance properties [3], and reflectivities as low as only  $\sim 1\%$  have been observed for black silicon surfaces.[1] There are several methods of fabricating the black silicon nanostructures, including dry etching methods like Inductively Coupled Plasma Reactive-Ion Etching (ICP-RIE) and wet etching methods like Metal-Assisted Chemical Etching (MACE).[1]

Using black silicon causes issues that are all related to the black silicon surface structure. Firstly, one issue is that the large surface area of black silicon results in increased surface recombination velocity.[3, 6] Secondly, emitter doping is usually heavier or non-uniform at the b-Si surface, which causes Auger recombination and shunting.[3] Lastly, forming uniform metal contacts on black silicon is difficult as the metal tends to be deposited only on the top

## CHAPTER 2. THEORY AND BACKGROUND

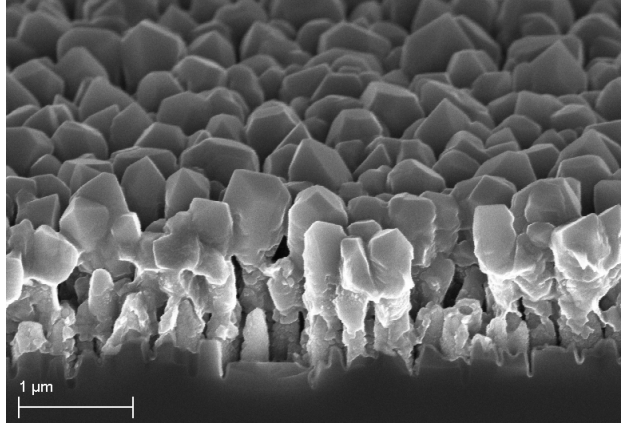


**Figure 2.5:** *Cross-sectional image of black silicon nanostructuring on silicon substrate. Image was taken with a scanning electron microscope (SEM) with magnification of 80 000. These structures were fabricated with Inductively Coupled Plasma Reactive-Ion Etching (ICP-RIE).*

of the nanostructures and does not reach the valleys of the structures, leaving air pockets in the structure.[6] An example of this phenomenon is shown in Figure 2.6, which has aluminum on black silicon by sputter deposition. The sputtering parameters optimized for flat silicon surfaces are not optimized for b-Si surfaces, leading to uneven metal layers as seen in Figure 2.6. Poor, nonconformal contacts are likely to lead to higher resistivities.[3, 6]

Black silicon is proving to be a very promising material especially for solar cells due to its low reflectance, but also other applications have been studied. For example, Roumanie et al. studied the use of black silicon for enhancing surface activity in silicon microreactors for chemical and biological applications.[4] The amplification of the surface activity was measured to be at least a factor of 10.[4] B-Si nanostructuring has also been offered as a solution for enhancing the collection efficiency of photodiodes for photon detection, to improve data quality, reduce the area of photodiodes and to decrease the cost per pixel.[5] Regardless of the application, all semiconductor devices need conformal good quality metal contacts.





**Figure 2.6:** *Cross-sectional image of non-optimized sputtered aluminum on black silicon structures. Because of the nanostructure of black silicon, it's difficult to form uniform metal layers on top of it. The material doesn't reach the bottom of the black silicon valleys which is likely to cause higher series resistance. Additionally, the sputtering result is quite angular and not a smooth layer of metal.*

## 2.4 Black silicon metallization methods in literature

In this section, the most popular methods of black silicon metallization (screen-printing, evaporation, and sputtering) and previous results are introduced. All of these methods are applicable on flat silicon surfaces as well and are widely used. Especially screen-printing is used already in industrial solar cells, evaporation and sputtering are widely used in research purposes for solar cell fabrication. Sputtering is also an industrially standard method for metal contact formation for example in Integrated Circuit, Microelectromechanical systems (MEMS) and Photodetector device fabrication.

All contacts have contact resistance and sheet resistance of the metal, and lowering both types of resistance losses is important as they also affect the total resistance and thus the efficiency and performance of the whole device.[7]

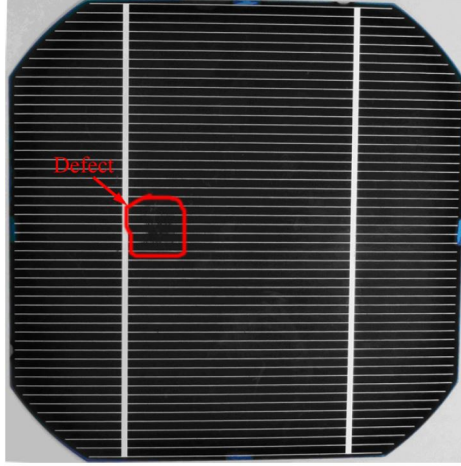
### 2.4.1 Screen-printing

Screen-printing is one of the most widely used fabrication technology in solar cell manufacturing.[2] It was first developed already in the 1970s. A screen with patterning is used along with metal paste, which is then dragged along the surface, forcing the metal paste through the holes of the screen and onto the sample. Both back and front contact are fabricated this way but they have a different patterning as the contacts on the front side don't cover the whole surface but have a grid-like structure. The paste is then baked afterward to solidify the metal.[2] The biggest advantages of screen-printing are its relative simplicity and cost-efficiency.[2, 10] Disadvantages are that screen-printed contacts have been typically quite wide, 125–150  $\mu\text{m}$  which has led to high shading losses. Also, the Fill Factor values often tend to be quite low ( $\sim 0.75$ ) because of high contact resistance, low metal conductivity, and junction shunting.[10] There are several processes and variations to the screen-printing technique.[2]

On black silicon screen-printed contacts have not lead to very high efficiencies. Yoo et al. reported efficiencies of 11.7% on mono-crystalline and 10.2% on multi-crystalline black silicon.[11] The achieved FF values were 0.73 and 0.72, respectively, which are not very high. In their study, Ag paste was used for creating the front metal contacts. However, they didn't report how well the contacts were formed and if the efficiency difference between the two cells can be explained by bad contacts.[11]

Xia et al. reached a higher efficiency of 15.68% with 0.783 Fill Factor in their black silicon cells.[12] They reported a lower conversion and quantum efficiency of the black silicon cell compared to a conventional cell, which they explained to be caused by higher doping concentration. Also, the b-Si cell showed larger series resistance and smaller shunt resistance (8.5  $\text{m}\Omega$  and 9.34  $\text{m}\Omega$ , compared to 6.67  $\text{m}\Omega$  and 24.86  $\text{m}\Omega$  in the reference cell), which suggests poor contact between the metal and wafer. On the solar cell, they saw a defect, shown in Figure 2.7 interrupting the grid fingers, leading to lower quality of the metallic contact.

Black silicon was reported to have superhydrophobic properties, which



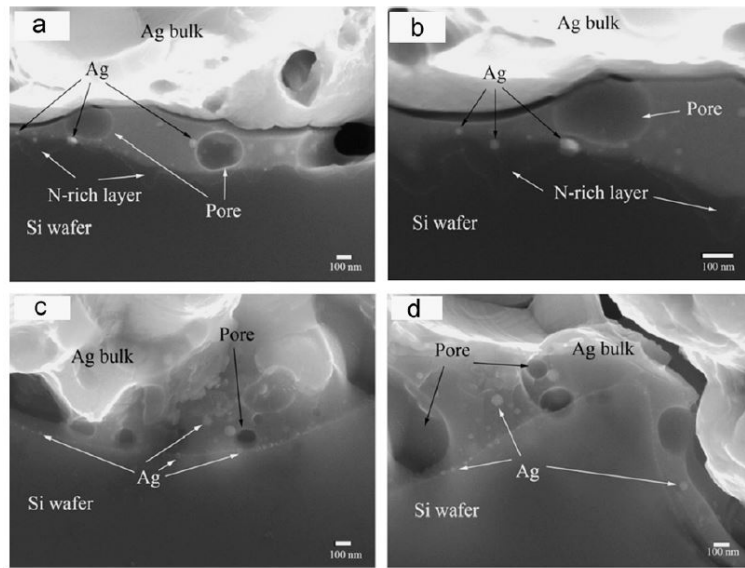
**Figure 2.7:** *The defect in Xia et al. sample on the front electrode of black silicon cell.[12]*

can lead to a defect in the front electrode during the screen-printing process. Thus, Xia et al. stated that improving the front contact process could lead to better conversion efficiency.[12] SEM images or other characterization methods of the formed metal contacts were not shown in their results.

Zhong et al. fabricated black silicon wafers by Plasma Immersion Ion Implantation (PIII) with Ag screen-printed front contacts.[13] As a reference, they used acid textured solar cells for characterization. Their highest efficiency value from PIII structured wafer was 15.99% with FF of 0.7644. However, the acid textured reference solar cell achieved higher FF of 0.7906 and efficiency 16.59%. This was due to the higher series resistance of the PIII cell (4.31 m $\Omega$ ) compared to the acid textured (2.43 m $\Omega$ ). The higher series resistance in PIII cells was caused by worse contacts. SEM images are shown in Figure 2.8.

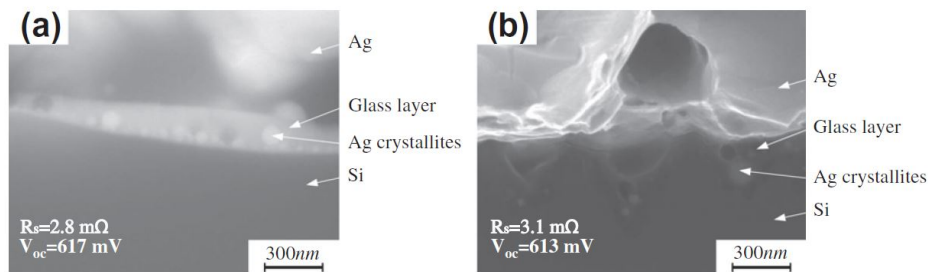
Images (a) and (b) in Figure 2.8 show the contact formation on the PIII textured cell at the silicon-Ag interface. The remaining N-rich layer there is believed to lead to a bad current transmission with high contact resistance whereas images (c) and (d) show no N-rich layer on the acid textured cell. The fine distribution of Ag crystallites in the acid textured cell is believed to lead to low contact resistance.[13] The contact resistance values were not reported.

CHAPTER 2. THEORY AND BACKGROUND



**Figure 2.8:** Cross-sectional SEM images of Ag-Si contact of the solar cells. (a) and (b) PIII textured, (c) and (d) acid textured.[13]

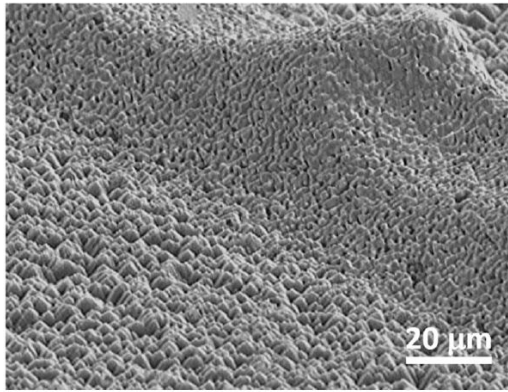
Liu et al. also used PIII textured cells with acid textured cells as a reference with Ag screen-printed contacts in their work.[14] The PIII textured cells achieved an FF value of 0.776 and an efficiency of 16.3%. The acid textured had FF 78.0 and efficiency 16.0%. Figure 2.9 (a) shows that a uniform glass layer was formed between the acid textured emitter and the Ag grid. This could lead to good ohmic contacts and high FF. However, image (b) shows that the glass layer between PIII textured cell and Ag grid is non-uniform and leads to higher series resistance.[14] Contact resistance values were not reported.



**Figure 2.9:** SEM images of the Ag-Si interfaces of (a) acid textured cell and (b) PIII textured cell.[14]

## CHAPTER 2. THEORY AND BACKGROUND

Putra et al. combined pyramid structures with nanopores and used screen-printed Ag contacts on their cells.[15] Their best nanopore/pyramid structured cell achieved an efficiency of 18.78% and FF 0.7859. This was slightly better compared to their reference cell, which was textured only with the pyramids. The reference cell achieved 18.18% efficiency and 0.7851 FF value. Figure 2.10 shows a side view of the Ag grids in contact with underlying hierarchical textures prepared with 8 minutes of catalytic etching for nanopore formation.[15] Contact resistance values were not reported in this study.



**Figure 2.10:** Side-view SEM image of Ag grid in contact with underlying hierarchical nanopore textures.[15]

Cabrera et al. studied how the size and sharpness of pyramid-like structures on silicon affect the specific contact resistivity and FF values with screen-printed Ag contacts.[16] They noticed that rounded or smaller pyramids increased the specific contact resistivity and decreased FF values. Their best combination was  $\rho_c$  1.2 m $\Omega$ ·cm<sup>2</sup> and FF 0.799 with efficiency of 17.9% for their standard height pyramids.[16]

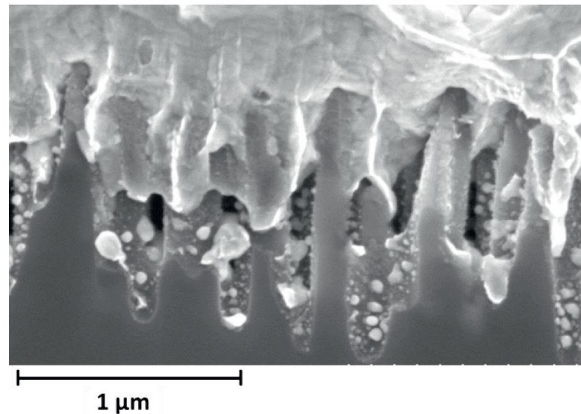
### 2.4.2 Evaporation

Physical Vapor Deposition (PVD) methods, like evaporation, sputtering and pulsed laser deposition, are commonly used for thin-film deposition. Evaporation is a fairly straightforward method. Metals are heated, for example, by

## CHAPTER 2. THEORY AND BACKGROUND

electron beam or thermal heating in a high vacuum. Metal atoms evaporate from the target surface and sublimate onto the substrate surfaces, as well as chamber walls. Uniform films can be produced by rotating the substrate. The electron beam can vaporize even high-melting-point and refractory metals like tungsten, however, the deposition rates are very low.[17]

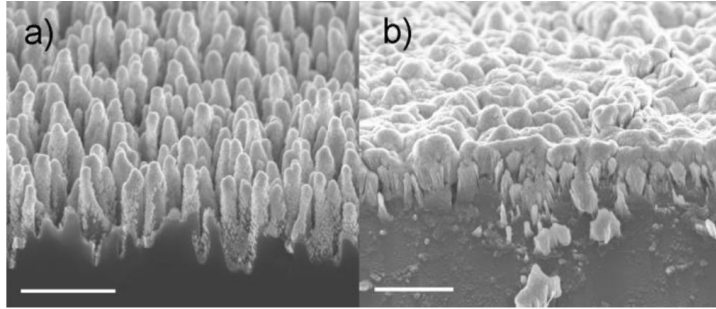
Evaporation is a widely used method for making the metal contacts (fingers and busbars, as well as rear contacts) of solar cells in research laboratories. In a study by Repo et al., they investigate n-type solar cells with black silicon texturing on the front.[6] The front surface grid was first defined by photolithography, then the contacts were formed by evaporation of Ti/Pd/Ag and finally thickened with electroplated Ag. The efficiency of the solar cell was 18.7%, although they claimed it could be higher with some process optimization. FF was 0.758. A cross-sectional SEM image (Figure 2.11) of the created contacts revealed that the metal contacts do not completely reach the valleys and gaps of the b-Si surface. This might lead to an increased series resistance.[6]



**Figure 2.11:** A SEM image of the black silicon and front metal contact interface, from the work by Repo et al., showing how the metal is mostly deposited on the nanostructure and does not reach the valleys of the structure.[6]

Von Gastrow et al. investigated 100–400 nm thick nickel and aluminum contacts of 1 μm on boron-doped black silicon.[18] Both contact materials were deposited by e-beam evaporation with low deposition rates of 0.1–0.5 nm/s. Specific contact resistivity was measured with the Transfer Length

Method. SEM images showed that nickel is covering the needles conformally but not all the way to the bottom of the valleys between them, as seen in Figure 2.12. Already 250 nm of nickel was enough to cover the needed structures of black silicon completely.



**Figure 2.12:** SEM images of b-Si structures from the work by von Gastrow et al. Metallization was done by electron gun evaporation with a) 100 nm of nickel and b) 250 nm of nickel. The scale bars represent 1  $\mu\text{m}$ . [18]

Ni contacts on b-Si without post-deposition annealing were able to reach specific contact resistivity results down to  $0.3 \text{ m}\Omega\cdot\text{cm}^2$ . The Al contacts reached the same value with  $400 \text{ }^\circ\text{C}$  annealing. [18] As Schroder et al. defined in their study that for solar cells in general, the specific contact resistivity  $\rho_c$  should be  $\leq 2 \text{ m}\Omega\cdot\text{cm}^2$  [8], implies that the results by von Gastrow et al. are very promising. Efficiency or FF values were not reported.

Oh et al. managed to fabricate black silicon solar cells with an 18.2% efficiency rate. In their solar cells, the front metal contacts were first formed by photolithography and etching in dilute HF. Next, the contact grid was formed by e-beam evaporation of Ti/Ag/Pd and lift-off process. However, the evaporation results or contact resistance were not reported. [19]

### 2.4.3 Sputtering

Sputtering is the most important PVD method as it is widely used in the semiconductor industry to fabricate metal contacts on devices like MEMS, photodetectors and transistors. During sputtering argon ions from a glow discharge plasma are used. The ions hit a negative target and eject one or

## CHAPTER 2. THEORY AND BACKGROUND

more target atoms backward. These ejected atoms are then transported to the substrate. Magnetron sputtering is mainly used, as the magnet behind the target creates a field, confining the electron movement and thus ionization is much more efficient. A vacuum is utilized during sputtering and the sputtered atoms can experience many collisions before arriving onto the substrate. Collisions with argon gas lead to cooling down and reduce the energy of particles that reach the substrate and also reduce the flux of particles to the substrate. Lower flux means lower deposition rate, but at the same time, less re-sputtering of the created film. Sputtering yield is the number of target atoms ejected per incident ion, and its value depends on the target material.[17] Some of the parameters can be changed to alter the sputtering results. In this thesis, the changed parameters were the sputtering power and sputtering time, although changing of argon flow and therefore the working pressure could be considered too.

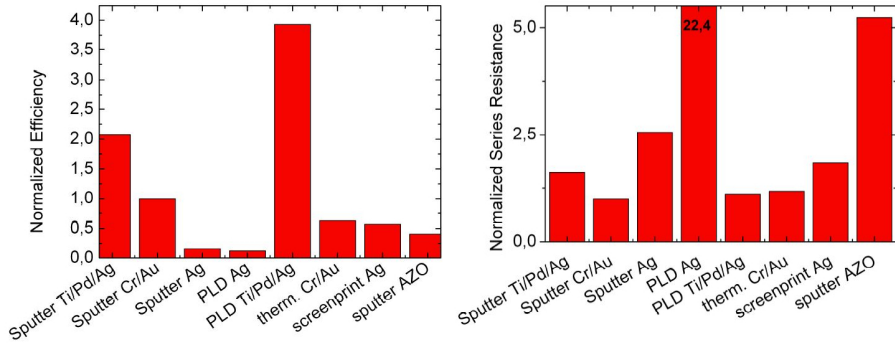
Metal contact formation by sputtering on nanostructured material has been studied several times in previous research.[4, 20] So far, sputtering has not proven to be an optimal way for fabricating the contacts for nanostructured silicon. However, this could be due to using the standard sputtering recipes which work well on flat silicon but which are not optimized for the nanostructured surface of black silicon. In the case of black silicon, the main issue is that the sputtered metal forms a layer only on top of the b-Si structures leaving the valleys open and the layer nonconformal.[4] It's difficult to confirm with SEM if the materials are deposited on the bottom of the valleys, but Roumanie et al. confirmed in their research by utilizing an energy dispersive X-ray probe for elementary analysis that some platinum was also deposited on the valley bottom.[4] However, the gaps are likely to cause conductance problems and increase the total resistance.[3]

Gimpel et al. compared contact materials and deposition methods on sulfur hyperdoped black silicon.[20] Deposition methods included screen-printing, sputtering, pulsed laser deposition (PLD) and thermal evaporation. For screen-printing of the front contact, silver paste was used. Comparing the results they found that the normalized efficiency for screen-printed Ag was  $\sim 0.6$ , whereas for PLD and sputtered contacts made of the multilayer



## CHAPTER 2. THEORY AND BACKGROUND

stack Ti/Pd/Ag the normalized efficiency was higher,  $\sim 3.9$  and  $\sim 2.1$ , respectively. Also, the normalized series resistance of sputtered contacts were slightly higher ( $\sim 1.5$ ) compared to PLD ( $\sim 1.1$ ). Screen-printed Ag contacts had slightly higher normalized series resistance, roughly  $\sim 1.6$ . [20] The values are estimated from the Figure 2.13. Their study did not report SEM, contact resistivity or FF results.



**Figure 2.13:** Normalized efficiency and series resistance values of the different metallization methods. [20]

Sputtering as a deposition method is important both in research and widely used in the semiconductor industry. However, there hasn't been much research on sputtering on black silicon nanostructures and the few previous studies have not been that successful. This is most likely due to using standard sputtering recipes, which are used on flat silicon but are not optimized on nanostructured surfaces. For these reasons sputtering was chosen as the method of metal deposition in this thesis by changing and trying to optimize the sputtering parameters for black silicon.

To summarize Section 2.4, Table 2.2 presents some key values found in literature on black silicon metallization. Most of the results presented here are found from studies that used screen-printed silver front contacts and three studies used evaporation. However, only two of these studies reported contact resistivity values. Fill Factor and efficiency values were reported in all studies, except one. FF values ranged between 0.72 and 0.799, and efficiencies between 10.2% and 18.78%.

## CHAPTER 2. THEORY AND BACKGROUND

Unfortunately, neither Roumanie et al.[4] or Gimpel et al.[20] reported contact resistance or FF values for their sputtered metal contacts. Also, as the efficiency and series resistance values reported by Gimpel et al. were normalized values, they were not comparable to the other studies on b-Si metallization. However, based on the normalized values in the study by Gimpel et al.[20], sputtered front metal contacts could prove promising with optimization, as they had similar or better results compared to screen-printed contacts, as seen in Figure 2.13.

**Table 2.2:** *Summary of results found in literature on b-Si metallization.*

Method	Metal	Doping	$\rho_c$ ( $m\Omega \cdot cm^2$ )	FF	Efficiency (%)	Ref.
Screen-printing	Ag	POCl <sub>3</sub>	–	0.73	11.7	[11]
Screen-printing	Ag	POCl <sub>3</sub>	–	0.72	10.2	[11]
Screen-printing	Ag	POCl <sub>3</sub>	–	0.783	15.68	[12]
Screen-printing	Ag	POCl <sub>3</sub>	–	0.76	15.99	[13]
Screen-printing	Ag	POCl <sub>3</sub>	–	0.776	16.3	[14]
Screen-printing	Ag	POCl <sub>3</sub>	–	0.7859	18.78	[15]
Screen-printing	Ag	POCl <sub>3</sub>	1.2	0.799	17.9	[16]
Evaporation	Ti/Pd/Ag	Boron	–	0.758	18.7	[6]
Evaporation	Ni, Al	Boron	0.3	–	–	[18]
Evaporation	Ti/Pd/Ag	POCl <sub>3</sub>	–	0.796	18.2	[19]

## Chapter 3

# Experimental

This chapter includes the experimental processes and methods used for fabricating the black silicon samples with sputtered front metal contacts. In Section 3.1 the sample fabrication methods and process flow are described. Characterization methods are described in Section 3.2. All processes used to obtain the structural and electrical properties of the sputter-deposited metal contacts on black silicon were done in Aalto University Micronova facilities, e.g. cleanroom and analyzation laboratory.

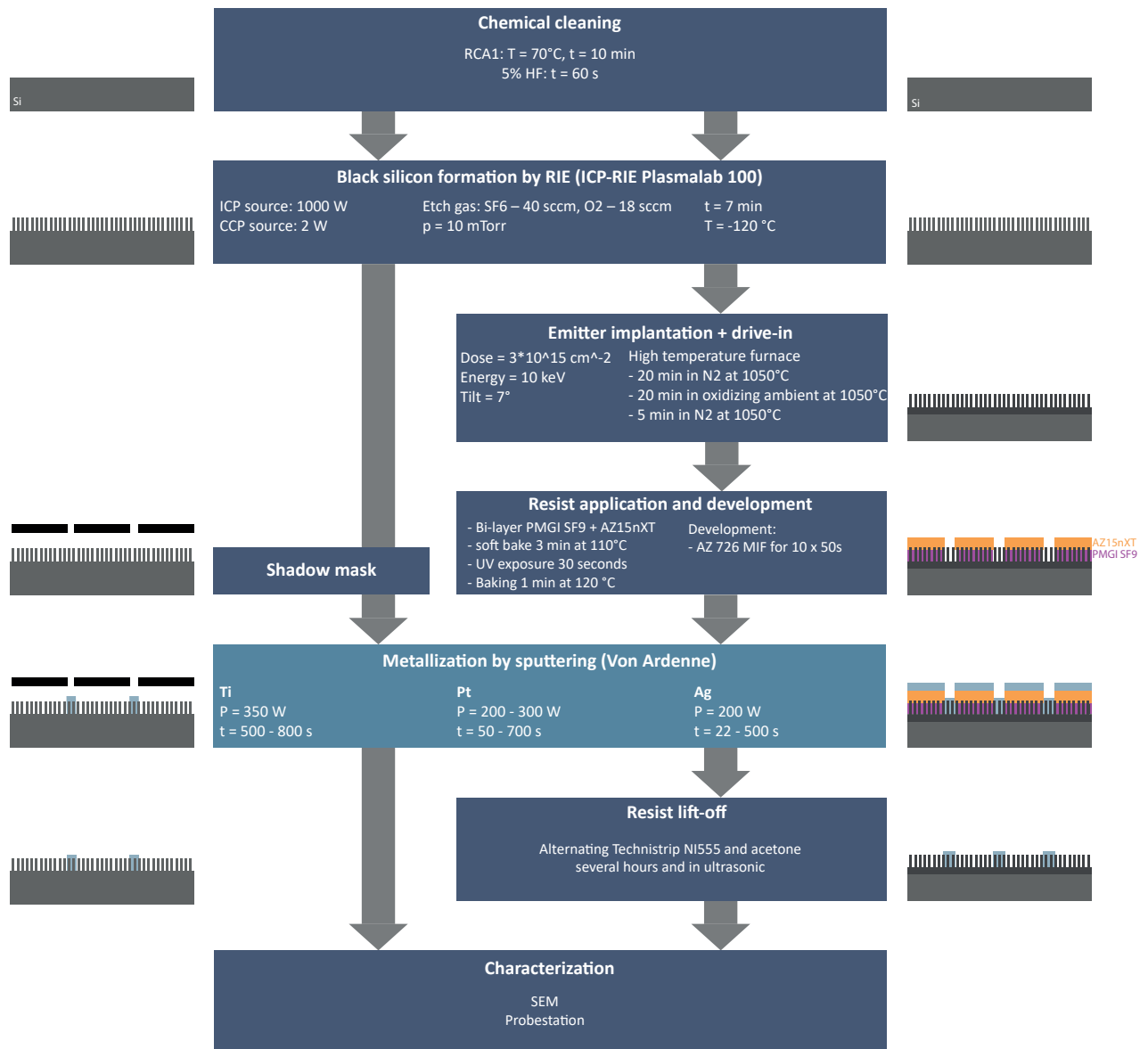
### 3.1 Sample fabrication and process flow

In this section, the sample fabrication processes and equipment are described. Samples were cleaned with the RCA1 cleaning process and etched with Inductively Coupled Plasma Reactive-Ion Etching (ICP-RIE) to create the black silicon nanostructuring. Metallization was done by sputtering and the main parameters changed in the process were the sputtering power and sputtering time. The hypothesis was that with lower sputtering power and higher deposition time the valleys will not get blocked as fast and it would be possible to reach the bottom of the valleys better and thus get a more uniform layer with lower contact resistance. For patterning of the metal contacts, two methods were used: one sample type utilized a steel shadow mask for pattern formation, whereas the second type was done by photoresist and lift-off process. The overall process flow is explained in detail in the process flow

## CHAPTER 3. EXPERIMENTAL

chart, Figure 3.1.

In the following subsections, 3.1.1–3.1.6, each fabrication method, and the used parameters are explained in more detail. As substrates for the optimization 4-inch silicon wafers (float zone, n-type,  $3 \pm 2 \Omega\text{cm}$ ) were used for each sample.



**Figure 3.1:** Process flow chart of the sample fabrication methods for the Ti/Pt/Ag metal contact optimization on b-Si.

### 3.1.1 RCA cleaning

The sample fabrication process started with cleaning the silicon wafers of any possible contamination like organics. Standard wet etching for Si-wafers was used.

RCA1 bath was used for both types of samples. RCA1 is an ammonia peroxide mixture ( $\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$ , mixing ratio 1 : 1 : 5) which is used for removing organic residues and films. Samples were dipped into heated ( $70^\circ\text{C}$ ) RCA1 mixture for 10 minutes. RCA1 cleaning removes particles by forming a thin oxide which encloses the particles. It also leaves the surface in a hydrophilic state.[17] Wafers were rinsed with deionized (DI) water afterward.

Next, the samples were dipped into 5% hydrofluoric acid (HF) for 60 seconds. HF removes any native or chemical oxide formed onto the silicon surface like the oxide film formed by the RCA1 cleaning.[17] Lastly, the samples were rinsed with DI- water and dried with nitrogen gas.

### 3.1.2 Inductively coupled plasma reactive-ion etching (ICP-RIE)

The black silicon structure was created with a maskless cryogenic Inductively Coupled Plasma Reactive-Ion Etching (ICP-RIE) process. RIE is a dry etching method that utilizes chemically reactive plasma of sulfurhexafluoride  $\text{SF}_6$  and oxygen  $\text{O}_2$  to remove material from the wafer surface.[17] Structures are formed by random micro-masking by silicon oxyfluoride ( $\text{SiO}_x\text{F}_y$ ) that are formed at the silicon surface and then etched by fluorine radicals ( $\text{F}^*$ ) in the plasma. The advantage of such dry etching method is that it maintains the substrate's crystallinity and results in a chemically clean surface and is easily adapted to industrial manufacturing chains.[21] It is also fast and inexpensive and does not require mask layers.[22] In an ICP-RIE system, the plasma is generated by RF powered magnetic field. The ion bombardment generates vertical needle-like structures onto the silicon surface. Cryogenic temperature suppresses lateral etching and thus etching proceeds vertically to produce pointed structures.[17] The fabricated surface structure, consist-

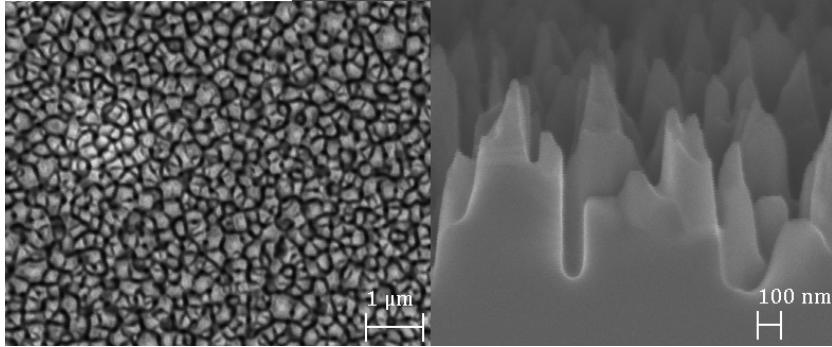
## CHAPTER 3. EXPERIMENTAL

ing of randomly shaped needles, does not reflect light but absorbs it and therefore the surface appears black, leading to the name black silicon.[3]

The etching processes were conducted with ICP-RIE Plasmalab 100 system from the Oxford instruments in Micronova facilities. The processing temperature was  $-120^{\circ}\text{C}$  and etching time 7 minutes in  $\text{SF}_6$  and  $\text{O}_2$  plasma. The parameters of the process were as follows:

- ICP source power 1000 W
- CCP source power 1 W
- Etching gas:  $\text{SF}_6$  40 sccm,  $\text{O}_2$  18 sccm
- Process pressure  $p = 10$  mTorr
- Etching time  $t = 7$  minutes
- Temperature  $T = -120^{\circ}\text{C}$

The resulting black silicon formation can be seen in Figure 3.2.



**Figure 3.2:** *Black silicon structures formed by ICP-RIE. On the left is the top view of the b-Si needles and on the right a cross-section image.*

### 3.1.3 Emitter implantation

Wafers with emitter implantation were provided by a colleague. Emitter doping was used on three samples (Run 13–15) for better conductivity. Metal contacts are optimized for solar cells with this emitter.

Boron implantation was done for both sides of the wafers with the following parameters:

## CHAPTER 3. EXPERIMENTAL

- Dose =  $3 \cdot 10^{15} \text{ cm}^{-2}$
- Energy = 10 keV
- Tilt =  $7^\circ$
- Drive-in treatment in high temperature furnace afterwards
  - 20 min in  $\text{N}_2$  at  $1050^\circ\text{C}$
  - 20 min in oxidizing ambient at  $1050^\circ\text{C}$
  - 5 min in  $\text{N}_2$  at  $1050^\circ\text{C}$

This process resulted in an emitter sheet resistance of  $\sim 100 \Omega/\square$  on the samples.

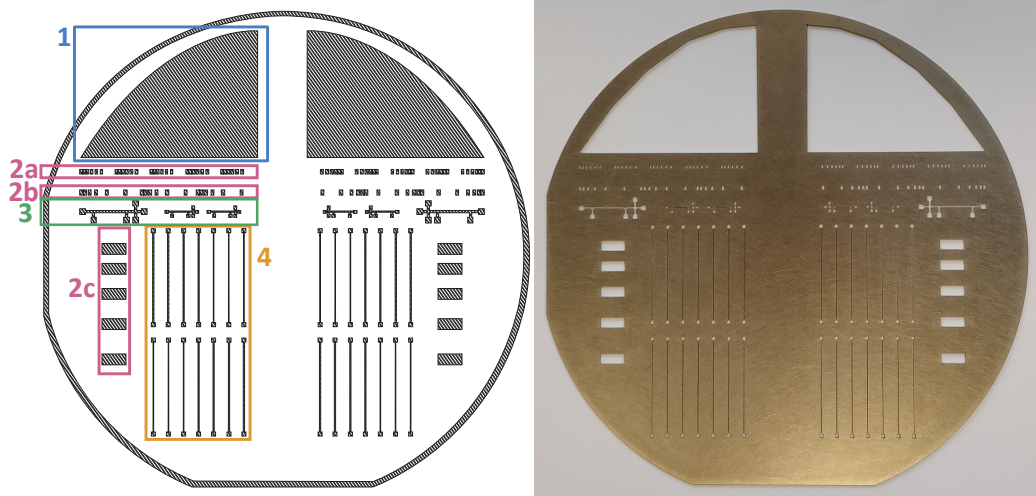
### 3.1.4 Shadow mask

For the first sample type, a shadow mask made of steel was used for metal contact pattern formation by sputtering. Using a shadow mask has several advantages; they are cheap and simple to use, do not require etching or lift-off process or any other chemicals. Its disadvantage is that it wasn't as precise to use and small structures were blocked by the mask structure walls.

The mask was ordered from Easy-Cad Oy according to the design containing the structures to measure the contact resistance and the resistance along the fingers. The design of the mask is shown in Figure 3.3. The thickness of the shadow mask was 0.3 mm. The mask had several different structures explained below and also marked into Figure 3.3.

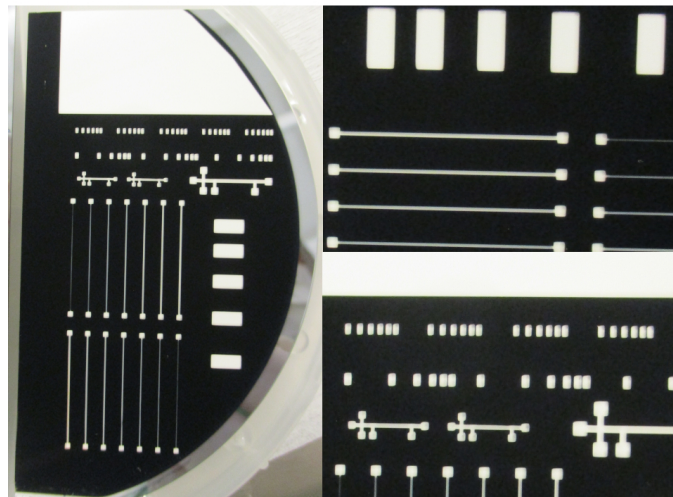
1. Larger area for taking SEM images (top view and cross-section)
2. TLM pads for measuring the contact resistance values with different sizes:
  - (a) size  $400 \times 800 \mu\text{m}$ , distances 200, 300, 400, 500, 600  $\mu\text{m}$
  - (b) size  $500 \times 900 \mu\text{m}$ , distances 200, 400, 800, 1600, 3200  $\mu\text{m}$
  - (c) size  $4670 \times 2000 \mu\text{m}$ , distances 2000, 3000, 4000, 5000  $\mu\text{m}$
3. Cross bridges to measure specific contact resistivity, width 350 or 175  $\mu\text{m}$ , length 6500 or 3250  $\mu\text{m}$
4. Fingers to investigate line resistance, length 18000  $\mu\text{m}$ , width 40, 60, 80, 100, 120, 140, 160  $\mu\text{m}$

### CHAPTER 3. EXPERIMENTAL



**Figure 3.3:** On the left is the design of the shadow mask and on the right the actual steel mask which was fabricated according to the design.

Before sputtering, the shadow mask was stuck to the wafers with heat resistant Kapton tape to make sure the wafer and the mask did not move against each other during the sputtering process and handling through the robot, to ensure clear structures with sharp edges after several deposition steps. The resulting image of the Ti/Pt/Ag sputtered b-Si wafer can be seen in Figure 3.4.



**Figure 3.4:** The black silicon wafer after Ti/Pt/Ag sputtering, patterned by a steel shadow mask.



### 3.1.5 Lift-off

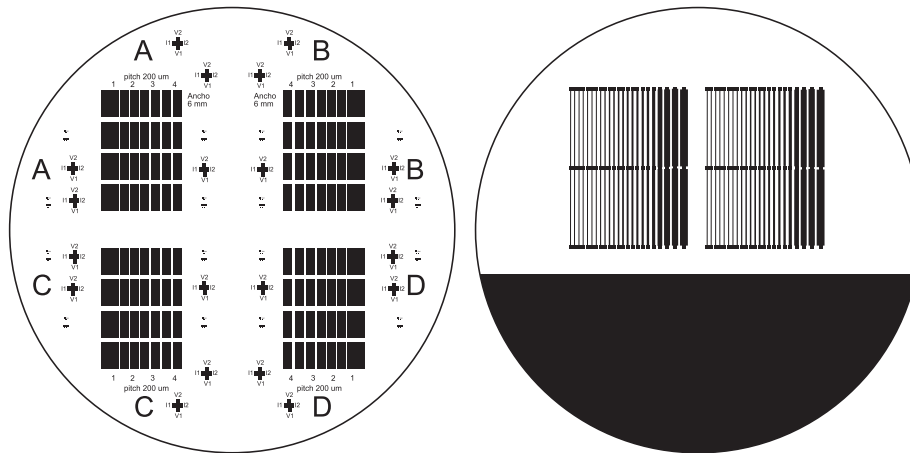
The lift-off process was chosen as an alternative contact patterning method because there were several issues with the shadow mask. One was that the mask shadowed the structures so much that the sputtered metal did not reach the wafer completely and also because the edges of the structures were not very sharp. Lift-off is a standard method but is not as simple as using a shadow mask.

The wafers were coated with bi-layer resist, PMGI SF9 on the bottom for easy removal, and on top AZ15nXT photoresist for creating a thick resist layer, which was essential for the contact structure formation. The idea was that the bottom layer is used to create an underetch around the structures during development before sputtering. This underetch has two purposes. First, the sputtered material cannot stick to the walls and second, it simplifies the lift-off after sputtering. At first, only the AZ15nXT photoresist was used but as it proved to be difficult to remove, it was necessary to change to bi-layer resist. The total thickness of the resist layers was estimated as  $\sim 5\text{--}6\ \mu\text{m}$  by the recipe. Figure 3.1 shows a simplified version of the resist coating process.

The process progressed as follows. First, the SF9 resist was spin-coated onto the wafer surface and soft baked for 5 minutes at  $180^\circ\text{C}$ . Next, the second resist layer, Az15nXT was spin-coated on top of the first one and both layers were soft baked on a hot plate for 3 minutes at  $110^\circ\text{C}$ . The samples were then aligned with a mask to cover the wanted contact structures and exposed with UV light for 30 seconds. Designs of the used masks can be seen in Figure 3.5. Post-exposure baking was done at  $120^\circ\text{C}$  for 1 minute on a hot plate.

The TLM structures in the mask on the left are  $2\times 6\ \text{mm}^2$ . The structures are paired so that there are four pairs in total in one structure. The measuring distances between each pair are 75, 275, 475 and  $675\ \mu\text{m}$ . The finger structures in the mask on the right have widths ranging from  $10\ \mu\text{m}$  to  $1200\ \mu\text{m}$ . The finger structures had three contact pads, in which distance between the outer and middle pad was  $18000\ \mu\text{m}$  and the distance between the outer pads was  $36000\ \mu\text{m}$ .

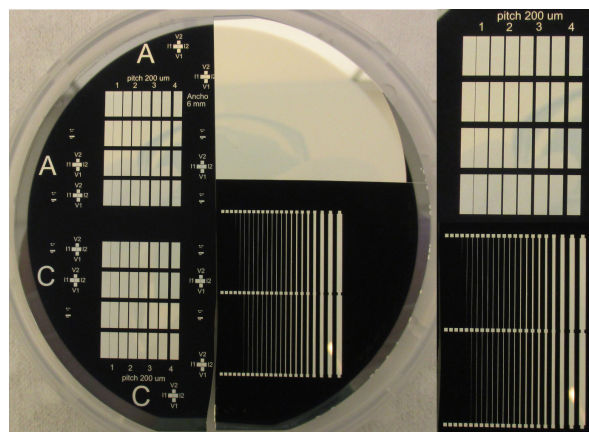
CHAPTER 3. EXPERIMENTAL



**Figure 3.5:** Photoresist masks for lift-off process. On the left are the TLM structures and on the right the finger structures together with SEM area.

For the last step before metal deposition, the resist was developed in AZ 726 MIF developer with rinsing steps for 10 x 50 seconds, as a contact to oxygen accelerates the development.

After the sputtering process, the resist layers along with the sputtered metal layer on top of the resist were removed with alternating between Technistrip NI555 batch and AZ 726 MIF developer for 2–3 hours in ultrasonic. As a result, only the wanted pattern of the metal layer was left on the b-Si. For each Run 11–15 half wafers with both structures of Figure 3.5 were used. The resulting patterned half wafers can be seen in Figure 3.6.



**Figure 3.6:** The resulting half wafers of sputtered black silicon wafers, patterned with photoresist and lift-off process.

### 3.1.6 Sputtering Ti/Pt/Ag

Sputtering was chosen as the method of deposition to fabricate the metal contacts, even though it is not widely used for industrial solar cells. However, Gimpel et al. showed that sputtering is a promising method.[20] Its advantages are also easy accessibility and the fact that it is a standard method in the semiconductor industry.

The main issue with sputtering is that the standard sputtering recipes, which are optimized for flat silicon surfaces, are not optimized for b-Si surfaces, which causes unconformity at the metal-semiconductor interface and the metal layer. To get better surface coverage and reaching the bottom of the valleys with metal, the aim was to find optimal parameters for sputtering metal on the black silicon surface.

Based on initial experiments and the results by Gimpel et al.[20], the stack of metals for the contacts was decided as titanium (Ti) at the bottom, platinum (Pt) in the middle and silver (Ag) on top. Ag is a highly conductive metal but doesn't stick to the Si surface very well, which is why Ti is used as an adhesive layer [23]. However, it has been shown that the Ti/Ag stack is not stable because of a thin oxide layer formation on the Ti surface which causes high corrosion resistance. Pt and palladium (Pd) have been shown to work as a passivating layer in between the Ti/Ag layers and thus solving the problem.[23]

The parameters changed for sputtering were the sputtering power and sputtering time, although also changing of argon flow and therefore the working pressure could be considered. The hypothesis was that with lower sputtering power, which is equal to lower deposition rate, the resulting metal layer would become more conformal and it would be possible to reach the bottom of the valleys better and thus get a more uniform layer with lower contact resistance.

For this process, CS73DS Cluster sputtering system from Von Ardenne was used to deposit the Ti/Pt/Ag stack. The typical sputtering parameters used on this device for flat silicon and the measured average thicknesses on flat silicon surface for this system are listed in Table 3.1.

CHAPTER 3. EXPERIMENTAL

**Table 3.1:** Typical sputtering parameters for Ti, Pt and Ag and the resulting average thickness of each material on flat silicon surface by using CS73DS Cluster sputtering system.

Material	Power (W)	Time (s)	Thickness (nm)
Ti	500	32	5
Pt	500	47	100
Ag	500	22	100

Table 3.2 shows the sputtering parameters which were used in the sputtering experiments on the b-Si surface. The resulting layer thicknesses were difficult to determine as the known values were for flat silicon surface and the results can be quite different on nanostructured b-Si. A roughly measured estimate of the thickness of metal contact for Run 15 sample was around 1  $\mu\text{m}$ .

**Table 3.2:** Table of sputtering parameters of Run 1–15.

RUN #	SPUTTERING POWER (W)			SPUTTERING TIME (s)			NOTES	Patterning
	Ti	Pt	Ag	Ti	Pt	Ag		
1	350	300	200	500	50	22		No patterning
2	350	300	200	800	100	22		
3	350	300	200	800	200	22		
4	350	300	200	800	300	22		
5	350	200	200	800	500	22		
6	350	200	200	800	700	22		
7	350	200	200	800	700	40		Shadow mask
8	350	200	200	800	700	300		
9	350	200	200	800	700	400		
10	350	200	200	800	700	500		
11	350	200	200	780	690	480	One-layer resist	Lift-off
12	350	200	200	780	-	480	No Pt target. Bi-layer resist test	
13	350	200	200	780	690	750	Emitter implanted	
14	350	200	200	780	900	900	Emitter implanted	
15	350	200	200	900	900	900	Emitter implanted	

Run 1–6 were proceeded without any patterning and Run 7–10 were processed with the shadow mask. Run 11–15 utilized lift-off process, thus the depositions had to be done with multiple short depositions (30 seconds) with cooling times (300 seconds) in between each sputtering round, as the photoresist will otherwise burn as the wafer is heating up due to the sputtering process.

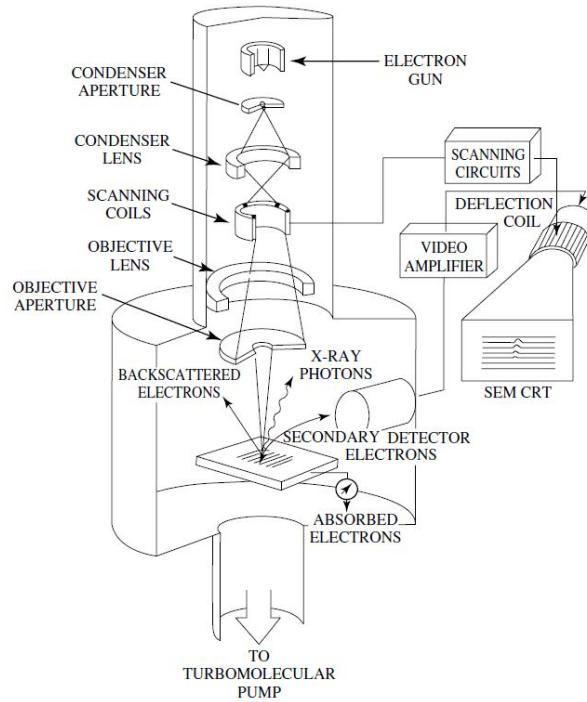
## 3.2 Characterization methods

Two main characterization methods were used for measuring the conformality results and the electrical properties of the samples. Scanning Electron Microscope (SEM) was used to take high magnification images of the sputtered metal contacts, and Transfer Length Method (TLM) with Probestation to acquire contact resistance values. Line resistance measurements were conducted with a simple multimeter. SEM and TLM measurement are explained in detail in this section.

### 3.2.1 Scanning Electron Microscope (SEM)

Scanning electron microscopes (SEM) use an electron beam to produce a magnified image of a surface. The focused electron beam hits the sample, which causes electrons to scatter in several different ways depending on the material, size, and texture of the sample. SEM detects the secondary and/or backscattered electrons and creates the images using these detected electrons while scanning the surface of the sample. SEM consists of an electron gun, an electrical lens system, scanning coils, an electron collector and a cathode ray display tube. Electron microscope's main advantages over optical microscopes are their much higher magnification and depth of field. However, taking sharp SEM images requires practice and good equipment, which are expensive.[7] The schematic of an SEM device is shown in Figure 3.7.

Scanning Electron Microscope measurements were conducted at Micronova cleanroom facilities with SEM EBL Zeiss Supra 40 equipment. Magnifications between 20 000 and 120 000 were used for imaging the samples. SEM images were taken in the top view of the samples both from larger sputtered areas and also the smaller fingers and TLM pad structures. Also, cross-sectional images from large sputtered areas and finger structures were taken after cleaving them. The results are shown and discussed in Section 4.1.



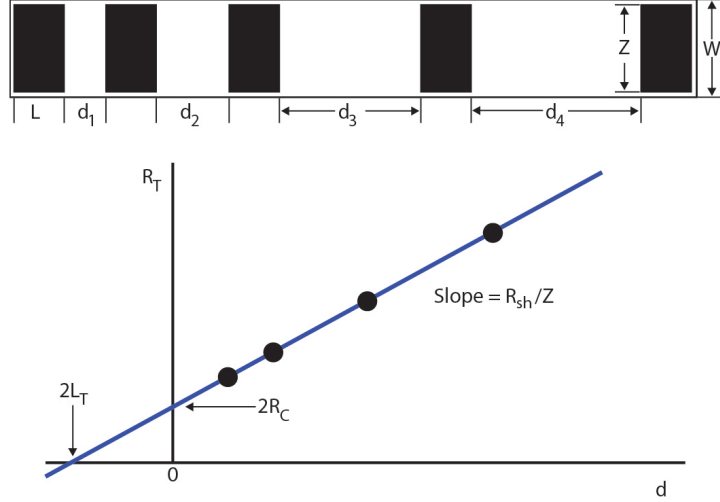
**Figure 3.7:** Schematic of a SEM device with the different working parts.[7]

### 3.2.2 Transfer Length Method (TLM)

The Transfer Length Method (TLM) can be used to measure the contact resistance  $R_c$  between the silicon substrate and the metal contacts. Contact resistance is described in detail in Section 2.2.1 and the contact resistance results are discussed in Section 4.2.1. Transfer length means the distance over which most of the current transfers from the semiconductor into the metal or vice versa. The idea of TLM is to measure the resistance between adjacent contacts, with bare semiconductor preferred in between the contacts. Schematics of the TLM structures used in these experiments can be seen in Figures 3.3 (areas 2a-c) and 3.5. The resistances are plotted against the spacing distances and the contact resistance can then be determined from the plot.[7] Figure 3.8 shows an example of a TLM test structure and a theoretical plot of total resistance as a function of contact spacing  $d$ . The black rectangles are the metal contacts and the white space in between them is the semiconductor. The resistance values are then measured between adjacent

CHAPTER 3. EXPERIMENTAL

metal contacts with increasing spacings  $d_1$ - $d_4$ . The resistance values are then plotted against the respective spacing  $d$ . [7]



**Figure 3.8:** A theoretical example of TLM test structure and a plot of total resistance as a function of contact spacing  $d$ . [7]

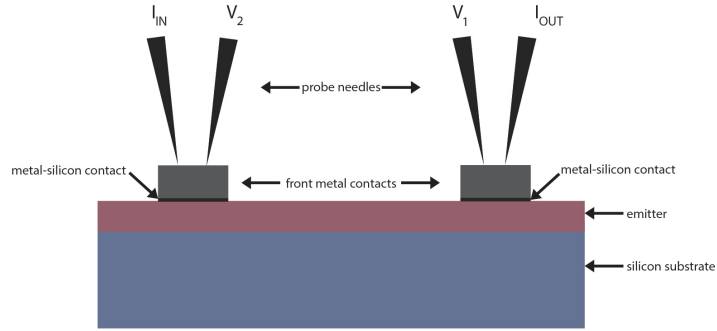
From this kind of plot it is possible to derive three parameters. The slope  $\Delta R_T / \Delta d = R_{sh} / Z$  leads to the sheet resistance  $R_{sh}$ .  $Z$  is the contact width, as can be seen in Figure 3.8. The contact resistance values for each sample can be derived from the linear fit with  $d = 0$ , meaning that when Contact Spacing ( $\mu\text{m}$ ) is set to 0. The total resistance values  $R_T$  on the y-axis (Total Resistance  $\Omega$ ) at  $d = 0$  gives then the contact resistance values so that  $R_T = 2R_c$ , which gives the value of interest in this thesis, the contact resistance  $R_c$ . The intercept at  $R_T = 0$  gives  $-d = 2L_T$ , where  $L_T$  is the transfer length, which can be thought of as that distance over which most of the current transfers from the semiconductor into the metal or vice versa. [7] Specific contact resistivity  $\rho_c$  is calculated by (3.1) [7]:

$$\rho_c = R_c L_T Z \quad (3.1)$$

The contact resistance measurements were conducted with a four-needle Probestation system using the Transfer Length Method (TLM) structures. The measurements were done so that two of the needles were on one TLM

CHAPTER 3. EXPERIMENTAL

pad and two other on a pad adjacent to it so that there was only black silicon in between the two pads. On both pads, one of the needles provided the current flow ( $I_{IN}$  or  $I_{OUT}$ ) and the second needle measured the voltage drop ( $V_1$  and  $V_2$ ) between the pads. A schematic of the used set up is shown in Figure 3.9.



**Figure 3.9:** A schematic of the utilized TLM set up for contact resistance measurements.

The resistance values were calculated by (3.2):

$$R = \left| \frac{V_2 - V_1}{I} \right| \quad (3.2)$$

During measurements, the current was swept between values -0.1 mA and 0.1 mA and  $\sim 20$  data points were recorded with the respective current  $I$  and voltages  $V_1$  and  $V_2$  for each distance. The resistance values  $R$  were then calculated by (3.2). The average values and standard deviations were calculated for each measured TLM structure and each pad distances.



## Chapter 4

# Results & discussion

The sputtering results were studied with two characterization methods; Scanning Electron Microscope (SEM) to acquire high magnification images of the sputtered metal contacts, and contact resistance measurements with Probestation. Line resistance measurements were conducted with a simple multimeter. The sputtering parameters were changed in between each run to optimize the sputtering results, as shown in Table 3.2.

The sample fabrication and characterizations were done simultaneously so that after each sputtering run of one sample, the results were checked with SEM to see the conformality of the contacts. Based on these results the parameters were further changed for the next runs. The SEM results are discussed in more detail in the next section.

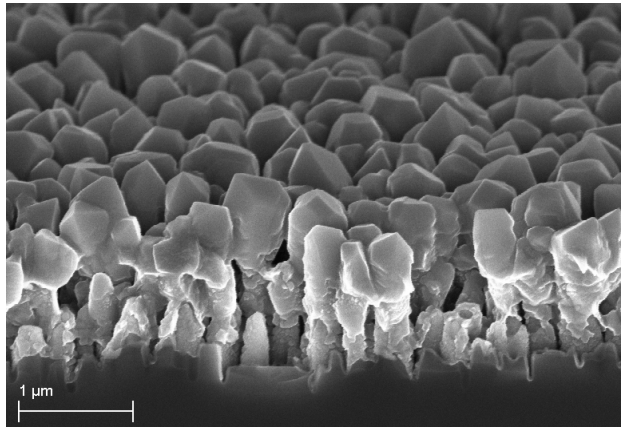
### 4.1 Scanning Electron Microscope results

Scanning Electron Microscopes (SEM) provides high magnification images of even nanoscale structures. The principles of the method have been described in detail in Section 3.2.1 Scanning Electron Microscope (SEM). SEM was used for studying the conformality of the sputtered metal contacts on black silicon nanostructures. Both top view and cross-section images were taken. The top view was used for checking the conformality and if the metallization was smooth and did not have holes in it. Cross-section images were used

## CHAPTER 4. RESULTS & DISCUSSION

to check how well the metal reached the bottom of the b-Si valleys and filled them up, and to see the thickness of the metal layer. Samples were sputter-deposited with metal one at a time and after each sputtering run, the samples were checked with the SEM to see how the deposited metal looked like on the nanostructures. This way, it was possible to change the sputtering parameters (power and time for the different metals) one at a time to find a better set of parameters for fabricating conformal metal contacts.

From initial investigations of sputtered Al metal contacts on b-Si solar cells, it could be seen, that the standard sputtering recipes for conventional flat silicon are not optimized for the nanostructured black silicon (b-Si). An example of previously sputtered Al metal contacts can be seen in Figure 4.1.



**Figure 4.1:** *Cross-sectional image of sputtered aluminum on black silicon structures from early experiments. The image proves that using standard sputtering recipes on black silicon samples is not optimal and leads to highly nonconformal metal crystals. The metal film does not reach the bottom of the b-Si valleys.*

From Figure 4.1 it can be seen that the metal is crystallized on top of the b-Si structures and the metal does not reach the bottom of the b-Si valleys. This proves that the standard sputtering recipes do not work very well on the b-Si structures. The main problem is the high sputtering power which leads to higher sputtering yield which is equal to more material being sputtered onto the sample in the same time period. The fast sputtering causes the material to build on top of the structures, leaving relatively huge

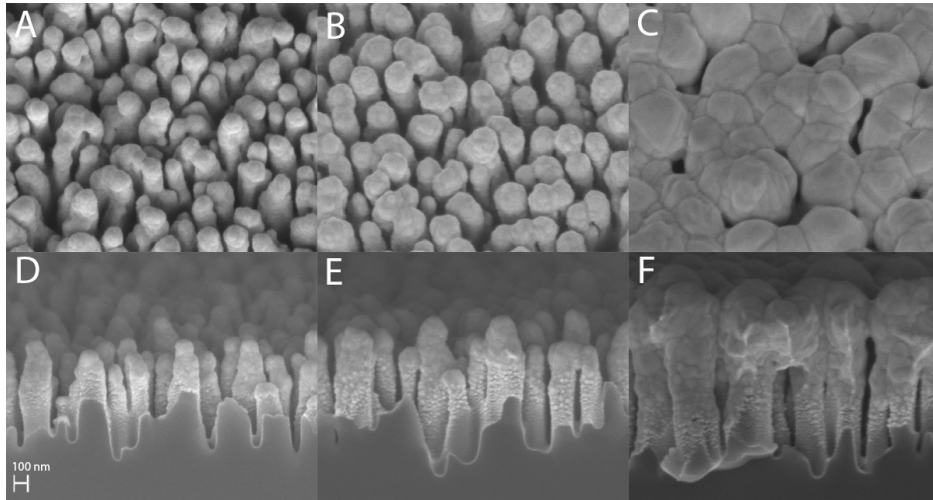
## CHAPTER 4. RESULTS & DISCUSSION

gaps underneath and not reaching the bottom of the b-Si valleys, thus leading to poor contact between the metal and the underlying semiconductor. To prevent this from happening, the goal of this thesis was to find better-optimized parameters for sputtering metal contacts on the b-Si structure. Following the hypothesis that smaller sputtering yield should lead to more conformality, the sputtering powers were significantly lowered compared to the standard values and consequently, the sputtering times were increased to gain enough material for the contacts. The standard values differ between sputtering systems, but the values were changed compared to the standard values of the VA system used in the Micronova cleanroom facility.

Aluminum is a standard material used for solar cells, but based on pre-experiments, Ti/Pt/Ag stack seemed to have significantly better conformality on the black silicon nanostructures compared to Al. Therefore it was chosen as the stack for metal contacts in this thesis instead of Al. Sputtering system von Ardenne, which is a magnetron sputtering system, was used for sputtering the contacts and the typical average sputtering thicknesses on flat surfaces are known for this system for the standard powers. On flat silicon surface, the parameters and resulting thickness of each material are shown in Table 3.1.

The investigation of the new metal contact was started by using lower sputtering powers and keeping the sputtering times short at first to then increase the sputtering time for each material one at a time. The first Runs did not include any patterning on the samples but instead, the whole b-Si surface was covered with the materials. After each run, SEM pictures were taken from the top view of the samples and then by cutting the wafer to get a cross-sectional image of the b-Si nanostructures and sputtered materials. Figure 4.2 shows a comparison of three different sputtering runs, which correspond to Run 2, 6 and 8 given in Table 3.2. Figures 4.2 A)–C) are top views of each sample, of Run 2, 6 and 8, respectively, and D)–E) are the corresponding cross-sectional views of each sample.

Run 2 still has a fairly low amount of metal on it since the sputtering powers and times are very low. In Run 2, the sputtering power and time were 350 W and 800 seconds for titanium, 300 W and 100 seconds for platinum and



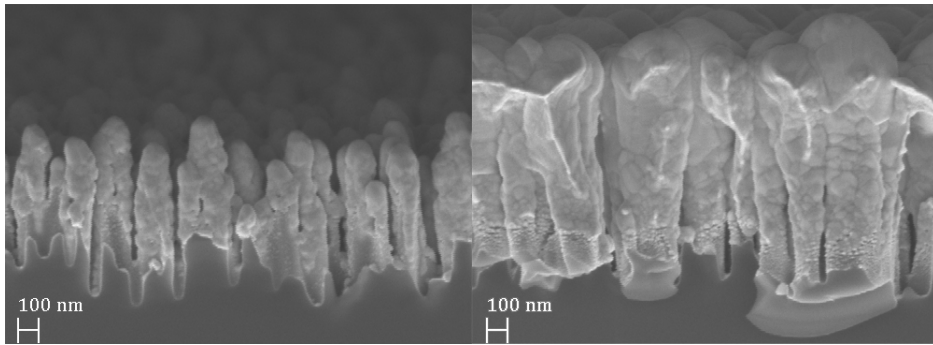
**Figure 4.2:** SEM images of Run 2, 6 and 8. A)–C) are top views of each run and D)–F) are cross-section images of the cleaved wafers. Run 2, A) and D), has still very little material due to the low sputtering power and short sputtering time. Sputtering times were increased, but as Ti and Pt are slow to sputter, the changes to Run 6, B) and E), are not as significant. In Run 8, C) and F), the amount of silver is significantly higher and thus can be seen clearly in the sputtering result.

200 W and 22 seconds for silver. On b-Si nanostructures these parameters will not build thick layers which can be seen in Figures 4.2 A) and D). For Run 6, which are B) and E), the titanium parameters are the same but sputtering power for platinum has been decreased to 200 W to gain more conformal results and the sputtering time is increased already to 700 seconds. The changes are not as clear compared to Run 2, but some more material is sticking to the b-Si nanostructures already. The changes are easiest to see when the sputtering time for silver was increased. Thus, in Figures 4.2 the significantly higher sputtering time for silver during Run 8 (300 seconds) can already be seen to fill the valleys of the b-Si structures and somewhat blocking the top of the structures already. The Run 8 pictures already look very promising regarding the conformality, but still need a lot more material to achieve good conductivity by filling the gaps, as well as to close the openings that can be seen in the top view (C).

From Run 7–10 a steel shadow mask was used for patterning the finger

## CHAPTER 4. RESULTS & DISCUSSION

and TLM pad structures for resistance measurements. The shadow mask structure and details are explained more thoroughly in Section 3.1.4 Shadow mask. It was quickly noticed, however, that despite the simplicity of the shadow mask, it was a poor way to pattern the wanted structures. One issue was that during sputtering the mask shifted slightly so that the sputtered materials did not stack on top of each other and the edges of the structures were blurry. This could somewhat be solved by fixing the shadow mask and the wafer together with heat resistant Kapton tape. The biggest issue, however, was that the shadow mask shadowed the finger structures so badly that the deposited material on the b-Si nanostructures in the finger patterning was significantly lower than on the big open area in the mask. An example of this shadowing effect can be seen in Figure 4.3.

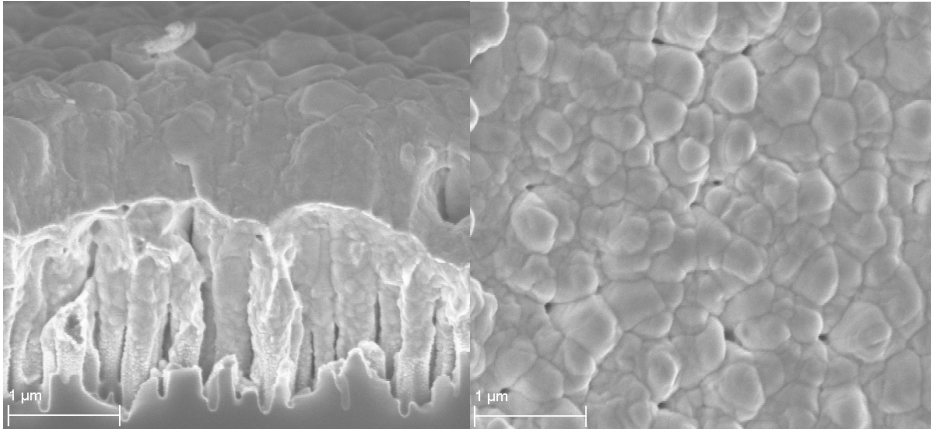


**Figure 4.3:** *Cross-sectional SEM images of Run 10 with shadow mask patterning. Left: a cross-section image of a finger, width  $140\ \mu\text{m}$ . Right: a cross-section image of the big sputtering area. The images are from the same sample and thus the sputtering powers and times were identical on both structures. The steel shadow mask shadows the significantly smaller finger structures so badly that not enough metal reaches the b-Si nanostructures.*

Because of the problems faced with the shadow mask, it was clear that another more complicated approach was needed. Photolithography and lift-off procedures are standard methods industrially used in semiconductor device fabrication. However, lift-off on black silicon wafers is a bit more tricky compared to flat silicon and some problems were faced with this method also. Details of the used lift-off methods are explained further in Section 3.1.5 Lift-off.

## CHAPTER 4. RESULTS & DISCUSSION

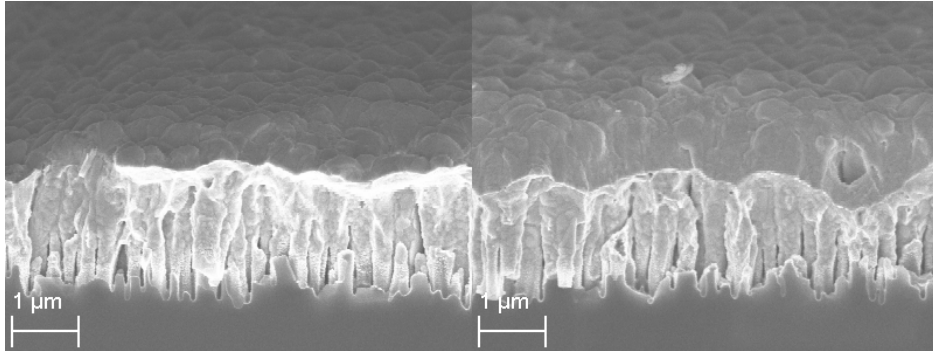
The resist for photolithography needed to be relatively thick as the sputtering result would be around  $1\ \mu\text{m}$ . The resist needs to be thicker than that for the structures to form. Thus there were some problems at first with removing the resist and the excess metal from the b-Si nanostructures. The resist used for the lift-off process was relatively difficult to remove and the b-Si nanostructuring probably was one reason why the removal chemicals didn't manage to remove all the resist and thus also some of the thick metal layers. This issue was fixed by changing to a bi-layer resist, in which the bottom layer is mainly for easy removal and the top one for getting thick enough resist. This way, when removing the bottom layer of the resist, the top layer would also come off nicely. As a result, quite fine and conformal fingers could be fabricated, as can be seen in Figures 4.4, 4.5 and 4.6.



**Figure 4.4:** SEM images of Run 15 finger with width  $1200\ \mu\text{m}$ . On the left is the cross-sectional image of the finger and on the right is the top view. From the pictures it can be seen that the sputtering result looks quite smooth and conformal.

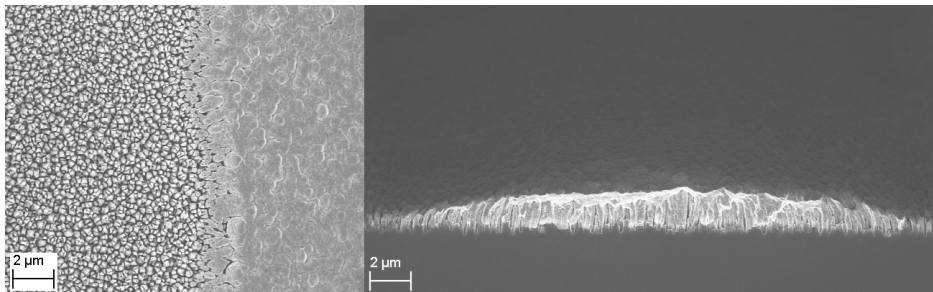
The lift-off process proved to be much better for fabricating the wanted conformal finger structures and to get enough material deposited on the fingers. Since the resists were relatively thin (estimated thickness of  $\sim 5\text{--}6\ \mu\text{m}$  with the recipe) compared to the steel shadow mask ( $300\ \mu\text{m}$ ), nearly no shadowing effect could be seen, as Figure 4.5 shows.

Only at the very edges of the structures, the layer was thinner and round, as can be seen in Figure 4.6, instead of very sharp angular edges. The metal



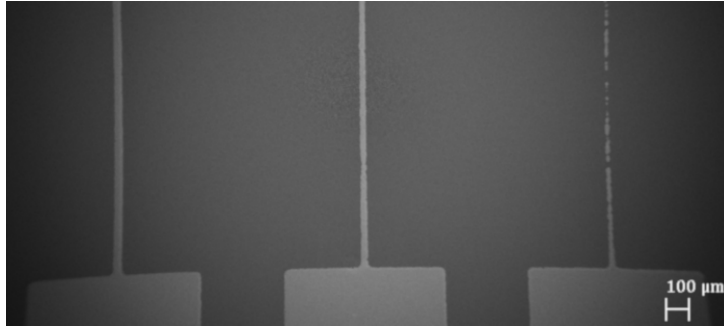
**Figure 4.5:** *Run 15 cross-section comparison of two different fingers. On the left is finger with width 60  $\mu\text{m}$  and on the right 1200  $\mu\text{m}$ . It can be seen that there is not any stark shadowing effect compared Run 10 shadow mask structures in Figure 4.3.*

contacts were formed as they should and could be thickened by increasing the sputtering rounds of silver. However, the contacts should probably still be even thicker for better conductivity.



**Figure 4.6:** *SEM images of Run 15 finger structures (lift-off). Left: top view from the edge of one finger. In this level of magnification, it can be seen that the finger edges are not completely straight. The left side of this image is a pure b-Si structure which, when moving to the right, gradually shifts to the sputtered metal on the b-Si structures. Right: cross-section image of how the fingers are built on the b-Si. It can be seen here that the metal layer is the thickest in the middle of the finger and lower on the edges.*

It could be seen from the SEM pictures that the finger structures, which are narrower than 30–40  $\mu\text{m}$ , are not uniform and have sections without metal on them. An example of this can be seen in Figure 4.7.



**Figure 4.7:** *Run 12 finger comparison. On the right is a finger which wasn't completely developed during the lift-off process and before sputtering. Thus, the metal layer is not conformal and the finger is not conductive.*

This ununiform structure was caused when developing the thick photoresist, which did not come off completely in the finer finger lines. There might be several reasons why this happened. One is that the photoresist was very thick and the developing process might not have been optimized for developing the resist on a b-Si structured silicon wafer. Additionally, the mask used for exposing the resist before development was a plastic mask, which might not be as detailed compared to glass chromium ones. With a plastic mask, there is always the possibility that the mask is bent while exposing and the printed structures might not be detailed and black enough to block the UV-light completely. Research solar cells on flat silicon have  $10\ \mu\text{m}$  wide fingers, whereas the most narrow fingers that could be developed in these experiments were  $\sim 40\ \mu\text{m}$ .

One possible issue that the lift-off process has, could be that the use of etching chemicals for many times could also lead to that the b-Si nanostructures are being slightly etched as well. Some of the wafers looked slightly less black by eye after the whole lift-off process, but this was not confirmed or compared thoroughly with wafers that were processed without the lift-off process. Losing the blackness means that the b-Si's antireflectance properties could somewhat worsen. The risk of this occurring should be small as the resist, developer and remover are all made for use with silicon. However, this effect was not studied in this thesis as the main focus was to achieve good metal contacts with as low contact resistance as possible.



## 4.2 Resistance measurements

The electrical properties of the fabricated metal contacts were characterized in two ways. The most important ones were the contact resistance measurements, which utilized the Transfer Length Method (TLM), described in detail in Section 3.2.2 Transfer Length Method (TLM). Contact resistance and specific contact resistivity were chosen as the most important values to measure because they imply best how good the semiconductor-metal contact is. Contact resistance is explained in detail in Section 2.2.1 Contact resistance  $R_c$  losses at the metal-semiconductor interface.

In addition to the contact resistance, the resistance along the finger structures was measured as well, by using a simple multimeter. The line resistance value indicates how conductive the fingers are and if the thickness of the fabricated metal layer is thick enough.

In the case of both contact resistance and finger line resistance, the lower the value the better the metal contact is. For example, it is possible to get good contact resistance values but the line resistance could still be poor if the metal layer is not thick enough. This is due to the materials, and the way in which the current is transferred are different. In case of contact resistance, the current goes from the metal contacts into the semiconductor underneath, transfers to the other metal contact and then out of the device. Line resistance occurs along the metal finger and thus is affected by the thickness and quality of the metal layer.

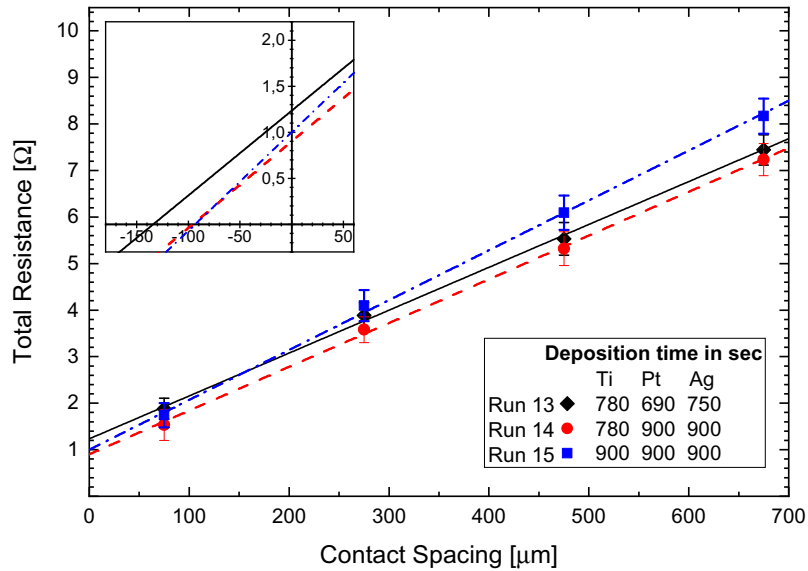
In the case of black silicon metallization, very few studies reported contact resistance or specific contact resistivity values. Schroder et al. defined in their study that for solar cells in general, the specific contact resistivity  $\rho_c$  should be  $\leq 2 \text{ m}\Omega\cdot\text{cm}^2$ . [8] Also, as mentioned before, von Gastrow et al. reached a specific contact resistivity value as low as  $0.3 \pm 0.2 \text{ m}\Omega\cdot\text{cm}^2$  on boron-implanted b-Si surfaces with nickel or aluminum contacts. [18]

For line resistance, Mette et al. reported a measured line resistance value of  $34 \text{ }\Omega/\text{m}$  ( $0.34 \text{ }\Omega/\text{cm}$ ) for conventional silver paste screen-printed contacts. [24] The contacts had a finger width of  $120 \text{ }\mu\text{m}$  and maximum height of  $13 \text{ }\mu\text{m}$ . [24]

### 4.2.1 Contact resistance

As mentioned in Section 2.2.1, contact resistance is characterized by two quantities, which are referred to as contact resistance  $R_c$  ( $\Omega$ ) and specific contact resistivity  $\rho_c$  ( $\Omega\cdot\text{cm}^2$ ). Specific contact resistivity includes the actual interface and also the regions immediately above and below the interface.[7] The principles of the Transfer Length Method (TLM) used to measure  $R_c$  and  $\rho_c$  has been explained in detail in Section 3.2.2.

The values derived with four-needle Probestation system were plotted with their respective pad spacing distance values to get the Figure 4.8.



**Figure 4.8:** Total resistance versus contact spacing by Transfer Length Method of Run 13-15. Each data point is the average resistance value of all 8 TLM structures with error bars calculated by the standard deviation. A linear fit was done on each sample and its respective data points. Black diamonds are Run 13, red circles are Run 14 and blue squares are Run 15.

Each data point in the figure is the average resistance value of all the TLM structures (8 on each sample) for the respective pad distance value over which the resistance was measured and calculated. The standard deviation

## CHAPTER 4. RESULTS & DISCUSSION

is used for the error bars of each data point. As can be seen in the figure, the resistance values are more or less linear when plotted against the distance between the TLM pads used for each measurement.

For plotting the TLM results samples from Run 13–15 were used. These samples had an emitter implanted on the front side for better conductivity. The contact width  $Z$  for these samples was 6 mm. The calculated contact resistance values  $R_c$  and further derived specific contact resistivity values  $\rho_c$  are shown in Table 4.1. The samples from Run 1–12 did not have emitters and the contact resistance values were derived only from Run 10 (shadow mask) and Run 12 (lift-off).

**Table 4.1:** Contact resistance  $R_c$  ( $\Omega$ ), specific contact resistivity  $\rho_c$  ( $\Omega\cdot\text{cm}^2$ ), semiconductor sheet resistance  $R_{sh}$  ( $\Omega$ ), Slope ( $\text{m}\Omega/\mu\text{m}$ ) and transfer length  $L_T$  ( $\mu\text{m}$ ) values of the samples from Run 13–15. The contact width value  $Z$  for Run 10 was 0.4670 cm and for Run 12–15 0.6 cm.

Run#	$R_c$ (m $\Omega$ )	$\rho_c$ (m $\Omega\cdot\text{cm}^2$ )	$R_{sh}$ ( $\Omega$ )	Slope (m $\Omega/\mu\text{m}$ )	$L_T$ ( $\mu\text{m}$ )
10	$\sim 17\cdot 10^3$	1869.63	33.53	7.18	2355.30
12	$\sim 16\cdot 10^3$	93.40	997.56	166.26	97.29
13	617.18	2.48	55.26	9.21	67.01
14	450.60	1.27	56.40	9.40	47.94
15	500.52	1.40	64.26	10.71	46.73

These results indicate that Run 14 has the lowest contact resistance and specific contact resistivity, as can be seen from Table 4.1. It seems that the increased Ti sputtering time in Run 15 could have caused it having slightly worse contact resistance compared to Run 14. Titanium is not a very good conductor and mainly works as an adhesive material on the silicon sample. Despite this, the sputtering time for Ti was relatively high during most Runs to ensure complete coverage, as it is slow to sputter a thick layer of Ti especially on b-Si where film growth is not as fast with the high aspect ratio surface. However, this does not explain why Run 13 has a worse contact resistance value compared to Run 15, as Run 13 and Run 14 have the same amount of Ti. So either the smaller amount of Pt or Ag in Run 13 probably

## CHAPTER 4. RESULTS & DISCUSSION

causes the difference between the Runs. As mentioned before, Schroder et al. defined in their study that for solar cells in general, the specific contact resistivity  $\rho_c$  should be  $\leq 2 \text{ m}\Omega\cdot\text{cm}^2$ . [8] Comparing to this value, however, both Run 14 and 15 are less than the  $2 \text{ m}\Omega\cdot\text{cm}^2$ , and even Run 13 is very close to this value. In that sense, all of these three Runs with emitters have good values.

From the slope of the linear fit lines in Figure 4.8 it was possible to calculate the sheet resistance  $R_{sh}$  values of the samples. This slope and thus  $R_{sh}$  are defined by the emitter and thus should be almost the same. It is to be noted that for Runs 13–15 two different wafers with the same implantation parameters were used. The wafers were cleaved in the middle and thus a half wafer was used for one measurement. Run 13 and Run 14 were cleaved from the same wafer which might explain why their  $R_{sh}$  and slope values are closer to each other compared to Run 15. If there was, for some reason, a difference in the emitter implantation between Run 14 and 15 despite them being processed and measured the same way, it might have lead to the slightly different  $R_{sh}$  and slope results. The slopes of Run 13 and Run 14 are very similar,  $9.21 \text{ m}\Omega/\mu\text{m}$  and  $9.40 \text{ m}\Omega/\mu\text{m}$ , respectively. Run 15 has a slope of  $10.71 \text{ m}\Omega/\mu\text{m}$ . The emitter sheet resistance of the wafers used for Run 13–15 was measured to be  $\sim 100 \Omega/\square$ . However, the  $R_{sh}$  values measured from the metal sputtered samples was significantly lower than that. It is stated by Schroder et al. that TLM can be problematic for determining the sheet resistance, as the sheet resistance under the contacts may differ from the sheet resistance between the contacts due to the effects of contact formation. [7] This might explain the differences in the results.

As very few studies have reported the contact resistance  $R_c$  and the specific contact resistivity  $\rho_c$  values, especially on black silicon, it was difficult to compare the results to literature. Muszyfaga-Staszuk et al. used pyramid-like nanostructures on silicon and used a commercial silver paste for contact fabrication. [9] Their samples had an  $n^+$  emitter fabricated by donor doping from a source of phosphorus trichloride ( $\text{POCl}_3$ ), which resulted in a sheet resistance value of  $\sim 50 \Omega/\square$ . The TLM results on these samples gave  $R_c$  values ranging  $0.40\text{--}1.94 \Omega$  and  $\rho_c$  values  $18.34\text{--}230.41 \text{ m}\Omega\cdot\text{cm}^2$ . [9] Compared

## CHAPTER 4. RESULTS & DISCUSSION

to the results in this thesis, the smallest  $R_c$  values are similar, but their  $\rho_c$  values are significantly higher. As the pyramid nanostructures are quite flat compared to the b-Si structures, these results are very promising for b-Si metallization as they are even better than commercially used silver paste metallization on pyramid-like nanostructures.

Another result from literature by Silva et al. was acquired from multi-crystalline flat silicon samples with a boron-doped emitter ( $R_{sh} \sim 70 \Omega/\square$ ) and silver-aluminum screen-printed contacts on the front surface.[25] Their lowest achieved  $\rho_c$  values were the order of  $3 \text{ m}\Omega\cdot\text{cm}^2$ , which is similar to the standard industrial value for screen-printed contacts.[25] Compared to this, the results for the sputtered front contacts in this thesis are even lower, which is promising.

Mette et al. fabricated screen-printed front contacts using hotmelt silver paste on boron-doped ( $R_{sh} \sim 40 \Omega/\square$ ) single crystalline silicon with pyramid-like surface texture.[24] They achieved contact resistivities of about  $1\text{--}3 \text{ m}\Omega\cdot\text{cm}^2$  by TLM on the emitter surface. These values are roughly the same as the results presented in Table 4.1.

As compared to planar and pyramid structured surfaces reported in literature, it can thus be stated that the results in this thesis are quite promising. As the b-Si nanostructures in this thesis have a very high aspect ratio and taking into account that the results are similar to previous studies with less high-aspect surfaces with standard screen-printed metal contacts, it is implied that sputtered Ti/Pt/Ag metal contacts on b-Si could be optimized to fabricate efficient b-Si solar cells.

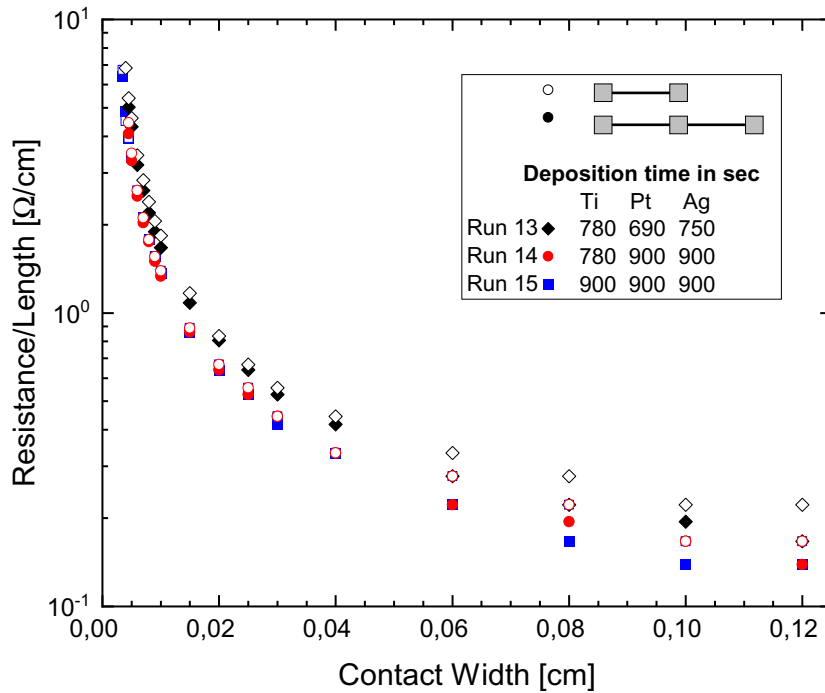
### 4.2.2 Finger line resistance

For measuring the finger line resistance values, each sample of the sputtering Runs 13–15 also had finger structures but no emitter. These were needed to measure the conductivity along the finger and thus to determine if the finger structures were thick enough. Finger widths ranged between  $10 \mu\text{m}$  and  $1200 \mu\text{m}$ , having 23 fingers altogether with different widths on the photolithography mask. It could be seen, however, both with a light microscope and

CHAPTER 4. RESULTS & DISCUSSION

SEM that about six of the fingers with the smallest finger-widths could not be opened during the photoresist development process and thus were barely conductive. Thus  $40\ \mu\text{m}$  was roughly the smallest finger width that could be measured.

The finger line resistance values were measured with a simple multimeter. The finger structures had three contact pads so that two different finger lengths,  $1800\ \mu\text{m}$ , and  $3600\ \mu\text{m}$ , could be used for measuring. The resistance per length ( $\Omega/\mu\text{m}$ ) value was then calculated for each sample and plotted against the finger width, see Figure 4.9. The open symbols are the shorter,  $1800\ \mu\text{m}$  finger lengths, and filled symbols are the longer,  $3800\ \mu\text{m}$ . Each color is for a different sample, black diamonds for Run 13, red circles for Run 14 and blue squares for Run 15.



**Figure 4.9:** Resistance values of Run 13–15 measured along the fingers and plotted against the respective finger widths. Open symbols:  $18000\ \mu\text{m}$ . Filled symbols:  $36000\ \mu\text{m}$ . Black diamonds are Run 13, red circles are Run 14 and blue squares are Run 15.

## CHAPTER 4. RESULTS & DISCUSSION

From Figure 4.9 it can be seen that the values from Run 14 and 15 are fairly similar but Run 13 has a bit higher resistance values. This is probably caused by the thickness difference of the silver layer, which is the most crucial one when it comes to the conductivity along the fingers. Run 14 and 15 have a thicker layer of silver which makes the fingers better conductors. Titanium is known to be a bad conductor but despite this Run 14 and 15 have very similar results which indicate that the amount of Ti is not as important in case of line resistance, as long as the silver layer is thick enough.

As expected of the results, the resistance values are lower when the finger widths are wider, and vice versa. This is due to the same reason as the thickness of the silver layer. When the finger is wider there is also more material and thus, it is more conductive. When the finger structures are narrow, defects disturb the conductivity more easily as there is less space for the electrons to move through. No line resistance values were found in the literature for contacts on b-Si, but the results are still good as even the most narrow fingers have resistance per length values that are less than  $10^{-3} \Omega/\mu\text{m}$ . As was already mentioned in Section 4.1, from Figure 4.7 it could be seen that some of the smallest fingers were not conformal and thus barely conductive if at all. The smallest finger-widths that could be used were around 30–40  $\mu\text{m}$ , whereas for research solar cells on flat silicon they are often around 10  $\mu\text{m}$ .

As in the case of contact resistance, it was difficult to find previous line resistance measurement results from the literature, especially on b-Si. The same study by Silva et al., which was mentioned already in Section 4.2.1, also reported the line resistance values.[25] Their values with the screen-printed silver-aluminum fingers were in the range of 0.3–0.4  $\Omega/\text{cm}$ , which is in line with the standard for a silver printed paste. Their front contact width was varying between 140 and 170  $\mu\text{m}$  and was around 18  $\mu\text{m}$  thick.[25] This thickness was much higher than the fingers on the samples used in this thesis, which had roughly  $\sim 1 \mu\text{m}$  overall metal thickness. Measuring the thickness was very difficult as it was hard to determine what are the endpoints on a highly structured surface. Nevertheless, the thickness was considerably lower compared to the results used in Silva et al. As seen from Figure 4.9

## CHAPTER 4. RESULTS & DISCUSSION

the resistance per length value at  $\sim 140\text{--}170\ \mu\text{m}$  ( $\sim 0.140\text{--}0.170\ \text{cm}$ ), which corresponds to the width by Silva et al., was around  $1\ \Omega/\text{cm}$ . This value is a bit higher than the  $0.3\text{--}0.4\ \Omega/\text{cm}$  of Silva et al., but considering the much lower finger thickness value, the result is still good and could probably be improved by increasing the finger thickness.

The study by Mette et al., which was mentioned in Section 4.2.1, also reported line resistance values.[24] The fingers in their samples were around  $120\ \mu\text{m}$  wide and had a thickness as high as  $30\ \mu\text{m}$ , which is much higher than the conventional screen-printed fingers that usually have a maximum height of  $13\ \mu\text{m}$ . Their line resistance value was around  $14\ \Omega/\text{m}$  ( $0.14\ \Omega/\text{cm}$ ), which is very low compared to conventional silver paste screen-printed contacts with line resistance of  $34\ \Omega/\text{m}$  ( $0.34\ \Omega/\text{cm}$ ).[24] The results of the experiments in this thesis indicate roughly  $\sim 1\ \Omega/\text{cm}$  values at the same finger width, which is most likely due to the significantly lower finger thickness value. With a higher thickness, the line resistance values would be expected to be much lower.

As a summary, it could be stated that the line resistance values are in good agreement with literature but could still be improved. As the metal fingers fabricated in this thesis had a significantly lower thickness compared to literature, the line resistance values were not as low as in those studies. However, considering the low thickness value of just  $\sim 1\ \mu\text{m}$ , the line resistance values in Figure 4.9 are still pretty good. By thickening the metal layers on the fingers it would be possible to improve the line resistance of the fingers. The estimated resist layer for the lift-off process was around  $\sim 5\text{--}6\ \mu\text{m}$ , meaning that the contacts could be further thickened by increasing the sputtering time for Ag. However, this is a very time-consuming method with the cooling times in between. Thus, some other methods could be considered, for example, electroless plating or electroplating.



## Chapter 5

# Conclusions

This thesis aimed to find optimized sputtering parameters for the Ti/Pt/Ag stack to fabricate good ohmic contacts on black silicon (b-Si) surface. Black silicon surfaces have been found to have exceptionally good optical properties for applications like solar cells with their reflectivities as low as only  $\sim 1\%$  over a wide range of visible light. However, conventional front contact fabrication methods have been shown to result in nonconformal contacts on b-Si surfaces. This thesis aimed to optimize the use of a widely used industrial sputtering deposition method for the black silicon surface.

Samples were fabricated and characterized in Aalto University Micronova facilities, e.g. cleanroom and analyzing laboratory. Black silicon nanostructures were formed by Inductively Coupled Plasma Reactive-Ion Etching (ICP-RIE) method. Two different patterning methods were used to produce the wanted front metal contacts. The first patterning method was a simple steel shadow mask, however, the shadow mask proved to be problematic as it shadowed the b-Si surface excessively and thus the small finger and Transfer Length Method (TLM) structures were not properly formed. Hence, a second patterning method was chosen, and a standard lift-off process was implemented for the b-Si metal contact formation. Sputtering was conducted by varying the sputtering power and sputtering time. The hypothesis was that with lower sputtering power and thus lower sputtering yield, the resulting metal layer would be more conformal on the b-Si structure. Scanning

## CHAPTER 5. CONCLUSIONS

Electron Microscope (SEM) was used to take high magnification images to study the conformality of the sputtered layers. For electrical measurement, a Probestation was used for four-point TLM measurements to gain the contact resistance and specific contact resistivity results. Line resistance values were measured with a simple multimeter.

The conformality of the sputtered Ti/Pt/Ag finger structures was shown to be much better compared to initial experiments with standard Al recipe. The measured TLM results of specific contact resistivity  $\rho_c$  (1.27–2.48  $\text{m}\Omega\cdot\text{cm}^2$ ) were in range with literature ( $\leq 2 \text{ m}\Omega\cdot\text{cm}^2$ ). The nanostructures on the samples used in this thesis have a much higher aspect ratio, and considering that the results are similar to previous studies on flat silicon surfaces, the acquired  $\rho_c$  values are promising. Line resistance values were higher as compared to planar surfaces reported in literature, which was most likely due to the much lower thickness of contacts compared to those studies. Higher line resistance affects the total output current of the solar cell and thus decreases the efficiency.

This thesis has shown that by changing the sputtering parameters (lowering the sputtering power and increasing the sputtering time), it is possible to achieve conformal, good ohmic front metal contacts on black silicon surface that might even have the possibility to surpass conventional screen-printing methods by further optimization. This offers great promise for further research in the field of b-Si metallization and to achieving more efficient solar cells with good antireflective properties. Sputtering is a standard method industrially, which is a desirable trait for further development. The challenge is to find simple enough patterning methods, as lift-off takes significantly much more time and increases the number of processing steps compared to a steel shadow mask or screen-printing. Also, increasing thickness of the finger structures enough by sputtering is slow.

By further optimizing the sputtering parameters and thickening the finger structures, it could be possible to achieve conformal, good ohmic contacts and also to increase the efficiency of b-Si solar cells. The goal of this thesis was to study the possibility of optimizing the sputtering parameters for Ti/Pt/Ag front metal contacts and the results were already promising but

## *CHAPTER 5. CONCLUSIONS*

further research would be needed to find the optimum amount of each material to minimize contact resistance and to make sure the Ti layer is covered enough so that it is not oxidized in the long run. Other materials like Al could be further investigated also. Research on optimizing the patterning methods and finding a simple and industrially compatible method is needed.

# References

- [1] C. Hsu, J. Wu, Y. Lu, D. J. Flood, A. R. Barron, and L. Chen. Fabrication and characteristics of black silicon for solar cell applications: An overview. *Materials Science in Semiconductor Processing*, 25:2–17, Sep 2014.
- [2] C. B. Honsberg and S. G. Bowden. Photovoltaics education website. <https://www.pveducation.org/> (in English). Accessed August 6th, 2019.
- [3] X. Liu, P. R. Coxon, M. Peters, B. Hoex, J. M. Cole, and D. J. Fray. Black silicon: fabrication methods, properties and solar energy applications. *Energy Environ. Sci*, 7(10):3223–3263, 2014.
- [4] M. Roumanie, C. Delattre, F. Mittler, G. Marchand, V. Meille, C. de Bellefon, C. Pijolat, G. Tournier, and P. Pouteau. Enhancing surface activity in silicon microreactors: Use of black silicon and alumina as catalyst supports for chemical and biological applications. *Chemical Engineering Journal*, 135(Sup 1):S317–S326, 2008.
- [5] M. A. Juntunen, J. Heinonen, V. Vähänissi, P. Repo, D. Valluru, and H. Savin. Near-unity quantum efficiency of broadband black silicon photodiodes with an induced junction. *Nature Photonics*, 10(12):777–781, Dec 2016.
- [6] P. Repo, J. Benick, V. Vähänissi, J. Schön, G. von Gastrow, B. Steinhäuser, M. C. Schubert, M. Hermle, and H. Savin. N-type black silicon solar cells. *Energy Procedia*, 38:866–871, 2013.

## REFERENCES

- [7] D. K. Schroder. *Semiconductor Material And Device Characterization*. John Wiley & Sons, 3rd edition, 2006.
- [8] D. K. Schroder and D. L. Meier. Solar cell contact resistance-a review. *IEEE Transactions on Electron Devices*, 31(5):637–647, May 1984.
- [9] M. Musztyfaga-Staszuk, D. J., and P. Panek. Correlation of different electrical parameters of solar cells with silver front electrodes. *Materials*, 12(3), Jan 1, 2019.
- [10] M. M. Hilali, A. Rohatgi, and B. To. Review and understanding of screen-printed contacts and selective-emitter formation: Preprint. In *14th Workshop on Crystalline Silicon Solar Cells and Modules*, United States, Aug 1, 2004.
- [11] J. S. Yoo, I. O. Parm, U. Gangopadhyay, K. Kim, S. K. Dhungel, D. Mangalaraj, and J. Yi. Black silicon layer formation for application in solar cells. *Solar Energy Materials and Solar Cells*, 90(18):3085–3093, 2006.
- [12] Y. Xia, B. Liu, J. Liu, Z. Shen, and C. Li. A novel method to produce black silicon for solar cells. *Solar Energy*, 85(7):1574–1578, 2011.
- [13] S. Zhong, B. Liu, J. Liu, J. Liu, Y. Xia, Z. Shen, Z. Xu, and C. Li. Influence of the texturing structure on the properties of black silicon solar cell. *Solar Energy Materials and Solar Cells*, 108:200–204, Jan 2013.
- [14] J. Liu, J. Liu, S. Liu, B. Liu, Z. Shen, S. Zhong, C. Li, and Y. Xia. Characterization of PIII textured industrial multicrystalline silicon solar cells. *Solar Energy*, 86(10):3004–3008, Oct 2012.
- [15] I. R. Putra, J. Li, and C. Chen. 18.78% hierarchical black silicon solar cells achieved with the balance of light-trapping and interfacial contact. *Applied Surface Science*, 478:725–732, Jun 1, 2019.

## REFERENCES

- [16] E. Cabrera, S. Olibet, D. Rudolph, E. Wefringhaus, R. Kopecek, D. Reinke, and G. Schubert. Influence of surface topography on the glass coverage in the contact formation of silver screen-printed Si solar cells. *IEEE Journal of Photovoltaics*, 3(1):102–107, Jan 2013.
- [17] S. Franssila. *Introduction to microfabrication*. Wiley, Chichester, 2004.
- [18] G. von Gastrow, E. Calle, P. Ortega, R. Alcubilla, A. Daniil, E. Z. Stutz, A. Fontcuberta i Morral, S. Husein, T. Nietzold, M. Bertoni, and H. Savin. Metallized boron-doped black silicon emitters for front contact solar cells. In *2017 IEEE 44th Photovoltaic Specialist Conference (PVSC)*, pages 944–947. IEEE, Jun 2017.
- [19] J. Oh, H. Yuan, and H. M. Branz. An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures. *Nature nanotechnology*, 7(11):743–748, Nov 2012.
- [20] T. Gimpel, K. Guenther, S. Kontermann, and W. Schade. Study on contact materials for sulfur hyperdoped black silicon. In *2011 37th IEEE Photovoltaic Specialists Conference*, page 2061. IEEE, Jun 2011.
- [21] M. Steglich, T. Käsebier, I. Höger, K. Füchsel, A. Tünnermann, and E. Kley. Black silicon nanostructures on silicon thin films prepared by reactive ion etching. *Chinese Optics Letters*, 11:S10502, Apr 19, 2013.
- [22] P. Repo, A. Haarahiltunen, L. Sainiemi, M. Yli-Koski, H. Talvitie, M. C. Schubert, and H. Savin. Effective passivation of black silicon surfaces by atomic layer deposition. *IEEE Journal of Photovoltaics*, 3(1):90–94, Jan 2013.
- [23] H. Fischer and R. Gereth. Electrochemically passivated contacts for silicon solar cells. *IEEE Transactions on Electron Devices*, 18(8):459–464, Aug 1971.
- [24] A. Mette, D. Pysch, G. Emanuel, D. Erath, R. Preu, and S. W. Glunz. Series resistance characterization of industrial silicon solar cells with

## REFERENCES

- screen-printed contacts using hotmelt paste. *Progress in Photovoltaics: Research and Applications*, 15(6):493–505, Sep 2007.
- [25] J. A. Silva, M. Gauthier, C. Boulord, C. Oliver, A. Kaminski, B. Semmache, and M. Lemiti. Improving front contacts of n-type solar cells. *Energy Procedia*, 8:625–634, 2011.