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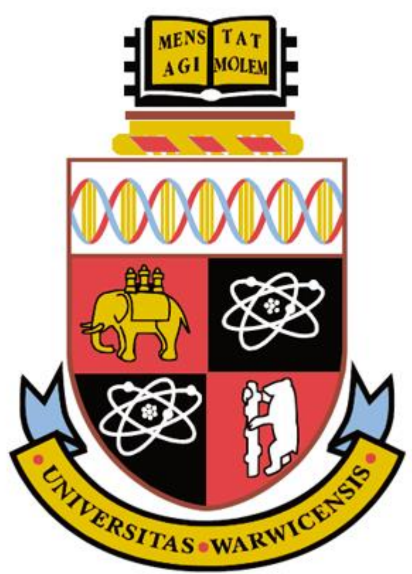
Design, simulation and fabrication of 4H-SiC Power MOSFETs



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A thesis submitted in partial fulfilment of the requirements for the degree of

Doctor of Philosophy

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Declaration

This thesis is submitted in partial fulfilment for the degree of Doctor of Philosophy under the regulations set out by the Graduate School at the University of Warwick. I certify that this thesis does not incorporate any material without acknowledgement previously submitted to any institution for a higher degree or previously published. The work is this thesis is my own except where stated, under the supervision of Dr Mike Jennings and Prof Phil Mawby.

Tianxiang Dai

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List of publications

1. T. Dai *et al*., "4H-SiC trench MOSFET with integrated fast recovery MPS diode," in *Electronics Letters*, vol. 54, no. 3, pp. 167-169, 2018

2. T. Dai, Z. Mohammadi, S. A. O. Russell, C. A. Fisher, M. R. Jennings and P. A. Mawby, "4H-SiC trench structure fabrication with Al_2O_3 etching mask," *2016 European Conference on Silicon Carbide & Related Materials (ECSCRM)*, Halkidiki, Greece, pp. 1-1, 2016

3. T. Dai, P. M. Gammon, V. A. Shah, X. Deng, M. R. Jennings and P. A. Mawby, "Design optimisation of 1.2kV 4H-SiC trench MOSFET", Manuscript submitted for publication, 2018

4. H. Rong, Y. Sharma, T. Dai, F. Li, M. Jennings, and P. Mawby, "High temperature nitridation of 4H-SiC MOSFETs", *Materials Science Forum*, Vols. 858, pp. 623-626, 2016

5. S. A. O. Russell, M. R. Jennings, T. Dai, F. Li, D. P. Hamilton, C. A. Fisher, Y. K. Sharma, P. A. Mawby, Amador Perez-Tomas, "Functional oxide as an extreme high-k dielectric towards 4H-SiC MOSFET incorporation", *Materials Science Forum*, Vols. 897, pp. 155-158, 2017

6. X. Deng, Y. Guo, T. Dai, C. Li, X. Chen, W. Chen, Y. Zhang, Bo Zhang, "A robust and area-efficient guard ring edge termination technique for 4H-SiC power MOSFETs, *Materials Science in Semiconductor Processing*, Volume 68, pp. 108-113, 2017

Abstract

For a 4H-SiC MOSFET to compete with Si counterparts, especially at lower voltages (1.2kV), the channel resistance contributes to a significant part in the total on-state resistance which must be addressed. Since most of the commercially available SiC wafer materials are grown on the {0001} crystal plane, a trench-gate MOSFET is necessary to take the advantage of the higher reported channel mobility on the $\{11\bar{2}0\}$ crystal plane.

1.2kV trench MOSFET design and fabrication is the main focus in this work. The micro-trench free dry etching process has first been developed with a systematic study on the dry etching parameters. Trench corner rounding has also been investigated since a rounded corner is normally preferred to avoid an electric field hot spot. Two generations of trench MOSFETs have been designed and fabricated. The 1st generation devices have been used to validate the fabrication process. A maximum breakdown voltage of 1600V has been achieved for the 1st generation devices. The p+ trench bottom shielding region provides the protection for the trench gate oxide since it shifts the peak electric field from the oxide/semiconductor interface to a semiconductor p-n junction; however, it also introduces a parasitic JFET region into the trench MOSFET structure which severely degraded the on-state performance of the 1st generation devices. The 2nd generation devices were designed to eliminate the effect of the parasitic JFET region and improve the on-state performance. The optimised device structure with a current spreading layer (CSL) and p+ implantation clearance in the 2nd generation design has successfully eliminated the effect of the parasitic JFET region. Further design and process optimisation is necessary to increase the current density of the device which was as low as $3A/cm^2$. A fabrication trial has been carried out on the MOSFETs with integrated Schottky contacts at the termination region and therefore, external Schottky diodes are not necessary for many applications.

A 10kV DMOSFET has also been designed and fabricated with maximum breakdown voltage at 13.6kV. The high voltage termination design options have been discussed among the floating field ring (FFR) termination and the junction termination extensions (JTEs). The on-state performance is poor due to a photo mask error on the JFET length which needs to be optimised for the next generation devices.

Novel device structures have been studied with simulation. These include trench MOSFET with integrated Schottky diode and 3.3kV superjunction trench MOSFET. The MOSFET with integrated Schottky diode not only reduces the chip area consumption, but also reduces the chip count in the system level. In the proposed design, the Schottky contact is placed at the bottom of the trench structure for the first time. The superjunction structure has a great potential for SiC devices rated at above 3.3kV. The proposed design

uses implanted p-pillar with a trench gate structure which combines the benefits of low channel resistance and low drift region resistance.

Abbreviations

Si	Silicon
SiC	Silicon Carbide
GaN	Gallium Nitride
SCR	Silicon Controlled Rectifier
SJ	Superjunction
E_g	Band Gap
E_{cr}	Critical Electric Field
λ	Thermal Conductivity
V_{sat}	Saturation Drift Velocity
HVDC	High Voltage Direct Current
MOS	Metal Oxide Semiconductor
μ	Mobility
μ_{FE}	Field Effect Mobility
μ_{eff}	Effective Mobility
ε_S	Semiconductor Relative Permittivity
ε_{ox}	Oxide Dielectric Constant
ε_o	Free Space Permittivity
BFOM	Baliga's Figure of Merit
CVD	Chemical Vapor Deposition
HTCVD	High Temperature Chemical Vapor Deposition
PVT	Physical Vapour Transport
RF	Radio Frequency
TSD	Threading Screw Dislocation
TED	Threading Edge Dislocation
BPD	Basal Plane Dislocation
SiH_4	Silane
C_3H_8	Propane
HCl_3Si	Trichlorosilane
C_2H_4	Ethylene
SRIM	The Stopping and Range of Ions in Matter
TCAD	Technology Computer-Aided Design
SIMS	Secondary Ion Mass Spectrometry
AFM	Atomic Force Microscopy
SEM	Scanning Electron Microscopy
TLM	Transmission Line Measurement
CV	Capacitance-Voltage
R_c	Contact Resistance
L_T	Transfer Length
R_{sh}	Sheet Resistance
ρ_c	Contact Resistivity
D_{it}	Interface Trap Density
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
C_{ox}	Oxide Capacitance

C_{lf}	Low Frequency Capacitance
C_{hf}	High Frequency Capacitance
A	Area
Al	Aluminium
V_{th}	Threshold Voltage
I_D	Drain Current
J_D	Drain Current Density
V_{DS}	Drain Source Voltage
V_{GS}	Gate Source Voltage
$R_{channel}$	Channel Resistance
g_m	Transconductance
POA	Post-Oxidation Annealing
RCA	Radio Corporation of America
RTA	Rapid Thermal Annealing
PSG	Phosphosilicate Glass
JFET	Junction Field Effect Transistor
E_{ox}	Oxide Electric Field
E_s	Semiconductor Electric Field
CSL	Charge Storage Layer or Current Spreading Layer
RIE	Reactive Ion Etching
ICP	Inductively Coupled Plasma
TEOS	Tetraethyl Orthosilicate
LPCVD	Low Pressure Chemical Vapor Deposition
SF_6	Sulfur Hexafluoride
rms	Root Mean Square
sccm	Standard Cubic Centimetre per Minute
JTEs	Junction Termination Extensions
FFR	Floating Field Ring
PEB	Post Exposure Bake
JBS	Junction Barrier Diode
MPS	Merged PiN Schottky
BV	Breakdown Voltage
N_D	Donor Concentration
AMS	Adjusted Multi-Section
τ	Minority Carrier Lifetime

Chapter 1 Introduction

The first industrial revolution started in late 1700s and it brought the human society into the era of mechanisation. The mechanisation of industry was enabled by the development of the new steam engine by James Watt. If steam energy is the symbol for the first industrial revolution, then electricity did the same for the second industrial revolution that started approximately one century later. The way we live today has been completely changed with inventions like telegraph, light bulb, the car and many more. The third revolution is normally referred to as that of information technologies and renewable energies which started in approximately 1970s. There is a common topic across all the three revolutions which is the utilization of energy no matter if it is the steam energy, electricity or the renewable energies nowadays.

1.1 Energy revolution and climate change

The topic of energy crisis has been discussed extensively in the last half century. Oil, coal and natural gas so-called fossil fuels are the main energy sources in the world that are used to power vehicles, feed manufacturing industry, heat houses and supply the electricity for everyday life. Before the 1970s, more than 94% of energy consumption was from fossil fuels according to data from the World Bank Group [1]. The global energy demand has increased by approximately 44% from 1971 to 2014 (1920.655 kg of oil equivalent per capita) [1]. The rapid increase of the energy demand has been driven by the population and economic growth. Given that the fossil fuels storage is limited, if no restrictions are applied to their consumption, there will be no fossil fuels left after several decades.

Climate change is another issue associated with burning fossil fuels which is having global impact. Burning of fossil fuels produces carbon dioxide (CO_2), which will interact with incident solar energy and cause the climate change over the world [2]. The average CO_2 level was 280 ppm in the atmosphere before industrialisation, this number has increased to 410ppm in 2018 [3]. It will be a catastrophe for some coastal cities if the sea

level is increased due to elevated average temperature [4]. As a result, it is not any single country but every country's responsibility to control the greenhouse gas emission to prevent or reduce the impact of human behaviour to the environment.

Renewable energy technologies were introduced to the energy market due to their sustainable and pollutant free nature [5]. In 1998, only 2% of world energy supply was generated from renewable energy sources which was mainly biomass energy [6]. In 2015, 15% of the global energy demand was supplied by renewable energy sources [7]. Renewable energy sources have become an important player in the energy market after two decades' steady growth and they are still growing.

The energy revolution is happening, however, Rome was not built in a day. Fossil fuels, as traditional energy sources, will keep supply the world energy for a long period of time. Improving energy efficiency is possibly the most important means for reducing the energy demand and so greenhouse gas emissions [8].

Electricity is more versatile and controllable compared to other energy forms. Electrical power can be generated from clean energy sources such as hydropower, solar and wind energy, it can be transported and distributed in the most efficient way. Nowadays, the policy makers are pushing to increase the electrification of industry and transportation. Many countries set their electric vehicles targets to reduce emissions, more electric airplane like the Airbus A380 have started to operate commercially more than ten years ago. In the airline industry, the power demand is driven by many factors like the society, technology, environment, economy and politics [30].

The evolution of the energy end users has indicated that electrical energy demand will keep increasing in the long term. The accessibility of electricity, the boost of the population and GDP growth are the main driving forces for the increased demand of electricity.

Power loss is generated during electricity generation, transportation, distribution and the final stage by the end users. To reduce power loss and improve the power conversion efficiency, there is an important and enabling technology available namely power electronics.

1.2 Power electronics – the enabling technology

Power electronics is a technology that uses solid state electronics to convert, control, and condition electrical energy in an efficient way [9-12]. Power electronics was born in 1902 when Peter Cooper-Hewitt invented the mercury-arc rectifier which was capable of transforming alternating currents to direct currents for feeding dc motors. In the following decades, the ratings of mercury-arc rectifiers were gradually increased [13] and such devices were used extensively in power grid applications; it was also in those decades when the fundamental converter topologies were developed [14].

It is impossible to describe the history of power electronics without mentioning the development of power semiconductor devices. The silicon-controlled rectifier (SCR) was first commercialised in early 1958 which was marked as a starting point of power electronics revolution [14]. The later development of thyristor, MOSFET, and IGBT technologies allowed power electronics to progress steadily with an increased number of applications.

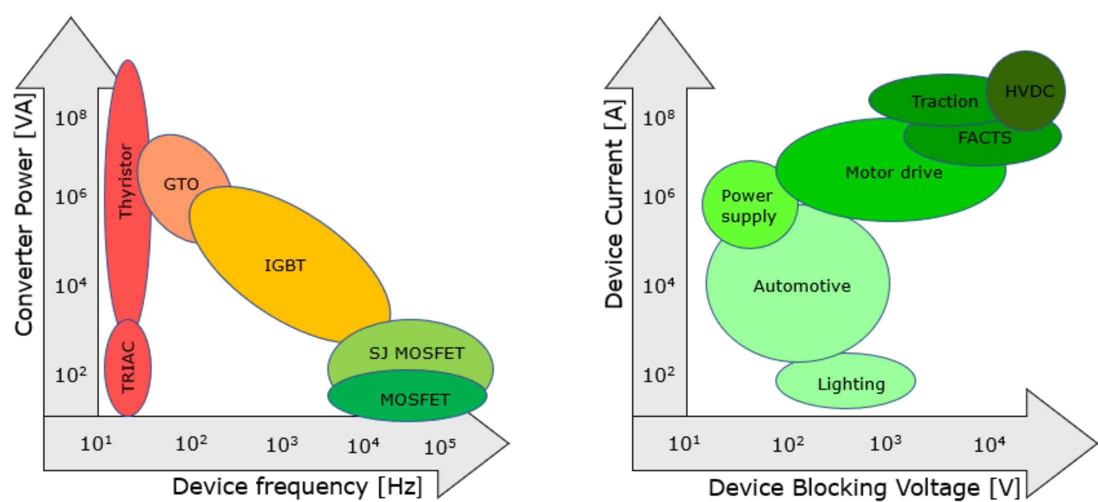

Fig. 1.1 a) Power and switching frequency ranges of the major power semiconductors; b) Power device ratings for various applications (adapted from [15])

The existence of various power device technologies reflects the diversity of power electronic applications. For applications like HVDC, high voltage and high current are usually needed while the semiconductor devices used in the automotive industry can be very different from the power grid. Fig. 1a shows the switching and power handling capabilities of different power semiconductors which have their own advantages and

disadvantages. Therefore, a wise selection of devices for specific applications is critical and it will affect the whole system design.

Power electronics is an enabling technology for the more electric society of the future, it is critical for smart grids and renewable energy networks [16]. Renewable energy plays a critical role in the energy revolution for reducing the greenhouse gas emission. The electricity generated by renewable energy sources like wind and solar is usually intermittent, therefore, power electronics is needed as an interface between renewable energy generation and the grid to regulate the voltage and frequency.

The increasing demand of power management has resulted in higher adoption of power electronics in the power grid, automotive, consumer electronics and many others. With the higher adoption of power electronics, the energy loss in the power electronics itself will become significant. To improve the converter efficiency, the energy loss will need to be minimised. Power semiconductor devices, as the main components in the power electronics converters, have a large impact on the system level design and total energy loss.

Silicon-based devices have been dominant in the power semiconductor market for many years and it is thought that the theoretical limit of the material fast being reached. The introduction of superjunction concepts in 1980s and 1990s have pushed silicon devices beyond the old theoretical limit [17-22]. The main application voltage range for superjunction devices varies from 500V to 800V and this voltage range has the potential to be extended [23]. In the 21st century, a new category of wide-bandgap semiconductor materials like silicon carbide (SiC) and Gallium Nitride (GaN) have been used to fabricate power semiconductor devices which opens a new chapter in modern power electronics.

1.3 Silicon carbide and other wide-bandgap semiconductors

The demand for high power density power converters operating in a harsh environment is growing rapidly, especially for applications such as automotive and aerospace. Although as mentioned in the last section, novel superjunction device structures have redefined the material limit of silicon by disconnecting the drift region doping concentration to the breakdown voltage, it is difficult for silicon-based power converters

to fulfil the requirements in some specific applications. Wide-bandgap device technology can bring current power electronics to the next level with increased power density, switching frequencies and junction temperatures [24].

Table 1.1 Fundamental properties of various semiconductor materials [25]

Property	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
Bandgap, E_g (eV)	1.12	1.43	3.03	3.26	3.45	5.45
Electrical breakdown field, E_c (kV/cm)	300	400	2,500	2,200	2,000	10,000
Thermal conductivity, λ (W/cm·K)	1.5	0.46	4.9	4.9	1.3	22
Saturated electron drift velocity, V_{sat} (10^7cm/s)	1	1	2	2	2.2	2.7

Table 1.1 summarises some of the most important parameters of different semiconductor materials. SiC and GaN, as the 3rd generation wide-bandgap semiconductor material, have superior physical properties over conventional Si power devices. The SiC bandgap energy is approximately three times larger than that of silicon while GaN bandgap is slightly higher than SiC. Silicon devices can operate up to 200°C without abnormal behaviour, even though the devices were rated at 150°C [26]. Theoretically, silicon carbide has an intrinsic temperature higher than 650°C [27] and NASA demonstrated stable operation of SiC JFETs at 500°C for more than 3000 hours [28]. Despite the low thermal conductivity, GaN devices have been tested for a temperature up to 900° [33] where the metallisation was the first failure mechanism instead of the material structure itself. The packaging technology must be upgraded in order to fully utilise the full potential of SiC and GaN devices. Most of the GaN devices are fabricated on Si substrate benefiting from the mature Si industry and therefore low cost. GaN on Si requires a non-conductive interlayer which makes it less possible for vertical devices. As a result, SiC and GaN have their own advantages at different voltage ratings with an intersection voltage. SiC devices will prevail at above the intersection voltage which is approximately 1000V and it will change along the advancement of the fabrication technology [34]. The breakdown electric field of SiC devices is at least seven times of Si devices which means the drift region of SiC devices can be made much thinner without compromising the breakdown voltage. In other words, SiC devices for the same voltage rating will have much lower on-state resistance compared to their Si counterparts.

Power electronic converters can benefit from SiC devices with less cooling required due to lower power losses and high thermal conductivity of SiC devices. In addition, the higher electron saturation velocity increases the switching speed of SiC devices and passive filtering components can be shrunk in size at elevated switching frequency.

Despite all the advantages, SiC does not have a perfect SiC/SiO_2 interface which leads to a high interface trap densities and lower channel mobilities for MOS-based devices. Nowadays, the channel mobility extracted from most fabricated devices is more than 20 times smaller than the bulk mobility. For a 4H-SiC MOSFET to compete with Si counterparts especially at lower voltages (1.2kV), the channel resistance contributes to a significant part in the total on-state resistance which must be reduced. Since most of the commercially available SiC wafer material is grown on the {0001} crystal plane, a trench-gate MOSFET is necessary to take the advantage of the higher reported channel mobility on the $\{11\bar{2}0\}$ crystal plane [29].

In 2001, SiC Schottky diode was first introduced to the market. Ten years later, SiC MOSFETs became commercially available. A market size of 302 million US dollars had been reached in 2017 for silicon carbide power semiconductors, which is still less than 1% of the total power semiconductor market size [31,32]. Nowadays, the commercially available SiC MOSFET voltage ratings vary from 650V to 1700V with a maximum current rating up to 200A per chip.

1.4 Thesis outline

This thesis focuses on the design and fabrication of 1.2kV trench MOSFET and 10kV DMOSFET. The next chapter reviews 4H-SiC material growth, semiconductor characterisation techniques and device concepts. Chapter 3 studies thermal oxidation and post-oxidation annealing processes. MOS capacitors and lateral MOSFETs were fabricated to extract the interface trap density and the channel mobility respectively. Chapter 4 provides a systematic study on the trench structure dry etching process. Al_2O_3 was used as dry etching mask instead of SiO_2. The target was to fabricate a trench structure without micro-trenches and ready for trench MOSFET fabrication in the next stage. In Chapter 5, the first-generation trench MOSFET devices were fabricated and characterised with a design target of 1200V. In the following chapter, the second-generation trench

MOSFETs were designed and fabricated trying to optimise the on-state performance of the devices. Chapter 7 presents the results of 10kV planar gate vertical MOSFET devices partially fabricated in Warwick cleanroom. This was a collaboration work between the University of Warwick and University of Electronic Science and Technology of China. Chapter 8 proposes some novel device structures based on simulation and previous experimental results. The thesis concludes at Chapter 9 with a summary and future work that can be done to optimise the device design and fabrication process.

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Chapter 2 SiC properties, bulk growth and characterisation

This chapter reviews physical properties and material growth of silicon carbide followed by the introduction of the physical and electrical characterisation techniques used in this study. Finally, the MOSFET device structure and operation principle will be outlined.

2.1 SiC polytypes

Silicon carbide is a covalently bonded compound semiconductor. Unlike silicon, silicon carbide has many different crystal structures called polytypes with identical SiC atomic layers being stacked in difference sequences [1]. Two tetrahedron bond rotation types exist in the silicon carbide crystal structure as shown in Fig. 2.1 where the second type can be obtained by rotating the first one along the c-axis by 180° (vertical axis in the figure). One type is responsible for zincblende stacking and the other one is responsible for wurtzite stacking.

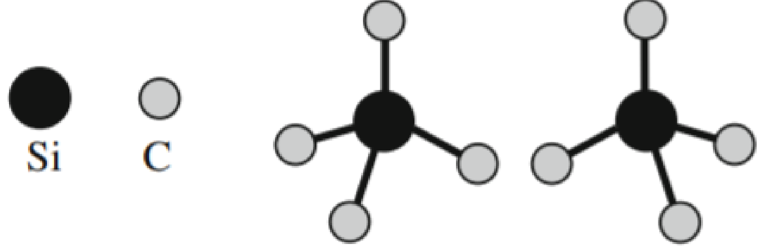

Fig. 2.1 Two fundamental types of tetrahedrons forming the building blocks of all the different SiC polytypes

There are three types of Si-C double-atomic layers in total named as A, B and C as shown in Fig. 2.2. Any specific SiC polytype can be formed by modifying the stacking sequence of A, B and C double-atomic layers. For instance, 3C-SiC has a stacking sequence of ABCABC which is identical to the cubic structure for silicon with half of the

atoms replaced by carbon. The letter "H" in 4H-SiC represents the hexagonal crystal structure like the letter "C" in 3C-SiC which stands for cubic structure.

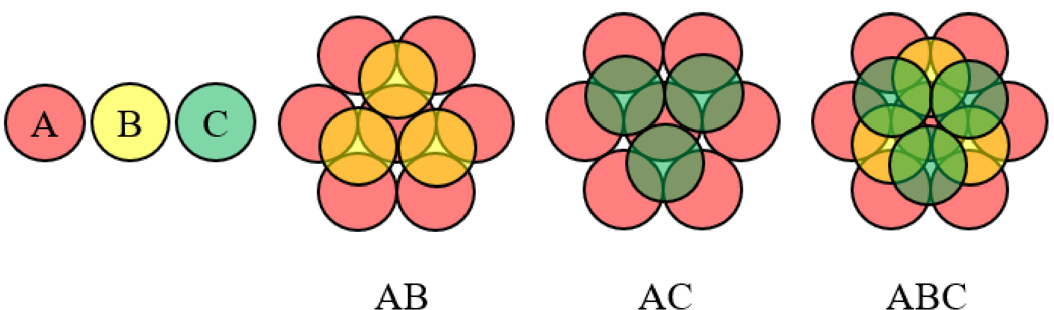

Fig. 2.2 Two fundamental types of tetrahedrons forming the building blocks of all the different SiC polytypes [2]

Even though there are over 200 SiC polytypes in theory, not many of them can be reproduced stably and therefore most of the polytypes are not favoured as electronic device material. Fig. 2.3 presents the SiC polytypes that are the most stable and mature. 4H-SiC has the stacking sequence of ABCB before it starts to repeat and the "6H" for 6H-SiC is named after the stacking sequence of ABCACB.

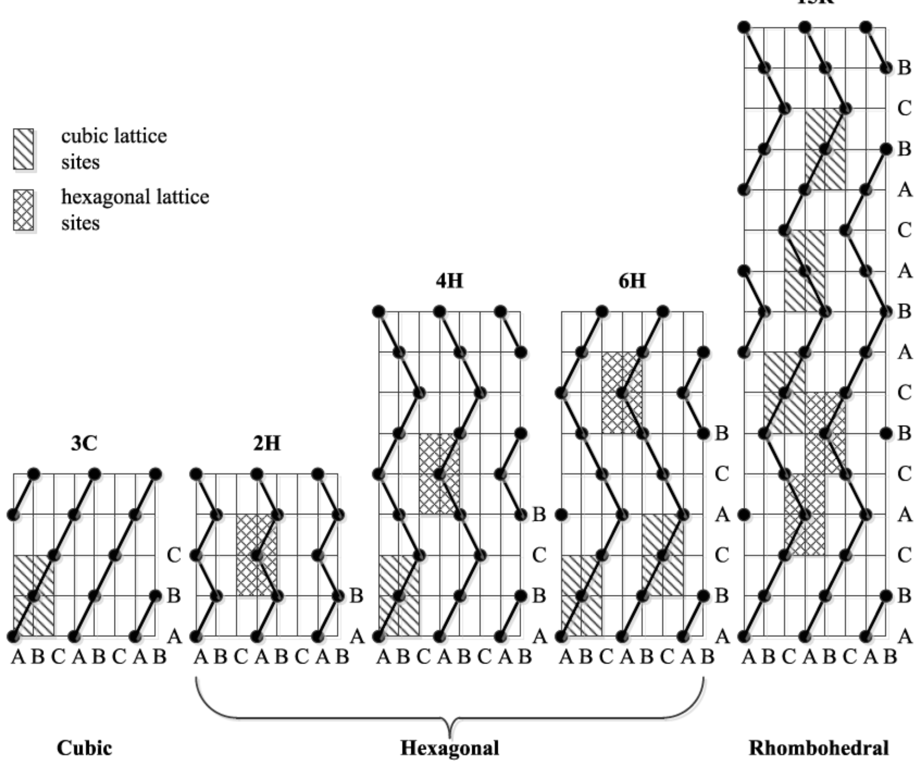

Fig. 2.3 Most favourable SiC polytypes in electronic applications [3]

As near interface traps are lower in density for the 3C-SiC metal-oxide-semiconductor (MOS) structure, compared to 4H-SiC, 3C-SiC offers the advantage of higher channel mobility [4]. The higher channel mobility was proved by the results of fabricated n-channel MOSFET based on 3C-SiC material [5,6]. Nowadays, most of the 3C-SiC material is heteroepitaxially grown on Si substrates which means lower production cost compared to 4H-SiC grown on 4H-SiC substrate. However, the 3C-SiC grown on Si substrates experiences 20% crystal mismatch and therefore, generates large amounts of extended defects which makes it difficult to fabricate both lateral and vertical devices [4]. It is suggested that part of these defects is possible to be eliminated by growing relatively thick SiC epilayers. There is a self-annihilation mechanism as two stacking faults intersect, either one or both the two defects will be eliminated. In this case, thicker epilayer can result in a higher chance of self-annihilation. It is also important to mention that SiC thermal expansion coefficient (CTE) is 8% different from silicon which can lead to a bow or cracks in the wafer [32]. To summarise, although 3C-SiC offers certain advantages, the crystal growth of 3C-SiC remains an issue that limits the wider adoption of this polytype for the fabrication of power semiconductor devices.

4H-SiC and other polytypes of silicon carbide have different physical properties across many aspects. For instance, the bulk electron mobility perpendicular to the c-axis is plotted for both 4H-SiC and 6H-SiC as shown in Fig. 2.4. The electron mobility of 4H-SiC is more than twice of 6H-SiC for doping concentration below $5\times10^{17}cm^{-3}$. This is not the worst case for 6H-SiC, the mobility of 6H-SiC along the c-axis is 20-25% of the value perpendicular to the c-axis, where in 4H-SiC the mobility increases to 120%. For vertical devices fabricated on {0001} wafer, 6H-SiC is lost in the competition. A more detailed comparison between 3C-SiC, 4H-SiC and 6H-SiC is made in Table 2.1.

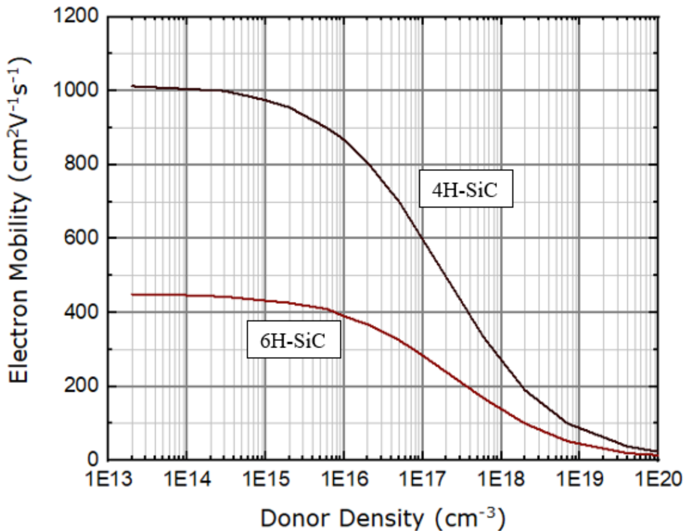

Fig. 2.4 Low field bulk electron mobility plotted against donor density for 4H- and 6H-SiC [7]

Table 2.1 The comparison of the major physical properties between 3C-SiC, 4H-SiC and 6H-SiC [7].

Properties	3C-SiC	4H-SiC	6H-SiC
Bandgap (eV)	2.36	3.26	3.02
Electron mobility ($cm^2V^{-1}s^{-1}$)			
μ perpendicular to c-axis	1000	1020	450
μ parallel to c-axis	1000	1200	100
Breakdown electric field (MV cm^{-1})			
E_B perpendicular to c-axis	1.4	2.2	1.7
E_B parallel to c-axis	1.4	2.8	3.0
Relative dielectric constant			
ε_S perpendicular to c-axis	9.72	9.76	9.66
ε_S parallel to c-axis	9.72	10.32	10.03
BFOM (n-type, parallel to c-axis)	61	626	63

Table 2.1 provides a summary of the most important physical properties of 3C-SiC, 4H-SiC and 6H-SiC material. Baliga's figure-of-merit (BFOM) for low frequency is included in the table which is basically made up by the product of $\varepsilon_S\mu E_B^3$ for the quick evaluation of material properties for vertical devices. It generates much higher value of

BFOM for 4H-SiC compared to the other two polytypes which explains why 4H-SiC has been used extensively for the fabrication of power devices [7].

2.2 Bulk growth and defects

As the properties of the major SiC polytypes have been studied in last section, this section reviews the main method that is used to grow the bulk crystal. SiC devices are still much more expensive than Si counterparts and large SiC wafers with good quality is the key to reduce the cost. Presently, the most commonly used technique for growing SiC bulk material is seeded sublimation method which is also called modified Lely method. Some alternative growth techniques have been developed which includes high-temperature chemical vapor deposition (HTCVD) and solution growth method.

HTCVD is a chemical deposition process which uses precursors and reactions normally happens at extremely high temperature (2100ºC – 2300ºC). There are several advantages for using HTCVD which includes higher purity, better C/Si ratio control and continuous supply of the source material. Solution growth method uses the congruent melt (solution) for the boule growth. This method is a common technique used for other semiconductor types. The solubility of carbon in the Si melt is as low as 15% even at 2800ºC which a challenge for solution growth method. Further development and optimisation are needed before this method can be widely adopted for SiC boule growth [7].

2.2.1 Sublimation growth (Physical Vapour Transport, PVT)

There are three steps involved in sublimation growth process where it 1) starts with the sublimation of the SiC source material followed by 2) the mass transport of sublimed species and 3) the final step is the condensation, surface reaction and crystallization [7].

Lely first applied the sublimation method to grow single crystalline SiC in 1955 [8]. The seeded sublimation method was then developed by Tairov and Tsvetkov which uses a high-quality seed layer to collect the sublimed SiC material [9,10]. A typical and simplified schematic of the crucible that is used for growing SiC boule is shown in Fig. 2.5 with the seed layer located on the top and SiC source material on the bottom of the crucible. The crucible is heated up with the radio frequency (RF) coil located outside the

crucible in the range of 1900-2400ºC. A temperature gradient inside the crucible is intentionally designed to keep the seed temperature lower than the SiC source material in order to direct the sublimed SiC species towards the seed layer, a typical value for this drop is 100ºC.

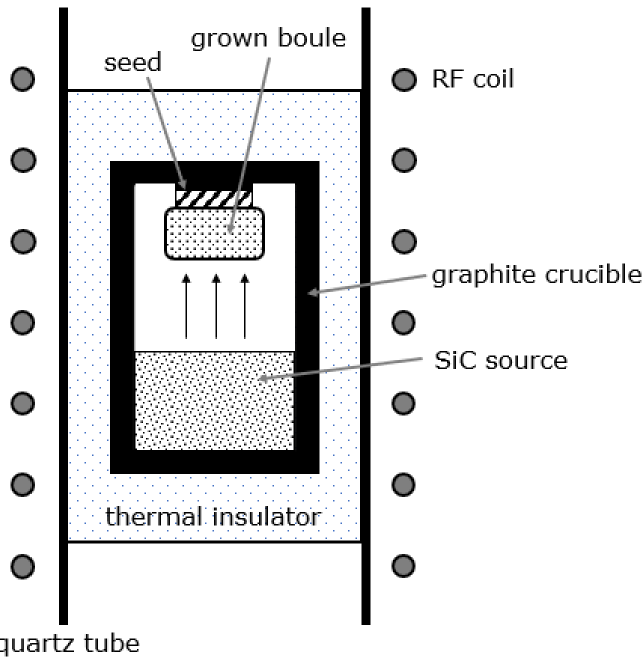

Fig. 2.5 Typical crucible layout for SiC growth with seeded sublimation method (adapted from [7])

The process control is critical for the growth of high-quality SiC boule material where the thermodynamic and kinetic conditions must be optimised. SiC source sublimation rate is mainly determined by the source temperature while the crucible pressure has a strong impact on the transport efficiency of the species [11].

Since SiC has many polytypes, it is crucial to be able to grow the specific single polytype for electronic applications. If the growth condition is not optimised, polytype mixing is possible to happen. It was reported by Knippenberg that 4H-, 6H-, 15R-SiC can often be observed at growth temperatures above 2000ºC [12]. It was suggested that the Si/C ratio in the sublimation growth ambient is closely related to the stability of the polytypes. For instance, 4H-SiC is more likely to be grown stability with higher percentage of carbon in the growth ambient [13]. It was also found in actual experiments that the polarity of the seed layer plays a decisive role for the determination of the SiC polytypes [14]. 4H-SiC is grown on the seed with {0001} crystal surface which is also

called carbon face and 6H-SiC is more favoured with {0001} silicon face. The static polytype stability can also be affected by the growth temperature and pressure. In contrast to 6H-SiC, relatively low temperature and pressure is the preferred condition to grow 4H-SiC single crystal [15]. In addition, it is believed that nitrogen incorporation can usually lead to a carbon-rich environment that stabilises 4H-SiC crystal which is why commercially available 4H-SiC substrates are often doped with nitrogen [7]. For the same reason of polytype control, it is difficult to fabricate p-type 4H-SiC substrates with aluminium doping which is also why not many SiC IGBTs have been demonstrated.

Even though the sublimation method is widely adopted by wafer manufacturers, it still has some problems. For instance, the SiC source material becomes carbon-rich during the growth process. Silicon needs to be added to the source material before the growth can be continued, this also means the SiC boule crystals are limited to the length between 30mm to 50mm if no modification is made to the crucible design [7].

2.2.2 Defects

There are four different types of major extended defects that exist during SiC bulk growth. Micropipes used to be the most destructive type of defect, which is a screw type dislocation with hollow core. Due to its pure screw nature and being macroscopic, micropipes are characteristically surrounded by large spiral steps on the SiC surface. The micropipe, so called the killer defect, will extend through the whole wafer which seriously degrades the device performance. There can be many reasons for the formation of micropipe defects. Thermodynamic and kinetic process imperfections may be responsible for micropipe generation as well as technical reasons like not carefully prepared seed layer and contamination [16]. Nowadays micropipe is no longer the most critical defect type for device fabrication since most manufacturers can produce almost micropipe-free wafers due to the optimised process control.

The three remaining defect types are threading screw dislocation (TSD), threading edge dislocation (TED) and basal plane dislocation (BPD). TSD defect creates a spiral with four Si-C bilayers step height for 4H-SiC. TSD defect is like the stairs in a building that connects first floor mistakenly to the third floor instead of the second floor. TSD defect can normally exist in the seed crystal and then being replicated into the SiC boule crystal [7]. It has been found that TSD defect can result in higher leakage currents and lower

breakdown voltages for fabricated 4H-SiC devices [17]. TED and BPD have a similar nature of having a crystal plane/half plane in the wrong place. BPD refers to the dislocation occurs in the basal plane while TED is defined for the dislocation along the {0001} direction. Like TSD, TED and BPD can be replicated from the seed crystal as well. For bipolar devices, BPD can severely degrade the performance when the minority carrier density reaches its threshold value [18].

More defects like downfall, carrot and triangular defects will be generated during epitaxial growth of SiC. The defects generated during bulk grow can propagate into the epitaxial grown layers as shown in Fig. 2.6.

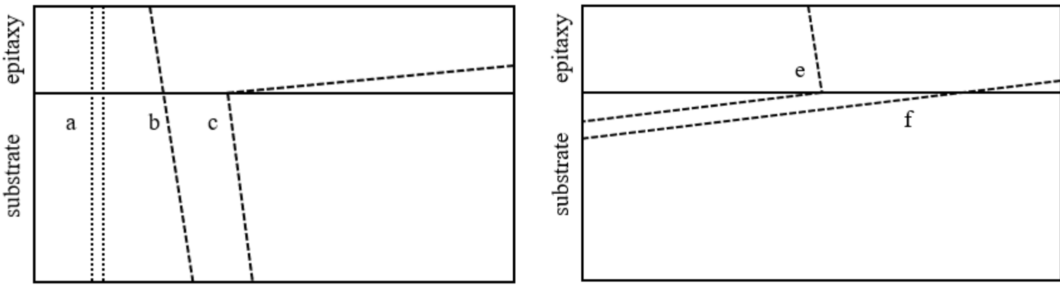

Fig. 2.6 Propagation of bulk growth defects into the epitaxial grown layer a) micropipe; b) TSD; c) TSD to carrot defect; e) BPD to TED; f) BPD [3]

It was reported that triangular and carrot defects can have a negative impact on the device blocking capability [19]. Since TSD and TED defects have negligibly small impacts on the device performance, BPD-TED conversion becomes significant in terms of device performance [18]. To summarise, the quality of SiC wafers can be improved if defect reduction is carefully applied to each of the growth steps including seed preparation, bulk growth and epitaxial growth.

2.2.3 Defect reduction

The RAF method (repeated a-face growth method) is one of the most effective techniques to reduce the number of extended defects in a SiC boule. This method does not focus on the optimisation of the growth conditions but instead, it is a technique to prepare high quality seed layers for subsequent sublimation growth. The preparation first starts with the normal growth process on {0001} seed which is apparently not dislocation free or high quality. A new seed layer can be acquired by slicing the boule in parallel to the growth direction which has less extended defects than the first one. This boule growth

and slicing new seed layer will be repeated for three times until a {0001} seed layer can be sliced out in which the level of dislocation is approximately three order of magnitude less than the initial seed layer [33].

Besides the seed layer preparation, the growth conditions also affect the defect levels. During a long sublimation growth, optimum temperature profile and pressure must be carefully maintained as well as the C/Si ratio from the source material.

2.3 Epitaxy, doping and ion implantation

4H-SiC wafer preparation consists of bulk crystal growth, slicing the bulk crystal into wafers, wafer polishing. Epitaxial growth, unlike the bulk growth, is the technique used to grow a SiC active layer with specific thickness and doping concentration for targeted device ratings.

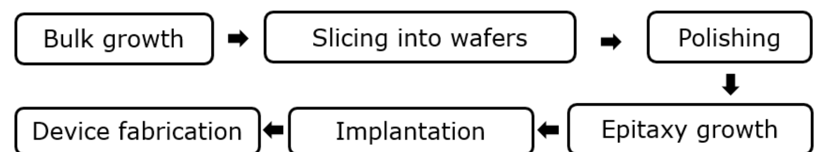

Fig. 2.7 Typical process flow from SiC bulk growth to device fabrication

Chemical vapor deposition (CVD) is the only method adopted by wafer manufacturers for 4H-SiC epitaxial growth [20]. The polytype control is important during epitaxial growth to maintain high quality single crystalline material. Homoepitaxial polytype control is achieved by "step flow control" on an off-cut wafer [21]. This mechanism is achieved by extending the steps on intentionally misoriented wafers in the slicing stage when steps from the {0001} planes are revealed as shown in Fig. 2.8.

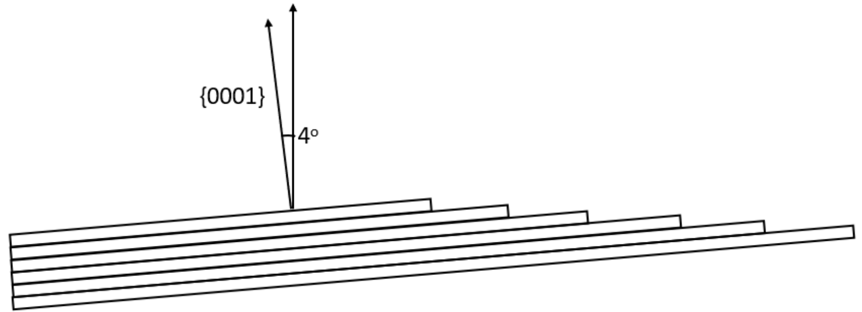

Fig. 2.8 Epitaxial growth on 4° off-angle towards the {0001} crystal face

Currently, 4° off-angle is most commonly used for 4H-SiC epitaxial growth. Standard processes involve silane (SiH_4) as Si-source and propane (C_3H_8) as C-source [21]. For production of standard layers, a Cl-based gas system is needed to achieve fast growth rates (either by the addition of HCL in gas or by using a chlorinated precursor) [22-24]. Growth rates of >100μm/h can be achieved using trichlorosilane (HCl_3Si) and ethylene (C_2H_4) [24]. Both p (Al) and n (N_2) doping are highly flexible with this method where doping values of 1×10^{14} to $1\times10^{19}cm^{-3}$ are routinely achievable. The doping concentration and thickness of the epitaxy layer must be controlled precisely with high uniformity to comply with the requirements of device design.

For Si devices, diffusion is a critical process for device fabrication. However, a diffusion process is not commonly used for SiC device fabrication due to the low diffusion coefficients for heavy ions like Al, therefore ion implantation has become the main doping technique during SiC device fabrication. Ion implantation has the advantage of selective region doping with controlled depth, doping concentration and limited lateral diffusion for SiC devices. Metals or dielectrics are used as masking films to block the implantation for the region that should not be implanted. The implanted ions with the highest energy must be kept inside the masking films which therefore needs to be thick enough.

Dopant ions will be accelerated to a certain energy with a defined dose before entering SiC crystal matrix. The energy of the ions determines how far on average they can travel in the targeting wafer. Implanted ions will need to be activated at a temperature up to 2000°C [25]. The implanted atoms need to compete with interstitial Si/C atoms during recrystallisation process. Higher temperature (500°C ~ 1000°C) implantation seems to be able to further improves the activation rate and reduce the implant damage to the crystal structure [26]. SRIM (The stopping and range of ions in matter) is a monte-carlo implantation simulation software which uses the transportation properties of ions in different materials to simulate dopant profiles after implantation. Implantation simulation can also be done with TCAD (Technology Computer-Aided Design) tools like Silvaco, Synopsys and others. A calibration step is normally needed when a specific ion beam service company is selected for the implantation process, otherwise the actual doping profile can be very different from the simulation results.

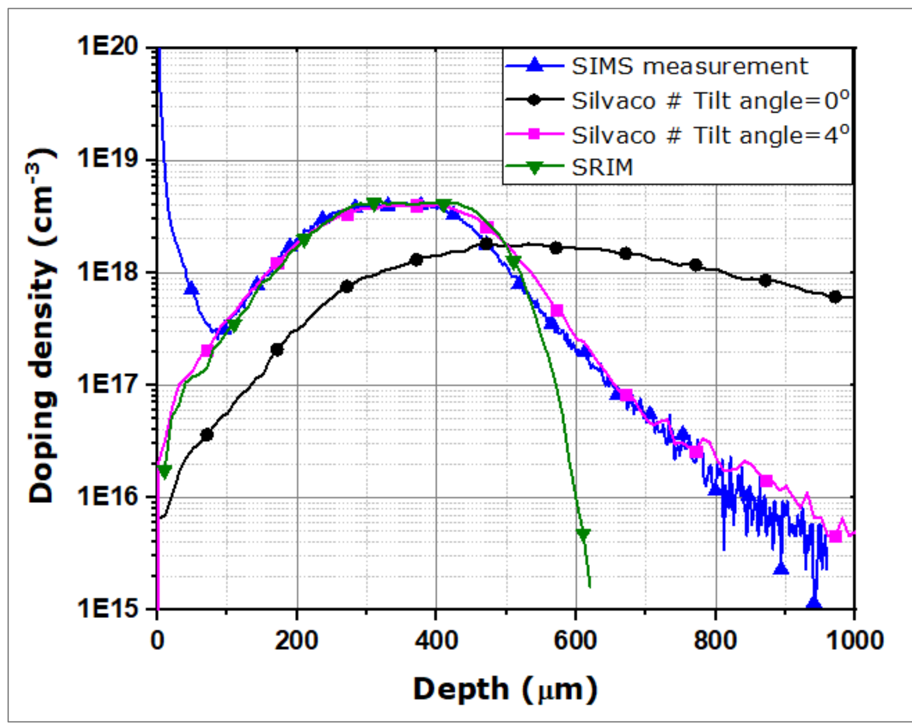

Fig. 2.9 Comparison of measurement and simulation results of p-type (Al) implantation

Table 2.2 The p-type implantation specification with Aluminum

	Energy (keV)	Dose (cm^{-2})
1st implant	350	8×10^{13}
2nd implant	230	4×10^{13}
3rd implant	30	1×10^{11}

P-type implantation with Al dopant was done by CuttingEdge Ions which is an ion beam service company in USA. Both SRIM and TCAD silvaco were used to calculate the doping concentration based on the implant energy and dose. Secondary ion mass spectrometry (SIMS) measurement was carried out after the implantation and the outcome is plotted together with the simulation results as shown in Fig. 2.9. The initial high doping concentration from SIMS measurement can be ignored which may be due to measurement errors or contamination. Tilt angle of 0° and 4° have both been simulated by TCAD Silvaco. With 0° tilt angle, the incoming ions align perfectly with the {0001} crystal face and a channelling effect will lead to much deeper implantation depth with reduced doping density [25]. Since most commercially available wafers are 4° off with

respect to {0001} silicon face, the simulation should not use 0° tilt angle to avoid channelling effect. With 4° tile angle, the results simulated with Silvaco agree well with the SIMS measurement results. SRIM simulation results also agree well to the measurement results except that the tail of the implantation is much steeper. Now that the simulation parameters have been proved valid, the same setup can be reused again and again for future device design without having to go through the SIMS measurement for every implantation.

2.4 Characterisation techniques

This section reviews the main characterisation techniques used in this thesis including both physical characterisation and electrical characterisation. The physical characterisation techniques consist of secondary ions mass spectrometry (SIMS), atomic force microscopy (AFM) and scanning electron microscopy (SEM). The electrical characterisation involves transmission line measurement (TLM), capacitance-voltage (CV) measurement.

2.4.1 Secondary Ion Mass Spectrometry (SIMS)

SIMS is a characterisation technique that can be used to analyse the secondary ions sputtered from a sample material by focused primary ion beam. In the semiconductor industry, SIMS can be used to extract the impurity doping concentration of the sample material as well as implantation profiles. The simplified schematic of a SIMS instrument is shown in Fig. 2.10. The ejected secondary ions will be isolated by a mass analyser and the detection system will collect and count the number of ions of interest. It is impossible to do the measurement if the doping concentration is below the detection limit. SIMS measurement with nitrogen and phosphorus were found to have detection limits of $5\times10^{16}cm^{-3}$ and $5\times10^{15}cm^{-3}$ respectively [27].

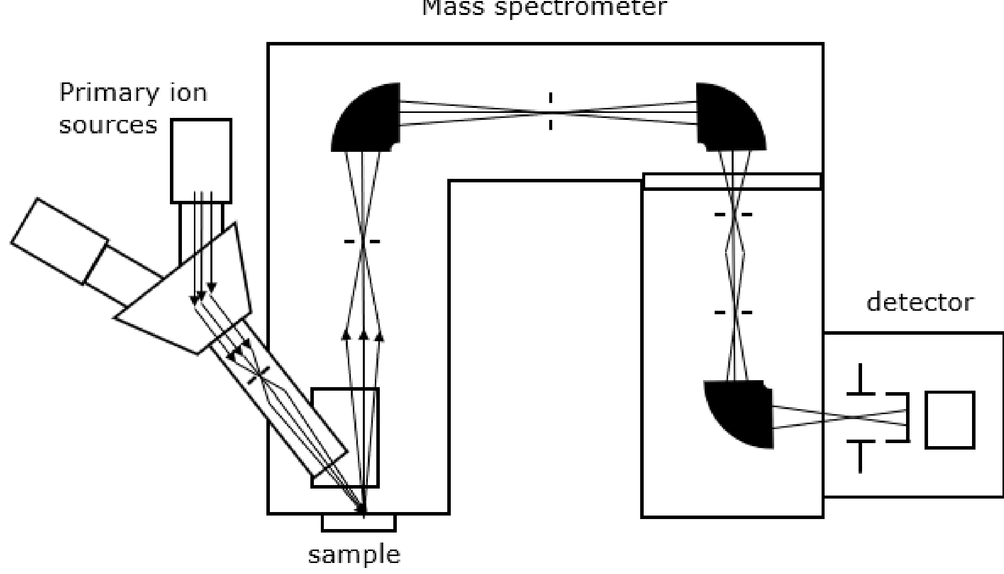

Fig. 2.10 Simplified schematic of a SIMS instrument [25]

2.4.2 Atomic Force Microscopy (AFM)

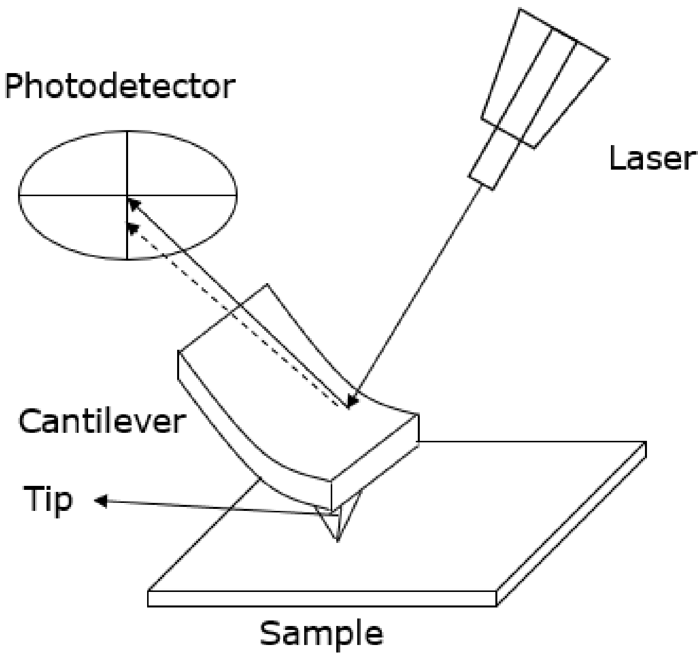

Fig. 2.11 Schematic illustration of the AFM operation principle

AFM can be used to image the sample surface with height resolution down to 0.1nm. A cantilever with a low spring constant is used to follow and respond to the surface morphology [28]. The whole system is accomplished by a focused laser directed to the

cantilever which is then measured by a four-quadrant photodetector, this is then fed into a piezoelectric stage which alters its height to keep the photodiode signal at a minimum. A surface image can be generated with after analysing the data received by the photodetector and the heights moved by the stage. In this thesis, AFM is used to extract the surface roughness.

2.4.3 Scanning Electron Microscope (SEM)

In a SEM, a high energy electron beam is focused on a small sample area and then rastered across the sample. The interaction from the electrons is complex but the secondary or backscattered electrons can be thought of as reflected from the sample surface which is then collected by a detector as shown in Fig. 2.12. The image will build up when the collected signals are changed by the properties (topography, roughness and density) of the sample [29]. In this thesis, SEM is mainly used for the study of the SiC dry etching process. In addition, SEM can be a very useful tool for analysing fabricated devices.

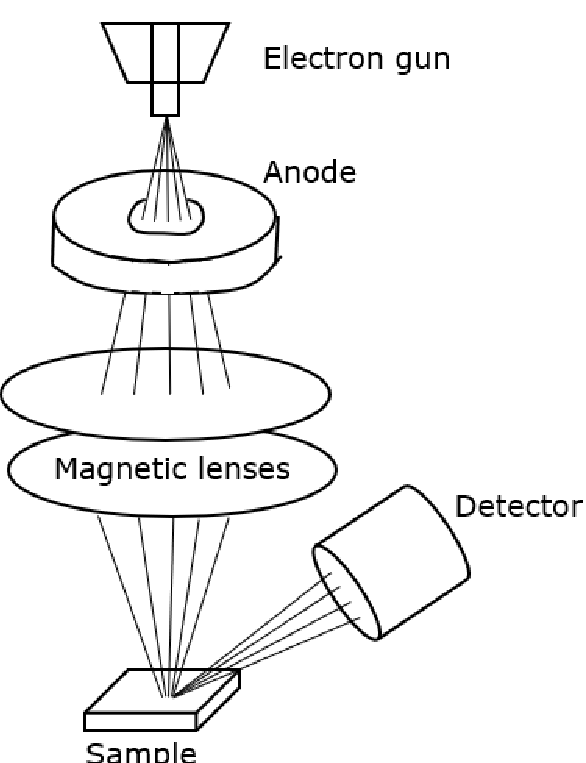

Fig. 2.12 Schematic illustration of the SEM operation principle

2.4.4 Transmission Line Measurement (TLM)

Transmission line measurement (TLM) is a characterisation technique commonly used to extract the ohmic metal-semiconductor contact resistivity. In this thesis, TLM is used to evaluate the quality of ohmic contacts fabricated on 4H-SiC wafers. A mesa structure is usually needed to isolate the active TLM area in order to avoid current spreading, then 5 or 6 metal pads are deposited with different defined distances. The total resistance can be plotted against the contact distance like Fig. 2.13. The intersection with the y-axis will give the resistive left when distance is zero and hence will be twice the value of the contact resistance ($2R_c$). This measurement is normally done in a 4-point measurement method, but a 2-point method can be used if the resistance of the metal pad is much smaller.

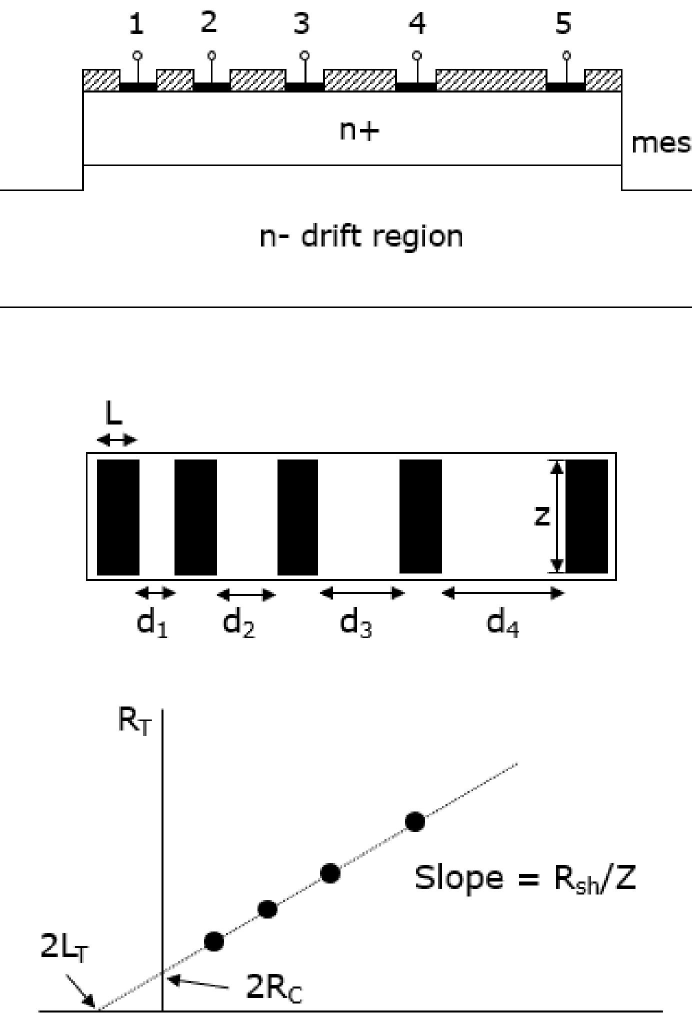

Fig. 2.13 TLM structure with cross-section and top view and the total resistance versus the distance between adjacent metal pads [30]

Not the whole contact pad area is used to contact the current, normally only a small fraction of the total contact length is active which is called the transfer length "L_T". The total resistance plot against the distance shown Fig. 2.13 corresponds to the equation below:

$$R_T = \frac{R_{sh}d}{Z} + 2R_c \approx \frac{R_{sh}}{Z}(d + 2L_T) \quad (2.1)$$

The contact resistivity calculation must use active pad area which conducts current. It was reported that a contact resistivity as low as 2.1E-6Ωcm^2 was achieved on n+ implanted region [31].

$$R_c \approx \frac{\rho_c}{LZ} \quad \text{for } L \leq 0.5\ L_T$$

$$R_c \approx \frac{\rho_c}{L_T Z} \quad \text{for } L \geq 1.5\ L_T \quad (2.2)$$

TLM is also an incredibly useful tool for diagnosing the contribution of ohmic factors independent of the complex device structure.

2.4.5 Capacitance-Voltage (CV) measurement / Dit Extraction

Metal-oxide-semiconductor (MOS) based devices are of great importance in the SiC device family. The silicon carbide thermal oxidation process does not form perfect SiO_2 layer like silicon, due to the existence of carbon in the crystal structure. The SiC/SiO_2 interface has been an issue for a long time, and capacitance-voltage (CV) measurement is a commonly used characterisation technique to extract the interface trap density (D_{it}). The defects or oxide charges are of less importance compared to the interface traps which can have a serious impact on the performance of metal-oxide-semiconductor field-effect transistor (MOSFET) devices. In this thesis, CV measurement is mainly used to analyse the quality of SiC/SiO_2 interface. In a CV measurement, a DC bias is applied to the MOS structure and this DC bias changes slowly according to the pre-set voltage range. A small AC signal applied on top of the DC bias will be used to perform the CV measurement [30]. Since the interface traps have different responses to AC signals at various

frequencies, two CV measurements made at low and high frequencies respectively can be used to extract D_{it}, this method is called High-Low CV measurement. The equation for the D_{it} extraction is [30]

$$D_{it} = \frac{C_{ox}}{Aq^2}\left(\frac{C_{lf}/C_{ox}}{1-C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1-C_{hf}/C_{ox}}\right) \tag{2.3}$$

C_{lf} and C_{hf} can be measured directly with a device analyser or an LCR meter, the value of C_{ox} can also be read from the measurement results, therefore it is a very convenient way to extract the D_{it} value from High-Low CV measurement. The extracted interface trap density corresponds to certain DC bias voltages, which can then be converted to the band gap location with respect to conduction band edge. Interface traps have different emission time constant which depends on the location in the bandgap. For a high frequency up to 1MHz, the interface trap density can be probed as close as 0.2eV from the conduction band edge [30].

Conductance method is one alternative technique to extract the D_{it}. The two equations below demonstrate how measurement result can be converted into D_{it} [30].

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{2.4}$$

$$\frac{G_p}{\omega} = \frac{q}{2}\frac{D_{it}}{\omega\tau_{it}}\frac{1}{\sqrt{2\pi\sigma^2}}\int_{-\infty}^{\infty} \ln\left[1 + (\omega\tau_{it})^2 e^{2\varphi_s}\right] e^{-\frac{\varphi_s^2}{2\sigma^2}} d\varphi_s \tag{2.5}$$

τ_{it} refers to the time constant of the interface traps; σ represents the surface potential fluctuation. Conductance G_p is an indicator which can be calculated using the measured total capacitance C_m and conductance G_m as shown in Eq 2.4. The theoretical value of G_p can also be calculated as shown in Eq 2.5 where D_{it} is one of the variables. In this case, D_{it} can be estimated using curve fitting techniques. Although conductance method can provide more comprehensive results including not only D_{it} but also τ_{it} and σ, High-Low CV method is used to study MOS interface in this thesis since it can fulfil the required measurement accuracy and the purpose of systematic study.

2.5 Summary

This chapter reviews SiC polytypes, bulk and epitaxial growth, defects, ion implantation process and finally the main characterisation techniques used in the following chapters. The continuous improvement of material growth techniques will lead to cost reduction of SiC wafers and therefore increases the advantages of SiC devices in the competition with GaN devices and traditional Si devices. Material defect reduction is of great importance since the distribution of defects on a wafer places a limit on the active area that can be used for device fabrication and therefore a limited current conduction.

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Chapter 3 MOS interface study and trench MOSFET

This chapter reviews the metal-oxide-semiconductor (MOS) interface which remains one of the most important topics for SiC metal-oxide-semiconductor field-effect transistor (MOSFET) fabrication. A systematic study was carried out on 4H-SiC thermal oxidation and post-oxidation annealing conditions. MOS capacitors and long channel lateral MOSFETs have been fabricated to extract the interface trap density and the channel mobility. A literature review is provided on general MOSFET theory and 4H-SiC trench MOSFETs.

3.1 MOS technology

Si MOS technology has been adopted widely in both information and power semiconductor industries because of the perfect Si/SiO_2 interface. SiO_2 is also the native oxide for 4H-SiC, however, interface traps are generated during the thermal oxidation process which degrades the performance of SiC MOSFETs. A MOS structure band diagram is shown in Fig. 3.1 using aluminium (Al) as an example of the metal.

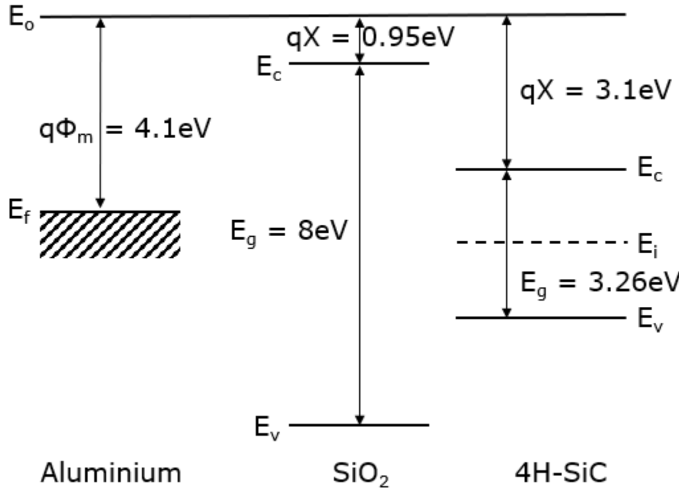


Fig. 3.1 The individual band diagram of Al-SiO_2-4H-SiC before joining together

The wafer used for the MOS capacitor fabrication in this thesis has a n- epilayer with a doping concentration of $4\times10^{15}cm^{3}$. The band bending in equilibrium is shown in Fig. 3.2 where the interface traps are located in the bandgap.

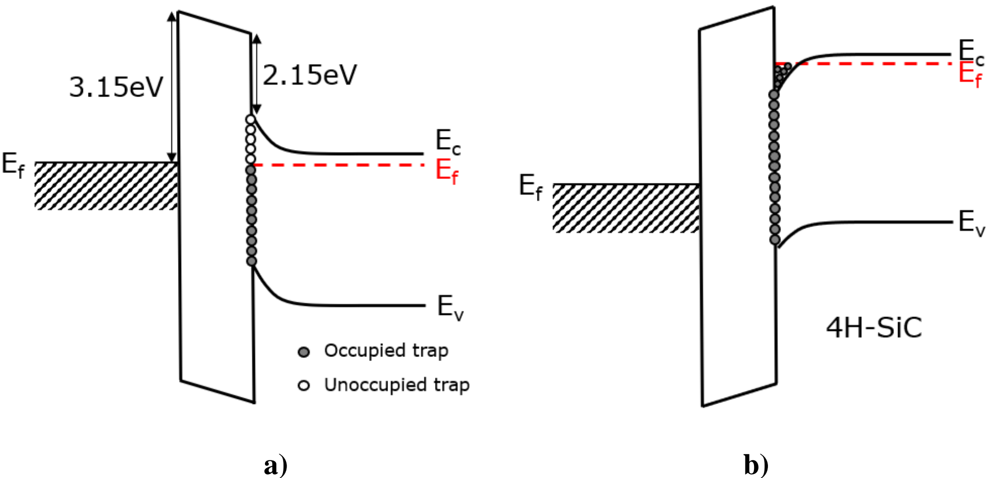


Fig. 3.2 The MOS band diagram with a) V_{MS} = 0; b) V_{MS} > 0 (accumulation)

The accumulation of the n-epi layer is equivalent or at least similar to the strong inversion of N-channel MOSFET, therefore MOS capacitors can be used as test structures instead of fabricating more complicated MOSFET structures to study the SiO_2/SiC interface. The DC bias voltage variation between the metal and semiconductor (V_{MS}) is directly related to the fermi level location at the SiO_2/SiC interface. Therefore the bias voltage sweep in the CV measurement essentially provides information on the interface trap density at specific location in the bandgap.

The MOS capacitor structure is shown in Fig. 3.3, this simple structure only needs one layer of photo mask.

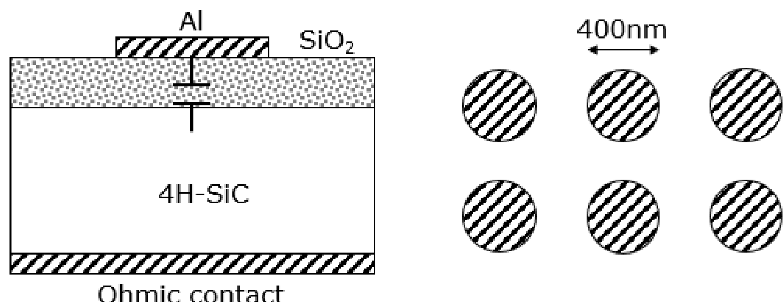


Fig. 3.3 Vertical MOS capacitor structure with Al metal pad on top of SiO_2 layer

3.2 Lateral MOSFET

A MOSFET uses the MOS structure to control the switching behaviour of a field-effect transistor (FET). The schematic of the lateral MOSFET is shown in Fig. 3.4. If a voltage larger than the threshold voltage (V_{th}) is applied on the gate terminal, an inversion channel is formed in the p-well region below the semiconductor/oxide interface which provides a current path between the source and drain terminal. At low V_{DS}, the MOSFET operates in the linear region where the drain current I_D increases with V_{DS}; if V_{DS} becomes larger than V_{GS}-V_{th}, MOSFET channel will pinch off and therefore I_D is disconnected with V_{DS}, the device then enters the saturation mode.

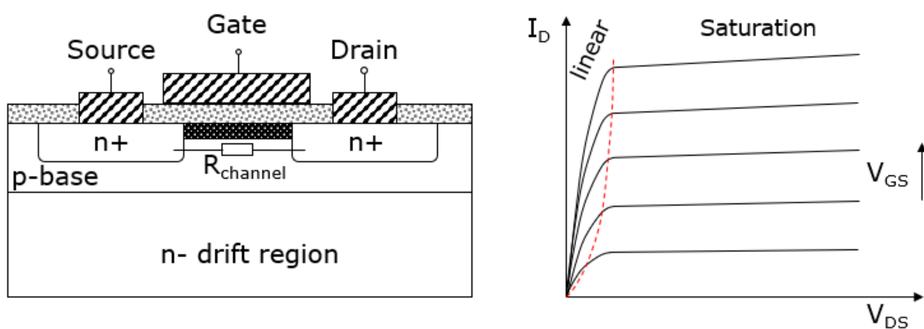


Fig. 3.4 Lateral MOSFET structure and typical I-V characteristics

The drain current in the linear mode and saturation mode can be calculated with Equation 3.1 and 3.2 [1]. These equations are deducted based on the gradual channel and constant depletion approximation. For instance, it is assumed that the voltage along the channel vary gradually from the drain to the source terminal which is named as gradual channel approximation.

$$I_D = \frac{1}{2}\mu_{eff}C_{ox}\left(\frac{W}{L}\right)[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \tag{3.1}$$

$$I_D = \frac{1}{2}\mu_{eff}C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \tag{3.2}$$

For a long channel lateral MOSFET, $R_{channel}$ is the main on-state resistance and Equation 3.1 can be rewritten as

$$R_{channel} \cong \frac{L}{\mu_{eff} C_{ox}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) W} \tag{3.3}$$

From Equation 3.3, it is not difficult to tell that the channel resistance $R_{channel}$ is dominated by the value of inversion channel mobility μ_{eff}.

Equation 3.1 can be simplified to Equation 3.4 if V_{DS} is sufficiently small.

$$I_D = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T) V_{DS} \tag{3.4}$$

As the transconductance g_m is defined by $\partial I_D / \partial V_{GS}$, Equation 3.4 can be rewritten.

$$\mu_{FE} = \frac{L g_m}{W C_{ox} V_{DS}} \tag{3.5}$$

In Equation 3.5, the field-effect mobility μ_{FE} is extracted if all the other parameters are known. L, W, C_{ox} are fixed parameters for fabricated devices, g_m can be measured by setting V_{DS} to 0.1V which should be small enough.

3.3 Device fabrication and characterisation

MOS capacitors were fabricated with various thermal oxidation and post-oxidation annealing (POA) conditions. Thermal oxidation at 1400°C without POA is used as reference since this was the standard condition in the local cleanroom.

Table 3.1 Various thermal oxidation, post-oxidation annealing (POA) conditions and the measured oxide breakdown electric field

No.	Oxidation temperature (°C)	N_2O passivation	Breakdown electric field (MV/cm)
1	1400°C 30min O_2	n/a	7.6
2	1400°C 30min O_2	1200°C 2h	9.6
3	1400°C 30min O_2	1300°C 2h	10.4
4	1400°C 30min O_2	1400°C 2h	10
5	1300°C 1h O_2	n/a	11
6	1300°C 1h O_2	1300°C 2h	10.3
7	1200°C 2h O_2	n/a	13.5
8	1200°C 2h O_2	1300°C 2h	11.2
9	1300°C 2h N_2O	n/a	11.6

Both CV and oxide breakdown measurement were performed on the MOS capacitor samples. The oxide breakdown field are recorded in Table 3.1. The thermal oxide breakdown field ranges from 10MV/cm to 14MV/cm based on the literature published by other research groups [8, 9]. The results in this experiment are reasonable compared to the literature. Thermal oxidation temperature is the only parameter that is changing if experiment no. 1, 5 and 7 are compared. It seems that the oxide quality is improved at lower thermal oxidation temperature since higher breakdown field is achieved. If the thermal oxidation temperature is fixed at 1400°C, the oxide breakdown field is almost constant referring to experiment no. 2, 3 and 4. It is interesting that the oxide breakdown field increases with N_2O POA if the thermal oxidation is done at 1400°C. It shows the opposite results as the oxide breakdown happens at lower voltages after N_2O POA if the thermal oxidation temperature is lower than 1400°C. 1300°C thermal oxidation in N_2O ambient is set as one of the conditions where no POA is needed.

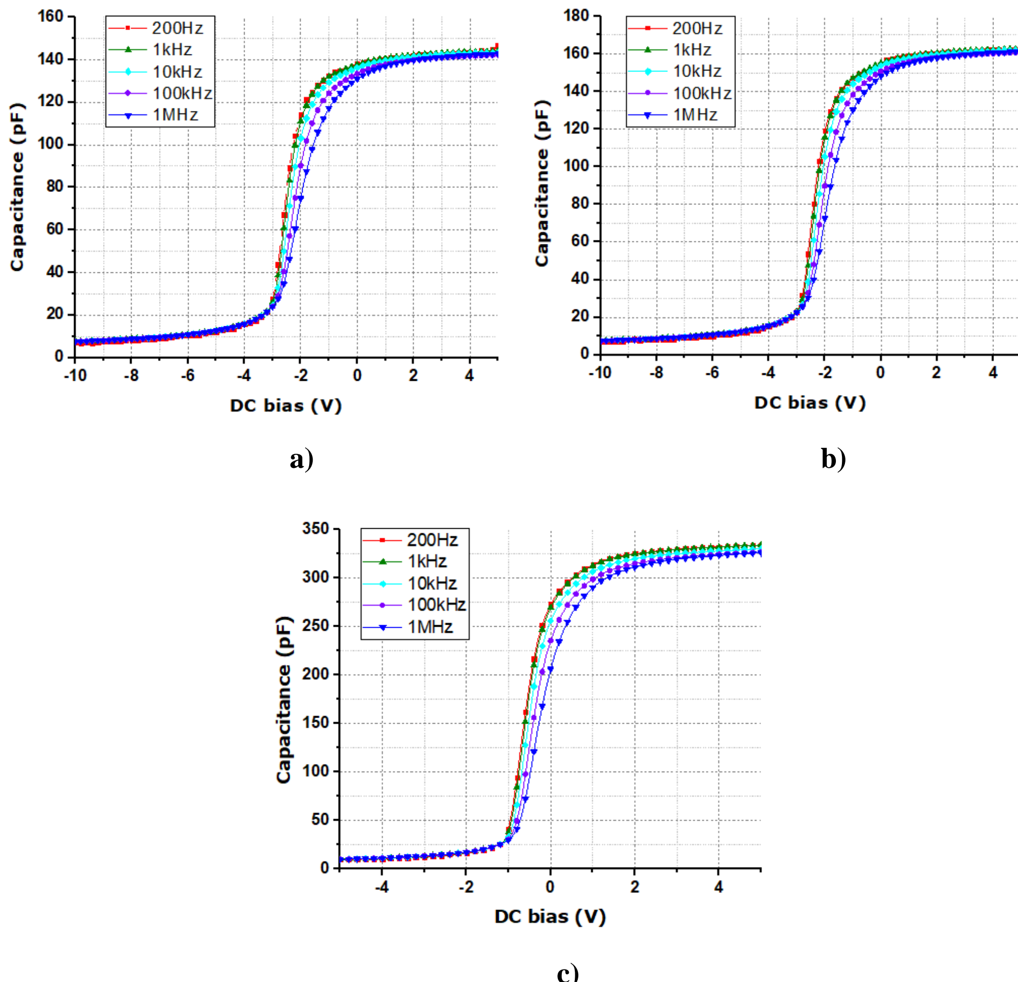


Fig. 3.5 CV measurement results for MOS capacitors fabricated at a) 1400°C O_2 without POA; b) 1300°C O_2 without POA; c) 1200°C O_2 without POA

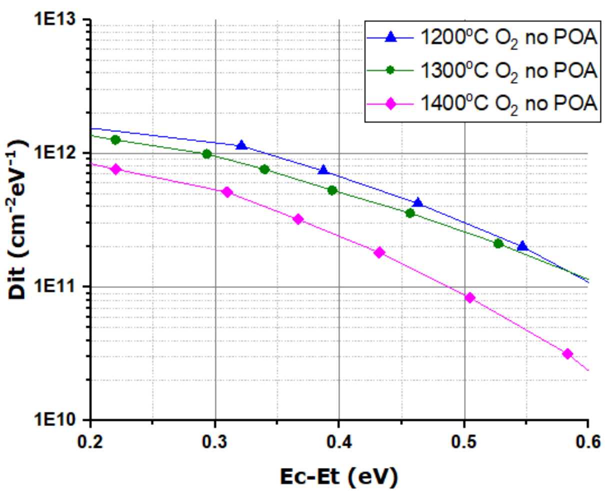


Fig. 3.6 Interface trap densities extracted using high-low frequency CV method

The CV measurement results for experiment no. 1, 5 and 7 are shown in Fig. 3.5 and the extracted D_{it} results are presented in Fig. 3.6. Thermal oxidation at 1200°C seems to produce more interface traps even though it has highest oxide breakdown field.

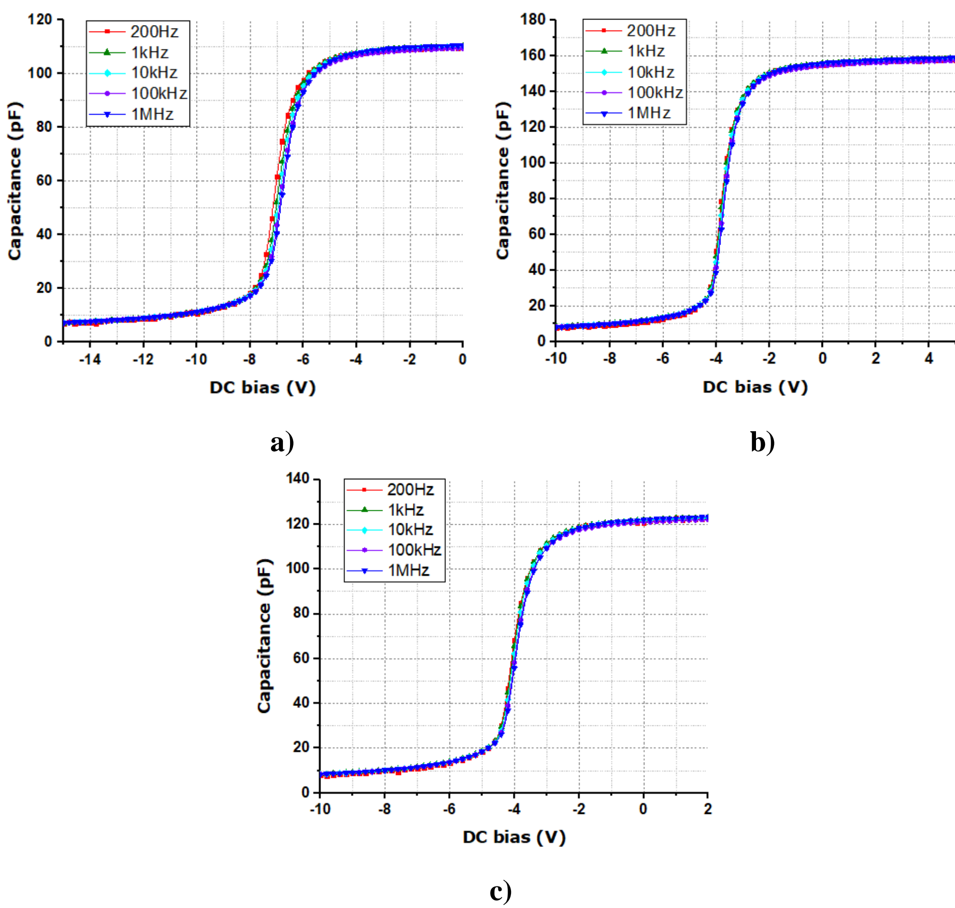


Fig. 3.7 CV measurement results for MOS capacitors with the same 1300°C N_2O POA condition but different thermal oxidation conditions at a) 1400°C O_2; b) 1300°C O_2; c) 1200°C O_2

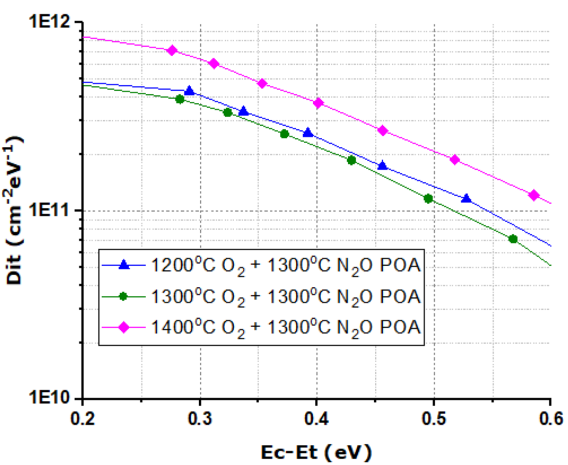


Fig. 3.8 Interface trap densities extracted using high-low frequency CV method where all the samples were annealed at 1300°C with N_2O

It is not difficult to identify the difference between the CV curves with and without 1300ºC POA as shown in Fig. 3.5 and Fig. 3.7. There is much less deviation of the measured capacitance at various frequencies after 1300ºC N_2O POA indicating reduced interface trap density which is confirmed by Fig. 3.8. The extracted Dit for 1200ºC thermal oxidation condition with ($5\times10^{11}cm^{-2}eV^{-1}$) and without N_2O POA ($2\times10^{12}cm^{-2}eV^{-1}$) are consistent with the Hua's work [2]. It is also suggested in [10] that the Dit decreases with increased thermal oxidation temperature. The same trend has been demonstrated in this work as shown in Fig. 3.6. Nevertheless, the Dit result is not very promising for the sample after 1400ºC thermal oxidation with 1300ºC POA since it is similar to the sample even without POA which is not consistent with the direct observation of the CV curves.

When the Dit results are analysed in combination with the oxide breakdown field presented in Table 3.1, it is found that the sample oxidised at 1200ºC without POA not only has the highest oxide breakdown field but also has the highest Dit value. These results suggest that Dit has limited effect on the oxide breakdown field. However, based on the literature [11], Dit can be responsible to higher leakage current. Fixed oxide charge is another important type of charges which locate closely to the interface. This type of oxide charges can be generated during oxidation process depending on the oxidation conditions like the temperature, gas combination, cooling conditions and the substrate crystal orientation [1]. In this case, it is believed that the excessive amount of fixed oxide charges can be responsible for the lower oxide breakdown field at higher oxidation temperature.

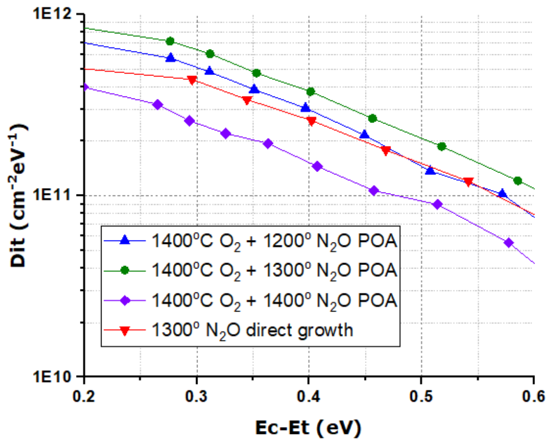


Fig. 3.9 Interface trap densities extracted using high-low frequency CV method where the N_2O POA temperature was varied

The effect of N_2O POA temperature on the interface trap density has also been investigated and the results are shown in Fig. 3.9. It seems that thermal oxidation and POA at both 1400°C generates the lowest number of interface traps. There was another batch of MOS capacitors fabricated collaboratively in this laboratory which is published in [2]. The Dit results of these two batches are not identical which means the cleanroom processes like sample preparation, material difference and equipment conditions can have an impact on the experimental results. The oxidation furnace is most possibly responsible for the difference of the results since the wafer holder was redesigned and upgraded once between these two batches of samples and therefore oxidation conditions were not 100% identical. However, the results on these two batches agree that direct thermal oxidation in N_2O ambient may be able to replace the traditional approach of O_2 oxidation with N_2O POA due to reduced interface trap density.

Lateral MOSFET have also been fabricated to study the effect of oxidation conditions on the channel mobility. This investigation was not carried out in the same time with the MOS capacitor work. The process flow for the lateral MOSFET is shown in Fig. 3.10.

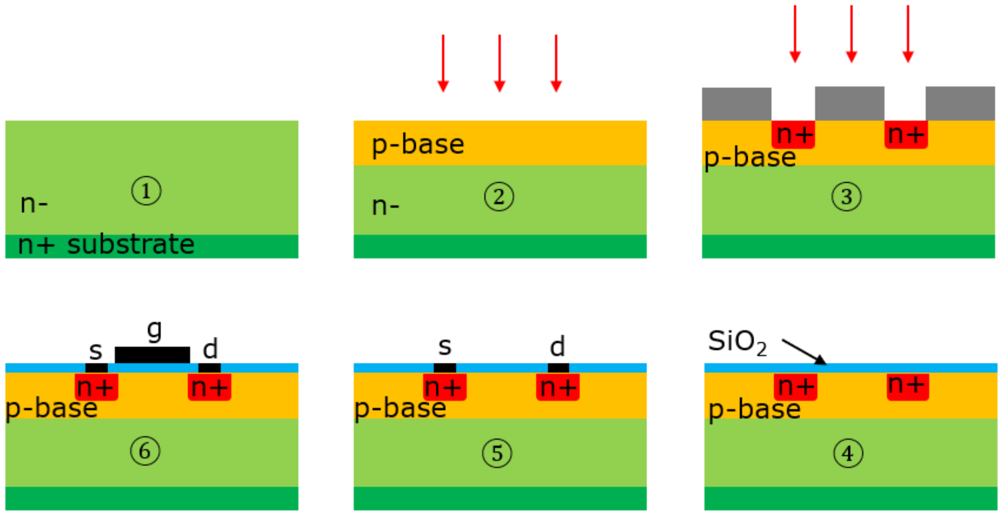


Fig. 3.10 Lateral MOSFETs fabrication process

P-base blanket multi-energy implantation was performed to produce a box profile. The implantation process was simulated using Silvaco and the result is presented in Fig. 3.11. After n+ implantation, the samples were placed into a high temperature tube furnace for implant activation at 1600° for 45 minutes. RCA (named after Radio Corporation of America) cleaning was performed before the thermal oxidation and POA process. Source and drain windows were then opened with photolithography process followed by wet

etching of the oxide. 30nm Ti and 100nm Ni were then deposited with an electron-beam evaporator followed by rapid thermal annealing (RTA) at 1000°C 2min to form ohmic contacts. The final step was the to open the gate window and deposit 500µm or 1µm Al metal pad. Most of the process steps have already be developed by the previous staff or students working in the cleanroom, therefore there was no need for reinvestigation at that stage.

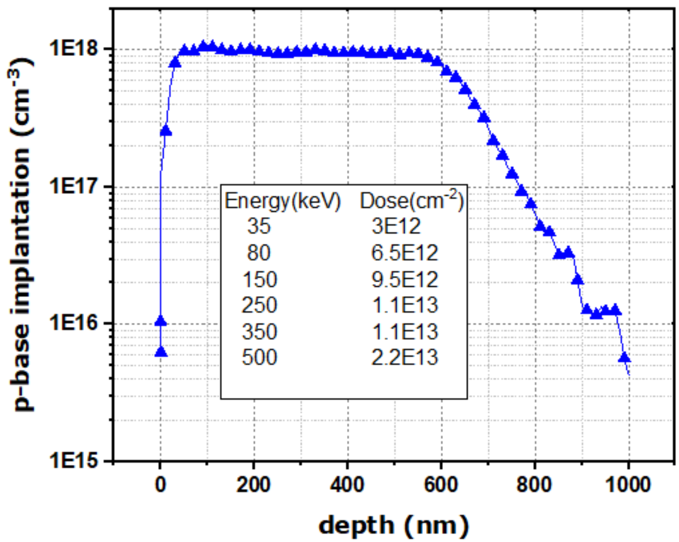


Fig. 3.11 p-base multi-energy implantation to produce box doping profile

The photo mask drawing and the top view of the fabricated devices are shown in Fig. 3.12. The channel length and width are 150µm and 290µm respectively. Various thermal oxidation and POA conditions were used for the gate oxide growth.

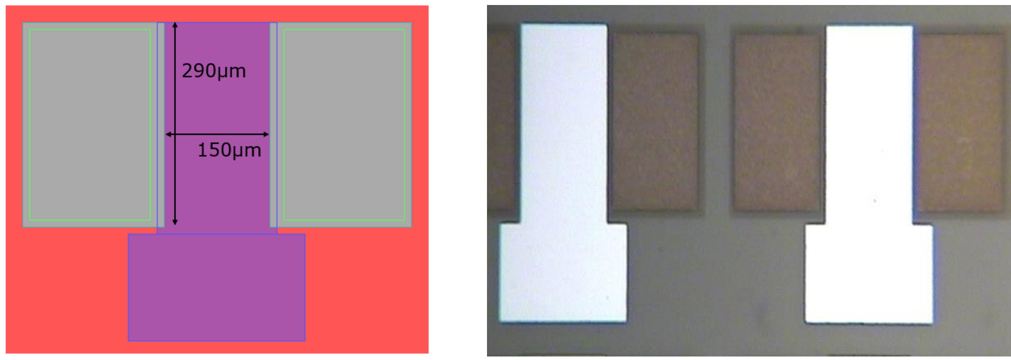
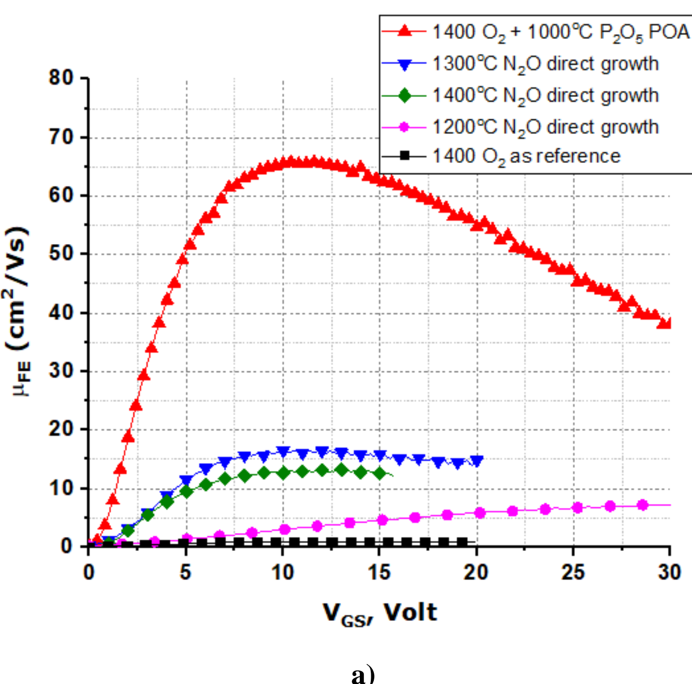


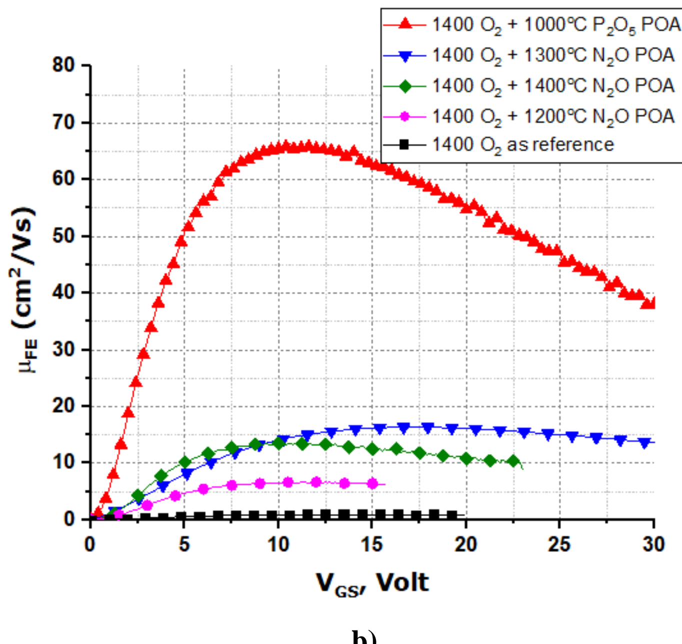
Fig. 3.12 The photo mask pattern for the lateral MOSFET (left) and the fabricated lateral MOSFETs (right)

It was reported in [3,4] that post-oxidation annealing in P_2O_5 ambient increased the channel mobility up to 80cm^2/Vs. SiO_2 was converted to PSG (phosphosilicate glass) at

the original SiO_2/SiC interface and the interface trap density was reported to be an order of magnitude lower than the thermal oxide with nitridation treatment. It is suggested that the carbon related defects and silicon dangling bonds can be reduced using PSG treatment [12]. Therefore, post-oxidation annealing in P_2O_5 ambient was used as one of the experimental conditions for verification purpose. PSG, as a polar material [5], can also cause threshold voltage instability of the MOS structure. In Yogesh's work, a 70nm thick PSG interfacial layer resulted in large variation (>3V) of threshold voltage during bias-temperature stress (BTS) measurement [6]. A thin PSG layer (10nm) instead of a thick one at the SiO_2/SiC interface could increase the stability of the threshold voltage, however, more reliability study needs to be done before P_2O_5 annealing can be used for a real MOSFET.



a)



b)

Fig. 3.13 Extracted channel mobility from fabricated lateral MOSFETs

The channel mobility values were extracted using Equation 3.5 and the results are shown in Fig. 3.13. The channel mobility of the device oxidised at 1400°C without any POA condition is as low as $1cm^2/Vs$ which is three orders of magnitude less than the electron mobility in the bulk material. A channel mobility of $65cm^2/Vs$ was achieved after the 1000°C POA in P_2O_5 ambient, this value is not too far away from others' work. The maximum channel mobility with N_2O treatment is approximately $17cm^2/Vs$. This maximum mobility can be achieved as long as the N_2O treatment temperature is 1300°C, N_2O direct oxide growth or POA does not make much difference. The channel mobility after N_2O treatment in this work is relatively lower compared to Nanen's work [7] where a mobility of $29cm^2/Vs$ was achieved. In this work, the p-base doping density is $1\times10^{18}cm^{-3}$ which is two orders of magnitude higher compared to that in Nanen's work which may be part of the reason. Furthermore, the N_2O flow rate in this work is limited up to 1 litre per minute (L/min) by the equipment and since it is a large furnace, the N_2O gas flow needs to be diluted with Ar at 4L/min flow rate to prevent air getting into the furnace. Possibly the full potential of N_2O treatment has not been fully realised due to the equipment limits. Some published work [13] use N_2 to dilute N_2O to enhance the N_2O decomposition in which the N_2O/N_2 ratio can affect the oxide growth rate. It is also suggested that carrier gas plays a less important role at temperature above 1300°C in which case Ar and N_2 as the carrier gas may not have significant effect to the oxidation process.

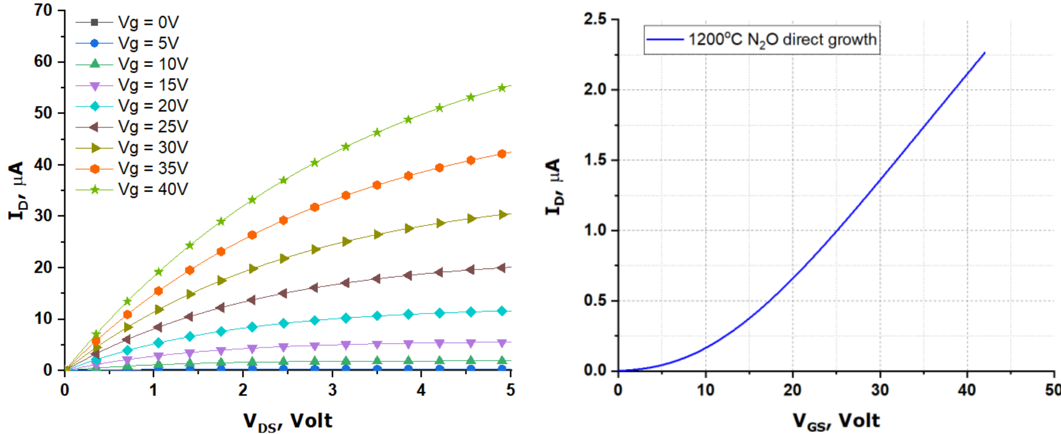


Fig. 3.14 IV and transconductance curves for the lateral MOSFET with 1200°C direct N_2O gate oxide growth

One set of on-state IV characteristics and transconductance curves are shown in Fig 3.14 as a representative of all the lateral MOSFET fabricated with various oxidation conditions.

3.4 Planar and trench gate power MOSFET

The difference between a power MOSFET and the basic lateral MOSFET is the power handling capability. Power MOSFETs are usually vertical devices with a thick n- drift region and the drain terminals are located at the bottom of the substrate. The schematic of the basic planar and trench gate power MOSFETs is shown in Fig. 3.15.

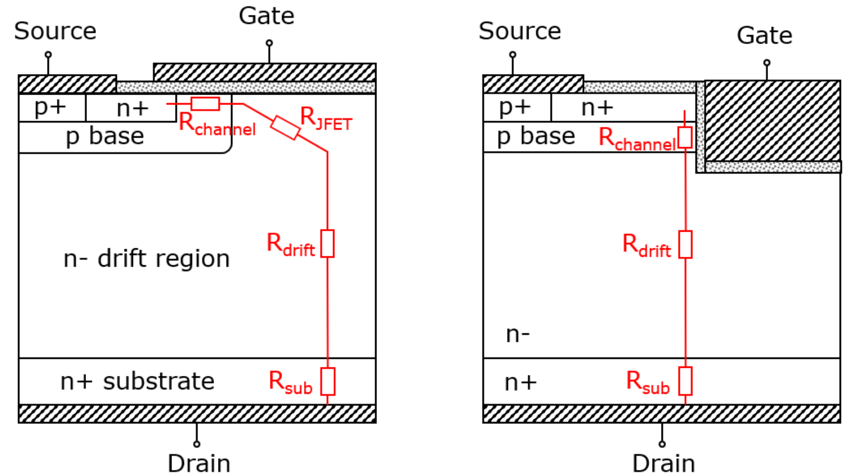


Fig. 3.15 The schematic for basic power MOSFETs with planar gate (left) and trench gate (right)

DMOSFET is also a type of planar gate power MOSFET like the UMOSFET for the trench MOSFET. In this thesis, UMOS and DMOS are sometimes used to describe these two types of devices. The main difference of the UMOSFET and DMOSFET structures is the location of the MOS channel. The channel in UMOS structure is vertical, therefore the current conduction is vertical as well. Compared to DMOSFET, UMOSFET structure does not have the parasitic JFET (junction field effect transistor) resistance R_{JFET}. When designing a DMOSFET, the JFET region must be large enough to reduce the resistance which imposes a minimum limit of the cell pitch. The case for UMOSFET is different, since the channel current flow is vertical, there is no such parasitic JFET region, therefore the cell pitch can be made smaller. It was reported higher channel mobility was achieved on {1120} crystal face for 4H-SiC devices [4]. As most of 4H-SiC wafers are commercially available with {0001} crystal face, the UMOSFET structure with the channel located in the {1120} plane produces lower channel resistance compared to the DMOSFET structure. As a result, the basic UMOSFET normally has lower on-state resistance compared to the DMOSFET indicating lower conduction power loss. This statement is particularly true for lower voltage ratings (<2~3kV) as the drift region resistance is not dominant in the total device on-resistance. The specific input capacitance ($C_{IN,SP}$) and reverse transfer capacitance (C_{GD}) of UMOSFET can be much larger than DMOSFET since the cell pitch of UMOSFET can be made much smaller than DMOSFET. A larger $C_{IN,SP}$ and C_{GD} increases the switching time and hence generate more switching power loss, it can also mean different gate driver design and higher driver circuit loss as well. The mesa/trench width ratio of the UMOSFET can be increased to reduce the $C_{IN,SP}$ and C_{GD} at the cost of higher specific on-state resistance (R_{ON_SP}) where a trade-off must be made [14].

The breakdown electric field for 4H-SiC is more than seven times higher than that of silicon, therefore, the average electric field in a 4H-SiC MOSFET is much higher than Si MOSFET. The electric field in the gate oxide is much higher than the electric field in the semiconductor side near the SiO_2/semiconductor interface where the relationship is given by Gauss's law as below

$$E_{ox} = \frac{\varepsilon_s}{\varepsilon_{ox}} E_s \quad (3.6)$$

Since the breakdown electric field of silicon is up to 0.3MV/cm, the oxide electric field is not a concern. Having the high electric field in 4H-SiC can easily increase the oxide electric field to above 3MV/cm which raises safety concerns for the oxide reliability and robustness. For a 4H-SiC UMOSFET with the basic structure shown in Fig. 3.15, the oxide electric field can be much higher than 3MV/cm during blocking state since the trench shape itself is the electric field hot spot.

The basic design must be upgraded for gate oxide protection to fully utilise the advantage of high breakdown electric field for silicon carbide. A common solution is to add an extra p+ implanted region below the trench bottom to protect the gate oxide from high electric field stress, the schematic is shown in Fig. 3.16.

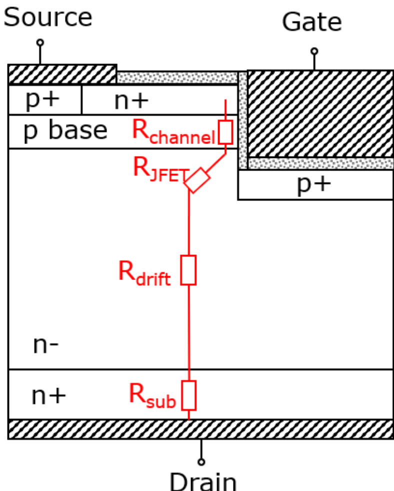


Fig. 3.16 The schematic for optimised 4H-SiC UMOSFET structure with added p+ shielding region below the trench structure

The electric field hot spot has now been transferred from the bottom of the trench structure to the corner of the p+ implanted region. However, the extra p+ implanted region also reintroduces a parasitic JFET into the structure which is marked in the schematic as well. As a result, the JFET resistance may be incredibly large if the design parameters like the trench depth are not adjusted properly. Other techniques like the use of CSL (charge storage layer) will be introduced in Chapter 6.

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Chapter 4 Trench Structure Fabrication

In this Chapter, the fabrication process of the trench structure has been developed. The dry etching process is one of the most critical steps during trench MOSFET fabrication. This chapter first introduces the micro-trenches which are created during the dry etching process, then Al_2O_3 is employed as dry etch mask followed by systematic study of the effects of ICP etch parameters on the shape of trench structure. Further optimization methods were investigated to improve the quality of the trench structure.

4.1. Micro-trench formation

A micro-trench can be generated during semiconductor dry etching process when the etch rates at the bottom of the sidewalls are larger than any other regions. The formation of micro-trenches can be attributed to the surface reflection of the high energy incident ions from the mask and trench sidewalls. These sidewall reflections have enhanced the etch rates at the bottom corners of the sidewalls [4]. Each of the parameters like ICP power, RF power, gas flowrate and pressure can affect the etching process and results in the formation of micro-trenches.

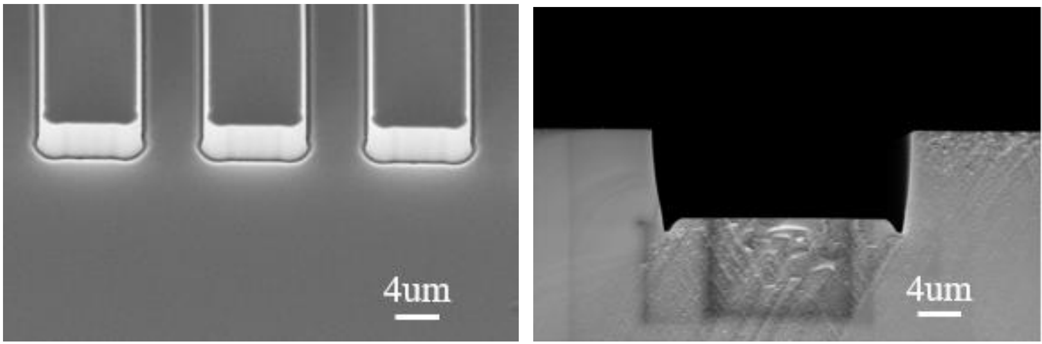


Fig. 4.1. Micro-trench formed after dry etching process

A micro-trench free structure with smooth sidewall is very important in terms of oxide quality and device reliability. Due to the strong Si-C bond, inductively coupled plasma (ICP) reactive ion etching (RIE) is necessary instead of traditional RIE etch. Corial 200IL was the equipment used to perform dry etching in the cleanroom.

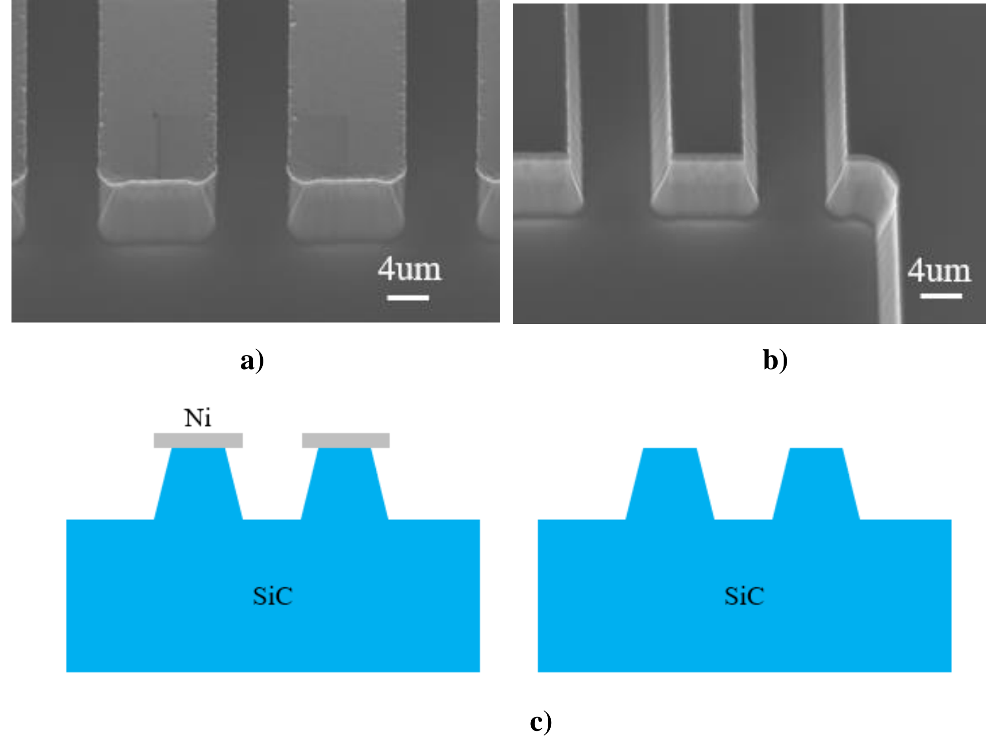


Fig. 4.2. The trench structure etched with Ni mask a) 45° cross-section view; b) 45° cross section view after removing the mask; c) Schematic drawing of a) and b) respectively

The etch results with a Ni mask are presented in Fig. 4.2 where micro-trenches are not present. It is believed that the micro-trenches were eliminated because of the high selectivity of the mask. It was quite clear that Ni had formed a shallow mask which protected the sidewall edge. The drawback of the shallow mask is the bad slope and the increased roughness on the trench sidewall. Ni mask has been used very often for SiC deep etching due to high Ni/SiC selectivity and a high etch rate of 1.35µm was achieved [5,6]. A high aspect ratio (18.5:1) has been achieved with Ni mask [7] which makes Ni a perfect choice for deep trench etching.

4.2. Introduction of Al_2O_3 as dry etching mask

Al_2O_3 is one of the dielectrics that can be used as an etch mask which has the advantage of high material density (3.95~4.1g/cm^3) compared to tetraethyl orthosilicate

(TEOS~0.93g/cm^3), deposited with a low pressure chemical vapor deposition (LPCVD) method. Hence it is more resistive to dry etching. Al_2O_3 has a high resistivity in the ambient of many plasmas, however, it can be easily cleaned with wet etch [8]. As a result, Al_2O_3 brings more process flexibility compared to the LPCVD deposited TEOS. Al_2O_3 is not new to semiconductor process and it has been used as hard mark to fabricate nanopores on SOI substrates with excellent selectivity over SiO_2 [9]. It is worth to investigate the feasibility of using Al_2O_3 hard mask for SiC etching.

Table 4.1 Selectivity of the etching masks

Mask	Selectivity
Photoresist (S1818)	<1
Al_2O_3	>8
TEOS	1~2
Nickel	46 (refer to literature [1])

It is shown in Fig 4.1 that the trench structure etched with Al_2O_3 mask exhibits a smoother sidewall with a micro-trench in contrast to the structure etched with Ni mask which is micro-trench free but has rough sidewall.

Ni mask has a very high selectivity of 46:1 from Table 1, which is an advantage for deep trench etching [1], however, the initial trench structure etching results have shown that the sidewall smoothness etched with Ni mask is not as good as the trench structures etched using Al_2O_3 mask. Since Ni masks have already been studied widely as an etch mask, this work investigates the potential of Al_2O_3 as an etch mask for future SiC trench device fabrication.

TEOS is traditionally used as etching mask in the cleanroom, however, the selectivity is not high enough. Compared to TEOS, Al_2O_3 has much higher selectivity referring to Table 4.1. In addition, Al_2O_3 can be deposited at room temperature therefore allowing lift-off process which means more process flexibility.

4.3. A systematic study of ICP etcher parameters

Systematic ICP dry etch experiment was performed to identify the optimum conditions for the fabrication of smooth and micro-trench free structure. The effect of different gases to the shape of trenches were investigated.

High ICP power enables a fast etching rate and selectivity [2], therefore, the ICP power was fixed at the 1000W which is also the maximum power of the equipment. Sulfur hexafluoride (SF_6) and Ar gas mixture were used since it was suggested this combination produced smoother surfaces/sidewalls and higher etching rates compared to SF_6 and O_2 mixture [3].

Table 4.2 Corial 200IL ICP etcher parameters and experimental conditions

ICP parameters	Experimental conditions
Pressure [mT]	10, 20, 40, 60
Gas flowrate [sccm]	SF_6: Ar = 50:40; 50:100; 50:25; 50:0; 1:10
RF power [W]	30, 60, 120
ICP power [W]	1000

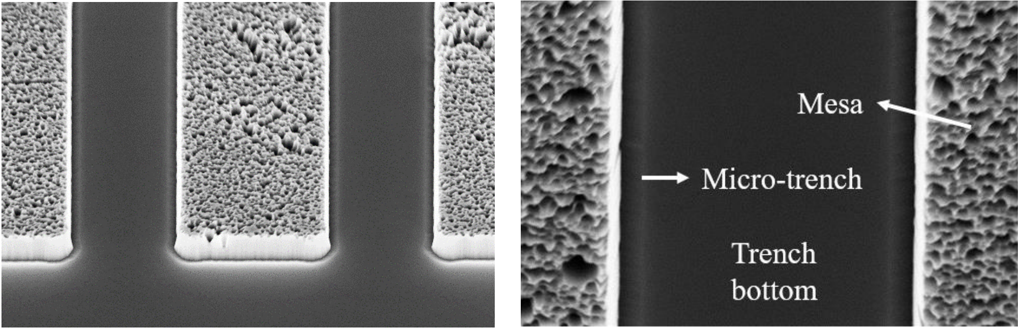
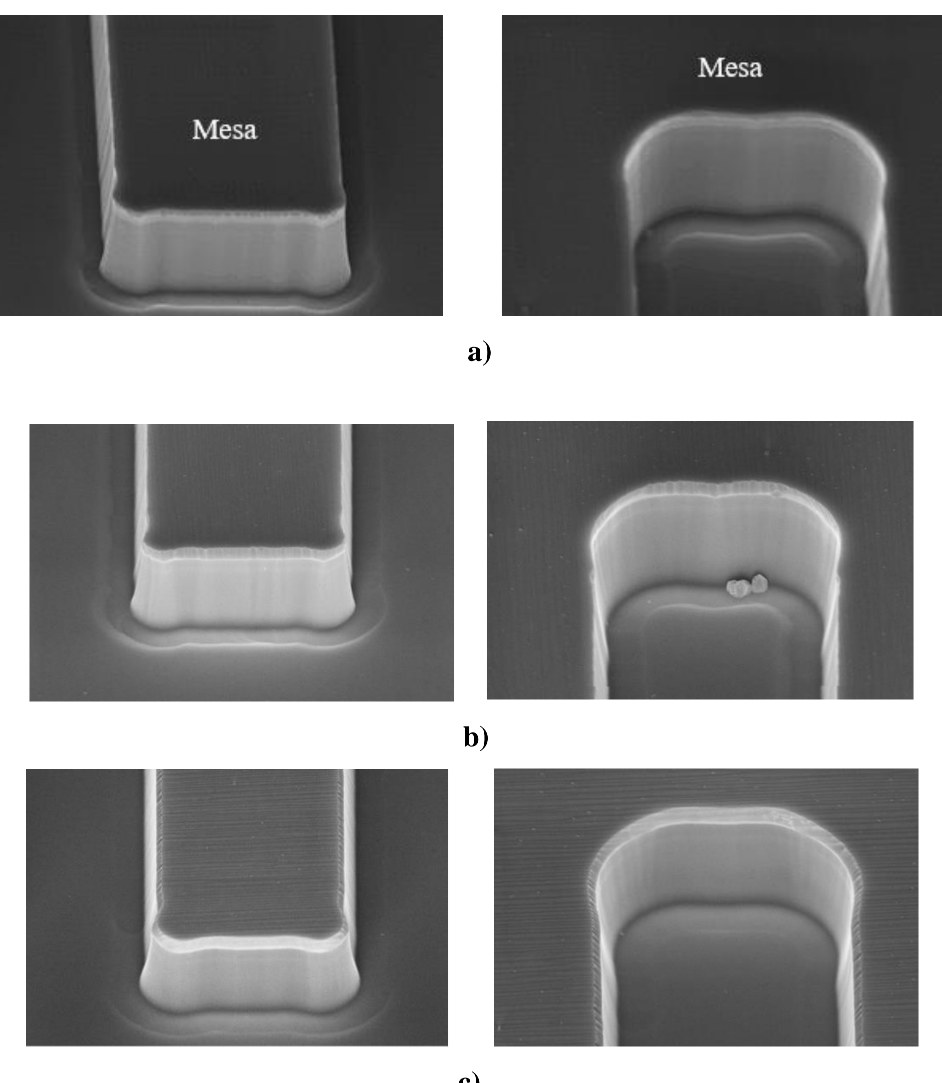


Fig 4.3. SEM photos of trench structures etched with thin Al_2O_3 layer (400nm)

It is shown in Fig 4.3 that the SiC surface is very rough after dry etching since the Al_2O_3 mask is not thick enough. Because the mask material itself is not perfect, pinholes exists in the mask, therefore, safe margin on etching mask thickness should be considered before dry etching process.

The trench structure shown in Fig 4.1 are the starting point of the systematic experiment with conditions of 60W RF power, 1000W ICP power, 50sccm SF_6, 40sccm Ar and 10mT pressure where “sccm” stands for standard cubic centimetres per minute.



a)

b)

c)

Fig 4.4. Dry etching results with 50sccm SF_6, 40sccm Ar and a) 20mT pressure; b) 40mT pressure; c) 60mT pressure

The first experiment shown in Fig. 4.4 investigates the effect of pressure on the trench structure etching. It is not difficult to identify that the micro-trench depth is reduced with increased pressure. It is a reasonable assumption that the micro-trench would be fully eliminated by further increasing the pressure.

Unfortunately, the results shown in Fig. 4.4 could not be reproduced with the same etching parameters after a period of equipment breakdown. The etching results using the same conditions with 60mT pressure is shown in Fig. 4.5, where the geometry of the micro-trench is very different from Fig. 4.4c) by observation. The whole experiment must be started from the beginning again.

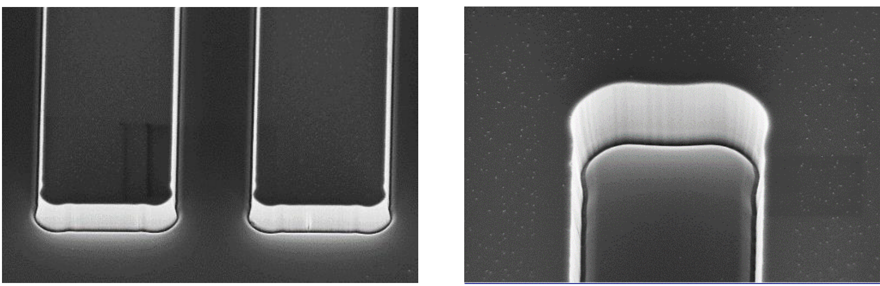


Fig 4.5. Dry etching results with 50sccm SF_6, 40sccm Ar and 60mT pressure

The RF power was varied between 30W, 60W and 120W to study the effect of RF power on the shape of the trench structure. The dry etching results with 30W and 120W RF power are showing in Fig. 4.6 where no conclusion is made in terms of the effect of the RF power on the trench structure shape. The trench sidewall seems to be rougher with 120W RF power which is believed to be the higher collision energy of the plasma.

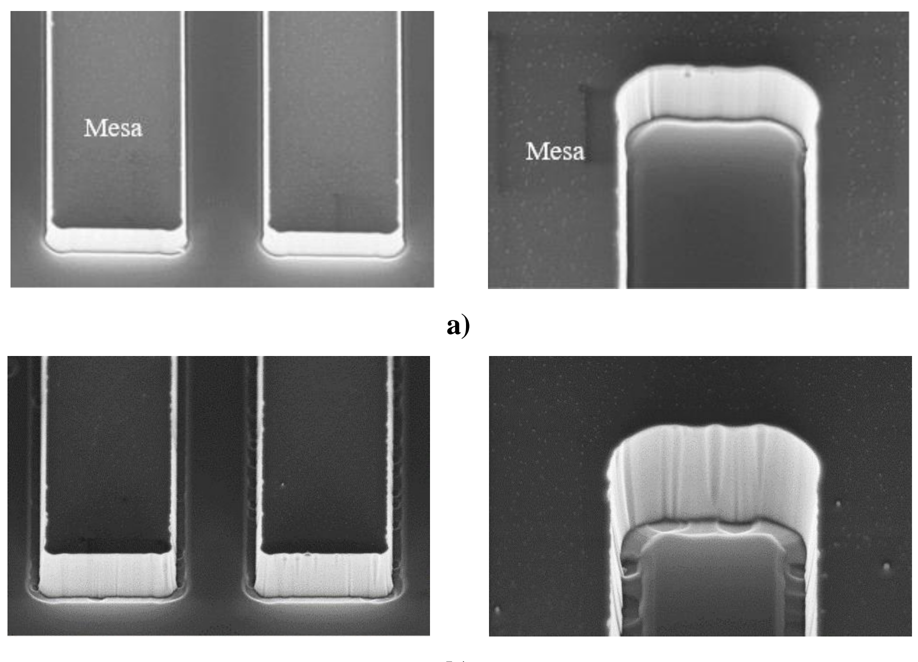


Fig 4.6. Dry etching results with 50sccm SF_6, 40sccm Ar, 60mT pressure and a) 30W RF power; b) 120W RF power

After the effect of RF power being studied, the investigation was focused on the effect of Ar plasma to the trench structure shape. The RF power was changed back to 60W for this experiment. The Ar gas flow rate was increased to 100sccm first and the result is shown in Fig. 4.7.

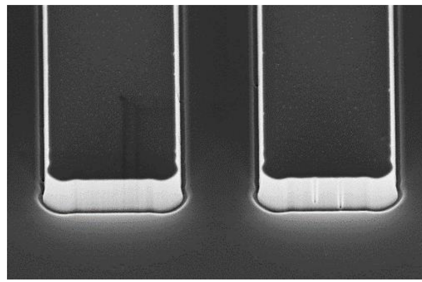
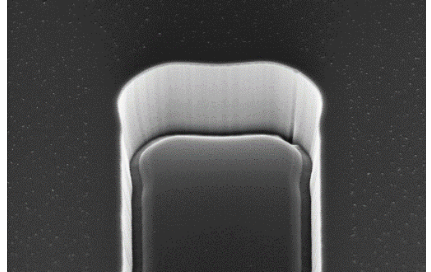



Fig 4.7. Dry etching results with 50sccm SF_6, 100sccm Ar and 60mT pressure

The micro-trench was relatively deep by observation. The next step was to reduce the Ar gas flow rate to 25sccm. This was supposed to keep the same pressure when reducing the gas flow rate, however, the pressure had to be reduced to 40mT since the total gas flow rate is related to the feasible pressure range in the chamber. The micro-trench was still not eliminated with the new conditions as shown in Fig. 4.8.

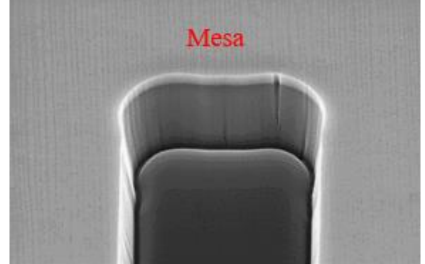


Fig 4.8. Dry etching results with 50sccm SF_6, 25sccm Ar and 40mT pressure

The Ar flow rate was further reduced to a minimum where there was no Ar flow at all. The dry etching result is shown in Fig. 4.9 and the micro-trench is still not eliminated. This experiment is critical since it draws a conclusion that most likely the formation of micro-trench is not relevant to Ar plasma since the micro-trench was formed even without Ar flowing into the chamber.

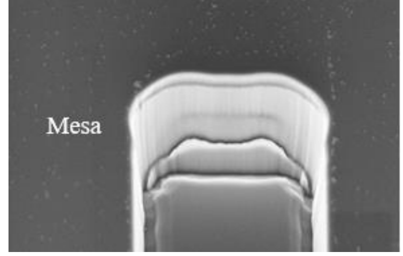
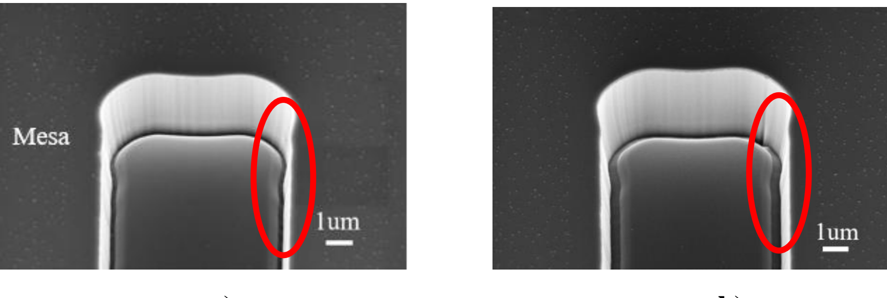


Fig 4.9. Dry etching results with 50sccm SF_6, 0sccm Ar and 40mT pressure

The systematic ICP parameter study finished here with more than 15 failure attempts that some of the experiments are not shown in this thesis. The effect of RF power, pressure and the gas flow ratio have been studied and no solution was found at this stage. Although

the best dry etching recipe was still not found, enough results were collected after the systematic study. The collected results were then analysed with one assumption made.



a) b)

Fig 4.10. Trench shapes etched with gas flow ratio a) SF6: Ar = 5:4; b) SF_6: Ar = 1:2

The etching results from Fig. 4.5 and Fig. 4.7 were compared in Fig. 4.10. The gas flow ratio of SF_6: Ar was the only different etching condition. From Fig. 4.9, only SF_6 can be responsible for the micro-trench formation. When the SF_6: Ar ratio was reduced to 1:2, the width of the micro-trench structure was expanded as shown in Fig. 4.10b). The question was then what would happen if the SF_6: Ar ratio was further reduced. There was an assumption that if the SF_6: Ar gas flow ratio is reduced further, the width of the micro-trench structure will be increased even more, if the micro-trench open width is increased to be half of the main trench width, then the micro-trench basically disappears. To verify this assumption, a new experiment was carried out. A SF_6: Ar ratio of 1:10 was used as an extreme condition. To make sure the trench sidewall is approximately 90 degrees to the top surface, the chamber pressure was reduced to 10mT. 100W RF power was employed for higher etch rate.

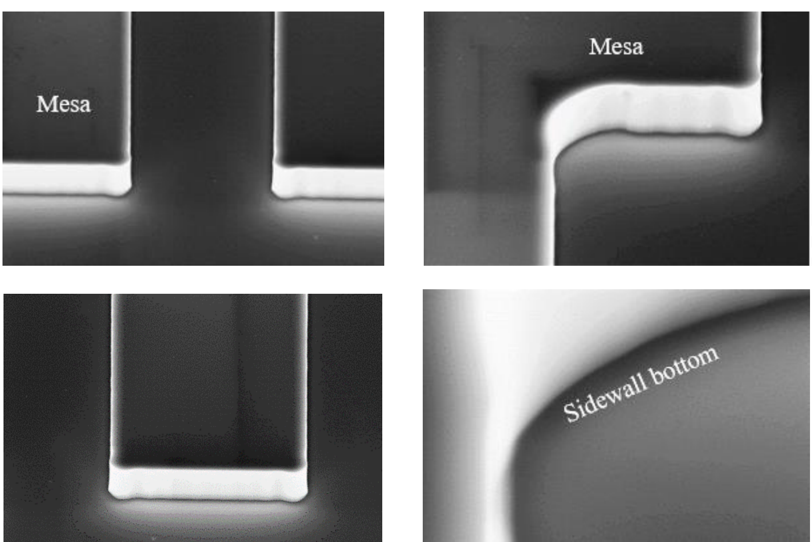
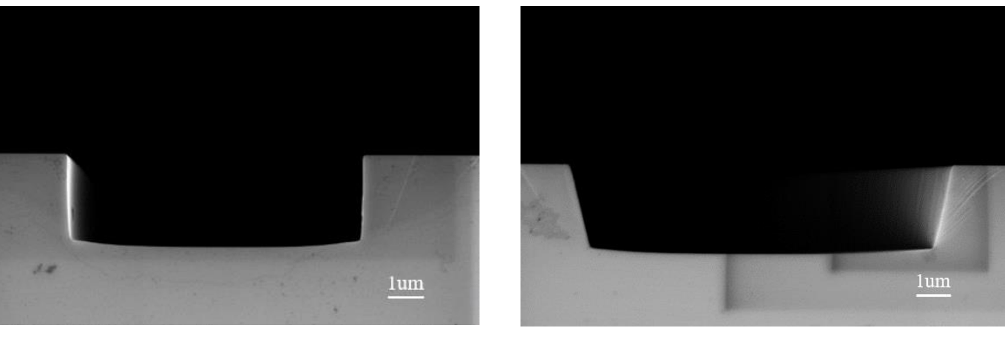


Fig 4.11. Trench shapes etched with SF_6: Ar gas flow ratio = 1:10, 10mT pressure and 100W RF power

The etching result for the new condition was shown in Fig. 4.11 and surprisingly the micro-trench was successfully eliminated. SF_6: Ar gas flow ratio was proved to be the most critical parameter for the micro-trench formation. Fig. 4.12 compares the etching results using the new recipe with varied RF power. If the RF power is increased from 100W to 150W, the trench sidewall angle is increased as well. The trench sidewall slope control with ICP parameters can provide more flexibility during device fabrication process.



a) b)
Fig 4.12. SEM photos on trench structures with a) Selectivity = 8:1 100W RF Power; b) Selectivity = 4:1 150W RF Power

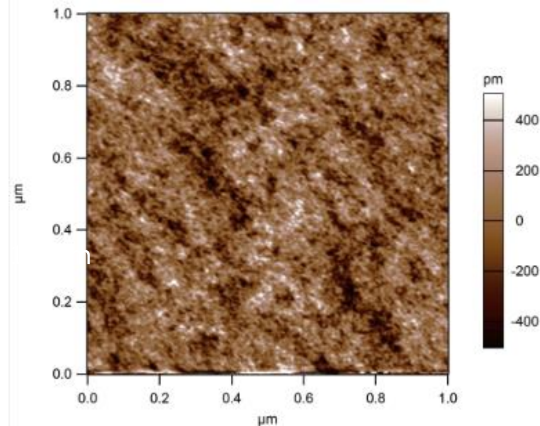


Figure 4.13. AFM measurement on etched trench bottom surface

Since the trench sidewall was difficult to characterise, the roughness of the bottom of the trench structure was measured by AFM for reference. A root-mean-square (rms) roughness of 183pm was extracted indicating that a very smooth surface was achieved by the dry etching process.

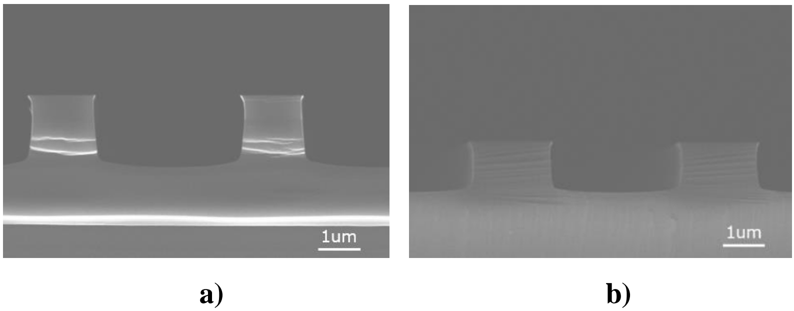
Table 4.3 Etching rate versus RF power, the pressure is fixed at 10mTorr

RF power (W)	SiC etch rate (nm/min)	Al_2O_3 etch rate (nm/min)	Selectivity
50	208	25	8.3:1
100	294	35	8.4:1
150	308	74	4.2:1

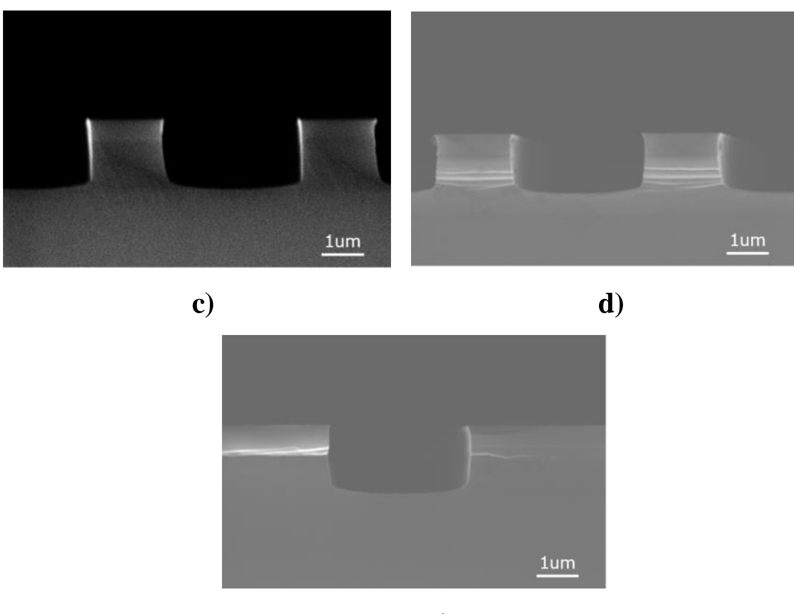
The etch rate and the selectivity of the etching recipe were measured and are presented in Table. 4.3. The SF_6: Ar gas flow ratio was fixed at 1:10. The pressure was kept constant at 10mTorr and only the RF power was the variable. The RF power seems to have clear effect on the etch rate of both SiC and Al_2O_3. When the RF power is adjusted from 100W to 150W, the etch rate of Al_2O_3 is doubled while the etch rate of SiC has not changed aggressively. When the RF power is reduced from 100W to 50W, both the etch rate of SiC and Al_2O_3 reduce accordingly, however, the selectivity remains the same. The high sensitivity of Al_2O_3 etch rate against RF power to some extent indicates that physical etch is more likely to dominate during the Al_2O_3 etching process. 100W RF power is a suitable choice to maintain acceptable SiC etch rate and high selectivity in the meantime.

4.4. Trench structure optimisation

This section investigates the further improvement of the trench structure with post-etch process and pre-etch treatment as well. It is shown in [4] that high temperature annealing with hydrogen ambient would round the trench top and bottom corners. It is very important to smooth any sharp corners in the trench structures since they will lead to early oxide breakdown and reliability issues.



a) **b)**



e)

Figure 4.14. The trench structures post-etch annealing under forming gas ambient for 2 hours at a) 450ºC; b) 600ºC; c) 800ºC; d) 1100ºC and e) 1500ºC

Unfortunately, it does not seem that the forming gas annealing has produced any positive effect on the shapes of the trench structures. All the trench structures look very similar even after annealing at various temperatures. It may be because of the low percentage (5%) of hydrogen in the forming gas, and the pressure of the tube furnace was not controlled as well. In this case, no direct comparison can be made to the literature.

Even though the trench corner rounding process was not successful, it is not difficult to fabricate a trench structure with rounded bottom corners. The proposed process flow is shown in Fig. 4.16. An extra TEOS layer will be deposited after the deposition of the Al_2O_3 as the etching mask followed by TEOS etch back process and a structure like Fig. 4.15c can be produced. Based on the different etch rate of TEOS and Al_2O_3, a trench structure with rounded bottom corner may be possible to fabricate.

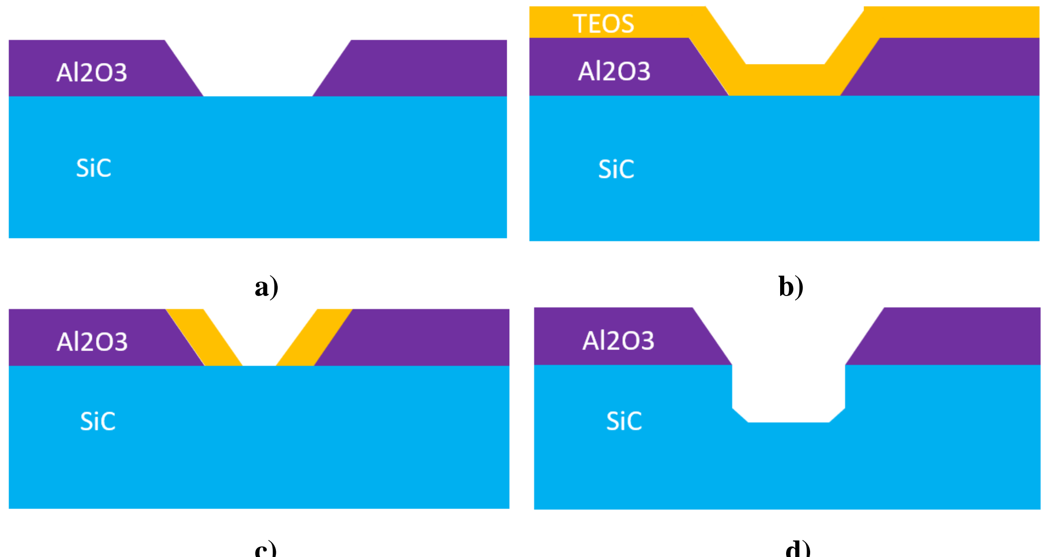


Figure 4.15. Self-alignment process used to produce rounded trench bottom corners

To verify the idea, trench structures were fabricated again following the proposed process flow. 600nm Al_2O_3 dry was deposited by evaporation and lift-off process. 1μm TEOS was then deposited with LPCVD followed by dry etching process to remove the TEOS on top of the Al_2O_3 layer. A SEM photo was taken to observe the TEOS remaining at the sidewall referring to Fig. 4.16a). SiC was then etched to a depth of 1.5μm using the recipe developed previously and the cross section is presented in Fig. 4.16b). It can be confirmed that the bottom of the trench corner has been rounded with the proposed processing flow. The trench surface can be further smoothed by thermal oxidation.

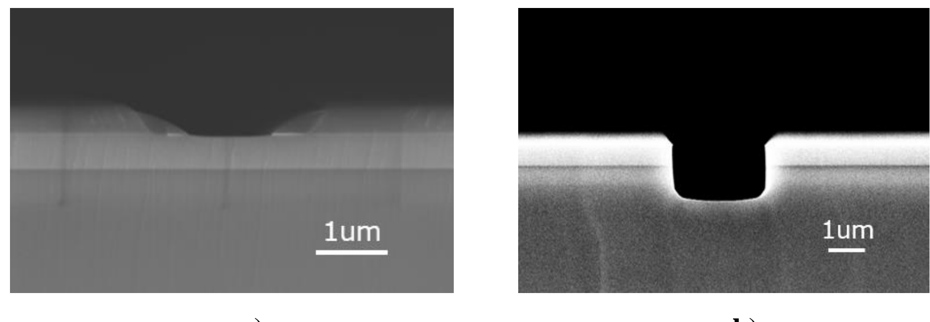


Figure 4.16. SEM photo taken after a) TEOS etch back; b) SiC etching

4.5. Summary

This chapter focuses on trench structure fabrication and optimisation. The quality of the trench structure is critical for trench device fabrication in terms of robustness and reliability. The physical shape of the trench structure also affects the design and fabrication process of the trench devices, for instance, the slope on the sidewall can result in unexpected implantation into the trench sidewall while the trench bottom implantation is needed.

The dry etching process with Al_2O_3 mask has been studied systematically and optimised recipes developed successfully. Trench structures can now be etched without micro-trenches and the trench bottom corner can be rounded with only one extra processing step. The trench top corner is not rounded intentionally or properly, however, a thermal oxidation process can help on trench corner rounding as well.

Trench device design and fabrication should be the next step since the trench etching process has been developed successfully. Further optimisation of the trench structure etching process will remain as future work which is beyond the scope of this thesis.

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Chapter 5 1st generation trench MOSFET design and fabrication

This chapter introduces the design and fabrication processes of the 1st generation trench MOSFETs. These first-generation devices are primarily used to verify the trench structure dry etching process developed previously. This chapter starts with technology computer aided design (TCAD) Silvaco simulation for the MOSFET cell layout followed by photo mask design. The fabrication processes are then described in detail followed by the electrical characterisation results.

5.1. TCAD Silvaco simulation

The design target of the blocking voltage for the 1st generation devices is 1200V. The wafer specification is shown in Fig. 5.1.

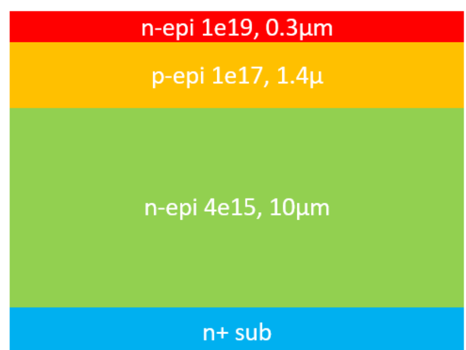


Figure 5.1. The wafer specification for 1st generation devices

The p-base and n+ layers are both epitaxial layers, therefore, it saves several implantation steps and makes the fabrication process easier to start with.

5.1.1. Edge termination design

Blocking capability is the fundamental requirement for power devices. With a proper device design, the avalanche breakdown should appear at the main junction. A proper edge termination design is critical for reducing the two-dimensional electric field crowding at the edge of the main junction and maximizing the blocking capability of the material. The breakdown often happens at the edge of the device at much lower blocking voltages if the edge termination is not designed correctly. Junction termination extensions (JTEs) and floating field rings (FFR) are the two most commonly used termination structures for power devices.

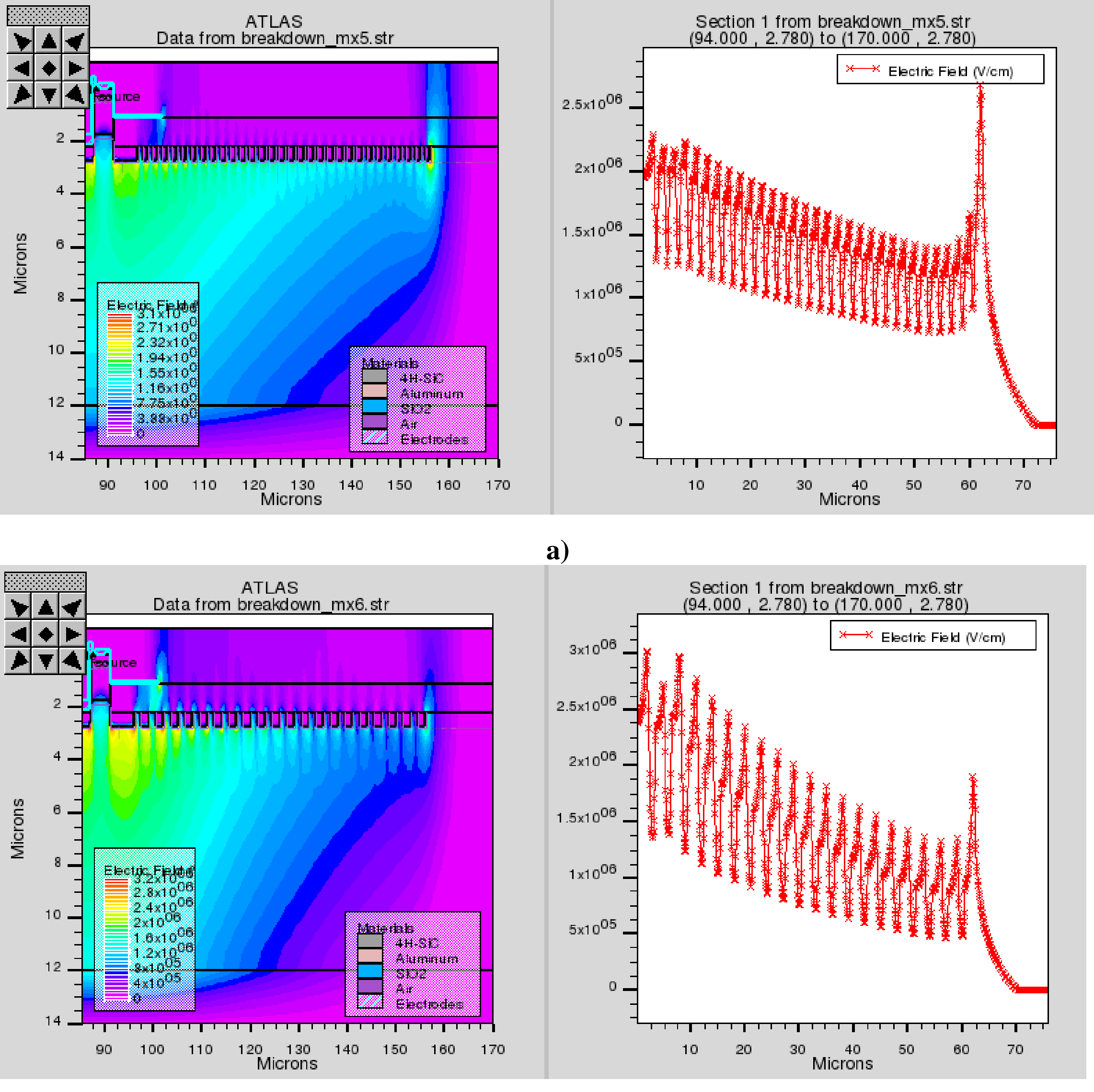
The simplest edge termination is the trench termination which only adds one extra dry etching step in the fabrication process. Trench termination is a useful design choice for devices with a blocking voltage less than about 2kV. Using this simple technique, the electric field can be linearized near the PN junction at the edge of the devices, therefore the electric field at the bottom of the trench can be significantly lower than the device without any termination [1]. For a trench termination either with or without a field plate, the electric field in the field oxide can be relatively higher compared to other termination techniques. There is a high risk of field oxide breakdown due to excessive traps in the LPCVD deposited oxide, and therefore trench termination was not selected for the 1st generation trench MOSFET design.

JTEs is a widely used technique especially for high voltage devices since it saves chip area in comparison to FFR termination. This termination is made of one or more p-type regions with carefully selected doping concentration next to the main junction. The dose of the termination region must be lower than the main junction so that these p-type regions can be fully depleted before avalanche breakdown can happen at the edges [1]. The electric field will be distributed across the JTEs and field crowding can be reduced.

FFR termination consists of isolated highly doped p+ rings with specific width and space between them [1]. Compared to JTEs, FFR termination does not usually require an extra implantation step. The rings need to be highly doped, therefore, p-ring implantation can be done in the same time with the p+ source implantation. Besides, FFR termination does not have strict requirements on the implantation activation rates which is more

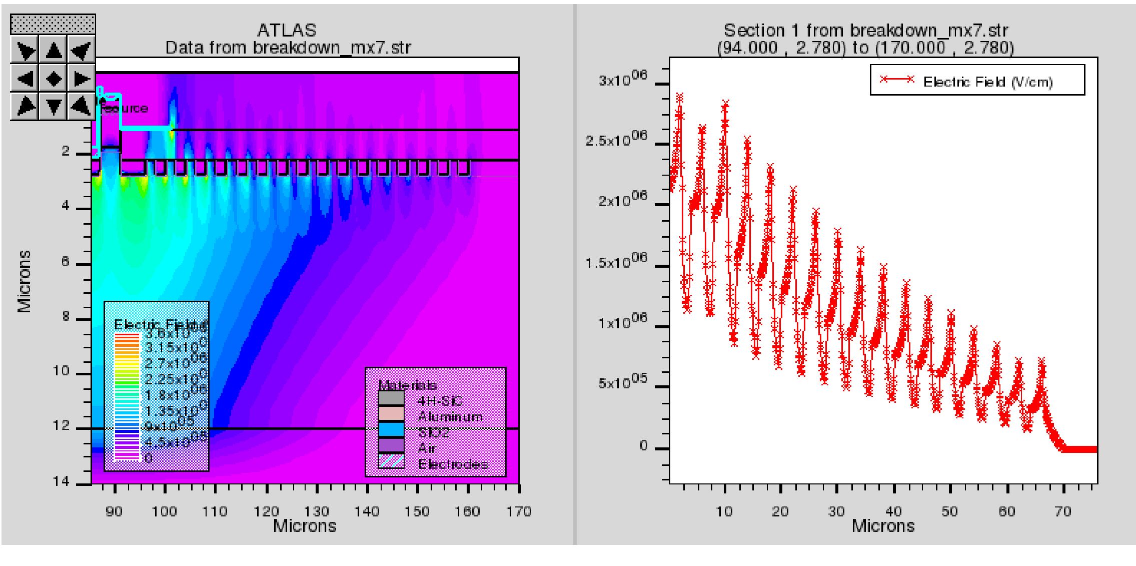
sensitive for JTEs. As a result, JTEs were considered as an option for the 1st generation trench MOSFETs based on the consideration of process complexity and cost.

FFR termination with fixed/varied p-ring space and width have both been considered in the design. Fig. 5.2 shows the simulation results of the electric field distribution with fixed p-ring space/width of 1μm, 1.5μm and 2μm respectively. The chip area allocated for this edge termination is fixed for all the three options.



a)

b)



c)

Fig. 5.2. The simulated electrical field distribution with fixed p-ring space/width at a) 1µm, Vbr=1440V; b) 1.5µm, Vbr=1830V; c) 2µm, Vbr=1550V

It is shown in Fig. 5.2a) that the electric field has been spread out efficiently with low electric field close to the main junction and most of the p-rings, however, the peak electric field locates at the last ring indicating that more floating rings are needed. Fig. 5.2c) presents the opposite results compared to Fig. 5.2a), where the electric field is not spread out effectively and the peak electric field is still close to the main junction. There is a trade-off when selecting the optimum p-ring space and width. If the p-ring space/width is too small e.g. 1µm, more chip area is necessary to spread the electric field and it also increases the difficulty in the fabrication process; if the p-ring space/width is too large e.g. 2µm, the electric field cannot be spread out effectively, therefore, adding more rings makes no difference in terms of the breakdown voltage; 1.5µm p-ring space/width is easier to fabricate and it saves chip area in comparison to the 1µm option, more importantly it is able to spread the electric field evenly away from the main junction.

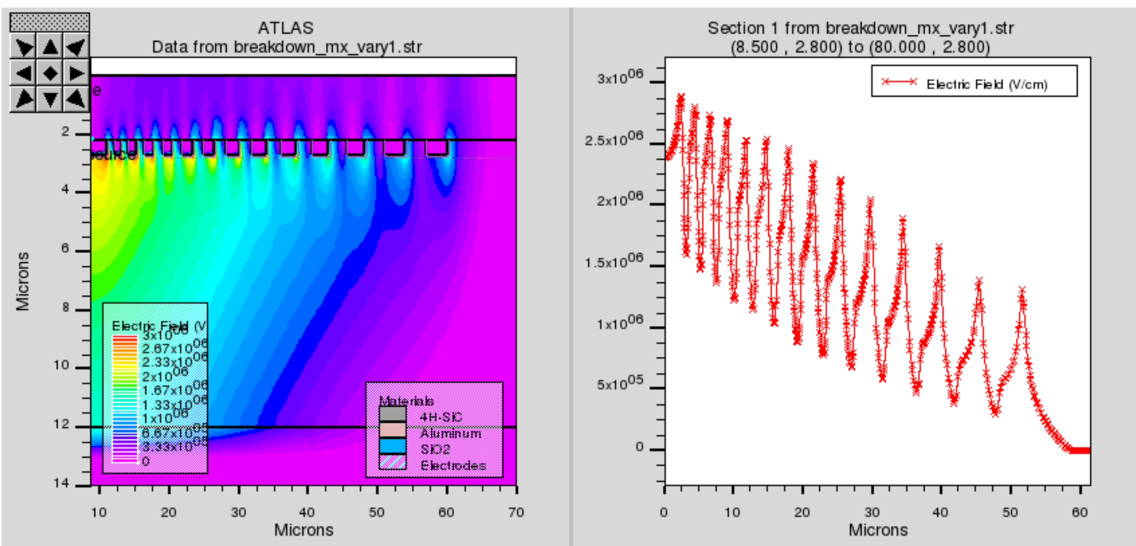
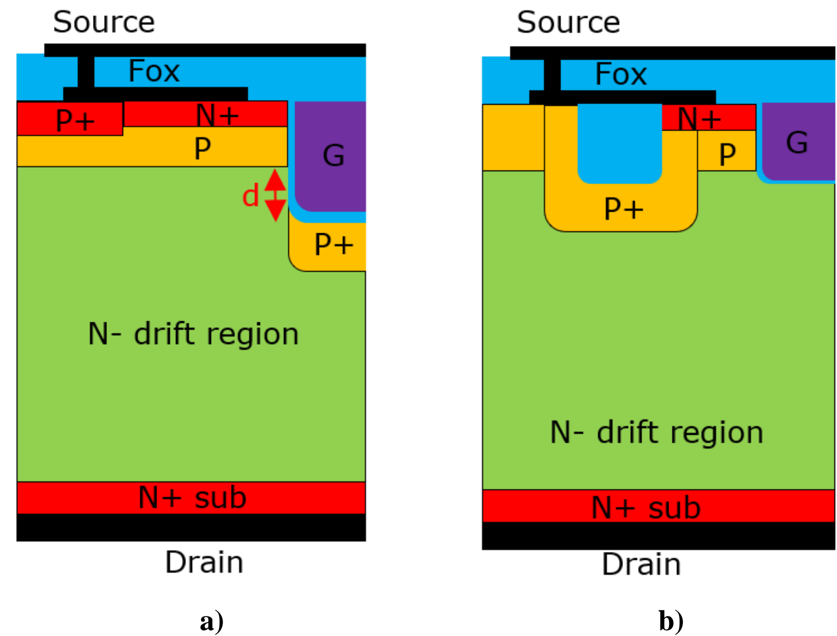


Fig. 5.3. The simulated electrical field distribution with p-ring/space starting from 1μm and an expansion ratio of 1.1

Varied p-ring space/width seems to be the most efficient option for the edge termination design as shown in Fig. 5.3, which then requires less chip area and spreads the electric field evenly away from the main junction. Both fixed and varied p-ring space/width options are used for the 1st generation trench MOSFETs.

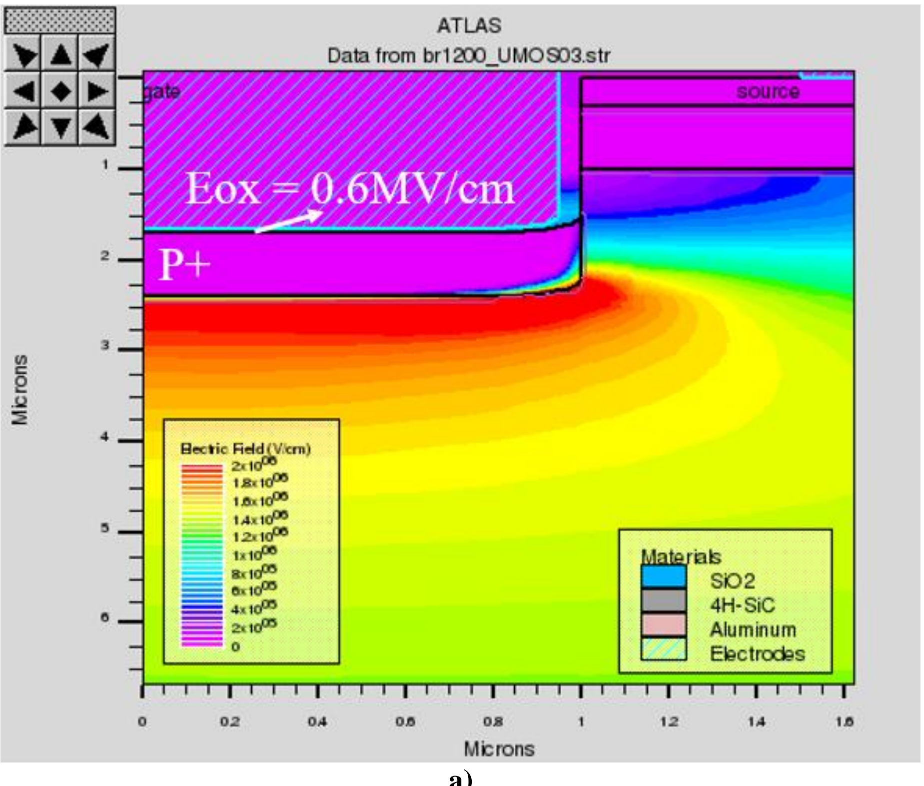
5.1.2. Gate oxide protection and on-state performance

Due to the high critical field of 4H-SiC material, the gate oxide grown on the trench structure exhibits a high electric field and reduces the device breakdown voltage. There are two main methods used to protect the oxide from high electric field in the literature. The first method is to introduce a p+ shielding region below the gate trench which effectively moves the high electric field away from the oxide towards the p+ n junction [2,3]; another method is to use a double trench structure as shown in Fig. 5.4b), the deep p+ implant at the source trench can effectively reduce the electric field at the gate oxide[4,5]. The simulated electrical field distribution of these two device layouts are presented in Fig. 5.5. Apparently, the added p+ region can effectively shield the gate oxide in both designs. The specific input and output capacitance will increase if p+ shielding region is added to the bottom of the trench structure while C_{GD} will decrease. This extra p+ region will create a parasitic JFET region and increase the R_{ON_SP} which must be designed or considered carefully.

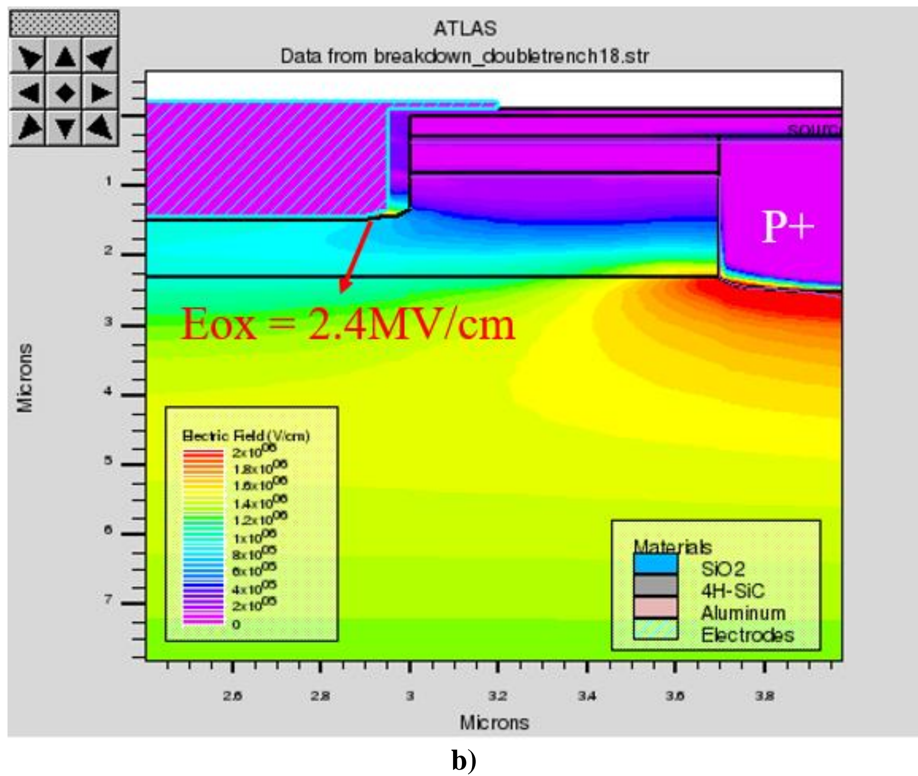


a) b)

Fig. 5.4. Trench gate oxide protection method a) P+ shielding region below gate trench; b) double trench method with p+ implant at the source trench bottom



a)



b)

Fig. 5.5. The simulated electric field distribution at 1.2kV reverse biased for a) P+ shielding region below gate trench; b) double trench method with p+ implant at the source trench bottom

For the 1st generation trench MOSFET design, the structure in Fig. 5.4a) was used since the p+ shielding region could be implanted at the same step with the floating field-ring termination and p+ source implant. The gate trench depth is a design parameter to which can be simulated if the p+ trench bottom implantation is needed. For Si devices, a trench gate structure eliminates the JFET region formed by adjacent p-base regions of planar gate MOSFETs. For SiC devices, the p+ shielding region implanted on the bottom of the gate trench re-introduces a parasitic JFET region formed by the n- drift region and p-base region and itself. This JFET region, if not dealt with carefully, will reduce the current density of the device drastically.

In these first-generation devices, only the clearance between the p+ shielding region and p-base region is modified as a design parameter. The clearance "d" is shown in Fig. 5.4a) which can be varied by controlling the trench etching process. Fig. 5.6 shows the simulation results of the on-state current density with various clearance distance between p+ trench bottom shielding region and the p-base region. The simulation used a device structure without p+ trench bottom shielding region as a reference. The current density is

not affected if the clearance is more than 1.5µm. Although using deeper trenches can mitigate the effect of the parasitic JFET region, it also reduces the breakdown voltage as well. The breakdown voltage is reduced from 1650V to 1450V if the clearance distance increases from 0.3µm to 1.5µm. As a result, a clearance of 1µm was chosen as a compromised solution.

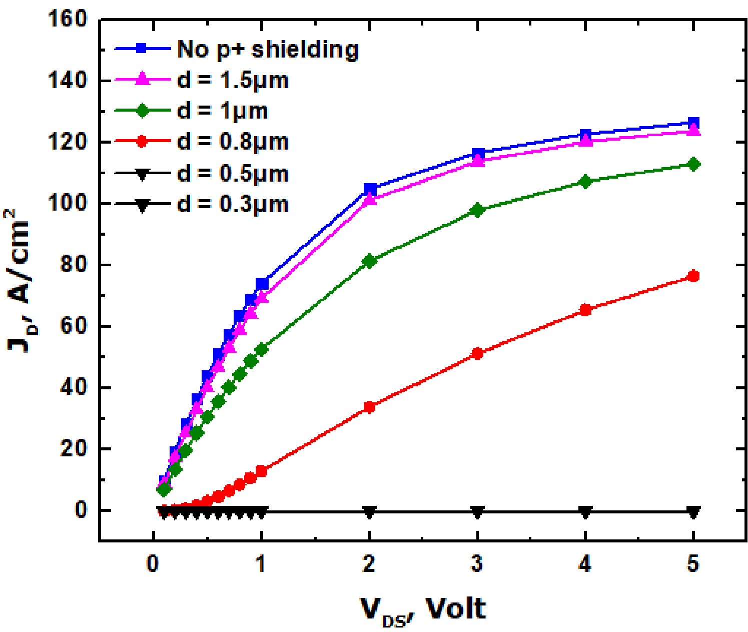


Fig. 5.6. The IV characteristics of the trench MOSFETs with varied clearance "d" between the p+ trench bottom shielding region and the p-base region

5.2. Photo mask design

Since it was the first-generation device design, it was reasonable to use small size chips (1cm × 1cm) for fabrication instead of quarter wafers or even a whole wafer to minimize the risk. A top view of the mask layout is presented in Fig. 5.7. The target current density for most of the devices is less than 150A/cm^2 to reduce the processing difficulty with a large cell pitch of 23µm. High current density cells were designed for process evaluation purpose with much smaller cell pitches. PiN diodes were included as well to verify the edge termination design.

The alignment marks are shown in Fig. 5.10 where the minimum alignment clearance is 2μm. In the alignment step, coarse alignment is first done with the large alignment marks followed by more accurate alignment with the small alignment marks.

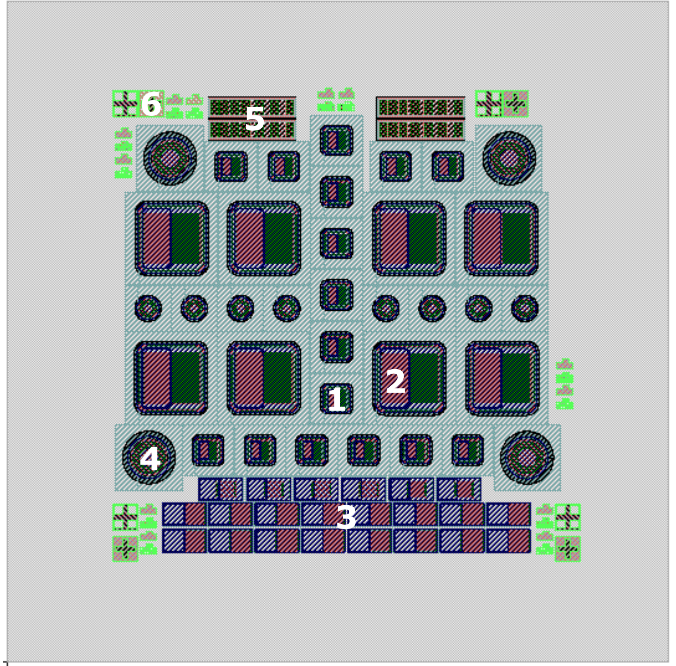


Fig. 5.7. Mask layout for the 1st generation trench MOSFETs

Number 1 to 6 are labelled in Fig. 5.7 for 13-finger MOSFETs, 37-finger MOSFETs, small pitch evaluation cells, PiN diodes, TLM structures and alignment marks respectively.

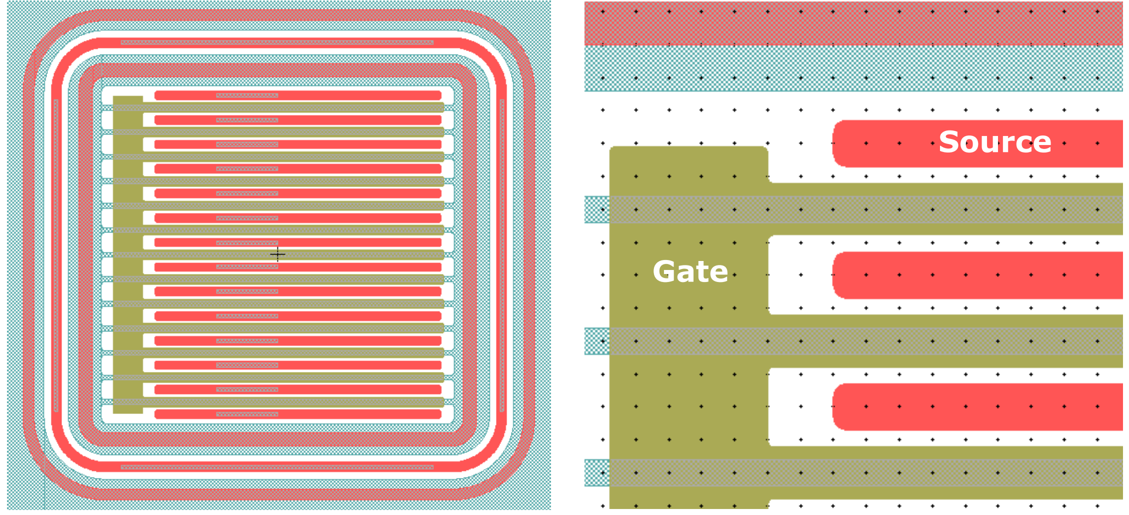


Fig. 5.8. 13-finger trench MOSFET mask layout

Red pattern in Fig. 5.8 corresponds to source contact region as the green pattern is for the gate metal and the light blue pattern is the gate trench and the mesa structure around the edge of the active area.

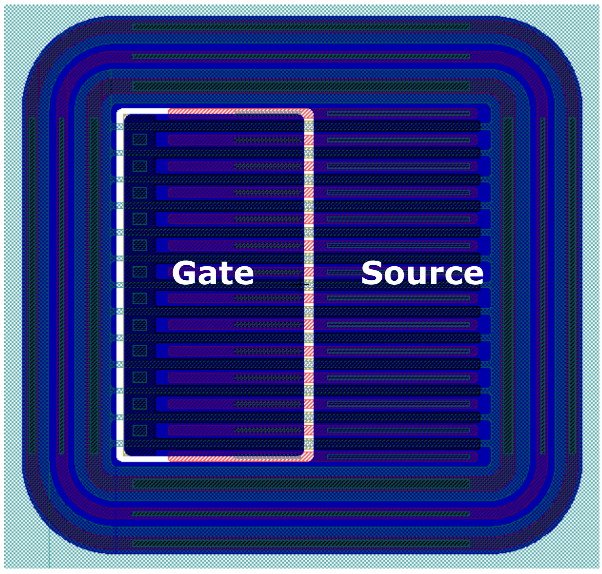


Fig. 5.9. 13-finger trench MOSFET mask layout with the pad metal

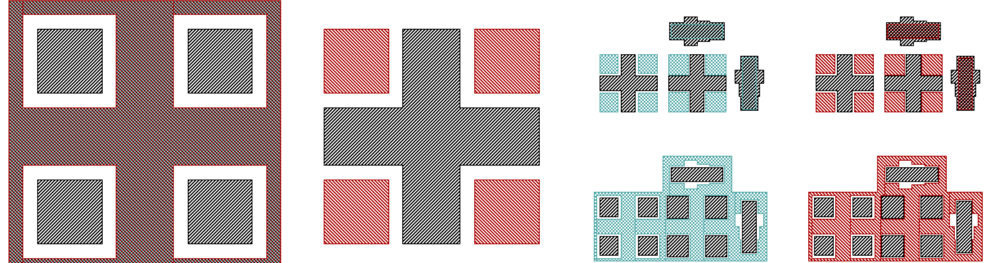


Fig. 5.10. Alignment marks used for the 1st generation trench MOSFET

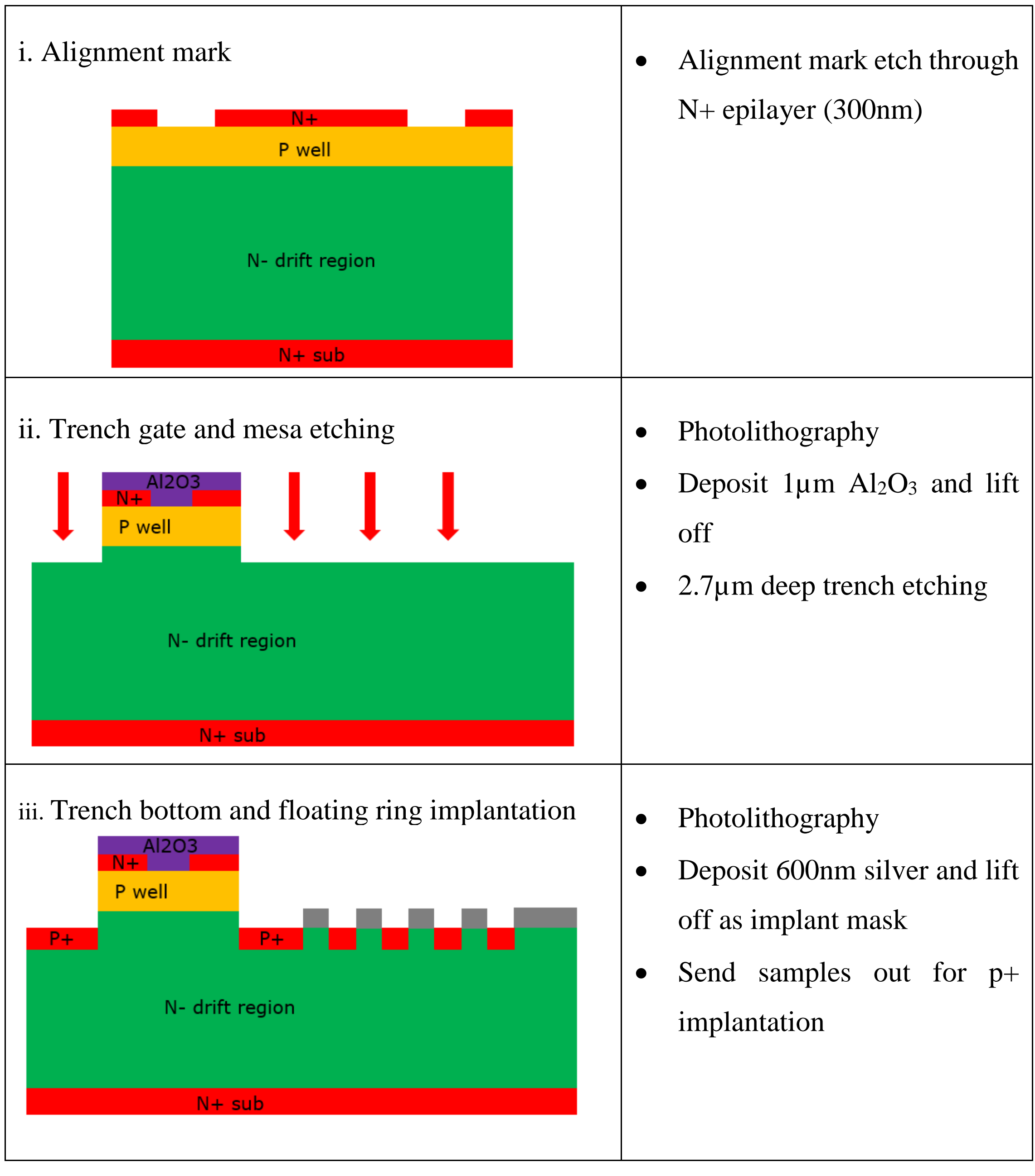
5.3. Device fabrication

5.3.1 Process flow

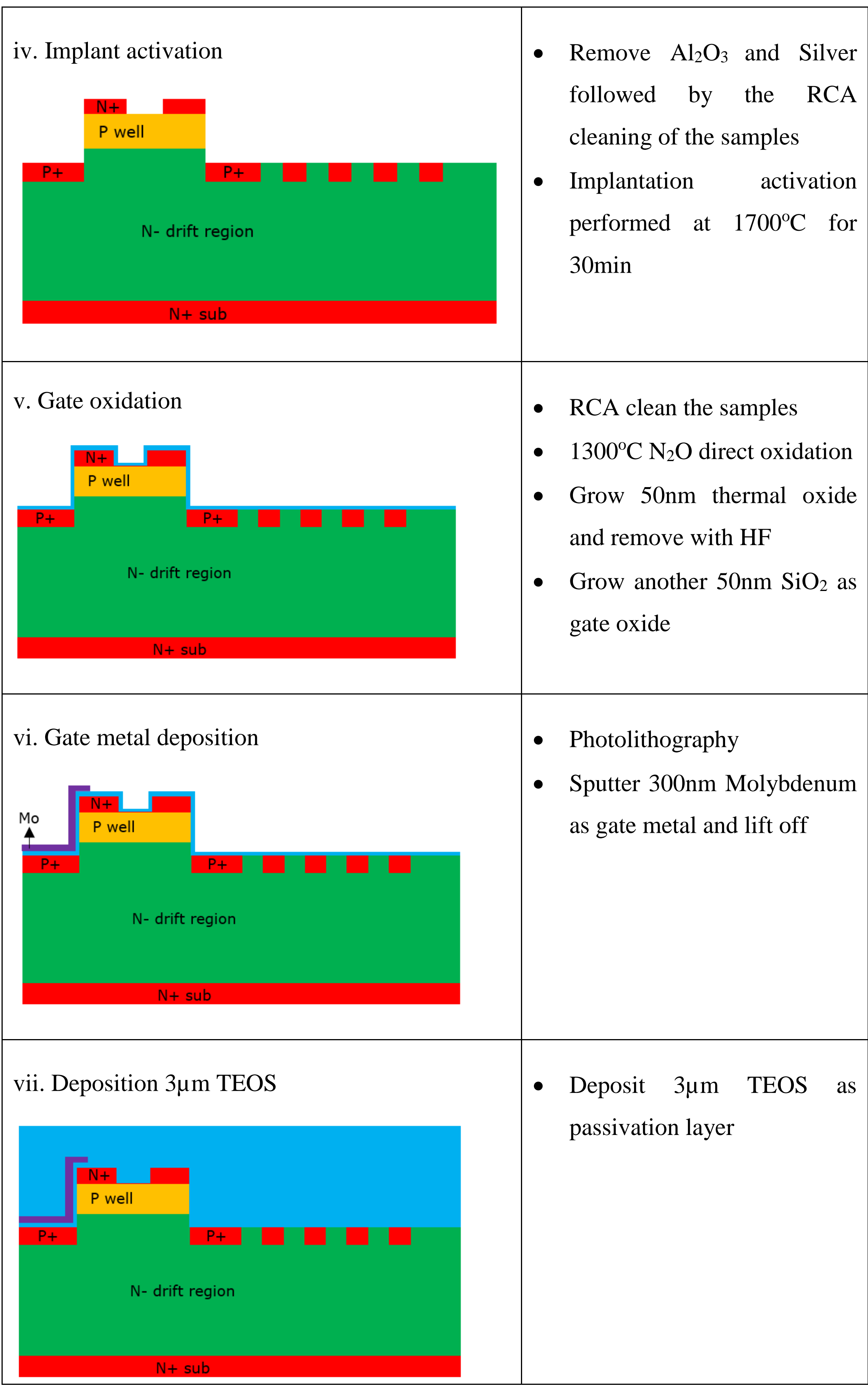
The process flow for the first generation 1.2kV trench MOSFET is presented in Table 5.1. The n+ epilayer doping is $1\times10^{19}cm^{-3}$ with a thickness of 300nm while the p-base epilayer doping is $1\times10^{17}cm^{-3}$ with a thickness of 1.4µm. With n+ and p-base epilayers, the fabrication process can be simplified since only one implantation step is necessary.

The p+ trench bottom shielding region can be implanted in the same step as the p+ floating field rings.

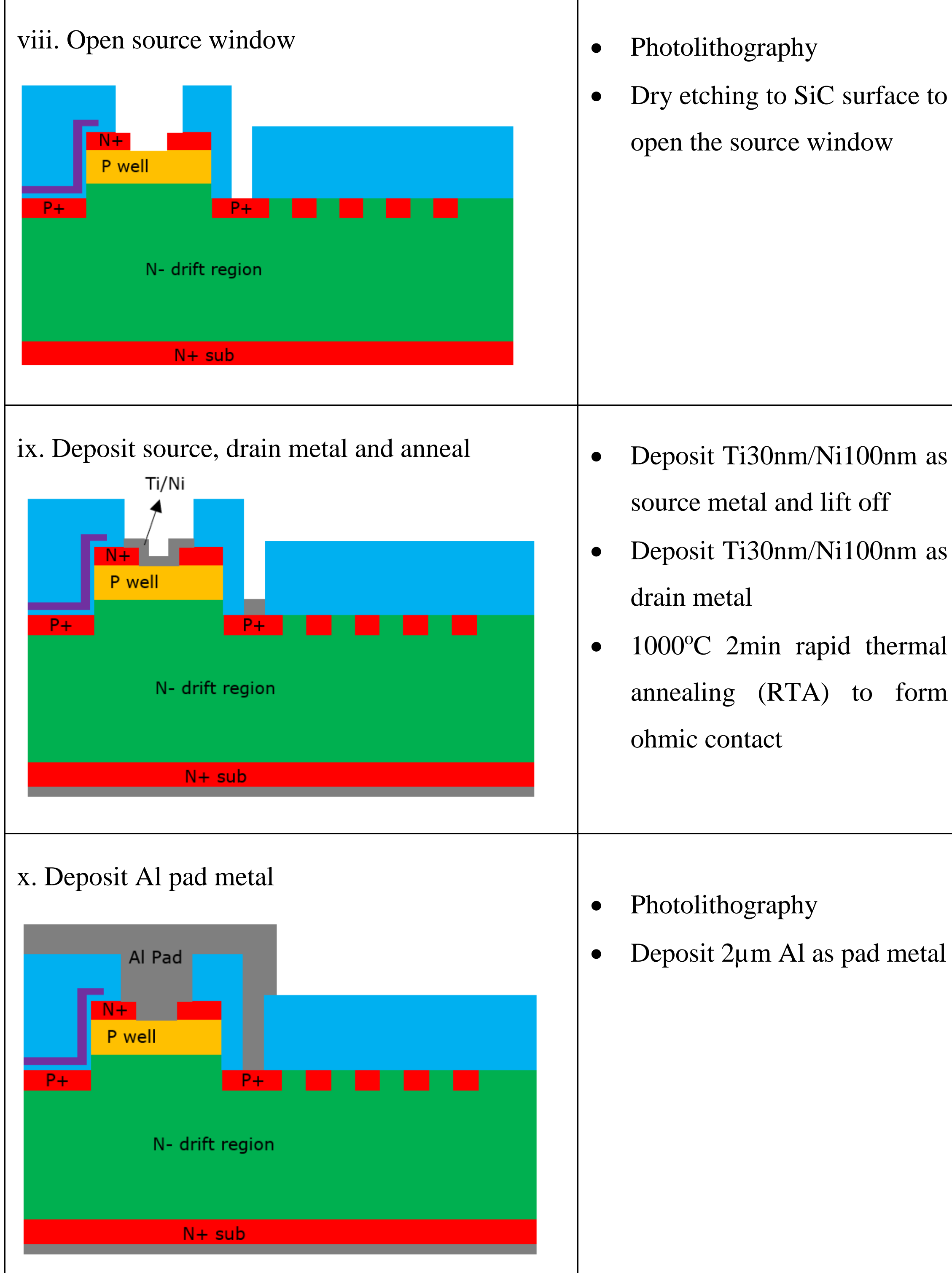
Table 5.1 The process flow for 1.2kV trench MOSFET



Step	Process
i. Alignment mark	• Alignment mark etch through N+ epilayer (300nm)
ii. Trench gate and mesa etching	• Photolithography • Deposit 1μm Al_2O_3 and lift off • 2.7μm deep trench etching
iii. Trench bottom and floating ring implantation	• Photolithography • Deposit 600nm silver and lift off as implant mask • Send samples out for p+ implantation



Process step	Description
iv. Implant activation	• Remove Al_2O_3 and Silver followed by the RCA cleaning of the samples • Implantation activation performed at 1700°C for 30min
v. Gate oxidation	• RCA clean the samples • 1300°C N_2O direct oxidation • Grow 50nm thermal oxide and remove with HF • Grow another 50nm SiO_2 as gate oxide
vi. Gate metal deposition	• Photolithography • Sputter 300nm Molybdenum as gate metal and lift off
vii. Deposition 3µm TEOS	• Deposit 3µm TEOS as passivation layer



Step	Process
viii. Open source window	• Photolithography • Dry etching to SiC surface to open the source window
ix. Deposit source, drain metal and anneal	• Deposit Ti30nm/Ni100nm as source metal and lift off • Deposit Ti30nm/Ni100nm as drain metal • 1000°C 2min rapid thermal annealing (RTA) to form ohmic contact
x. Deposit Al pad metal	• Photolithography • Deposit 2μm Al as pad metal

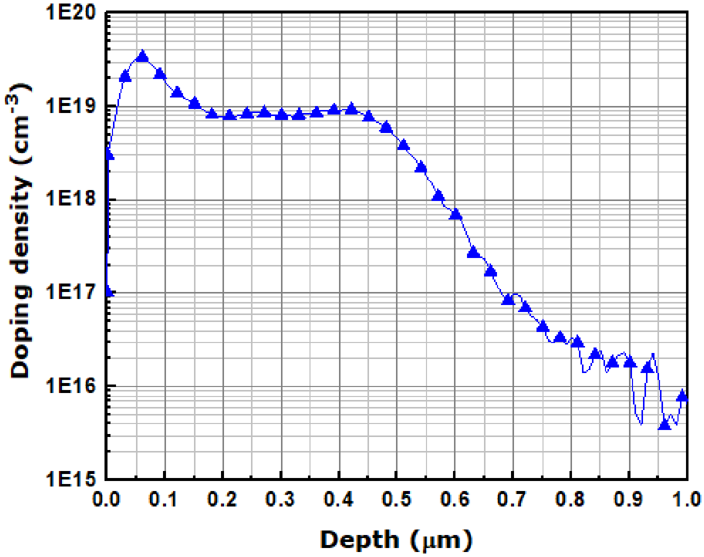


Fig. 5.11. Implantation profile simulated by TCAD Silvaco

The p+ implantation profile was simulated using Silvaco and the result is presented in Fig. 5.11. The initial higher doping is set for the ohmic contact formation and followed by a box profile with several implants.

5.3.2 Processing difficulties

High resolution photolithography is quite a challenge for trench devices since the surface is not flat. A minimum feature of 1.5μm is required for the floating field rings which is relatively difficult to achieve.

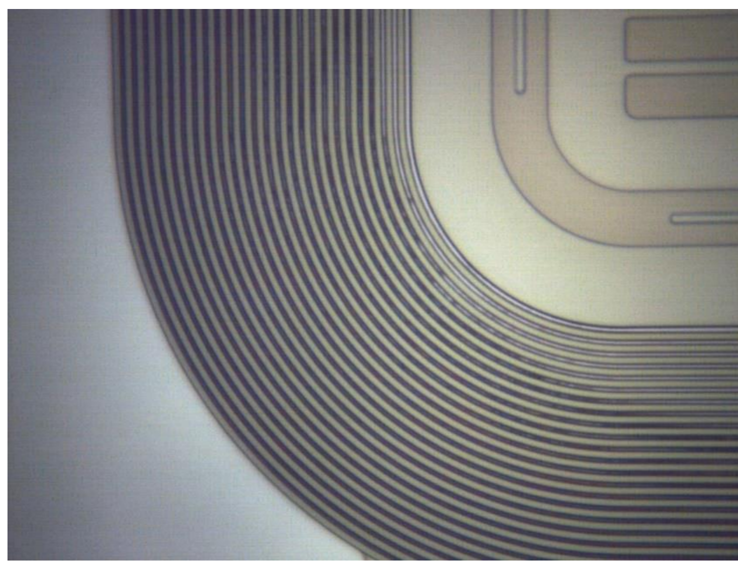


Fig. 5.12. The challenge for high-resolution (1~2μm) lithography process

It is shown in Fig. 5.12 that the photolithography process had a problem in opening a 1.5μm window. Because the photolithography process for the floating field rings will be done at the bottom of the mesa structure where the the n+ and p-base epilayers is etched away, it increases the processing difficulty. To solve this problem, each step of the photolithography processes needs to be reinvestigated and improved including the spin coating process, softbake, edge bead removal, exposure dose, post-exposure bakes and development as shown in Fig. 5.13.

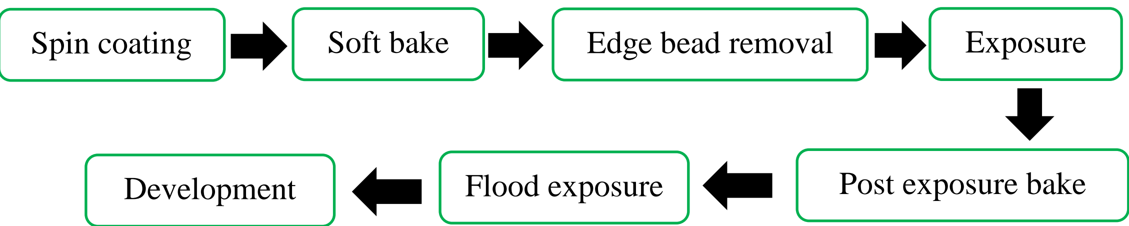
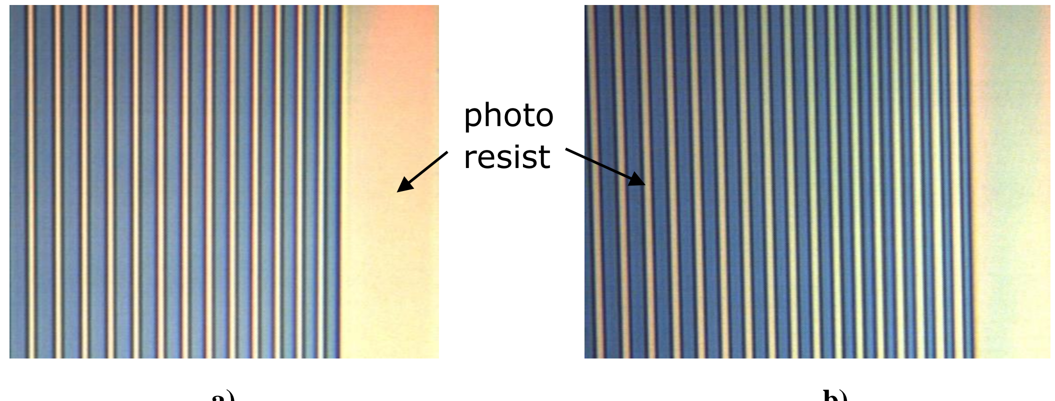


Fig. 5.13. The photolithography processes used for typical negative photoresist AZ5214

The spinning speed should be increased accordingly to reduce the thickness of the photoresist for small features. Edge bead removal is a critical step to eliminate the thick photoresist at the edge of the sample to reduce the distance between the mask and the active area of the sample during exposure as shown in Fig. 5.14.

Fig. 5.14. The gap between the mask and the photoresist a) with edge bead; b) without edge bead

Post exposure bake (PEB) is the most important step for a negative photoresist like AZ5214. The bake time and temperature have a very large effect, especially on small features. When the bake time is too long, or the temperature is too high, it results in the increased difficulty of development; if the bake time is too short, or the temperature is too low, the feature size can be widened compared to the original design.



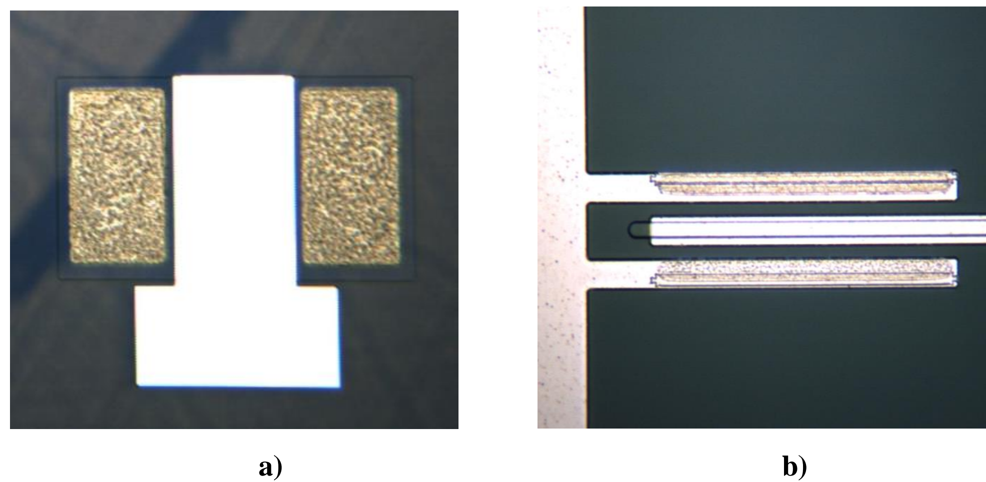
a) **b)**

Fig. 5.15. Floating ring photolithography results with a) PEB temperature = 115°C; b) PEB temperature = 120°C

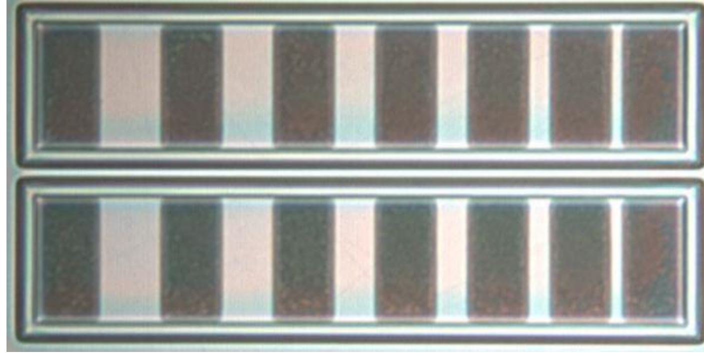
As a result, the photolithography process for small features must be calibrated carefully to produce the designed features.

5.3.3 Test structures

Test structures were fabricated with the real MOSFET devices to verify the fabrication process. Long channel MOSFETs were used to extract and verify the channel mobility. TLM was employed to validate the quality of the ohmic contact. A single finger trench MOSFET without termination structure was fabricated to focus on on-state performance.



a) **b)**



c)

Fig. 5.16. Test structure optical microscopy photos of a) Long channel MOSFET; b) Single finger vertical trench MOSFET; c) TLM structure made on n+ epilayer

5.3.4 Fabrication process

This section presents some of the fabrication processes with optical microscope and SEM images. For instance, it is shown in Fig. 5.17 that 1µm Al_2O_3 was deposited as dry etch mask. The same Al_2O_3 layer was used as an implantation mask as well to form the self-aligned p+ trench bottom shielding region.

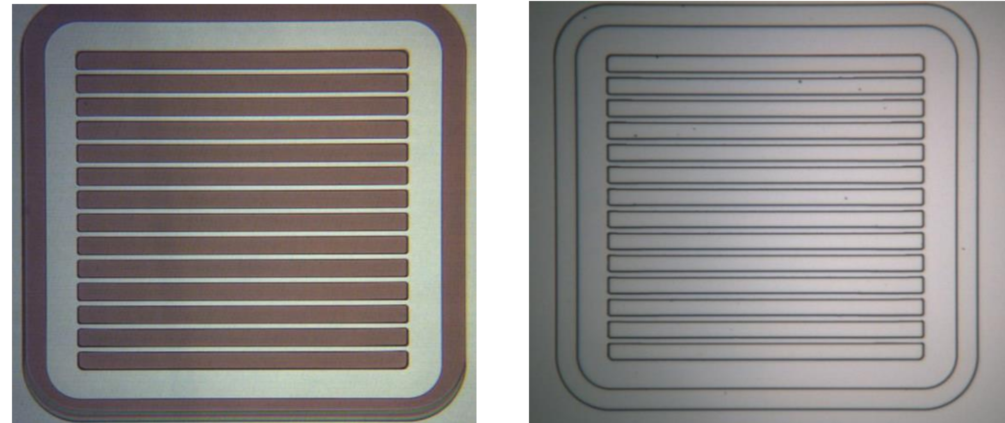
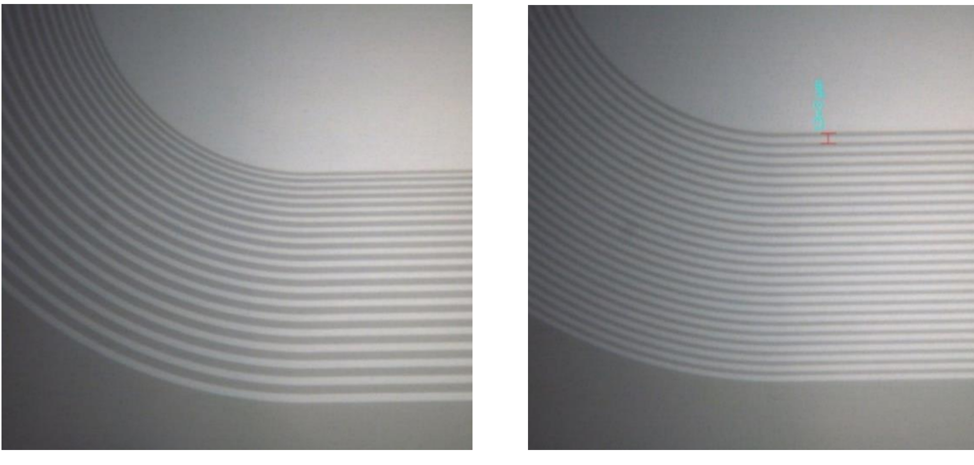


Fig. 5.17. Sample with Al_2O_3 deposited as trench etching mask (left) and the sample cleaned after the implantation process (right)



a) b)

Fig. 5.18. Floating field rings implantation damage on SiC surface with a) varied ring space/width; b) fixed ring space/width

Fig. 5.18 shows the implantation damage pattern for the floating field rings. The ring space is either fixed or varied. The minimum ring space of 1.5μm width was fabricated successfully with the optimised photolithography process.

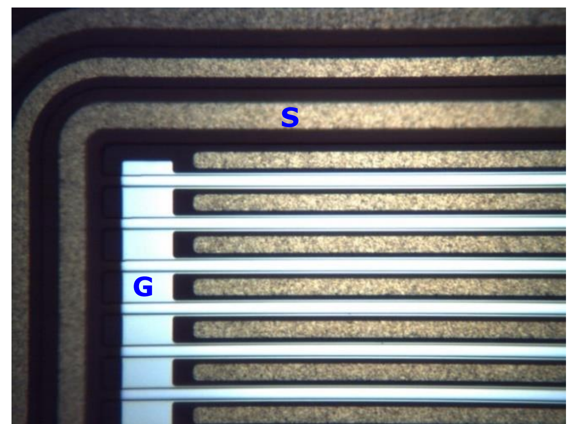


Fig. 5.19. 300nm molybdenum gate metal sputtered

The source metal was annealed at 1000°C for 2 minutes to form ohmic contact. Molybdenum (Mo) was used as the gate metal since polysilicon is not available in the cleanroom. Fig. 5.19 shows the image of the device after gate metal deposition. 2μm thick LPCVD SiO_2 was then deposited to passivate the surface and act as metal interlayer. The pad access window is opened as shown in Fig. 5.20 and the 2μm SiO_2 was etched away followed by 3μm aluminium deposition as pad metal. The top view of the finished 1.2kV trench MOSFET is presented in Fig. 5.21.

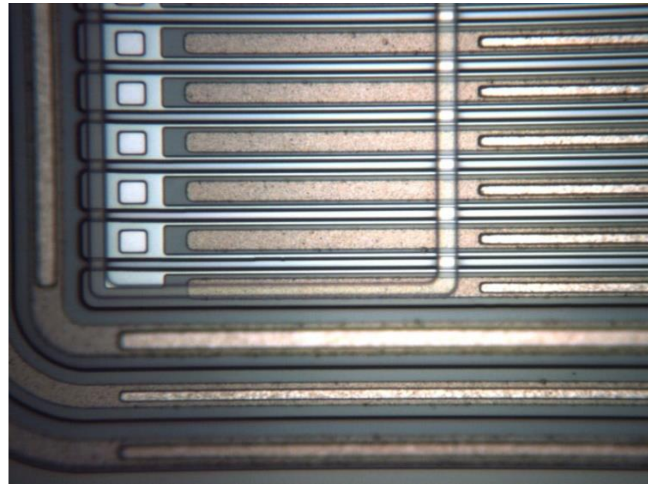


Fig. 5.20. Gate access opened for pad metal deposition

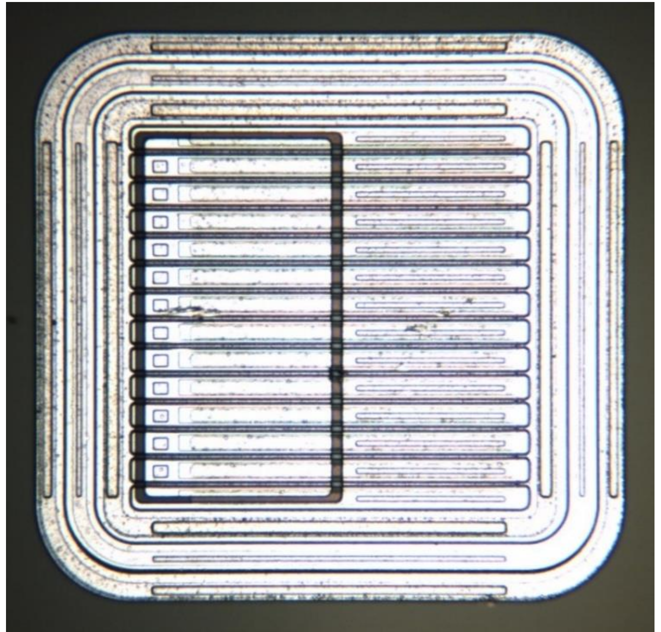


Fig. 5.21. The top view of the finished 1.2kV trench MOSFET

5.4. Device characterisation

This section presents the characterisation results of the 1st generation trench MOSFETs. The characterisation results of the TLM structure is shown in Fig. 5.22.

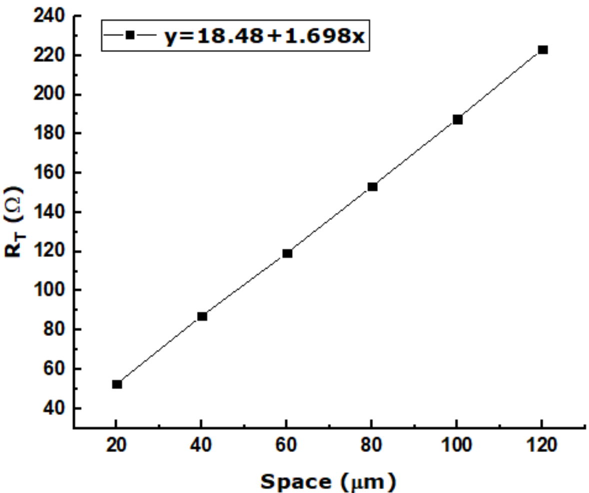


Fig. 5.22. The result of TLM structure on 1×10^{19}cm^{-3} n+ epi layer

The theory of the TLM structure was introduced in Chapter 2. The contact resistance can be extracted by extrapolating the plot in Fig. 5.22 until it intercepts the vertical axis. The contact resistance is therefore 9.24Ω. The transfer length L_T = 5.44μm can be extracted by extrapolating the plot until it intercepts the horizontal axis. Since the length of the pad is 120μm which is much larger than the transfer length, the contact resistivity of 1.2E-4Ωcm^2 is calculated using Eq. 2.2.

A contact resistivity of 1.2E-4Ωcm^2 is not as good as 1E-6Ωcm^2 reported in [6] for 4H-SiC n+ ohmic contact, however, this value is acceptable since contact resistivity is not the focus of this work. In future, this contact resistivity can be further reduced by optimising the annealing process and increasing the doping concentration of the n+ layer.

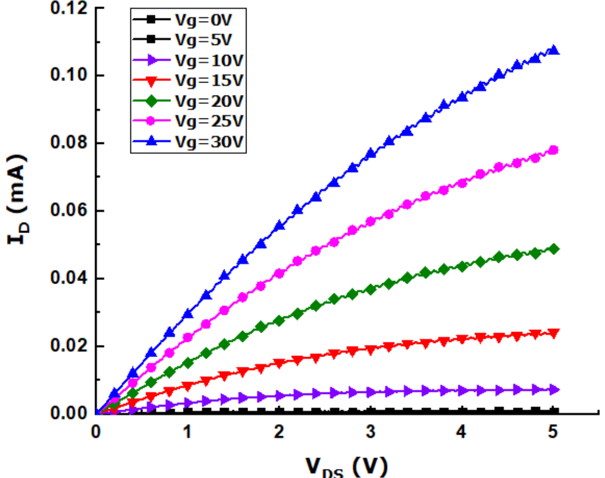


Fig. 5.23. The IV characteristics of the long channel MOSFETs

Lateral MOSFETs with long channel length (100μm) have also been fabricated on the same chip to verify the channel mobility. These test structures are very useful for fault analysis if the real devices do not work properly. Fig. 5.23 shows the on-state IV characteristics of the long channel MOSFETs. The transconductance curve is plotted in Fig. 5.24 which will be used to extract the channel mobility. Direct N_2O growth at 1300ºC was used as the thermal oxidation condition and the oxide thickness was determined to be 77nm by the ellipsometer.

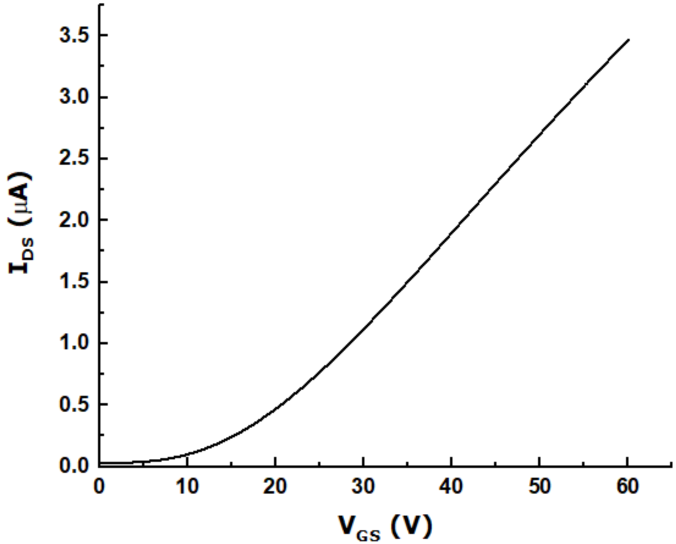


Fig. 5.24. The transconductance of the fabricated long channel MOSFET

The gate source voltage "V_{GS}" was applied up to 60V due to relatively thick gate oxide. The drain source voltage "V_{DS}" was set to be 0.1V as a constant to ensure a low electric field was applied across the device.

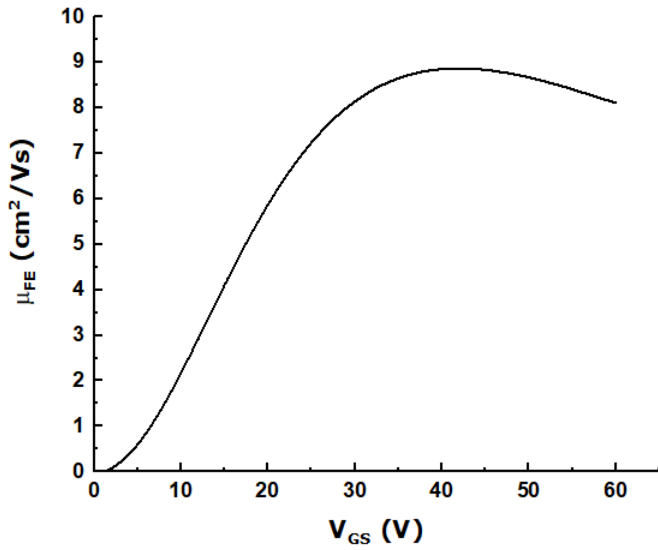


Fig. 5.25. The plot of field effect mobility against gate source voltage

The field effect mobility "μ_{FE}" can be extracted from the transconductance curve using Eq. 3.5. The channel length and width are 100µm and 200µm correspondingly. The gate source capacitance per unit area can be calculated since the oxide thickness is known as 77nm. The peak mobility of the long channel MOSFET is approximately 9 cm^2/Vs. The slightly lower mobility value compared to previous results can be due to the different material, doping and processes.

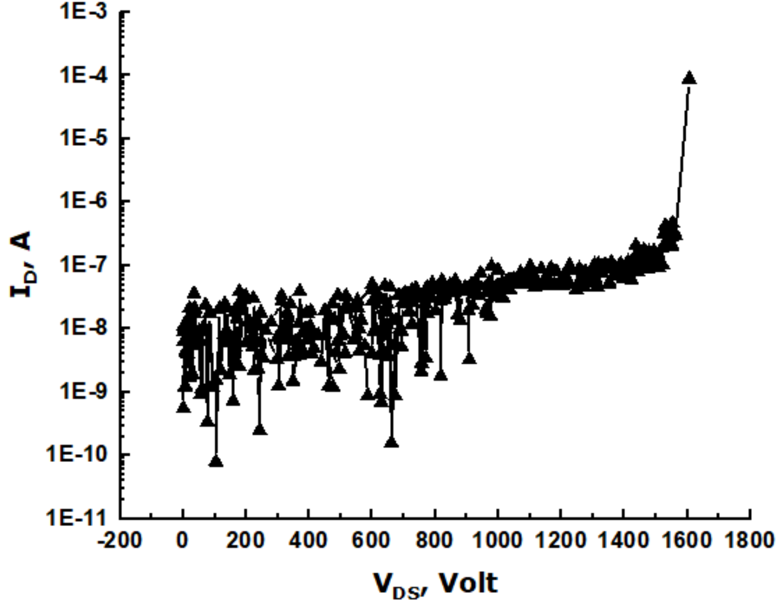


Fig. 5.26. The breakdown I-V curve of the 1.2kV trench MOSFET

The blocking capability of the trench MOSFETs has been characterised and the highest breakdown voltage is approximately 1600V where the design target (1200V) is achieved successfully. The edge termination design is therefore proved valid, though the yield is only 30%. Fig. 5.27 presents a more realistic view of the breakdown characteristics for this batch of trench MOSFETs.

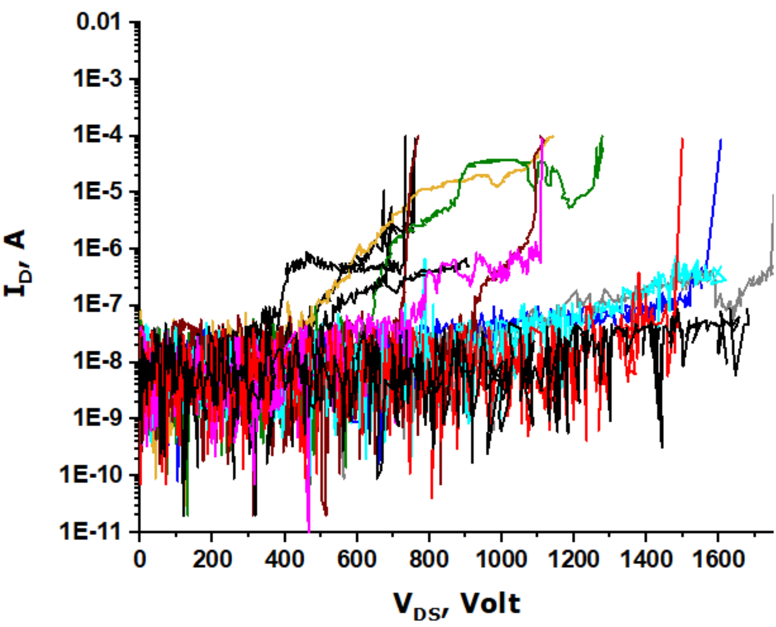


Fig. 5.27. The breakdown I-V curves for most of the trench MOSFET cells

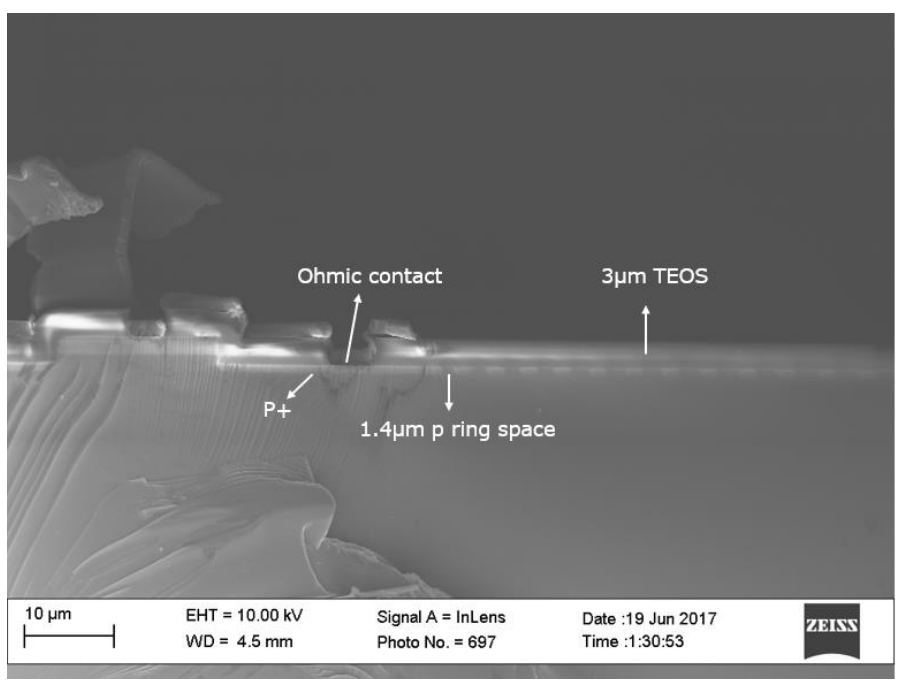


Fig. 5.28. SEM image focused on the edge termination region

The functioning devices have verified the edge termination design, the fact that the yield is relatively low should therefore result from the cleanroom processing problems. The early breakdown can be due to the many reasons like low passivation oxide quality, trench sidewall striation, non-perfect p-ring patterning during lithography processes, possible sharp trench corners and some other unknown issues.

Fig. 5.28 shows the cross section of the 1.2kV trench MOSFET focused specifically on the edge termination region. Since the conductivity of the p+ implanted regions are very different to the n- drift region, the p+ regions can be easily identified in the SEM image.

Some of the trench MOSFETs do not have the p+ trench bottom shielding region and the edge termination. The on-state characteristics of these devices are presented in Fig. 5.29. The current density is approximately 30A/cm^2 which is due to very large cell pitch of 24µm. The gate voltage is applied up to 80V since the gate oxide grown on the trench sidewall seems to be very thick. The oxide thickness on the planar surface was measured to be approximately 100nm, however, it was difficult to measure the oxide thickness on the trench sidewall.

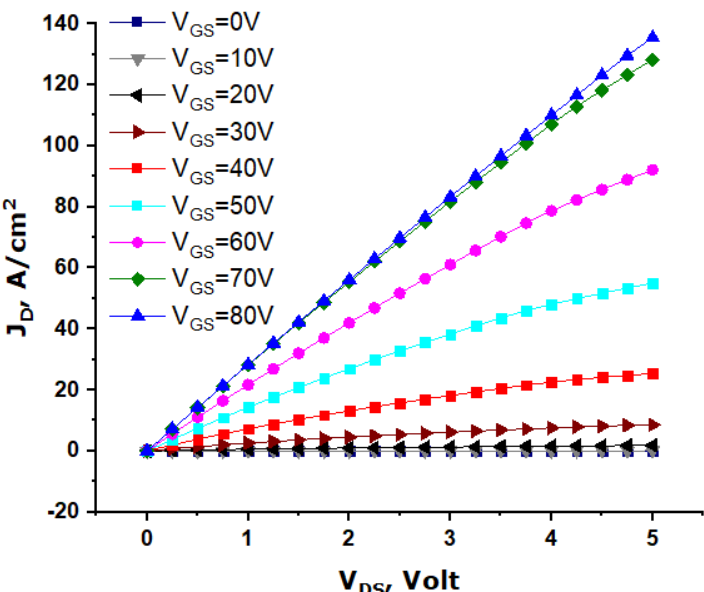


Fig. 5.29. The on-state IV characteristics of the trench MOSFET without trench bottom p+ shielding region and edge termination

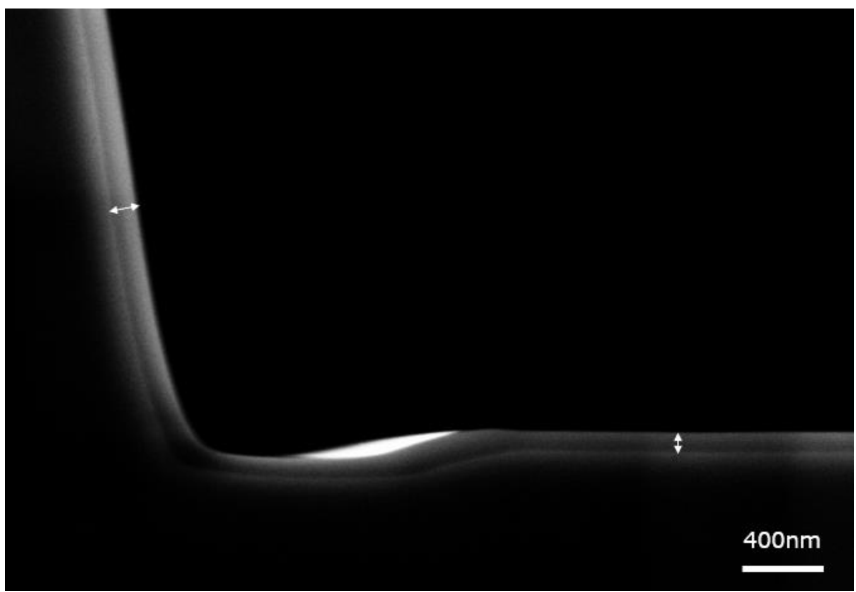


Fig. 5.30. The SEM image focused on the SiC/SiO₂ interface of the trench structure

From Fig. 5.30, one can identify that the oxide growth rate on the sidewall is much faster than the bottom of the trench structure, the sidewall oxide thickness can be estimated to be more than 130nm.

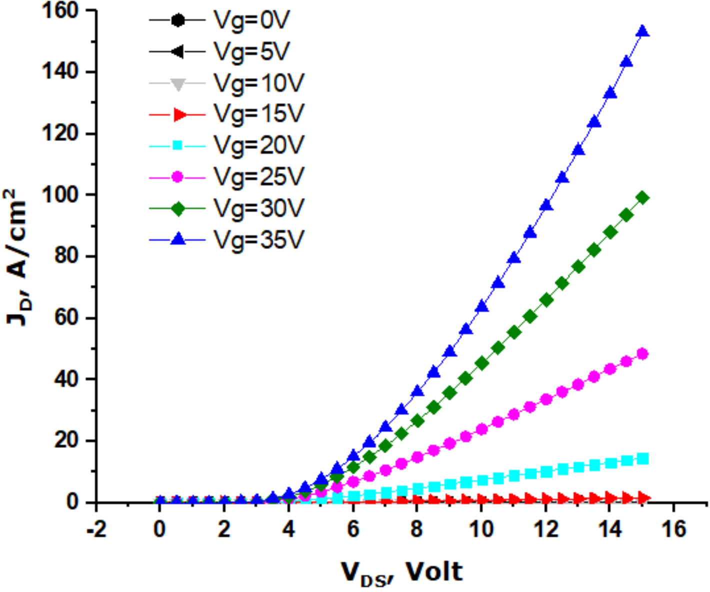


Fig. 5.31. The on-state IV characteristics of the trench MOSFET with trench bottom p+ shielding region

To reduce the oxide thickness on the sidewall, a combination of thermal growth and LPCVD deposition was used. The deposited oxide has similar thickness on the planar surface and the trench sidewall, therefore, a thin layer of oxide (<30nm) was thermally grown followed by 50nm LPCVD oxide deposition.

The I-V characteristic for the real 1.2kV trench MOSFET is shown in Fig. 5.31. The gate voltages are much lower compared to the devices fabricated earlier, however, the devices are highly resistive when the drain voltage is below 5V. It is not difficult to find out that the high resistance is in fact the JFET resistance introduced by the trench bottom p+ implantation. This parasitic JFET was considered in the design stage, and a 3μm deep gate trenches were fabricated aiming to minimise the parasitic JFET effect. The fact is that the experiment does not fit the simulation perfectly, therefore, a larger safe margin is necessary. In this specific case, it is believed that the p+ implantation may have entered the trench sidewall since the sidewall is not perfect 90 degree to the planar surface.

5.5. Discussion and Summary

The simulation models have been calibrated based on the experimental results for discussion. A fabricated lateral MOSFET with a channel length of 5μm and a single-finger trench MOSFET were used for the calibration. The Silvaco CVT model (inversion channel modelling) parameters and the D_{it} profile were modified to fit the experimental data.

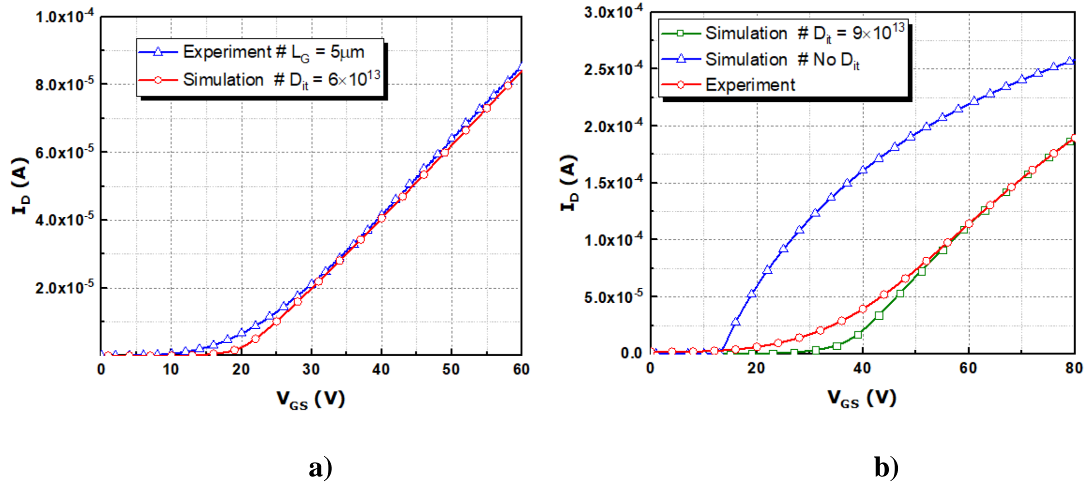
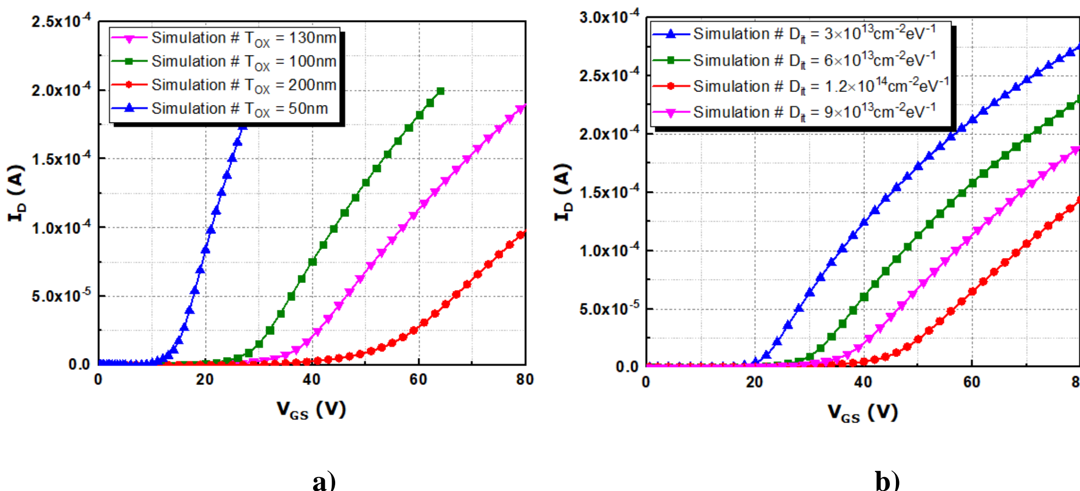


Fig. 5.32. The simulation calibration for a) a lateral MOSFET with 5μm channel length; b) a single-finger trench MOSFET without p+ shielding region

As shown in Fig. 5.32, the calibrated simulation results fit the experimental data relatively well except the data points around the threshold voltage which somehow indicates that the real device interface is more complicated and difficult to simulate with simple models.



a) b)

Fig. 5.33. The simulated transfer characteristics with the variation of a) gate oxide thickness; b) D_{it} profile

After the simulation model calibration, the gate oxide thickness "T_{OX}" and D_{it} have been varied to evaluate the effect to the transfer characteristics of the trench MOSFET. The threshold voltage is very sensitive to the oxide thickness as indicated in Fig. 5.33a. Since the trench sidewall oxide thickness was measured to be approximately 130nm by SEM, T_{OX} = 130nm is used as the reference condition. D_{it} level has a direct impact on the threshold voltage shift as shown in Fig. 5.33b, D_{it} peak value of $9\times10^{13}cm^{-2}eV^{-1}$ has been used as reference condition here. As a result, thin gate oxide on the trench sidewall and optimised oxide passivation techniques should be used to reduce the threshold voltage and improve the device performance. Nevertheless, it increases the risk of early gate oxide breakdown with reduce T_{OX} since the trench structure has not been fully optimised. The reduction of D_{it} also remains a challenge in the cleanroom.

This chapter has introduced the design, fabrication and characterisation processes for the 1st generation 1.2kV trench MOSFETs. TCAD silvaco is the main simulation tool used for the device design. Design parameters like the trench depth, floating field ring space and other dimensions can be determined by the simulation results. A high-resolution photolithography process (1~2μm) has been developed to address the fabrication issues encountered with the floating field rings. The edge termination design has been verified with a maximum breakdown of 1600V achieved for the fabricated trench MOSFETs. The parasitic JFET region, formed by the trench bottom p+ implanted region together with the p-base region, is believed to have degraded the on-state

performance. The JFET issue will be dealt with in the 2nd generation trench MOSFET design.

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Chapter 6 2nd generation trench MOSFET design and fabrication

The trench MOSFET fabrication work is continued in this chapter which focuses on the optimisation of the MOSFET on-state performance. The issue of the parasitic JFET is dealt with more carefully at the design stage. In addition, a fabrication trial on a Schottky contact embedded MOSFET structure has been carried out in order to achieve higher degree of integration.

6.1. TCAD Silvaco simulation

The wafer specification was modified compared to the 1st generation design. There is no n+ epilayer on the surface of the wafer, and therefore the source region has to be implanted. There is another higher doped n-type epilayer below the p-base region as a current spreading layer (CSL).

Figure 6.1. The wafer specification for the 2nd generation devices

The channel length for the 2nd generation devices was reduced to 0.5μm and the p-base doping was increased to $5\times10^{17}cm^{3}$ to reserve a safe margin for epitaxial growth.

6.1.1. Edge termination design

The edge termination structure remains the same as in the 1st generation devices since the design has already been validated. Floating ring space and width with a fixed value of 1.5μm is the best option in terms of chip area consumption and the complexity of the fabrication process. As a result, simulation of the termination region is necessary for the 2nd generation devices.

6.1.2. On-state optimisation

As described in Chapter 5, the implantation of a p+ trench bottom shielding region forms a parasitic JFET region which will severely degrade the on-state device performance. To solve this problem, an optimised structure is proposed as shown in Fig. 6.2b.

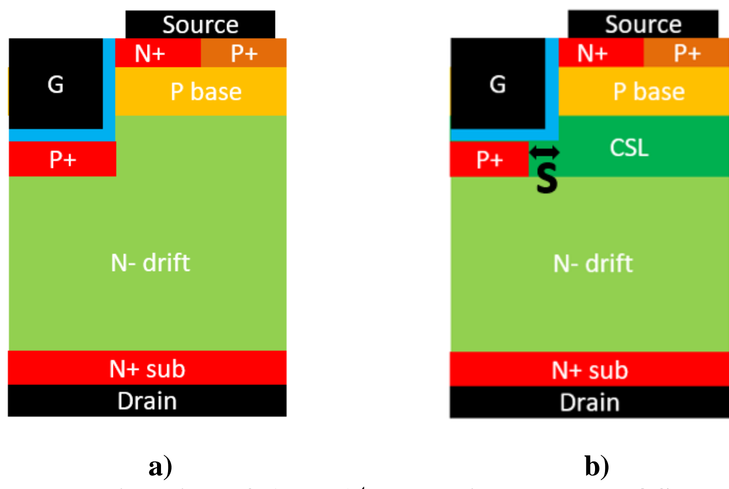


Fig. 6.2. The cross-section view of a) the 1st generation trench MOSFETs; b) proposed 2nd generation trench MOSFET

Adding the CSL layer is a common technique to improve on-state performance [1]. Besides, the alignment of the p+ shielding region to the gate trench can also have an impact on the device performance. The design optimisation process focuses on determining the CSL parameters and the p+ shielding region clearance "s" which is marked in Fig. 6.2b. The p+ shielding region implantation is normally done using a self-alignment process following the gate trench etching, however, trench sidewall can be mistakenly implanted as well if the sidewall is not perfectly 90 degrees and this will completely change the doping of the channel region. A large clearance "s" value will

improve the on-state performance at the cost of increased oxide electric field, therefore, there is a trade-off between the on-state and off-state performance.

Silvaco simulation has been carried out to determine the best design parameters for the 2nd generation trench MOSFETs. In the simulation, the clearance “s” was varied from 0 to 400nm and the CSL doping was varied between 4×10^{15}cm^{-3} to 1×10^{17}cm^{-3}. The on-state current density J_D at V_{GS} = 20V and V_{DS} = 1V was extracted as well as the oxide electric field at the trench bottom. The simulation results are shown in Fig. 6.3.

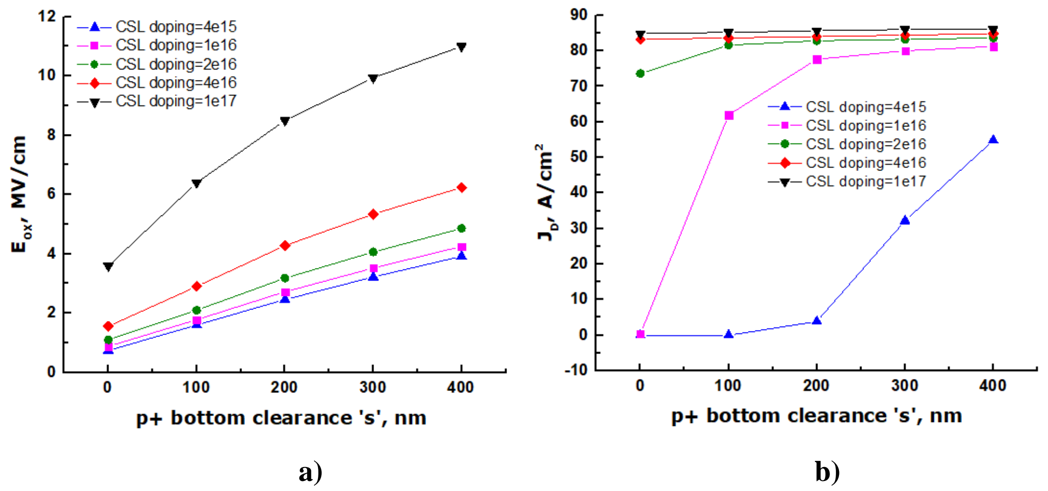


Fig. 6.3. The effect of p+ bottom clearance “s” and CSL doping on a) trench gate oxide electric field at 1200V reverse biased; b) current density at V_{GS} = 20V & V_{DS} = 1V

If the CSL doping concentration is kept the same with n- drift region (4×10^{15}cm^{-3}), very low on-state current density J_D can be observed in Fig. 6.3b). When the CSL doping is unnecessary high like 1×10^{17}cm^{-3}, the oxide electric field increases dramatically as shown in Fig. 6.3a). A CSL doping of 2×10^{16}cm^{-3} and 200nm p+ bottom clearance “s” seems to be a good trade-off between the on-state current density and the off-state oxide electric field. The 200nm p+ bottom clearance “s” can be achieved by depositing 200nm TEOS and then etch back.

6.1.3. Integration of Schottky contacts

Compared to the body diode in the MOSFET structure, Schottky diodes have a much lower turn on voltage and no reverse recovery charges, therefore external Schottky diodes are commonly used in parallel with MOSFETs to provide the current freewheeling path in many power electronic applications. A higher level of integration can be achieved if

the Schottky diode is embedded into the MOSFET structure. It reduces the total number of chips required in the system level, and it saves the chip area as well since the MOSFET and Schottky diode will share at least the edge termination region. Two types of integration are available where the first one is that the MOSFET and Schottky diode only share the termination region, and for the second type of integration, they share both the termination region and active region so that total chip area needed is minimized. In this chapter, only the first type of integration is included in the design for the fabrication trial.

6.2. Photo mask design

The mask design for the 2nd generation trench devices contains two separated mask sets for 1cm x 1cm chips and 2cm x 2cm chips respectively. The reason for using larger chips is to accommodate high current devices that have ~120 trench fingers. The cleanroom fabrication process is not like the commercial foundry, much lower yield is reasonable because of the amount of manual operations instead of automatic ones. It is challenging to fabricate large area devices; the device may not work properly if one finger/cell went wrong. In terms of the characterisation, higher current devices (>1A) are necessary to suppress the noise in the system especially for switching measurements. The active area of the big devices is 1mm x 1mm, the active area is actually small compared to commercial devices.

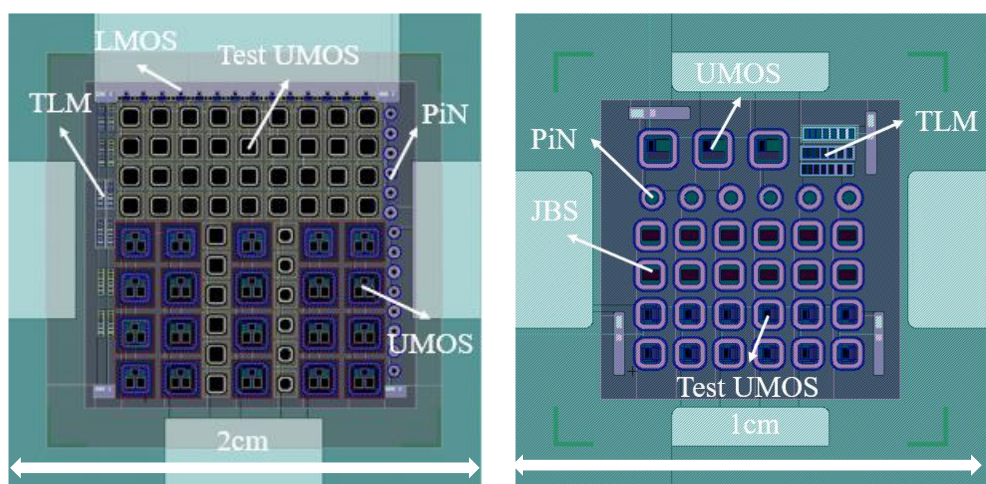


Fig. 6.4. Mask layout for the 2nd generation trench MOSFETs

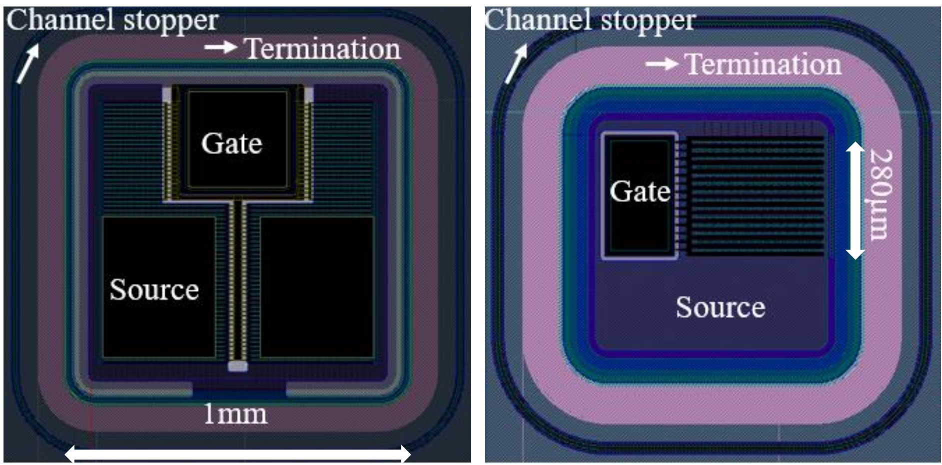


Fig. 6.5. Large and small device layout for 2nd generation trench MOSFETs

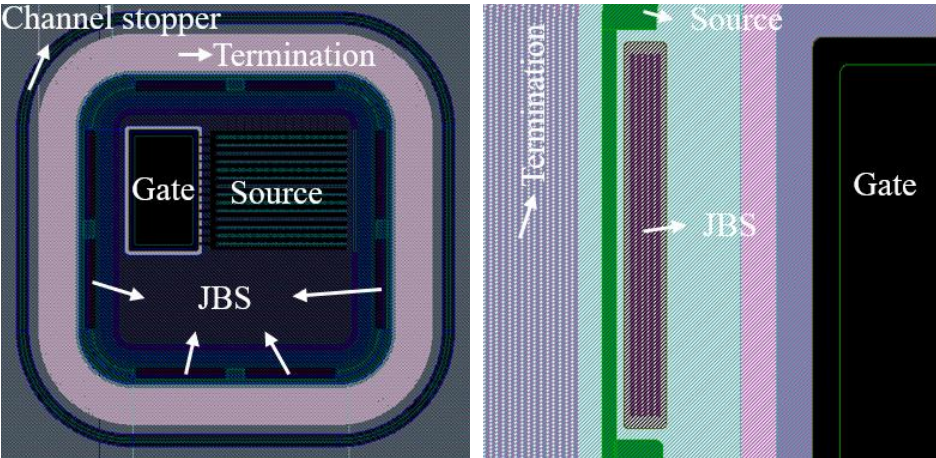


Fig. 6.6. Demonstration of integrated Schottky contacts in the edge termination region

The Schottky contact is embedded on the edge of the MOSFET active area and inside floating field ring termination so that the MOSFET and Schottky diode shares the same termination structure. The schematic of the MOSFET structure is included in the process flow as shown in Table 6.1. A PiN diode structure with integrated Schottky diode was studied in [2]. Similarly, simple junction barrier diode (JBS) structures are used as shown in Fig. 6.7. with “s” and “d” combination of 1.5μm and 2μm, 3μm and 3μm, 4μm and 3μm, and finally 5μm and 4μm. The p+ junction can be implanted together with the floating field rings, therefore, the JBS diode embedment does not increase implantation cost.

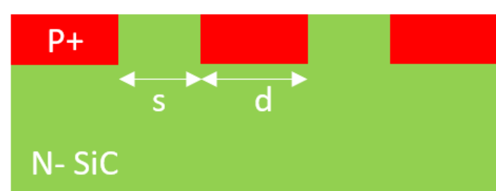
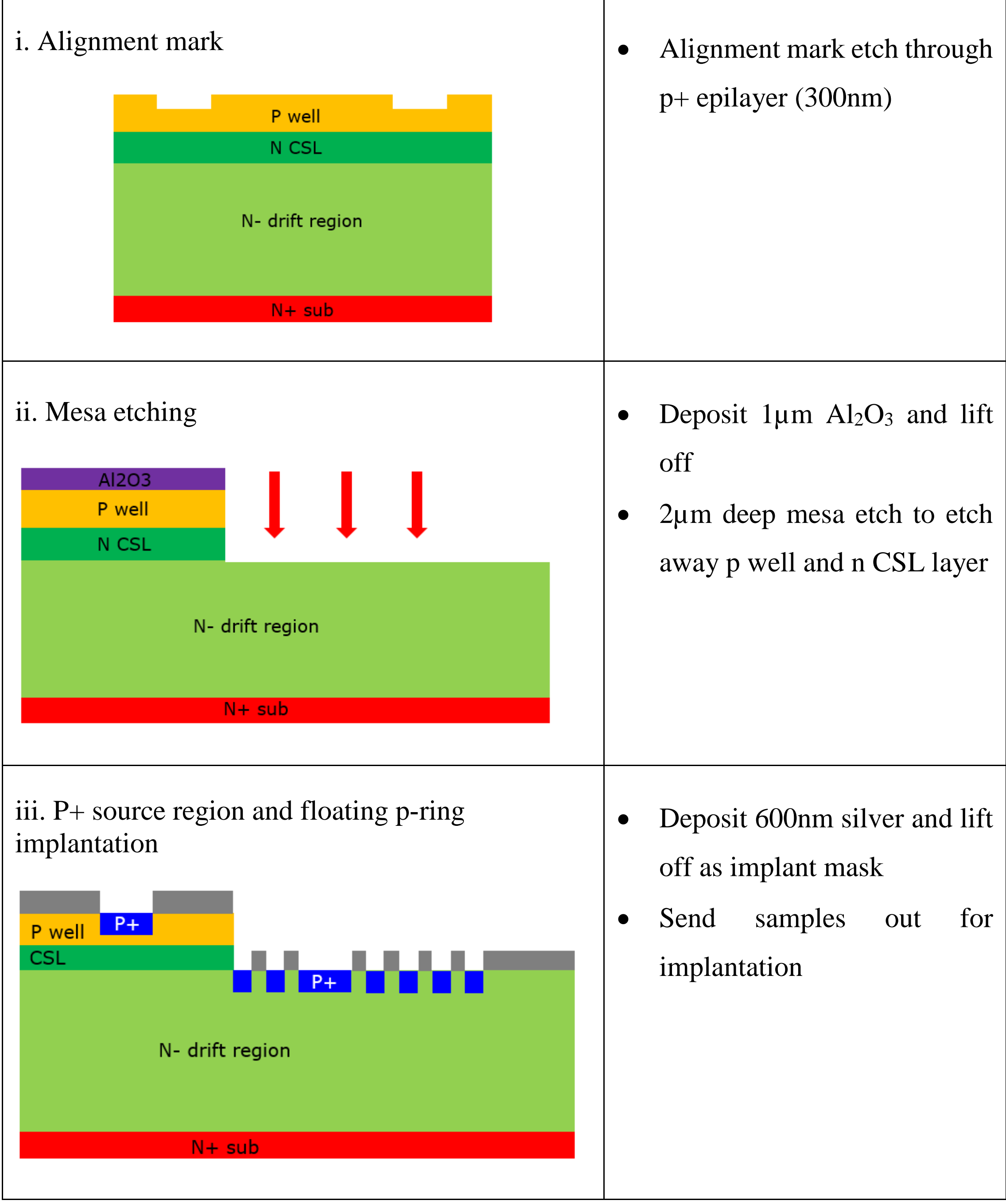


Fig. 6.7. JBS diode structure integrated in the MOSFET structure

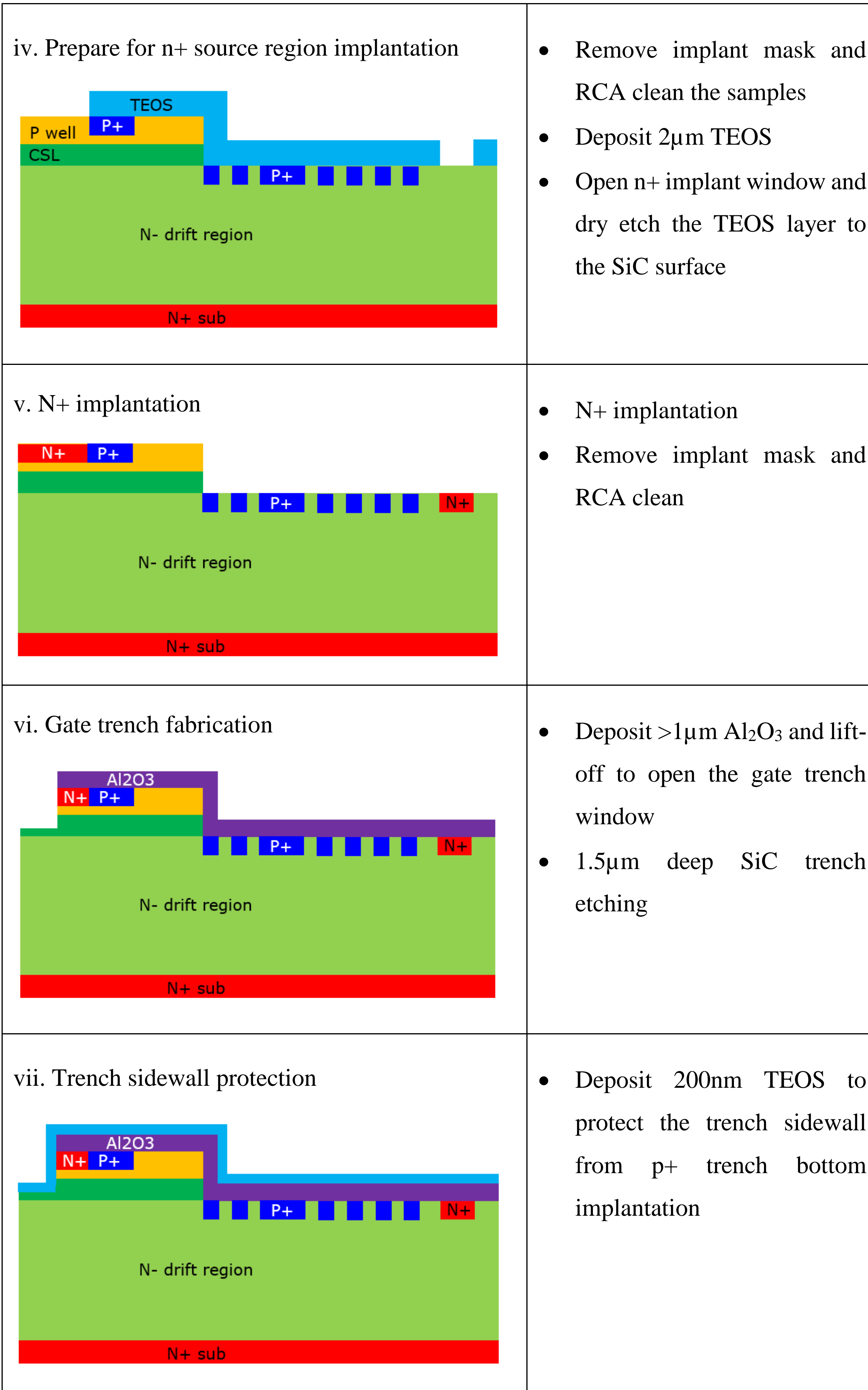
6.3. Device fabrication

The process flow for the 2nd generation devices is similar to those in the previous generation. The p-base epilayer doping is 5×10^{17}cm^{-3} with a thickness of 1μm and the n-CSL epilayer doping is 2×10^{16}cm^{-3} with a thickness of 0.8μm. Three implantations are needed in total which includes two Al implantations to form a p+ region and one N implantation to form an n+ region.

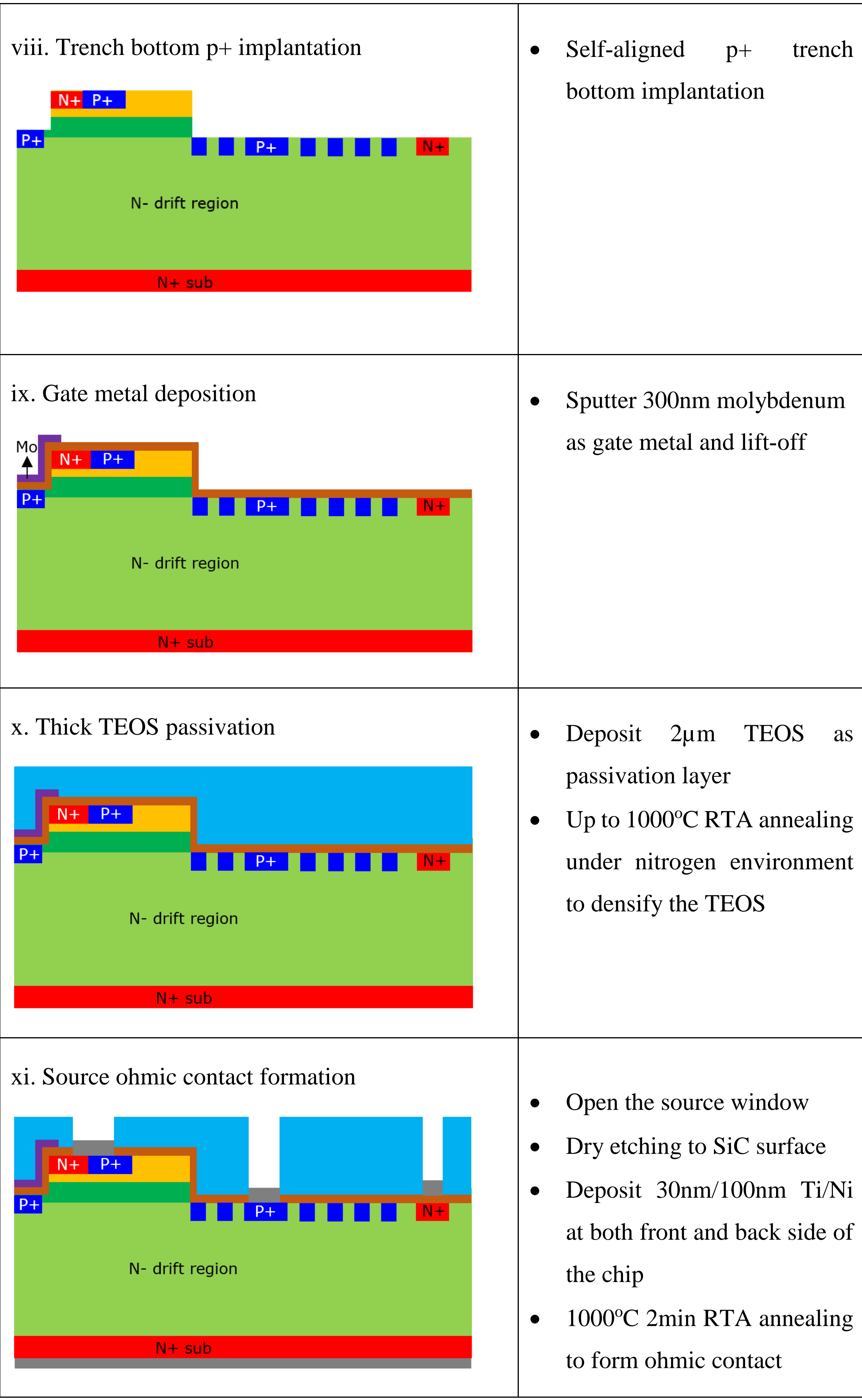
Table 6.1 The process flow for 1.2kV trench MOSFET



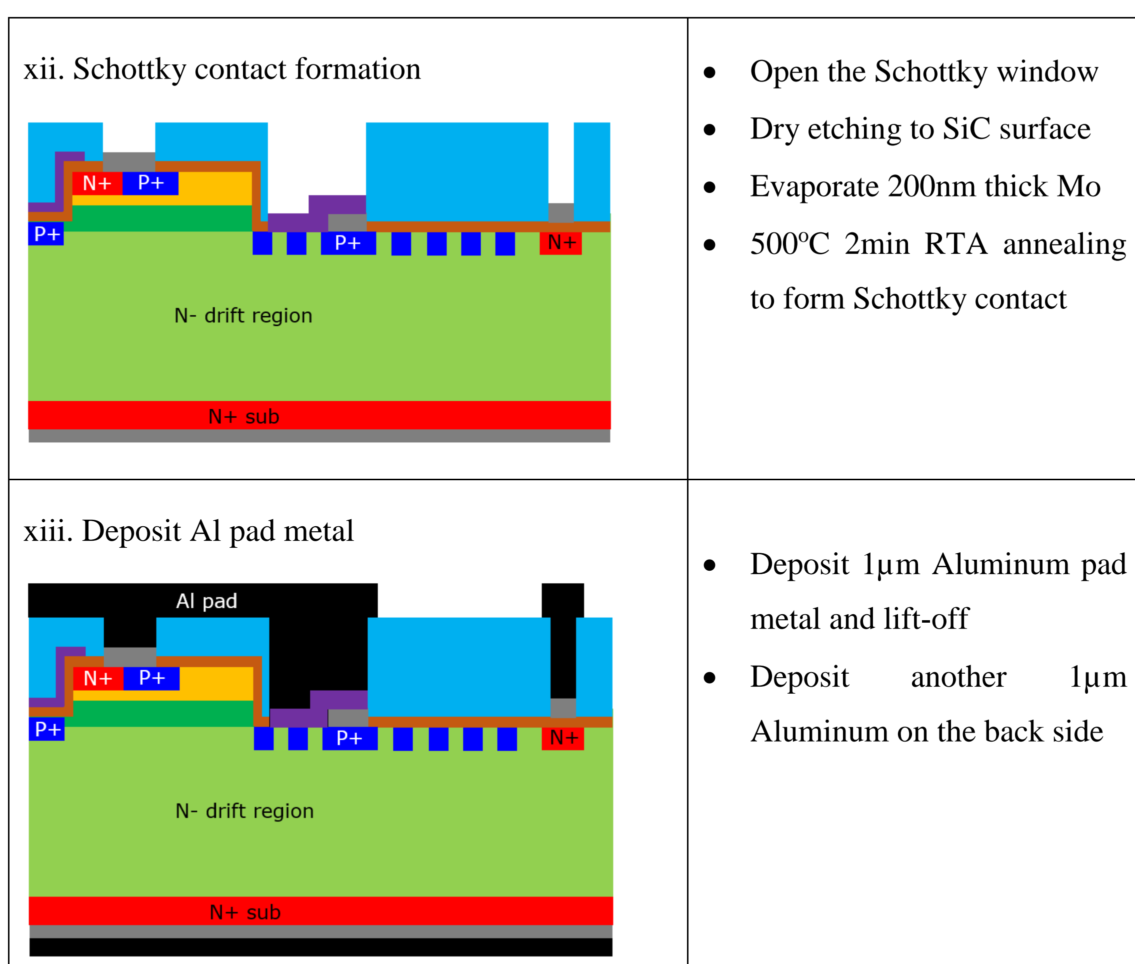
Step	Description
i. Alignment mark	• Alignment mark etch through p+ epilayer (300nm)
ii. Mesa etching	• Deposit 1μm Al_2O_3 and lift off • 2μm deep mesa etch to etch away p well and n CSL layer
iii. P+ source region and floating p-ring implantation	• Deposit 600nm silver and lift off as implant mask • Send samples out for implantation



Step	Process
iv. Prepare for n+ source region implantation	• Remove implant mask and RCA clean the samples • Deposit 2μm TEOS • Open n+ implant window and dry etch the TEOS layer to the SiC surface
v. N+ implantation	• N+ implantation • Remove implant mask and RCA clean
vi. Gate trench fabrication	• Deposit >1μm Al_2O_3 and lift-off to open the gate trench window • 1.5μm deep SiC trench etching
vii. Trench sidewall protection	• Deposit 200nm TEOS to protect the trench sidewall from p+ trench bottom implantation



Process step	Description
viii. Trench bottom p+ implantation	• Self-aligned p+ trench bottom implantation
ix. Gate metal deposition	• Sputter 300nm molybdenum as gate metal and lift-off
x. Thick TEOS passivation	• Deposit 2μm TEOS as passivation layer • Up to 1000°C RTA annealing under nitrogen environment to densify the TEOS
xi. Source ohmic contact formation	• Open the source window • Dry etching to SiC surface • Deposit 30nm/100nm Ti/Ni at both front and back side of the chip • 1000°C 2min RTA annealing to form ohmic contact



Process step	Description
xii. Schottky contact formation P+ / N+ / P+ / P+ / N+ / N- drift region / N+ sub	• Open the Schottky window • Dry etching to SiC surface • Evaporate 200nm thick Mo • 500ºC 2min RTA annealing to form Schottky contact
xiii. Deposit Al pad metal Al pad / N+ / P+ / P+ / P+ / N+ / N- drift region / N+ sub	• Deposit 1µm Aluminum pad metal and lift-off • Deposit another 1µm Aluminum on the back side

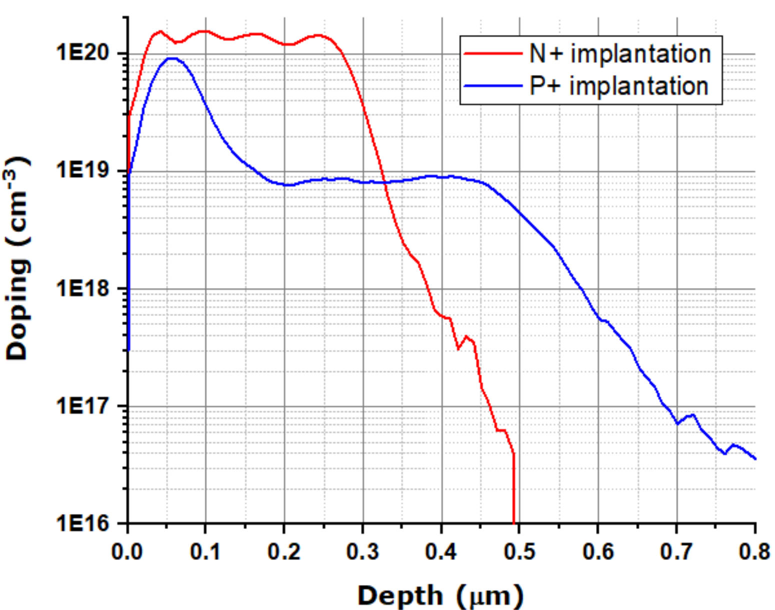


Fig. 6.8. N+ and P+ implantation profile simulated by Silvaco TCAD

The implantation profile is simulated using Silvaco TCAD and the result is presented in Fig. 6.8. A box profile with $1\times10^{20}cm^{-3}$ doping concentration has been designed for n+ source region, the p+ doping concentration is one order of magnitude less except for the region closer to the surface which is necessary for the formation of the ohmic contact. The implantation energy and dose specifications are shown in Table 6.2.

Table 6.2. Implantation specification

P+ (Aluminium) implantation		N+ (Nitrogen) implantation	
Energy (keV)	Dose (cm^{-2})	Energy (keV)	Dose (cm^{-2})
50	6×10^{14}	20	5×10^{14}
100	1×10^{14}	50	8×10^{14}
200	1×10^{14}	90	1×10^{15}
350	2×10^{14}	150	1.5×10^{15}

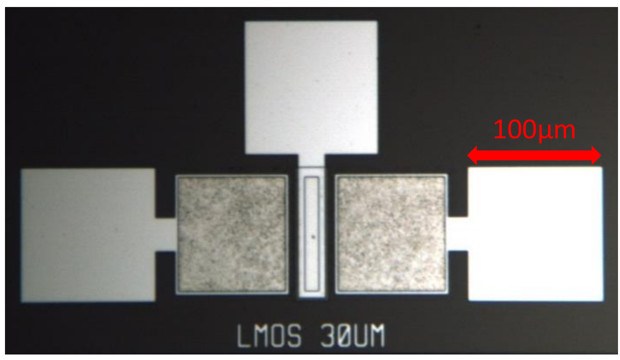
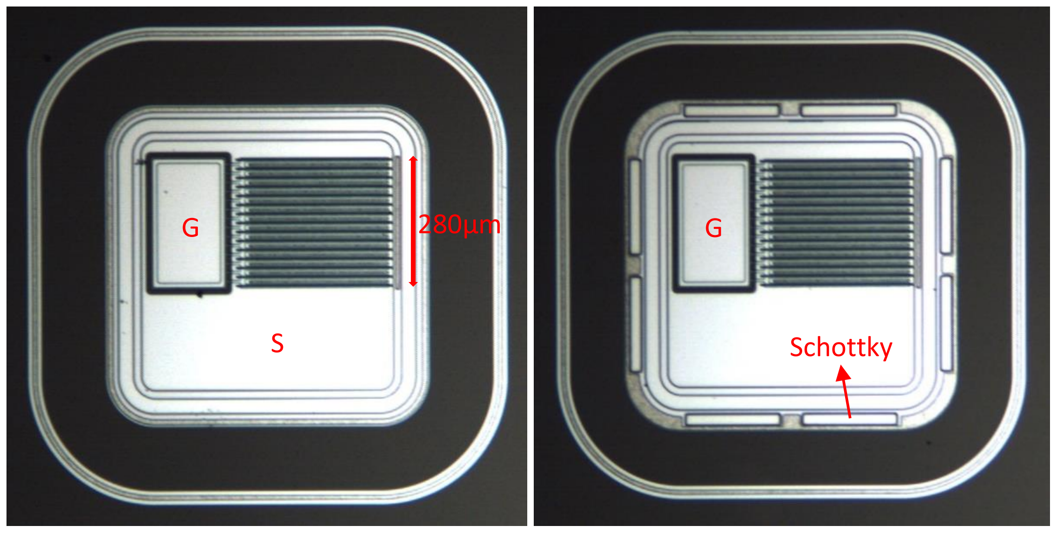


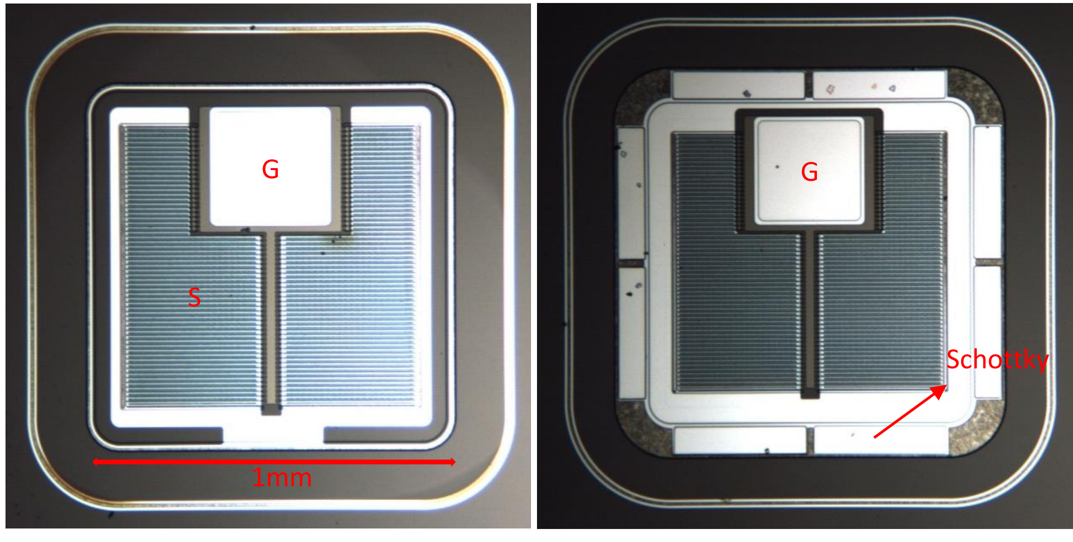
Fig. 6.9. Lateral MOSFET structure on 2cm x 2cm chips

Like the devices fabricated in the previous generation, a lateral MOSFET structure is used to extract the channel mobility. The lateral MOSFETs are only available on the 2cm x 2cm chips which later proves to be a mistake. As a useful test structure, lateral MOSFETs should be placed on every single chip. A lateral MOSFET provides information about the channel mobility on the planar surface, however, it will be very useful for fault analysis if trench MOSFETs do not work properly. An image of fabricated lateral MOSFET is shown in Fig. 6.9.



a) b)

Fig. 6.10. Fabricated trench MOSFET with 15 fingers a) without integrated Schottky contacts; b) with integrated Schottky contacts



a) b)

Fig. 6.11. Fabricated trench MOSFETs with 120 fingers a) without integrated Schottky contacts; b) with integrated Schottky contacts

Fig. 6.10 presents the image of fabricated trench MOSFETs with 15 trench fingers, these 15-finger devices are more like test devices to demonstrate the idea. Fig. 6.11 shows the relatively higher current devices with active area of 1mm x 1mm which is the largest MOSFET device ever made in this cleanroom. It is more difficult and very risky to process devices with large active area with all the manual or semi-automatic operations compared to the more automatic fabrication processes in industry.

6.4. Device characterisation

This section presents the characterisation results of the 2nd generation trench MOSFETs. Two main test structures are the TLM structures and long channel MOSFETs.

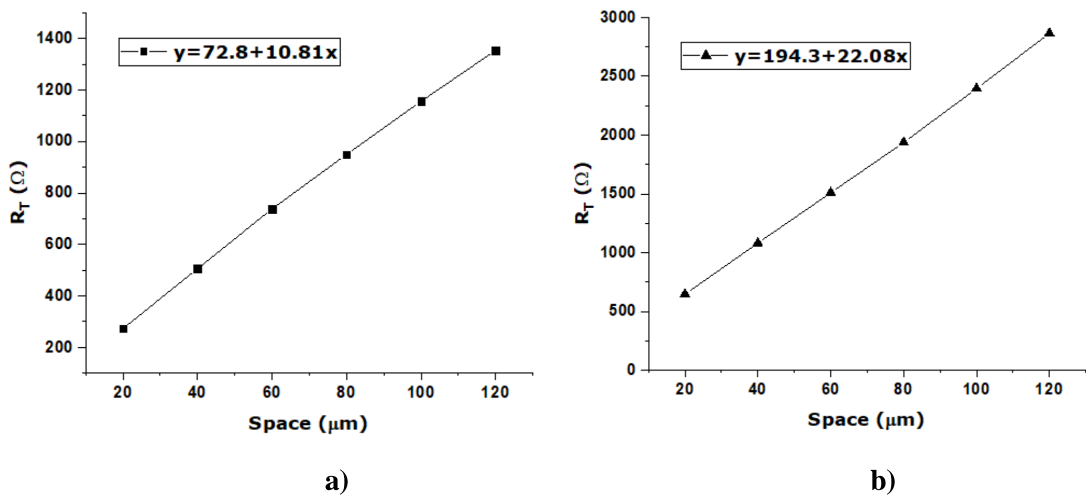


Fig. 6.12. TLM results on the implanted n+ layer of the a) 1cm x 1cm chip; b) 2cm x 2cm chip

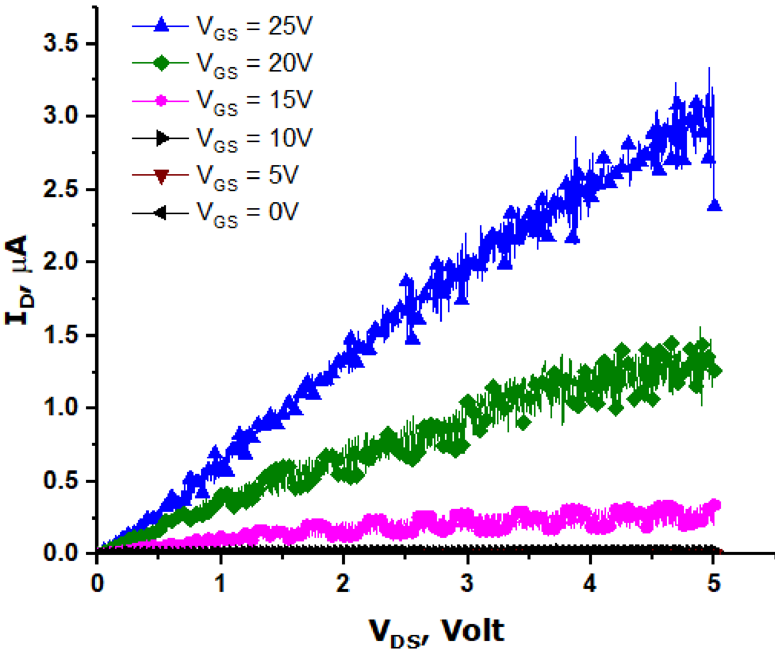


Fig. 6.13. The IV characteristics of the lateral MOSFET with channel length of 100μm

The TLM plot is shown in Fig. 6.12. A contact resistivity of 3E-4Ωcm^{-2} can be extracted for 1cm x 1cm chip using the same method as the 1st generation devices. Surprisingly, the contact resistivity for the 2cm x 2cm chip is 1E-3Ωcm^{-2} which is approximately three times of the contact resistivity for the 1cm x 1cm chip. Both samples were processed in the same time with the same conditions, therefore, it is difficult to explain the difference.

Lateral MOSFETs with 100µm channel length were fabricated on the 2cm x 2cm chip and the IV characteristic is shown in Fig. 6.13. The transconductance curve is extremely noisy and therefore it is not shown in this thesis as it cannot provide any useful information. As a result, the field effect mobility cannot be extracted from the lateral MOSFETs fabricated. The drain current measured at 1V drain voltage is approximately 50 times smaller compared to the measurement results of the 1st generation devices. It is worth to mention that the p-base doping for this generation is 5×10^{17}cm^{-3} instead of 1×10^{17}cm^{-3} used for the 1st generation devices, moreover, the channel length for current generation is 0.5~0.7µm compared to 1.4µm for the 1st generation devices.

The blocking capability of the trench MOSFETs were characterised only up to 200V due to limitation of the equipment. The 1st generation devices were sent to University of Electronic Science and Technology of China for breakdown characterisation. New high voltage probe station has been bought in the cleanroom, and once everything has been set up correctly the breakdown characterisation will be done on site up to the breakdown voltage.

The on-state characterisation results of 15-finger and 120-finger trench MOSFETs on the 2cm x 2cm chip are shown in Fig. 6.14 and Fig. 6.15. The current density is incredibly low which is approximately three order of magnitude lower than the first-generation devices. The low current issue seems to be consistent for the fabricated lateral MOSFETs, 15-finger and 120-finger trench MOSFETs on the 2cm x 2cm chip.

The IV characteristics for the 15-finger trench MOSFETs on the 1cm x 1cm chip exhibits a completely different result compared to the 2cm x 2cm chip. As shown in Fig. 6.16, the on-state IV characteristic is as expected and the parasitic JFET effect has been eliminated with the optimised design. The current density is only ≈3A/cm^2 which is still relatively low value, however, it is due to the higher p-base doping density (5×10^{17}cm^{-3}),

large cell pitch (20μm), high threshold voltage and low channel mobility limited by the equipment.

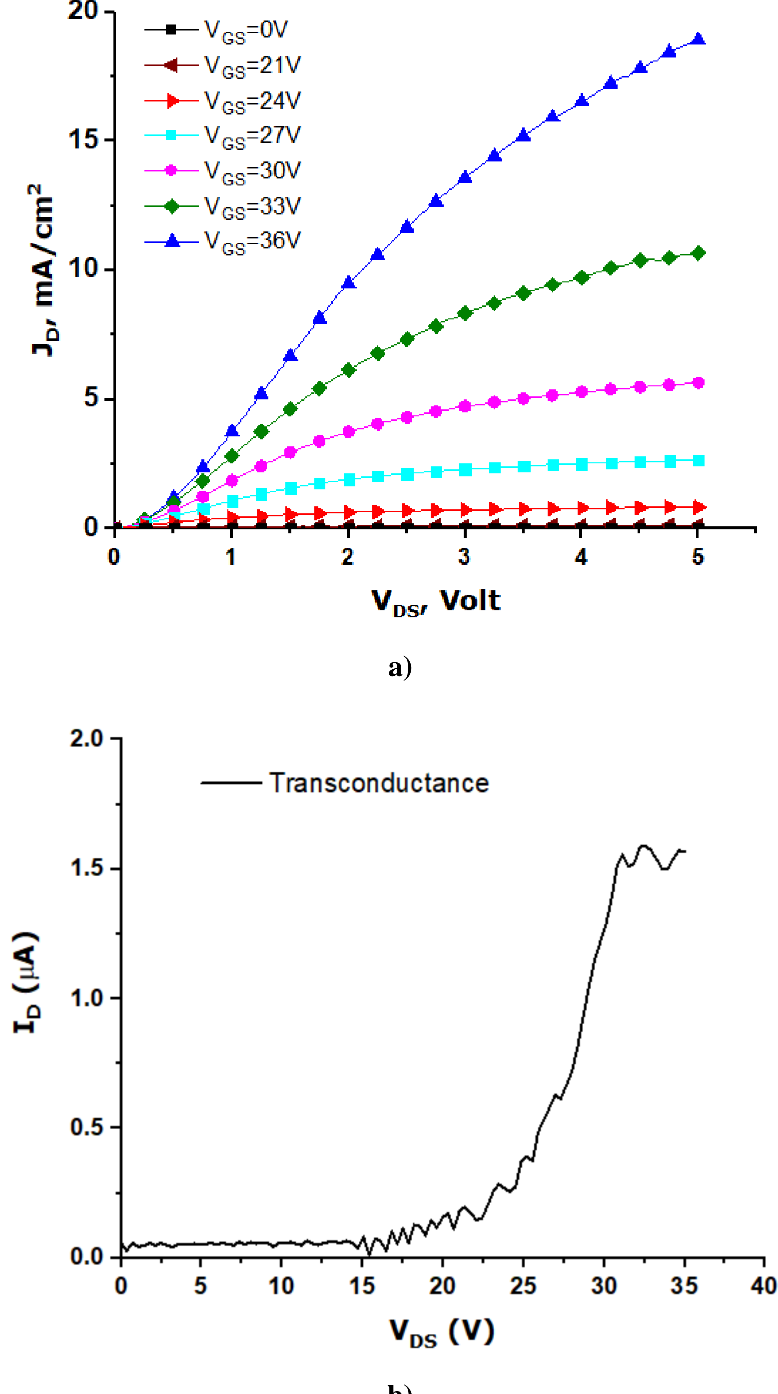


Fig. 6.14. The on-state characteristics of the 120-finger trench MOSFET device on the 2cm×2cm chip a) IV characteristics; b) Transconductance curve

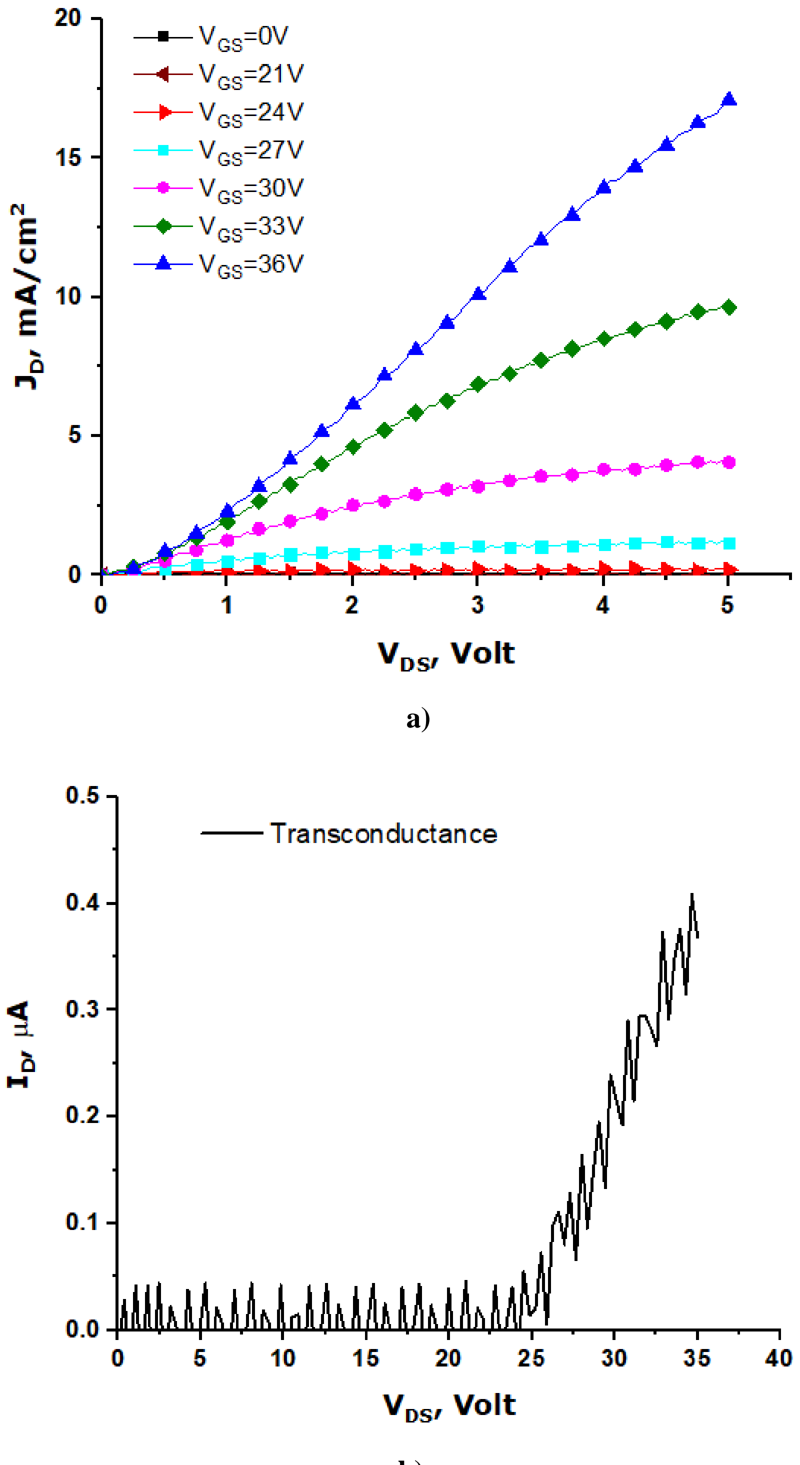


Fig. 6.15. The on-state characteristics of the 15-finger trench MOSFET device on the 2cm×2cm chip a) IV characteristics; b) Transconductance curve

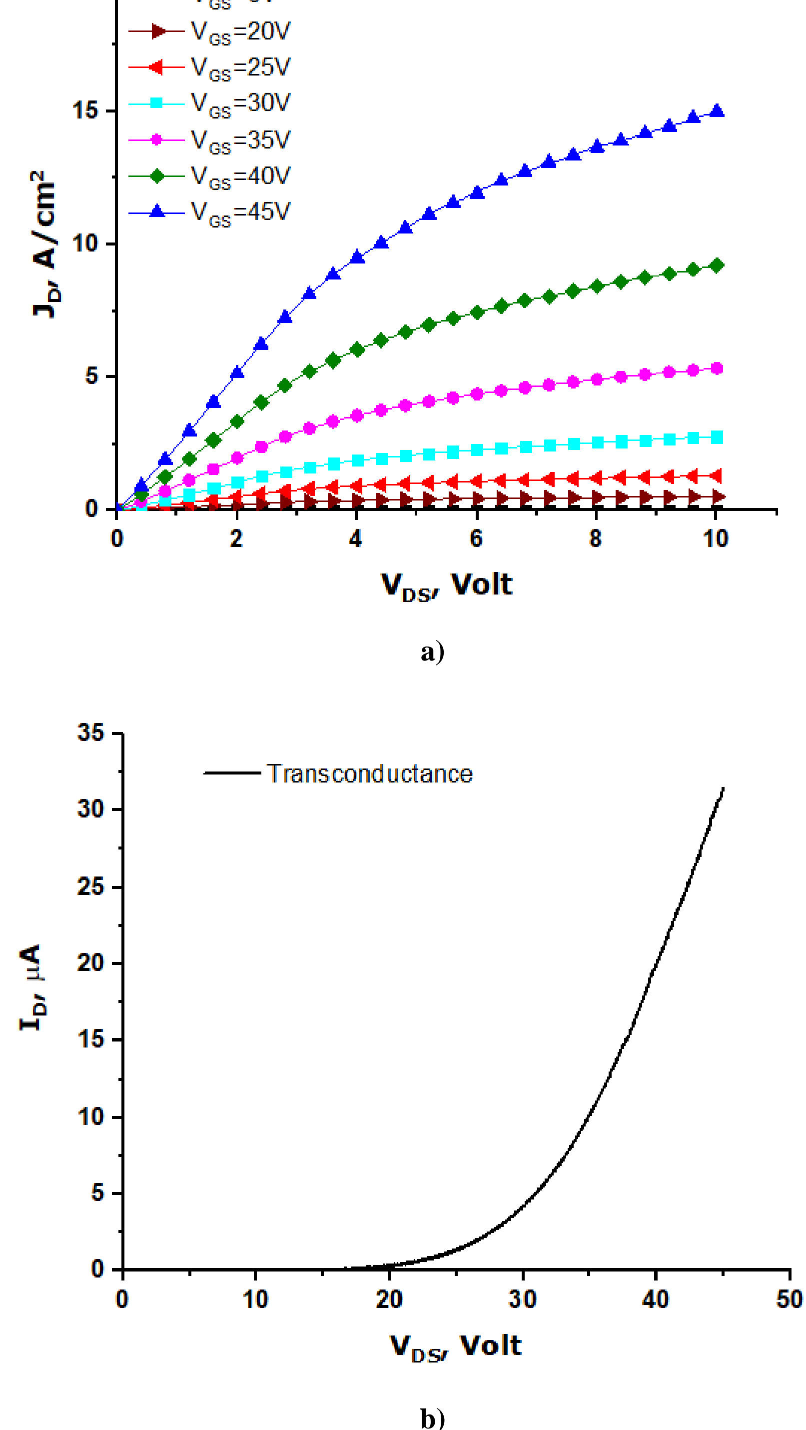


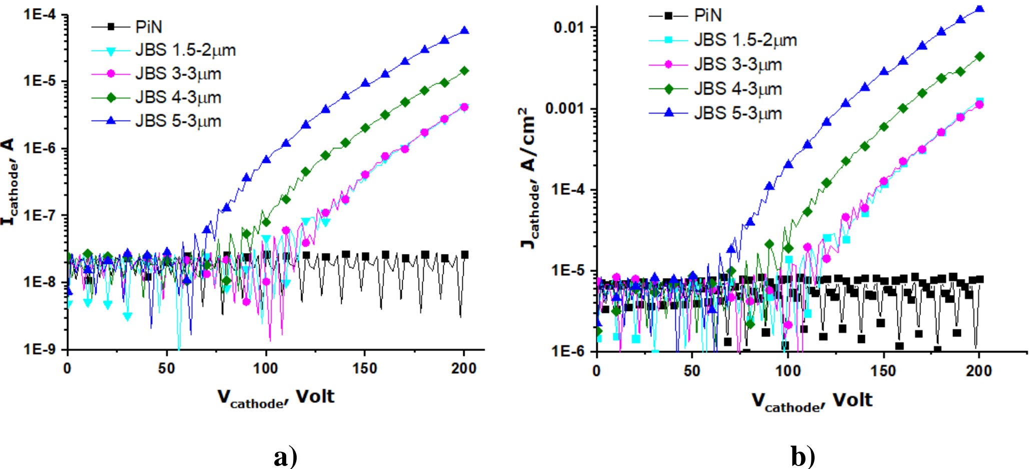
Fig. 6.16. The on-state characteristics of the 15-finger trench MOSFET device on the 1cm×1cm chip a) IV characteristics; b) Transconductance curve

As mentioned previously, the lateral MOSFETs have experienced the similar low current issue with the trench MOSFET devices on the 2cm×2cm chip, therefore only the implantation and oxidation process can be responsible for the low current issue. Since both the 1cm×1cm and 2cm×2cm chips were oxidized at the same time, the oxidation

process can be ruled out as the 15-finger trench MOSFET on 1cm x 1cm are working properly. In this case, the implantation process for the 2cm x 2cm chip may be responsible for the low current issue and the TLM results shown in Fig. 6.12 may provide some evidence for this but the detailed explanation is still not available.

The main target for the second-generation device design was to solve the parasitic JFET problem raised in the first-generation devices. This target has been achieved successfully based on the on-state performance of the 15-finger devices demonstrated in Fig. 6.16. Cleanroom process optimisation is still needed to keep consistency between different samples and different batches of devices.

Although the MOSFETs on the 2cm x 2cm chip do not work properly, the Schottky diode embedded near the termination region works fine. The off-state characteristics of the JBS and PiN diodes are shown in Fig. 6.17. The active area for the JBS diodes is $3.2\times10^{-3}cm^2$ for all the design splits. The leakage current level in this work is similar to the work published by Lin Zhu in [3].



a) **b)**

Fig. 6.17. The off-state characteristics of integrated JBS diodes and PiN body diode on 120-finger trench MOSFETs a) for leakage current; b) for leakage current density

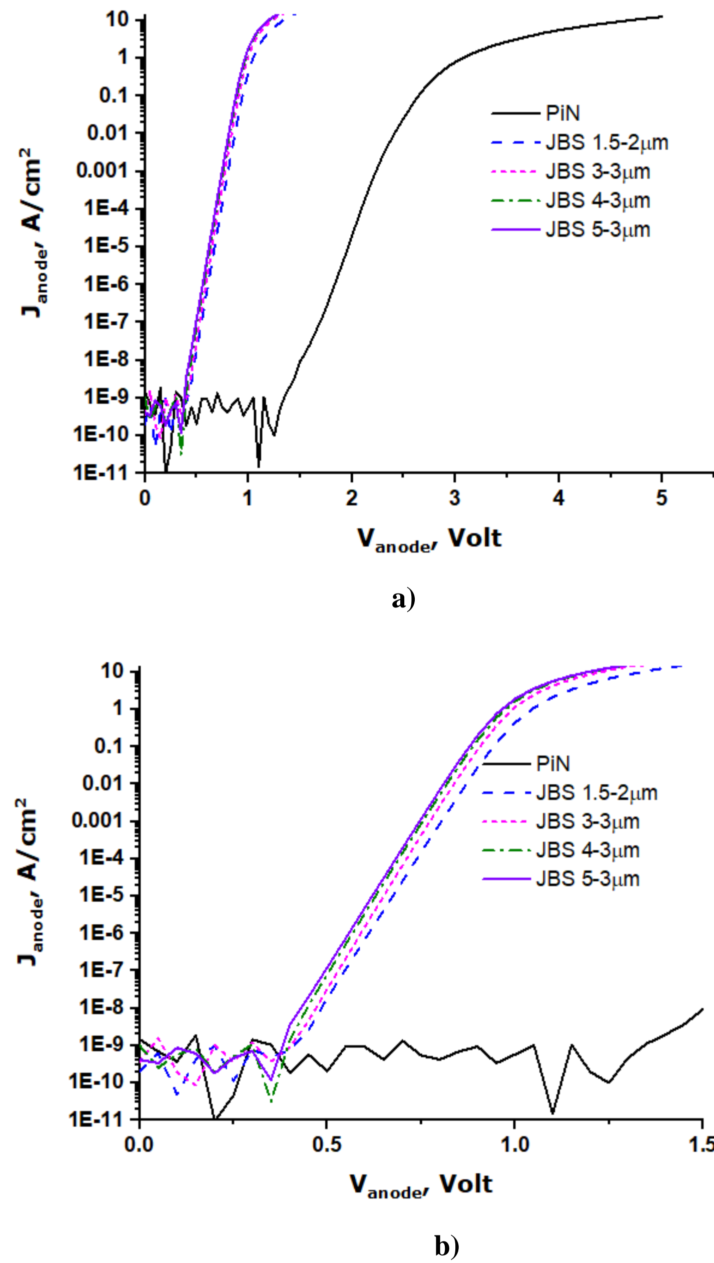


Fig. 6.18. The turn-on characteristic of integrated JBS diodes and PiN body diode

The turn-on characteristics of the embedded JBS diodes and the body PiN diode are shown in Fig. 6.18. For a proper design, the on-state and off-state performance of embedded Schottky diode must match the MOSFET itself. It is a waste of chip area if the Schottky diode is too large, and if the chip area allocated to Schottky diode is too small, the body diode will be activated and the Schottky diode embedment becomes useless.

5.5. Summary

The 2nd generation device was designed to mitigate the parasitic JFET effect and hence improve the on-state performance of the trench devices. A CSL layer and the p+ implantation clearance “s” were introduced to the 2nd generation devices. and a trade-off decision (CSL doping at $2\times10^{16}cm^{-3}$ and “s” = 200nm) was made based on the simulation results. The design target has been achieved and the parasitic JFET induced high turn-on voltage has been eliminated successfully as shown in Fig. 6.16. There is still a process issue since all the devices fabricated on the 2cm×2cm chip including lateral MOSFETs have experienced extremely low current density. It is believed that there might be some mistakes during the implantation step which should be responsible for the low current issue on the 2cm×2cm chip, however, a detailed explanation is still not available.

As a result, further process optimisation is necessary to keep consistency between different batches of samples. There is another key feature in the 2nd generation design which is the integration of the Schottky contact in the edge termination region. With an embedded Schottky contact, the total chip area consumption is reduced compared to externally connected Schottky diode and it also reduces the total chip count in a system level. The fabricated device is only for the demonstration of the concept, further optimisation of the Schottky diode is necessary to reduce the leakage current without sacrificing the on-state performance. The device rating for the MOSFET and the embedded Schottky diode must match perfectly for the optimum performance.

References

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[2] H. Niwa, J. Suda and T. Kimoto, "Ultrahigh-Voltage SiC MPS Diodes with Hybrid Unipolar/Bipolar Operation," in *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 874-881, March 2017

[3] Lin Zhu, T. P. Chow, K. A. Jones and A. Agarwal, "Design, fabrication, and characterization of low forward drop, low leakage, 1-kV 4H-SiC JBS rectifiers," in *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 363-368, Feb. 2006.

Chapter 7 10kV 4H-SiC DMOSFET design and fabrication

The competition between SiC MOSFET and Si IGBT/superjunction MOSFETs at relatively lower voltages may last for a long time depending on how rapidly SiC technology progresses in terms of better performance, cost reduction and reliability. The advantage of SiC devices at higher voltages (>10kV) is more noticeable since Si devices are limited up to 8kV [1]. At 10kV or higher voltages, SiC MOSFET has the potential to bring the revolution for the next generation high power systems. This chapter introduces the design and fabrication processes of the 10kV 4H-SiC DMOSFET.

7.1. Background

In recent years, SiC devices rated at more than 10kV have been fabricated and tested in real power electronics systems. Cree (now Wolfspeed) demonstrated their 10kV/20A SiC MOSFETs with higher power handling capability and switching frequency compared to 6.5kV Si IGBTs [2]. Avalanche ruggedness of a 10kV SiC MOSFET was studied by Ashish [3] with unclamped inductive switching circuit. The advanced liquid cooling system was designed specifically for power modules with 10kV SiC MOSFETs [4]. Power converter prototypes were built based on 10kV SiC MOSFET [5,6]. All these exciting researches were driven by the potential of high voltage power devices enabled by silicon carbide.

7.2. Device design

The device design has been separated into two parts which includes the edge termination design and the on-state optimisation. The n- drift region needs to be 100µm thick for a blocking voltage of more than 10kV. For such a thick epilayer, usually epilayer growth companies cannot guarantee the doping concentration, therefore, device design

normally starts after receiving the ordered wafer so that the actual doping density can be confirmed. In this work, the epilayer doping concentration is $3.5\times10^{14}cm^{-3}$.

Equation 7.1 below was approximated with experimental data and it describes the relationship between the critical field and the doping concentration of the drift region [7].

$$E_{cr} = \frac{2.49\times10^6}{1-0.25\,log_{10}(N/10^{16})}\ V/cm \tag{7.1}$$

A critical field of 1.83MV/cm can be calculated from this equation. The theoretical blocking voltage can be calculated with Equation 7.2 [8] for punch through structures.

$$BV = E_{cr}W - \frac{qN_DW^2}{2\varepsilon_s} \tag{7.2}$$

The theoretic breakdown voltage is approximately 15kV using the critical field value calculated from Equation 7.1.

7.2.1. Edge termination

7.2.1.1. Floating field rings termination

Efficiency, reliability and cost are the most important criteria for the evaluation of the edge termination structures. For the 1.2kV trench MOSFETs, FFR termination is no doubt the better option compared to JTEs. The advantage is however questionable for 10kV devices. FFR termination may consume a large device area in this case since the drift region is 100μm thick. FFR termination with fixed ring space/width was first simulated as a reference.

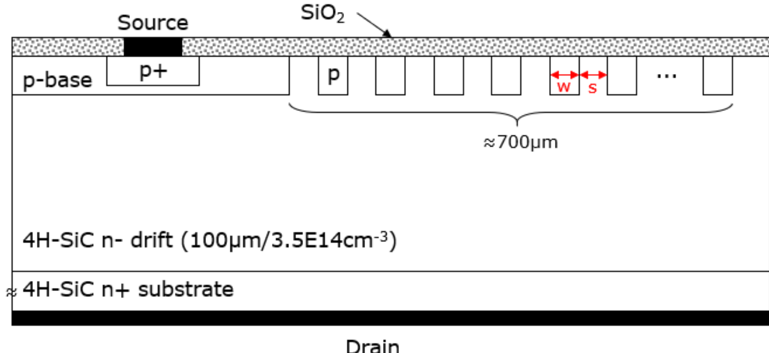

Fig. 7.1 A basic cross-sectional view of the FFR edge termination

A 700µm extended length was initially allocated for the termination region. In most cases p-ring width was set to 3µm and only the p-ring space was varied. P-ring s/w combination of 1.3µm/3µm, 1.5µm/3µm and 2µm/3µm were simulated and the results are shown in Fig. 7.2.

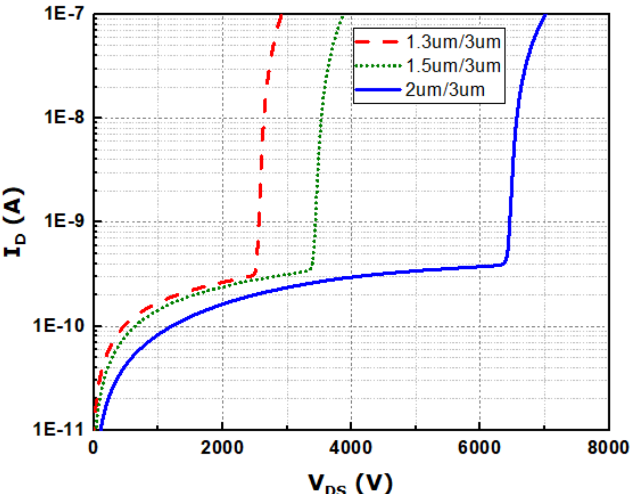

Fig. 7.2 Simulated breakdown down characteristics for p-ring space/width combinations

According to simulation results, fixed p-ring space/width is not effective to spread the electric field out with the allocated 700µm length. The electric field at slightly below p-rings are shown in Fig. 7.3 where the peak electric field for all three cases appear at the last rings.

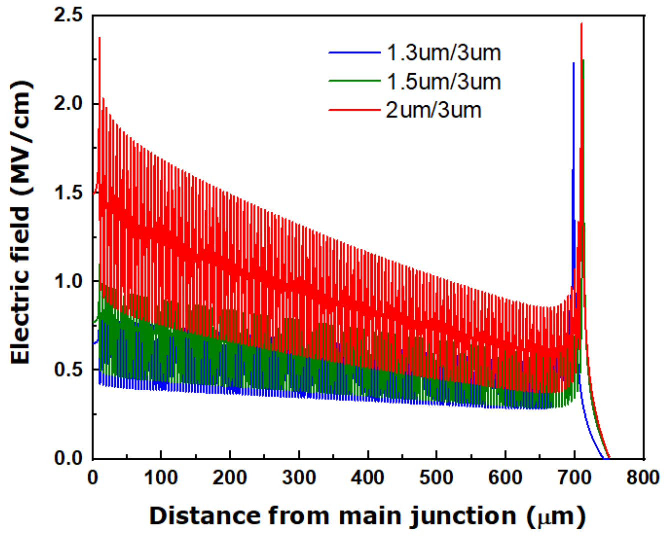

Fig. 7.3 Electric field at the bottom of the floating field rings with fixed ring space/width

For the FFR structure with fixed ring space/width, the breakdown voltage may increase slightly more if more rings are added which also means more areas to be allocated. In this case, the marginal increase on the breakdown voltage is limited with significantly wasted chip area. As a result, fixed ring space/width is not suitable for 10kV devices. Therefore, a constant expansion ratio is added for the field rings.

$$S_n = W_n = \delta S_{n-1} \tag{7.3}$$

In Equation 7.3, S_n and W_n are the space and width for the n_{th} p-ring where δ represents the expansion ratio. Three p-ring expansion ratios are used in the simulation including δ=1.03, δ=1.05 and δ=1.1. The minimum size of the first ring space S_1 is set to 1.3μm due to experimental limit. S_1=1.5μm has also been simulated for reference. The breakdown voltage has been plotted in Fig. 7.4.

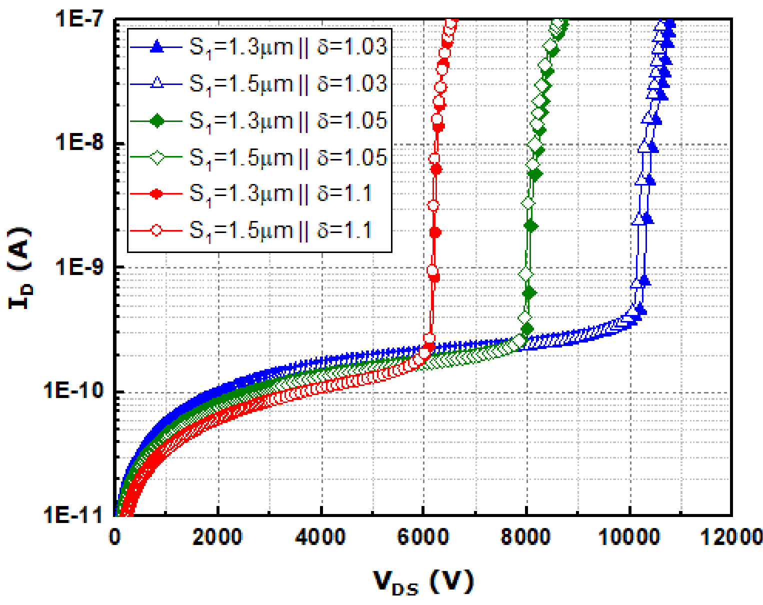

Fig. 7.4 The simulated breakdown voltage with different p-ring expansion ratio

The maximum breakdown voltage of 10.2kV has been reached with 1.03 expansion ratio which corresponds to 68% termination efficiency. The breakdown voltage reduces significantly with increased p-ring expansion ratio which means that the p-rings space and width becomes unnecessarily wide for large δ values that the electric field crowding appears in the first few rings as shown in Fig. 7.5. Further reduction of the δ value may increase slightly the breakdown voltage, however it will eventually transfer the structure back to the p-rings with fixed ring space/width where δ equals to 1.

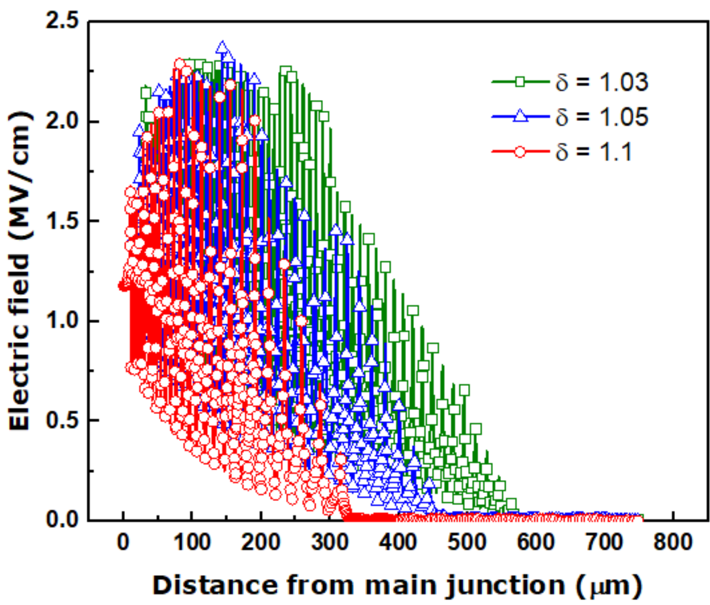

Fig. 7.5 Electric field at the bottom of the floating field rings with various expansion ratios "δ"

To further increase the termination efficiency, adjusted multi-section (AMS) p-rings with a combination of fixed and variable space/width will be investigated. This AMS structure was studied by Deng [8] at a voltage level below 3kV, which proved to be much more efficient than fixed p-ring space/width.

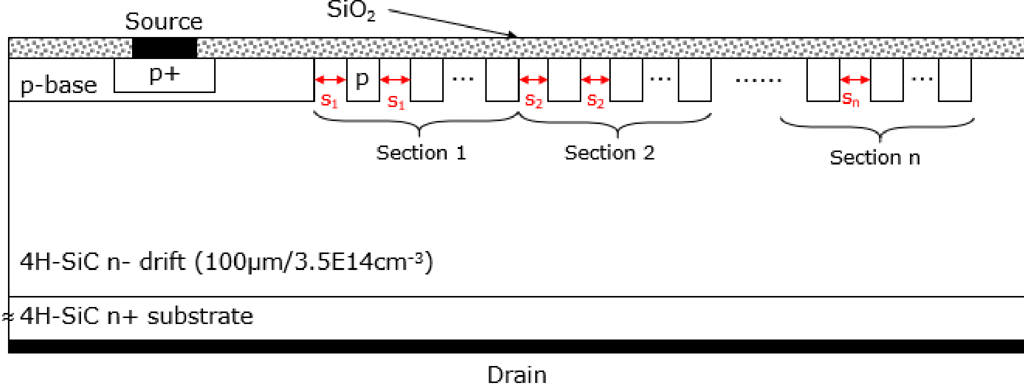

Fig. 7.6 The cross-sectional view of the multi-section p-rings structure

The cross-section view of the AMS p-ring structure is presented in Fig. 7.6. In the same sections, the p-ring spaces remain constant. However, the p-ring space for each next section increases by δ as shown in Equation 7.4.

$$S_n = S_{n-1} + \delta \tag{7.4}$$

The p-ring width is fixed at 3µm in all the sections. δ has been varied from 0.1 to 0.3µm in the simulation. It is worth to mention the AMS p-ring structure is equivalent to the p-ring structure with fixed ring space/width if δ is set to 0µm. In the simulation, 11 rings are allocated to each section and there are 12 sections in total.

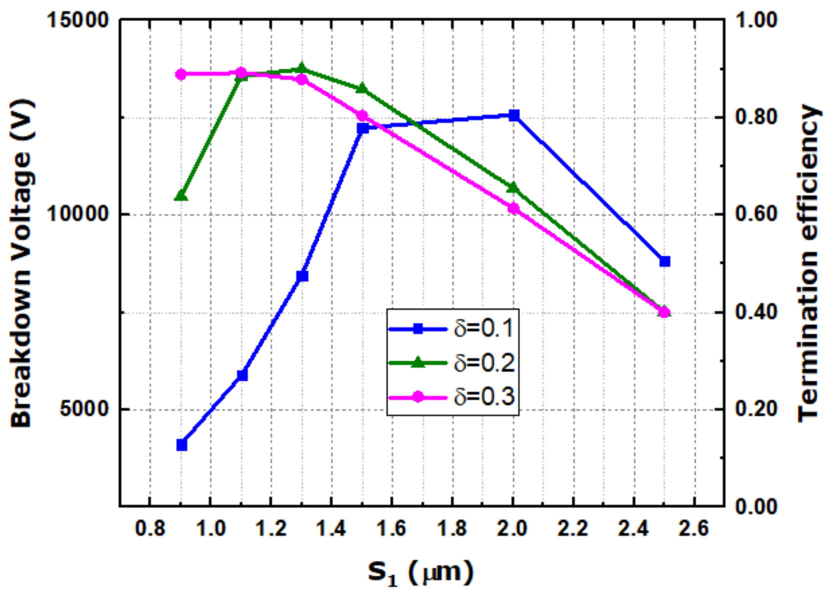

Fig. 7.7 Simulated breakdown voltages for the multi-section p-ring structure with the variation of δ and S_1

The simulated breakdown voltage and the corresponding termination efficiency are presented in Fig. 7.7. A maximum breakdown voltage of 13.7kV has been achieved with corresponding efficiency of 91% at S_1=1.3µm and δ=0.2µm. It is necessary to clarify that these results are only valid for the initial setting of 12 sections with 11 rings in each section. The electric field distribution has been extracted for the AMS p-ring structure with S_1=1.3µm and δ=0.2µm as shown in Fig. 7.8. The peak electric field appears in section 5 of the p-ring structure. The electric field decreases rapidly from section 8 which suggests that section 8 to 12 can still be further optimised. However, a simulated breakdown voltage at 13.7kV should be enough for the 10kV design target and further optimisation work should be done after the feedback from device fabrication and characterisation results

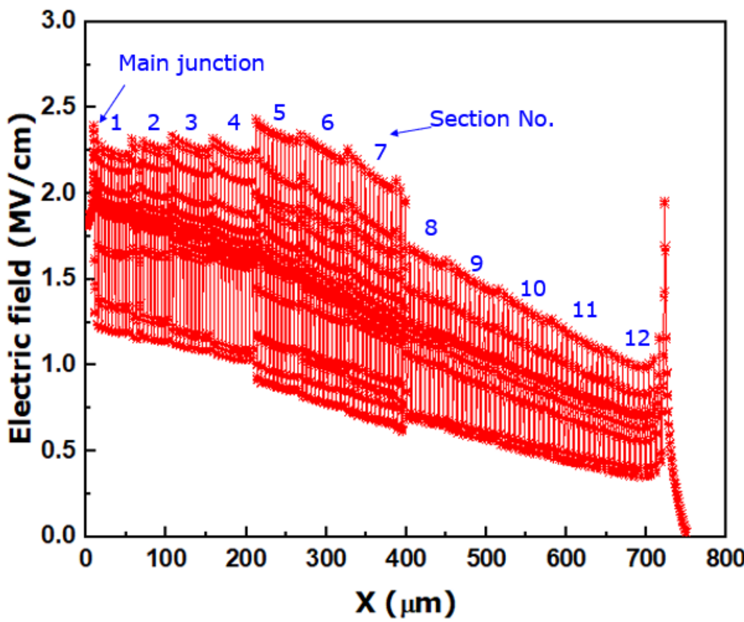

Fig. 7.8 Electric field at the bottom of the multi-section p-ring structure with S_1=1.3μm and δ=0.2μm

7.2.1.2. Junction termination extensions (JTEs)

Junction termination extensions (JTEs) is another widely used termination technique especially for high voltage (>10kV) devices because less chip area is required compared to floating field rings termination. Various structures of JTE termination such as mesa edge single-zone JTE [9], multiple-step JTE [10] and multiple-floating-zone (MFZ) JTE [11] have been proposed for high voltage SiC device fabrication. The breakdown voltage is very sensitive to the shape of the mesa structure if the JTE termination is combined with a mesa edge. For the multiple-step JTE structure, the etching steps must be controlled precisely for the optimum performance. MFZ-JTE has a similar structure with the floating field rings termination and it requires only one implantation. MFZ-JTE can achieve higher breakdown with larger implantation process window compared to single-zone JTE [11]. However, it also consumes more chip area due to the multiple-floating-zone layout. In this section, the more conventional multiple-zone JTE structure has been studied with simulation and benchmarked to the floating field rings termination. Single-zone JTE (SZ-JTE) has been studied first to extract some useful parameters like required zone width, maximum achievable breakdown voltage and the breakdown voltage sensitivity to the doping density.

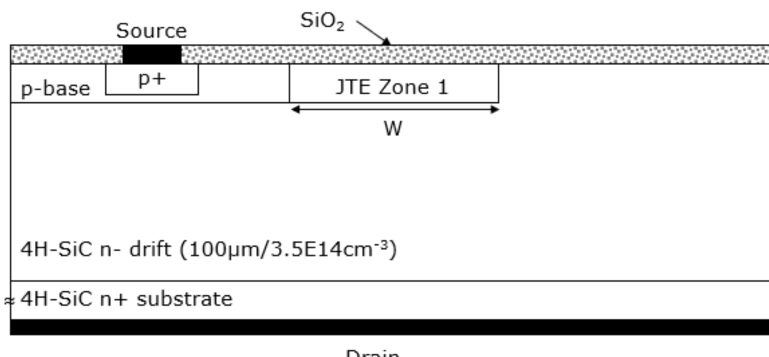

Fig. 7.9 The cross-sectional view of single-zone JTE structure

The zone width "W" and the doping density were varied during the simulation and the results are shown in Fig. 7.10. A zone width of 100µm is apparently not enough for 10kV devices. The results for 200µm and 300µm zone width are similar with a maximum breakdown voltage of 9.7kV achieved with 300µm zone width. The implantation process window is extremely narrow, the breakdown can decrease to 7.3kV when the doping density changes from 9×10^{16}cm^{-3} to 7×10^{16}cm^{-3} and the situation is worse if the doping density is higher than 9×10^{16}cm^{-3}. It seems to be difficult for single-zone JTE to be further optimised by increasing the zone width. A double-zone JTE was then simulated based on the results of the single-zone JTE.

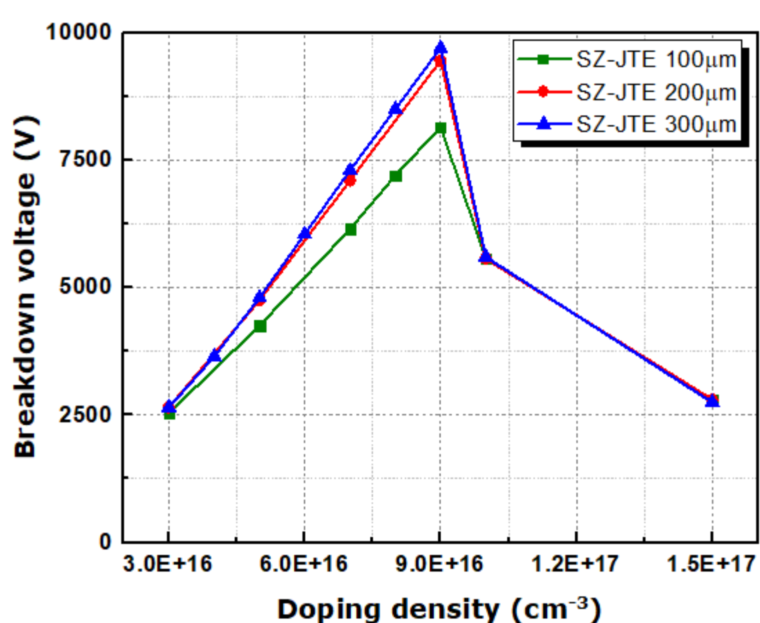

Fig. 7.10 The simulated breakdown voltage against the doping density for single-zone JTE

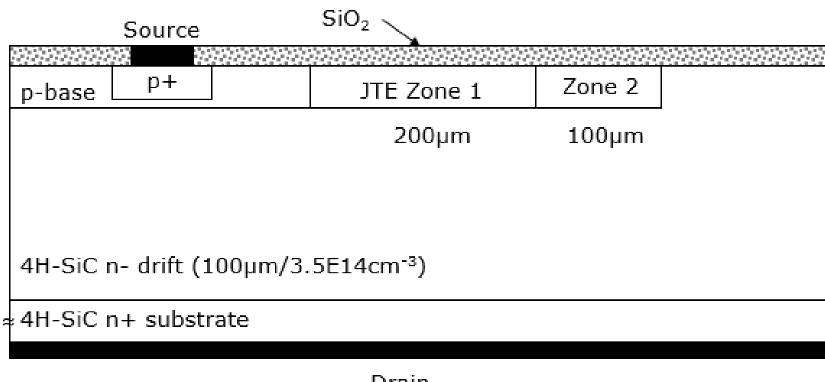

Fig. 7.11 The cross-sectional view of double-zone JTE structure

Even though single-zone JTE is no longer the design choice, the simulation results do provide useful information that can be used for double-zone JTE (DZ-JTE) design. The zone width of the double-zone JTE are fixed at 200μm and 100μm for Zone 1 and Zone 2 respectively. Double-zone JTE is essentially adding a second zone to the single-zone JTE to relieve the electric field stress at the end of Zone 1. In this case, the doping density of Zone 1 for the double-zone JTE must be higher than the optimum doping density in the single-zone JTE, otherwise the peak electric field will locate at the main junction and existence of the second zone is not significant. The simulation results for the double-zone JTE are presented in Fig. 7.12 where the breakdown voltage is plotted against the doping density of Zone 2.

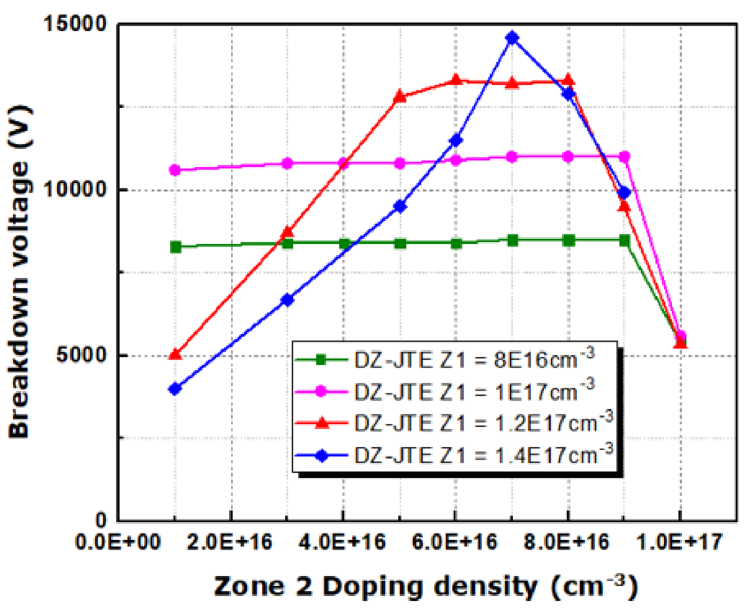

Fig. 7.12 The simulated breakdown voltage against Zone 2 doping density for DZ-JTE

A maximum breakdown voltage of 14.6kV was achieved by the double-zone JTE with the doping densities of $1.4\times10^{17}cm^{-3}$ and $7\times10^{16}cm^{-3}$ for Zone 1 and Zone 2 respectively. With reduced Zone 1 doping, the implantation process window can be increased at the cost of lower breakdown voltage. When Zone 1 doping density is lower than or equals to $1\times10^{17}cm^{-3}$, the breakdown voltage is virtually independent of Zone 2 doping density if Zone 2 doping density is lower than $9\times10^{16}cm^{-3}$.

It seems that the design target has been achieved with high breakdown voltage and large implantation process window for the double-zone JTE. However, the early conclusion about the large implantation process window is not entirely correct because the breakdown voltage is still very sensitive to the doping concentration of the first zone. For instance, if the implantation activation rate is only 50% with a targeted Zone 1 doping density at $1.4\times10^{17}cm^{-3}$, the actual Zone 1 doping density will be lower than $7\times10^{16}cm^{-3}$ resulting in very low breakdown voltage based on the simulation results. To further increase the implantation process window, the so-called triple-zone JTE is then introduced.

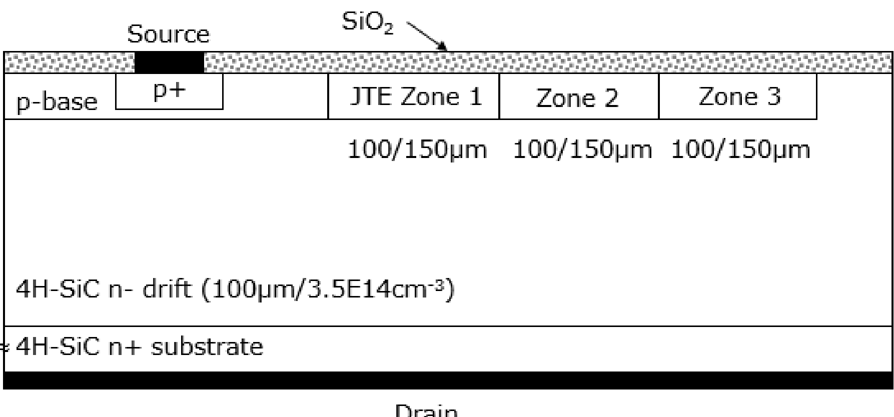

Fig. 7.13 The cross-sectional view of triple-zone JTE structure

The zone width for the triple-zone JTE has been adjusted to be equal for all the three zones. Again, the simulation results of the double-zone JTE can now provide valuable information to start the simulation for the triple-zone JTE. The best Zone 1 and Zone 2 doping density are $1.4\times10^{17}cm^{-3}$ and $7\times10^{16}cm^{-3}$ for double-zone JTE, therefore, it is reasonable to set the doping density of Zone 2 as twice the value of Zone 3 and the same principle is applied for Zone 1. In this case, if the implantation activation rate is only 50%,

the golden doping density combination of adjacent zones ($1.4\times10^{17}cm^{-3}$ and $7\times10^{16}cm^{-3}$) simply shifts from Zone 2 and Zone 3 to Zone 1 and Zone 2 as shown in Table 7.1 below.

Table 7.1 Actual doping density based on the activation rates

Activation rate	Zone 1 ($2.8\times10^{17}cm^{-3}$)	Zone 2 ($1.4\times10^{17}cm^{-3}$)	Zone 3 ($7\times10^{16}cm^{-3}$)
100%	$2.8\times10^{17}cm^{-3}$	$1.4\times10^{17}cm^{-3}$	$7\times10^{16}cm^{-3}$
50%	$1.4\times10^{17}cm^{-3}$	$7\times10^{16}cm^{-3}$	$3.5\times10^{16}cm^{-3}$

There should be two peaks in the plot of the breakdown voltage against Zone 3 doping density for the triple-zone JTE, this can be verified by the simulation results presented below in Fig. 7.14.

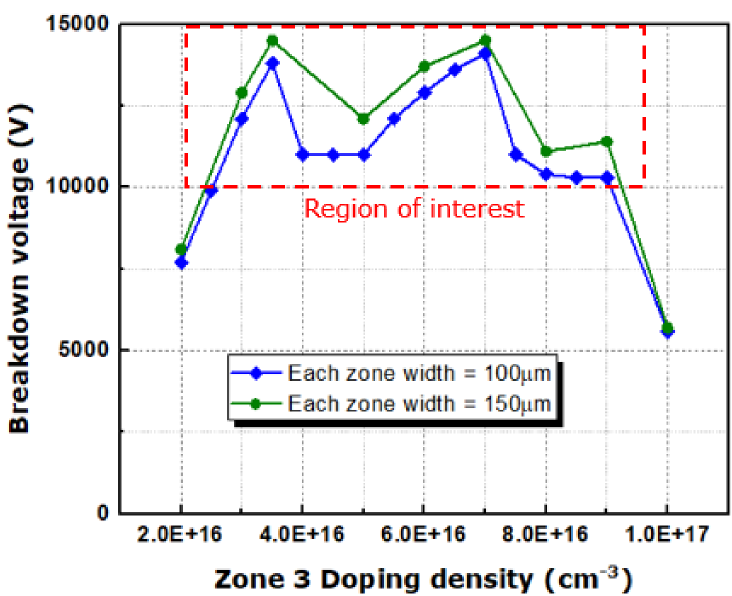

Fig. 7.14 The simulated breakdown voltage against Zone 3 doping density for TZ-JTE

The maximum breakdown voltage appears at $3.5\times10^{16}cm^{-3}$ and $7\times10^{16}cm^{-3}$ Zone 3 doping density. The highlighted region of interest in Fig. 7.14 provides a relatively wide implantation process window ranging from $2.5\times10^{16}cm^{-3}$ to $9\times10^{16}cm^{-3}$. The breakdown voltage curve can be shifted up slightly if the zone width is increased from 100µm to 150µm which also requires larger chip area. The electric field and potential distribution have been plotted at the location below the main junction and the tripe-zone JTE as shown in Fig. 7.15. The peak electric field shifts from the Zone 2/3 junction to the Zone 1/2 junction if Zone 3 doping density is decreased from $7\times10^{16}cm^{-3}$ to $3.5\times10^{16}cm^{-3}$. For any

other doping densities, neither of the three zones are at the optimum point therefore the breakdown voltage will decrease. The electric field distribution at various drain voltage is shown in Fig. 7.16 which can help better understand the JTE structure for future optimisation.

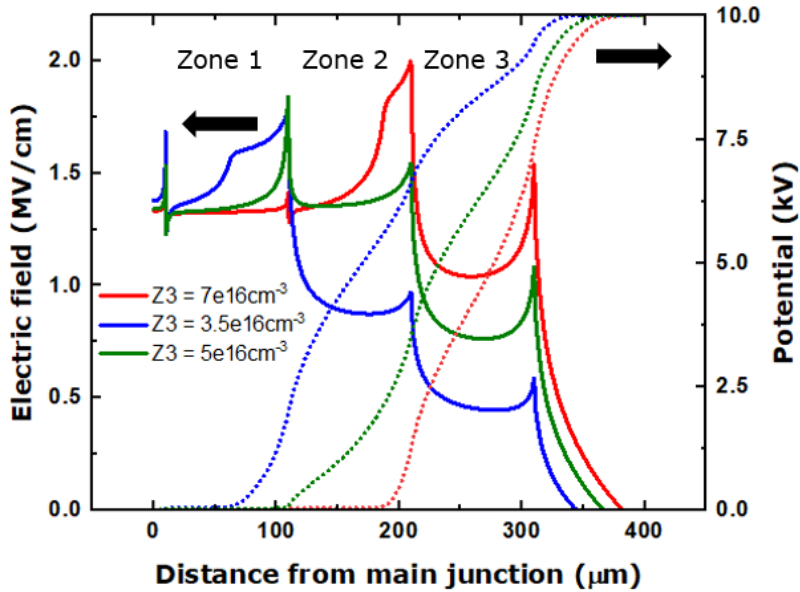

Fig. 7.15 The electric field and potential distribution at below the main junction and the triple-zone JTE with $V_{DS} = 10kV$

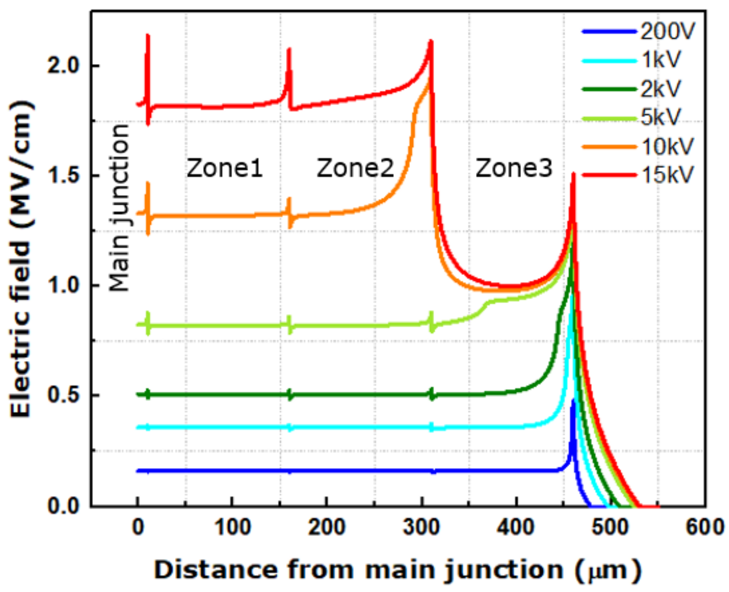

Fig. 7.16 The electric field distribution at below the main junction and the triple-zone JTE at different V_{DS} voltage with fixed Zone 3 doping density of $7\times10^{16}cm^{-3}$

To summarise on the edge termination design, the 10kV breakdown voltage can be achieved with both multi-sections floating field rings and the triple-zone JTE structure. A triple-zone JTE requires much less chip area (a minimum total width of 300μm) with higher implantation cost. Multi-sections floating field rings can be implanted in the same time with the p-base region with no extra implantation cost, however, the p-ring structure can occupy more than twice the chip area compared to the triple-zone JTE design. Although the maximum breakdown voltage of 14.5kV can be achieved by the triple-zone JTE design according to simulation, it is not likely that this optimum breakdown can be realised in the experiment. In this work, multi-sections floating field rings were chosen as the edge termination topology due to lower cost and the convenient process despite the higher consumption of the chip area. The floating field rings with fixed ring space/width = 2μm/2μm was also used as the termination for reference.

7.2.2. On-state optimisation

For a 10kV DMOSFET, the design optimisation mainly focused on the JFET region and the threshold voltage control. The general schematic of the half cell structure is shown in Fig. 7.17.

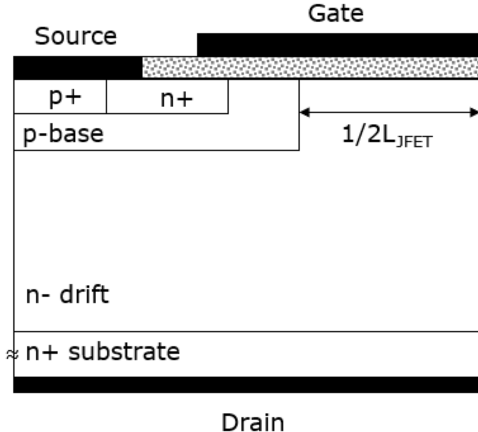

Fig. 7.17 The cross-sectional view of the DMOSFET half cell structure

The on-state performance of the device has been simulated with various JFET width. The channel mobility was set to ~10cm^2/(Vs) which reflects the real on-site device processing capability. The current density and specific on-resistance "R_{on_sp}" have been plotted against the JFET length in Fig. 7.18.

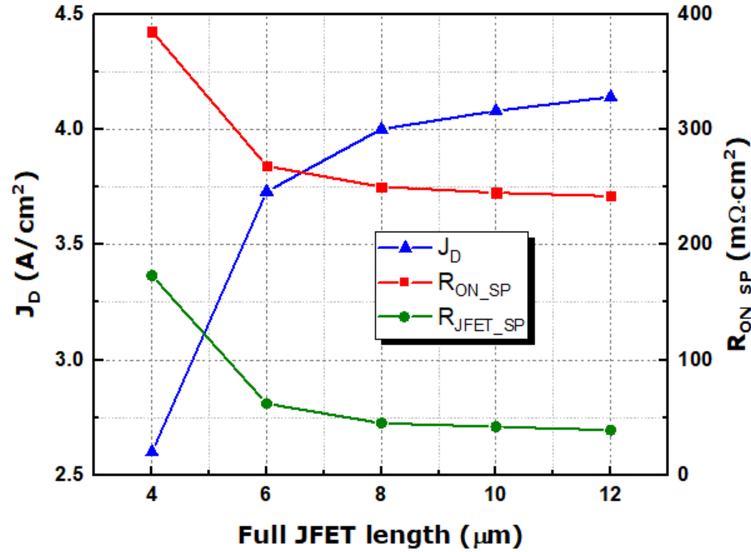

Fig. 7.18 The simulated J_D , R_{ON_SP} and R_{JFET_SP} results with different full JFET length

R_{on_sp} is as high as 380mΩ·cm^2 for a JFET length of 4μm, this value decreases to below 250mΩ·cm^2 as the JFET length increases to above 8μm. R_{on_sp} will rise again if the JFET length is above 12μm due to the increased channel resistance. As the drift region contributes to the majority part of the total resistance for 10kV devices, JFET implantation is not necessary at this stage. A suitable choice of the JFET length can be made between 8μm and 12μm.

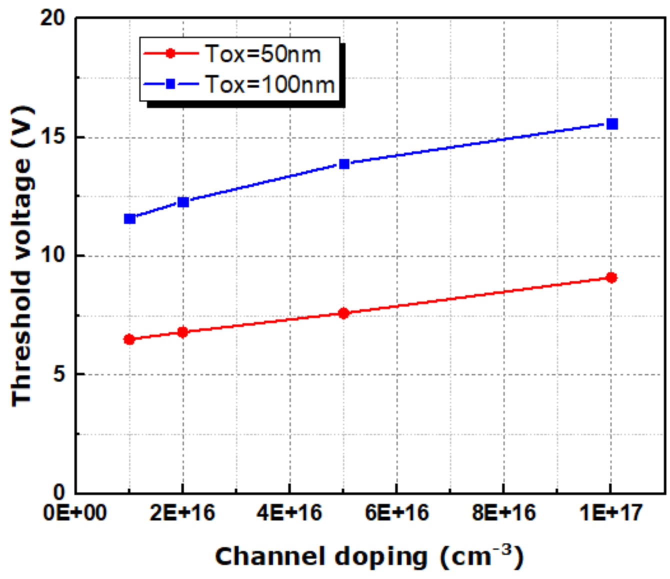

Fig. 7.19 The simulated gate threshold voltage against the channel surface doping density with 50nm and 100nm oxide thickness

The gate threshold voltage was simulated with various channel doping density and the gate oxide thickness. Commercial SiC MOSFETs normally have a threshold voltage in the range of 2 ~ 3V at room temperature. The minimum threshold voltage extracted from the simulation is 6.5V at a doping density as low as $1\times10^{16}cm^{-3}$ and the further reduction is limited by the interface trap model. As a result, 50nm gate oxide thickness seems to be the best choice to keep a low threshold voltage even though thicker gate oxide layer tends to be more reliable based on the cleanroom fabrication experience.

7.3. Device fabrication

The 10kV DMOSFET fabrication processes are introduced in this section which includes photo mask design, ion implantation and the standard cleanroom device fabrication steps.

The mask layout of the 10kV DMOSFET and the PiN diode are shown in Fig. 7.20. The PiN diode was mainly used to verify the termination structure. For instance, if the breakdown votlge of the MOSFET is very low, the PiN diode will be able to determine either the termination structure or the active region is responible. The active area of the MOSFET is approximately 1mm by 1mm which is quite small and cost inefficient for such a large termination region, however, high current devices have better chance to be fabricatd successfully in a proper foundry instead of the cleanroom research facility inside the university.

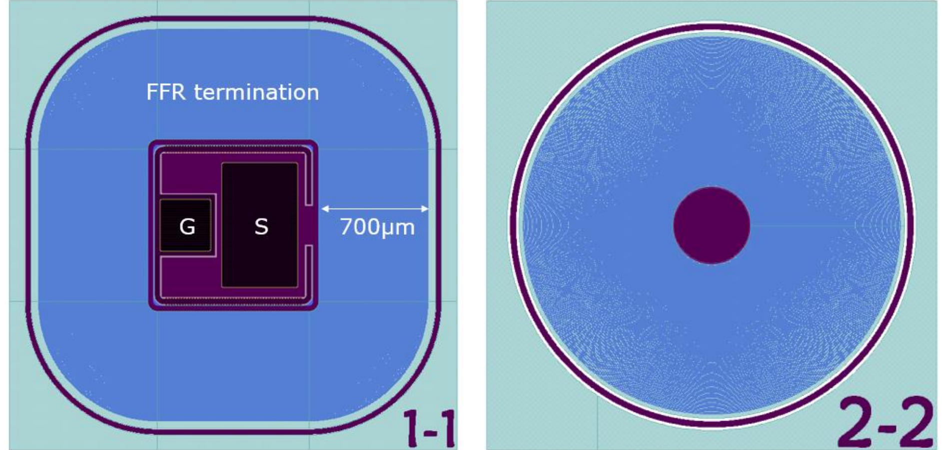

Fig. 7.20 The photo mask top view of DMOSFET (left) and PiN diode (right)

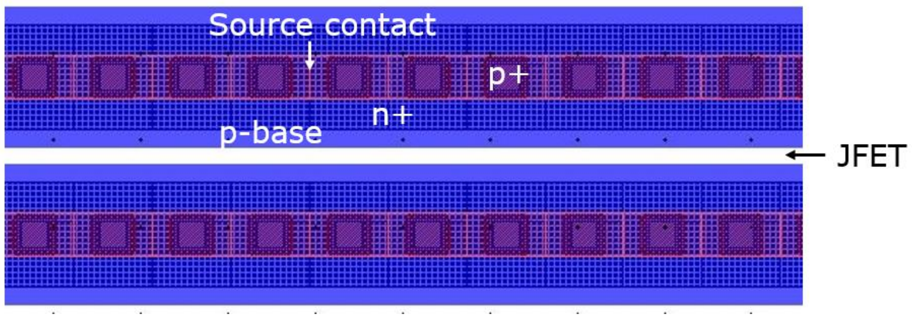

Fig. 7.21 Mask layout of two adjacent MOSFET fingers/strips

The discrete squares were the process window reserved for p+ implantation, a smaller cell pitch can be achieved with this layout instead of a full p+ stripe. The channel length was set to 2μm. For channel length below 2μm, self-alignment process should be considered which remains a future approach. The JFET length should be in the range of 8μm ~ 12μm for good on-state performance based on the simulation results. Unfortunately, a mistake was made on the photo mask design and the JFET length for the fabricated devices is only 2μm which is a catastrophe for the on-state performance of the devices. Since this mistake was identified after the implantion process, it was too late and the device fabrication was therefore carried on since the more important termination design can still be verified.

Three implantation steps are needed for the 10kV DMOSFET fabrication. The implantation dose and energy have been listed in Table 7.2.

Table 7.2 Implantation specifications for the 10kV DMOSFET fabrication

	Dose No.	Energy (keV)	Dose (cm$^{-3)}$
p-base/ring	1st dose	535	4.5×10^{13}
	2nd dose	410	9.5×10^{12}
	3rd dose	300	8.5×10^{12}
n+	1st dose	150	2×10^{15}
	2nd dose	90	1.4×10^{14}
	3rd dose	50	9.5×10^{14}
p+	1st dose	180	4×10^{14}
	2nd dose	100	2×10^{14}
	3rd dose	40	1×10^{14}

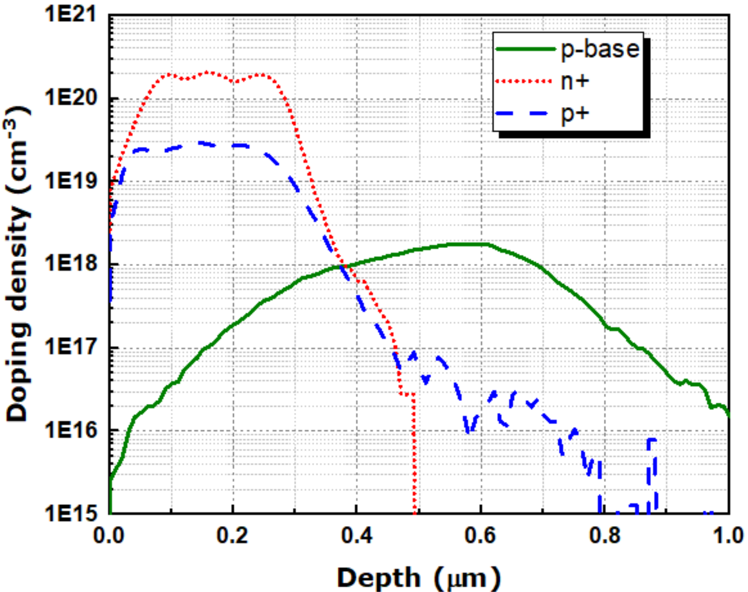

Fig. 7.22 Implantation profile simulated by TCAD Silvaco

As shown in Fig. 7.22, the n+ and p+ implantation conditions were adjusted to produce a box profile where the doping density is almost constant up to a certain depth. A retrograde p-base doping profile is preferable for 10kV devices so that the highly doped bottom region is used to prevent device punch through and the lightly doped surface region is used to control the threshold voltage and reduce the channel resistance.

The process flow of 10kV DMOSFET is described in Table 7.3. The key notes about each fabrication step are listed on the right-hand side of the table as before. The ordinary alignment mark etching step is not shown in the table. SiO_2 was used as the implantation mask for all the three implantations.

Table 7.3 10kV DMOSFET process flow

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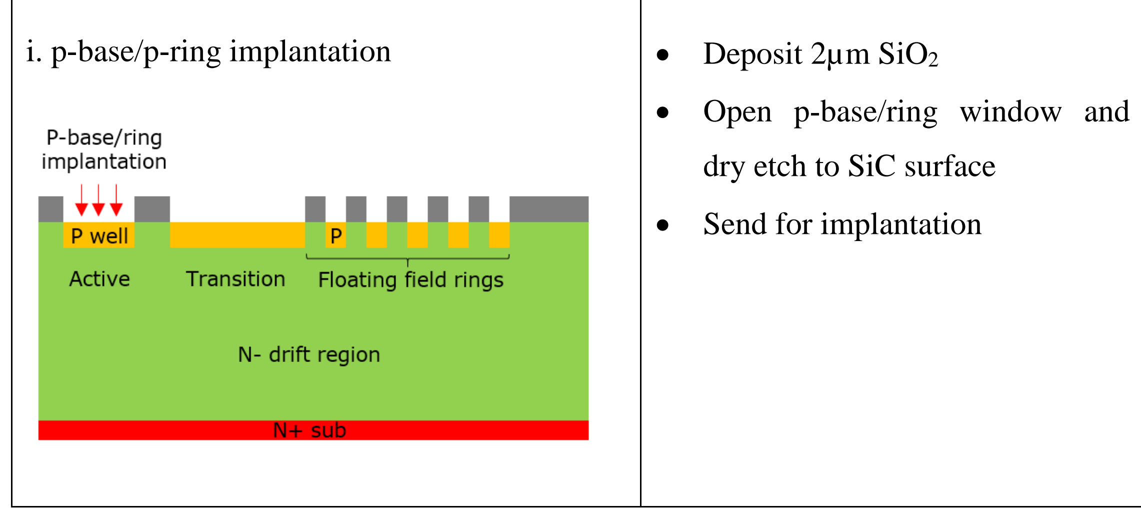
<td>
i. p-base/p-ring implantation



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- Deposit 2μm SiO_2
- Open p-base/ring window and dry etch to SiC surface
- Send for implantation

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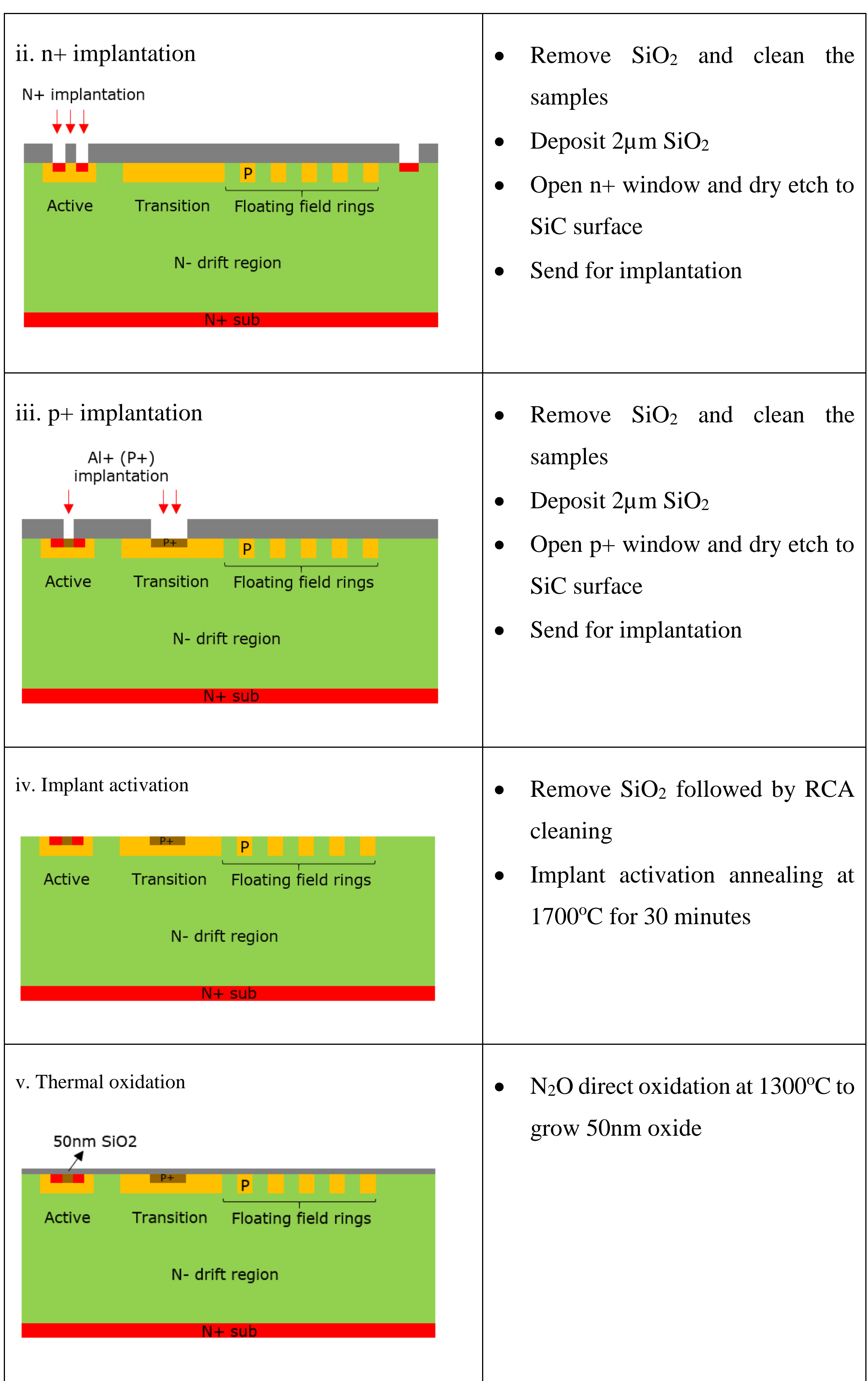
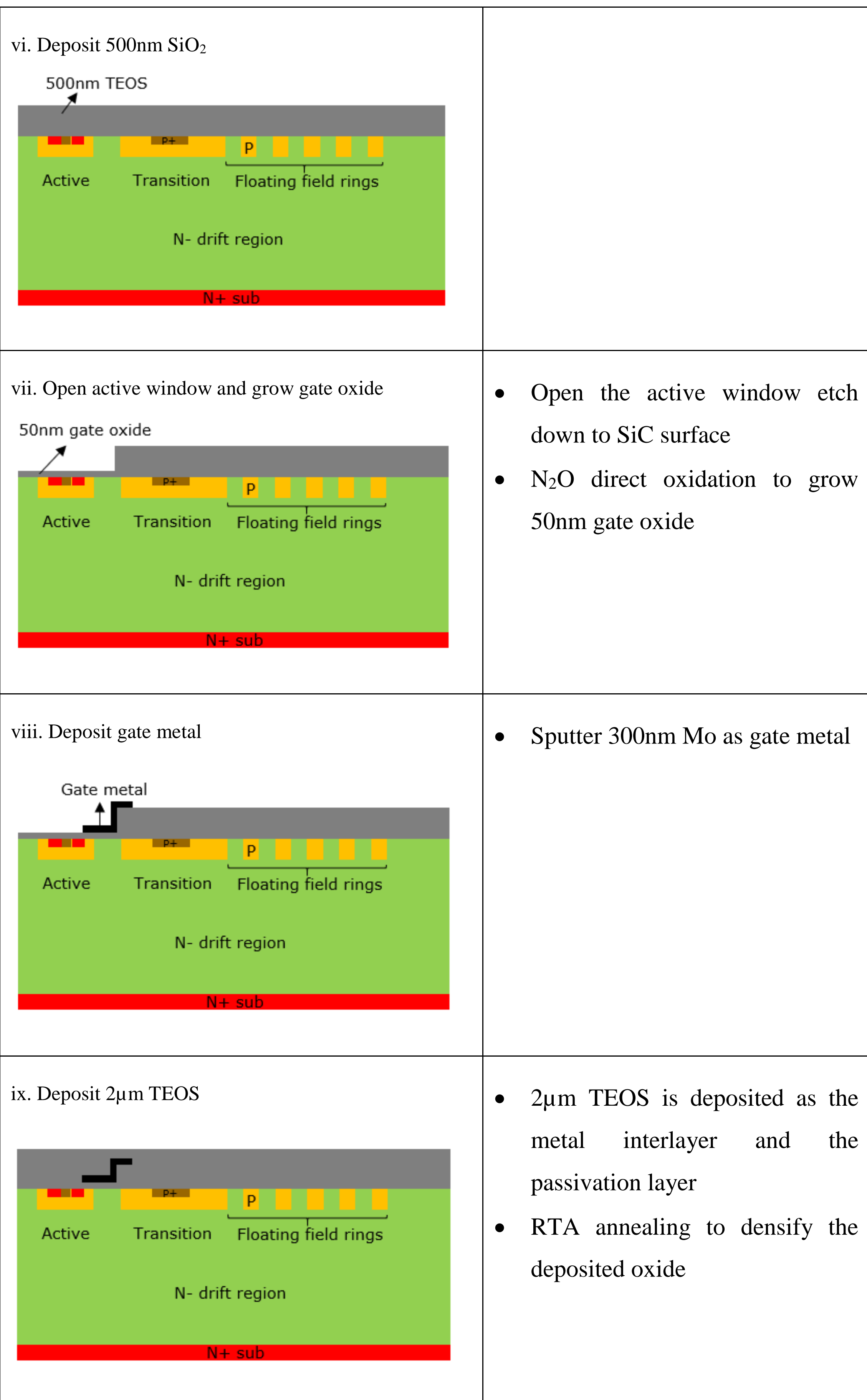


Step	Process
ii. n+ implantation	• Remove SiO_2 and clean the samples • Deposit 2μm SiO_2 • Open n+ window and dry etch to SiC surface • Send for implantation
iii. p+ implantation	• Remove SiO_2 and clean the samples • Deposit 2μm SiO_2 • Open p+ window and dry etch to SiC surface • Send for implantation
iv. Implant activation	• Remove SiO_2 followed by RCA cleaning • Implant activation annealing at 1700°C for 30 minutes
v. Thermal oxidation	• N_2O direct oxidation at 1300°C to grow 50nm oxide



Step	Description
vi. Deposit 500nm SiO_2	
vii. Open active window and grow gate oxide	• Open the active window etch down to SiC surface • N_2O direct oxidation to grow 50nm gate oxide
viii. Deposit gate metal	• Sputter 300nm Mo as gate metal
ix. Deposit 2µm TEOS	• 2µm TEOS is deposited as the metal interlayer and the passivation layer • RTA annealing to densify the deposited oxide

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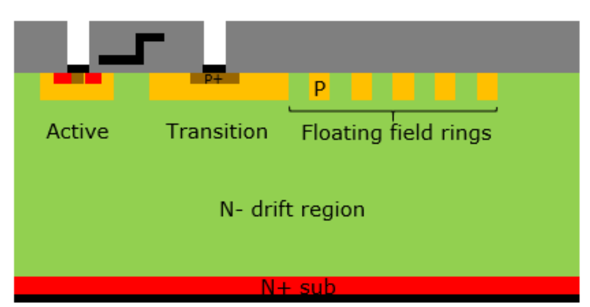
<td>x. Drain and source ohmic contact formation
</td>
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- Open the source window and etch down to SiC surface
- Deposit Ti/Ni 30nm/100nm on both the top surface and the bottom of the substrate and anneal at 1000°C for 2min to form ohmic contact

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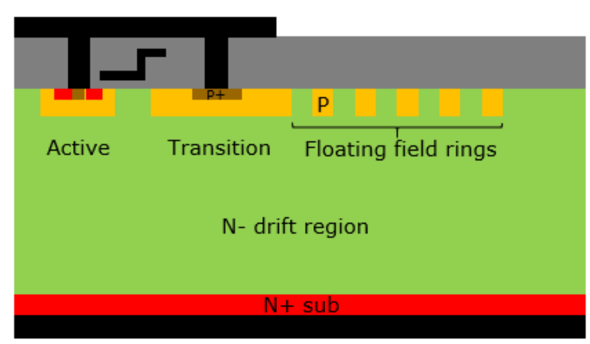
<td>xi. Deposit >2μm thick aluminium pad metal
</td>
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- Deposit thick Al pad metal for both the top surface and the bottom of the substrate

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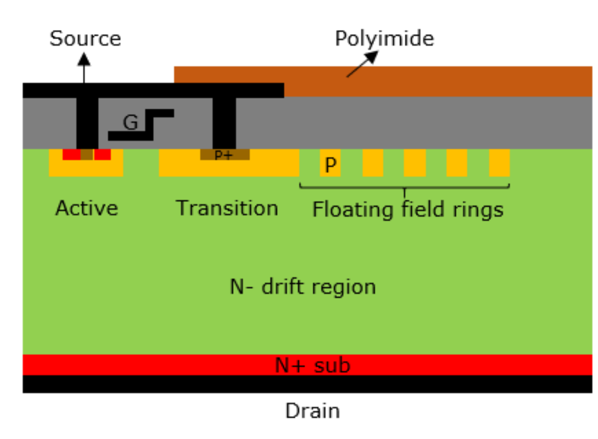
<td>xii. Deposit polyimide passivation layer
</td>
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- Polyimide deposited as passivation layer

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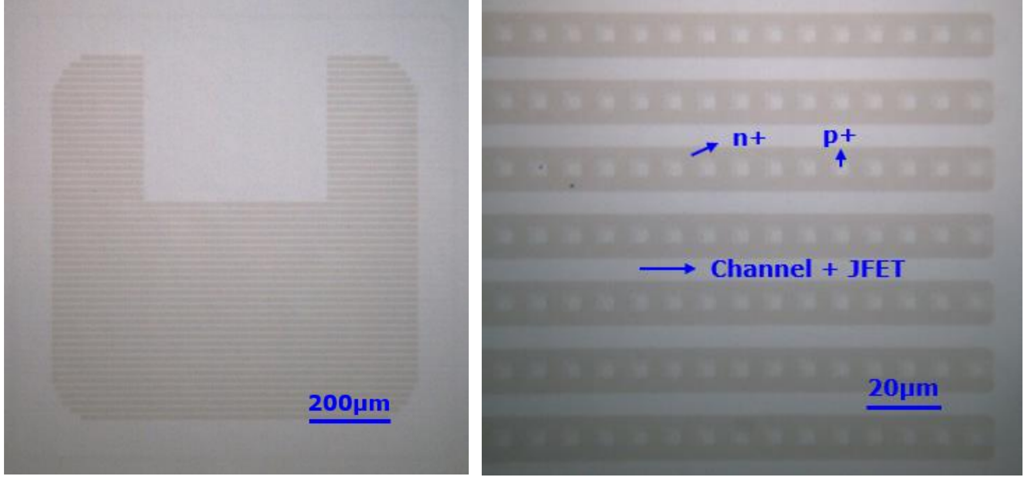
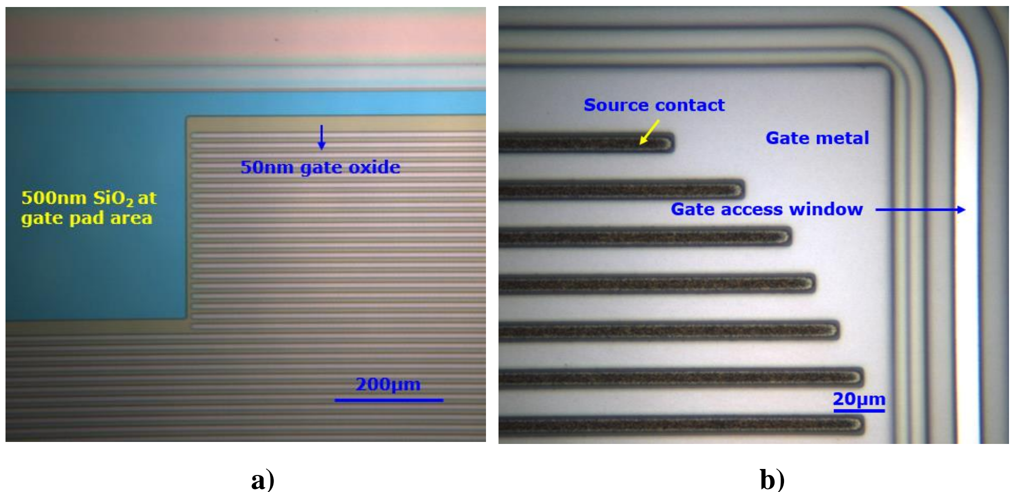


Fig. 7.23 Microscopic images about the SiC surface visible damages after the implantation steps

Implantation damages were observed with optical microscope and the relevant images are presented in Fig. 7.23. These damage patterns sometimes can be useful for the photolithography process to reduce the misalignment.



a) b)

Fig. 7.24 Microscopic images taken before gate metal deposition (left) and after source ohmic contact annealing (right)

Fig. 7.24a is the image captured before depositing gate metal. 500nm SiO_2 was deposited for the gate pad area to reduce the gate capacitance and increase the robustness of the gate contact during packaging processes. The other image in Fig. 7.24 was taken after source ohmic contacts annealing. After the source window is opened with the photo lithography process, dry etching process will be needed to etch 2µm thick SiO_2 before the source metal can be deposited. Firstly, this photo lithography step is critical since a misalignment can introduce a short circuit between gate and source. Secondly, the photo

resist must be thick enough so that the metal lift-off process can still be done after 2µm SiO_2 dry etching process.

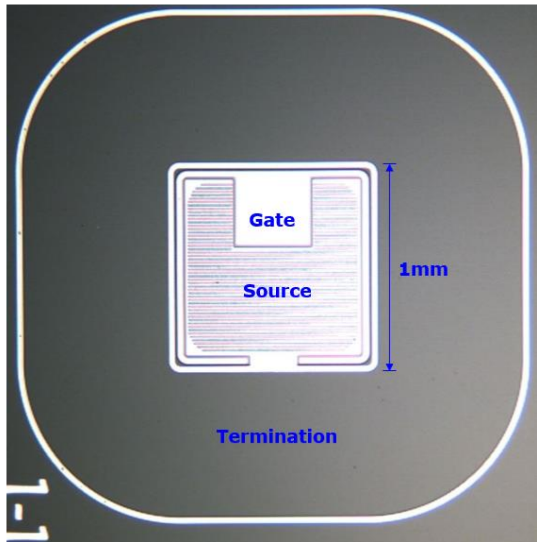


Fig. 7.25 A microscopic photo of fabricated 10kV DMOSFET before polyimide deposition

The fabricated 10kV MOSFET is shown in Fig. 7.25 with 1mm × 1mm active area. The termination and device active area ratio is relatively large for these first-generation devices. Once the termination design has been optimised, large current devices can be fabricated in the future.

7.4. Device characterisation

Device characterisation was performed by the collaboration partner in China. The on-state performance of the MOSFETs were first characterised and the results are shown in Fig. 7.26. As mentioned before, an incorrect JFET length parameter was used during the photo mask design which was not discovered in time. An extremely narrow JFET region can lead to a large building potential and very low current when the device is switched on. In this case, the poor on-state device performance shown in Fig. 7.26 are not difficult to explain. The on-state performance can be optimised by introducing larger JFET region as suggested by the simulation results.

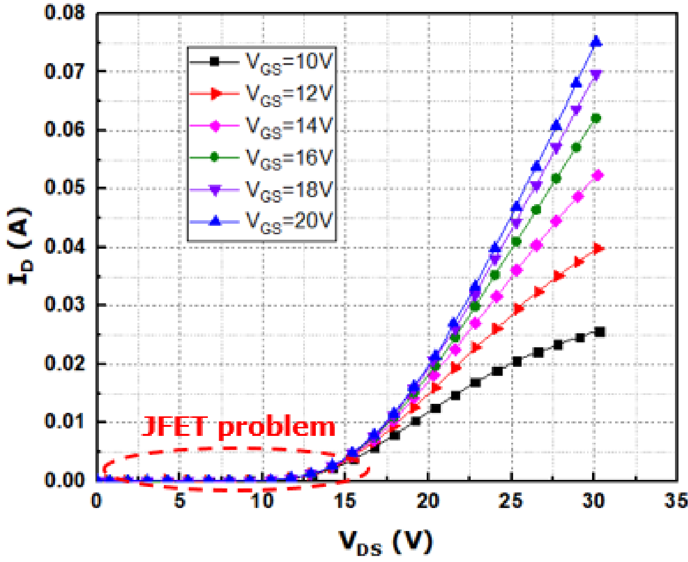


Fig. 7.26 On-state characteristics of the fabricated 10kV MOSFETs

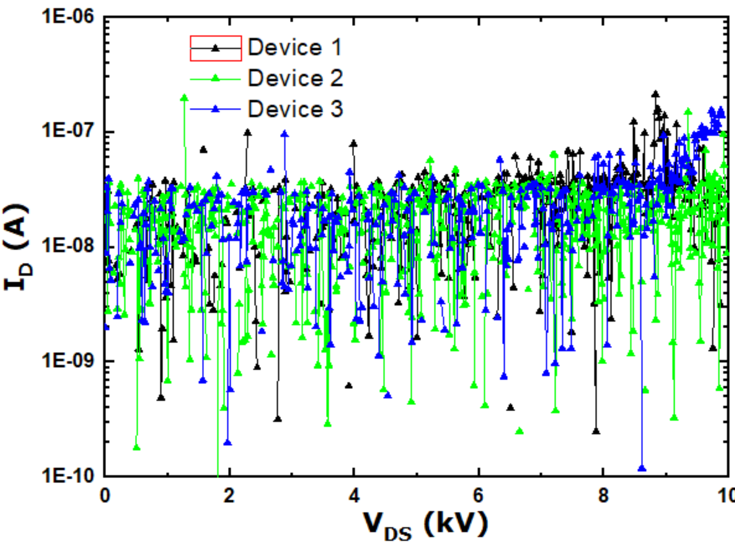


Fig. 7.27 Blocking characteristics of the fabricated 10kV MOSFETs

The off-state characterisation was performed on bare dies with high voltage probe station up to 10kV. Fig. 7.27 presents the results collected from the fabricated MOSFET devices with multi-sections floating field rings termination (S_1 = 1.3μm). The real breakdown voltage can not be determined since the device analyser measurement capability is limited up to 10kV. Point measurement was then performed up to 15kV with a current compliance of approximately 4E-5A. The extracted breakdown voltages are listed in Table 7.4 for various p-ring termination with a maximum breakdown voltage of 13.6kV achieved.

Table 7.4 Comparison of the experimental and simulated breakdown voltages

Termination design	Breakdown	Simulation
a) Multi-sections FFR with S_1 = 1.3μm	13.6V	13.7kV
b) Multi-sections FFR with S_1 = 1.5μm	12kV	13.2kV
c) FFR with fixed ring space/width = 2μm/2μm	10kV	10.3kV

The experimental results with termination option a) and c) agree well with the simulation results. The measured breakdown voltage for multi-sections FFR with S_1 = 1.5μm is 1200V less than the simulated result, the reason for this is not known explicitly. Overall the 10kV blocking voltage target has been achieved successfully with multi-sections FFR edge termination.

7.5. Summary

In this chapter, 10kV SiC MOSFETs have been designed and fabricated. The 10kV design target of the blocking voltage has been achieved successfully with multi-sections FFR termination. The on-state performance is rather poor due to a mistake made on the JFET length, this has been corrected for the next generation devices. Although multi-sections p-ring termination design has been proved valid, it does consume large chip area which needs to be optimised in the future.

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Chapter 8 Novel device structure

This chapter proposes some novel device structures that have the potential to be fabricated soon. The main concepts include the SiC trench MOSFET with integrated Schottky contact and the feasibility study of superjunction SiC MOSFETs with implanted trench sidewalls. All the results presented in this chapter are based on TCAD silvaco simulation.

8.1 SiC MOSFETs with integrated Schottky contact

For applications with inductive load like motor drives, external Schottky diodes (SBD) are usually connected antiparallelly to MOSFETs to provide the freewheeling current path. The body PiN diode in the SiC MOSFET structure has a high knee voltage because of the wide band-gap nature of silicon carbide material. Higher conduction losses can be generated if the body diode is used as the freewheeling diode. In the meantime, bipolar degradation was reported for SiC PiN diodes [1] which raises serious reliability concerns about the bipolar operation of SiC MOSFETs. This section proposes a 4H-SiC UMOSFET design with integrated merge-PiN Schottky (MPS) diode named as MPS-UMOS.

The total chip count can be reduced if the Schottky diode is embedded into the MOSFET structure. A SiC DMOSFET with embedded Schottky diode was proposed in [2] which demonstrated smaller reverse recovery charges and lower switching losses in comparison to conventional MOSFETs with the body diode conduction. The fabrication of a UMOSFET with embedded Schottky diode was reported in [3], however, the MOSFET structure and the embedded Schottky diode only share the termination region instead of the active region. In this work, a Schottky contact is embedded at the bottom of the gate trench which achieves a high-level structure integration since the MOSFET and Schottky diode share both the active region and the termination region. The schematic of the proposed structure is shown in Fig. 8.1.

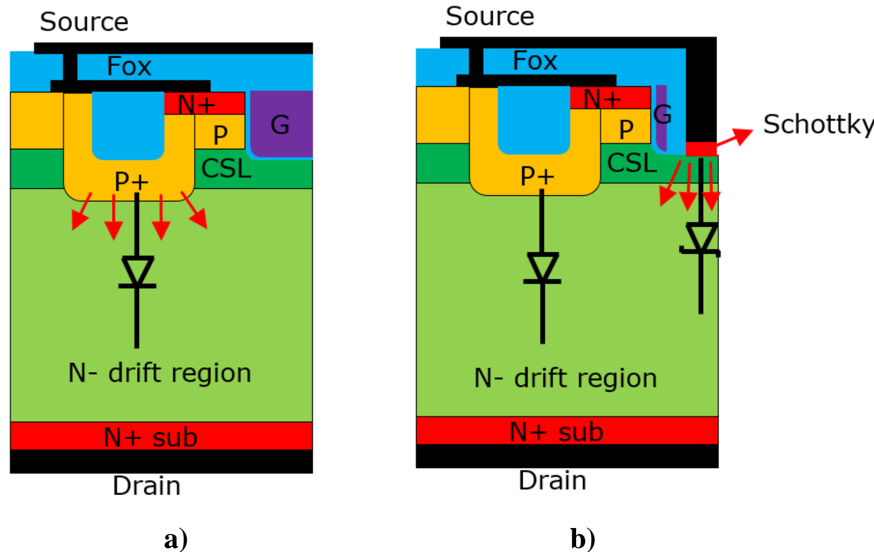


Fig. 8.1 a) the conventional UMOS structure; b) proposed MPS-UMOS structure with embedded Schottky contact

The conventional UMOS structure is shown in Fig. 8.1a for reference. The deep p+ implanted region is used to protect the gate oxide from high electric field stress [4]. The trench bottom gate oxide requires electric field shielding and the Schottky contact has similar requirement to avoid high leakage current, therefore, it is reasonable to embed the Schottky contact at the bottom of the gate trench as shown in Fig. 8.1b. The advantage of this design is that the Schottky diode can use the p+ implanted region to shield the Schottky contact as well, there is no need for an extra p+ region to form the merged-PiN Schottky diode because the "PiN" diode is already in the conventional UMOS structure. This design leads to a total chip size reduction in comparison to the configuration with MOSFETs and external Schottky diodes.

The proposed structure has been simulated using TCAD Silvaco by varying the p+ implantation depth and the CSL doping concentration. The simulation results are presented in Fig. 8.2 and Fig. 8.3. It is demonstrated in Fig. 8.2a that the Schottky diode reverse leakage current can be reduced by increasing the p+ implant depth as the Schottky contact is shielded more effectively from the peak electric field. However, deeper p+ region also leads to higher parasitic JFET resistance and therefore the forward voltage drop of the Schottky diode at 200A/cm^2 current density has also been plotted against the p+ implant depth. In addition, the electric field on both the gate oxide and the surface of the Schottky contact has been extracted from simulation and the results are plotted in Fig. 8.2b.

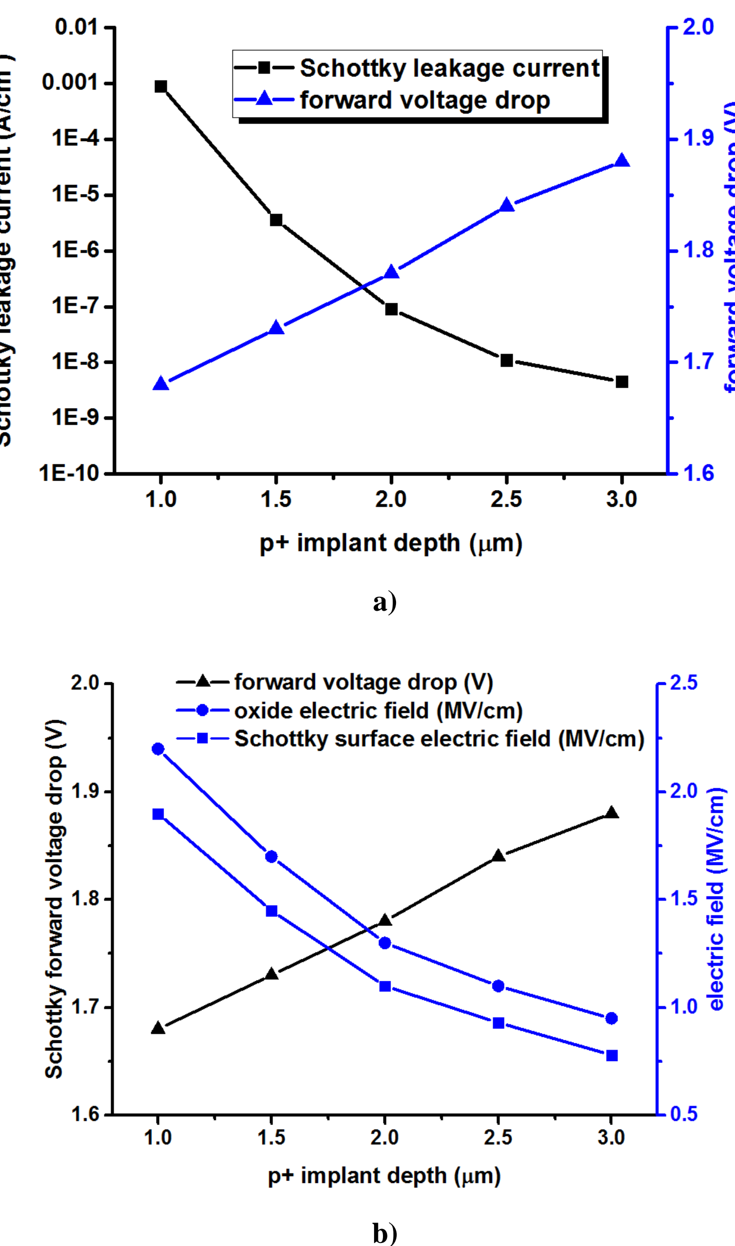


Fig. 8.2 The plot of the Schottky forward voltage drop at 200A/cm^2 a) versus the leakage current density at 1000V drain voltage; b) versus the electric field on the gate oxide and Schottky contact surface at 1000V drain voltage

The electric field on the trench gate oxide is lower than 1.3MV/cm while the Schottky surface field is 1.1MV/cm with 2μm p+ implant depth. When the p+ implant depth is increased, there is a slight increase on the Schottky diode forward voltage drop at 200A/cm^2 current density which is not as sensitive as studied in [5]. Based on the simulation results, 2μm~2.5μm deep p+ implant depth seems to be a proper design choice which guarantees low electric field and low Schottky reverse leakage current without significantly compromising the on-state performance.

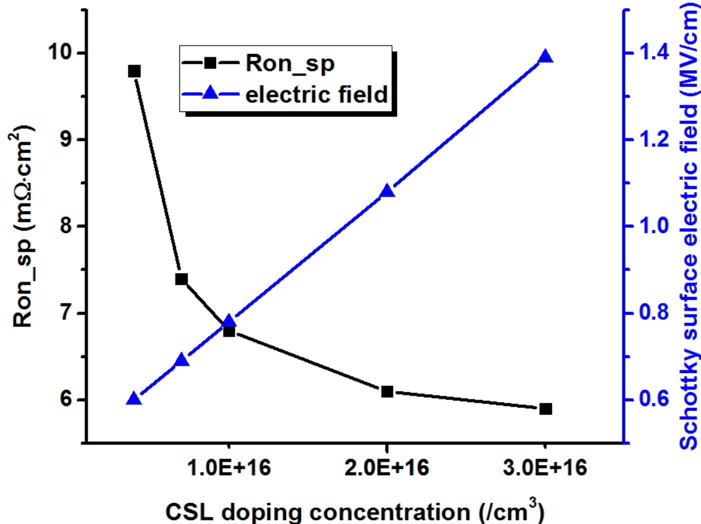


Fig. 8.3 The trade-off between R_{on_sp} and the Schottky surface electric field versus the CSL doping concentration

CSL doping is used as another design parameter which affects MOSFET R_{on_sp} and the Schottky surface electric field in the opposite way as shown in Fig. 8.3. Therefore, a trade-off point exists for the optimum CSL doping. It is not difficult to find that a proper CSL doping concentration lies in between $1\times10^{16}cm^{-3}$ and $2\times10^{16}cm^{-3}$ which offers low MOSFET R_{on_sp} and low Schottky contact surface electric field at the same time.

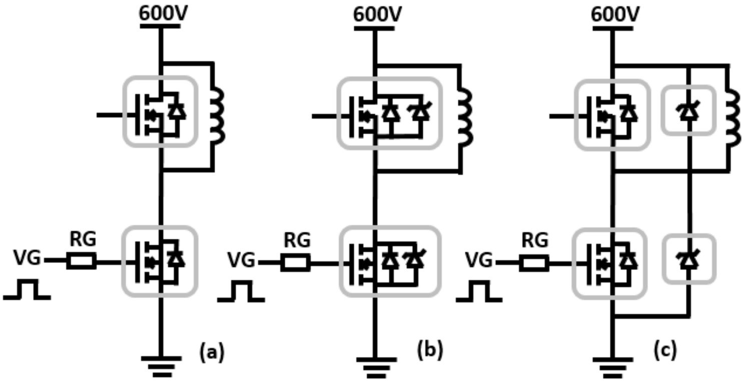


Fig. 8.4 Silvaco mixed mode double pulse simulation circuit for a) conventional UMOS; b) MPS-UMOS; c) conventional UMOS with external SBD

The dynamic performance of the proposed MPS-UMOS structure has been simulated with Silvaco mixed mode tool and compared to the conventional UMOS with and without external Schottky diodes. The mixed mode clamped inductive switching circuit diagram is shown in Fig. 8.4. A standard double pulse setup was used for the characterisation of the MOSFET turn-on and turn-off performance. The high side conventional UMOS in configuration a) uses the body PiN diode for current conduction. Schottky diode either

integrated or externally connected will be used for current conduction for configuration b) and c) as shown in Fig. 8.4. The chip dimension was fixed at 0.1cm^2 for the external Schottky diode, the conventional UMOS and the proposed MPS-UMOS.

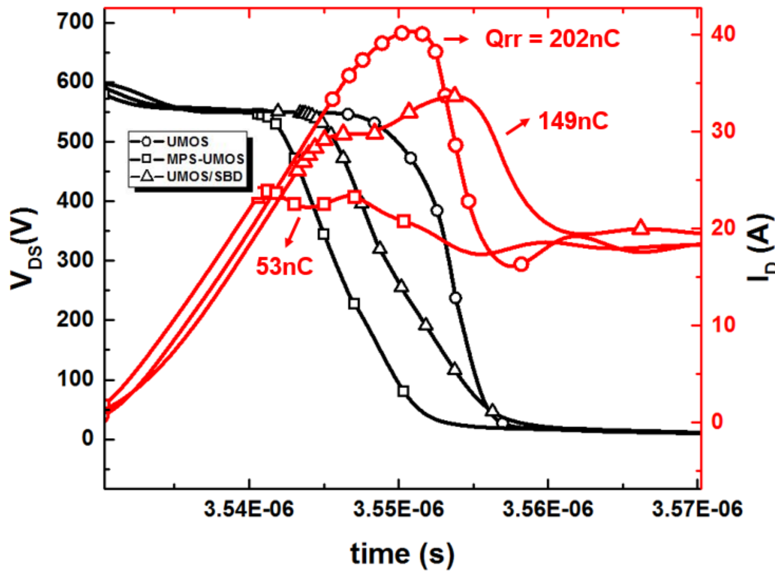


Fig. 8.5 The simulated turn-on switching transient of the low side device with 100ns minority carrier lifetime and R_G = 10Ω

It is shown in Fig. 8.5 that there is significant reverse recovery charge Q_{rr} if the body diode of the conventional UMOS is used for current conduction. The peak recovery current has been suppressed by using the proposed MPS-UMOS as the high side switch since the integrated Schottky diode is responsible for current freewheeling. The UMOS/SBD setup uses an external Schottky diode for current freewheeling which increases the total chip area and hence the capacitive charge resulting in higher turn-on current of the low side switch. The UMOS/SBD setup has higher turn-on loss in comparison to MPS-UMOS since the extra capacitive stored energy needs to be released into the MOSFET for every switching cycle. Since the MOSFET structure is relatively identical, the difference of the MOSFET conduction losses can be ignored.

In the mixed mode simulation, the minority carrier lifetime (τ) was varied to investigate the influence on the switching losses. The minority carrier lifetime does not affect MPS-UMOS or UMOS/SBD configurations since the Schottky diode is responsible for current freewheeling instead of the body PiN diode. The simulation results are presented in Fig. 8.6 and the minority carrier lifetime has been varied from 10ns to 1μs. The switching loss of the conventional UMOS is similar to the proposed MPS-UMOS and the UMOS/SBD

setup if the minority carrier lifetime is reduced to 10ns. However, the switching power loss for the conventional UMOS increases significantly if the lifetime is increased to 1μs. The minority carrier lifetime can be even higher than 1μs if no lifetime reduction is carried out on the material.

If the MOSFET body diode is used for normal forward conduction, the conduction power loss can be much higher than Schottky diode due to approximately 4V turn on voltage. Under some circumstance, the body diode only needs to be activated for a short amount of time before the current being directed into the MOSFET channel which is called "synchronous rectification". In this case, it seems that Schottky diodes are not necessary if the dead time can be minimised [11]. Although for many commercial SiC MOSFETs, the reverse recovery performance of the body diode is like the SiC Schottky diode, it does have a temperature dependence. When the temperature is raised from 25°C to 150°C, the reverse recovery charge for the body diode can increase dramatically depending on the forward current level and the current slope di_{DS}/dt [12].

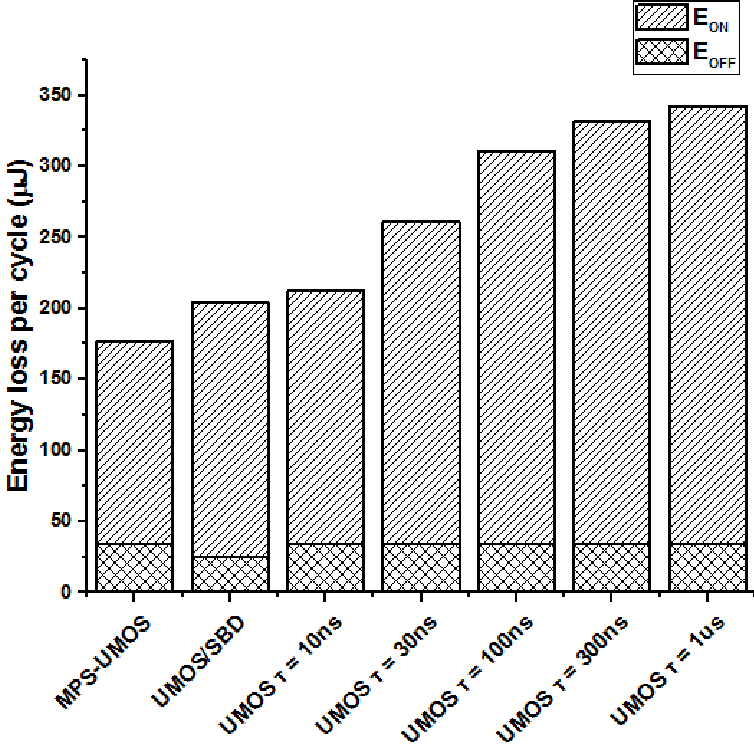


Fig. 8.6 Switching power losses of the low-side MOSFET with various configurations

Although the MPS-UMOS offers great benefits compared to the conventional UMOS devices, there are some disadvantages for this design. Two extra fabrication steps will be needed which includes gate material etching and Schottky contact formation, there is also

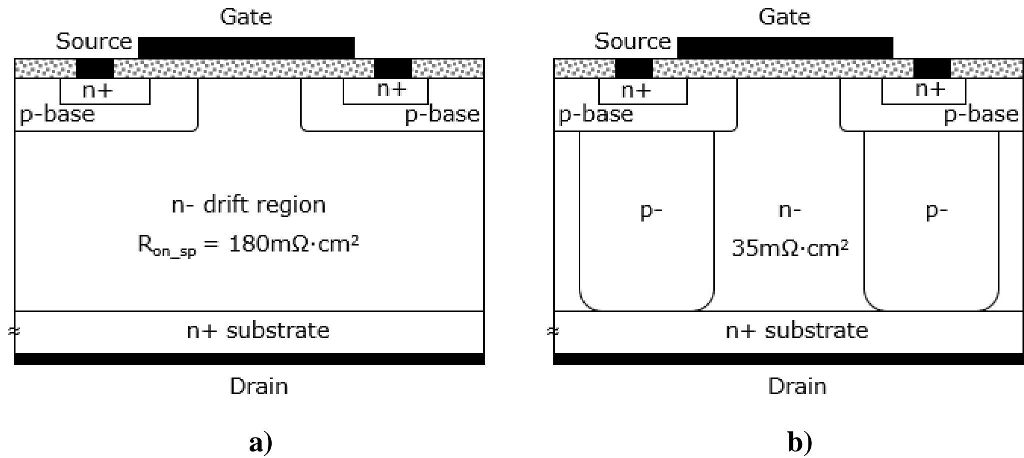
reliability concerns about the MPS-UMOS design since the device structure is relatively complicated.

To summarise, the proposed MPS-UMOS structure reduces switching power loss in comparison to the conventional UMOS with the body PiN diode as freewheeling diode. The suppression of the reverse recovery current can be achieved using the embedded Schottky diode in the MOSFET. In the proposed design, a high-level integration is achieved since the existing p+ implanted region in the MOSFET structure is used to form the merged-PiN Schottky diode. In general, the concept of Schottky contact integration should become more popular in the near future since it brings great system benefit by adding only a slightly more complexity into the device fabrication process.

8.2 SiC Superjunction MOSFET with trench sidewall implanted p-pillar

8.2.1 Background

Superjunction is the only available concept to break the well-known but not entirely correct theoretical limits of silicon devices. The schematic of the classic CoolMOS is shown in Fig. 8.7 which was the first commercial product that uses superjunction technology [6].



a) b)
Fig. 8.7 Cross section of a) a standard 600V vertical MOSFET; b) a 600V CoolMOS

The old theoretical limit of silicon material is normally calculated assuming the depletion region expands in only one dimension in the n- epilayer which is the vertical direction for a vertical device. By introducing the p-pillars into the n- epilayer, the depletion region expands in two dimensions for a superjunction structure and therefore the drift region is depleted efficiently with roughly identical electric field across the whole drift region. As a result, the blocking voltage is determined only by the drift region thickness and independent of the doping concentration allowing the drift region with higher doping concentration to be used. The blocking voltage of a conventional MOSFET is however determined by the n- drift region doping concentration and thickness. The CoolMOS specific on-resistance was reduced by a factor of 5 compared to the standard MOSFET rated at the same voltage [6].

Two methods are commonly used to fabricate superjunction devices which are the multiepitaxy growth and the trench sidewall epitaxy growth as illustrated in Fig. 8.8 and Fig. 8.9. Multiepitaxy method allows the individual doping control over each epitaxial layer and the trench filling method produces a smooth p-pillar which requires precise control of the process [7].

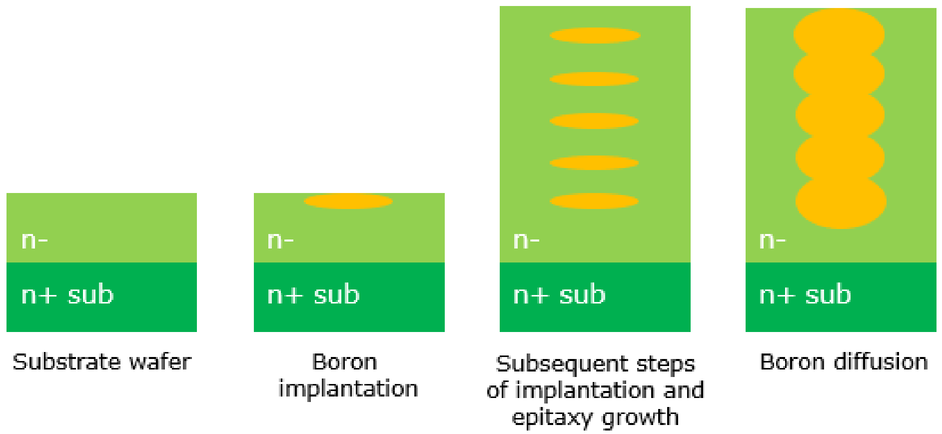


Fig. 8.8 Typical multiepitaxy process flow for superjunction device fabrication

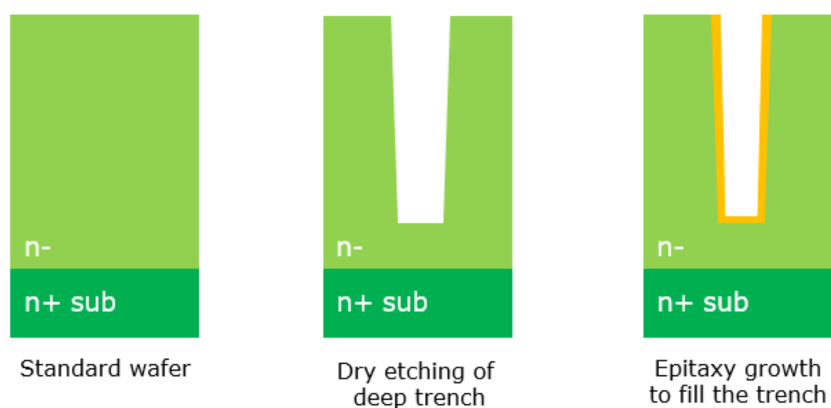


Fig. 8.9 Typical epitaxial deep trench filling process flow for superjunction device fabrication

8.2.2 Feasibility study of 3.3kV-class SiC superjunction MOSFET

The superjunction concept can also be applied to silicon carbide which can further enhance the performance of SiC devices. The low impurity diffusion rates in silicon carbide makes it difficult and expensive to use the multiepitaxy process since more implantation and epitaxy steps will be needed. Therefore, majority of the work have focused on the deep trench filling process. A 25μm deep trench was epitaxially filled successfully which suggested that the crystal orientation is critical for the trench filling process [7]. Even if the trench filling process is perfectly controlled, one still need to worry about the doping control on different crystal surface. Overall, more work needs to be done to transfer the popular superjunction concept from silicon to silicon carbide. Despite all the processing difficulties, there is a compromised approach that can be used for the fabrication of SiC superjunction devices using deep trench sidewall implantation instead of epitaxy growth. The process flow is shown in Fig. 8.10.

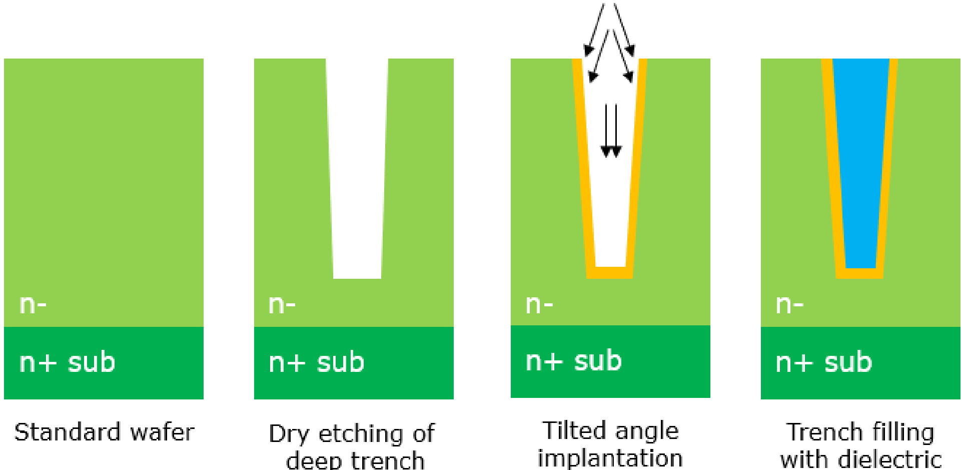


Fig. 8.10 Deep trench sidewall tilted angle implantation process

A SiC superjunction Schottky diode was fabricated successfully with implanted sidewall p-pillar and a maximum breakdown voltage of 1350V was achieved with an epilayer doped at $7\times10^{16}cm^{-3}$ [7]. This section studies the feasibility of SiC superjunction MOSFET fabrication with deep trench sidewall implantation based on simulation.

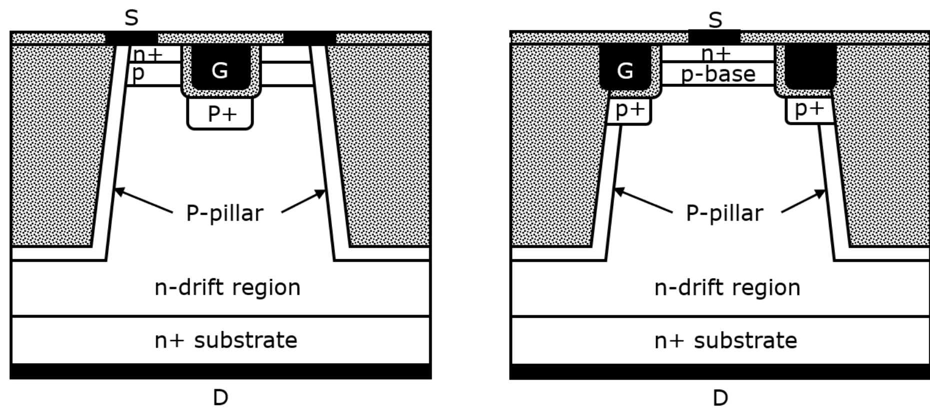
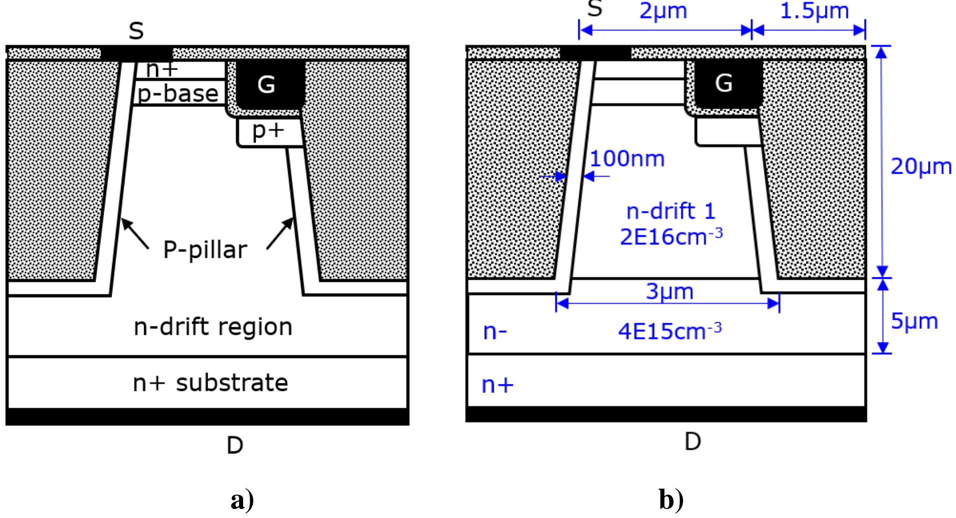


Fig. 8.11 Cross-section of potential superjunction UMOS structures

Since a deep trench with high aspect ratio is normally required to keep the cell pitch small, it increases the difficulty of the tilted angle implantation. As a result, the implanted p-pillar will be shallow and highly doped. Assuming that the n- drift region is doped at $2\times10^{16}cm^{-3}$ with a width of 2μm and the p-pillar width is 100nm, the p-pillar doping concentration has to be approximately $2\times10^{17}cm^{-3}$ or slightly higher to guarantee charge balancing. 2μm n-drift region width is enough for a Schottky diode structure fabricated in [7]. However, it cannot accommodate a MOSFET structure with two electrodes on the top surface. If the drift region width is increased to 4μm, the corresponding p-pillar doping concentration will have to be higher than $4\times10^{17}cm^{3}$ to achieve charge balancing.

The higher concentration of the p-pillar increases the risk of punch through occurring on the trench sidewall as long as the charge balancing is not perfect, and therefore reduces the breakdown voltage. The superjunction UMOS structures presented in Fig. 8.11 requires wide n-drift region, and therefore they are of less interest.

A UMOS design was proposed by Infineon [8,9] which only uses one trench sidewall for current conduction. The MOS channel can be aligned accurately along the $\{11\bar{2}0\}$ crystal plane to achieve the highest channel mobility. The same concept can be applied to the superjunction MOSFET design and the modified drawing of the structure is shown in Fig. 8.12a.



a) **b)**

Fig. 8.12 Cross-section of the proposed SiC superjunction UMOS structure

The width of the n- drift region can be kept small for the proposed superjunction structure. A 3.3kV SiC superjunction UMOS has been studied with simulation. The superjunction structure has been slight modified to add a second drift region below the deep trench which is a lightly doped region as shown in Fig. 8.12b. The p-pillar doping concentration is the only variable in the simulation. The breakdown voltage is plotted against the p-pillar doping concentration as shown in Fig. 8.13. A maximum breakdown voltage of 4.4kV can be achieved with p-pillar doping concentration at 2.5×10^{17}cm^{-3}, it is unlikely that this optimum balance can be realised in real fabrication process. However, if the target is set above 3.3kV, the process window is acceptable as highlighted in Fig. 8.13.

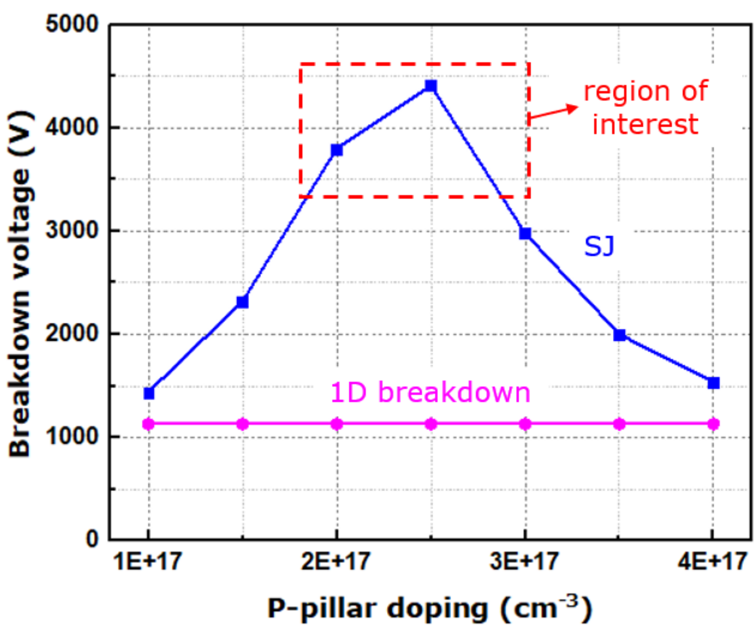
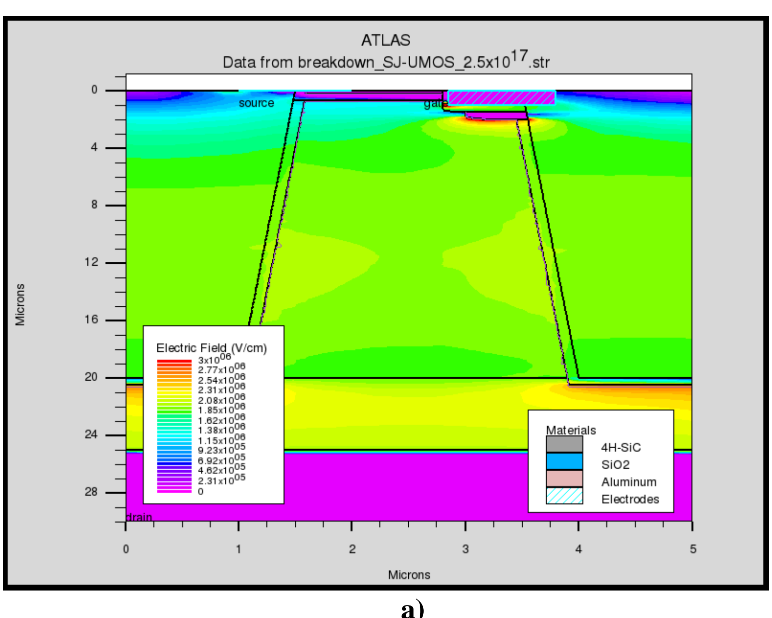
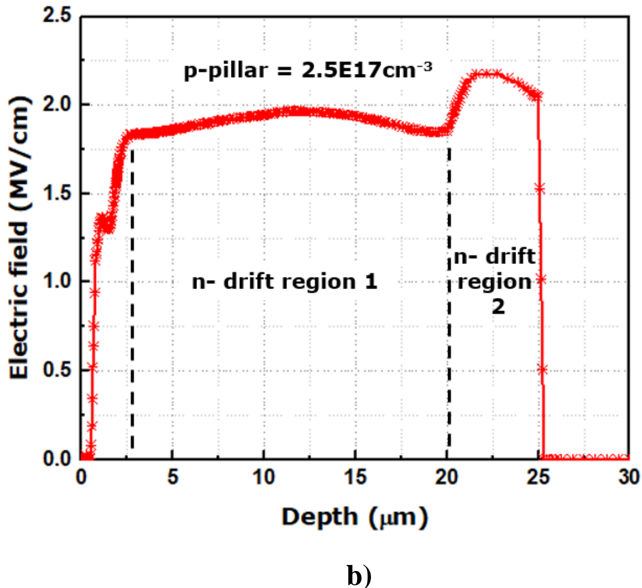


Fig. 8.13 Simulated breakdown of the proposed superjunction UMOS structure



a)



b)

Fig. 8.14 a) Simulated electric field distribution during breakdown; b) the electric field cutline in the centre of the structure

Fig. 8.14 presents the electric field distribution at the breakdown voltage and the electric field cutline in the centre of the structure. The rectangular electric field distribution indicates that the optimum charge balancing has been achieved. The on-state IV characteristics has also been simulated and the result is presented in Fig. 8.15.

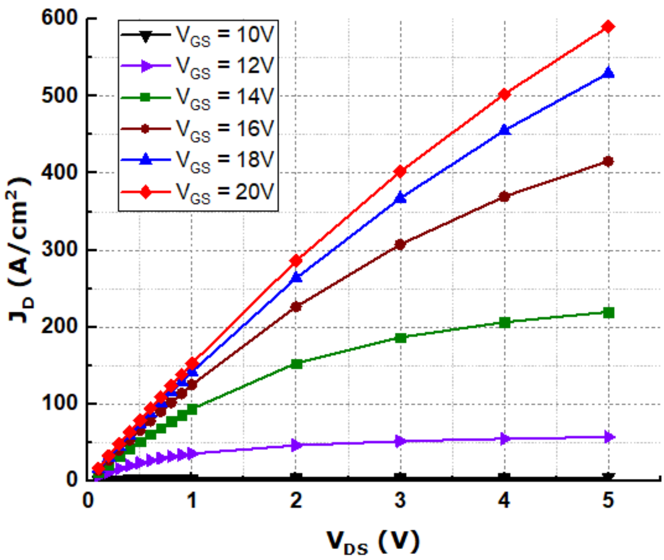


Fig. 8.15 On-state IV characteristics of the superjunction UMOS structure

A specific on-resistance of 7.3mΩ·cm^2 has been extracted from the simulation results. A channel mobility of ~35cm^2/Vs was used in the simulation. A lowest R_{on_sp} of 8.3mΩ·cm^2 was reported in the literature for fabricated 3.3kV class 4H-SiC UMOS [10]. A comparison of the on-resistance distribution is shown in Fig. 8.16.

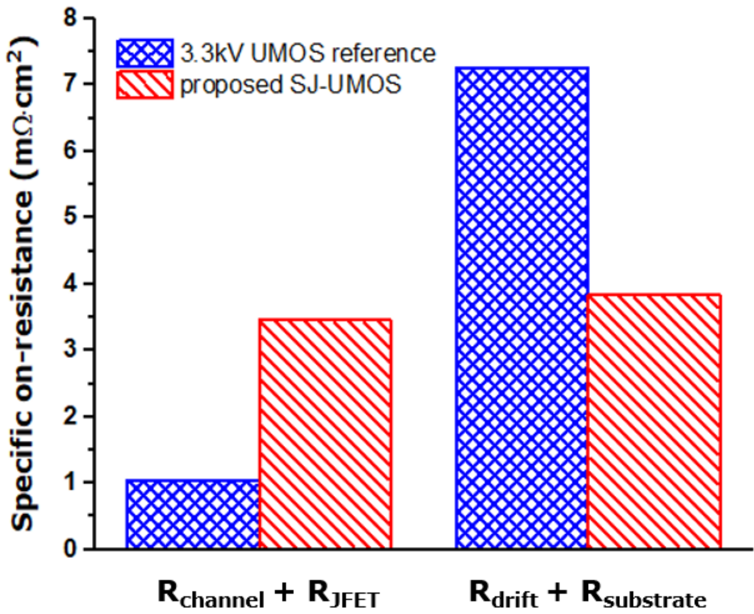


Fig. 8.16 Specific on-resistance benchmarking with published work on 3.3kV UMOS

The specific on-resistance of the drift region is reduced by more than 50% with the superjunction structure. The channel and JFET resistance for the published 3.3kV UMOS is much lower than the simulation results of the superjunction UMOS due to the optimised hexagonal cell layout and maybe higher channel mobility.

With optimised cell layout design and improved channel mobility, superjunction structure can make a significant difference to 3.3kV class SiC MOSFETs. Superjunction technology has great potential for SiC MOSFETs rated at even higher voltages, however, the fabrication process will be more difficult for this implanted trench sidewall method.

8.3 Summary

This chapter has discussed two device concepts that have the great potential to improve SiC UMOSFET performance. Integration of Schottky diode into MOSFET structure saves large chip area by only adding one or two fabrication steps into the standard MOSFET processes. The device level integration can also bring benefits to the system design with less chip count and higher power density. The superjunction technology was a saviour for Si devices, and it will play an important role for SiC devices in the near future which is specifically true for high voltage devices.

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Chapter 9 Conclusion and Future Work

In this final chapter, the conclusions on the conducted research work in this thesis are provided. The future work on 4H-SiC MOSFET design and fabrication are listed mainly into three categories including on-state optimisation, Schottky contact integration and superjunction structure.

9.1 Conclusions

The conducted research work presented in this thesis has focused on 4H-SiC trench MOSFET design and fabrication as well as the 10kV termination design. A MOSFET with the trench gate structure takes the full advantage of the high channel mobility on the $\{11\bar{2}0\}$ plane, which is critical for lower voltage devices (<3.3kV). If the fabrication process is not optimised, the channel resistance can contribute a significant part in the total R_{on_sp} even for a 3.3kV-class device. Therefore, design optimisation of the trench MOSFET structure is critical.

The MOS interface properties have been studied in Chapter 3 using fabricated MOS capacitors and lateral MOSFETs. The maximum channel mobility achieved is approximately 65cm^2/Vs by P_2O_5 post-oxidation annealing, however, this interface treatment can also cause the instability of the threshold voltage and therefore it has not been used for the rest of the device fabrication work in this thesis. Instead, N_2O treatment was mainly used for the interface passivation and channel mobility enhancement. It was found that 1300ºC is the most effective reaction temperature for N_2O to passivate 4H-SiC/SiO_2 interface since the highest mobility of 17cm^2/Vs can be achieved at this temperature. This mobility is lower than the published work within other research groups, it is highly possible that the full potential of the N_2O treatment has not been exploited due to the low gas flow rate limited by the equipment.

Chapter 4 has focused on the development of the dry etching process which is one of the most critical processing steps for 4H-SiC trench MOSFET. A poor trench structure with rough sidewall and micro-trenches can severely degrade the performance of the trench MOSFET leading to early breakdown and reliability issues. A systematic study of the dry etching process using Al_2O_3 mask was conducted and the optimised recipe was developed successfully which produces a micro-trench free structure. The trench corner rounding process has also been discussed in this chapter.

The 1st and 2nd generation trench MOSFET design and fabrication processes are presented in Chapter 5 and Chapter 6 respectively. The target of the 1st generation design was to validate the process flow using the dry etching recipe developed in Chapter 4. A breakdown voltage up to 1600V was achieved successfully for the 1st generation devices with the floating field rings termination. A high-resolution photolithography process (1~2μm) has been developed to address the encountered fabrication difficulties for the floating field rings. The poor on-state performance of these devices was caused by the implanted p+ shielding region below the gate trench structure fabricated with self-alignment process. This parasitic JFET has resulted in a high turn-on voltage for the 1st generation devices. The 2nd generation device was designed to mitigate the parasitic JFET effect and hence improve the on-state performance of the trench devices.

The 2nd generation design has introduced the CSL layer and the p+ implantation clearance “s” and a trade-off decision (CSL doping at $2\times10^{16}cm^{-3}$ and “s” = 200nm) was made based on the simulation results. The design target has been achieved and the parasitic JFET induced high turn-on voltage has been eliminated successfully as shown in Fig. 6.16. There is still a process issue since all the devices fabricated on the 2cm×2cm chip including lateral MOSFETs have experienced extremely low current density. It is believed that there might be some mistakes during the implantation step which should be responsible for the low current issue on the 2cm×2cm chip, however, the specific cause has still not been defined. As a result, the further process optimisation is necessary to keep consistency between different batches of samples. There is another key feature in the 2nd generation design which is the integration of the Schottky contact in the edge termination region. With embedded Schottky contact, the total chip area consumption is reduced compared to externally connected Schottky diode and it also reduces the total chip count in a system level. The fabricated device is only for the demonstration of the

concept, further optimisation of the Schottky diode is necessary. The device rating for the MOSFET and the embedded Schottky diode must match perfectly for the optimum performance.

Chapter 7 presents the design and fabrication process for the 10kV DMOSFET. At this voltage level, the channel resistance is not significant compared to the drift region resistance, therefore, a trench gate structure is not necessary. A comparison between the FFR and JTEs termination structure has been made. For this voltage level, the FFR termination can consume a large chip area (500µm~700µm) without adding any extra implantation steps. A multi-section FFR structure seems to be the most effective option in terms of the chip area and the simulated breakdown voltage. A triple-zone JTE is another option which has been investigated and it consumes much less chip area (300µm). In the meantime, a wide implantation process window has been achieved based on the simulation result shown in Fig. 7.14. The disadvantage of the tripe-zone JTE of course is the three extra implantation steps. The multi-section FFR option was selected for the 10kV DMOSFET fabrication. A maximum breakdown voltage of 13.6kV has been achieved which agrees well to the simulation results. A mistake on the JFET length has led to the poor on-state performance which needs to be optimised for the next generation.

Proposed novel device structures are included in Chapter 8 which includes trench MOSFET structure with integrated Schottky diode and 3.3kV superjunction trench MOSFET design. This chapter is purely based on simulation, and the trench MOSFET with integrated Schottky diode concept has been published in IET Electronics Letter. Superjunction structure has a great potential for SiC devices rated at above 3.3kV. The proposed design uses implanted p-pillar with a trench gate structure which combines the benefits of low channel resistance and low drift region resistance.

9.2 Future work

The future work can mainly be separated into four categories including the on-state optimisation of the 1.2kV trench MOSFET, optimisation of the Schottky embedded MOSFET structure, on-state and off-state optimisation of the 10kV DMOSFET and process development for the 3.3kV superjunction trench MOSFET.

For the 1.2kV trench MOSFET, the further optimisation should mainly focus on the channel region. Each process parameters like gate oxide thickness, threshold voltage and the p-base doping concentration must be optimised in order to achieve higher current density.

For the trench MOSFET structure with integrated Schottky diode, it is necessary to optimise the design and fabrication process for the Schottky diode to achieve lower leakage current without comprising the on-state performance. The Schottky contact can either be integrated in the edge termination region or the active region, design splits can be used to explore all these possibilities.

On-state optimisation is required for the 10kV DMOSFET. Schottky diode integration into the 10kV DMOSFET structure can also be an interesting topic.

Process development is critical for the fabrication of the 3.3kV superjunction trench MOSFET. A 20μm deep trench with high aspect ratio (20:1 ~ 40:1) is required. Filling the trench without void is another challenge to overcome. Once these two processes have been developed, a fabrication trial can be carried out on the 3.3kV superjunction trench MOSFET.

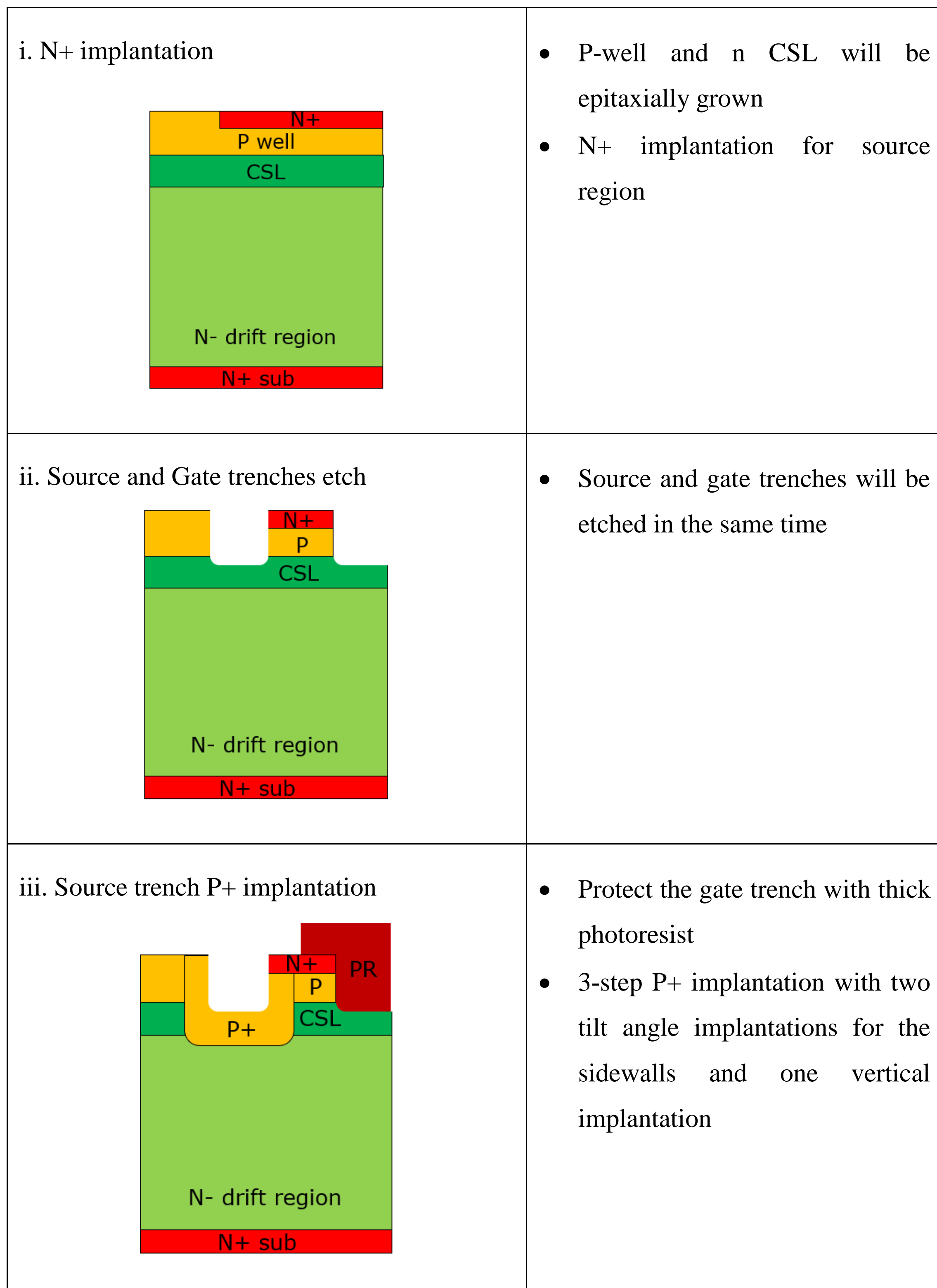
Appendix A.

```
# TCAD Silvaco code for 10kV MOSFET in Chapter 7

go atlas simflags="-128 -p 32"

mesh infile=JFET1.str

intdefects tfile=sicex03.dat numa=24 numd=24 continuous \

        ega=0.805 egd=0.805 nga=1e10 wga=1 wgd=1 \

        nta=6e13 ntd=6e13 wta=0.1 wtd=0.1

# Band parameters

material material=4H-SiC bgn.n=1.0E17 bgn.e=2.0E-2 bgn.c=0.5 \

       gcb=2 edb=0.065 gvb=4 eab=0.191 eg300=3.26 egalpha=3.30E-2 \

       egbeta=1.0E5  nc300=1.83e19  nv300=1.86e19 affinity=3.7

# SRH

material material=4H-SiC etrap=0.0  an=1 bn=0 cn=1 en=0.3 taun0=5.0E-7 nsrhn=3e+17 \

        taup0=1E-7  nsrhp=3e17  ap=1 bp=0 cp=1 ep=0.3

# Auger

material material=4H-SiC augn=5E-31  augp=2E-31

#impact

impact aniso sic4h0001 e.side

# Permittivity

material material=4H-SiC permitti=9.76

# Constant mobilities

mobility material=4H-SiC mun=900.0 tmun=2 mup=124.0 tmup=2

# Analytic model

mobility material=4H-SiC mu1n.caug=40  alphan.caug=-0.5 mu2n.caug=947 \

       betan.caug=-2.4 gamman.caug=0  deltan.caug=0.61 ncritn.caug=1.94e17 \
```

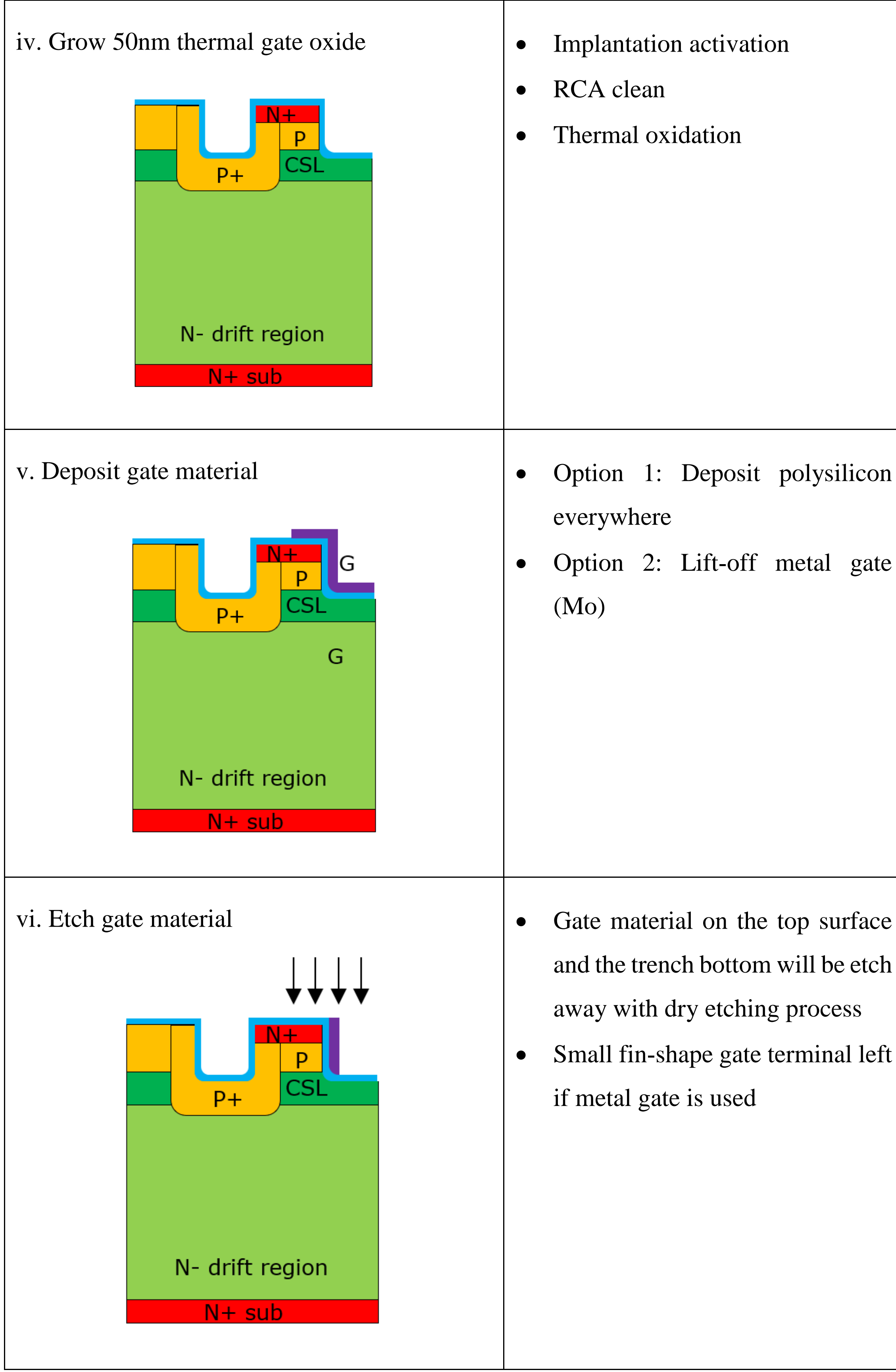
```
        mu1p.caug=15.9  alphap.caug=-0.5  mu2p.caug=124  betap.caug=-2.15 \
        gammap.caug=0  deltap.caug=0.34  ncritp.caug=1.76e19
# fldmob parameters
mobility material=4H-SiC vsatn=2E7 betan=0.9 vsatp=2E7 betap=0.9
#CVT model
mobility material=4h-SiC bn.cvt=7.82e7  cn.cvt=4.431e5 taun.cvt=0.284  \
        dn.cvt=1.237 en.cvt=1.239 \
            feln.cvt=1e70 kn.cvt=2 deln.cvt=5.82e14
models CVT analytic fldmob srh incomplete BGN  auger print fermi optr
method  climit=1e-10  itlimit=15  ir.tol=1e-10  ix.tol=1e-10  pr.tol=1e-10  px.tol=1e-10
cr.tol=1e-10 cx.tol=1e-10
output TAURN TAURP  TRAPS qfn qfp con.band val.band E.LINES E.VELOCITY \
       EX.VELOCITY  EY.VELOCITY  FLOWLINES  HX.VELOCITY  H.VELOCITY
HY.VELOCITY e.mobility
solve    init
solve    prev
solve prev vfinal=20 vstep=1 name=gate
log outf=JFET1_onstate.log
solve prev vfinal=1 vstep=0.1 name=drain
solve prev vfinal=10 vstep=1 name=drain
save outf=JFET1_onstate.str
tonyplot JFET1_onstate.log
```

Appendix B.

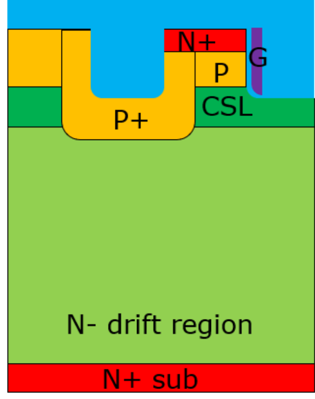
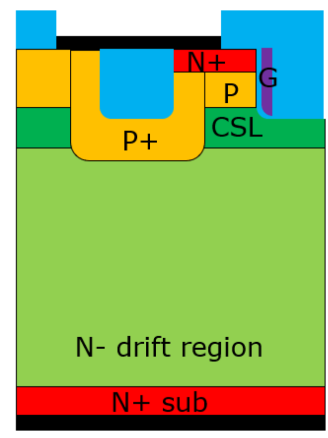
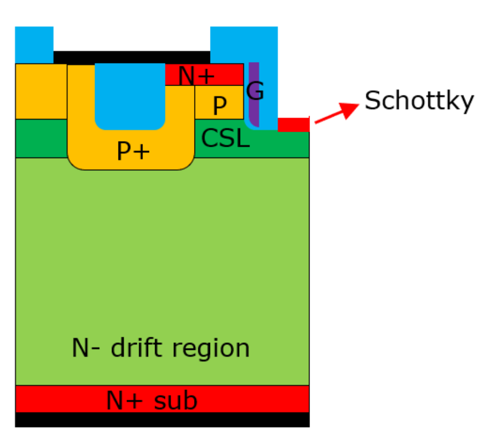
The process flow for the proposed MPS-UMOS structure in Chapter 8.

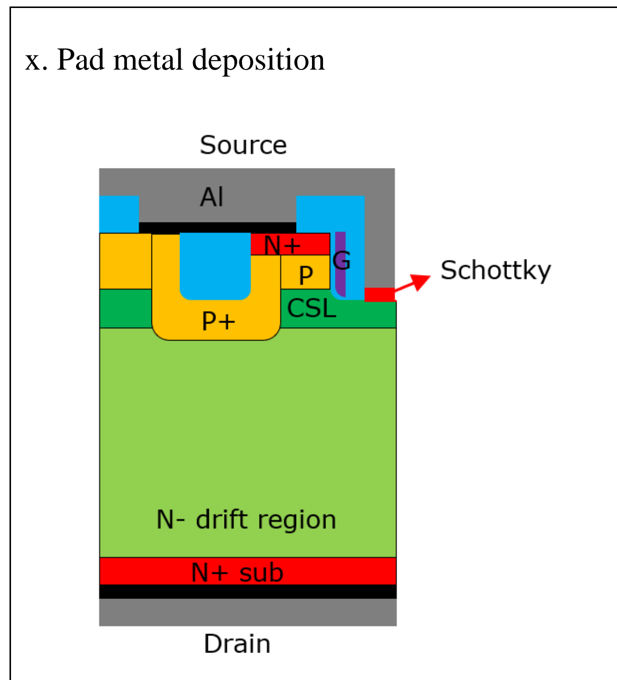


i. N+ implantation	• P-well and n CSL will be epitaxially grown • N+ implantation for source region
ii. Source and Gate trenches etch	• Source and gate trenches will be etched in the same time
iii. Source trench P+ implantation	• Protect the gate trench with thick photoresist • 3-step P+ implantation with two tilt angle implantations for the sidewalls and one vertical implantation



iv. Grow 50nm thermal gate oxide	• Implantation activation • RCA clean • Thermal oxidation
v. Deposit gate material	• Option 1: Deposit polysilicon everywhere • Option 2: Lift-off metal gate (Mo)
vi. Etch gate material	• Gate material on the top surface and the trench bottom will be etch away with dry etching process • Small fin-shape gate terminal left if metal gate is used

vii. Deposit metal interlayer (TEOS) 	• Deposit 2µm TEOS and densify it at 1000ºC for 2min in Ar
viii. Source and drain ohmic contact formation 	• Open the TEOS window • Dry etch down to SiC surface • Deposit Ti/Ni and lift-off • Deposit Ti/Ni on the backside • 1000ºC 2min RTA annealing to form ohmic contact
ix. Schottky contact formation 	• Open the TEOS window in the gate trench • Dry etch to SiC surface on the bottom of the gate trench • Deposit Mo and lift-off • 500~600ºC 2min to form Schottky contact

x. Pad metal deposition 	• Deposit thick Al pad metal on the top surface and lift off • Deposit thick Al pad metal on the backside • Polyimide deposition