Modelling, Simulation and Control of Photovoltaic Converter Systems

by

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SYNOPSIS

The thesis follows the development of an advanced solar photovoltaic power conversion system from first principles. It is divided into five parts.

The first section shows the development of a circuit-based simulation model of a photovoltaic (PV) cell within the 'SABER' simulator environment. Although simulation models for photovoltaic cells are available these are usually application specific, mathematically intensive and not suited to the development of power electronics. The model derived within the thesis is a circuit-based model that makes use of a series of current/voltage data sets taken from an actual cell in order to define the relationships between the cell double-exponential model parameters and the environmental parameters of temperature and irradiance. Resulting expressions define a 'black box' model, and the power electronics designer may simply specify values of temperature and irradiance to the model, and the simulated electrical connections to the cell provide the appropriate I/V characteristic.

The second section deals with the development of a simulation model of an advanced PV-aware DC-DC converter system. This differs from the conventional in that by using an embedded maximum power tracking system within a conventional linear feedback control arrangement it addresses the problem of loads which may not require the level of power available at the maximum power point, but is also able to drive loads which consistently require a maximum power feed such as a grid-coupled inverter.

The third section details a low-power implementation of the above system in hardware. This shows the viability of the new, fast embedded maximum power tracking system and also the advantages of the system in terms of speed and response time over conventional systems.

The fourth section builds upon the simulation model developed in the second section by adding an inverter allowing AC loads (including a utility) to be driven. The complete system is simulated and a set of results obtained showing that the system is a usable one.

The final section describes the construction and analysis of a complete system in hardware (c. 500W) and identifies the suitability of the system to appropriate applications.

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List of principal symbols and their definitions

arb - Arbitrary units of irradiance proportional to W/m^2

C_r - Resonant circuit capacitor

Double-exponential model parameters used in PV cell modelling (section 2):

- I_{ph} - Photocurrent
- I_{s1} - First saturation current (zero for single-exponential model)
- I_{s2} - Second saturation current
- A - 'Diode quality' parameter (fixed at 2 for double-exponential model)
- R_s - Series resistance
- R_p - Parllel resistance

δ - Inverter duty cycle defined as t_{on}/T_s where T_s is the switching period. If used in conjunction with Δ refers to the 'small signal' perturbations in δ

Δ - Large-signal duty cycle in the steady state. Used in reference to control algorithms which drive PWM modulators

δ_f - Delta-filter operator. Essentially an accumulation defined by $\delta_f = z-1$

DSP - Digital signal processor

E - Irradiance upon a solar array, often measured in W/m^2

e - Electronic charge (1.6×10^{-19} coulombs)

G_i, K_i - Current loop proportional-integral controller parameters in the form $G_i(s+K_i)/s$

G_v, K_v - Voltage loop proportional-integral conroller parameters in the form $G_v(s+K_v)/s$

I - current

I_{avg} - Average inductor or diode current

I_d - diode current

I_L - inductor current

I_{mpp} - Photovoltaic array currrent at the maximum power point

I_{out} - Output current

I_{sc}	-	photovoltaic array short circuit current
k	-	Boltzmann's constant (1.38×10^{-23} J/K)
K_0-K_{12}	-	Thirteen constants in equations relating irradiance and temperature to double exponential model parameters
L_r	-	resonant circuit inductor
N_p	-	number of series chains of cells in parallel in a photovoltaic array
N_s	-	number of cells in a single series chain in a photovoltaic array
P_{out}	-	output power
PV	-	photovoltaic
PWM	-	pulse-width modulation.
T	-	absolute temperature (kelvin)
T_s	-	switching period
V	-	voltage
V_{oc}	-	open circuit voltage of a photovoltaic array
V_{mpp}	-	voltage of a photovoltaic array at the maximum power point
V_{out}	-	output voltage
V_{peak}	-	peak voltage

SECTION 1: INTRODUCTION

1.1 Introduction to this thesis

This section provides an overview of research in solar photovoltaic (PV) power conversion systems.

From the start it was decided that the research should be confined to power electronics, that is the energy conversion systems as opposed to the design, development and optimization of PV cells and arrays. The research therefore took place with a view to improving the power electronics technology present in PV conversion systems. Computer simulation figured extensively in the research as a means to verify the performance of circuits and control strategies and to determine whether the proposed system would be worth implementing in hardware. As such a description of the various computer simulation and modelling tools used in the project is given in this section.

1.2 Solar power - an introduction

Solar power falls largely into two categories, namely solar thermal systems and solar photovoltaic power systems. Solar thermal systems rely upon the use of energy from the sun to generate heat, often to heat water. Electricity is seldom used as a means of transporting energy in such systems. Solar photovoltaic power relies on the conversion of the sun's energy directly into electricity by means of a p-n junction. Polycrystalline and amorphous silicon are currently the most frequently used materials in which the junction is created. Photons provide electrons with sufficient energy to cross the band-gap and develop a voltage across the terminals. A single cell provides very low current and voltages, so to provide sufficient power for an application cells are

connected in series and parallel chains to form a solar array in order to build up the required amount of current and voltage.

The current and the voltage available from such a cell, however, is not constant. There are two environmental parameters which affect it. Firstly the level of irradiance of solar light, often given the symbol 'E' and measured in watts/m^2, will clearly directly affect the level of energy obtainable from the cell. The temperature of the cell itself will also significantly affect the characteristics - it is well known that the characteristic of a p-n junction is variant with respect to temperature and the solar cell is no different.

The net effect of this variation in the characteristics is that for every given value of solar irradiance and cell temperature there will be a unique cell characteristic. The total array power available will thus vary. Solar irradiance varies with the position of the sun in the sky, the passage of clouds, flying objects and so on while the array temperature will also vary with ambient temperature. In addition most PV cells are dark in colour which means that they will absorb heat from the sun adding a further dimension of variability.

Finally, the characteristic of a p-n junction is such that the photovoltaic array does not appear as a pure voltage source. If, for example, the array terminals were to be short-circuited in conditions of high irradiance, this would not result in the destruction of the array. The array would continue to pass a high current into the short circuit (at zero terminal voltage). In the open circuit condition a voltage will appear across the terminals, the value of which is largely dependent upon temperature. Such a characteristic, which can drive what is effectively zero power loads at both open and short circuit, must have an optimum point between the two conditions at which the power drawn from the array is at a maximum. PV cells do indeed demonstrate this characteristic. **Figure 1** shows a sample PV current /voltage (I/V) characteristic curve and **Figure 2** a power curve from a sample cell and serves to demonstrate this. Such a characteristic is possessed of two major disadvantages. Firstly, the maximum power point lies within the normal operating region of the array, and this point moves with irradiance and temperature. This can pose a problem for possible converter control schemes which conventionally rely on 'stiff' supplies. Secondly the

array can provide a continuous current into a short circuit - this could conceivably be a safety hazard as the characteristic indicates that a solar array could easily sustain an arc in such a condition.

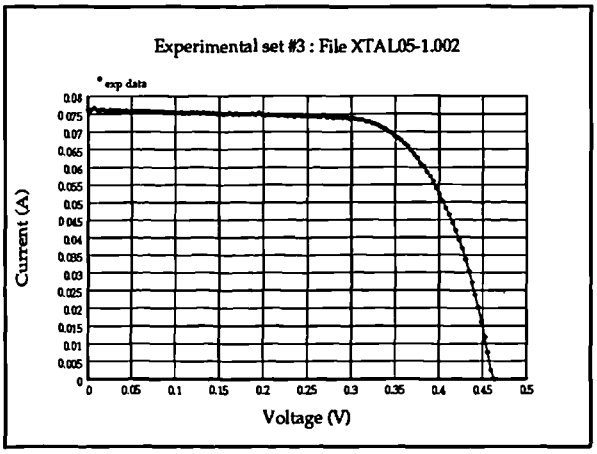

Figure 1 Sample PV characteristic curve.

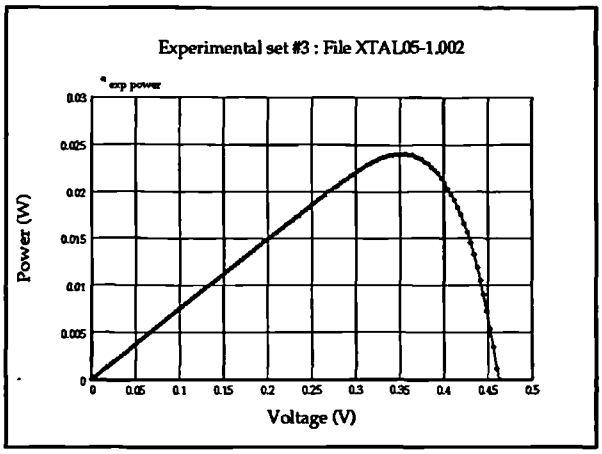

Figure 2 Sample PV power curve.

A solar photovoltaic power conversion system must therefore take into account the characteristic of the power source as well as those of the load. Such a system requires control algorithms which are quite different to those required by an offline power supply, for example, which has the low-impedance mains as a source.

1.3 Computer simulation philosophy

Computer simulation was used extensively in the analysis and development of converter systems during this research. It was intended that the simulation be used as a means to verify that the power electronic circuits and control systems proposed during the course of the research were worth implementing as prototypes in hardware.

1.3.1 Simulation environment

The circuit-level simulator used in this research was SABER [1], a UNIX workstation-based simulator package with a series of model libraries ideally suited to power electronics. These models, known as templates, are written in a C-like modelling language known as MAST. MAST supports floating-point operations, state machines, and most trigonometric functions as well as

an integration function essential to dynamic simulation. The basic simulator is general purpose, and it is possible to write MAST templates to simulate anything, providing the characteristics are known. A schematic-capture utility, DesignStar, is available to Saber as a front-end. Symbols referencing new MAST templates may be produced for DesignStar in order to facilitate seamless simulation of a system from its schematic description..

The choice of SABER was based largely upon its immediate availability, its extreme ease of use and also the availablility of template libraries containing models for most common power electronics components. The use of schematic capture entry together with a fast workstation platform upon which to run SABER also aids in providing an environment conducive to the rapid input, simulation and analysis of systems to be tested.

1.3.2 Additional computer simulation systems used

For some of the mathematical-based simulations MATLAB [2] was used. This package, effectively a matrix-algebra library with a very powerful front-end and graph plotting features added, was used extensively during the development of the control algorithms as it is for this type of work that MATLAB is optimized. MATLAB was available on both workstations and IBM PC compatibles, and formed a very useful companion to SABER throughout the research for some of the more mathematically based analyses.

1.4 Current developments and how this research enhances them

The field of solar photovoltaic converter systems is quite broad, with many different applications and converter types. It was intended that this research should target the area which is underdeveloped but also may be seen as having potential. To this end a study of existing work was carrried out in order to determine the types of conversion systems that were currently in use and make an attempt to classify them dependent upon their intended application. Once this was carried out it was then decided how the research should proceed.

1.4.1 Converter types and uses

It appears that there are four major categories into which existing systems fit. Firstly, in **category 1**, are the large-scale grid connected systems [3], [4], [5],[6] with power outputs ranging from tens of kilowatts to hundreds of kilowatts. These are usually used in countries where space is plentiful and the climate is conducive to large extended periods of unobstructed sunshine.**Category 2** comprises the remote applications where much smaller photovoltaic plant is used to drive smaller loads such as air conditioning, refrigeration or irrigation pumps in remote areas of the world where, once again, sunshine is in abundance [7], [8], [9]. **Category 3** forms the lower power (c. 2kW) units which are grid connected and are intended for use in residential areas where solar arrays may be mounted on the roof of the dwelling and a zero-maintenance inverter system be placed somewhere out of the way [10], [11]. **Category 4** is a combination of category 2 with other alternative energy systems in a combined alternative energy installation, sometimes including a battery bank to ensure uninterrupted supply [12], [13], [14]. This is done as no alternative energy source is guaranteed to be present all the time (the sun goes down!) and these combined systems provide energy from at least one source most of the time. The power conversion systems in these installations can be slightly more complex than that for a solar installation alone, as each generator unit for each specific form of alternative energy used will have fundamentally different characteristics from the others and often compromises between cost, efficiency and complexity have to be met.

1.4.2 Choice of small-scale solar power systems for this research - the reasoning.

Given the sheer diversity of applications for solar photovoltaic power it appeared prudent to develop an efficient system that was flexible as possible, had no ties to specific array types, makes or models, and was limited only by maximum power throughput (this is purely a function of the devices used in the power-handling stages). Some thought was given to the form of the system, and the applications in which it may find itself. The categories defined in section 1.4.1 can be viewed in terms of the type of load to be driven. There are three such load types: a d.c. load, a 'dead' a.c. load and a live a.c. load (usually a utility distribution system). Categories 1, 3 and 4

more often than not support a utility feed while category 2 systems are stand-alone systems supporting d.c. loads and/or dead a.c. loads. Category 4 systems in certain applications where there is no grid connection can support 'dead' a.c. and d.c. loads.

An examination of the current uses of photovoltaic power show that a large number of application-specific systems have been developed for both category 1 and category 2 applications. Commercial inverter systems are readily available for category 1 applications. Although a number of experimental category 3 power conversion systems have been developed, it appears that there is considerable scope for growth in this area, particularly in temperate climates such as the U.K. where it is often thought that there is insufficient hours of unobstructed solar radiation to make photovoltaic power a viable proposition. Category 4 systems are quite popular here for this reason.

In addition, category 1 systems require a large surface area in which to cover with arrays. Since (as a guide) a mean power of 1GW would require an area of approximately 100km^2 of arrays [15], serious questions then arise relating to the subsequent stability of the soil beneath them - this would in effect be rendered sterile. No plant life would be able to exist below the arrays, and any taller plants reaching above the height of the arrays would 'poach' sunlight from them.

It was decided to consider the following. If a small category 3 PV-only system with a roof-mounted array was installed in an individual domestic dwelling not only would a significant difference be made to the electricity demand from the utility but when the energy demand from the dwelling is lower than that provided by the PV arrays, the excess could be exported back to the utility. In addition, in the presence of sufficient sunlight the converters could be designed in such a manner as to provide the dwelling with a modest amount of power should the utility supply fail. Such conversion systems would be quite small owing to the limits on the size of the arrays, and could be constructed as a low-maintainance unit requiring little intervention from the owner of the dwelling.

It would, however, be possible to implement category 3 systems on a larger scale in the future - as PV arrays become cheaper and more efficient so it could be possible to construct complete housing estates where each house has its own PV arrays and converter system. Such a scheme would go a long way to reducing overall energy demands on the utility.

In the light of this consideration (no pun intended!) it was decided that to develop primarily for category 3 applications would be the most feasible. At these power levels (c. 1-3 kW) the technology required is readily available, not too expensive and within the developmental capabilities of Loughborough University. Category 1 systems could then be developed, if desired, based upon the same techniques scaled up to suit the power levels and employing similar control algorithms.

Further, the research would involve the development of a flexible converter system which could be used in both category 2 and 3 applications by developing a d.c.-d.c converter module and an a.c. inverter section employing a control scheme which is simple to alter to allow either live a.c. loads (a utility connection) or a 'dead' a.c. load (for example an induction motor such as may be used in an irrigation pump). If it is required to drive a d.c. load only the d.c. section of the system is required. The d.c. converter will provide a stable d.c. voltage at a fixed level to all loads at or below the current array maximum power point, eliminating the awkward characteristic of the photovoltaic arrays which would prevent direct connection of such a load (if the load power requirement at the regulated voltage exceeded the maximum power available from the PV array, the converter could be arranged to either shut down or continue to deliver maximum power into the load). Such a control algorithm is not easy to design, and virtually no currently available systems are designed with such loads in mind. The modularity of the system would make for a general-purpose power conversion approach which, if successful, would form the basis for an advanced system. Such a system would effectively combine category 2 and category 3.

In relation to the power electronics and associated control systems, the main requirement is to ensure that the system is efficient. PV arrays are not cheap and therefore to minimize the payback period it is essential not to waste energy in the conversion process. Resistive elements

in the converters must be minimized, and steps taken to minimize dissipative losses in the switching elements. The intention from the start was to implement the control algorithms digitally, using a readily available digital signal processor (DSP) card. The possible complexity of the algorithms and the requirement for a form of adaptive control suggested that the flexibility of a digital implementation would be advantageous.

1.5 Program of research and structure of this thesis.

As it was intended to develop advanced solar photovoltaic conversion systems in simulation before committing the most promising approach to prototype hardware, it became apparent that it would be necessary to develop a simulation model for a PV cell. The analysis of currently available PV modelling techniques and the subsequent development of a model with power electronics development in mind forms section 2 of this thesis.

With a usable circuit-based model of PV cells available within the SABER enviroment attention was turned to the power electronics. Section 3 deals with the development in simulation of a d.c. - d.c. converter capable of providing both a regulated d.c. output into loads requiring less power than PV array maximum power at the regulated voltage, and switching to a maximum power tracking control scheme once the load power requirement exceeds array maximum power allowing output voltage to fluctuate to maintain array maximum power into the load. The use of advanced control algorithms is investigated in order to circumvent problems involved with instability of conventional feedback control in the neighbourhood of the array maximum power point and to ensure smooth operation across the entire converter load characteristic.

Section 4 describes the practical implementation of a low power prototype of the scheme described in section 3. A description of the design of the power circuit, signal conditioning, control circuit and software development is given in detail. Practical results are provided and compared to the simulation results.

Section 5 presents the design and simulation of the add-on inverter section and associated control system. The inverter section includes a novel single-rail to dual-rail resonant converter system to feed the inverter itself from the single output d.c.-d.c. converter. The state of the art predictive current mode control scheme used by the inverter is also presented. The performance of the d.c.-d.c. converter/inverter combination is also investigated in simulation with the solar array model source. A number of different loads were used in the investigation including 'awkward' loads such as those which draw current with a high crest factor, in order to verify the control algorithms.

Section 6 presents the implementation of a complete high-power hardware prototype of the system described in section 5 was constructed. The d.c.-d.c. converter system was virtually unchanged from the low-power test implementation other than in the uprating of the components - even the control algorithm constants were not altered significantly. With the PV array-interactive algorithms tested at low power, and the lack of availability of suitable large-scale array simulators with known, presettable characteristics with which to test at high power, the tests on the front end were simply to determine that it was capable of tracking a maximum power point in the source (provided by a variac and a resistive divider) as well as operate in voltage regulating mode. The inverter block, was tested under all load conditions tested in simulation, including utility feeds and high crest factor loads, Practical results are presented and compared to the simulation results .

Finally, an appraisal and overall summary of the work carried out, together with some recommendations as to the direction in which further work may take are presented in the conclusion in section 7. While not absolutely exhaustive in what is a very broad field, this thesis seeks to present research which was carried out with a view to improving the form and type of power electronics used in photovoltaic power generation, particularly in small to medium scale.

SECTION 2: DEVELOPMENT OF A CIRCUIT-BASED PV CELL MODEL

2.1 Introduction.

In order to be able to develop a complete solar photovoltaic power electronic conversion system in simulation, it is necessary to define a circuit-based simulation model for a PV cell so as to be able to study the interaction between a proposed converter (with its associated control arrangement) and the PV array. To do this it is necessary to approach the modelling process from the perspective of power electronics - that is to define the desired overall model in terms of the manner in which the electrical behaviour of the cell changes with respect to the environmental parameters of temperature and irradiance. This section covers the development of a general model which can be implemented on simulation platforms such as PSPICE or SABER and is designed to be of use to power electronics specialists. The model accepts irradiance and temperature as variable parameters and outputs the I/V characteristic for that particular cell for the above conditions

2.2 Modelling strategy

In order to develop such a model, firstly a data acquisition system was devised to gather PV current-voltage data across a range of temperatures and irradiances. A description is given of the data acquisition system. For each of the data sets a set of double-exponential model parameters were then extracted from the data using specially developed software running on a standard IBM PC compatible. The relationship between double-exponential model parameters and irradiance and temperature was then defined.

It is not difficult to find existing PV array characteristics models ([16], [17], [18]), also the theoretical models based upon the physics of the device are not difficult to come by ([19], [20]). Owing to the fact that physical parameters such as semiconductor doping densities are not readily realized as practical values that remain constant over a production spread, a large amount of published work has been involved with the extraction and analysis of experimental cell characteristic data - this being then fitted to an appropriate model. However, often the work has not given much attention to the physical loads to which such a cell may be connected. Likewise, from the power electronics perspective an interest has developed in the field of maximum power tracking systems, often in relation to battery charging as well as in the area of grid-coupling. This often seems to make little use of circuit-based simulations of photovoltaic arrays in the optimization of the array to converter electrical interface. Such circuit-based models appear to be quite sparse. A large number of current solar photovoltaics modelling systems are often very system-specific and are designed to model a complete photovoltaic installation [16],[17] to aid such calculations as projected global efficiencies over time.

Photovoltaic systems research seems largely to be divided into two, fairly distinct areas; namely array physics, design and optimization, and solar power conversion systems. Better, more efficient converter systems may be developed by matching the control and drive requirements of the converter system to the characteristics of the array. Alternative energy specialists often appear not to have sufficient expertise in power electronics in order to develop advanced converter systems which can match the input characteristic of the power electronic system to those of the array in order to make best use of the array. Examples of such systems can be found in the field of solar array/battery combinations for stand-alone use [7],[8],[10] and in the area of utility interactive systems [3],[4],[5],[7],[8].

A number of powerful component-based electronics simulation systems such as SPICE and SABER have become available over recent years and such systems are often used during the development of power electronics systems. In their basic form they do not provide a circuit model, or a component model, of the solar array itself and thus are difficult to integrate with

current electronics simulation technology used in the generic modelling of PV power electronic systems at a circuit level.

One of the requirements for this program of research aimed at optimizing PV conversion systems is to provide a circuit-based simulation model of a PV array that can be implemented in any circuit-based simulation system such as SABER. Due to the availability of SABER, it was decided from the outset to implement the model using SABER. Such a model did not appear to be readily available, and one was developed to attempt to fill this gap. This model of a PV array will be used in simulation studies of proposed power electronic PV conversion systems.

2.3 Direct mathematical model for a photovoltaic cell.

A mathematical description of the current/voltage terminal characteristic for PV cells has been available for some time. The double-exponential model **(1)** is derived from the physics of the p-n junction and is generally accepted as reflecting the behaviour of such cells, especially those constructed from polycrystalline silicon [18]. This equation gives rise to a curve of the shape shown in **Figure 1**. It is also suggested that cells constructed from amorphous silicon, usually using thick-film deposition techniques do not exhibit as sharp a 'knee' in the curve as do the crystalline types (this is sometimes described as having a lower 'fill' factor - in that the area under the current/voltage curve across the current range of zero to open circuit is less). It is often suggested that the current/voltage model of equation **(2)** provides a better fit to amorphous cells. Equation **(2)** is in effect a subset of the double exponential model effected by setting the second saturation current I_{s1} to zero. Both of these models are implicit and non-linear - therefore determination of an analytical solution is extremely difficult. The parameters are listed below:

$$I=I_{ph}-I_{s1}[e^{\frac{e(V+IR_s)}{kT}}-1]-I_{s2}[e^{\frac{e(V+IR_s)}{AkT}}-1]-\frac{V+IR_s}{R_p} \qquad (1)$$

$$I = I_{ph} - I_s(e^{\frac{e(V+IR_s)}{AkT}} - 1) - \frac{V+IR_s}{R_p} \qquad (2)$$

where:

V: Solar cell terminal voltage

I: Solar cell terminal current

I_{ph}: Photogenerated current (linear with irradiance)

I_{s1}: Saturation current due to diffusion mechanism

I_{s2}: Saturation current due to recombination in space-charge layer

A: 'Diode quality' factor. Variable with cell type for amorphous cells using the single exponential model, but for polycrystalline cells may be set constant to 2 across all cell types. Approximation for Shockley-Read-Hall recombination in the space charge layer [21]

R_s: Cell series resistance

R_p: Cell shunt resistance

Working backwards from the equations, an equivalent circuit can be easily determined and this aids development of the simulation model. This equivalent circuit is shown in **Figure 3.** Simulation systems based upon this electrical model have been used previously [22].

Owing to the nature of these relationships, there lies a problem in determining values for the five double-exponential model parameters which would be representative of those of a physical array system. Although it is not beyond the bounds of possibility to use the device physics to develop expressions for the I/V curve

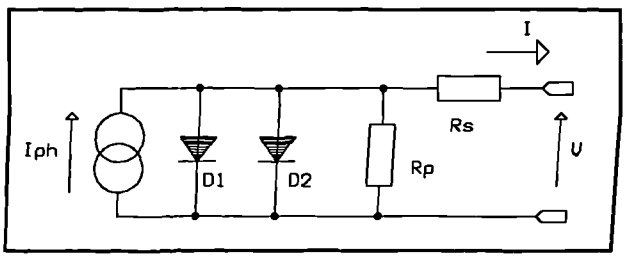

Figure 3 Cell equivalent circuit (double exponential model)

parameters, these would then only be in terms of semiconductor material constants and manufacturing variables such as doping densities. Most semiconductor constants vary quite considerably with production spread, are not provided on a manufacturer's data sheet and are also sometimes quite difficult to determine with accuracy.

The model should behave as a 'black box', in that the power electronics designer may select the desired values of the environmental parameters of irradiance and temperature in order to study the operation of a converter system at either a fixed or a varying point upon the cell characteristics. To this end equation **(1)** is of little use alone. It is necessary to relate the five variable parameters of the equation to the two environmental parameters. The essential modelling requirement may be seen in **Figure 4** and it can be seen to be a two-stage process. Firstly the five parameters of the double-exponential equation must be determined from the cell type and the environmental parameters of irradiance and temperature, and secondly the double exponential current-voltage equation may be solved in order to yield the electrical characteristics of the cell.

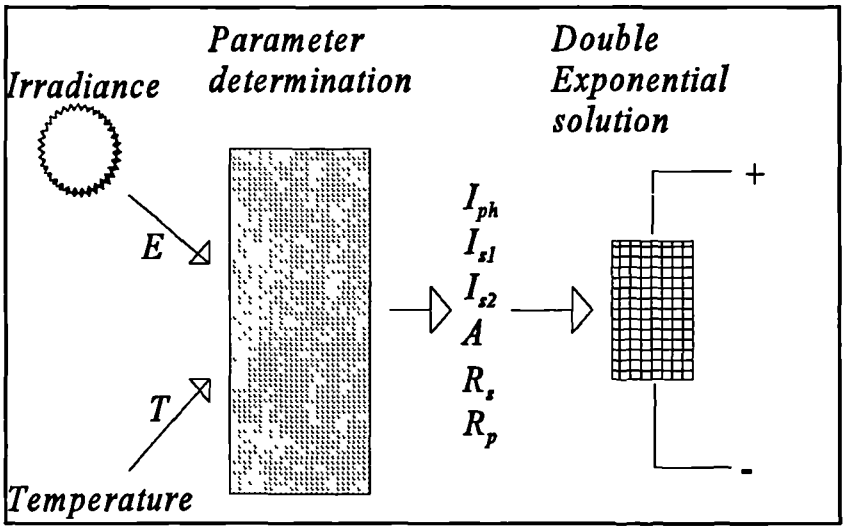

Figure 4 Basic modelling process.

Solution of the double-exponential model equation for current in terms of voltage (or indeed vice-versa) is relatively straightforward once the five parameters are known. These parameters will be different for each cell type, and will vary with the environmental parameters. It is necessary to define the law with which this variation takes place (for a given cell type) in order to complete the model. To do this a set of equations must be defined; the solution of which

will relate each double-exponential model parameter in turn to the current values of irradiance and temperature, possibly incorporating constants which vary according to the specimen of array used.

2.3.1 Double-exponential model parameter variation

Little appears to be known about the variation of the double-exponential equation parameters with respect to irradiance with the exception of the photocurrent, which is known to be linear. However, the temperature variation is relatively simple to define. The general relations of the double exponential model parameters with respect to temperature at a constant level of irradiance can be obtained from p-n junction physics [23] and are shown in equations (3)-(7).

$$I_{ph} = I_{ph(nom)}(1+K_0(T-300)) \tag{3}$$

$$I_{s1} = K_1 T^3 e^{\left(-\frac{eV_g}{kT}\right)} \tag{4}$$

$$I_{s2} = K_2 T^{\frac{3}{2}} e^{\left(-\frac{eV_g}{2kt}\right)} \tag{5}$$

$$R_s = R_{s(nom)}\left[1-K_3(T-300)\right] \tag{6}$$

$$R_p = R_{p(nom)} e^{(-K_4 T)} \tag{7}$$

The constants K_0-K_4 and V_g are specific to a given specimen of cell, while the base parameters $I_{ph(nom)}$,$R_{s(nom)}$ and $R_{p(nom)}$ are values for the parameters at a temperature of 300K. To complete the model it is necessary to modify equations (3)-(7) to take into account the variation of the five paramaters with respect to irradiance. Irradiance and temperature could then be related mathematically to cell current and voltage with no further variables of unknown behaviour being present. In order to define the modifications, it is necessary to analyze aquantity of PV cell

current/voltage data over a range of irradiance and temperature in order to determine the nature of the variation with irradiance. Sections 2.4-2.9 explain how this is carried out.

2.4 Array current-voltage curve measurement.

It is intended to analyze a large quantity of current/voltage (I/V) data from a specimen solar cell across a defined range of irradiances and temperatures. This is in itself a two-stage process. A unique set of double-exponential model parameters must be determined for each experimental I/V data set for a specific cell at a specific value of irradiance and temperature. Once a number of sets of these parameters have been built up across the desired ranges of temperature and irradiance for which it is desired that the model be valid, it is possible to use these data sets to determine the law relating irradiance and temperature to the double-exponential parameters.

To characterize a cell, sufficient data sets across the operating range of the cell must be obtained by measurement. A data acquisition system is required which should rely, if possible upon equipment which is readily available to the power electronics specialist and be relatively quick to use. Such a development would enable a power systems designer to quickly determine the characteristics of a sample of PV array should it be a requirement to develop converter systems in simulation which are to use a specific array. For the purposes of this research a purpose-built data acquisition system as described below was developed which would automate the process to some degree.

2.4.1 PV data acquisition system.

To model a complete array, however large the scale, it is only necessary to characterize a single cell from it, as a simulation model of an array may be constructed from individual cells. To this end an acquisition system used to measure I/V curves need only consider the voltages and currents available from a very small array, or even a single cell, of the type it is desired to characterize. This assists in bringing the voltages and currents down to reasonable levels.

The data acquisition system developed was designed to use a standard IBM PC compatible as the computational core. Software was developed to control the I/V data extraction process and also to automate it to some degree. The additional hardware required to facilitate the measurement was developed in two parts, an acquisition card designed to plug into a standard 8-bit PC expansion slot, and a separate 'pod' containing the analog amplification and signal conditioning circuitry. The pod was developed in such a way that if an array of higher power needs to be characterized, the same software and acquisition card may be used and only the pod needs to be altered. The pod is the only part of the system which may be array-dependent, although it has been designed to be able to characterize most small arrays with a V_{oc} up to 10V and an I_{sc} up to 200mA (limited by the voltages and currents available on the PC expansion bus - if higher voltages and currents are required an external power supply must be used). The pod is range-switchable in software to make optimum use of available headroom, resolution of the analog to digital converters (ADC) and to improve the signal to noise ratio. Commercial data acquisition cards are not cheap, and often display performance figures well in excess of the requirements here - therefore in the interests of cost and convenience a dedicated data acquisition card was designed. This card contains a single-chip four-channel 12-bit ADC, and a single channel 8-bit digital to analog converter (DAC) together with a simple 8-bit digital output port to drive the range-switching. The performance of the prototype system was perfectly adequate for the task of solar cell characterization - the total cost of the card being considerably less than the cost of a commercial PC-based acquisition system which may not have had (in one card) all of the features necessary while having additional features not required for photovoltaic cell characterization.

2.4.1.1 Pod design - an overview

A simplified schematic of the pod is given below in **Figure 5** showing the manner in which the PV cell is driven and monitored. The cell itself is driven from the voltage-source output of one op-amp/transistor combination while the current flowing through it is sensed using the summing junction of the second op-amp/transistor combination. The supply was from the +12V/-5V rails obtained from the PC expansion slot. Two possible voltage ranges were provided. Given that the

DAC on the acquisition card had an output between 0-10V one selectable range was arranged to give a maximum cell voltage of 7V and the other 10V. The change was effected by switching a second resistor in parallel with the resistor R1 in **Figure 5**. Four current ranges are provided for, 0-267 mA, 0-160mA, 0-80mA and 0-40mA by a similar method, using two relays and appropriate value resistors in parallel across R3 in **Figure 5**. The relays were driven from the bottom three bits of the 8-bit digital output port on the acquisition card.

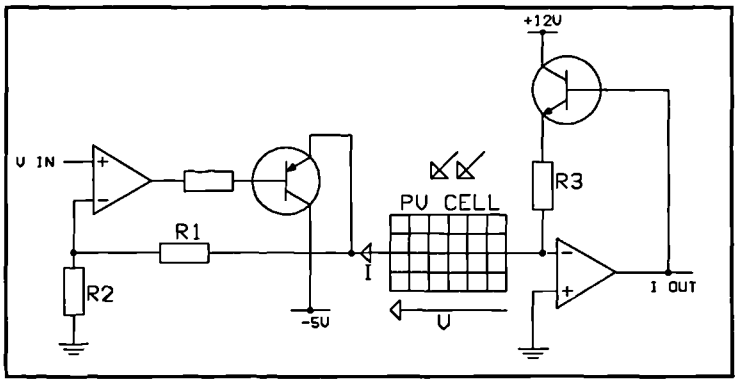

Figure 5 Simplified pod schematic : SC characterizer

In order to measure the light irradiance on the surface of the cell, an irradiance probe was constructed on a separate board allowing it to be placed in the same plane as the array under test. A large-area photodiode of 1cm^2 was used as the sensor. It is known that the photocurrent I_{ph} of a photovoltaic cell is linear with irradiance, and thus this photodiode was operated in photovoltaic mode into a virtual earth in accordance with the specifications on the manufacturer's data sheet, all but eliminating the effects of the exponential terms and the parallel resistance and providing a current output that was linear with irradiance. This photodiode had a response curve which coincided with the bulk of the solar spectrum and thus appeared a suitable choice. **Figure 6** shows the schematic for the irradiance probe.

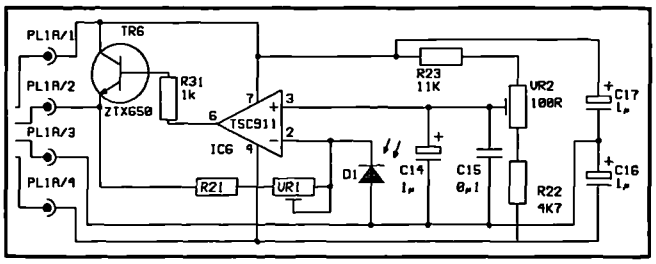

Figure 6 Irradiance probe

Cell temperature was sensed by a small dedicated temperature-sensing IC which was physically attached to the rear of the photovoltaic array under test using thermal transfer compound. The output is amplified by a single non-inverting voltage amplifier with a gain of 11

giving a possible measurement range of 0-90°. This range is sufficient for the purpose of the cell temperature measurements, the cell temperature never reached 90° in any of the practical tests.

The pod is constructed as a single PCB containing the cell characterization circuitry, temperature probe amplifier and a unity gain buffer for the output of the irradiance probe. The PCB is mounted on a baseboard, with the cell, temperature and irradiance probes on a panel mounted perpendicular to the baseboard allowing ease of irradiation of the cell and irradiance probe. The connection to the acquisition card is via a single 12-core 'umbilical' cable. If a cell with a V_{oc} greater than 10V is to be characterized, the same pod design may be used (with appropriate modification to the range-setting resistors and to the range constants in the software) but an external power supply will be required.

2.4.1.2 Card design - an overview.

The data acquisition card is based around the Siemens SDA1812D four-channel 12 bit ADC. This device is designed to be simple to interface to a standard 8-bit microprocessor bus as it carries the required bus decoding on-chip, as well as an autocalibration system to minimize offset errors. It can sample at over 100kHz and has an on-chip clock generator which can be asynchronous with the bus. A 'busy' signal is asserted during the conversion and autocalibration so that the device can either be polled or generate interrupts as the software requires. The multiplexing and sample/hold is carried out on-chip, all that is required externally is a voltage reference (+5V) and signal conditioning. Some decoding of the PC XT bus signals is required to decode the addressing and the chip-select signals, and this is done in a small programmable logic device.

The single DAC channel was based around a Ferranti ZN558 8-bit DAC. This device uses a latched input making the decoding and interfacing straightforward. The device has a unipolar voltage-source output between zero and 2.5V. The output is buffered by a non-inverting amplifier with a gain of 4, giving an output of 0-10V. 8 bits gives sufficient resolution, 255 sample points

are possible across the solar cell characteristic which is more than enough - the expense of a 12 or 16 bit DAC is not really justified.

The card was constructed on an XT prototyping card produced in kit form by Maplin Electronics Ltd [24]. This card provides a selectable address decoder and buffering for the XT bus built in TTL logic, together with a matrix-board upon which the system under development may be built.

The software that handles the conversion control and channel selection for the ADC, the drive to the DAC and the I/O from the digital ports was coded in 80286 assembler in a separate module. Each low-level support procedure is C-callable, providing a simple interface to the control software developed in C.

2.4.2 PV acquisition software

The software driving the acquisition card was developed to run under the commonplace MS-DOS™ operating system of the PC. Essentially the core of this software performs three steps. The first of these - autoranging - determines the optimum ranges for current and voltage that should be used for a particular run. The optimum is such as to maximize the number of data points that may be obtained, also to make the greatest use of the available dynamic range of the ADC channels. Autoranging is performed in two stages. Initially a scan from V=0 upwards is made, one on each of the two available voltage ranges to locate the position of the cell open circuit voltage V_{oc}. The range yielding the maximum number of sample points is selected. The second step is to set V=0 and determine the output from the ADC for each of the four current ranges - the selected range is that which will place the cell short-circuit current I_{sc} in the uppermost quadrant of the ADC range - failing that the range yielding the highest output is selected. This method of autoranging will sometimes fail, however, and if this occurs prompts for the manual selection of the range required are displayed. The autoranging may be disabled altogether, in which case the ranges and number of sample points are entered manually.

Once autoranging is complete, the acquisition run starts. To aid in the elimination of noise, each sample point consists of the average value of a number of sample points. The number of points taken is selectable, as is the delay between the sampling and any range switching. This averaging process forms a crude, but remarkably effective filter to attenuate periodic noise such as radiation from 50Hz mains that may be picked up by the acquisition pod and umbilical. Random noise is also reduced. The values obtained from the ADC channels corresponding to the current, temperature and irradiance sensing is then multiplied by an appropriate calibration constant for the range used to yield values in appropriate units - all these constants may be modified by the user and are saved in a configuration file upon exit.

Finally the I/V data is saved in a text-file format. A function is provided to allow the data set to be plotted on the screen and examined, thereby giving an opportunity to reject a data set which contains glitches, or does not meet required criteria in other ways. The plot may also be printed to a PostScript™ [25] printer, or to an encapsulated-PostScript™ file.

Implemented as an overlay to the software package is a small program allowing adjustments to be made to the results to compensate for the dimensions of the array (the number of cells in series/parallel within the array) in order to present results that correspond to those for a single cell. This program simply multiplies current and voltage values by a factor appropriate to the dimensions of the cell array before saving the files under the same name. The overlay can be executed from the command line if necessary. A powerful mouse-driven user-interface was written and added so as to facilitate ready and quick access to the functionality of the acquisition system in order to speed up its operation.

2.5 Double-exponential model parameter determination

With the aforementioned I/V data acquisition system, it is possible to generate sets of I/V curves from a specimen solar cell across its operating range. However, in order to be able to determine the law linking irradiance and temperature to the five double-exponential model

parameters it is necessary to determine for each of the available I/V data sets a corresponding set of double exponential model parameters .

The double-exponential model equation is both non linear, and implicit. To arrive at an analytical solution of its five parameters given a set of data at a specific temperature is no easy task and a better solution would be to look towards a numerical approach such as curve-fitting.. Some analytical methods have been published [21], [26] but even these require an iterative approach, and/or a less complex curve-fit in the vicinity of the areas of interest such as the maximum power point. Such methods would be no more costly in terms of computational requirements and time than a dedicated well-designed curve-fitter. A curve fit is not necessarily difficult to implement, or less accurate either providing good initial 'seed' values for the parameters can be found, and that the trade-off between the number of iterations and the overall computation time is made carefully.

It was decided to develop a powerful PV based curve fitting and data analysis package to complete the model. This system was used initially to determine sets of double-exponential model parameters from experimental data obtained with the aid of the data acquisition system. These sets of parameters were used to determine the as yet unknown algorithm linking both irradiance and temperature to the double exponential model parameters. Once this algorithm had been determined the data analysis package was extended to evaluate the constants in these algorithms which are specific to the cell. The analysis package could then solve the entire model from irradiance and temperature figures through to a current-voltage curve in order to be able to display an experimentally obtained I/V curve superimposed upon one calculated from the model at the same values of temperature and irradiance. In this way the validity and accuracy of the model may be seen. The cell specific constants, once determined could be submitted to a template running under Saber which would perform the complete circuit-based simulation of an array of the cells in conjunction with the power electronics.

2.5.1 PV data analysis package - development environment

The parameter extraction system was developed to run on a readily-available IBM PC compatible, as was the data acquisition system. An advantage of this is that the results obtained from it may be used with any simulation template, not necessarily one based around Saber, (providing the model can be implemented within the environment of the alternative simulator) thereby making the system attractive to power electronics specialists who use alternative component/circuit level simulators. All software was coded in the C programming language.

2.5.2 I/V curve fitter - design methodology

In the early stages of development, some trials were made with elementary curve fitting systems in order to determine the manner in which they behaved, and whether or not they were suitable. Initially a useful library of fast generic matrix-algebra procedures was built up in a C program module, in a form which could be readily accessible to any further parts of this system requiring matrix functions. Such an approach ensures there are no code overheads as there would be if a commercial numerical-solutions library was used. Such a library would doubtless check validity of input, array bounds etc. and the code required to do this would significantly add to the processing time if the functions are called repetitively. Such checking is unnecessary here as careful programming will always ensure the validity of the arguments passed to matrix functions. Long-double precision (10-byte reals in IEEE format) were used throughout the system for all constants, multipliers, matrices and in all areas where a precision or rounding error could be introduced. The decision to use these high-precision numbers was based upon the fact that the hardware floating-point coprocessors in IBM PC compatibles internally stores all numbers in 80 bit reals, and since the intention was to use the coprocessor for speed, there seems little point in losing precision while transferring data from the coprocessor stack to main memory. The increased demands on memory brought about by the high precision was considered - however most modern PCs contain a considerable amount of memory, and a virtual memory driver was used to extend the DOS-based 640K limit. No memory-related problems were experienced in practice.

The parameter extraction package, incorporating the curve fitter, performs two functions. The first level fit is to extract a number of definitive sets of parameters of the solar cell equation to fit an I/V curve obtained at each specific level of temperature and irradiance. Once the relations between temperature, irradiance and the double-exponential model parameters are determined the second level fit was implemented. This is a two-dimensional exercise examining the relationship between the parameters extracted during the first level fits on a number of data sets, and the irradiance and temperature levels of those runs. This entails fitting a surface to these points if all dimensions are to be considered.

2.5.3 Newton-Raphson PV model solution engine

All methods of curve fitting require a method of solving the equation to be fitted - in this case equation **(1)**. Equation **(2)** is a subset of equation **(1)** and may be evaluated by the same code simply by setting I_{s1} to zero. Equation **(1)** is both non-linear and implicit, and therefore proves to be intractable analytically. Numerical solution is the only avenue, and code was written to solve this equation using the well-known Newton-Raphson technique [27]. The code segment is shown in **Figure 7**, while equations **(8)**, **(10)** and **(9)** show the iterative equation set solved by the system.

$$I_n = I_{n-1} - \frac{\phi}{\phi'} \tag{8}$$

$$\phi' = 1 + \frac{eI_{s1}R_s}{kT}.e^{\frac{e(V+IR_s)}{kT}} + \frac{eI_{s2}R_s}{AkT}.e^{\frac{e(V+IR_s)}{AkT}} + \frac{R_s}{R_p} \tag{9}$$

$$\phi = I - I_{ph} + I_{s1}(e^{\frac{e(V+IR_s)}{kT}} - 1) + I_{s2}(e^{\frac{e(V+IR_s)}{AkT}} - 1) + \frac{V+IR_s}{R_p} \tag{10}$$

During the initial development of the curve-fitter it was necessary to use an I/V curve for which the double exponential parameters were already known, in order to test it. I/V data was

generated using this algorithm from a set of published extracted double-exponential model parameters [28]. Measurement error and random noise was then simulated by superimposing a normally-distributed random variable of known constant mean and variance. Such data was found to be useful in the testing and evaluation of the curve-fitting engine before actual data from the acquisition system was used. The code also formed the backbone of the parameter extraction system - the procedure from which **Figure 7** was taken additionally calculates the partial derivatives of equation **(1)** with respect to its parameters - this will be described later.

```
im=i_init;
for(iter=0,*NR_error=1;(*NR_error>0.00001)&&(iter<max_iter);iter++) {

   phi=im-params[0]+params[1]*(expl((V+im*params[4])/vt)-1)+
          params[2]*(expl((V+im*params[4])/(params[3]*vt))-1)+
          ((V+im*params[4])/params[5]);

   phiprime=1+
           ((params[1]*params[4])/vt)*expl((V+im*params[4])/vt) +
           ((params[2]*params[4])/(params[3]*vt))*
           expl((V+im*params[4])/(params[3]*vt)) +
           (params[4]/params[5]);


   in=im-phi/phiprime;
   if (in==0)
       *NR_error=0;
   else
       *NR_error=fabsl(((im-in)*100)/in);
   im=in;
}
```

Figure 7 C code fragment for the Newton-Raphson solution of the double-exponential solar cell model.

Note that this implementation of the Newton-Raphson algorithm solves the equation for current in terms of voltage. This was found to be the most numerically stable of the two possible ways of solving this equation, the other being to solve for voltage in terms of current, and certainly the less critical as regards the initial, or seed, value. In most cases it was found that setting the seed to be roughly half of the short-circuit current ensured convergence over the entire characteristic. This method of solving the solar cell equation has appeared so far to be quite suitable and also efficient - convergence to an acceptable level (0.00001% error) is usually obtained within 20 iterations.

Convergence failures can occur when the seed value exceeds the short circuit current. So far there appears not to have been any serious problems with numerical instability, but should it ever arise code may have to be implemented to internally obtain a better approximate to the root to use as a seed. A possible way of doing this would be to approximate the I/V curve as two straight lines, one between I_{sc} and the maximum power point, the other between the maximum power point and V_{oc}. The constants in the two equations for the lines could be determined from the parameters by splitting equation **(1)** into two parts, one governing the characteristic from I_{sc} to the maximum power point, the other from the maximum power point to V_{oc}, taking a first-order approximation for the exponentials (valid as the characteristic in these regions does not show a particularly high degree of curvature) and evaluating. A disadvantage of this method is that the raw I/V data would have to be scanned in advance in order to know the position of the maximum power point, and this would render the Newton-Raphson engine dependent not only upon the equation parameters, but upon the characteristic as a whole for its seed. So far this problem has not surfaced.

The Newton-Raphson solution of equation **(1)** was found to be intrinsically stable, with a large convergence region. The only evidence of misconvergence in the system was if an attempt was made to evaluate **(1)** with parameters out of the range of physically acceptable values. However, this is not a problem as such values would only be presented if the curve fitting system attempted a minimization step which brought the parameters into such regions - this would indicate a failure on the part of the curve fitter and code is in place to trap this condition and terminate the fitting run before non-recoverable errors occur in the maths runtime support.

2.6 First level curve fit: initial attempt.

Once the Newton-Raphson double exponential model solution engine and the matrix algebra library was built, the development of a suitable curve-fitting engine to perform the first-level curve fit was commenced - that of curves obtained at a specific level of irradiance and temperature to a specific set of parameters. It may be necessary to fit quite a large number of

curves to build up a database of parameter values at specific temperature and irradiance levels, in order that the second-level fit may be accurate.

There are a number of non-linear curve fitting methods available, amongst them the downhill simplex method [16], the simple Gauss-Newton nonlinear methods, and the Levenberg-Marquardt algorithm [27], most of which have been used to fit PV current-voltage curves, often however to the single exponential model only. Initially, experimentation commenced with an implementation of the Gauss-Newton method, this being the simplest (and quickest) to implement. The experimentation used as input an I/V curve generated from a set of published parameters for a cell using the Newton-Raphson evaluation procedure, with a normally-distributed random variable superimposed on it. The parameters used were:

I_{ph}: 11.77mA
I_{s1}: 3.59×10^{-20} A
I_{s2}: 2.95×10^{-11} A
A: 2.0
R_s: 0.037 R
R_p: 6.10×10^4 R
T: 20°C
E: 100W/m^2
Random variance : 0.001

The plot of this curve is shown in **Figure 8.**

During the experimentation it became clear that the Gauss-Newton method was very sensitive to certain of the parameter values. It was found to be very difficult to obtain convergence of R_p at all, and when convergence of all the parameters occurred it was often to nonphysical values (below zero), particularly of the saturation currents. It was felt to be far too unstable to use as the core of a general-purpose curve-fitting system, and as a result it was decided to attempt to use one of the more complex algorithms. This instability is not unduly

surprising as the relative magnitudes of the parameters are quite large - R_p is of the order of 10^7 whereas the saturation currents are of the order of 10^{-12}. This difference can lead to difficulty with the convergence of R_p.

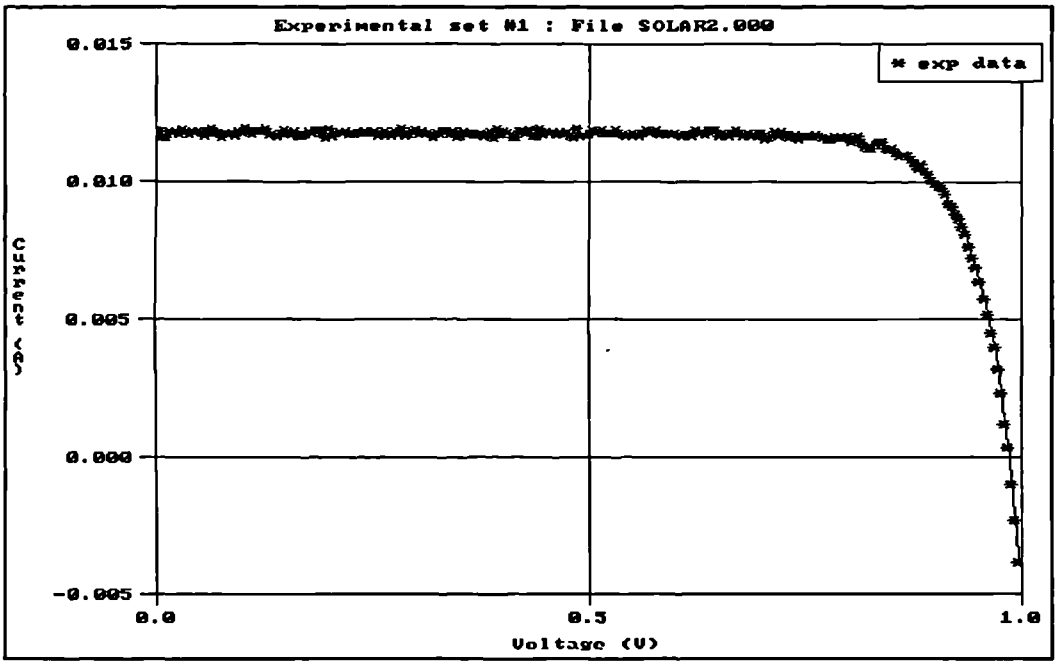

Figure 8 Raw data used as a test.

2.6.1 First level curve fit: Levenberg-Marquardt method

The two likely methods for curve fitting of nonlinear functions that would be usable in this case are the simplex method and the Levenberg-Marquardt method - which is in itself a method of implementation of standard chi-squared fitting. The only advantage of the simplex method is that it does not require the evaluation of fitting function derivatives - useful when these functions can not be obtained analytically. In the case of PV modelling, it is not difficult to obtain a symbolic solution of the first partials of equation **(1)** with respect to the parameters (equations **(12)** through **(17)**). The Levenberg-Marquardt algorithm is an implementation of chi-squared fitting, where the algorithm is used to minimize the chi-squared value of the problem, equation **(11)**, with respect to the (in this case) six parameters of the function to be fitted.

$$\chi^2 = \sum_{i=1}^{N}\left[\frac{y_i - y(X_i;a)}{\sigma_i}\right]^2 \tag{11}$$

$$\frac{\partial I}{\partial I_{ph}} = 1 \tag{12}$$

$$\frac{\partial I}{\partial I_{s1}} = 1-e^{\left(\frac{e(V+IR_s)}{kT}\right)} \tag{13}$$

$$\frac{\partial I}{\partial I_{s2}} = 1-e^{\left(\frac{e(V+IR_s)}{AkT}\right)} \tag{14}$$

$$\frac{\partial I}{\partial A} = -\frac{I_{s1}e(V+IR_s)}{A^2kT}.e^{\left(\frac{e(V+IR_s)}{AkT}\right)} \tag{15}$$

$$\frac{\partial I}{\partial R_s} = -\frac{e.I.I_{s1}}{kT}.e^{\left(\frac{e(V+IR_s)}{kT}\right)} - \frac{e.I.I_{s2}}{AkT}.e^{\left(\frac{e(V+IR_s)}{AkT}\right)} - \frac{I}{R_p} \tag{16}$$

$$\frac{\partial I}{\partial R_p} = \frac{V+IR_s}{R_p^2} \tag{17}$$

The algorithm searches for a minimum by varying between the inverse-Hessian method and the steepest-descent method across the surface of the chi-squared function. Each iteration returns a better estimate of the parameters. The method is well known, and is also fairly robust as it tends to avoid the generation of internal matrices which are either singular, or impossible to invert due to a zero pivot.

The implementation of this method was found to be successful at locating a set of parameters for best fit when presented with the same data as in section 2.6. Convergence was usually to physical values (>0); this was dependent upon the method of determining initial seed values for the parameters. Initially this was done by guesswork with the test data, as an effective analytical method had yet to be determined. The curve of **Figure 9** shows the 'raw' test data of **Figure 8** fitted, with the fit curve superimposed and the extracted parameter set shown.

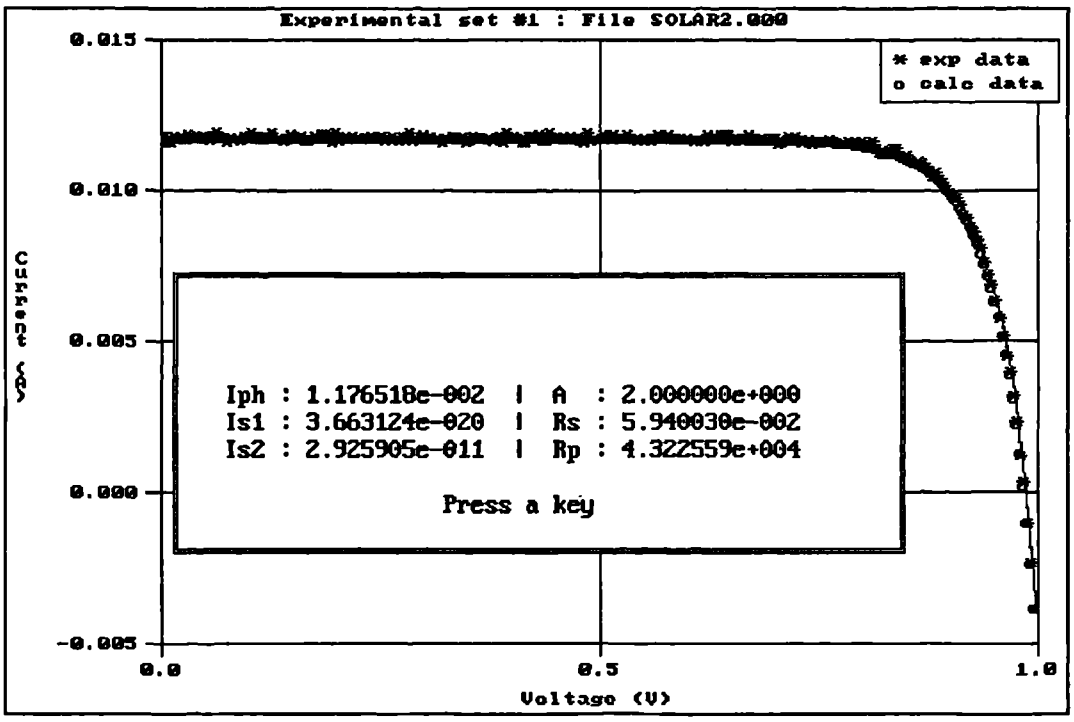

Figure 9 Fitted data set superimposed upon 'raw' data.

It can be seen that the parameter set extracted and shown in **Figure 9** shows good agreement with the parameters in section 2.6 that were originally used to generate the curve. Excluding A, which is held constant over the fit run, it can be seen that I_{s1} is the closest to the original - this is not surprising as the short circuit current is highly dependent upon I_{ph}. I_{s1} and I_{s2} are also quite close to the original value, but it can be seen that R_s and R_p differ noticeably. Visibly, the curve back-calculated from the extracted parameters (shown in blue) can be seen to fit the experimental data well. The statistical nature of curve-fitting and the number of degrees of freedom proffered by the variability of five parameters in the equation allows for the fact that several different parameter sets may result in a curve which arrives at a chi-squared minimum and fits the experimental data. also R_p is several orders of magnitude larger than the other parameters, which suggests that small variations in some parameters during the fit run may result in larger variations in R_p. The convergence bound of R_p is thus somewhat wider than that of the other parameters. Owing to the statistical nature of curve fitting in that there are a number of possible valid parameter sets that would form a best fit to a specific set of experimental data; if

consistency is maintained in the method of initial parameter extraction, the final parameter sets across a number of data sets will also show consistency in their trends This, therefore, does not compromise the usefulness of the curve-fitting technique as a tool in determining the trends of the five variant parameters with temperature and irradiance.

The parameter-extraction program allows for on-screen plotting of the curves, both that from the experimental data, and a solution of the model equation using the fitted parameters. **Figure 9** together with **Figure 8** are screen dumps taken from the system using a screen-capture utility as experimentation on these data sets took place prior to the development of the PostScript™-based X-Y plotter code which was added at a later date. These may be superimposed in order to view the fit, and accept or reject if necessary. The plotter also allows the power curves to be displayed, again of both sets of data and either separately, or superimposed upon the I/V data. It is possible to manually reject a parameter set if it is deemed to be unacceptable, for example if any of the parameters had converged to nonphysical values. An enhancement to the method is that the same curve fitter code and equations may be used to fit to the single exponential model **(2)**. The code allows each parameter value to be held constant during the iterative process if desired, and to fit to **(2)** all that is necessary is to hold I_{s1} constant at zero and allow A (the 'diode quality' factor) to vary during the fit run. During double-exponential fitting A is held constant at 2 and I_{s1} is allowed to vary. All other parameters are allowed to vary.

2.7 Methods of initial point (seed value) determination for the PV data curve fitter.

Owing to the numerical curve-fitting system used to perform the double exponential model fit to the I/V data sets, initial approximate solutions are required for this procedure to provide a seed with which to start the iteration. In the case of the Newton-Raphson solution of equation **(1)**, a suitable initial point was found to be relatively simple to determine. However, the determination of initial values of the five parameters of **(1)** used in the curve fit proves to be considerably more difficult and a more elaborate system had to be developed and is explained by way of a flow chart in **Figure 10** and in more detail below.

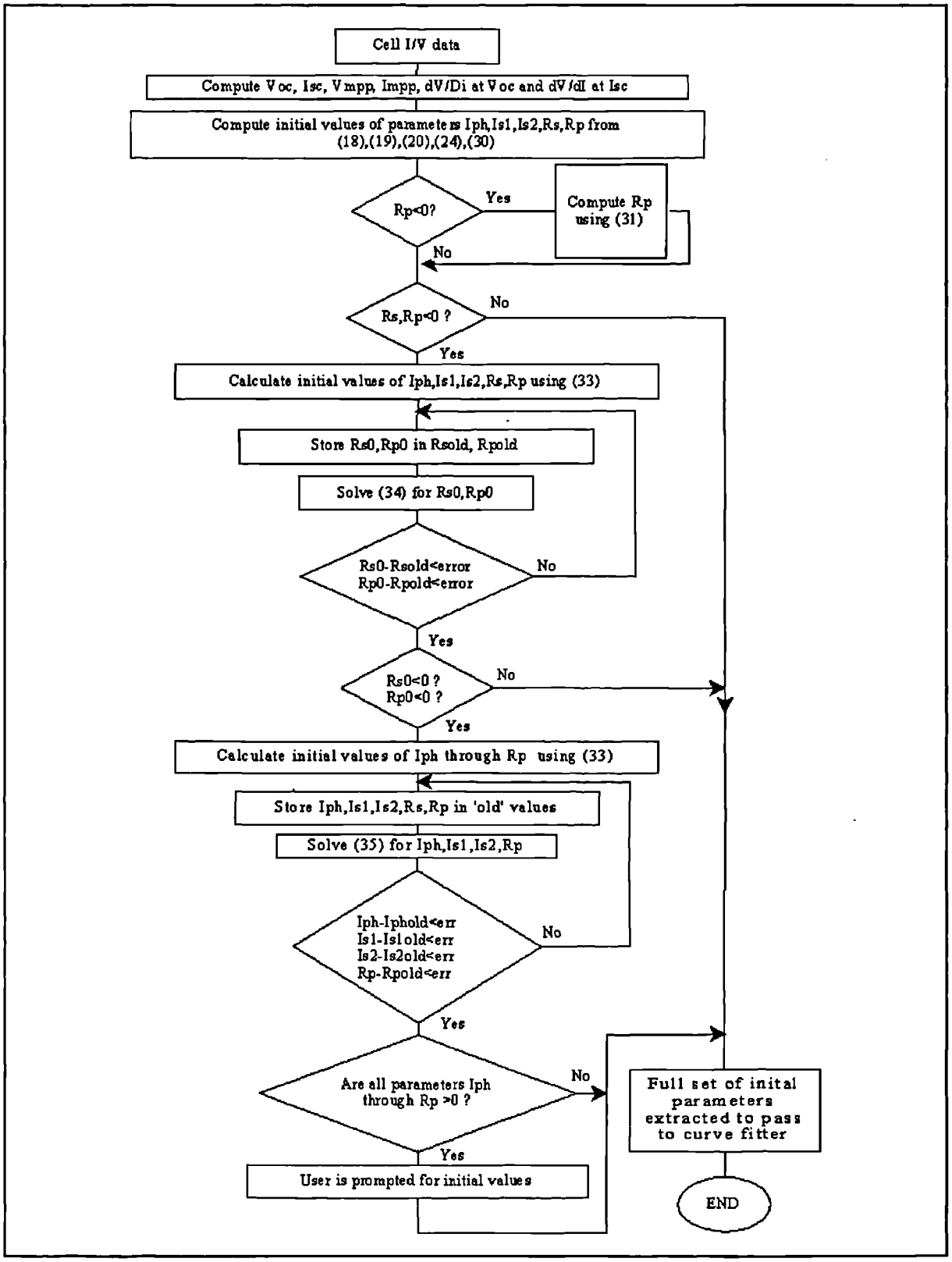

Figure 10 Flow chart of software-based initial point extractor for the PV double-exponential model curve fitter.

2.7.1 Initial value extraction : double-exponential model parameter fitter.

The double-exponential model parameter fitter using the Levenberg-Marquardt method requires a more complex method of initial point extraction. Each of the five variable parameters of **(1)**, namely R_s, R_p, I_{s1}, I_{s2} and I_{ph} (A is held constant equal to 2 across the fit run for double exponential modelling, whereas for single exponential modelling I_{s1} is held constant at zero and A is allowed to vary), require initial values to be determined. The success of the fit does depend to a degree upon the accuracy of these initial values, since the curve fitter has a large number of degrees of freedom in as much as all the parameters may be varied in the attempt to minimize the chi-squared value and it is quite possible that a range of different parameter sets may well satisfy this condition. The initial values for the parameters I_{ph}, I_{s1} and I_{s2} are fairly easy to determine, and the method follows from examination of the equivalent circuit for the cell (**Figure 11**) together with equation **(1)**. In the following descriptions initial values of the parameters are denoted by the subscript 0.

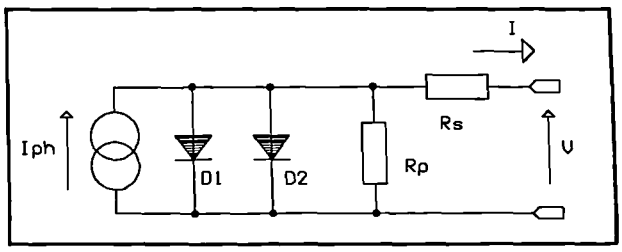

Figure 11 Solar cell equivalent circuit

At $I=I_{sc}$, $V=0$, I_{ph} is approximated well by I_{sc} as the portion of current flowing down the diodes and the parallel resistance is very small : R_s is small therefore the voltage drop across it is also small. At $V=V_{oc}$, $I=0$, the terms in R_s drop out of the equation, and the current flow in the parallel branches is dominated by the two diode currents. Therefore:

$$I_{ph0} = I_{sc} \tag{18}$$

The saturation currents may then be approximated by making an assumption that these two currents are roughly equal as the cell voltage tends to zero, yielding equations **(19)** and **(20)**.

$$I_{s10} = \frac{1}{2} \cdot \frac{I_{ph0}}{\left(e^{\left(\frac{eV_{oc}}{kT}\right)} - 1 \right)} \tag{19}$$

$$I_{s20} = \frac{1}{2} \cdot \frac{I_{ph0}}{\left(e^{\left(\frac{eV_{oc}}{2kT}\right)} - 1 \right)} \tag{20}$$

This leaves only R_{s0} and R_{p0} to be determined. This is not an easy task. Most of the approximations that could be used are derived in some way from equation **(1)** and therefore rely upon the already-approximated values of the other parameters. Other systems require dark I/V measurements for the cells: the design methodology behind this system was to require only the use of the light I/V curve at irradiance levels between V=0 and $V=V_{oc}$. Reference [21] presents a method based upon the use of the numerical values for the integral under the I/V and power curves which appears to be valid; however although the equations are dimensionally correct it was found to be impossible to obtain sensible values for the resistances using them - often R_{p0} would end up negative. Eventually it was decided to attempt a different approach. A method involving the slope of the I/V curve at $V=V_{oc}$, at V=0 and the value of I and V at the maximum power point was developed.

Experimentation with the I/V curve, by investigating variations of the curve with a known parameter set while varying R_s and R_p showed that R_s has a very marked effect upon the slope of the I/V curve at $V=V_{oc}$. R_p, however, has a marked effect upon the lateral position of the maximum power point together with a less marked effect upon the slope of the curve at V=0, $I=I_{sc}$. To this end, the following system was developed. Equation (1) is differentiated to yield **(21)**:

$$\frac{dI}{dV} = -\left[\frac{X_1 + X_2 + \frac{1}{R_p}}{1 + R_s(X_1 + X_2 + \frac{1}{R_p})} \right] \tag{21}$$

where X_1 and X_2 are given by (22)

$$X_1 = \frac{eI_{s1}}{kT} e^{\left(\frac{e(V+IR_s)}{kT}\right)} \quad and \quad X_2 = \frac{eI_{s2}}{AkT} e^{\left(\frac{e(V+IR_s)}{AkT}\right)} \tag{22}$$

This is then evaluated at $V=V_{oc}$, $I=0$ to yield (23)

$$\left.\frac{dI}{dV}\right|_{V_{oc}} = -\left[\frac{X_{1_v}+X_{2_v}+\frac{1}{R_p}}{1+R_s(X_{1_v}+X_{2_v}+\frac{1}{R_p})}\right] \tag{23}$$

$$where \quad X_{1_v}=\frac{eI_{s1}}{kT} e^{\left(\frac{eVoc}{kT}\right)} \quad and \quad X_{2_v}=\frac{eI_{s2}}{AkT} e^{\left(\frac{eVoc}{AkT}\right)}$$

If (23) is now rearranged in terms of R_s, the result is (24)

$$R_{s0} = -\left[\left.\frac{dV}{dI}\right|_{V_{oc}} + \frac{1}{\left(X_{1_v}+X_{2_v}+\frac{1}{R_p}\right)}\right] \tag{24}$$

Note that (24) is in the form of the slope of the IV curve at $V=V_{oc}$ added to a 'compensation value'. Examination of (24) shows that in the neighbourhood of V_{oc} the terms X_{1v} and X_{2v} dominate over the much smaller $1/R_p$ and therefore the $1/R_p$ term may be neglected. The final equation for R_{s0} is given by equation (25)

$$R_{s0} = -\left[\left.\frac{dV}{dI}\right|_{V_{oc}} + \frac{1}{X_{1_v}+X_{2_v}}\right] \tag{25}$$

In practice this gave remarkably good approximations for R_s. Convergence in the case of almost all of the test data from the cell (to be shown later) was to acceptable values of the parameters with the only exception being at the low extremes of irradiance. At this end of the cell's characteristics, the fill factor drops off considerably, and it would appear that either the approximations for the saturation currents no longer hold, or the parallel resistance term in the denominator of **(24)** becomes important. In addition to this, another source of error in the value is largely due to the method used to determine the value of dV/dI at V_{oc} - this is done currently by performing a standard linear least-squares fit of the last ten points of the I/V curve. This is acceptable for high fill factors where the slope does not change considerably in the neighbourhood of V_{oc}, but for lower fill factors a greater curvature is observed and this could lead to a less accurate value of dV/dI being determined. A polynomial fit may be an improvement, although this was not implemented as only one I/V data set defied the initial point extractor. A quadratic fit would be sufficient as this will provide a constant second derivative giving an indication that the behaviour of the curve at the V_{oc} point will be acceptable. The code allows for the user to enter approximations should the numerical system fail, and if a fit is required in these regions of operation it may still be obtained.

In addition, a better fit is likely to be obtained if there are more sample points in the curve in its entirety, which may (depending upon the type of acquisition system used) be difficult at the bottom end of irradiance values as here more amplification of the signals will be required, and therefore the likelihood of poor noise factors will increase and make an accurate curve fit even more difficult.

Determination of R_{p0} is considerably more difficult. The approximation for R_{s0} depends upon the accuracy of already-approximated values for the saturation currents. It is not easy to isolate R_p from R_s in a single equation that may be solved for R_{p0} ; to this end a number of approaches were tried, without success. These included rearranging **(24)** in terms of R_p, substituting into **(1)** and evaluating for R_s at $V=V_{mpp}$, $I=I_{mpp}$ using iteration, before back-substituting into **(24)** to obtain a value of R_{p0}. Owing to the manner in which I_{s1} and I_{s2} are approximated, this led to negative values for R_{p0}, which clearly are not acceptable. It became

apparent that dependence upon the previously approximated parameters I_{ph0}, I_{s10}, and I_{s20} would have to be minimized. In the light of the described successful method of determining R_{s0}, it was decided to attempt a similar approach based upon the slope of the IV curve at $I=I_{sc}$. Although the slope at this point does not seem to bear as marked a dependence upon R_p, the position of the maximum power point does. Two methods were set up, and compared. The first of these involved evaluating **(21)** at $I=I_{sc}$, and rearranging in terms of R_p. **(26)**

$$R_{p0} = -\left[\frac{1}{\frac{1}{\left(\left.\frac{dV}{dI}\right|_{I_{sc}}+R_s\right)}+X_{1_i}+X_{2_i}}\right] \qquad (26)$$

$$\text{where } X_{1_i}=\frac{I_{s1}}{vt}e^{\left(\frac{I_{sc}R_s}{vt}\right)} \text{ and } X_{2_i}=\frac{I_{s2}}{Avt}e^{\left(\frac{I_{sc}R_s}{Avt}\right)}$$

The second of the two methods involved evaluating (1) at the maximum power point, using the approximated value of R_{s0} and rearranging for R_{p0} **(27)**

$$R_{p0}=\frac{V_{mpp}+I_{mpp}R_{s0}}{I_{mpp}-I_{ph0}+I_{s10}\left(e^{\left(\frac{e(V_{mpp}+I_{mpp}R_{s0})}{kT}\right)}-1\right)+I_{s20}\left(e^{\left(\frac{e(V_{mpp}+I_{mpp}R_{s0})}{AkT}\right)}-1\right)} \qquad (27)$$

Both systems gave a value of R_{p0} *that resulted in convergence in most cases*, but the approximation was not as good as that of R_{s0} from **(25)**. This is not surprising. R_p is a parameter with a large value, and small perturbations in the saturation currents can have a large influence upon the approximated value of R_{p0}. However, the reliability of convergence was better from the values calculated from equation **(27)** and this was used in the final implementation. The manner in which the code is developed allows for the future implementation of better methods to improve this approximation and can be implemented as they are arrived at - the initial point extraction is performed in a single function and it is a simple matter to modify the appropriate part of it.

As with R_s, the convergence of R_{p0} was found to be much worse for the cases of extremely low irradiance. This again is not surprising as R_p has greater dependence upon changes in other parameters - it is the largest and could be of the order of 10^{+3}, whereas the saturation currents are of the order of 10^{-12}. However, bad approximation leading to nonphysical convergence of the curve fitter was largely confined to regions of low irradiance. At present, initial values may be entered by hand should the computed method fail. The system implements a heuristic algorithm based upon **(26)** and **(27)**, with algorithm selection depending upon the curve data and success or failure of one or the other algorithm.If one algorithm fails, the other is attempted. As stated, if both methods fail on a difficult curve then values can still be entered by hand.

The final parameter to be determined is an initial value for A. In the double exponential model A can be set to 2 and not allowed to vary during the curve fit, as this provides a first approximation for Shockley-Read-Hall recombination current in the junction depletion region and is acceptable for all practical cases [22]. However, if it is desired to fit to the single exponential model, A will vary. As yet a deterministic method of approximating A has not been defined, and until such is developed the initial value computation function simply sets this to an arbitrary value of 3 : if a different value is required it may be entered by hand.

All the above equations can be used with the single exponential model simply by setting I_{s1} to zero, and in the approximation for I_{s20} from which the factor of 2 in the denominator is replaced by A, giving **(28)**

$$I_{s20} = \frac{I_{sc}}{\left(e^{\left(\frac{eV_{oc}}{AkT}\right)}-1\right)} \qquad (28)$$

The code performing the initial value determination was implemented in two functions. The first of these extracts the values V_{oc}, I_{sc}, V_{mpp}, I_{mpp}, dV/dI at V_{oc} and I_{sc}. The second of the two functions calculates the initial cell parameter values depending upon the cell type. A least-squares line fit in the neighbourhood of V_{oc} and I_{sc} involving the first and last ten points of the curve (if there are less than 40 data points available, the last five points are used) allows determination of the slopes, as well as V_{oc} and I_{sc} if these are not present explicitly in the data file - i.e. the function

will extrapolate if necessary. V_{oc} is determined by looking for the lowest I value in the data set - some acquisition cards that are not designed for bipolar signals may well give indeterminate values if V_{oc} is exceeded and the cell is effectively forward-biassed. This method prevents such values from misleading the initial point determination although it may be necessary to edit the data file to remove these erroneous values in order to prevent them from being incorporated into the curve fit.

A better approach to the determination of initial values, particularly of R_{s0} and R_{p0} can be an iterative one, including within the iterative loop a better approximation for the two saturation currents and the photocurrent. It was seen that equations **(25)**, **(26)** and **(27)** could be placed in such a loop, with two additional equations determining the I_{ph} and $I_{s1/2}$ values. The equation sequence is given below in **(29)** and **(30)** (for the double-exponential case). Equation **(29)** gives the initial conditions, while equation **(30)** gives the equations solved in the iterative loop.

Initial condition equations:

$$R_{s0}=\left.\frac{dV}{dI}\right|_{V_{oc}} \quad , \quad R_{p0}=\left.\frac{dV}{dI}\right|_{I_{sc}}$$

$$I_{ph0}=I_{sc} \quad , \quad A_0=2 \qquad (29)$$

$$I_{s10}=\frac{I_{sc}}{2e^{\left(\frac{eV_{oc}}{kT}\right)}-1} \quad , \quad I_{s20}=\frac{I_{sc}}{2e^{\left(\frac{eI_{sc}R_{s0}}{2kT}\right)}-1}$$

Iterative loop equations:

$$X_{1_v}=\frac{I_{s1}e}{kT}e^{\left(\frac{eV_{oc}}{kT}\right)} \quad , \quad X_{2_v}=\frac{I_{s2}e}{AkT}e^{\left(\frac{eV_{oc}}{AkT}\right)} \quad , \quad R_{s0}=-\left[\left.\frac{dV}{dI}\right|_{V_{oc}}+\frac{1}{X_{1_v}+X_{2_v}+\frac{1}{R_p}}\right]$$

$$X_{1_i}=\left[\frac{I_{s1}e}{kT}e^{\left(\frac{eI_{sc}R_{s0}}{kT}\right)}\right] \quad , \quad X_{2_i}=\left[\frac{I_{s2}e}{AkT}e^{\left(\frac{eI_{sc}R_{s0}}{AkT}\right)}\right] \quad , \quad R_{p0}=-\left[\frac{1}{\frac{1}{\left.\frac{dV}{dI}\right|_{Isc}+R_{s0}}+X_{1_i}+X_{2_i}}\right] \qquad (30)$$

Alternatively, using the second of the two methods previously described and which involves evaluating (1) at the maximum power point:

$$R_{p0}=\left[\frac{V_{mpp}+I_{mpp}R_{s0}}{I_{mpp}-I_{ph}+I_{s1}\left(e^{\left(\frac{e(V_{mpp}+I_{mpp}R_{s0})}{kT}\right)}-1\right)+I_{s2}\left(e^{\left(\frac{e(V_{mpp}+I_{mpp}R_{s0})}{AkT}\right)}-1\right)}\right]$$

$$I_{s20}=\left[\frac{I_{ph}-\frac{V_{oc}}{R_{p0}}}{e^{\left(\frac{eV_{oc}}{AkT}\right)}-1}\right],\quad I_{s10}=\left[\frac{I_{ph}-\frac{V_{oc}}{R_{p0}}}{e^{\left(\frac{eV_{oc}}{kT}\right)}-1}\right] \tag{31}$$

$$I_{ph0}=I_{sc}+\frac{I_{sc}R_{s0}}{R_{p0}}+I_{s1}\left(e^{\left(\frac{eI_{sc}R_{s0}}{kT}\right)}-1\right)+I_{s2}\left(e^{\left(\frac{eI_{sc}R_{s0}}{AkT}\right)}-1\right)$$

The system basically places the existing solutions of R_{p0} and R_{s0} within an iterative loop. Each iteration arrives at a better approximation of the parameters. Note. that **(30)** allows for the solution of R_{p0} by either equation **(26)** or **(27)**. Once again the software uses a heuristic implementation of the initial parameter value extraction. If the static methods **((25),(26))** fail to deliver sensible initial condition values the iterative method is tried. If this fails the software prompts for manual input of initial values. Once sensible values for initial parameter values are determined by one means or another, the curve-fitter is then called. The data set is rejected if the curve-fitter again fails to converge or returns unacceptable parameter values.

In the case of the single-exponential model used for amorphous cells the same equation set as **(30)** is used except that I_{s1} is not calculated, but held at zero (thereby forcing $X1_i$ and $X1_v$ to zero). The problem here is determining an equation for the diode quality parameter A. As yet a method for determining this (in the amorphous cell case only) has not been developed, and this parameter is currently set to 3 for the initial condition determination and allowed to vary during the curve fit.

2.8 Second level curve fit: Temperature/irradiance

Once a unique parameter set has been fitted to each data set, it becomes necessary to determine how the parameter values vary with temperature and irradiance. This provides the link between these cell variables and the circuit characteristics, and therefore is a vital part of the circuit-level modelling process. The temperature dependence of the parameters have been defined, and it is now necessary to determine two-dimensional relationships for the parameters with respect to both temperature and irradiance.

2.8.1 Cell types used in the determination of the second-level fit algorithms

A quantity of I/V data from a sample cell of a specific type is required in order to determine these algorithms. Two cell types were made available for this purpose, one a polycrystalline cell with which it was intended to define the algorithms for the double-exponential model, and one a thin-film amorphous type with which the single-exponential model would be investigated. The cells were two readily available solar modules obtainable from RS Components [29]. The specifications of the modules are detailed in **Table 1** and all measurements were specified under the test conditions of irradiance: 1kW/m^2, air mass 1.5 and a cell temperature of 25°C.

Although for cost reasons only one of each type of cell was available to be used in the definition of a law relating irradiance and temperature to the double-exponential model parameters, this is

Table 1 PV cell specifications.

	Amorphous cell	Polycrystalline cell
Output power	not specified	0.446W
Load voltage	7.5V	3.3V
Open circuit voltage	12V	4.6V
Load current	45mA	150mA
Short circuit current	54mA	160mA
Temp. coeff (V/°C)	-30m	-16m
Temp. coeff (A/°C)	0.05m	0.15m

neither restrictive nor unrepresentative of cells as a whole. The laws that define the trends of the behaviour of the cell originiate from the device physics, and thus while the constants in the equations for a given cell type may change with manufacturing variables and cell design, the actual form of the equations will remain constant providing no aspect of the device physics changes. It is the determination of the form of these equations which is of interest here; it is expected that the constants will be different for different cells. Once the form of the equations is known, to use the model to define the behaviour of a specific cell within the power electronics simulation environment, the constants for that specific cell type must first be determined by characterization of a sample of that cell. For this reason this modelling system was developed with the ability to perform this characterization (once the equation form was known) to thus make it useful in an engineering context.

2.8.2 Irradiance measurement

One of the problems involved with the irradiance measurements is simply that of the measurement of solar insolation. The characteristics of the cells are somewhat dependent upon the spectrum of the incident light, and the spectrum of sunlight varies considerably with atmospheric conditions etc. The unit of irradiance is W/m^2 and this takes into account the fact that several wavelengths of light are present. However, a reference measurement is required, and a calibrated pyrometer may be used to provide this, the calibration being valid only for a given spectrum. The acquisition system developed for the characterization of these cells uses an irradiance probe based around a $1cm^2$ photodiode and suitable amplification. The photodiode is operated in photovoltaic mode, in short circuit, where the output current will be proportional to irradiance. Initially this was calibrated against an Epley Radiometer D82 using Thorn CSI1000W lamps as a solar spectrum simulator. However, when it came to characterise the cells it was found that the lamps, being discharge devices and run from AC mains, had a 100Hz ripple upon the light output which therefore was not at constant intensity with time. Photovoltaic cells have a sufficiently fast response time that the ripple is noticeable on the characteristic. As a result, use of the solar simulator lamps was abandoned, and a set of curves was generated at varying temperature/irradiance with the use of a pair of 500W halogen units, which, unlike the CSI1000W

lamps, could have the intensity varied on demand. As no reference device for calibration of the irradiance probe was available for the halogen lamps, it was decided to circumvent this problem by taking the values obtained from the ADC channel associated with the irradiance probe as the irradiance values in arbitrary units. This signal is directly proportional to the irradiance in W/m^2, and serves adequately to determine the parameter variations. A power electronics specialist is interested in the manner in which a converter connected to the arrays will behave as the array characteristics change with environmental parameters. On this point, it is not absolutely necessary to be able to determine the absolute value of irradiance (providing the model is valid across the required range of irradiances), as it is the variation which is important in the development of these relations. Providing the measured irradiance level is directly proportional to the true irradiance in W/m^2, any correction factor in the units used will only affect the constants in the model. Should a calibration become available, all that is necessary is to multiply the irradiance figures by an appropriate factor in order to obtain the corresponding irradiance in W/m^2 - the calculations and derivation of the equations may proceed without this calibration factor. The 'arbitrary units' of irradiance used during this research, which are proportional to the irradiance in Wm^{-2} are simply defined as 'arb'.

2.8.3 Temperature measurement.

The acquisition system uses a dedicated temperature sensor IC to determine the temperature of the solar cells under test. The solar cells are dark in colour, and therefore will absorb energy which will be dissipated as heat - the surface temperature could be considerably higher than ambient. To this end the sensor IC, which is supplied housed in a TO92 package, is mounted with its flat portion against the cell at the rear to avoid obscuring any part of the light-sensitive surface, and to improve thermal conductivity thermal transfer compound is used. The device gives a voltage output directly proportional to temperature (10mV/°C) based on 0V at 0°C, thus providing an accurate measurement of absolute temperature simply by multiplying by an appropriate factor to suit the input of the acquisition system and adding 273 to the result in Celsius to give absolute temperature in Kelvin.

2.8.4 Data sets extracted from cells.

From each of the two cells fifty I/V curves were extracted using the data extraction system. The fifty I/V curves were taken at five different levels of effective irradiance, at 4000arb (corresponding to about 1kW of halogen lighting), 3000arb, 2500arb, 1500arb and 1000arb. The ten I/V curves at each level of irradiance corresponded to a range of array temperatures. The heat from the light source itself was sufficient to effect a temperature sweep from 300K to 329K, more than adequate to determine the general trends. The speed of the sweep is more than fast enough to avoid a problem with the cell temperature changing during the sweep itself, and sufficient time was allowed between irradiance changes for the light source to stabilize. The automated I/V curve acquisition process ensured that the irradiance and temperature were sampled just prior to the sweep, this ensured greater accuracy in that the actual temperature and irradiance of each sweep was recorded.

2.9 Implementation of first level fit: double-exponential parameters to data sets

The fifty data sets, one for each cell, were passed through the first level curve fitter in order to extract double-exponential model parameters for each curve. It was here that an interesting characteristic of the amorphous cell was discovered.

Initially, the polycrystalline cell data was fitted, and no problem was discovered here. All data sets were fitted successfully in an average of 20 iterations of the curve fitter. Only one set required manual input of initial values and even then it was just the initial value of R_p that was required. Curves back-calculated from the extracted double-exponential model parameters and superimposed upon the experimental data showed good agreement between them - most of them were virtually identical thus confirming the robustness of the curve-fitting approach. All data sets were usable for the determination of the irradiance/temperature to double exponential model parameter equations. The complete set of experimental curves obtained from this cell are shown

in Appendix A of this thesis, together with curves derived from the model and here the accuracy of the fitted curves may be seen.

However, the amorphous cell curves did not fare so well. The curve fitter was designed to be able to fit to the single exponential model, which as stated previously has always been considered to be the better model for amorphous cells which do not exhibit such a sharp 'knee' in theI/V curve. This fit ability was effected by holding I_{s1} at zero and allowing A to vary during the curve fitter iterations. Out of the fifty data sets used, only twenty-five of them gave rise to valid single-exponential model parameters. The other twenty-five sets either converged to parameters which were nonphysical (less than zero) and unacceptable or failed to converge at all. The ones that did fit required considerably more iterations of the curve-fitter to achieve a reasonable accuracy, and then did not show quite as good a fit as all of the polycrystalline I/V sets did. It was possible to get more of the data sets to fit, with only a few rejections, by increasing the limit upon the maximum number of iterations, but the quality of the fits were still not as good after a considerably greater number of iterations.

The extraction process was repeated and a new set of experimental I/V curves produced in an attempt to eliminate any possibility of error in the original I/V data - this did not make any difference. There appeared to be no obvious relation between the I/V sets that did fit and the irradiances or the temperatures, of them.

It was not until recently that some work was carried out which appeared to suggest that perhaps the single exponential model was not necessarily the best suited model for amorphous cells, and that the model equation itself may be at fault [30]. With the amorphous cell I/V data failing to always fit to the single exponential model, and the validity of the single exponential model itself indeed under question, it was decided to abandon the amorphous cell and proceed with the characterization of the polycrystalline cell model. The interest here is in power electronics as opposed to array device equations, and a model based around the double-exponential equation would in itself be of use in applications that use cells that fit the model, such as polycrystalline types. The technique used for the determination of the irradiance/temperature - model parameters

may still be able to be applied to a modified model for the amorphous cell, although if the base model equation is modified the curve-fitting algorithm will also have to be modified to fit to it.

2.10 Second level fit - double exponential parameters to irradiance and temperature

A small block of code was written to dump the double-exponential model parameter sets from the fitted data to a comma-delimited ASCII text file to allow them to be imported into a charting package. This package allowed the parameters to be plotted alongside temperature and irradiance. A further block of code was written to evaluate the parameter variation equations as they were developed and export a further block of ASCII text containing the calculated parameters at the same values of temperature and irradiance in order to allow superimposition of the fitted values for the parameters upon the same graphs.

The parameters were plotted against temperature and irradiance, the plot being used as an aid to determine the nature of the relationships involved. The behaviour of I_{ph} with irradiance is known to be linear, and the temperature dependence has been defined in equation **(3)**.An equation combining the two relationships in a manner that led to a good fit of the experimental data may be seen in equation **(32)**

$$I_{ph} = K_0 E(1+K_1 T) \qquad (32)$$

where the constants are to be determined. **Figure 12** shows the plot of the experimentally-derived values of I_{ph} together with the values obtained when equation **(32)** is fitted to it using a straightforward linear chi-squared minimizer [27]. The five different irradiance values can clearly be seen, the value of I_{ph} increases with increasing irradiance. The fit yielded the values of constants K_0=-5.729e-7 and K_1=-0.1098.

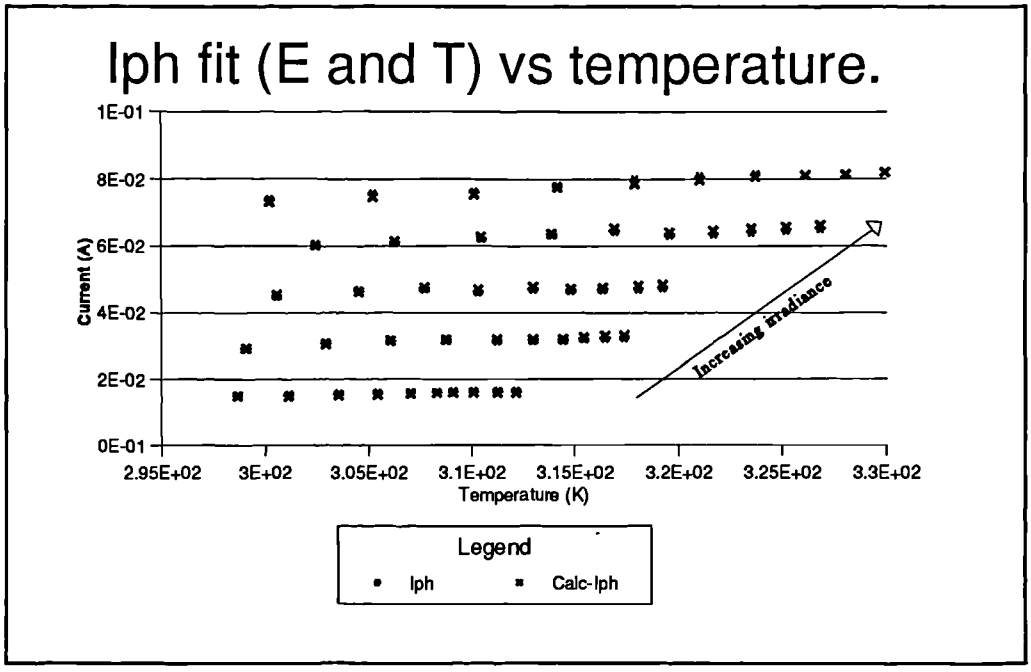

Figure 12 Variation of I_{ph} with temperature and irradiance, together with fitted points.

The two saturation currents have a temperature dependence which follow **(33)** and **(34)** respectively as they are proportional to n_i^2 and n_i, respectively, where n_i is the intrinsic carrier concentration of the semiconductor material. V_g is the band-gap voltage [23]. The equations themselves are very similar:

$$I_{s_1} = K_2.T^3.e^{-\left(\frac{eV_g}{kT}\right)} \tag{33}$$

$$I_{s_2} = K_4.T^{\frac{3}{2}}.e^{-\left(\frac{eV_g}{AkT}\right)} \tag{34}$$

These equations are not necessarily complete as they do not contain a possible irradiance dependency. Lumping $-(eV_g/k)$ and $-(eV_g/Ak)$ into the constants K3 and K5 respectively gives **(35)** and **(36)**.

$$I_{s_1} = K_2.T^3.e^{\left(\frac{K_3}{T}\right)} \tag{35}$$

$$I_{s_2} = K_4.T^{\frac{3}{2}}.e^{\left(\frac{K_5}{T}\right)} \tag{36}$$

The natural logarithm of I_{s1}/T^3 was plotted against temperature, as was the natural logarithm of $I_{s2}/T^{3/2}$ in order to linearize the equations so that a simple linear chi-squared minimizer may be used. The linearization allows the temperature dependance to be clearly seen and any irradiance dependance may be then more easily determined. These plots are shown in **Figure 13** and **Figure 14**. The different style markers represent the values of $\ln(I_{s1}/T^3)$ in **Figure 13** and $\ln(I_{s2}/T^{2/3})$ in **Figure 14** for each of the five nominal values of irradiance.

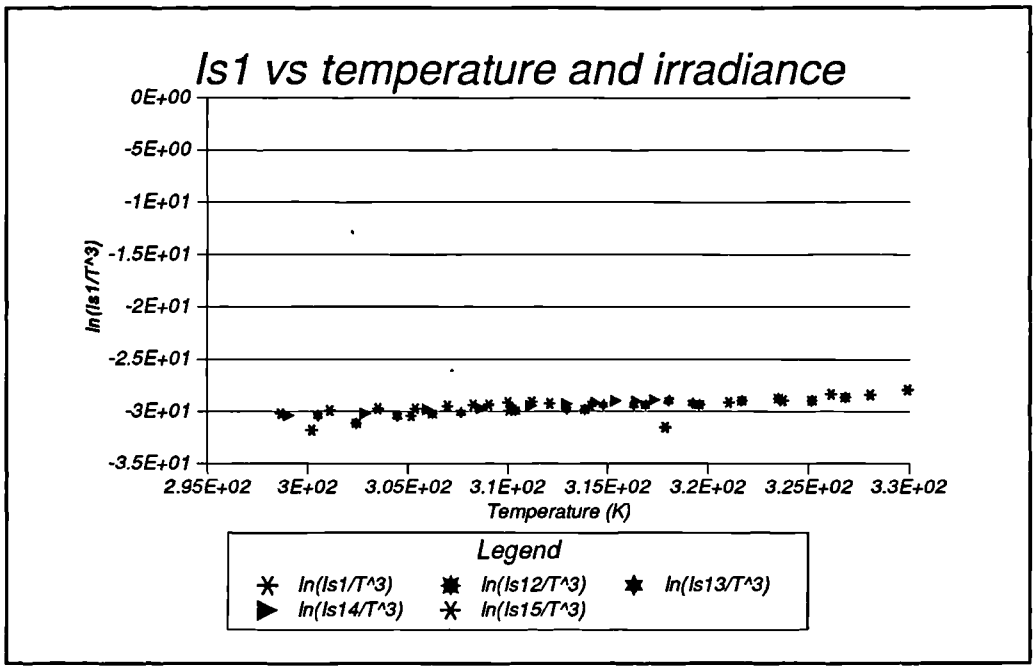

Figure 13 Variation of $\ln(I_{s1}/T^3)$ with temperature

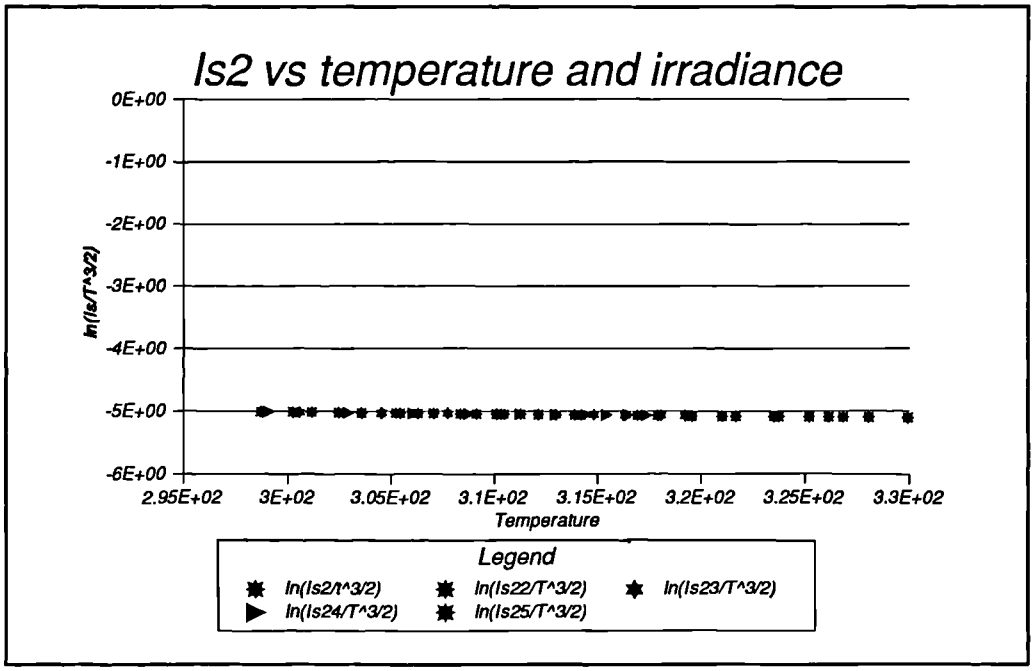

Figure 14 Variation of $\ln(I_{s2}/T^{3/2})$ with temperature.

Figure 13 and **Figure 14** show no variation of either of the saturation currents with respect to irradiance, but they do show that the temperature dependence is as expected. Fitting the linearized versions of these equations yielded values for K2 to K5 and chi-squared values as follows:

K2= 4.453e+1

K3= -1.264e+4

K4= 1.180e+1

K5= -7.317e+3

A plot of the values of Is1 and Is2 against temperature, together with the fitted curve, is shown in **Figure 15** and **Figure 16**. There is clearly no visible dependence upon irradiance of these parameters.

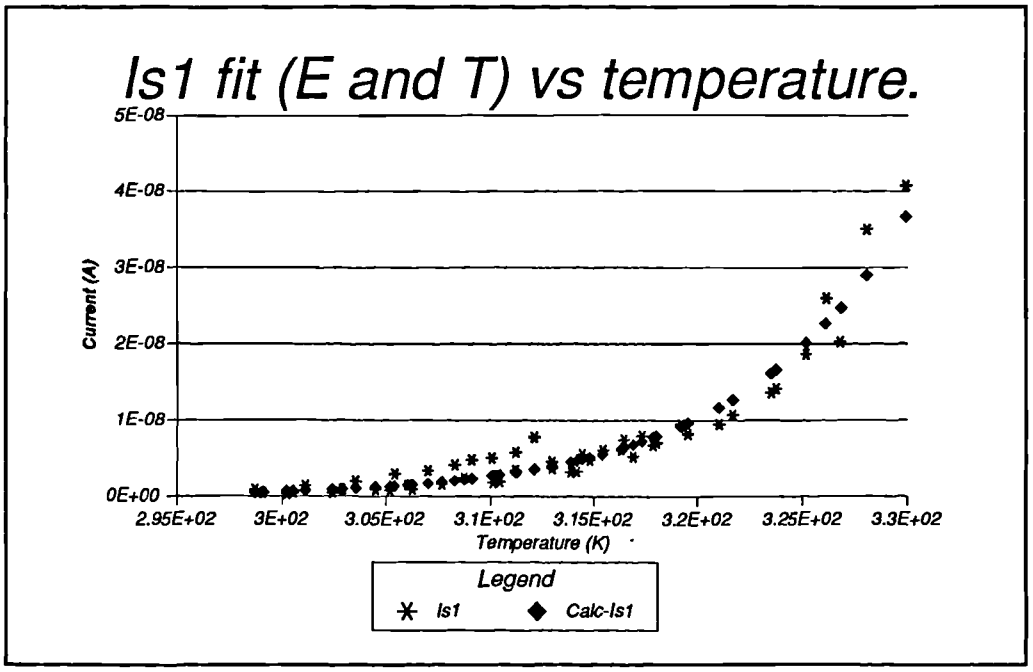

Figure 15 Variation of all values of I_{s1} with temperature, together with corresponding fitted points.

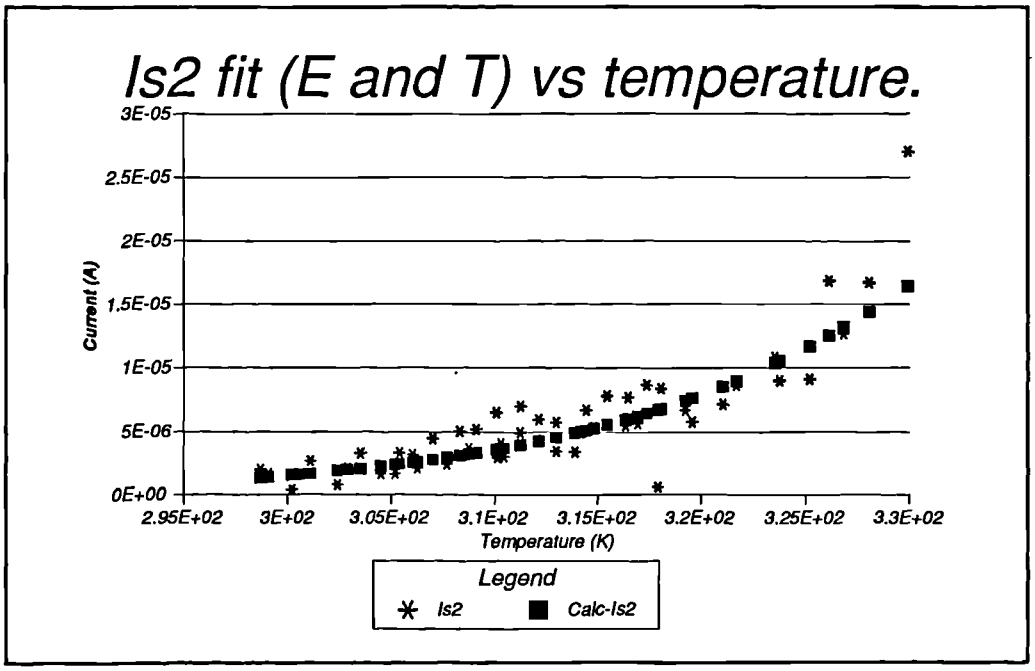

Figure 16 Variation of all values of I_{s2} with temperature, including corresponding fitted points.

The parameter A is held constant at a value of 2 in the double-exponential case, but if it was allowed to vary with temperature it would follow the linear relation given by **(37)** (from

[23]). Code was implemented to fit this using a linear chi-squared minimizer in anticipation of the use of the single exponential model, although in the double exponential case it is held constant by the first-level curve fitter at a value of 2..

$$A = K_6 + K_7 T \tag{37}$$

The linear curve-fitter thus simply returned a value of K6=2 and K7=0, as A is held constant at 2 over all double-exponential model parameter sets.

R_s, the series resistance, varies in both temperature and irradiance, as **Figure 17** shows. The form of the temperature dependence is known to be linear from equation **(6)**, but the irradiance dependence does not appear to have been investigated. The irradiance dependence appears to dominate over the temperature dependence.

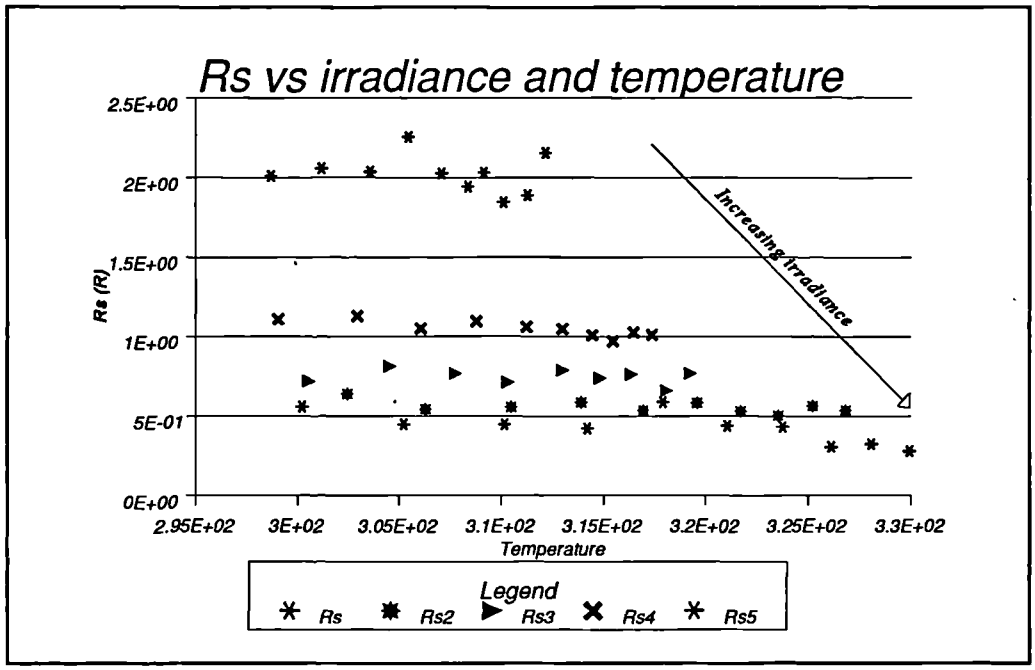

Figure 17 Variation of R_s with temperature and irradiance

The temperature dependence is indeed clearly linear, but the irradiance dependence is not. At first this was thought to be exponential owing to its appearance, but experiments with a non-linear curve fit showed it not to be. It was found to be an inverse-proportionality, and plotting $1/R_s$ with respect to irradiance confirmed this. As a result equation **(38)** was written and fitted.

The fitted curves are shown superimposed upon the experimental data in **Figure 18.** The fit of (38) yielded the following values for the constants therein:

$$R_s = K_8 + \frac{K_9}{E} + K_{10}T \qquad (38)$$

K8 = 1.470

K9 = 1.612e+3

K10 = -4.474e-3

The constant term in (38) comes about due to the component of Rs formed by the ohmic contact and bond-lead resistance of the cell, this is not irradiance dependent, and its temperature dependence is accounted for in the third term.

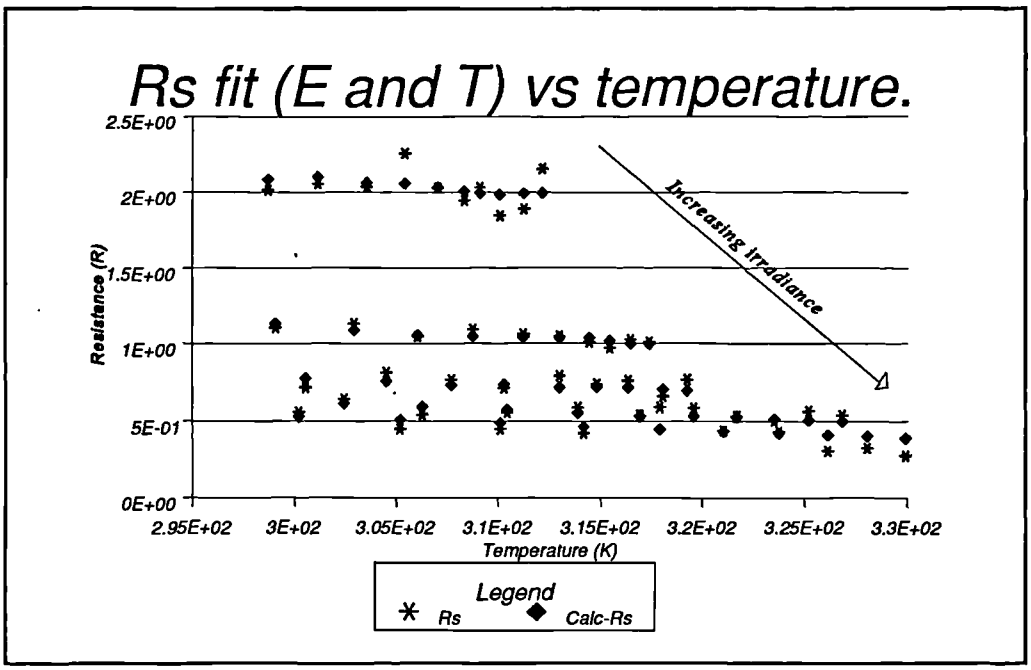

Figure 18 Variation of R_s with temperature, with corresponding fitted points superimposed.

R_p, the parallel or shunt resistance, is known to display an exponential relationship with temperature [23] as shown in equation (39). The natural logarithm of R_p was plotted against

temperature and this is shown in **Figure 19**. There is no dependence upon irradiance and the constants determined as a result of the linear curve fit were as follows:

$$R_p = K_{11} e^{K_{12} T} \tag{39}$$

K11 = 2.303e+6

K12 = -2.812e-2

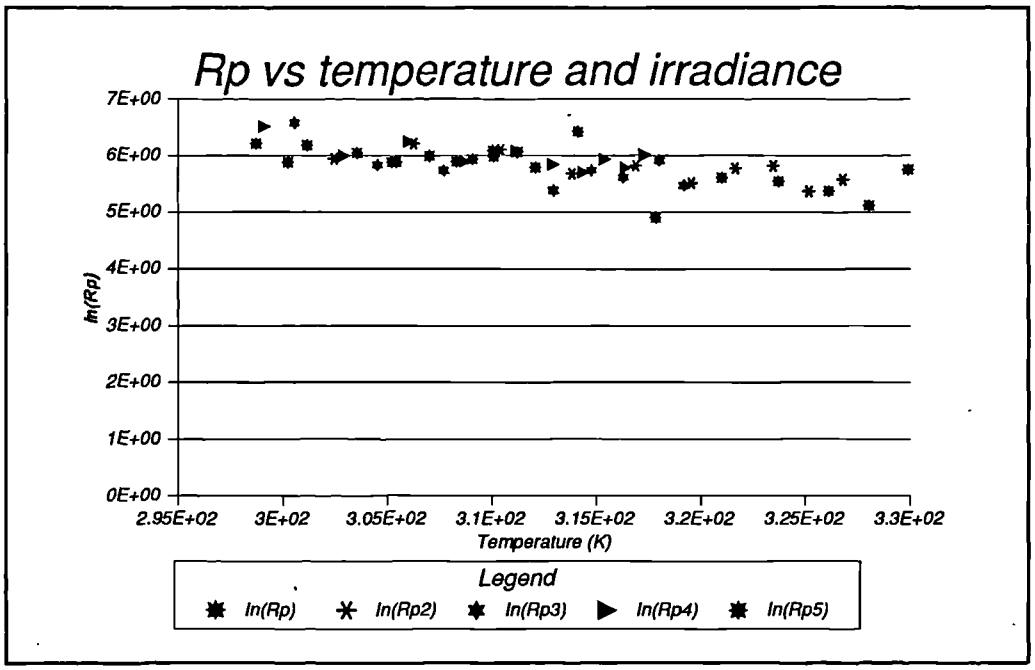

Figure 19 Variation of the natural logarithm of R_p with temperature.

Figure 20 shows the variation of R_p with temperature, with the corresponding fitted points superimposed.

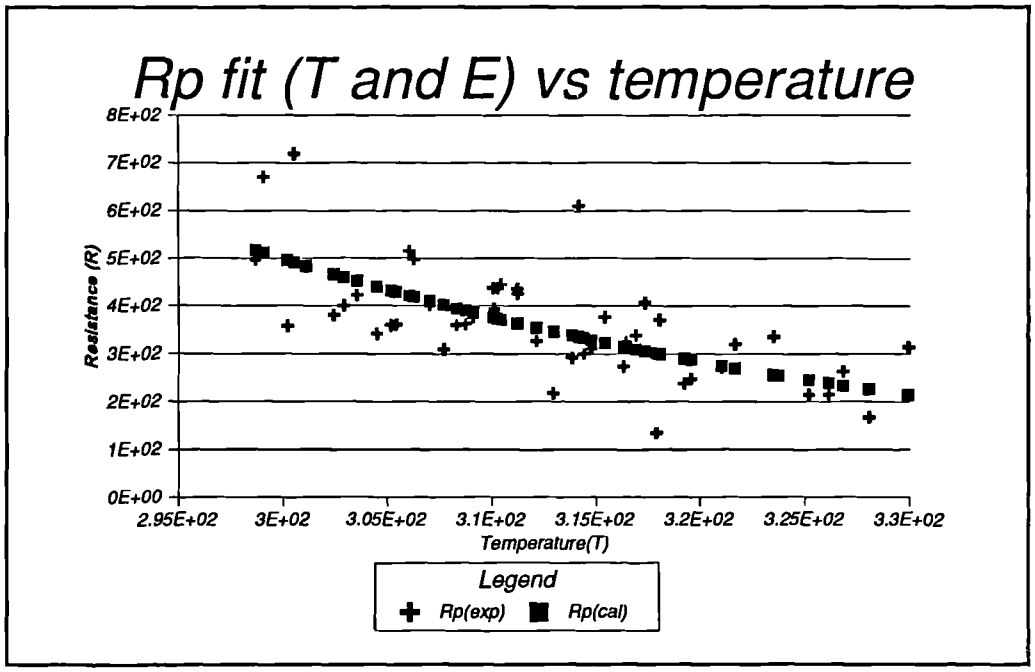

Figure 20 Variation of R_p with temperature, with the corresponding fitted points superimposed.

The overall result of the described modelling system is a set of equations which model the behaviour of the double exponential parameters with respect to temperature and irradiance. Two of the parameters, I_{ph} and R_s exhibit irradiance dependence, while all the parameters exhibit temperature dependence to varying degrees. The irradiance dependence of R_s is quite noticeable, and since the value of R_s bears considerable relation to the position of the maximum power point the incorporation of this term into the model equations is quite important.

The accuracy of determination of K_0 through K_{12} depends upon the accuracy of, and amount of, cell characteristics at different values of irradiance (E) and temperature (T). Obviously the more curves obtained at individual E and T values the more accurate will be the parameter fit. Fifty values seemed to be quite a reasonable compromise between time taken during the first level fit, and accuracy of the second level fit. The ASCII data export has been incorporated into the final version of the parameter extraction system, thereby allowing for manipulation and further plotting of the data by way of a spreadsheet or similar. An on-screen plot of the parameter values versus temperature and irradiance is available, with the fitted values superimposed - this may be used to visually verify the fit if so desired. The PostScript™ -compatible X-Y plotting engine was

developed and incorporated into both the curve-fitter and extraction package in addition to the acquisition package. It can also generate encapsulated-PostScript files and all plots that are obtainable on-screen from either package may now be printed using a PostScript printer, or saved as an encapsulated-Postscript file for importing into another document.

Finally, any simulation package, capable of modelling a component from the characteristic equation and accepting run-time parameters, may be used to provide the circuit model. This system need not only be used in conjunction with the Saber template. The circuit-level simulator simply accepts, as parameters, values of the constants K_0 through K_{12} together with a temperature and irradiance value. The parameters K_0 to K_{12} do not change for a given cell, therefore this has reached the goal of developing a modelling system that effectively consists of a 'black box' with temperature and irradiance as input, and two electrical terminals as output. Providing values for K_0 through K_{12} can be determined for a given cell, the template is capable of modelling that cell across its operating range of irradiance and temperature. For example, a PSPICE model may be developed from **(1)** and if PSPICE was the system to be used to simulate the power electronics.

2.11 Summary of complete model equation set

The required relationships between the environmental parameters E and T and the double exponential model parameters have now been defined and are shown together below in equations **(40)**-**(44)**.

$$I_{ph} = K_0 E\left(1 + K_1 T\right) \tag{40}$$

$$I_{s1} = K_2 . T^3 . e^{\left(\frac{K_3}{T}\right)} \tag{41}$$

$$I_{s2} = K_4 . T^{\frac{3}{2}} . e^{\left(\frac{K_5}{T}\right)} \tag{42}$$

$$R_s = K_8 + \frac{K_9}{E} + K_{10}T \tag{43}$$

$$R_p = K_{11}e^{(K_{12}T)} \tag{44}$$

The thirteen constants K_0-K_{12} provide the model with the information specific to a sample of polycrystalline cell. Any such sample may be characterized using this system to generated a set of constants specific to the cell. The MAST template, running under Saber, or indeed the modelling system for any other simulator will accept constant parameters of K_0-K_{12}, and two variable parameters of E and T (which may be changed during a simulation run in order to simulate changes in irradiance and temperature). It simply has to solve, at each simulation time step, equations **(40)**-**(44)** followed by the double-exponential model equation **(1)** in order to simulate the electrical behaviour of the cell. The constants for the cell used during the tests together with the chi-squared value of the fit may be seen in **Table 2**.

Table 2 Table of constants for polycrystalline cell used in tests.

Parameter	Constant values		
I_{ph}	K_0: -5.729e-7	K_1: -0.1098	
I_{s1}	K_2: 44.5355	K_3: -1.264e+4	
I_{s2}	K_4: 11.8003	K_5: -7.3174e+3	
A	K_6:	K_7: 0	
R_s	K_8: 1.47	K_9: 1.6126e+3	K_{10}: -4.474e-3
R_p	K_{11}: 2.303e+6	K_{12}: -2.812e-2	

It is possible for the characterization system to export scatter-graphs showing for each of the double-exponential model parameters, the position of the parameters extracted from the experimental I/V curves and the values of the parameters obtained from equations **(40)**-**(44)** on

the same pair of axes, either to a base of irradiance or temperature. The curves for the polycrystalline cell are shown in **Figure 21-Figure 26**. Experimental data is marked with a circle, whereas points calculated from the model are marked with a cross.

To avoid cluttering the graphs the irradiance figures have been left off the curves - they may be easily determined as the clusters on the graphs of parameters which exhibit an irradiance dependance are in order. The experimental irradiance values used are 4000arb, 3000arb, 2500arb, 1500arb and 1000arb. The photocurrent rises with irradiance. R_s is inversely proportional to irradiance. These curves demonstrate that the model captures the behavioural trends of the polycrystalline cell very well.

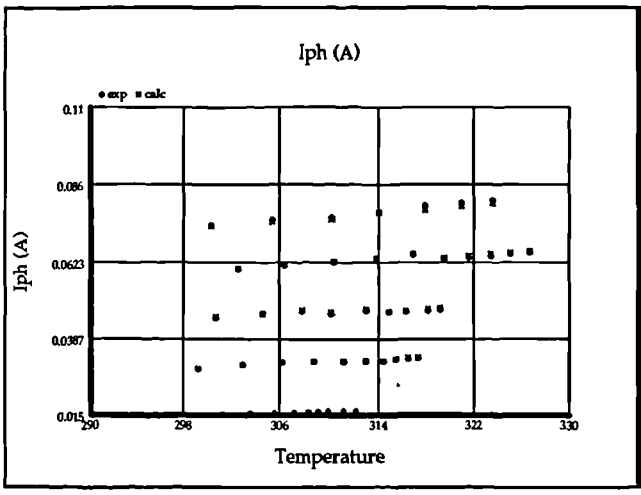

Figure 21 I_{ph} versus temperature

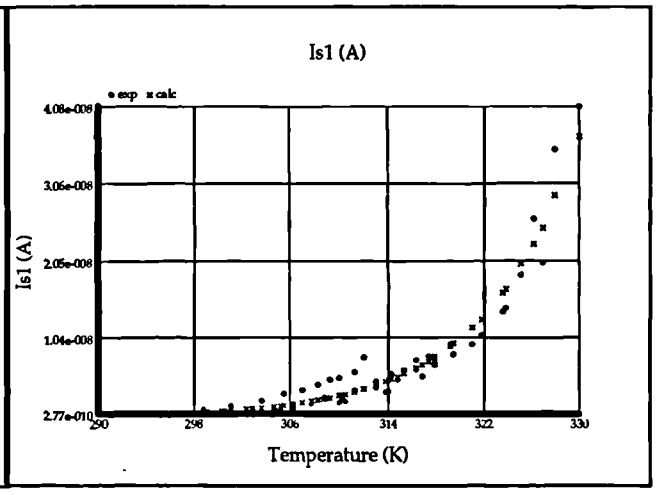

Figure 22 I_{s1} versus temperature

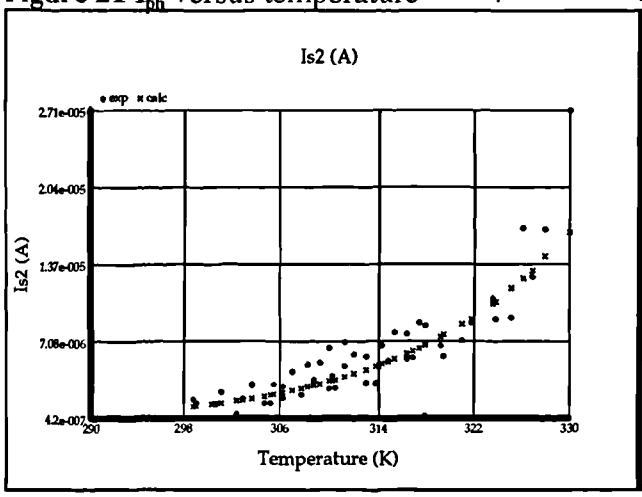

Figure 23 I_{s2} versus temperature.

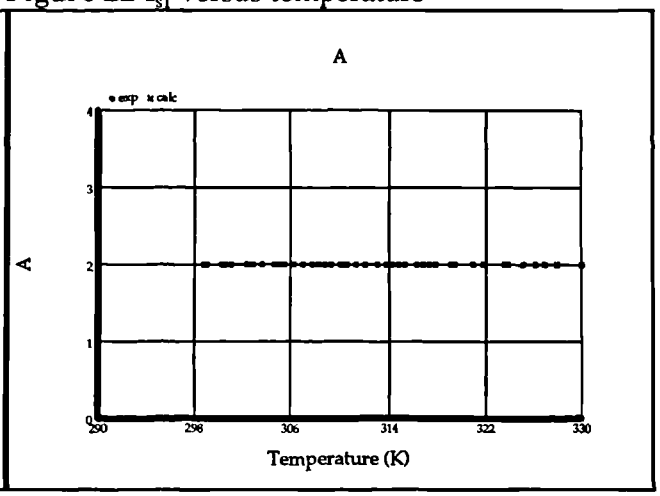

Figure 24 A versus temperature.

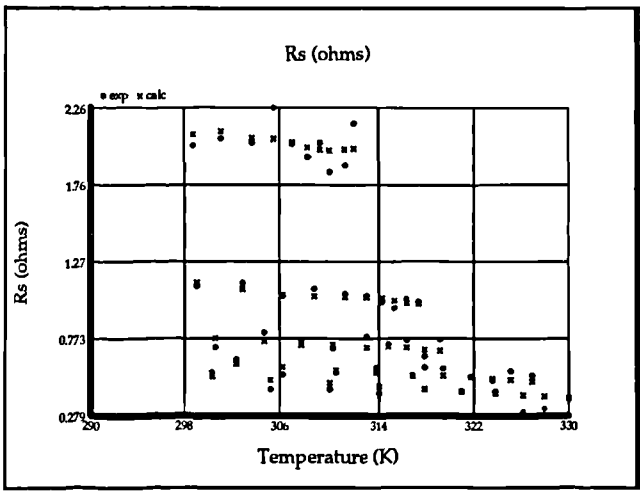

Figure 25 R_s versus temperature

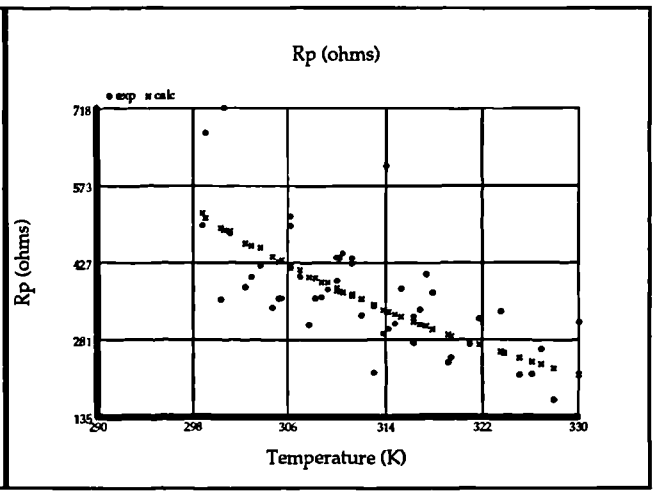

Figure 26 R_p versus temperature

2.12 Saber model

The Saber model, coded in MAST, is quite simple. The modelling system developed is based around the characteristics of a single PV cell.The models of the cells are such that if connected in an array the array can be treated (mathematically) as a single cell with multipliers incorporated accordingly dependent upon the number of series/parallel chains in the array. This only holds if the irradiance and temperature are constant across the entire surface of the array. For a small array (c. $1m^2$) this is likely to be true. However for a field of arrays such as encountered in a large photovoltaic plant this may well not be the case - and the simulated array would have to be constructed from discrete Saber cell templates each representing the appropriate combination of cells, as necessary. **Figure 27** shows the arrangement of an m x n array, while **Figure 28** shows the decomposition for a 2x3 array as an example.

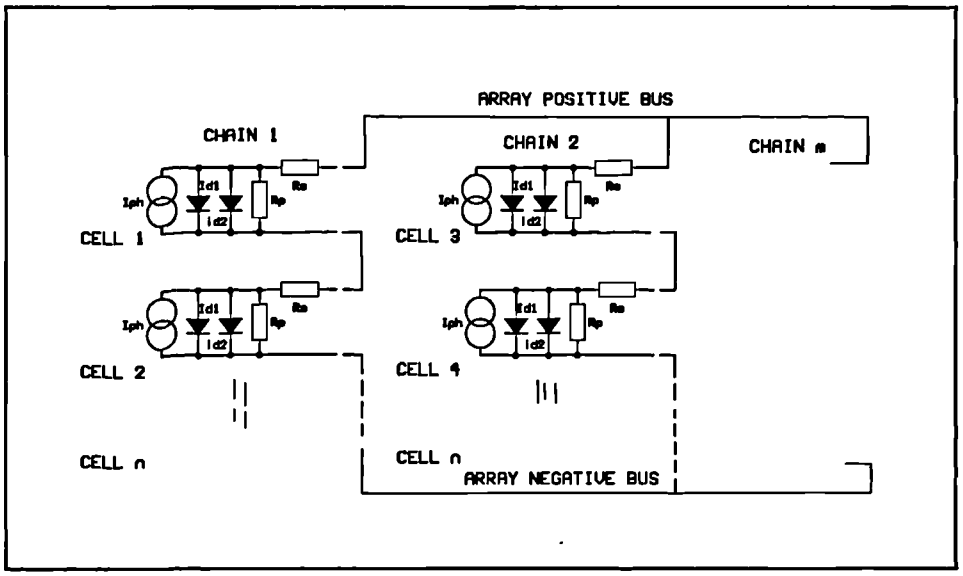

Figure 27 Cell connections forming an array.

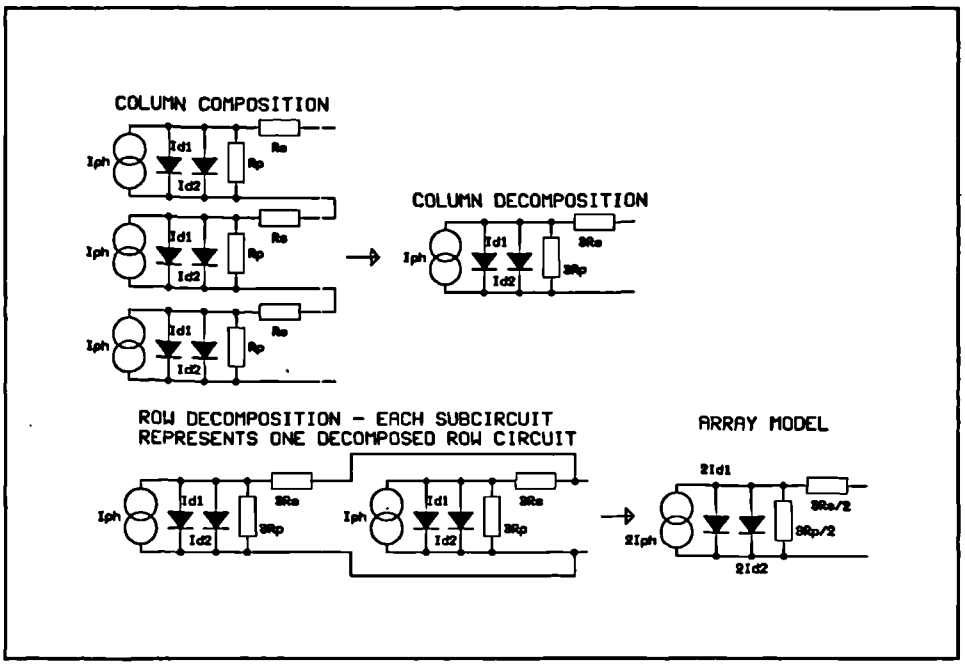

Figure 28 Array decomposition to form composite model.

The parameters add by superposition to an extent, with the exception of the two diode currents. As these are nonlinear, a multiplier N_s must be placed within the exponential term. Depending upon the design and dimensions of the array it may be possible to simulate the array by collapsing the series chains into a number of paralleled modelling units - or in the case of a large plant the best approach may be to collapse the model of each panel into a single modelling unit, as the irradiance, and hence the temperature, is unlikely to change across the dimensions of

a single panel but could possibly change across the plant in its entirety. Either way, the modelling system opted for gives the greatest flexibility in the manner in which the array may be simulated - the effect of a cloud passing could be simulated by reducing and increasing the irradiance across the plant in a 'Mexican wave' fashion, for example.

In **Figure 27** and **Figure 28** the two diode currents I_{d1} and I_{d2} are the solution of the second and third exponential terms in equation **(1)** - thus in the composite models, to represent series chains, the IV equation must incorporate the N_s multiplier. The complete multidimensional array model equation is shown in equation **(45)** below.

$$I = N_p \left[I_{ph} - I_{s1} \cdot \left(e^{\frac{e\left[\left(\frac{V}{N_s}\right)+\left(\frac{I}{N_p}\right)R_s\right]}{kT}} - 1 \right) - I_{s2} \cdot \left(e^{\frac{e\left[\left(\frac{V}{N_s}\right)+\left(\frac{I}{N_p}\right)R_s\right]}{A.kT}} - 1 \right) - \frac{\left(\frac{V}{N_s}\right)+\left(\frac{I}{N_p}\right)R_s}{R_p} \right] \quad (45)$$

where N_s and N_p are the number of series cells, and the number of parallel cells, respectively.

The actual implementation in MAST is very straightforward - consisting of a solution to equations **(40)**-**(44)** followed by a solution to **(45)**. The constants K_0-K_{12} together with the environmental variables temperature and irradiance are passed to the template through fields in a solar-cell symbol designed for the DesignStar schematic-capture utility front-end. Although temperature is required by the model, it is a global variable within the Saber environment and does not need to be passed through the template parameter field. The parameter 'EI' in **Figure 29** is irradiance. The symbol has terminals to which the load may be connected in the schematic of the system it is wished to simulate, and the symbol may be seen in **Figure 29**.

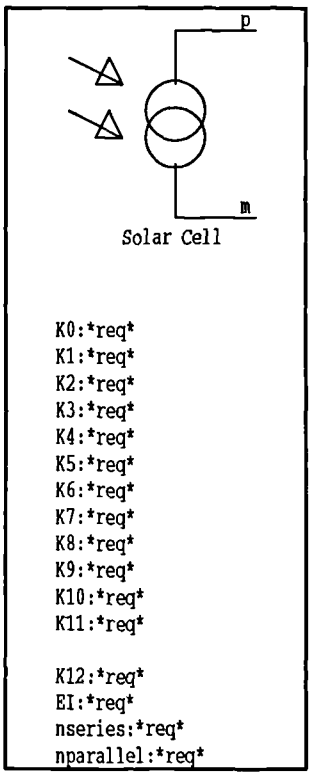

Figure 29 PV cell symbol. using DesignStar in Saber.

2.12.1 Saber model result

As a demonstration of the output of the Saber model, **Figure 30** shows a sample data set from those extracted from the cell

including the power curve for the cell. The I/V and power data back-calculated from the model is also superimposed upon the curve and serves to show the accuracy of the fit. **Figure 31** is an I/V sweep taken from the Saber model at the same irradiance and temperature as **Figure 30**, and using the constant K_0-K_{12} set extracted. It can be seen that the curves are virtually identical.

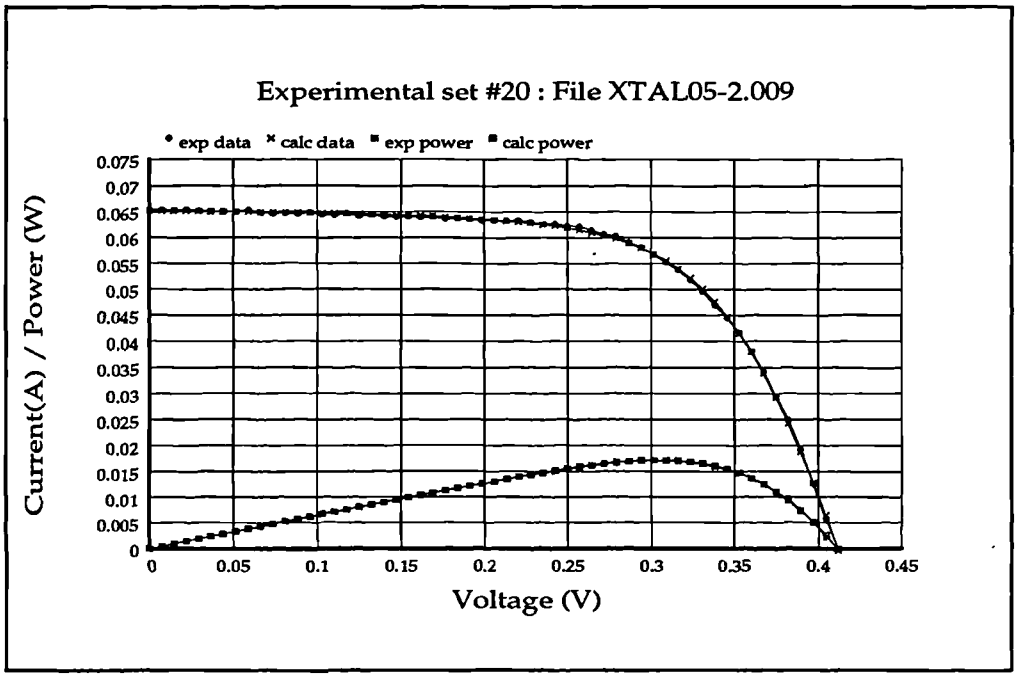

Figure 30 Experimental I/V data at irradiance: 3291 temperature: 326.8

2.13 Summary

A model has been developed for the polycrystalline cell, and has been published in a concise form in reference [31]. This model can be applied to other photovoltaic cell types whose device physics conform to double-exponential behaviour. Using this system, cell samples may be characterized to obtain a set of constants. If these constants are submitted to a circuit-level simulation template the electrical behaviour of arrays of cells may be simulated across the range of irradiance and temperature for which the model has been defined. In the context of power electronics, there is now available a model for a photovoltaic array installation which will allow the effects of varying irradiance and temperature to be simulated in conjunction with a power conversion system. This will enable the behaviour of the power conversion system to be analyzed and optimized for operation in the field of solar photovoltaic power conversion.

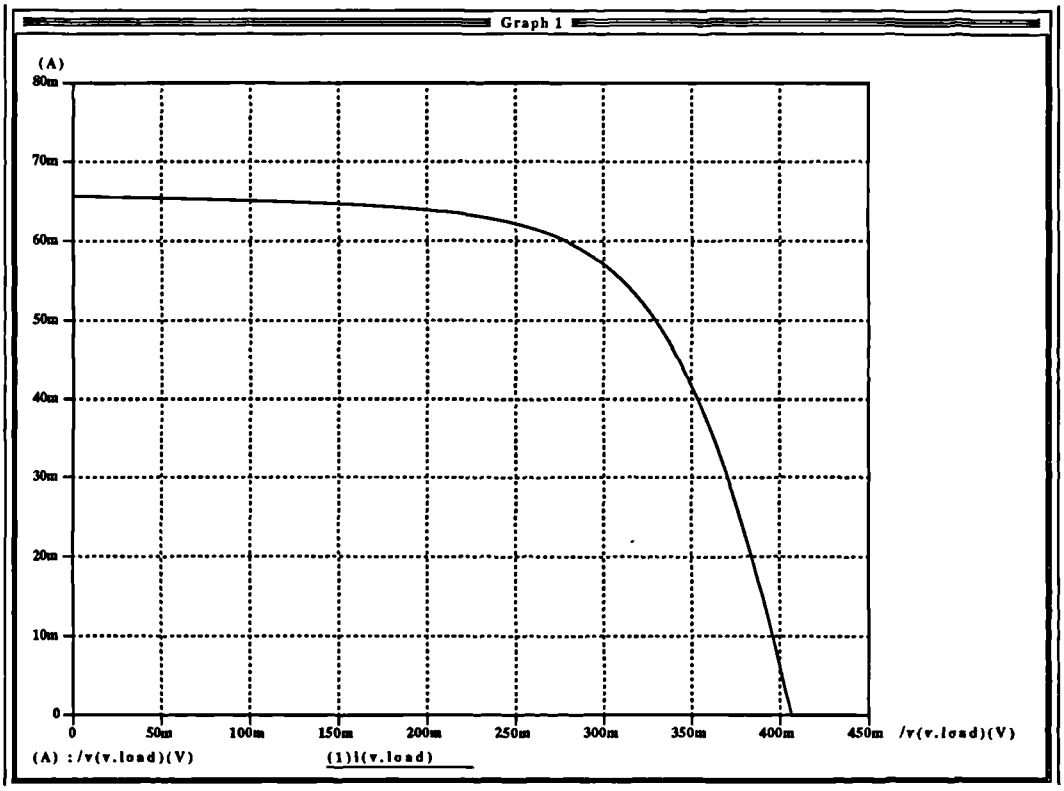

Figure 31 I/V sweep obtained from Saber template using extracted parameters at irradiance: 3291.3 temperature 326.8K

SECTION 3: Development of PV array interface: front end

A flexible converter capable of operating in both category 2 and category 3 (see section 1.4.1 for a definition of the categories) can be developed by employing a 'modular' approach similar to that of [32], that is a d.c. to d.c. converter followed by a separate inverter module. This arrangement may be seen in **Figure 32.** To drive d.c. loads, only the initial power conditioning and conversion stage is required in order to match the characteristic of the PV array to the load. This receives energy from the PV array and converts it to a constant d.c. voltage. Should it become necessary to drive an a.c. load, an inverter stage may be coupled to the output of the first stage. The difference in drive requirements between a live a.c. load and a 'dead' one is simply a matter of the manner in which the inverter is controlled, so the change in operating mode may be taken up easily by the flexibility inherent in a digital control scheme. To this end, in a category 2 application where the load is a refrigerator or a d.c. motor in an irrigation system only the first stage of the converter system would be required.

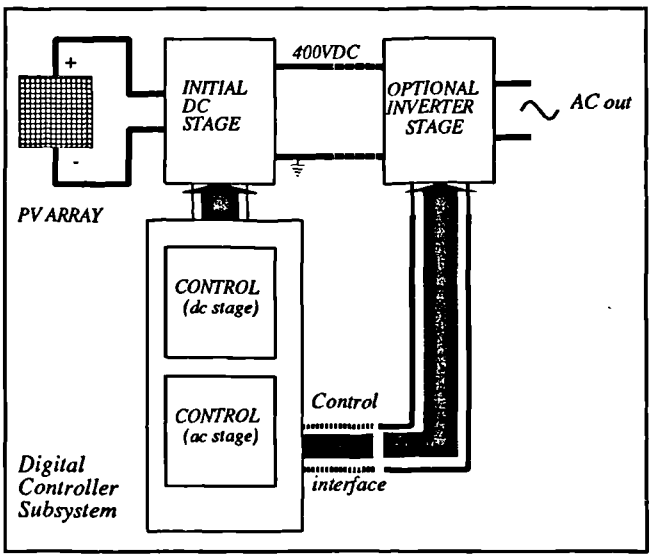

Figure 32 Overview of power conversion system.

In a category 1 or 3 application the inverter stage would be added with the associated control arranged for a live a.c. load, while a category 2 application where (for example) an induction motor is being driven the inverter stage would be required with the control arranged for a 'dead' a.c. load. If efficiency of the individual converter stages is maintained at a very high level, then this system would be of considerable value if for no other reason than it is not dedicated to any specific use and may continue to be used should the load requirements of the photovoltaic

installation change. If, for example, a grid connection became available and it became viable to connect an existing stand-alone system to the grid it would only be necessary to add an inverter stage in the case of an existing d.c. system, or in the case of a stand-alone a.c. system to reprogram the controller. This would be considerably cheaper and much more environmentally sound than to remove and dispose of the existing converter system in order to renew it completely. Providing the efficiency of the d.c. and inverter stages is kept high, and that the inverter is designed to require low, or better still zero maintenance, then this avenue of system structure would appear to be the most desirable.

3.1 Overview of this section.

The front end is the key aspect of the system as it provides the matching between the characteristic of the PV array and the load, be it inverter or a d.c. load. It is here where the control must be arranged to allow the front end to drive both a load requiring maximum power and also to loads requiring a regulated d.c. voltage. It was with the front end where the initial power electronics development was undertaken. The power chain topology of the front end will be described, followed by an analysis of existing conventional converter control strategies in order to determine just why they are not always suitable for PV applications in their standard form. A novel control arrangement using an embedded maximum power tracking scheme will then be described and a full set of simulation results presented to demonstrate its performance.

3.2 Front end converter design - source and load

A PV array has a characteristic which for each specific value of temperature and irradiance will exhibit a definite point of maximum power. An example of such a curve may be seen in **Figure 2**. It may be said that below the maximum power point, the source is closer to a current source, while above the maximum power point the source approaches a voltage source. This may be seen from looking at the equivalent circuit for the cell (**Figure 3**). At low cell load currents most of the photocurrent I_{ph} is flowing down the diodes and the parallel resistance thus creating a voltage drop across them. Light loads will draw current away from the diodes, but the slope of

the diode curves at this point is such as not to cause the voltage across them to change by a large amount. The cell thus approximates a Thevenin (voltage) source at light loads as the cell voltage does not change much with cell current.

At heavy currents, most of the photocurrent is flowing into the load. The diodes are operating at the bottom of their characteristic where little current is flowing in them, and their effects can largely be ignored in this condition, as can the effects of the parallel resistance R_p which is large and also will be passing very little current. With heavy loads, therefore, where the load current is approaching the short circuit current the cell will appear as a Norton (current) source. At the maximum power point, the cell could be considered as approximating either a Norton or a Thevenin source. The cell may be considered a current generator in parallel with a resistance which will vary as a nonlinear function of the load current.

When designing a conversion system for such a source, both the input characteristics (fixed by the requirements of the cell characteristics) and the output characteristics (specified by the designer for matching to appropriate loads) must be defined. In this case the requirements were fairly simple: match the solar cell characteristics using a converter to produce a constant 400V d.c. output voltage with high efficiency.

3.3 Converter requirements

A regulated 400V output of the first stage allows ease of development of inverters for coupling to a 240Vrms grid (such as the UK mains). This forms the first of the modules in the 'modular converter' system. The overall control scheme will be implemented within a single digital controller subsystem, which can directly generate pulse-width modulated (PWM) signals to drive the switching devices.

3.3.1 Array specifications

Developmental capabilities aside, domestic applications suggest a limited area in which to place photovoltaic arrays (the roof area of an average domestic dwelling) and it was initially decided to work around a 'nominal' power figure of 1kW. There is also a safety issue to consider: the characteristic of **Figure 1** clearly shows that an arc could easily be sustained under fault conditions.

The desire to develop a system which is array-independent (although there will always be a nominal, maximum and minimum input voltage specification), together with the wide range of values of solar irradiation that will be encountered requires that the converter system be able to operate over a very wide range of input voltages. In fact, the array open circuit voltage does not vary a great deal with irradiance (E), but does exhibit significant variation with temperature (T). **Figure 33** was generated by Saber for the cell modelled in section 2 and shows this variation as a family of curves, one at each value of temperature, of array open circuit voltage as a function of irradiance. It is interesting to note that the open circuit voltage *variation* with irradiance (due largely to the R_s dependence upon irradiance) is constant with temperature except at very low levels of irradiance and that this variation is small across a wide range of irradiance compared with the much larger variation of open circuit voltages across the operating temperature range. Since the cells are dark in colour they tend to run hotter at higher levels of solar irradiation so there is an overall variation of cell voltage which tends to alter the position of the maximum power point (as well as its magnitude). As seen previously the variation in E affects the maximum amount of current that the cell can supply and therefore the maximum power available from the cell. The choice of switching converter topology is somewhat dependent upon the source type as well as the load. In this case it is desirable to start with a low maximum array open circuit voltage of 200V to reduce both the likelihood of arcing and fire in the event of a fault, while at the same time not requiring too high a boost ratio in order not to push the converter into regions of inefficient operation at extremes of its operating range. For a given array power, if the number of series chains of cells in the array, and hence the array voltage, is reduced, then to maintain the same power output the number of parallel chains must be increased so that the total number of cells in

the array is the same. This will increase the current output from the array for a given power level and the higher current will increase power dissipation in any resistive elements in the converter. On the other hand, if the nominal array voltage is raised and the current reduced by connecting more of the cell chains in series then a limit will be reached due to the maximum voltage ratings of switching elements. A compromise between these limitations of the converter and the limitations of the array is what forms the basis for the choice of nominal array input voltage. This will vary across a considerable range with temperature and irradiation.

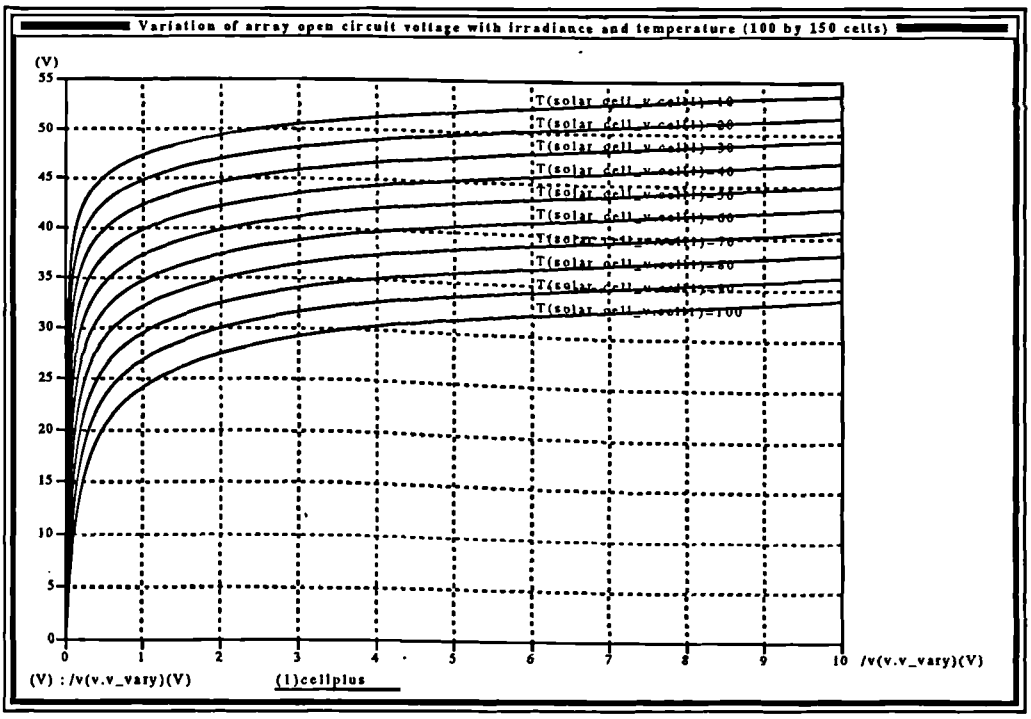

Figure 33 Variation of V_{oc} of a PV array with irradiance and temperature as a parameter: temperatures in Celsius, irradiance in arbitrary units $x10^{3}$.

3.3.2 Load specifications: first stage

The converter may be considered as an impedance-matching system, where the complex varying source-impedance of the solar array must be matched to a load which requires a supply of a voltage source with low source resistance. However, the characteristics of the arrays being

what they are (**Figure 1**) it is clear that it would be impossible for the load to draw more power than the array may supply. The array terminal voltage will fall off as more current is drawn. If a power system is thus to provide a steady d.c. (or a.c. through an inverter) voltage to a 'dead' load, and that load starts to demand more than the maximum power available under current environmental conditions, then a converter can not maintain its output voltage. When feeding distribution systems it is desired to pass as much power as is possible from the arrays to the distribution system and in these circumstances the front end control must ensure that the array/inverter interface is always operating at the maximum power point on the array characteristic. The position of this can never be known in advance, and will also move within large bounds as a function of solar irradiance and array temperature, and must be determined from the array characteristic in real time by one method or another. As will be shown, standard inverter controls as would be used for a 'normal' voltage or current mode system with a fixed-voltage input must be modified and made adaptive, otherwise they will not function correctly once the array operating point moves beyond the maximum power point. Controllers must trap this condition and ensure that once the operating point traverses the maximum power point the control changes to a maximum power algorithm. This form of control holds the array current at that for maximum power over the duration of the load demand being greater than maximum power. Once the current demand falls below the current for maximum power the algorithm reverts to the conventional. This brief explanation serves to exemplify the importance of maximum power algorithms in the management and matching of photovoltaic array systems to a wide range of loads.

3.4 Converter topology

The choice of converter topology is based upon a number of factors. For example, is galvanic isolation required? What are the nominal source and load voltages and does the converter have to step up or down? Is continuous or discontinuous current required in the source, the load or both? In the case of this converter, the source and load voltages are already pre-defined, as is the power throughput. The upper limit upon converter input voltage is defined by the desired ratings of the silicon in the converter, and this limit must be specified as a maximum array open circuit voltage. In this case the upper maximum array V_{oc} has been set at 200V. As the input

voltage drops the converter boost ratio must increase, and the lower limit is governed both by regions of inefficiency of the boost converter at very high boost ratios due to the high currents encountered at the input, and the resolution of the sampling channels of the front end control system associated with the power electronics. In this case a lower limit of 50V was decided upon. This limit is the voltage at which array maximum power occurs, since at lower load powers the array terminal voltage will increase. The front end control system will initiate a shutdown if these limits are exceeded.

For the purpose of determining the values of the passive power handling components in the converter, a 'nominal' input voltage was used which was set at half way between the lower limit of input voltage and the maximum power voltage of an array with a V_{oc} at the upper input voltage limit. Since the voltage at the maximum power point is approximately 70% of the open-circuit voltage this gives a range between 50V and 0.7x200=140V. The mid point is at 95V, and a round 'nominal' input voltage of 100V was used in the calculations.

The output voltage and power specifications are 400V d.c. and 1kW respectively. Note that for d.c. output voltges below 400V but above the V_{oc} of the array the boost converter can still be used. Lower d.c. output voltages can only be achieved with the boost converter by using an array with an appropriately lower open circuit voltage i.e. $V_{oc} < V_{out}$. For a 400V output a step-up converter with a nominal boost ratio of 1:4. The question of continuous current is an interesting one. The load could be a single-phase inverter drawing sinusoidal current and hence pulsing power, thus the load current can be continuous or discontinuous.. It is thus necessary to design the converter with a capacitative output to absorb pulsing power. As for the source, although discontinuous current flowing in the array is not in itself a problem, it would prevent the converter from ever drawing maximum power continuously. There would be too large a current excursion between the off and on times - and during the off-times no power would be drawn from the array at all. A converter drawing continuous input current would always be superior in terms of efficiency as it would never have a period during which the array current (and hence power) would be zero. Continuous current would allow the converter input operating point to be placed

in the immediate vicinity of the maximum power point, and the operating point at the array would exhibit much smaller excursions.

It is interesting to note that some commercial designs make use of converters that have a discontinuous input current and avoid the problem by placing a large capacitor across the PV array in order to smooth out the variation [11]. However, it is valuable not to require large capacitors across the array for two main reasons. Firstly the array voltage will be smaller than the d.c. output voltage of the converter, requiring a higher value of capacitance to facilitate smoothing. Secondly, the array characteristic itself is (to a degree) fault tolerant. If the switching element is rated above the maximum short circuit current and a converter short circuit fault occurs, it is possible for the converter to draw only the maximum short circuit current from the array and the switching silicon in the converter will be protected providing it can withstand this current. A capacitor input will compromise this protection as the energy stored in the capacitor could well be sufficient to destroy the switches.

As to galvanic isolation, this is only really pertinent to grid-connected systems as stand-alone installations do not necessarily need to be isolated from the arrays [34]. Grid-connected systems are more at risk from failures in the inverter stages, and energy from the grid can also damage the power electronics, even to the arrays themselves. However, most modern grid-coupled systems can protect against such eventualities by way of breakers and fuses as well as fail-safe controls. Since the design of the inverter does not necessarily require galvanic isolation in the form of a transformer, there is no real need to include it unless local electricity supply regulations demand it and if this is the case it may be included as a 50Hz transformer at the output of the inverter section of this system [35]. This gives the requirements of the converter topology: the 150V (nominal MPP voltage) of the solar arrays must be boosted up to 400V d.c. from which up to maximum array power may be drawn. The array current must be continuous.

3.4.1 Boost converter topology

The specification would be easily met by a single ended boost converter. This topology is tried and tested. Such a converter is shown in **Figure 34**. The switching device used in the converter is intended eventually to be an IGBT, modern versions of these devices being fast enough for duty at 20kHz with higher voltage ratings than power-MOSFETS of similar silicon area. In a boost converter of this nature no reverse voltages are applied across the switch, and the maximum off state switch voltage can never be greater than V_{out} plus a diode drop. To speed up simulation generic MOSFET models from the Saber libraries were used during the simulation studies as these resulted in a faster simulation time than if IGBT models were used. This yields no significant difference as the drive characteristics of IGBTs and MOSFETS are not that dissimilar.

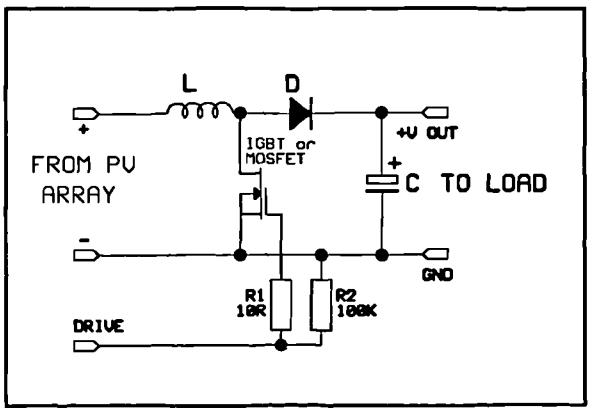

Figure 34 Skeleton schematic of single-ended boost converter.

3.5 Control algorithms, initial investigations.

In order to determine exactly what the pitfalls with the use of conventional control strategies in PV applications are, an investigation into the behaviour of a conventional continuous-mode boost converter control strategy when the converter is fed from the variable voltage and current source of the photovoltaic array was undertaken. The results of this provided all the information required to redesign the controller to make best use of the PV power source. Continuous mode operation was felt to be a necessity owing to the requirement for operation in close proximity to the maximum power point of the array characteristics despite the small-signal disadvantages of a boost converter in continuous mode.

With a conventional control arrangement, the requirement is to provide a fixed d.c. output voltage which is unaffected by line (input) or load changes over a predefined range; also that the transient characteristic of the output voltage in the system is within an acceptable bound for the system under consideration. The steady-state d.c. response of the converter and the small-signal a.c. response must be examined. The simplest way of performing this mathematically is to develop a linearized averaged state-space model for the boost converter [33] (or if it is not necessary to account for the effects of parasitics in the circuit a circuit-average model may be used). From the resulting equations, any small-signal or d.c. transfer function for any part of the system may be obtained.

For the boost converter, operating in continuous mode, the skeleton schematic of **Figure 34** is redrawn in **Figure 35** showing the state variables, the output and the input. A full set of working for both the state-space method and the circuit-averaged method (neglecting parasitics) may be found in [33] and the linearized state equations derived therein are given in **(46)** for both the small signal and the d.c. components of the state variables and duty cycle δ. From this equation set, all small signal and d.c. relationships may be derived for the converter.

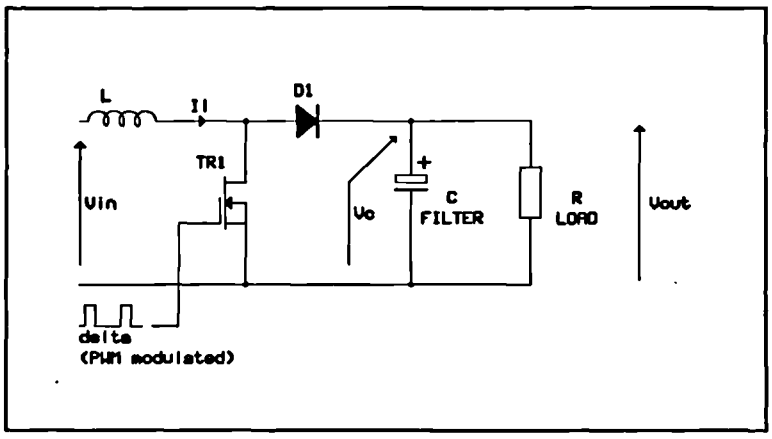

Figure 35 Boost converter with state-variables shown.

It is important to note at this point that the sole purpose of performing the state-space modelling and analysis of the boost converter was to facilitate the development of a stable and working converter system which could then be used to determine how the maximum power source of the photovoltaic arrays affected the operation of the converter. In addition to the usual assumptions made when carrying out averaged state-space modelling [33] it was decided to neglect the series resistance of the source in the development of the model. This was for two main

$$\begin{bmatrix} \dot{i}_l \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-\Delta)}{L} \\ \frac{1-\Delta}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix} + \delta . \begin{bmatrix} 0 & \frac{1}{L} \\ -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} I_l \\ V_c \end{bmatrix}$$

$$v_0 = [0 \quad 1] \begin{bmatrix} i_l \\ v_c \end{bmatrix} \tag{46}$$

$$0 = \begin{bmatrix} 0 & \frac{-(1-\Delta)}{L} \\ \frac{(1-\Delta)}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} I_l \\ V_c \end{bmatrix} + V_{in} . \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

reasons. Firstly, the equations for the effective cell series resistance would have to be derived from the double exponential equation **(1)** and would thus be very nonlinear. Such an expression if used in the small-signal modelling would result in a source impedance which is a non-linear function of not only the steady-state value of the state variables but additionally of irradiance and temperature. This would tend to add significant complexity to the model. Secondly, as will be shown later, the converter will only operate in a conventional manner when the converter input is on the portion of the array characteristic between open-circuit and maximum power, when the array appears as a voltage source. It is possible to approximate the value of the source resistance in this region. **Figure 36** shows a portion of the I/V curve of the array to be used in the simulation studies (see section 3.8.1 for more detail) in this region. Although the shape of the curve is nonlinear, the curve is quite gentle in this region and from the graph it is possible to determine that the resistance is

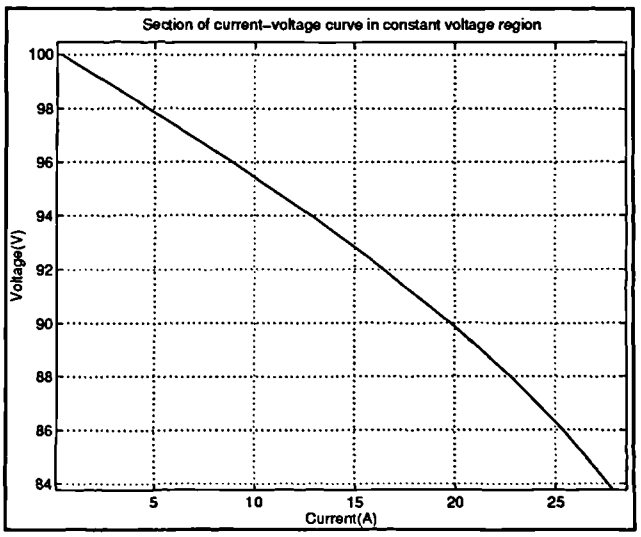

Figure 36 Portion of I/V curve in the region V_{oc}-V_{mpp}

approximately 0.5Ω. Although this is much greater than would be expected from a true 'stiff' source, it is still quite small. Furthermore, the effect of a series resistance in the supply was considered - this will be to increase the overall damping of the system. This is advantageous as if the converter control parameters can be determined so as to arrive at a stable system without the resistance, its presence will serve to increase any available phase margins in the system and reduce the likelihood of instability occurring. The relatively small effective value of the series resistance should not result in excessive slugging of the transient response.

Returning to equation **(46)**, the first equation in the set provides the state-variable information for the small-signal parameters of the system. The second of the two gives the output-to state variable relation, and it can be seen from the schematic alone that this is simply the capacitor voltage and is one of the state variables. The last of the set of three equations gives the d.c. characteristics. Small-signal (a.c.) parameters are denoted by lower-case values while corresponding d.c values are denoted by upper case. δ and Δ are the small signal and d.c values of the duty cycle of the switch, forming the control input to the converter. From these equations any small-signal transfer function for the converter may be derived by the use of Laplace transforms.

3.5.1 Conventional control algorithms.

In widespread use for the control of hard-switching PWM converter systems are two control strategies, that of voltage mode control, and the slightly more diverse field of current mode control. In voltage mode control, a single loop and compensating network is built around sampling the output voltage, comparing it to a reference and using this error

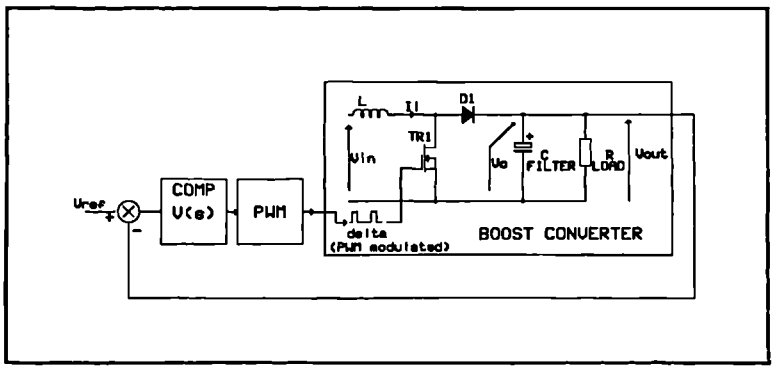

Figure 37 Voltage-mode control arrangement.

signal to drive the PWM modulator through the compensating network (**Figure 37**). Current mode control is marginally more complex in that a second loop is employed, buried within the first to sample (usually) inductor current, compare that with the error signal from the voltage loop, and use this to drive the PWM modulator through another compensator (**Figure 38**).

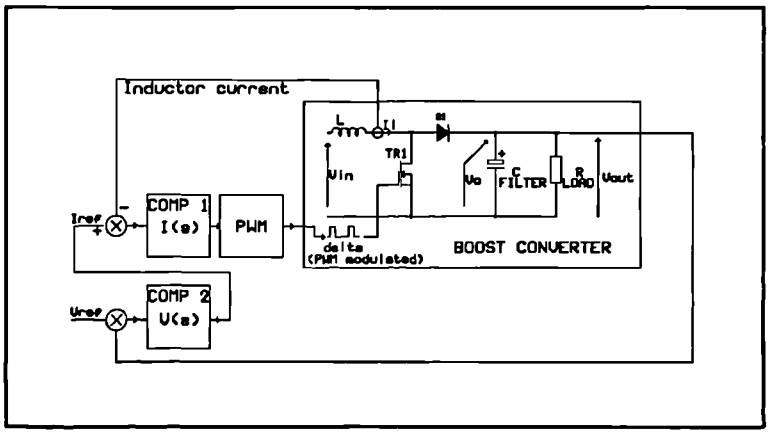

Figure 38 Conventional current mode control arrangement.

In voltage mode, the state-space relations can be rearranged to give a small signal transfer function for the boost converter relating the output voltage v_o (or v_c) to the value of the duty cycle of the control input (**47**).

$$\frac{v_o}{\delta} = \frac{V_o}{(1-\Delta)} \cdot \frac{\left(1 - s\left(\frac{L}{(1-\Delta)^2 R}\right)\right)}{s^2\left(\frac{LC}{(1-\Delta)^2}\right) + s\left(\frac{L}{(1-\Delta)^2 R}\right) + 1} \qquad (47)$$

From the schematic of **Figure 35**, the presence of the LC network indicates that a complex pole would be present in the function. What is not immediately obvious is the reason for the presence of the first-order right hand plane zero, although if the operation of the converter is investigated at the instant of commencement of switching operation the reason may be seen. The output voltage will drop in value momentarily as the switch closes before starting to rise as the switch opens. Compensating this nonminimum-phase system to prevent stability problems can only be effected by limiting the bandwidth before the extra lag induced by the RHP zero reduces the phase margin excessively. This is an inherent characteristic of continuous-mode flybacks.

Voltage mode could be used in this application, but investigation of the characteristics and design of possible current mode control strategies brought to light some interesting possibilities.

Current mode systems may be paralleled with ease, whereas voltage mode systems may not be. If the voltage loop is opened, the outputs of the converters paralleled and a single voltage loop closed over the complete system, the individual converters will current-share. In a photovoltaic application, this is an extremely useful property as while the system is primarily being designed as a single stand-alone unit for domestic/remote zero-maintenance application, if a number of discrete units could be paralleled there would be a possibility for use in large-scale applications as well, each converter with its own array.

Conventional current mode control algorithms control the inductor current. With this arrangement, the complex pole (with its possible large phase lag) is removed from the inductor current to output voltage transfer characteristic, rendering it first-order (although the complex pole is still present in the δ-to inductor current response). It is possible to design the current loop to be much faster than if the RHP zero was present: the first order LHP zero together with the complex pole ensure that the phase shift as $s \to \infty$ can not be more than 90°, although it may be more at intermediate frequencies within the band depending upon the relative locations of the complex pole and the LHP zero. The RHP zero is, however, still present in the voltage loop. The equation set for the converter dynamics under average inductor current mode control is given in (48).

$$\frac{i_l}{\delta} = \frac{2V_o}{(1-\Delta)^2 R} \cdot \left[\frac{s\left(\frac{CR}{2}\right)+1}{s^2\left(\frac{LC}{(1-\Delta)^2}\right)+s\left(\frac{L}{(1-\Delta)^2 R}\right)+1} \right]$$

$$\frac{v_o}{i_l} = \frac{(1-\Delta)R}{2} \cdot \left[\frac{1-s\left(\frac{L}{(1-\Delta)^2 R}\right)}{1+s\left(\frac{CR}{2}\right)} \right] \qquad (48)$$

The faster inner loop of current mode control systems ensures that any changes in input voltage are corrected for within the inner loop, without having to pass through the relatively slow voltage loop filter. The result is that changes in the input voltage are rejected before they manifest as a transient in the time-response of the output voltage at the instant of change. With photovoltaic arrays being subject to change in terminal voltage this is quite a useful property for a PV converter system to possess. Such changes occur very slowly in comparison to the time constants in the converter chain, and therefore the dynamics of this correction offered by current mode operation need not be particularly fast, providing the steady state error is small.

The price and complexity of the extra loop is small in comparison to some of the advantages proffered by current mode control, especially if the control is implemented digitally where apart from the provision of an extra ADC channel and signal conditioning the overhead over voltage mode is only extra computational requirements.

3.5.2 Diode current mode control.

During the investigation into suitable control algorithms for use in the system, it was noticed that a simple modification to the conventional current mode system gave some quite interesting benefits over the conventional approach. The technique is not new, but its applications seem to be quite few and far between, and a perusal of literature to hand showed only one instance of it being used [36], and there were no examples of it being implemented digitally. To this end it was decided to investigate it further.

The modification hinges upon the fact that average *diode* current is sampled, not the average or peak inductor current as is used in conventional forms of current mode control [33], [37]. This transforms the portion of the converter chain prior to the filter capacitor into a current source. This will enhance paralleling of converters without the dynamics of individual sections being altered - it would be possible to have several converters feeding a single filter capacitor; although this would require separate inductors, in a very high power arrangement it could reduce the currents in each switch to a much lower level and thus facilitate use of cheaper components.

In addition, the very fact of turning the converter (less filter capacitor) into a current source has some interesting effects upon the system dynamics. The RHP zero is still present, indeed it is intrinsic in the dynamics of the continuous mode flyback and cannot be removed, but this arrangement buries it in the current loop. The compensator for the current loop will be marginally slower than that used in the current loop of a conventional average inductor current method, but in comparison to voltage mode both the complex pole and the RHP zero have been removed from the inductor current to output voltage charcteristic, reducing it to a single first-order pole. Initially this could be seen as a retrograde step, as a lot of the advantages of current mode control rely on the high gain and wide bandwidth of the current loop. The problem with continuous mode flybacks is the dependence of the position of the RHP zero upon L, as may be seen from equation **(51)**. If L is made large, to prevent light loads from causing the inductor current to go discontinuous, the RHP zero frequency is very low and the bandwidth of the compensator must be restricted to prevent instability. The result is that if the system was to go discontinuous, the overall open loop gain of the system would be reduced still further by the drop in gain of the converter as the mode boundary is traversed, thus worsening its performance.

If the inductor is reduced in size the result is to increase the RHP zero frequency. The system will also go discontinuous at a heavier load and therefore taking this action in a conventional current mode system will prevent the effective operation into light loads. With diode current control, if L is reduced the compensator can be given a higher bandwidth and more gain at the frequencies of interest due to the correspondingly higher frequency of the RHP zero, sufficient indeed to allow the mode boundary to be traversed for light loads without detriment to the system bandwidth. The net result is that in the *overall system*, the effect of the RHP zero is reduced and the system speeded up. In a conventional current mode system, the RHP zero is present in the voltage loop, and causes an overall reduction of bandwidth. Note that there is no conflict with the continuous current requirement of the maximum power tracking algorithm, as the size of the loads referred to here that would make the system go discontinous would be well below the MPP of the array - this is at a converter operating point well within the constant voltage section of its intended characteristic - not even near a maximum power load.

To show the dynamics of the system, two transfer functions relating I_d to δ and v_o to i_d are required. These can be derived from the state-space relationships of **(46)**, but an additional equation is required relating the diode current i_d to the state variables. Since i_d is identical to the inductor current i_l for the period $(1-\Delta)/T$, and zero for the rest of the cycle, a linearized averaged equation can be written:

$$I_d+i_d = I_l(1-\Delta)+i_l(1-\Delta)-I_l\delta \qquad \textbf{(49)}$$

Separating out the steady-state terms from the small-signal terms:

$$\begin{aligned} &\textit{For steady state:} \quad I_d = I_l(1-\Delta) \\ &\textit{For small signal:} \quad i_d = i_l(1-\Delta)-I_l\delta \end{aligned} \qquad \textbf{(50)}$$

It is now possible to Laplace-transform the set of equations formed by **(46)** and **(50)** and solve the resulting linear equation set for the desired transfer functions (eliminating the inductor current i_l) The resulting equations for i_d/δ and v_o/i_d are given below in **(51)**.

$$\begin{aligned} \frac{i_d}{\delta} &= \frac{(1+sRC)\left(1-s\left(\dfrac{L}{(1-\Delta)^2R}\right)\right)}{s^2\left(\dfrac{LC}{(1-\Delta)^2}\right)+s\left(\dfrac{L}{(1-\Delta^2)R}\right)+1} \\ \frac{v_o}{i_d} &= \frac{R}{1+sCR} \end{aligned} \qquad \textbf{(51)}$$

As can be seen, both the complex pole and the RHP zero are now buried in the current loop. A hidden advantage of this system, discovered experimentally, was that the ease of stabilization is enhanced. The system can be compensated by two proportional+integral (PI) compensators, placed in each loop, to stabilize the system and optimize the transient response. If the system is optimized for maximum load, it remains stable for all loads across the design range with little degradation in transient response. The single-pole current-to-voltage transfer function makes stabilization of the voltage loop very simple, providing the compensator coefficients in the inner current loop are chosen carefully.

Finally, for a digital implementation the sampling of diode current requires no change to the hardware used in a conventional control arrangement - the inductor current is the same as the diode current during the period when the switch is off, and therefore the only change required (other than to the compensator arrangement) is to modify the manner in which the average current is calculated. **Figure 39**, also equations **(52)** and **(53)** show the difference. Note that the calculation for the diode current is simpler than that for the average inductor current, removing one multiplication and one addition, thus slightly easing the load on the computational core.

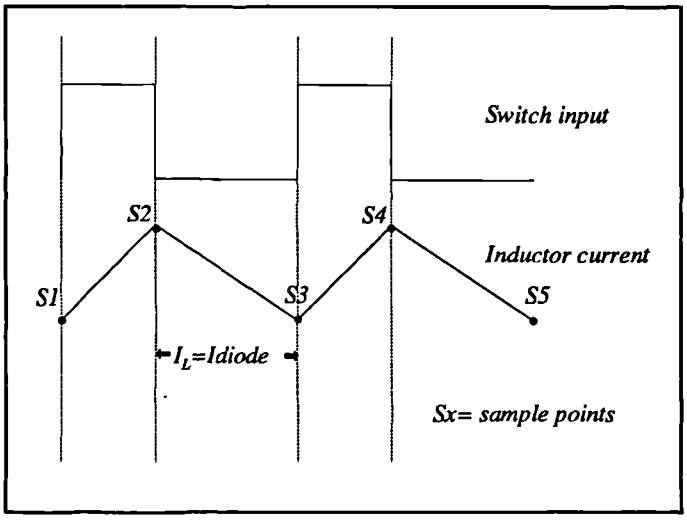

Figure 39 Inductor current waveforms showing samples

Average inductor current:-

$$I_{avg} = \frac{1}{2}[S1\Delta + S2 + S3(1-\Delta)] \tag{52}$$

Average diode current:-

$$I_{avg} = (1-\Delta)\left(S3 + \frac{S2-S3}{2}\right) \tag{53}$$

3.5.3 Averaging delay.

In a discrete implementation of either type of current mode control, as opposed to the continuous system, there is an additional delay introduced by the averaging calculation used for the inductor current and output voltage. The reason for this is the finite time required by the

processor core to complete the calculations of the new value of Δ from the averaged system parameters. A complete switching cycle is required to obtain the information required to calculate the average value, further time is required then to actually perform the calculation. The earliest time the duty cycle can be updated, therefore, is one further switching cycle later. The net result is a two-cycle delay in the calculation of the average values. The reason for this is shown graphically in **Figure 40**, and this will modify the model of the control system to that shown in **Figure 41**.

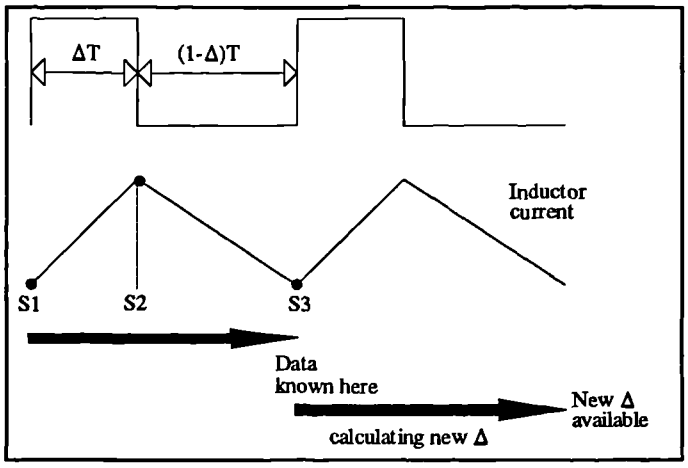

Figure 40 Averaging delay in sampled current sensing.

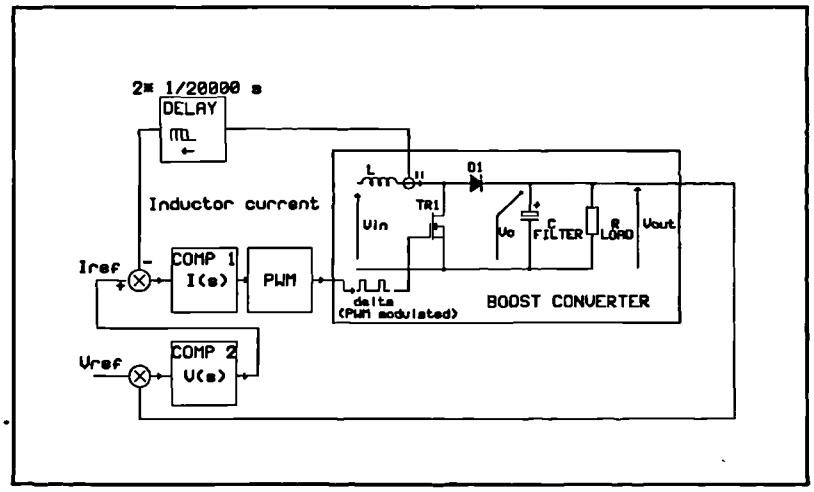

Figure 41 PI control arrangement with delay.

This delay will clearly affect the dynamic response of the system. Considering the current loop alone, the delay will cause a progressive increase in loop phase lag as frequency is increased, while leaving the magnitude response unaffected. The question is will the lag caused by the delay be significant at the crossover point to seriously affect the achievable phase margin of an

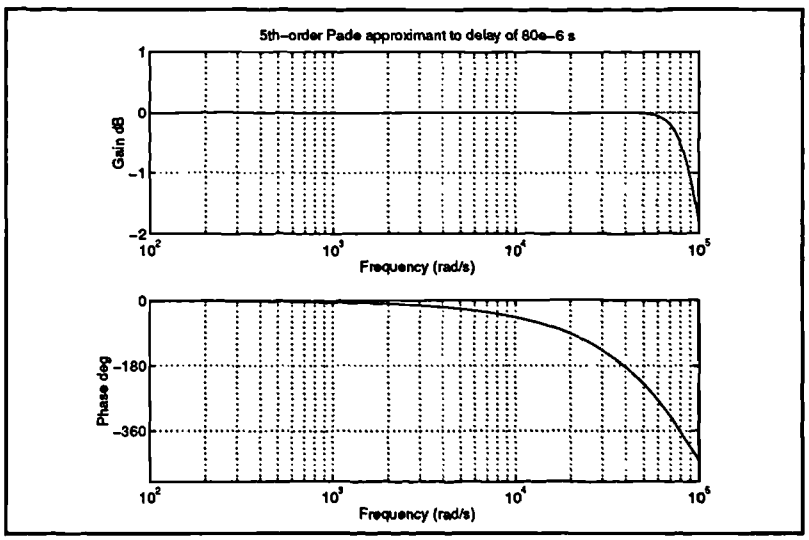

Figure 42 Bode plot of 5th-order Pade approximant

undelayed system? **Figure 42** shows the Bode plot of a fifth-order Pade transfer-function approximation to the delay function e^{-sT}. The aberrations in the magnitude response are due to the approximation - the true function e^{-sT} will indeed leave the magnitude response unaffected ($e^{-sT}=e^{-j\omega T}=\cos \omega T+j \sin \omega T$, which has a magnitude of unity).

The addition of this delay to the loop will considerably dent the phase margin that is achievable in a system without it. For example, without the delay it is possible to compensate the current loop in this converter to achieve a phase margin of 47.79 degrees at an angular frequency ω=25840 ($f=25840/2\pi=4.1$kHz). The actual delay time caused by averaging at a switching frequency of 20kHz is 2/20000=100μs, at a frequency of 4.1kHz, the phase lag introduced by the delay will be $360 \times 80 \times 10^{-6} \times 4100=118°$. This will clearly result in instability if the compensator coefficients calculated for the undelayed case are used since the phase margin will go negative to a value of 47.79-118=-70.21°. It is therefore necessary to incorporate this delay into the calculation of controller coefficients.

It must be appreciated that the presence of this delay will slow the current loop down significantly, and that little can be done about this short of raising the switching frequency to reduce the delay, but this would also reduce the time available to the processor core for the calculation of the new value of Δ. A reasonable response was still achieved at 20kHz, however, and given the difficulties of moving to a faster DSP processor core it was decided to continue using a 20kHz switching frequency.

3.6 Converter parameter calculation for diode-current mode control.

In order to make the best use of diode current mode control, it was decided to calculate the values of L and C for the converter bearing in mind the fact that reducing the value of L will tend to speed up the system. It was at this point that some preliminary calculations suggeseted that the switching frequency should be set at 20kHz in order to maximize available computation time. The switching frequency does not appear in the small signal transfer functions and this choice will not affect the operation of the controllers in any other way.

The calculations were made as follows. The nominal (steady-state) switch duty cycle, Δ, is given simply by substituting the values for V_{out} and V_{in} in the equation for the steady state transfer characteristic for a boost converter:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-\Delta} \therefore \Delta = \frac{V_{out}-V_{in}}{V_{out}}$$
$$\Delta = \frac{400-100}{400} = \underline{0.75} \tag{54}$$

The inductor ripple current was set at 2A, this is 2A ripple on a 1kW (nominal) array with a V_{mpp} at approximately 100V, ie 2A ripple on 10A. Maximum ripple occurs at Δ=0.5, the new value of inductance was calculated as:

$$L = \frac{Edt}{di} = \frac{100 \times 50 \times 10^{-6} \times 0.5}{2} = 1.25mH \tag{55}$$

while the new value of capacitor came from It=CΔV where ΔV is set at 50mV and I is the value of load current of 1kW/400V=2.5A:

$$\therefore C = \frac{It}{V} = \frac{2.5 \times 0.5 \times 50 \times 10^{-6}}{0.05} = 1250 \times 10^{-6} F \tag{56}$$

A close standard value is 1000μF, this can be used with a slight increase in ripple voltage and should be of a low e.s.r. type. The full set of converter parameters have been laid out in **Table 3** for ease of reference.

Table 3 Table showing list of nominal converter parameters used during the development of the controller.

Vin (nominal)	100V	Δ:	0.75
Vout	400V	(1-Δ):	0.25
L:	1.2mH	C:	1000μF
I_{mpp} (1000W array):	10A nominal at MPP	T_s:	50μs
R:	100Ω		

Given these values of C and L, it is possible now to place the numbers in equation **(51)** and use this to aid the determination of suitable coefficients for the compensators of **Figure 38.**

3.7 Determination of suitable controller and its coefficients.

Simple PI controllers were chosen for both the inner current loop and the outer voltage loop as it was felt that this type of controller is capable of stabilizing the system without too much complexity, and gives zero d.c. errors due to the integral term.

To develop the controller coefficients, the mathematical modelling and simulation package MATLAB was used. Although Saber has the capability to perform just the same type of simulations, MATLAB is considerably faster for this type of work where a number of transient response simulations may have to be run before suitable values are arrived at.

The method used was to optimize the system from the inside-out - stabilize and optimize the current loop first, followed by the voltage loop. The load value resistance chosen was for maximum load, stability of the closed loop system is worse the higher the load resistance. The transient response was determined using a step change in the reference from zero to nominal. The complete system was entered as a model in SIMULINK (**Figure 43**), and this was used in

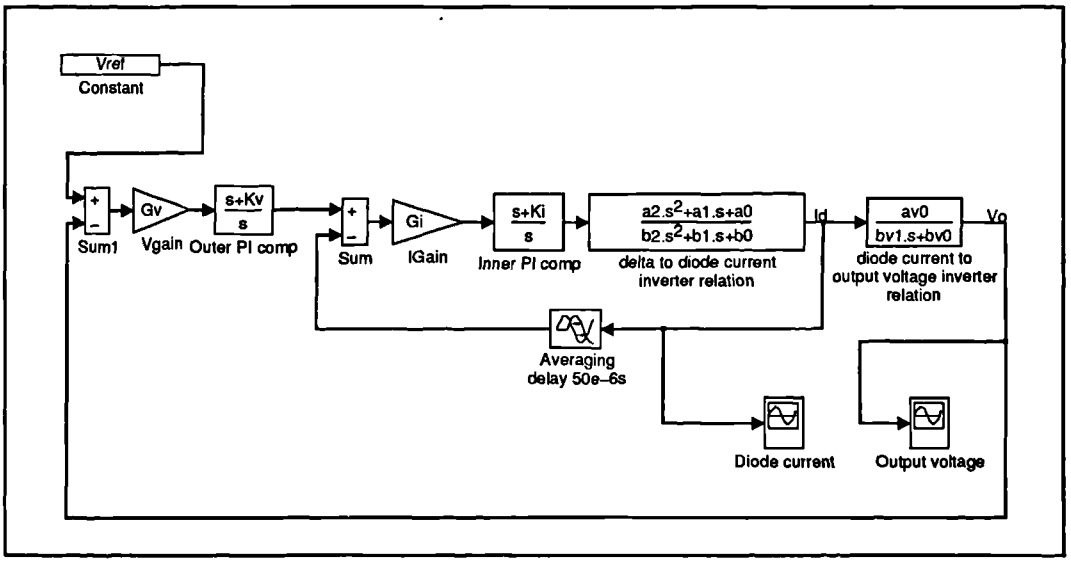

Figure 43 SIMULINK model of system

$$
\begin{aligned}
&a0=1\ ,\quad a1=RC+\frac{L}{(1-\Delta)^2R}\ ,\quad a2=\frac{LC}{(1-\Delta)^2}\\
&b0=1\ ,\quad b1=\frac{L}{(1-\Delta)^2}R\ ,\quad b1=\frac{LC}{(1-\Delta)^2}\\
&av0=R\ ,\quad bv1=CR\ ,\quad bv2=1
\end{aligned}
\tag{57}
$$

conjunction with scripts which calculated the parameters a0,a1,a2,b0,b1,b2,av0,bv0,bv1 using (57) to obtain the transient response. Optimization of the loops was performed using Bode plots and gain/phase margin techniques. A MATLAB script was written allowing entry of values for the PI controller coefficients, after which the Bode plots were plotted and the phase margin calculated. The values of the PI controller coefficients could be altered and the resulting Bode plot superimposed over the previous one, allowing the changes to be seen. The coefficient selection is an iterative one where both the Bode plot for the system together with the transient response were plotted during each phase of the iteration. When the desired response was obtained the closed-loop response was plotted and the process repeated for the outer loop. The averaging delay was taken into account by making use of a 5th-order Pade approximation to the delay. However, owing to an apparent inability on the part of MATLAB to correctly plot a transient response of a system containing a Pade approximant (the generated plot is nonsensical), the transient responses were generated from the SIMULINK model. This appeared to contain a better intrinsic function for the time delay block. It calculates the time response directly in the time domain using a numerical integration method.

Using the MATLAB scripts, the controller coefficients were optimized for the system variables detailed in **Table 3** and the Bode and transient plots are shown here for the optimized system. The controller coefficients determined for this system are given in **Table 4**.

Table 4 Controller characteristics: 400V system

Voltage loop filter characteristic:	Gv=1, Kv=50
Current loop filter characteristic:	Gi=0.03, Ki=150

3.7.1 System performance

The Bode plot of the current loop, without the compensator is given in **Figure 44**. The effect of the RHP zero can be clearly seen in that at about $2x10^4$ rads/s the phase begins increasingly lagging while the gain begins to flatten out. The Bode plot of the compensated open current loop, including the phase margin value, is shown in **Figure 45**. Proportional plus integral (PI) compensators are eminently suitable for this application owing to the near-zero steady-state error afforded by the integrator, and in a d.c. power supply this is ideal. The PI compensator also contains a zero; careful positioning of this zero, together with the gain of the filter, is made to ensure the widest stable bandwidth possible.

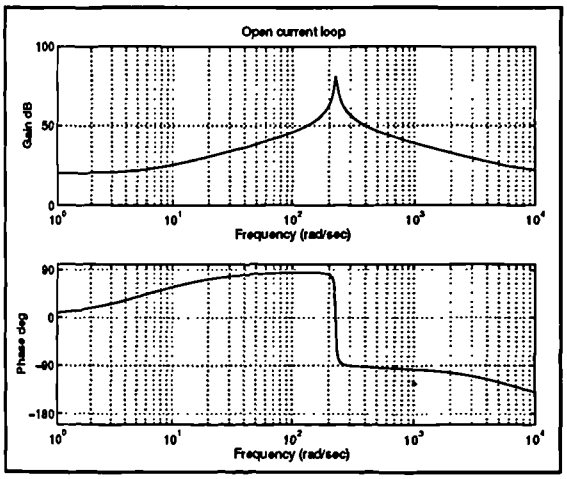

Figure 44 Bode plot: Open current loop without compensator.

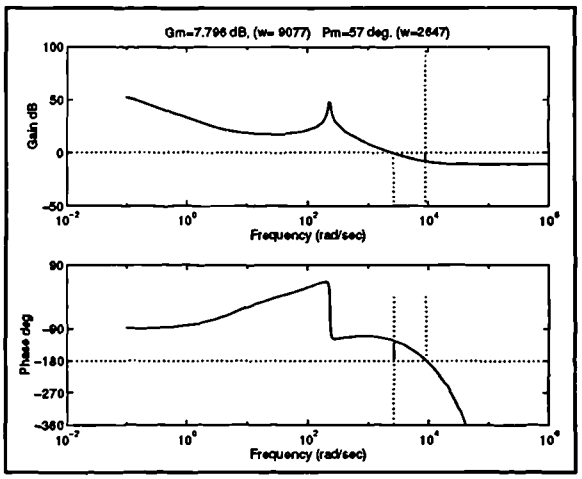

Figure 45 Gain and phase margins: compensated current loop.

The Bode plot of the compensated voltage loop system including the gain and phase margin figures forms **Figure 47**. Finally, the closed loop response, and transient response from SIMULINK is given in **Figure 48** and **Figure 49**.

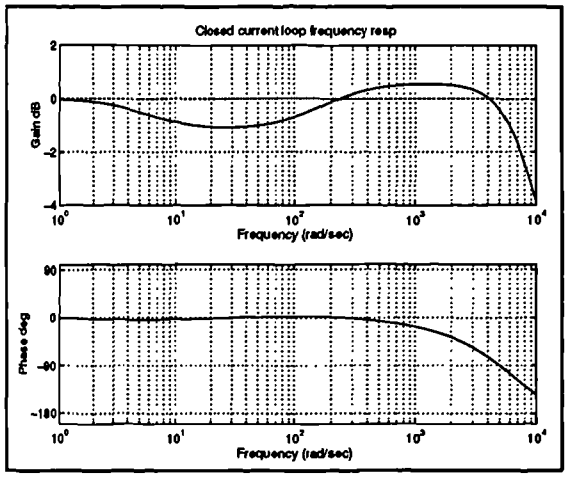

Figure 46 Bode plot: closed current loop.

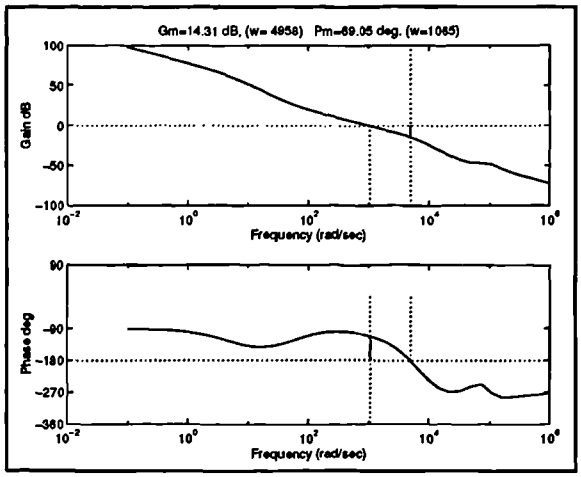

Figure 47 Bode plot: compensated voltage loop.

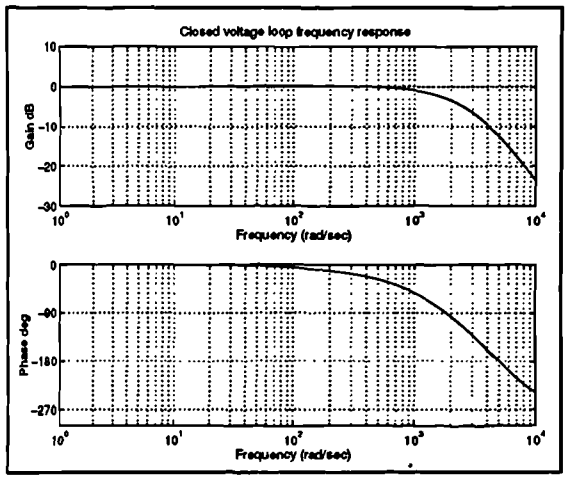

Figure 48 Bode plot: closed voltage loop.

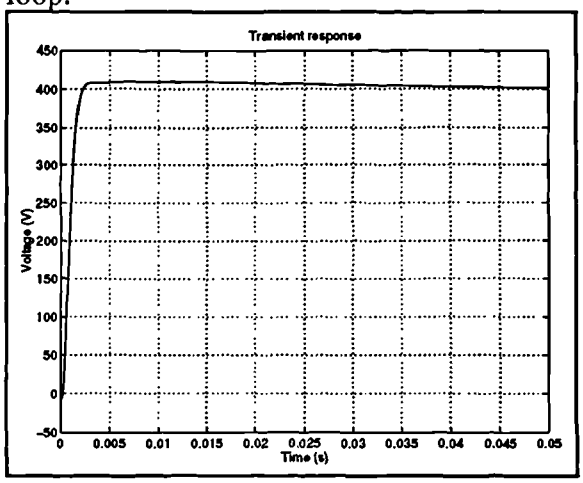

Figure 49 Transient response of SIMULINK system with final controller constants.

3.7.2 Characteristics of compensated system: small-signal

The current loop and voltage loop have been compensated using PI compensators under nominal conditions, i.e. maximum load for fixed output voltage. This will in turn mean that the system has been stabilized for a fixed input voltage. In a practical photovoltaic system of this nature, however, the load will not necessarily be constant. This is no unusual characteristic of d.c. power supplies. Due also to the nature of the I/V characteristic, the array terminal voltage will not be constant with load (although this variation is relatively small below and out of the neighbourhood of the maximum power point. Most converter designs assume a constant input voltage with a small variation, or operation over a range of possible fixed input voltages. It forms

an interesting investigation to observe the dynamics of the system with these changes in mind; i.e. change of input voltage with load.

Considering the current loop with reference to equation **(51)**, it can be seen that there is a considerable dependence of equation parameters on $(1-\Delta)^2$, and R, the load resistance. The variation of R would be expected to result in the variation of the damping of the second-order system created by the LCR network. However, the more significant is the nonlinear variation of the transfer characteristic with Δ. For a fixed output voltage, if the input voltage changes so will Δ and so will the dynamics of the system. The question is will such changes destabilize the system.

A MATLAB script was written to solve the system given in **Figure 43** for varying Δ and R and to plot the transient response with respect to the reference. The plots are given in **Figure 50** and **Figure 51**. Note that the negative output voltages plotted are a function of the small signal transfer functions if the system in **Figure 43** and do not exist in the real system. The system is stable for all values of R and Δ simulated.

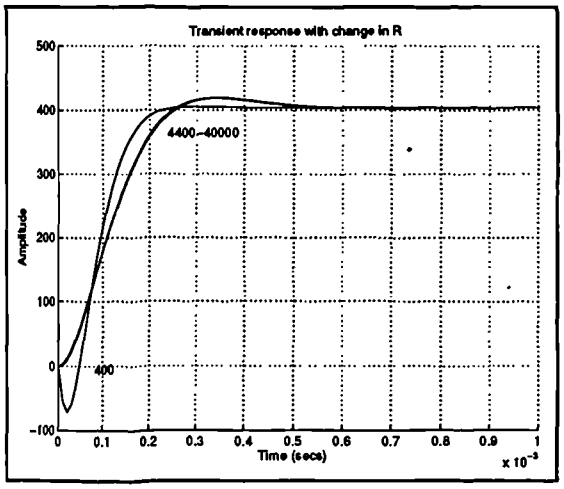

Figure 50 Transient response family showing variation with load.

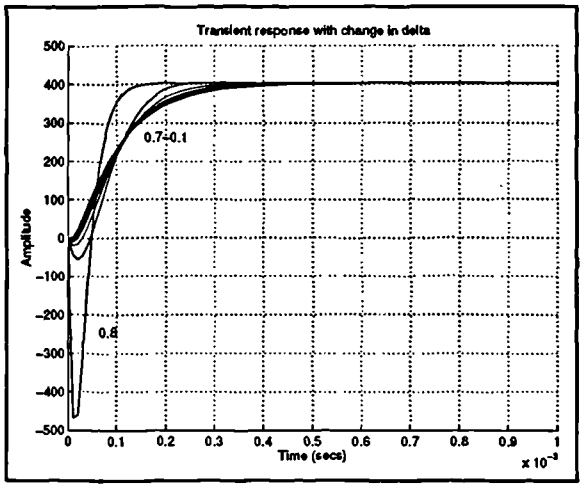

Figure 51 Transient response family showing variation with Δ.

3.7.3 Discrete-conversion of s-domain compensator arrangements

The final step in the design process was to convert the continuous-frequency domain compensator equations to those that could be used in a sampled-data environment. This was a

straightforward undertaking. A PWM based switching system is naturally a sampled-data system as it can only update its outputs (switch on-time) at intervals of the base switching frequency. The average values of the control variables (inductor current, array and output voltages) are known at the end of each cycle after a simple averaging calculation. Updated values of the outputs must therefore be calculated. The switching frequency is high in relation to the crossover frequency and all other time-constants in the system. The controller is to be implemented with the aid a 16x16 bit multiplier with a 32 bit product (in the DSP) using scaled coefficients. This implementation allow the simple bilinear transform to be used to effect the conversion as under these conditions the errors involved in its use should be fairly small. The gains are retained throughout the transformation so the frequency-dependent portion of the compensator is all that must be translated, the results are given in **(59)** and **(58)**. Multiplying out the z-domain transfer functions written in descending negative powers of z gives the difference equations, the implementation of which (in Saber) is very straightforward.

$$\frac{i}{v}=\frac{s+50}{s} \equiv \frac{1.001-0.999z^{-1}}{1-z^{-1}} \tag{59}$$

$$\frac{\delta}{i} = \frac{s+150}{s} \equiv \frac{1.003-0.997z^{-1}}{1-z^{-1}} \tag{58}$$

giving rise to the difference equations:

$$i_{[k]} = 1.001v_{[k]}-0.999v_{[k-1]}+i_{[k-1]} \tag{60}$$

$$\delta_{[k]} = 1.003i_{[k]}-0.997i_{[k-1]}+\delta_{[k-1]} \tag{61}$$

3.8 Initial simulation implementation of current-mode system.

To enable a simulation model for the front end to be constructed, a PV array must first be defined and implemented in simulation.

3.8.1 Simulated PV array used in initial front end simulation.

These tests were intended to determine whether or not a PI compensated system would allow a regulated d.c voltage to be supplied to loads drawing less than the maximum power across the design range of the converter. A load can not draw more power than the maximum that the array can provide, and so it is expected that the PI compensated controller will need to be modified for the converter to operate in the neighbourhood of the maximum power point as at this point the regulated d.c. voltage can not always be sustained into loads drawing array maximum power. Therefore, for these tests upon a system controlled by conventional PI compensators, a simulated array was implemented with a maximum power point well above the nominal inverter power of 1kW.

Figure 52 shows the IV characteristic of the arrays used in this simulation: a 200*200 matrix of cells at 37°C and 10000arb irradiance. The maximum power point is at 2.5kW, more than twice the nominal converter design power. The deviations from a conventional voltage source are obvious. For values of array current above 30A, the array voltage falls off very rapidly with increasing current, up to the limit when the array current is at its short-circuit value I_{sc}. In this region dV/dI is very high, and the array appears close to a current source (constant-current

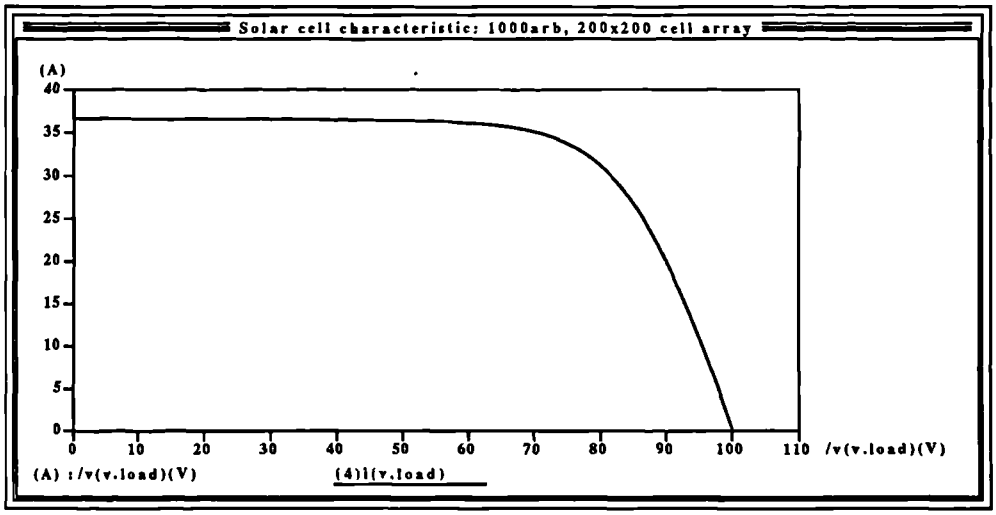

Figure 52 Array curve for simulation runs

region). As the current demand decreases below 30A, however, the variation in array voltage is small in comparison with array current, with the open-circuit voltage V_{oc} being 100V. In this region dV/dI is small, and the array appears close to a voltage source (constant voltage region). It now remains to relate this to the converter characteristics.

3.8.2 Simulation of front-end.

A MAST template was written containing the controller elements as well as the PWM subsystem and is given in Appendix B section A7. A symbol was created and the schematic for the system can be found in **Figure 53**. Three types of loads are represented in **Figure 53**, a resistive load, a piecewise-linear load and a sinusoidally varying load. The minimum load is set by the value of the load resistance and the current through this may be changed by modifying the values of the variable voltage sources. With this implementation, a number of time domain simulations were run. The first of these was from zero to 200ms and this may be found in **Figure 54** (This was run in two stages to avoid generation of large files and this is the reason for the change in line style at 100ms). The second of these simulations involved changing the load value in a system running at steady state. The output voltage from this simulation may be found in **Figure 55** where the load changes occurred as listed below:

250m: 200R-1000R

300m: 1000R-100R

350m: 100R-80R

400m: 80R-1000R

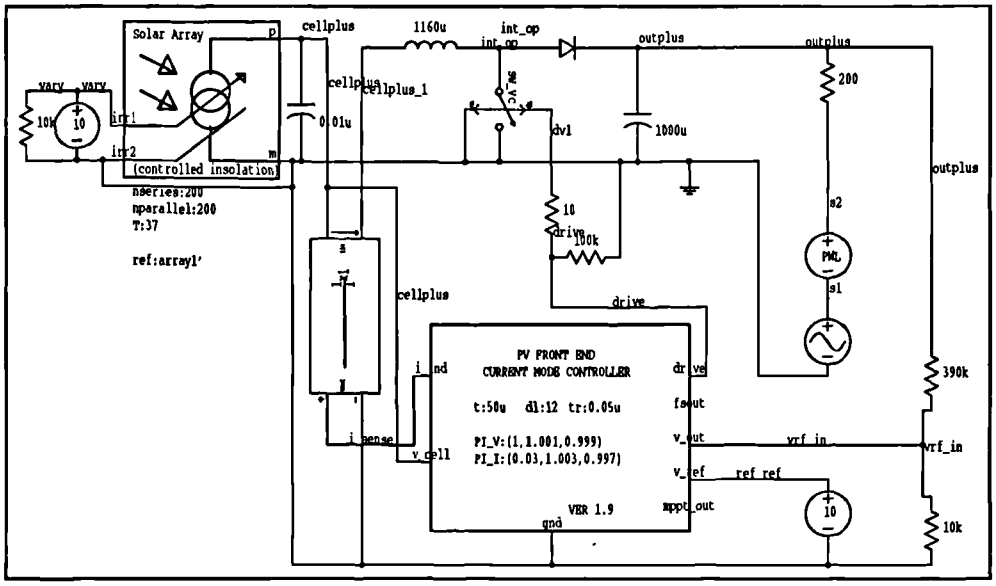

Figure 53 DesignStar schematic of the first implementation of the current-mode controller.

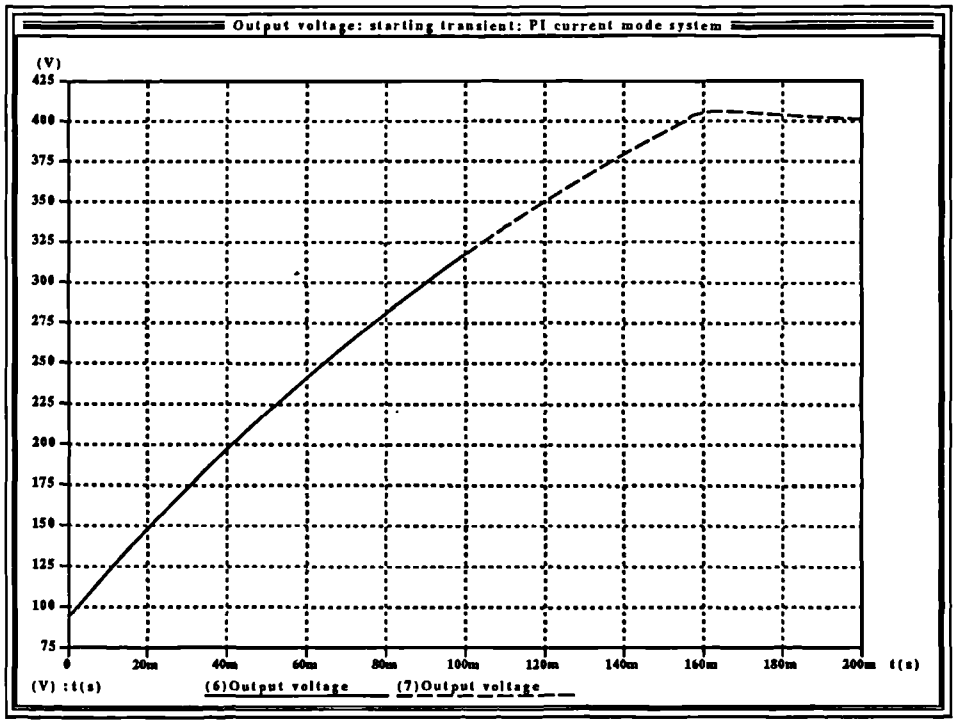

Figure 54 Output voltage of converter starting up into 200R load.

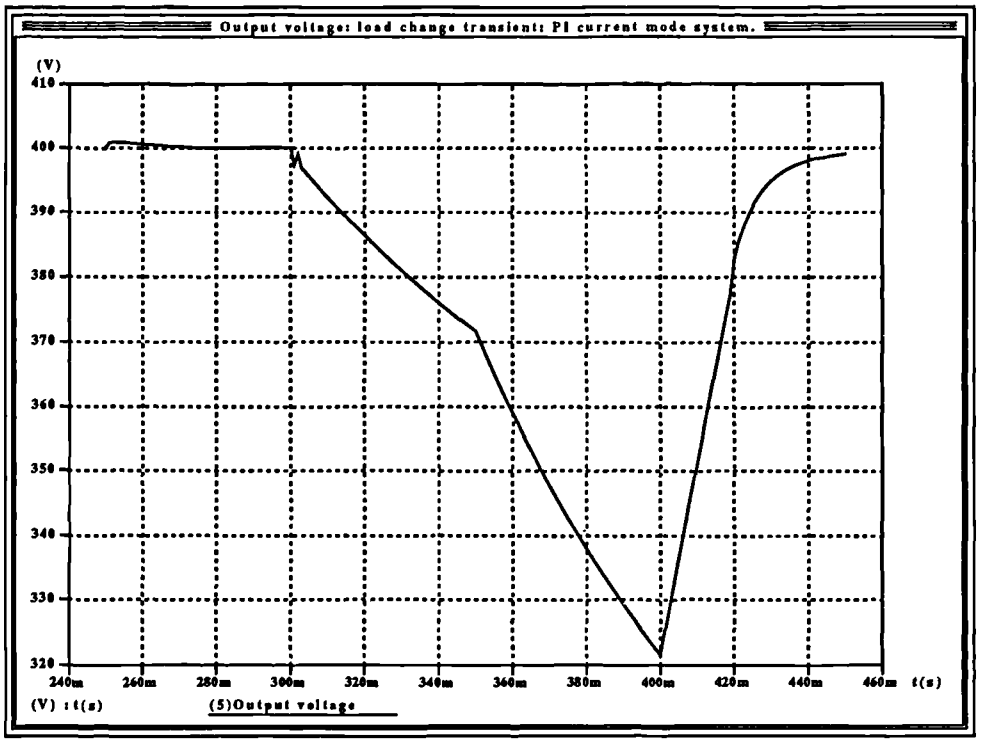

Figure 55 Output voltage of converter in response to given load changes.

The third of these simulations was an extended simulation of a load change from 200R to 100R, and the result of this can be seen in **Figure 56**. These responses are not what would be expected from a conventional current mode controller with PI compensators and it shows up some interesting characteristics of the photovoltaic power converter system that are not present with the conventional voltage-fed converters.

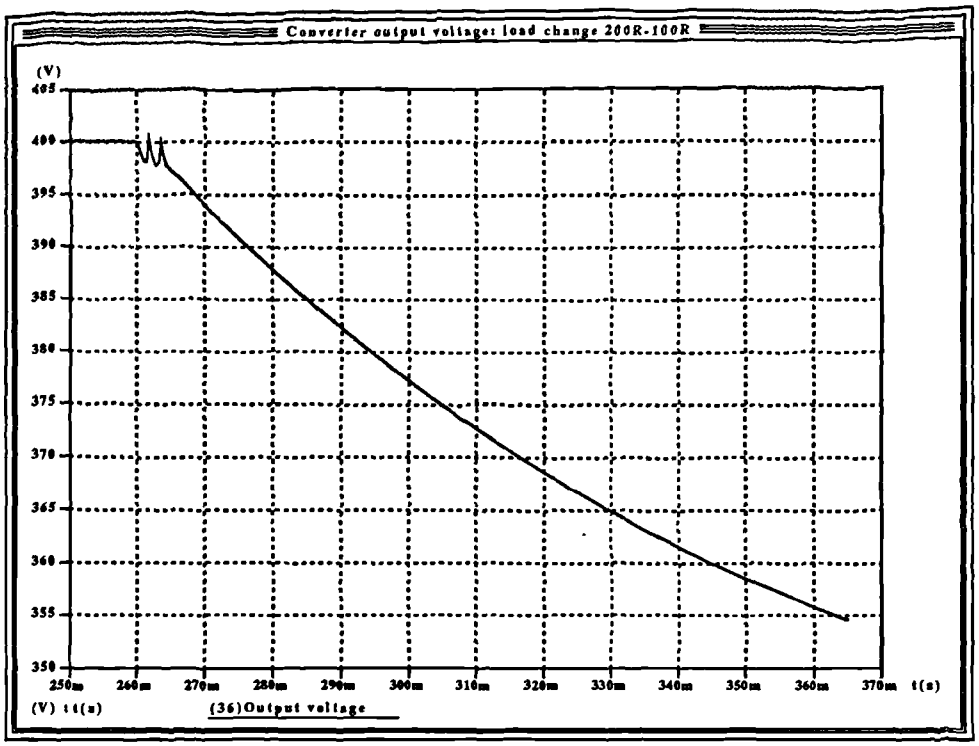

Figure 56 Extended simulation after load change 200R-100R.

The first of these curves, **Figure 54** does not exhibit the steeply curved rise as would be expected from a conventional system. For the bulk of the time taken to rise to rail voltage the slope is much less steep, and only slightly curved. This is consistent with the curve formed when a network consisting of a resistor and capacitor in parallel is fed from a constant current source. From the curve, it can be seen that normal operation of the PI network resumes just before 160ms where the characteristic gentle peak and rapid settling back to 400V occurs.

The second of these curves, that of the changing loads shown in **Figure 55**, shows some more unusual effects. The first transition, to 1000R at 250m shows no aberration from the expected response of a PI compensated current mode controller - the transient in V_{out} is very small and has the expected shape. The final transition, back to a 1000R load shows recovery of the system. The major deviation from the expected response occurs in the transitions to the heavier load values: here the shape of the response is once again consistent with a constant current feed to an RC parallel network. Note that the system will recover if the load is shed.

Finally, the response of **Figure 56** shows the effect of a change to a lower value of load in more detail. The load value was changed from 200R to 100R at 260ms, and after one and a half cycles of oscillation of unknown origin the output voltage falls off with a gentle curve. Owing to the extreme length of time that such a simulation takes to run (about 3-4hr for the 110ms of **Figure 56**) the simulation was not continued further in **Figure 56**, but extrapolation showed that curve would eventually flatten out at a lower value of just over 300V.

The shape of these responses was expected, and is a function of the characteristic of the solar arrays in combination with the voltage and current large signal transfer characteristics of the converter. To explain these effects in a subjective manner, it is expedient to consider the voltage transfer characteristic and the current transfer characteristic separately, although as it will be shown that a photovoltaic array as input, in this case, will introduce a measure of dependency of the two upon each other.

Consider the converter operating into a fixed value of load. If the maximum current available from the array is fixed at I_{sc}, as Δ increases from zero so the load voltage will rise as $V_{in}/(1-\Delta)$. As the load voltage rises so the load current (I_{load}) will increase, and so will the average current flowing in L ($I_{Lavg}=I_{load}/(1-\Delta)$). For low values of Δ, I_{load} and hence I_{Lavg} will be small, and the array will be operating on the constant voltage portion of the array characteristics. The converter will be operating normally in this region and V_{out} will increase with Δ.

Figure 57 shows the manner in which V_{out} varies with Δ in a boost converter fed from a 100V low-impedance voltage source (100V is the V_{oc} of the array used in the simulation studies). The manner in which V_{out} increases with Δ can clearly be seen from this curve, which is that of the steady-state voltage transfer characteristic of the converter, $V_{out}=V_{in}/(1-\Delta)$. V_{in} is invariant with I_{in} if the impedance of the source is negligible.

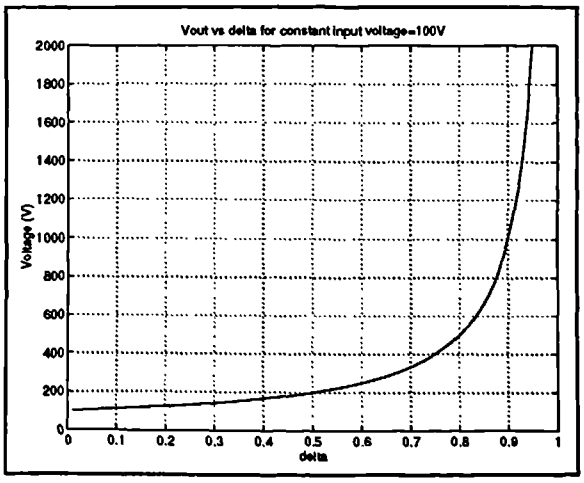

Figure 57 Variation of voltage-sourced converter output with Δ

Returning to the PV-array fed converter, as Δ increases, so does I_{Lavg}, and there will come a point $\Delta=\Delta_1$ where V_{in} will start to fall rapidly as the operating point moves on to the constant current portion of the array characteristic. Any further increase in Δ will result in V_{in} falling still further until it reaches zero, and V_{out} will fall similarly.

In this region, the value of interest is the average value of inductor current I_l ($=I_{in}$). As Δ passes Δ_1, variation in Δ causes little increase in I_l, which remains close to I_{sc}. The peak value of I_l at the instant of switch turnoff (I_{peak}) will increase slightly with Δ in this region, but it can never exceed I_{sc}. The converter now behaves as if it is being fed from a source with a high impedance: a current source.

Figure 58 shows the output voltage variation with Δ of a boost converter fed from a 36A constant-current source into a 100Ω load (36A is the I_{sc} of the 200x200 array used in these simulation studies). This was generated from the equation formed by solving for I_{out} and multiplying by the load resistance: $V_{out}=I_{in}(1-\Delta)R$. Note that in an ideal case if the load is zero the output voltage would be infinite. The points to note is that the slope of this curve is *negative*, as Δ increases, so V_{out} decreases. The curve is also linear. This is the direct opposite of the V_{out} versus Δ curve formed when the converter is fed from a voltage source. It is clear that the control requirements for a converter operating in this region will be different. The small-signal dynamics will alter accordingly; when being driven from a current source the inductor current will be the same as the source current, thus the dynamics of the inductor will be removed from the system. The chopping action of the switch will simply cause the average diode current to become a stepped-down version of the inductor current, and the converter dynamics will reduce to a single pole formed by the d.c. link filter capacitor and the load resistance.

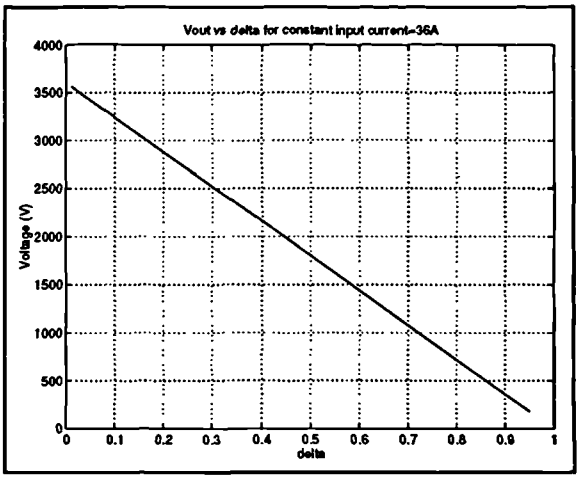

Figure 58 Variation of output voltage with Δ for a current-source fed converter.

Returning once again to the PV-fed converter, **Figure 59** shows the inductor current waveform taken during a portion of the simulation of the starting transient when the output voltage was on the sloped part of the curve -duty cycle here is 0.9, the upper limit. Now current is only flowing in the *diode* for the period of time (1-Δ)T. Therefore, for all values of $\Delta > \Delta_1$, the average diode current flowing will be approximately $I_{sc}(1-\Delta)$. In effect, the portion of the converter between the input and the output filter capacitor now behaves as a current source. Since the switching period T is constant, then it can be seen that the average diode (output) current will actually *fall* as Δ increases beyond Δ_1. As the load current falls, so will the load voltage.

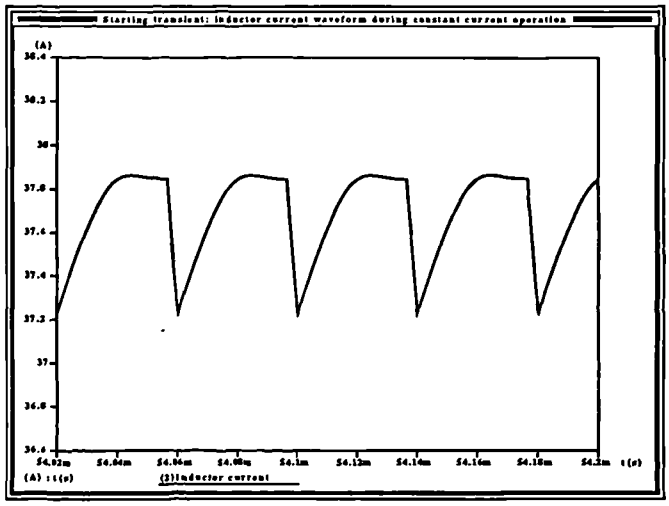

Figure 59 Inductor current waveshape during starting transient.

It remains to explain the effects observed in the complete system, with closed control loops, when the inverter is fed from a PV source. Consider the starting curve, which exhibits the slow climb to rail voltage instead of the steep curve normally associated with systems compensated by PI controllers. During startup the integrators in the controllers start to ramp up from zero, gathering speed as the error at this point is high. Unfortunately, in this system, the integrator in the current loop pushes Δ past Δ_1 into the constant current region of operation of the PV array. Further increase in Δ actually brings about a fall in load current, the integrators in the current loop compensators ramp up further still in an attempt to increase the load current, and hence voltage, until they reach their saturation limits (Δ=0.9 max, 0.1 min, in order to allow for ADC conversion time). At this point the system must wait with the integrators against their limits for the load voltage to rise, the voltage and current error to fall and bring Δ down below Δ_1, before normal operation can resume. This explains the shape of the starting curve (constant current), and the simulator showed Δ to be at the upper limit of 0.9 during the upward slope. A

point remains in that into heavier loads, the converter may never reach rail voltage, as $0.1I_{sc}R_{load}$ may be less than (in this case) 400V and the slope will flatten out at this voltage. The converter will need to shed its load to recover.

In the simulation results of **Figure 55** and **Figure 56**, of the load changes to heavier loads, the same effect is occurring. If the load suddenly increases, and demands more current, the integrators will sense the error and start to increase Δ in an attempt to supply the extra current to correct the error. However, if the voltage loop is fast then the current error will be large and it is likely that the integrators will cause Δ to rise past Δ_I and into the constant current region. As shown, in this region an increase in Δ will cause load current (and hence voltage) to fall, and that this in effect reverses the variation of V_o with Δ. The controller attempts to increase Δ still further to bring up the load current, but this increases the error still further. The integrators in the compensators 'wind up' until they reach their limits, at which point the output voltage has fallen to a very low value of $0.1xI_{sc}xR_{load}$ where 0.1 comes from $(1-\Delta)$ when Δ is at its upper limit of 0.9, and it will stay there. The only way in which this system can recover is by shedding its load, whereupon all energy is supplied to the filter capacitor which will start to charge up, slowly, and the output voltage will start to increase. The startup time from zero will also always be severely impaired due to this effect, but the effect is also prevalent when the load increases suddenly. Slowing down the change of load will reduce the chance of Δ entering the constant current region, as the integrators will be better able to track the change in demand, with lower transient error.

One way of reducing this effect is to slow down the voltage and current loops, so that the integrators do not ramp up so quickly. The simulation of a load change from 200 to 100R was run again, only this time the gains of the PI controllers were both reduced by about a third. The result of this is shown in **Figure 60**, where it can be seen that the output voltage recovers normally, albeit slowly with a transient peak of only 1.8V. However, slowing down the compensators will mean a reduced bandwidth. This will not only increase the transient recovery times significantly, but it will also reduce the tolerance of the system to noise (and more

importantly 50/100Hz ripple if the regulator is to feed an inverter) and is not desirable unless it is absolutely necessary.

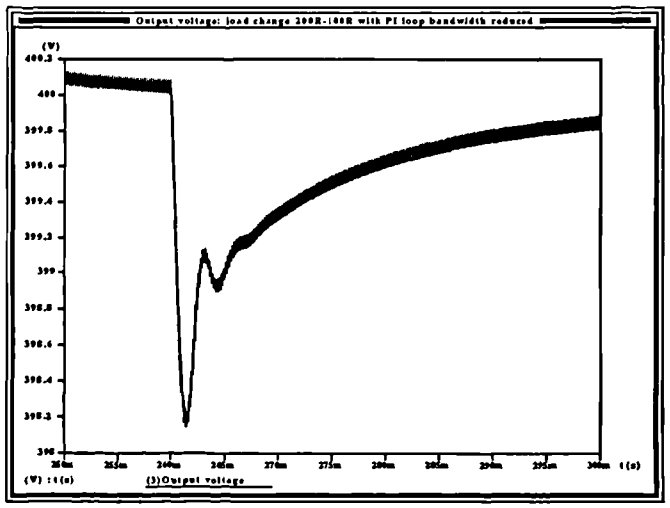

Figure 60 Output voltage of converter in 200-100R load change with slow compensators

A load that is extremely heavy would cause Δ to pass Δ_1 anyway, and the controller will not operate correctly in this region. This system in its current form has not only an upper limit to the value of load that can be handled, but also a maximum rate of change of load for a given set of PI controller constants.

The control strategy will need to be modified to get the best from this system, and a more detailed investigation into the characteristics of the PV-sourced converter with a view to understanding and improving the control scheme is the subject of the next section.

3.8.3 Characteristics of converter with variant sources: investigations.

It has been established in the previous section that across the converter operating range of Δ (and hence source voltage and current), the source moves from constant voltage operation to constant current operation. If the characteristics of **Figure 58** and **Figure 57** are superimposed upon each other on axes of the same scale (**Figure 61**), then the point at which they intersect should show (approximately) the point at which the transition between constant voltage and constant current occurs. For a fixed load, it can be seen from the graph that this occurs at maximum power.

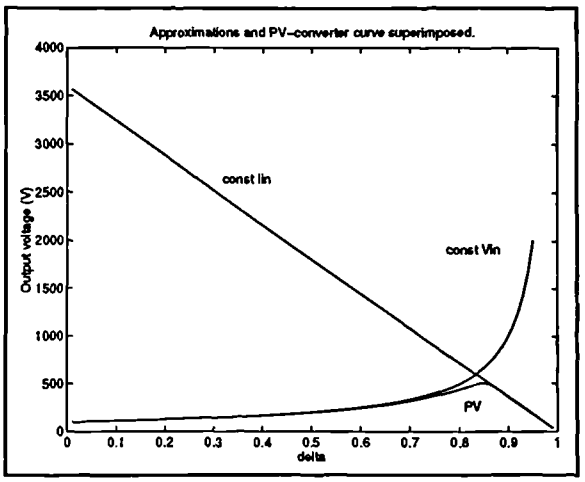

Figure 61 Constant voltage and constant current curves superimposed.

Loads that exhibit the characteristics of a voltage source with current limiting (or a current source with voltage limiting) such as the PV arrays fall into a class of sources that have a maximum power point. All practical sources exhibit this effect as they possess series resistance which will limit the current drawn from the source, although in most traditional sources used for power supply this resistance is very low and it can be considered to be negligible across the operating range of any connected converter. Sources such as the photovoltaic array, however, have intrinsic resistances which are not only larger than those associated with conventional power sources, but also nonlinear. The result is that the transition between constant voltage and current limiting occurs within the operating range of the converter. Consider a load resistor connected across the source. As the resistance decreases from infinity, so the power drawn from the source increases. A point is reached when the converter input impedance is equal to the source impedance - beyond this point the source impedance dominates and limits the current that may be drawn from the source hence reducing the power into the load for heavier loads.

Since the maximum power point is a source-load phenomenon and the converter is little more than an impedance-matching device between source an load, then the maximum power point in the Δ versus output characteristic of the converter should coincide with the maximum power point of the photovoltaic array. To investigate this it is necessary to solve the steady-state transfer equations for the system simultaneously with the characteristic equation of the solar array. The nature of the solar array equation is such that it may only be solved effectively using numerical techniques. A MATLAB script was written in which the steady state transfer function for the boost converter was solved to give an expression relating input voltage and current to Δ and the load resistance **(62)**.

$$\frac{V_o}{V_{in}} = \frac{1}{(1-\Delta)}, \frac{I_o}{I_{in}} = (1-\Delta)$$

$$\therefore \frac{V_o}{I_o} \cdot \frac{I_{in}}{V_{in}} = \frac{1}{(1-\Delta)^2} \qquad (62)$$

$$\text{and since } R = \frac{V_o}{I_o},$$

$$\frac{I_{in}}{V_{in}} = \frac{1}{R(1-\Delta)^2}$$

This was in turn substituted into the solar cell equation **(1)** and solved using Newton-Raphson techniques to obtain values of V_{in},I_{in}, and by back-substitution into **(62)** values of V_o,I_o. Solar cell parameter values were obtained using a MATLAB script to solve the parameter equations determined in section 2.

Four values of load were used in the generation of these plots, to show the effect of different converter loads on the position of the maximum power point. The first of these plots shows the array current (**Figure 62**) and voltage (**Figure 63**) versus Δ.

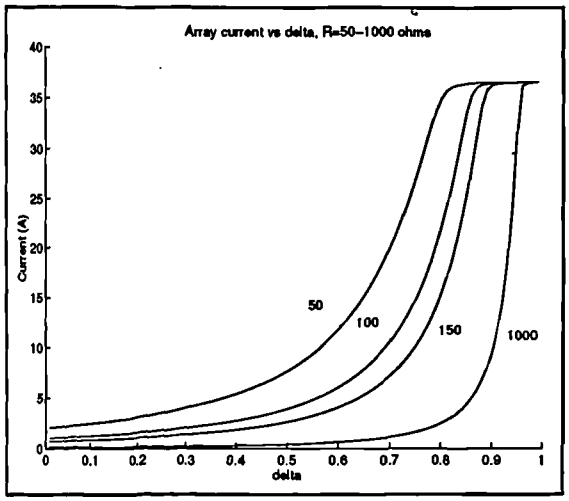

Figure 62 Steady state array current versus Δ.

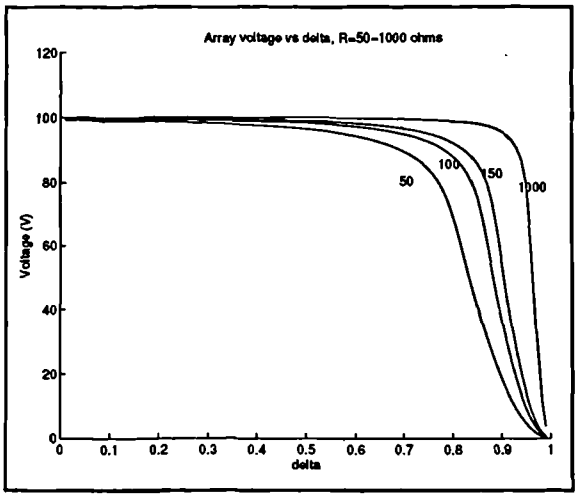

Figure 63 Steady state array voltage versus Δ

It can be seen from **Figure 62** that the minimum array current (when Δ=0) differs with load, and is equal roughly to V_{oc}/R_{load}. The maximum array current, however, for all loads is equal to I_{sc}=36A.

The two plots of **Figure 64** and **Figure 65** show the load voltage and current versus Δ. The maximum voltage point is clearly defined, and moves up and outwards with load as would be expected. Load current also shows maxima for each load value, and these maxima coincide with the voltage maxima.

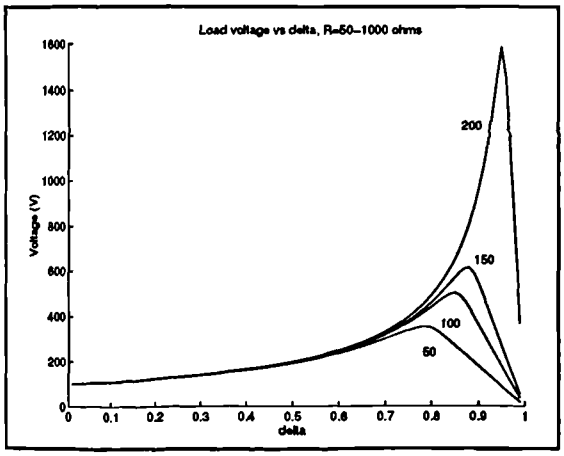

Figure 64 Load voltage versus load and Δ

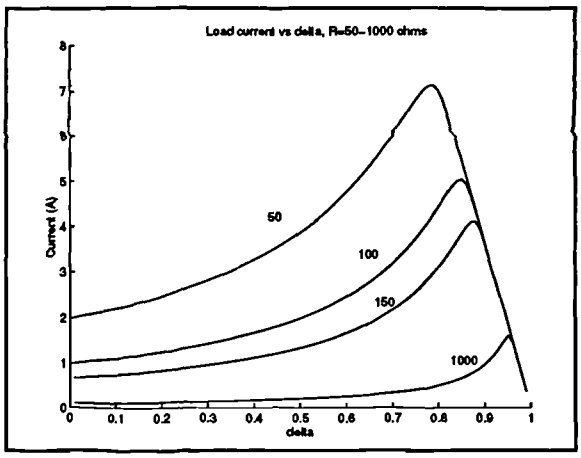

Figure 65 Load current versus Δ

Finally, **Figure 66** shows the variation in array power with Δ for different values of load, while **Figure 67** shows the variation of load power with Δ for the same load values. As can be seen these curves are exactly the same, reinforcing the concept of the converter as an impedance-matching device. The maxima may clearly be seen and are all at the same value of power, and this value coincides with the maximum power obtainable from the array under the environmental conditions prescribed for it (10000arb, 37°C).

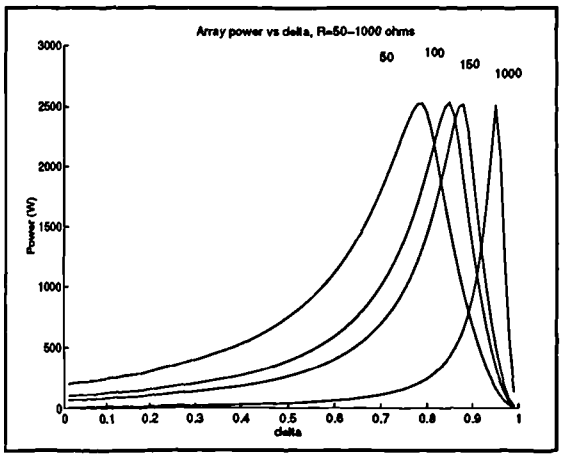

Figure 66 Array power versus Δ

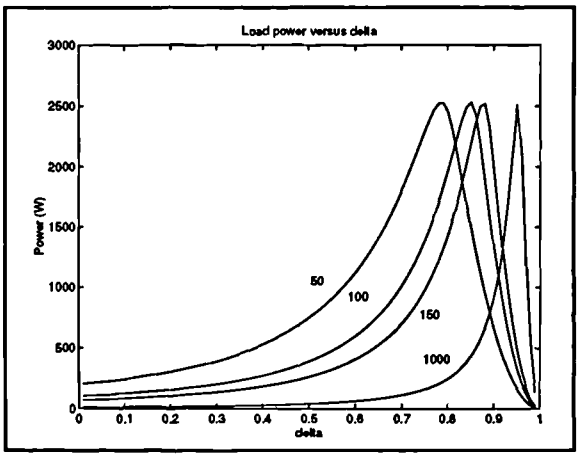

Figure 67 Load power versus Δ - resistance values in ohms.

If the two curves of **Figure 61** are superimposed also upon the curve obtained using the real array model for the 200R load (**Figure 68**), then it can be seen that the point of intersection of the constant current and constant voltage curves makes quite a reasonable approximation to the position of the maximum power point (where $\Delta=\Delta_1$). It also shows just how close to constant voltage and constant current the two sides of the cell characteristic are: in fact the approximation is quite good out of the neighbourhood of the maximum power point. This indicates that in the region of $\Delta<\Delta_1$, the conventional control methods associated with constant-voltage sourced converters should work without problem - and the Saber simulation results back this up. However, it remains to be seen how to improve the control algorithms in the region of $\Delta\geq\Delta_1$.

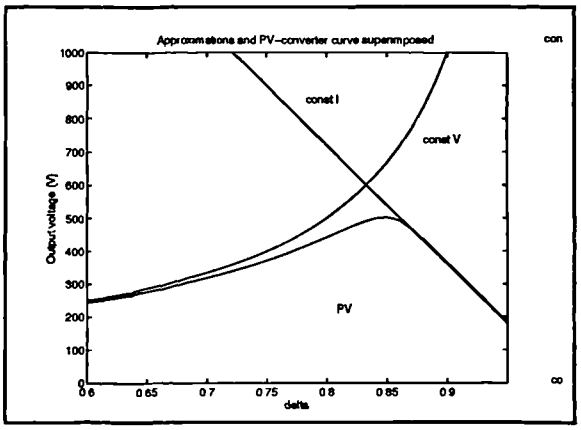

Figure 68 Approximations and array curve superimposed.

3.8.4 Control algorithms in the constant-current region.

It has been shown that for values of Δ below Δ_1 the converter will exhibit steady state characteristics consistent with those of a voltage-sourced converter. However, for values of $\Delta>\Delta_1$

the converter behaves differently. One of the major differences is that in this region, the slope of the curve of V_{out} versus Δ is negative. This indicates that if operating in this region, to increase the output voltage (or current) the controller must reduce Δ: in this region I_{out} is proportional to $(1-\Delta)$.

Consider a conventional PI compensator in the inner (current) loop, a block diagram of which is shown in **Figure 69** complete with the feedback paths. The current loop has direct control over Δ, and is therefore more relevant to this issue. For a fixed, positive demand signal I_{set}, the error will be large initially, and the integrator output will start to ramp up from zero, increasing Δ. I_d increases with Δ and the error is reduced. If the error is sufficiently large, so the integrator will ramp up faster, causing Δ to increase beyond Δ_1. At this point the characteristics of the converter change so that as Δ increases, I_d decreases. If nothing is done to modify the algorithm, the integrator will continue to increase Δ faster in an attempt to reduce the error, while it is actually increasing it. The larger error will cause the integrator to eventually reach its saturation limit in the positive direction, with no way of recovery unless the error is reduced i.e. the load is shed reducing I_d.

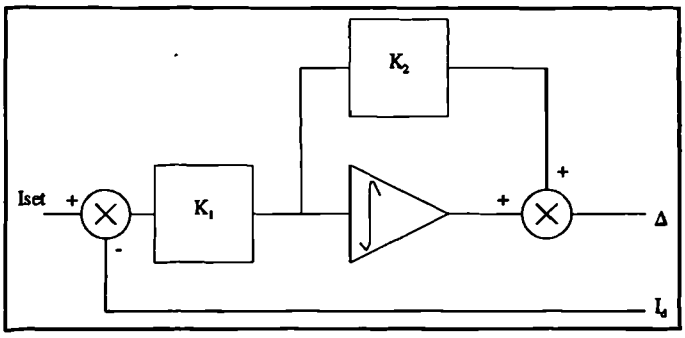

Figure 69 PI compensator block diagram.

In a constant current sourced inverter the output current reduces with increasing Δ, with $I_{out}=0$ for $\Delta=1$. The simplest way of controlling this type of converter in this region is to change the sign of the gain in the compensator in the current loop (K_1 in **Figure 69**), and set an initial condition on the integrator prior to startup of full saturation ($\Delta=1$ for zero output with constant current source). The result of this would be that the integrator would now ramp downwards for an increase in error, and would meet the criteria for control of a constant-current sourced converter. The net effect is that in current sourced operation, the sign required of the compensator in the control is negative. Note that the change in sign is within the compensator only, it can not be in the feedback as to obtain a valid error signal the positive I_d must still have a positive I_{set}

subtracted from it in order to maintain a 180° loop phase. The sign change only reverses the direction of the integrator in the compensator.

3.8.5 Embedded maximum power algorithm

The requirement of a PV system converter as with any converter driven from a maximum-power source, is simply to combine control for voltage source and current source in the same system. The same controller can be used, with some method of reversing the sign in the current loop compensator gain should Δ pass Δ_1. In the region $\Delta<\Delta_1$, the current loop compensator operates with a positive gain, whereas in the region of $\Delta>\Delta_1$ the compensator operates with a negative gain. This is shown graphically in **Figure 70**. Some method of detecting the transition between operating regions is needed. Given that the fact that into a given load the slope of the curves of both the load voltage and the load current versus Δ change sign, the simplest way would be to detect the change in slope by sensing $dI_{diode}/d\Delta$ or $d_{Vout}/d\Delta$. However, to do this in real-time would mean perturbing Δ, which is undesirable. The variation of these parameters could be determined using the natural variation in Δ caused by the integrator in the PI compensator, but there is another method which uses the inverter characteristics alone.

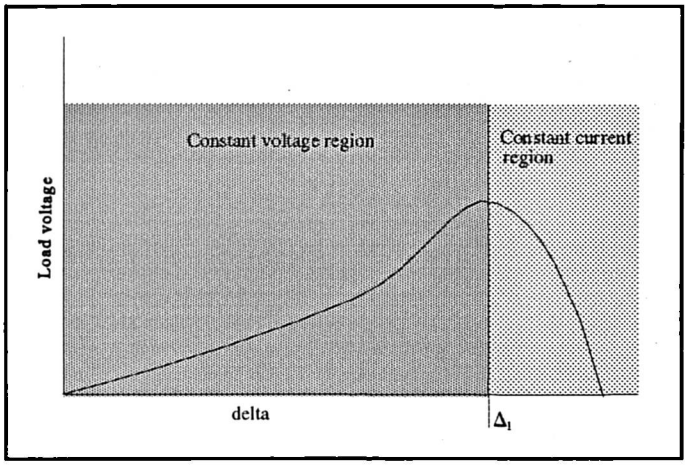

Figure 70 Regions of operations of PV controller.

It has been shown that the point of transition between voltage source and current source coincides with the point at which the array is providing maximum power. A simple way of detecting the position of Δ_1 and hence when to switch algorithms is to detect the maximum power point as it is traversed. To do this it is necessary to determine dP_{array}/dI (or dP_{array}/dV) and detect when its magnitude is zero: at this point where it changes sign the array is operating at maximum

power, and the current value of Δ is equal to Δ_1. Several different techniques have been developed to perform the calculation of dP_{array}/dI and these methods will be discussed in detail with maximum power tracking systems in section 3.9.

If at every switching cycle the value of dP_{array}/dI is evaluated, then the current region of operation may be detected. Once this has been established, the current loop controller can then operate with a positive gain, or a negative gain depending on whether Δ is less than Δ_1 or greater than Δ_1. The result of this is that correct operation will be maintained in either region.

3.8.6 Maximum power tracking: the link with conventional control

This control scheme results in some interesting effects. Consider the conditions at startup. The error is large and the integrator will cause Δ to increase. As Δ passes Δ_1 so the power sense indicates to the controller to change the sign of the compensator gain. There is still considerable error (I_{set}-I_{diode}),and now, owing to the sign change the integrator ramps *downwards*, decreasing Δ, in an attempt to decrease the error. The error remains large, however, and Δ decreases until it drops below Δ_1 where the sign of the compensator gain is reversed and the integrator ramps up once more.

The net result is that under conditions of large error, Δ will always oscillate about Δ_1. Since the point of Δ_1 coincides with the array maximum power point, the system will in fact function as a maximum power tracker. As the environmental variables change and move the maximum power point so the converter, under conditions of large error, will always move its operating point towards the array maximum power point. Such conditions of large error are: at startup, immediately after a significant load change, and if a very heavy load is applied. These areas were all where the PI-only system was not able to operate as they entailed Δ increasing beyond Δ_1.

When the error drops past zero, the operating point will change - it will move down the I_d versus Δ curve away from the point where $\Delta=\Delta_1$, and with this system, the region it operates

in will then depend upon which region of operation the system was in at the instant of the error dropping (see **Figure 71** for a graphical description). Since every operating point on the power curve in the constant current region is duplicated in the constant voltage region, theoretically the region of operation of steady state does not matter. In fact, why allow operation in the constant current region at all? The range of Δ in the constant current region is much less than that in the constant voltage region, and in the interests of DAC and PWM subsystem resolution in a discrete system it would be better to operate in the constant voltage region in the steady state for low loads as the range of Δ to I_{out} is larger. It is difficult to justify operation in the constant current region even if some other factor is present, such as the desire to parallel a number of converters -the current mode control already allows the converter to appear as a current source to its load while the *array* is operating in the constant voltage or maximum power region. To prevent operation above Δ_1 some mechanism must be in place to force the sign of the compensator gain positive once the error is cancelled, forcing Δ to drop with falling error, and placing the operating points in the constant voltage region. This will prevent operation in the constant current region. This is simple to implement, especially so in a digital implementation.

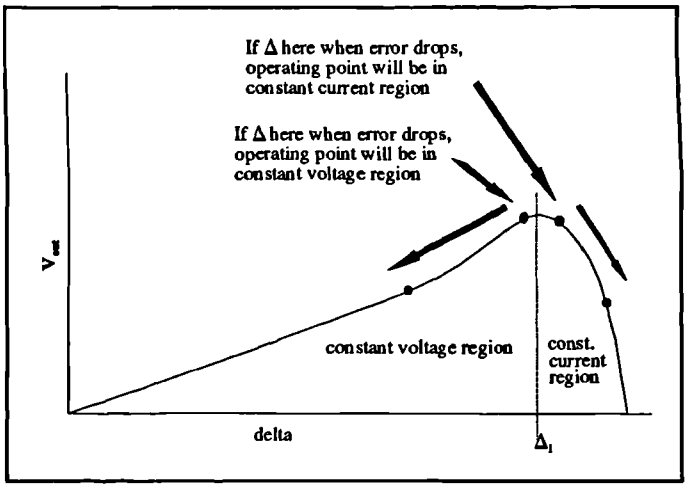

Figure 71 Regions of operation upon error drop with simple system.

There is one final aspect to the use of the PI compensator in the immediate neighbourhood of Δ_1. This is that if the error is large, the resulting steps taken by the integrator will be large, and these could easily step over the Δ_1 point and end up quite far down the curve in the constant current region. Then, when the sign of the gain is reversed the integrator input will still be large, so its step size will still be large and it could again step well over the Δ_1 point again, far back into the constant voltage region. If the error increases, then the integrator step size will also increase and worsen the problem. Some mechanism is required to slow down the integrator in the

neighbourhood of Δ_1 in order to reduce step size and operate closer to the maximum power point for greater efficiency. One way would be to force the integrator step size (time constant) smaller as Δ is close to Δ_1. Doing this means that for large error, as the operating point gets closer to Δ_1 so the error signal is no longer calculated as the difference of the current demand and sensed average current, and is reduced (down to a finite nonzero limit to prevent asymptotic approach to Δ_1). This action is that of a maximum power tracking controller.

The result of these requirements are effectively a combination of conventional PI control and a maximum power tracking system. To improve the response a dedicated, embedded maximum power tracker with superior characteristics can be switched in to replace the current loop under conditions of large error - and switched out again when the error falls. Care must be taken to preserve the state of the integrator in the PI controller while the maximum power tracking is active so as to ensure smooth transition between PI and maximum power operation and vice-versa.

A final note is concerned with transient effects. Note that momentary excursions of Δ past Δ_1 are acceptable in transient conditions in order to allow the inductor current to ramp up more quickly. Providing that these excursions of Δ do not cause the *average* inductor current (over one cycle) to increase beyond that associated with the maximum power point, the converter will continue to operate normally under PI control and there is no need for the MPP controller to switch in. In fact, the algorithm used for initiation of MPP operation should ensure that MPP operation will only commence if the average inductor current increases beyond that associated with maximum power - the initiation criterion is dependent only upon array power.

In order to implement the maximum power tracking function required in a convenient and efficient manner, an investigation was carried out into maximum power tracking systems with a view to determining a suitable approach to be used in this context. The maximum power tracking system must be able to be switched in and out of the current loop as required, as well as being efficient at tracking the maximum power point.

3.9 Maximum power tracking systems

It has been shown that an aspect unique to the control of photovoltaic systems and other systems with a defined maximum power point is that of the maximum power tracking algorithm. It has also been shown that the presence of a maximum power tracking system is essential to the correct operation of a conventional control strategy aiming at regulated voltage outputs. The position of the maximum power point will vary considerably across the 2-D parameter space (irradiance and temperature) of the arrays, but there are a number of points of interest to note regarding this variation:

1. Although the variation is across a wide range, the speed of the variation will be very slow with respect to all the time constants in the converter chain (a matter of seconds, for example for a cloud to pass causing a fluctuation in irradiance). To this end in tracking maximum power the dynamics of the converter chain may be neglected if the dynamics of the maximum power tracker are organized so as to be considerably slower.

2. The position of the maximum power point varies largely with irradiance. However, changes in irradiance will also bring about changes in array temperature (cell surface is dark in colour and will absorb energy), and this will also affect the position of the maximum power point as the cell voltage is inversely proportional to temperature. The net effect is that the position of the maximum power point may occur at quite a number of different combinations of cell voltage and current across the operating region of the cell.

3. If the cell characteristic at any given temperature/irradiance combination is plotted, it may be found that the maximum power point is not far from the cell open circuit voltage. Indeed, some very crude maximum power trackers used in battery-charging applications simply hold the cell operating voltage at about 70% of open circuit voltage. This is not the most efficient way of performing maximum power tracking, but this attribute of the cell characteristic is worth note.

4. Further to (2) and (3) above, the changes in solar irradiance tend to alter the *height* of the maximum power point, i.e. the level of maximum power that the cell can supply, except at very low levels of irradiance (and hence power) which are out of the normal converter operating range anyway. Changes in temperature tend to alter the lateral position (i.e. its position with respect to cell voltage) of the maximum power point in addition to its height, (see **Figure 72**).

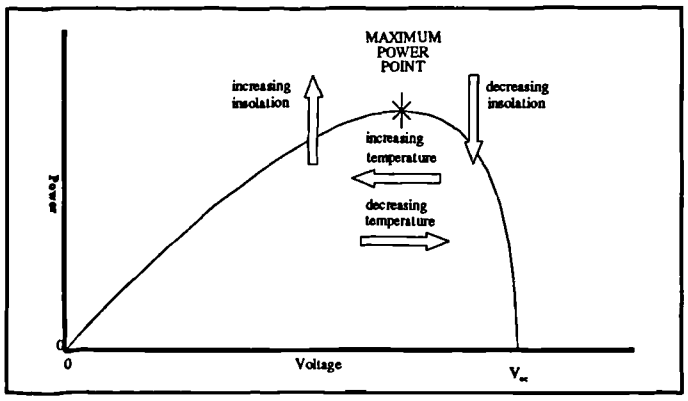

Figure 72 General effects of changes in insolation and temperature upon array maximum power point.

While a degree of information relating to maximum power tracking controllers has been published ([3],[4],[11],[38],[39],[40],[41],[42],[43],[44],[45],[46]) publication of detail of the actual technique used is infrequent (References [11],[38],[42],[43],[46] give some detail). These controllers rely on well known techniques for achieving a maximum power tracking controller which fall into two categories. The first of these categories is referred to in this thesis as the 'dither' method, as it relies upon the provision of an additional signal to provide slope information. The second category relies upon the control strategy itself to provide the operating point motion - this is referred to as the 'running-sample' method. The physical implementation of the techniques, however, differs with the specific requirements of the system as a whole. Given the importance of the maximum power tracking strategy as part of the overall control requirements of the converter system, it was decided to carry out a study of the two basic methods using implementations developed from scratch to suit the boost converter and control environment. In the light of the findings an improved technique for maximum power control strategy was then developed making use of a characteristic of the boost converter itself - the 'boost converter method'. This will cause the simple boost converter system described in section 3.4.1 to pass maximum power to a load (within the ranges that the power circuit can handle). This will result in an output with a characteristic such that the output voltage will change with load.

Obviously such a system is unworkable in practice unless the load is such that it requires the maximum array power at all times. Even a battery charger [8],[38] (which in the interests of speed and efficiency will want to operate at the array maximum power point for a discharged battery) will require some means of reducing the energy throughput once the battery starts to reach capacity. Although maximum power tracking is to form a part of the overall control strategy of a practical system, it may be developed and simulated alone. Once the maximum-power algorithm is found to work then it may be combined with the diode-current mode regulator to form the advanced control system.

3.9.1 Maximum power tracking - information available to controller.

The maximum power point will move around with changes in irradiance and temperature and it becomes necessary for the controller to follow this peak as it moves. The controller need not be particularly fast, as changes in insolation and temperature are slow in comparison to the dynamics of the power chain and controller. A limitation of the controller is that it must not require any embedded information about the type of array that is feeding the converter as this would limit the flexibility. The converter must thus determine its operating point using the array characteristic alone. To do this the array operating point must be made to deviate slightly by one means or another in order that the controller has more than one point of reference from which it may deduce which side of the maximum power point the operating point is currently positioned - it can not do this from a single point alone since in order to determine the position of the current operating point relative to the maximum power point, slope information is required. **Figure 73** shows this graphically. If the controller was only to know its current operating point, it would have no way of knowing at what

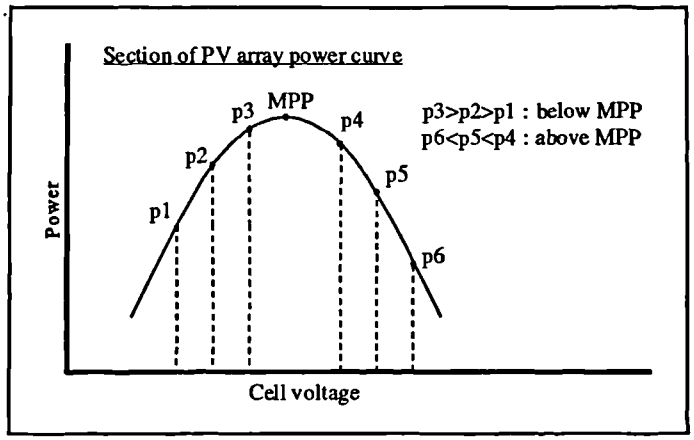

Figure 73 Operation of maximum power point tracking system.

side of the maximum power point, or how close to it, the system was operating. To obtain this information, the controller must therefore sample and store the value of power at its current operating point, change its operating point by either making use of the characteristics of the controller or by some specific signal and then sample the values at its new operating point. Once this is done, the controller is then able to determine in which direction it should move the operating point in order to intercept the maximum power point. Since varying Δ has a direct effect upon inductor, and hence input, current, during this analysis of maximum power tracking systems array power curves in this section have been considered with respect to array current as opposed to voltage. The basic shape of the curve is similar, however.

3.9.2 Maximum power systems, a concise overview

An analysis was carried out using a more formalized approach of the requirements of maximum power tracking systems in general. The manner in which any maximum power tracking systems must operate is given in **Figure 74**. This model is valid providing the dynamics of the maximum power tracker (the time constants of the integrator and those involved in the calculation of dP_{out}/di) are slow enough that the converter dynamics do not have to be considered. Providing input power is proportional to converter duty cycle δ, the maximum power algorithm can be expressed in the simple equation **(63)**.

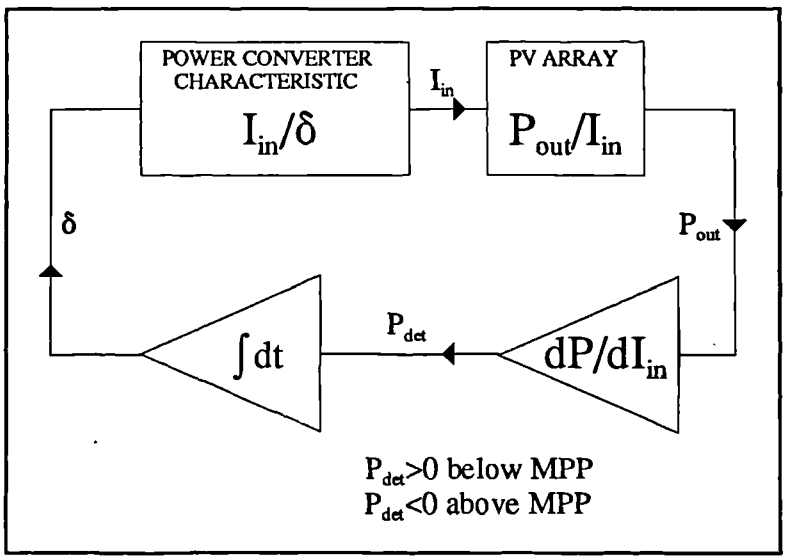

Figure 74 Block diagram overview of generalized maximum power tracker.

$$\delta = A_0 \int \left(A_1 \frac{dP}{di} \right) dt \qquad \textbf{(63)}$$

where A_0 and A_1 are the gains of the integrator and differentiator respectively.

All maximum power tracking systems must solve **(63)** in one manner or another. The differentiator identifies the maximum power point, and determines the position of the current operating point with respect to it while the integrator allows the operating point to move, in the direction of maximum power. Sometimes a comparator is placed after the differentiator, comparing the output of the differentiator with zero and providing either an 'up' or 'down' signal to the integrator. If this is the case, the speed of the integrator is fixed and is not dependent upon the magnitude of the derivative of the power curve with respect to current - only the sign of it. In this context this is referred to as a 'fixed integration' system. Without the comparator, the speed of the integrator is dependent upon the value of the derivative of the cell power - in this thesis this is referred to as 'proportional integration'.

The implementation of the maximum power tracking systems that were investigated as part of this research differ from each other only in the manner in which dP_{out}/di is calculated, all of them use an integrator to move the operating point. The magnitude of the slope given by dP_{out}/di must be calculated with care, as it is this calculation that nearly always governs the effectiveness of a maximum power tracking algorithm. The integrator gain will have some bearing on the transient response of the system, particularly if it is large enough not to allow the converter dynamics to be ignored.

Although in this set of applications the derivative of the power curve is taken with respect to array current, there is no reason at all why the derivative should not be taken with respect to array voltage if the power chain topology makes this approach desirable. The curve of array power with respect to voltage has a very similar shape as that with respect to current: the major difference being that the negative slope beyond the maximum power point is much steeper and integrator time constants may have to be modified as less overshoot of the maximum power point would be tolerable (it would cause a much larger deviation in power throughput.

Since a maximum power tracking system requires slope information, and to gain this slope information it is necessary to move the converter operating point, it is clear that the converter will not be continuously operating exactly at the maximum power point. When the converter is tracking maximum power, the operating point will move from one side of the maximum power point to the other. **Figure 75** shows this effect when a maximum power tracker is operating at the maximum power point. The power curve slope information is obtained by forcing the array current to move between two limits (di in **Figure 75**). When the converter is operating at the maximum power point, the difference in array power between the points at i and i+di will be zero (dP=0). Since the operating point is moving between these points a small portion of the power curve is swept, and the average power will be formed by the area of the power curve swept divided by the amplitude of di and this will be slightly below array maximum power.

It can be seen that the larger the deviation in converter operating point while tracking maximum power, the further below maximum power the converter power throughput will be. In order to determine the slope of the power curve some deviation in converter operating point is necessary, however in the interests of best exploitation of the PV arrays this deviation should not become excessive.

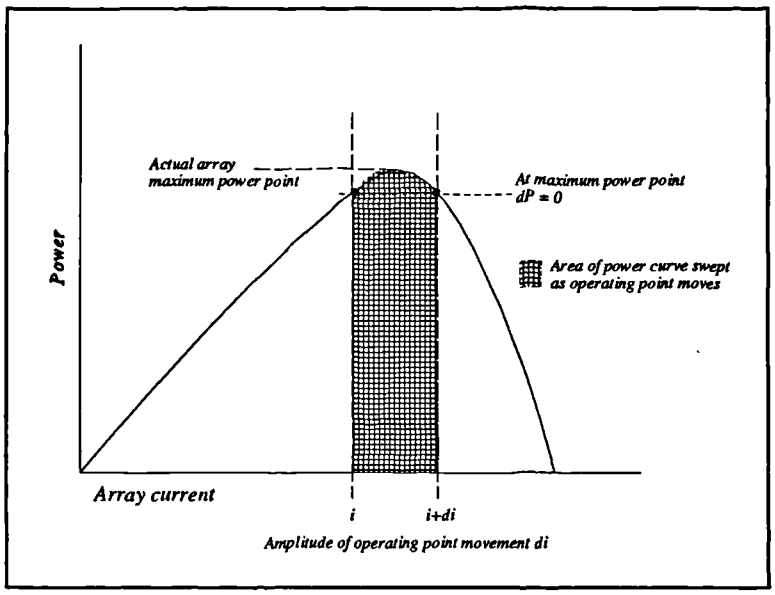

Figure 75 Maximum power throughput reduction caused by the need to determine array power curve slope information.

The actual reduction in power throughput caused by this effect will not usually be large enough to cause a problem unless the deviation really is excessive as the majority of array power curve maxima are not particularly sharp. It is worth noting this phenomenon, however should new array types become available which do possess sharp maxima in the power curves. It is worth noting that in addition to any signal deliberately introduced in order to facilitate power curve slope

determination the converter input ripple current itself will bring about a similar effect and this also should not be allowed to become excessive in relation to the size of the array full load current.

3.9.3 Dithering signal methods

A simple method of calculating dP_{out}/di is to vary the current operating point by superimposing a small-amplitude low frequency squarewave upon the converter control signal, and sampling the array power just before each transition of the squarewave. The boost converter has a single control input consisting of a pulse-width modulated switching signal. The input to the pulse-width modulator is directly proportional to the pulse-width, and may contain any frequencies from d.c. to less than half the switching frequency. The operating point of the converter as seen from the input may be varied by altering the steady-state value of this control signal. The first power sample is taken at the end of the low period and the second at the end of the high period. The direction of the change of operating point required to intercept the maximum power point may then be calculated. Owing, however, to the serious non-linearities of the array power characteristic it would be impossible to calculate the *exact* relative position of the maximum power point without the controller being aware of the array parameters in advance - even then it would be a computationally intensive task. To avoid this problem the old and new values of the operating point provided for by the dithering signal can then be used to determine in which *direction* the operating point should move to always tend toward maximum power ($dP_{out}/di=0$). If the second sample is larger than the first, as converter input current rises with the control signal amplitude, the operating point is below the maximum power point and

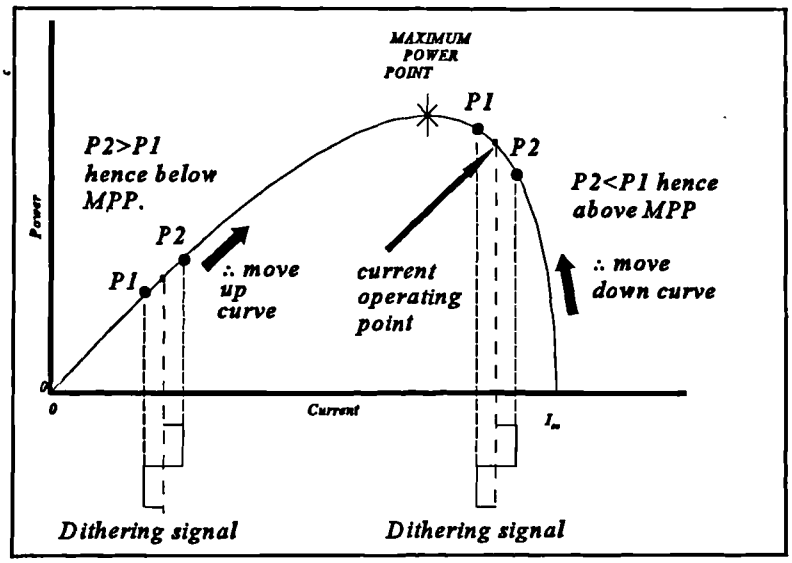

Figure 76 Maximum power tracker: external dither method.

should be moved in the direction of increasing cell current. If the second sample is less than the first, the operating point must be above the maximum power point, and the operating point should move in the direction of decreasing array current. Therefore the necessity of a means of obtaining power curve slope information is met. **Figure 76** shows the operation of the system both above and below the maximum power point. For correct operation, the speed of the general motion of the operating point should not be so fast that the dithering signal is unable to establish the two samples with the second further up the curve than the first, otherwise dP_{out}/di will be invalid and the system will be unlikely to acquire the maximum power point, let alone track it. The time-constant in the integrator must be selected to be much slower than the dynamics of the converter power chain, while the amplitude of the dither signal must be large enough to be resolved when the position of the maximum power point changes (relatively) rapidly. A lower limit upon the integrator time constant is ensured by the simple fact that the system will not track a fast moving maximum power point if the integrator time constant is too slow: it will follow it, but the converter operating point will fall short of the maximum power point as the integrator tries to 'catch up', unless the maximum power point ceases to move whereupon the operating point will eventually intercept it. If the integrator time constant is too fast, the integrator will 'wind up' as the converter dynamics change slowly, and the result will be decaying oscillations as the integrator 'chases' the operating point. Although the technique is not new, (an example of the use of this approach may be found in reference [11], where the dither signal is in fact formed by allowing a small amount of 120Hz ripple from the live load to appear on the input), the implementation was developed from scratch.

Apart from any question of converter power throughput being reduced at maximum power in the presence of large dither signals, an upper limit upon the amplitude of the dither signal is brought about by the more important consideration that the dither signal will not be rejected at any point in the converter chain and will appear superimposed upon the output voltage signal - the tolerable level of which provides an upper limit.

As a result, a disadvantage of this system is the interdependence of control parameters required to produce the optimum arrangement: namely dither signal amplitude and integrator time

constant (assuming the converter dynamics are fixed for a given design strategy). To obtain the optimum values of these parameters requires an empirical evaluation for a given design, together with a knowledge of both the range and the fastest slewing of the environmental parameters: temperature and irradiance.

3.9.3.1 Implementation in simulation of dither method.

Implementation of this method is fairly straightforward. An integrator may be used to provide the necessary motion of the operating point, while the square-wave dither signal is easily generated. The array power is obtained by sampling current and voltage, and multiplying the two values. A comparator generates the sample difference P2-P1. An integrator converts this to a ramp and moves the operating point. One point worthy of note is that the output of the comparator will be invalid during the period between the two samples P2 and P1, and therefore there must be some form of latch at the output of the comparator to gate this out while the samples P1 and P2 must be held using a sample and hold system. The resulting controller is relatively simple, requiring a multiplier, two sample and holds, a comparator, a latch and an integrator.

3.9.3.2 Design of appropriate controller.

The above implementation may be realized in the block diagram of **Figure 77**, where the associated timing is shown in **Figure 78**. This system is quite amenable to easy implementation in a digital form where the sampling would be very easy to achieve and timing could be derived from the same source as the timing for the PWM modulator - the

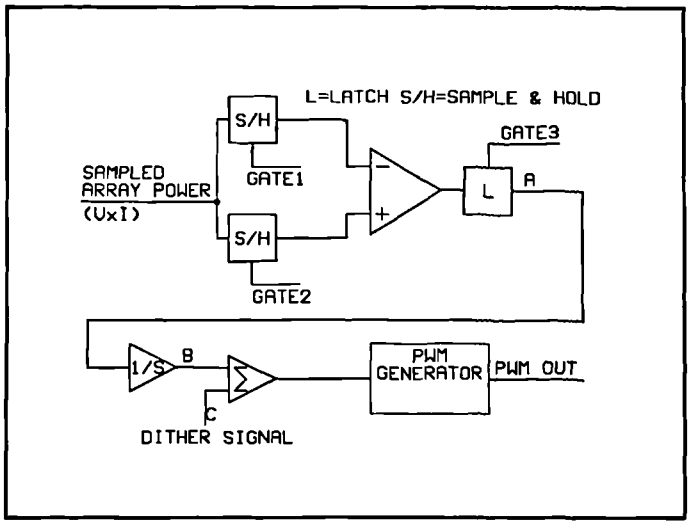

Figure 77 Implementation of dither algorithm.

entire controller could be implemented digitally with little difficulty.

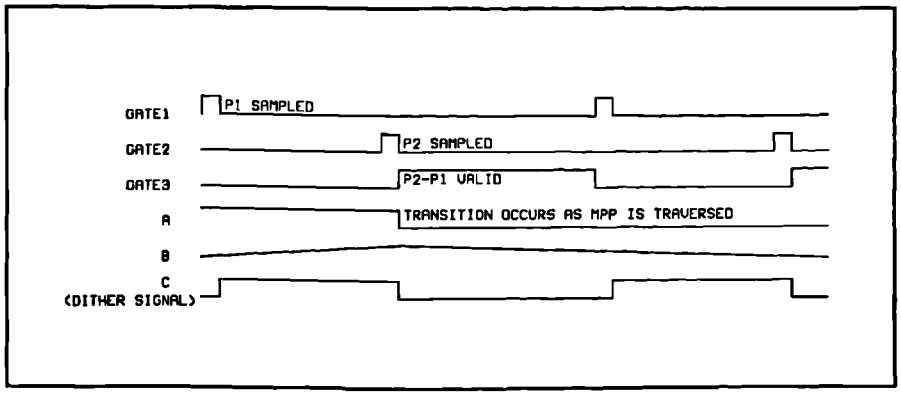

Figure 78 Timing *diagram for dither method*

3.9.3.3 Implementation of simulation model.

The implementation of the simulation model of this system was effected by entering the schematic of **Figure 34** using appropriate component models and netlisting it using the DesignStar front end. The controller was implemented using a single template, and a symbol was created with which to reference it through DesignStar. The complete schematic for the simulation model exported from DesignStar is given in **Figure 79**.

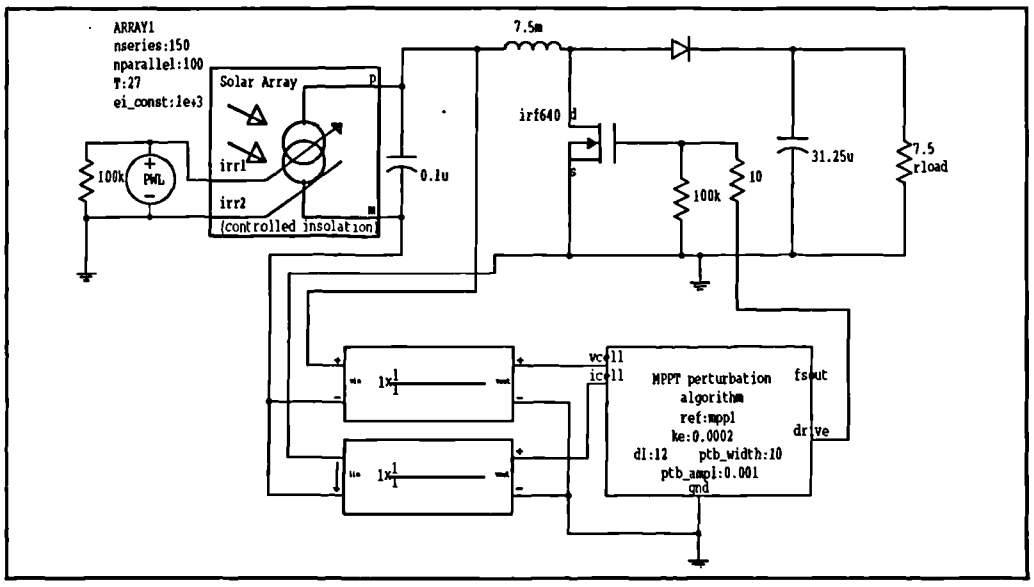

Figure 79 DesignStar schematic for dither method system.

Most of the MAST template referenced by the block 'MPPT perturbation algorithm' in **Figure 79** is associated with declarations, parameter passing and type-checking, the generation of a 'clock' signal at 25kHz from which the PWM switch drive is derived, also the generation of the PWM signal itself. The parameters passed to the template from DesignStar are:

t	:	1/(desired frequency of PWM) = maximum on or off time
ke	:	Time constant of integrator
dl	:	Amplitude of drive signal to switching device
ptb_width	:	Period of dither signal, measured in an (integral) number of PWM switching cycles
ptb_ampl	:	Amplitude of dither signal in terms of δ, i.e. how much should δ vary with the fluctuation in dither signal.

The template implements **Figure 78** in a discrete form, where the integration is performed by increasing δ in finite steps, the amplitude of which is specified by the parameter 'ke'.

3.9.3.4 Operation of simulation model of dither method.

The irradiance profile was set as in **Figure 80** by way of the piecewise-linear source coupled to the irradiance control pins of the array model. (this was simply a convenient way of making the irradiance variable across the duration of the simulation run). The array specification was modified from that in section 3.8.1 to place the maximum power point within the design range of the converter, and a 150x100 cell array gave maximum powers of 1430W at 15000 arbitrary irradiance units, 950W at 10000 irradiance units and 850W at 700 arbitrary units. The efficiency and operation of the maximum power tracker will be dependent upon the value of the integrator time constant. This was initially set to 0.0005, that is a step increase in δ of 0.0005 after

each complete dither cycle. A 200ms time-domain simulation was run and **Figure 81** shows a plot of the array power and irradiance profile versus time. Although the tracking is quite reasonable when the array powers at the 'flat' portions of the curve are compared with the corresponding powers obtained from the associated irradiance for the given array, when the irradiance changes to a different level the maximum power tracker has to 'catch up'. It should be able to follow a much slower change with little difficulty, but to simulate a change that would be realistic in terms of actual changes in environmental variables would take an excessive period of time to run, as well as demanding too much storage space for simulation output files. However, it proves interesting to investigate the effects of changes in the integration constant (ke).

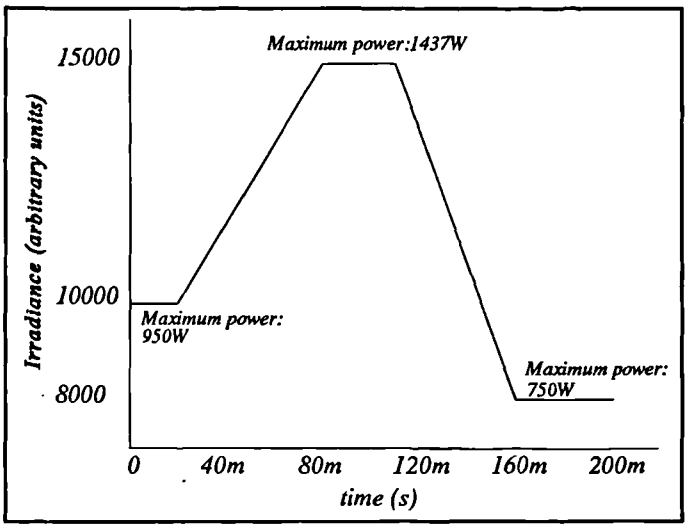

Figure 80 Irradiance profile as used in MPP experiments.

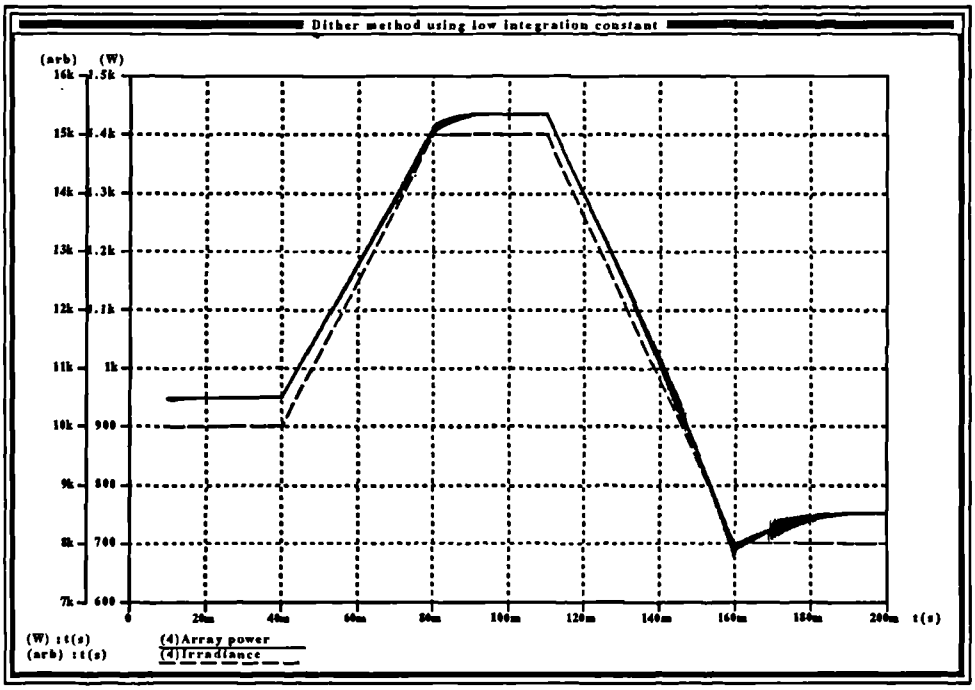

Figure 81 Array power and irradiance profile with ke=0.0005

As the tracker in **Figure 81** is operating too slowly, the integration constant was increased to 0.001, and the simulation re-run over the same interval and with the same irradiance profile. The result is shown in **Figure 82.** This power profile follows the irradiance profile much more cleanly, with only a small amount of lag at the end of the downward slope. If the tracker will track a maximum power point that is moving that fast, it will have no trouble with much slower, more realistic profiles. However, if the integration constant is set too high, then the controller is much less able to track the changes effectively, as is shown in **Figure 83** where the simulation was re-run with an integrator time constant of 0.005. It can be seen from this that the useful range of integrator time constants is limited, and very narrow. If this is scaled down to the much lower values used in an actual system where the irradiance profile changes a lot more slowly, then care will have to be taken to ensure that an appropriate value of 'ke' is selected.

Note that the effective total integrator time constant is in fact a combination of the 'ke' parameter and the width of the dither signal. In effect, 'ke' gives the resolution of the integrator, i.e. the size of the minimum integration step while the width of the dither signal gives the length of time between step changes in δ - the combination is the equivalent of the time constant of an analog integrator. The dither signal width is fixed at the minimum possible value which just allows the converter chain to stabilize in steady-state after the change in δ brought about by the dither signal itself. This ensures that the converter dynamics do not enter the maximum power control algorithm. With the dither signal width fixed in this manner, variations in 'ke' alone controls the integrator time constant with its upper limit fixed by the relationship between the converter dynamics and the width of the dither pulses.

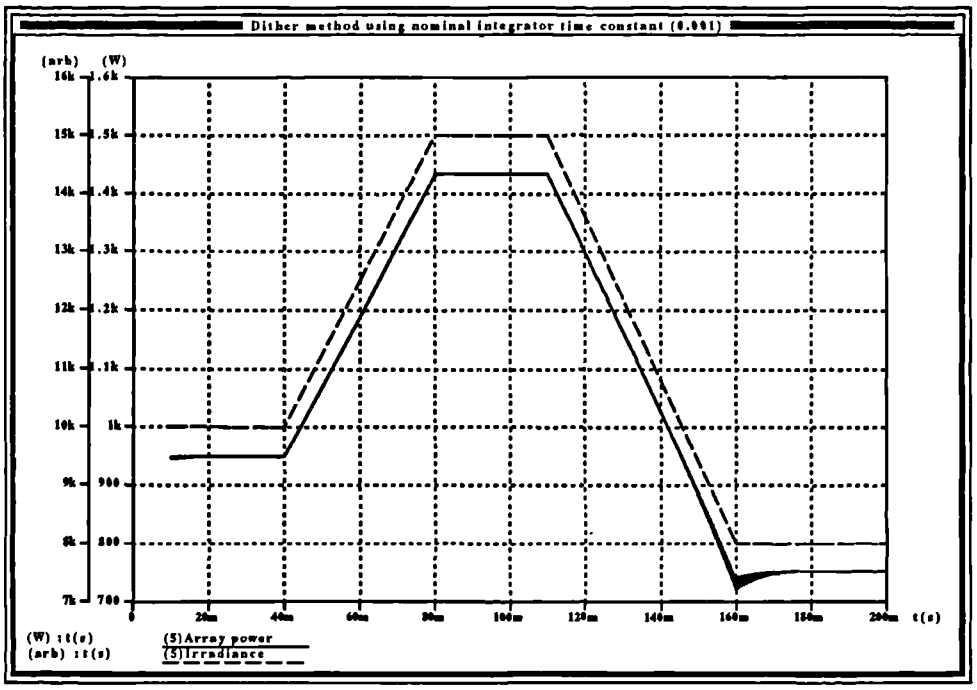

Figure 82 Dither method using nominal integration constant.

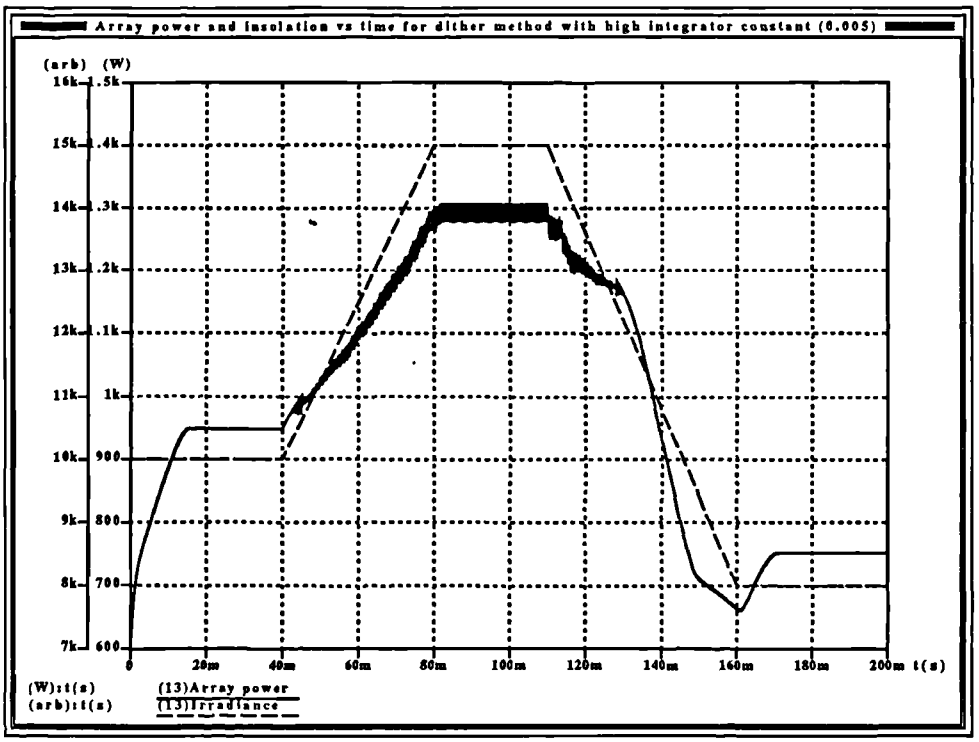

Figure 83 Effects on power curve of higher than nominal integration constant.

Given that this method involves the direct injection of a dither signal into the control, it is also important to investigate its effects. It is important that the dither signal is not swamped by an operating point which is moving so fast that the controller is unable to establish two power samples, one further along the curve from the other in the direction of increasing current. This means that the higher the integration constant 'ke', the greater the amplitude the dither signal needs to be in order not to be swamped. In the case of this template, both dither signal and integrator constant are measured in fractions of δ to be added and subtracted and the dither signal amplitude should always be larger in value, or equal to, the integrator constant. However, as the dither signal amplitude is increased, so the converter power throughput while tracking will be less than array maximum power.To improve efficiency, the amplitude of the dither signal must be as low as possible given both the integrator time constant and the fastest likely rate of change of environmental variables.

A further aspect of operation is that the dither signal will make itself known at the converter output. Owing to its low frequency it is impractical to filter it. The dither signal used in the simulation runs had an amplitude of 0.001, i.e δ would change by 0.001 across the dither cycle. **Figure 84** shows the output voltage waveform from the converter at 15000arb irradiance across a small portion of the simulation run of **Figure 82** and clearly shows, apart from the fast switching ripple, a superimposed ripple with a period of 20 switching cycles (400μs) and an amplitude of about one volt. This may, or may not be significant depending upon the application, but is something that has to be considered when using this algorithm. **Figure 85** shows the complete curve of load power, as opposed to array power, where the effect of the switching ripple and dither signal ripple can clearly be seen.

A lower limit on the amplitude of the dither signal is enforced by factors of the physical implementation of such a system. If the dither signal is too small it is possible for the A/D converters sampling cell voltages and currents to run out of resolution: if amplification was used to avoid this problem then noise would become evident. Filtering of the higher frequency noise is possible as the only frequency of interest to the controller is that of the dither signal.

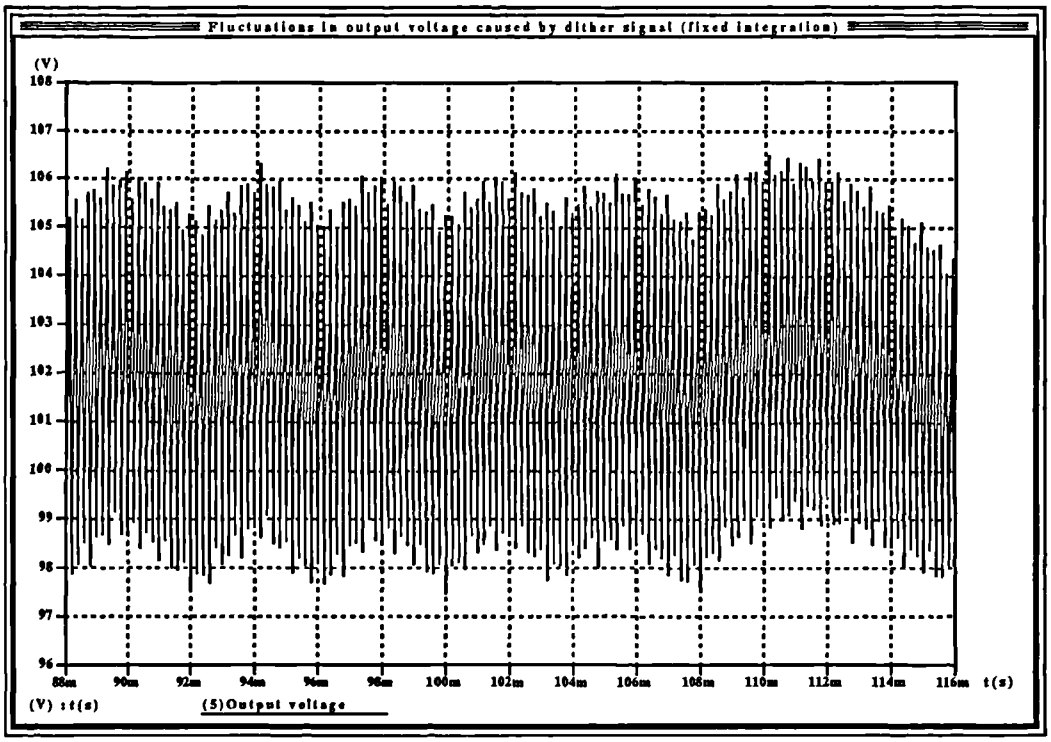

Figure 84 Output voltage of converter showing ripple due to dither signal.

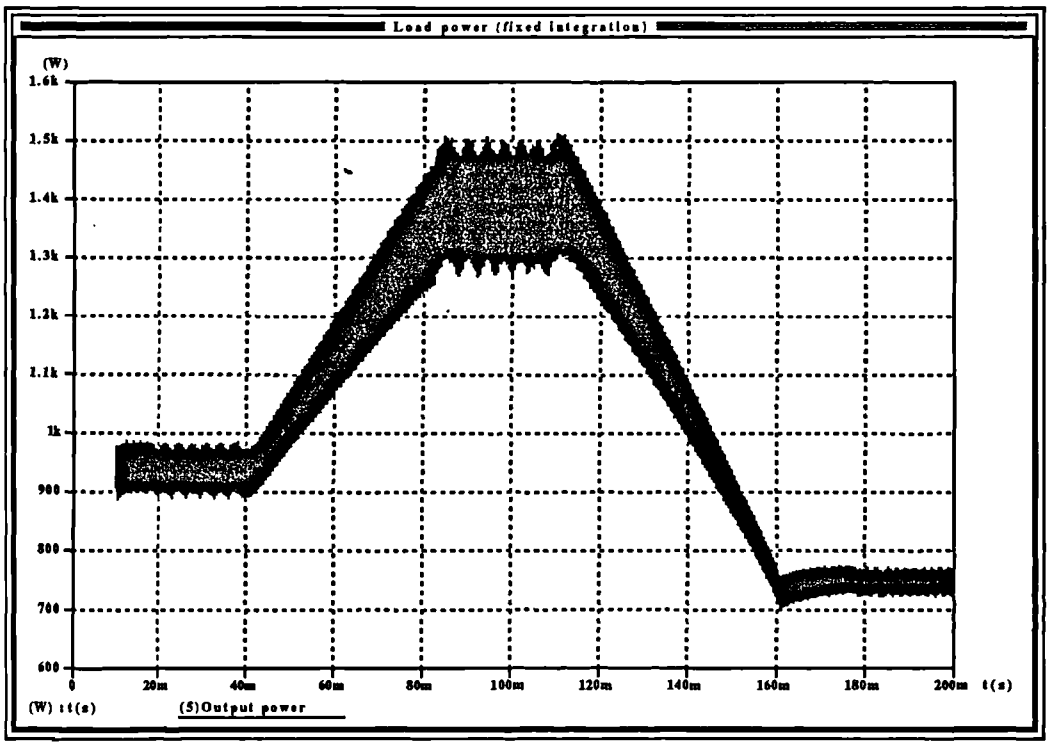

Figure 85 Load power from dither method.

3.9.3.5 Dither method with proportional integration.

The difference between two power samples taken each side of a small known variation in array current gives the value of the slope of the power curve at this point. It was found that if this is used directly as an input to the integrator then proportional integration can be achieved. Such a scheme has the potential to improve maximum power tracking. Far away from the maximum power point, the slope of the power curve is large compared to the slope of the curve in the neighbourhood of the maximum power point. If the speed at which the operating point moves can be made relative to the position from the maximum power point, it is possible to achieve a fast rate of acquisition to maximum power while reducing the amplitude of the oscillations about the maximum power point once the system has reached it.

It is slightly better to make the value obtained from p2-p1 (**Figure 73**) subject to a limit such that as the sample difference exceeds a certain predefined level the integrator time constant is limited at the associated value. This prevents integrator windup and saturation. In addition the magnitude of the integrator time constant is never allowed to fall below a much lower minimum value to prevent asymptotic approach to the maximum power point and slow acquisition. The slope of the power curve moving away from the maximum power point increases, and thus this system should result in fast acquisition of maximum power, while improving the tracking. With fixed integrator time constants, so the operating point will oscillate about the maximum power point with an amplitude proportional to the time constant of the integrator. The larger the amplitude of these oscillations, the further from maximum power the average power throughput. If the amplitude of these oscillations can be reduced as the maximum power point is approached, the average power throughput will be closer to maximum power.

The disadvantage of this system is that the maximum amplitude of the dither signal when the integrator time constant is small will have to be much greater than that used in the dither method without proportional integration. This is necessary to avoid swamping the dither signal when the operating point is moving quickly. If the dither signal amplitude was allowed to vary with the integrator time constant, so as the time constant decreased so the dither signal amplitude

was increased, the problems of continuously high dither signal amplitude would be surmounted. However, this would increase the complexity of the controller, as the varying amplitude of the dither signal would affect the magnitude of the difference between power samples and this variation would have to be compensated for in the calculation of the new integrator time constant.

To evaluate the proportional integration scheme, a design based upon a fixed dither signal amplitude was developed as a simulation model where the dither signal amplitude was set at a value (0.1) which would not be swamped by the fastest change in δ brought about by the action of the integrator.

3.9.3.6 Implementation of simulation model of proportional integration

The implementation of this method is very simple, the DesignStar schematic is shown in **Figure 86** and it can be seen that this differs from **Figure 79** only in the controller template.

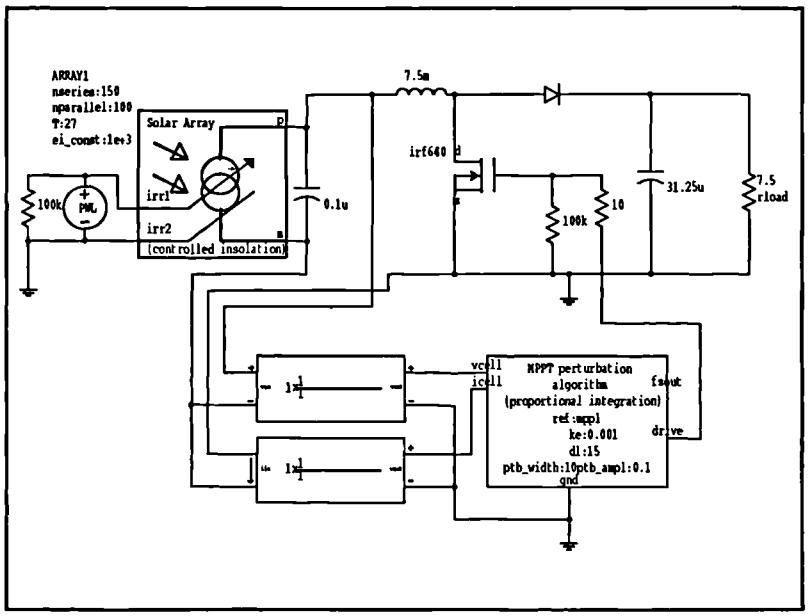

Figure 86 Schematic for dither method with proportional integration.

The result is that the integration constant is allowed to increase with 'e' (the difference between the two power samples) in either direction up to the limit of 20 times the nominal

integration constant (chosen to prevent excessive integrator windup). A lower limit is provided for: the magnitude of e is never allowed to drop below unity in order to prevent asymptotic convergence to maximum power and poor tracking. The result is a system which should combine the advantages of a proportional integration system (fast acquisition) with the advantages of the fixed integration system (good tracking for slow changes in maximum power point). This scheme uses a fixed dither signal amplitude, there is no reduction with maximum power point proximity.

3.9.3.7 Operation of simulation model of dither with proportional integration

The same irradiance profile of **Figure 80** was used in the simulation runs of **Figure 86** over a time of 200ms. Again this should be sufficient to demonstrate the operation of this maximum power tracking algorithm, and to determine how well it performs relative to other algorithms. The first run was taken using a minimum integrator step (ke) of 0.001. The result of the run (array power and irradiance vs time) may be seen in **Figure 87**. This clearly is not giving ideal results owing to the transient behaviour during the descending portion of the irradiance curve. However, the acquisition time from startup is very short (about 8ms, while the tracking of the ascending portion is very good; both as expected from this type of algorithm.

The transient behaviour during the descending portion of the curve may be explained by examining the shape of a typical array power curve (**Figure 2**). It can be seen that the slope of this curve drops sharply beyond the maximum power point. If the value of maximum power starts to drop off, i.e. the maximum power point moves in the direction of decreasing power, the integrator will attempt to follow it. There is an immediate overshoot where the system will be operating above the maximum power point temporarily and will be positioned on the steep drop of the power curve beyond the maximum power point. As the integrator catches up, so the array power rises again - and the cycle is then repeated. To remedy this, the minimum integrator time constant (and hence the maximum) may be increased. Slowing the integrator down reduces the overshoot.

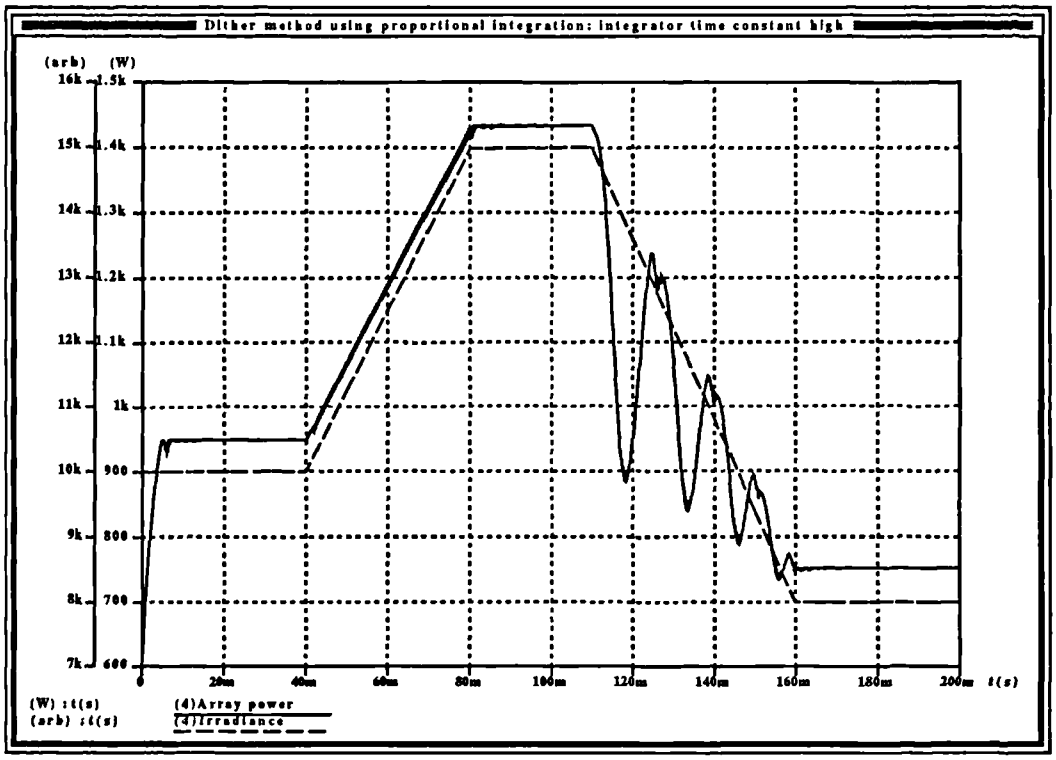

Figure 87 Array power and irradiance vs time with ke=0.001

The run of **Figure 88** was made with the minimum integrator step size (ke) changed to 0.0001 and this shows acceptable behaviour. There is evidence of a small overshoot (more obvious on the inductor current curve, **Figure 89**) at the discontinuities in the irradiance profile. In normal use there will never be discontinuities in an irradiance profile and therefore this is not an issue. Acquisition is not as good as for the fast integrator, this is due to the limitations on the maximum value that the integrator step size can reach - widening the range between maximum and minimum could help to improve this subject to the upper limits. Finally, a run was made using a much smaller integrator step size (**Figure 90**) in order to demonstrate its effect - where mistracking can clearly be seen.

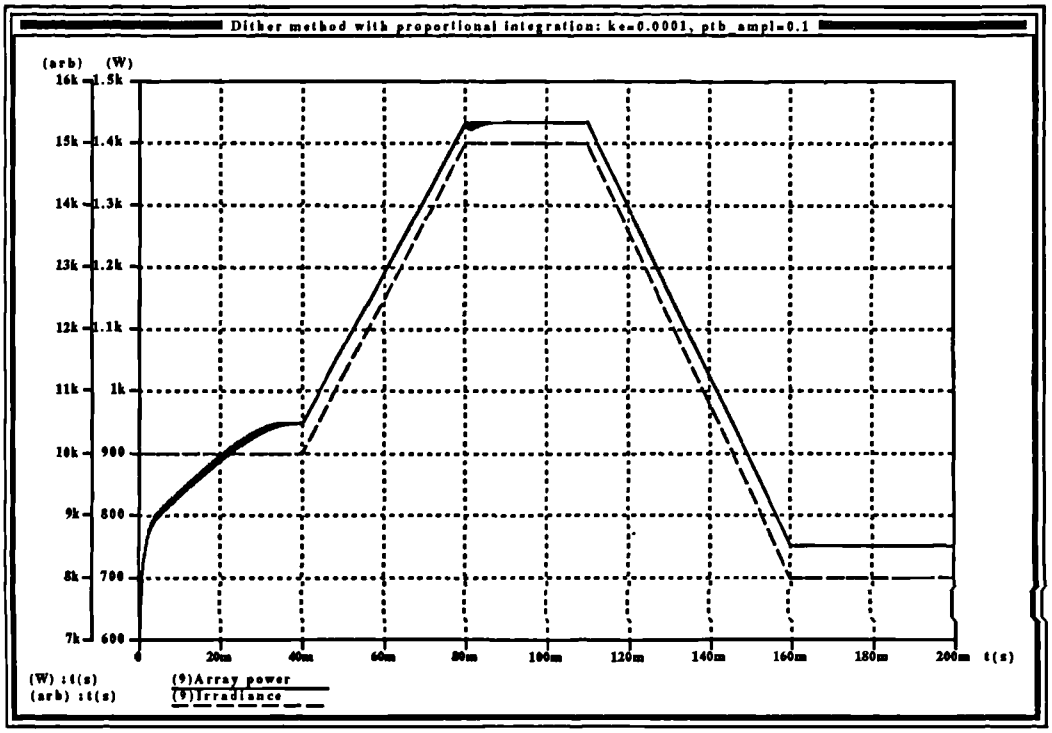

Figure 88 Integrator time constant of 0.0001, power and irradiance curves.

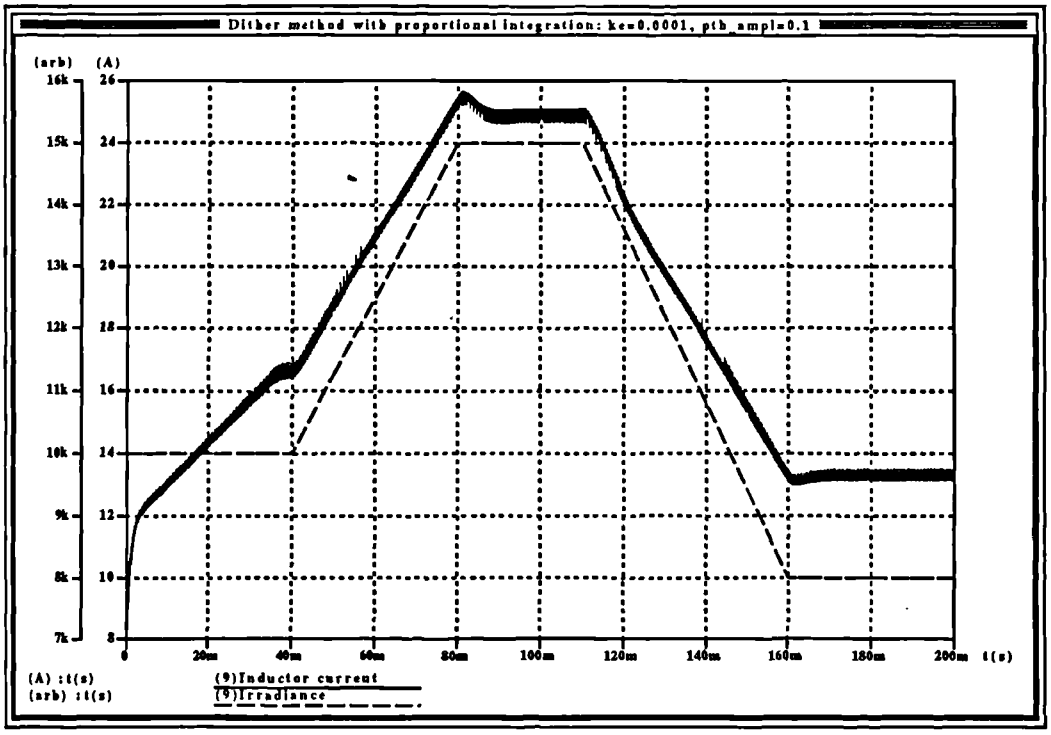

Figure 89 Inductor current using integrator time constant of 0.0001

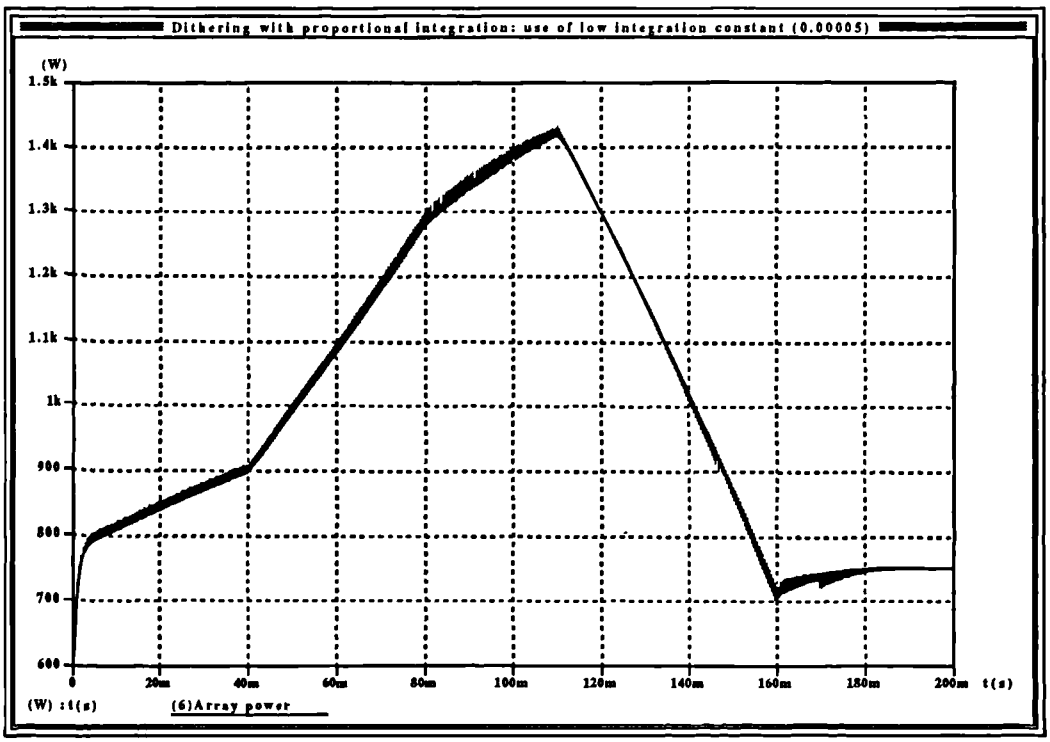

Figure 90 Power and insolation vs. time using low integrator step size.

3.9.4 Running-sample methods

Dithering methods all rely upon the injection of an additional signal in order to move the operating point slightly as a means of obtaining power curve slope information. Such systems always will have a disadvantage that the dither signal will appear at the output. This disadvantage may be overcome by the use of running-sample methods, which eliminate the dither signal completely and provide the required power curve slope information by maintaining the converter operating point in a constant state of motion ([42],[43],[46]).

All maximum power trackers require the operating point to move in the direction which will intercept the maximum power point. Since the operating point itself is moving due to the action of the integrator (from startup it will move up the curve in the direction of increasing current) it can be seen that the dithering signal may be removed and dP_{out}/di calculated by using two samples taken with a fixed time between them, for example an integral number of switching

cycles of **Figure 34**. Since the operating point would have moved in the duration between the two samples, the requirement of two samples to provide slope information is met. There will be a dependency of the magnitude of this value on the speed at which the operating point is moving, making this method unsuitable for proportional integration: as the speed of travel of the operating point reduces, the magnitude of the difference between the two power samples will also decrease, decreasing the integrator speed still further. Eventually the integrator will stall and result in tracking failure.

The sign information will always be correct providing the direction of travel of the operating point is taken into account. Assuming the operating point is moving up the curve in the direction of increasing current, if the first sample is greater than the second, the operating point is moving away from maximum power, if the second sample is greater than the first, the operating point is moving towards the maximum power point.

This method requires that the direction in which the operating point is moving be retained by the controller and used by the algorithm. For example, if the operating point is below the maximum power point and moving up the curve in the direction of increasing current then P2 (the second sample) will be greater than P1 (the first sample) and P2-P1 > 0. If the operating point then traverses the maximum power point it is then moving away from the maximum power point, and P2-P1 < 0. If the controller then reverses the direction of motion of the maximum power point in order to allow it to intercept the maximum power point, it is then moving *towards* the maximum power point and P2-P1 > 0 even though the operating point is still above the maximum power point. Thus the inequality is reversed once the direction of motion is changed and the algorithm used in the control must use the direction of motion of the operating point in order to resolve the true meaning of P2-P1 in terms of the position of the operating point relative to the maximum power point. **Table 5** shows this information in a more concise form. An alternative way of stating this is that there is a sign change in P2-P1 as the maximum power point is traversed for a given direction of motion, or that there is a sign change in P2-P1 as the direction of motion is reversed. P2-P1 alone does not provide all the information required to acquire and track

maximum power - the direction of operating point travel provides the extra variable necessary to complete the control algorithm.

Table 5 Power samples for running-sample method.

	Ascending curve	Descending curve
below MPP	P2-P1>0	P2-P1<0
above MPP	P2-P1<0	P2-P1>0

3.9.4.1 Implementation

At converter power-up the operating point is well below the maximum power point. From power-up the average inductor current in **Figure 34** will ramp up from zero. As the maximum power point is traversed, denoted by the point at which P2-P1 changes sign, then the direction of motion of the operating point is reversed by the controller to cause it to move in the direction of decreasing current. As the maximum power point is once again traversed, so P2-P1 once again changes sign and the controller reverses the direction of travel of the operating point. P2-P1 alone gives no indication of the direction of travel therefore the controller must retain this information. The controller simply changes the direction of travel of the operating point upon change of sign of P2-P1, while a memory retains the direction of travel and ensures that the operating point continues in the direction of the maximum power point until it is once again traversed. **Figure 91** shows

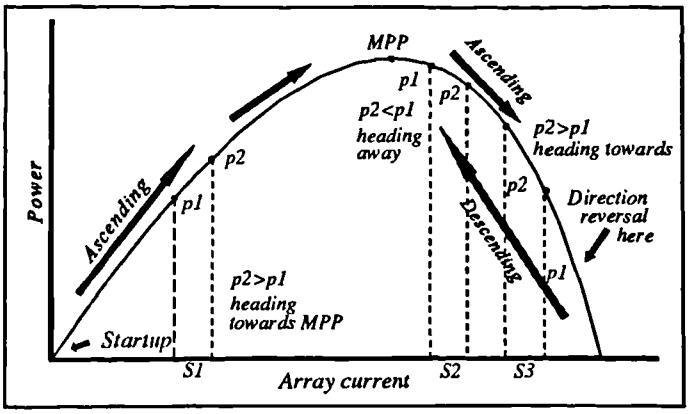

Figure 91 Mechanism of running sample maximum power tracker

this method graphically. The figure shows an exaggerated deviation from the maximum power point. S1 and S2 are sample point pairs taken as the operating point is ascending the curve, while S3 is a sample point pair taken during the period when the operating point is descending the curve. The result is that the operating point oscillates about the maximum power point, the amplitude of the oscillations depending upon the amount by which the operating point moves between power sample pairs.

3.9.5 Design of controller.

As with the dithering signal method, an integrator can provide the operating point variation as its output will ramp up for a positive input and down for a negative input. To implement this, the controller could take the form of the block diagram of **Figure 92**, with the timing shown in **Figure 93**. This is not dissimilar from the block diagram of the controller for the dithering method, the major difference being the absence of the dithering signal. The timing diagram shows two sets of sample points at the point at which the maximum power is traversed. The second power sample is taken at a fixed time after the first (usually an integral number of converter switching cycles) and the corresponding samples fed to a comparator which is used to detect the point at

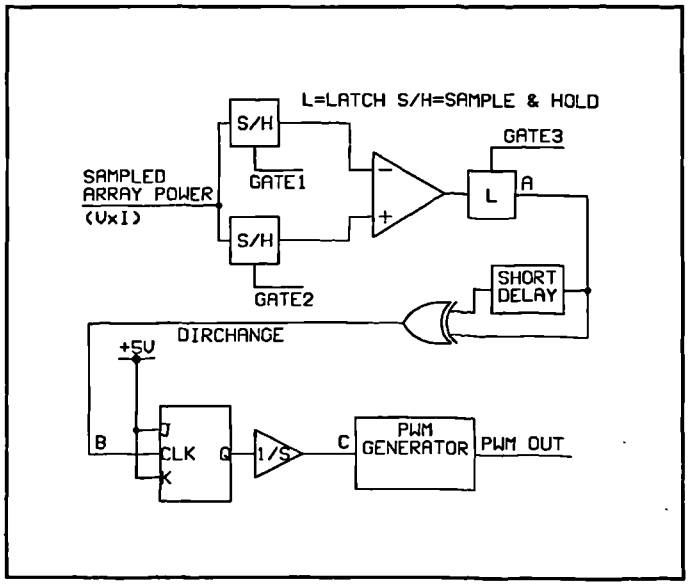

Figure 92 Maximum power controller block diagram.

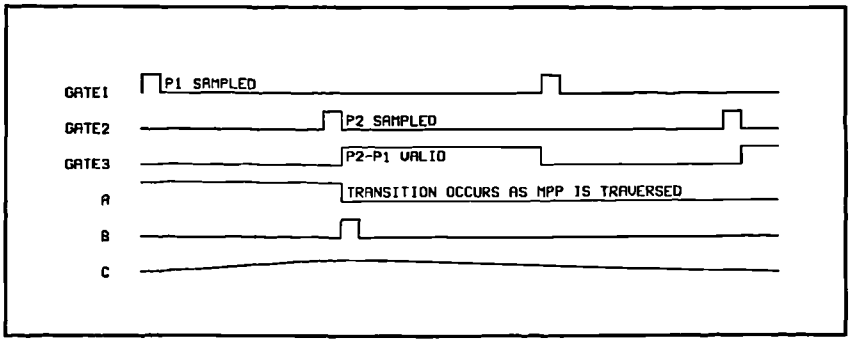

Figure 93 Timing for running sample implementation

which the difference between the two samples changes sign, corresponding to when the maximum power point is traversed. At this point a pulse is generated which toggles a bistable which forms the memory - the output of this changes state causing the integrator to change the direction of integration. This integrator provides the signal that the PWM controller converts into a pulse width. The net result is a pulse width that initially starts at zero and ramps upwards until the maximum power point is reached, whereupon the direction is reversed and the pulse width ramps down again. The next crossing of the maximum power point results in the integration direction changing again and this ensures that the operating point is always moving towards the maximum power point. The integrator time constant is very large, much larger than any of the time constants in the system but less than environmental time constants. The space between the two sample points can therefore be quite large.

3.9.5.1 Running-sample method without memory

The above method was arrived at after considerable experimentation with the sample-point methods. A memory is required to store the current direction of travel of the operating point on the power curve. An alternative method of providing this position infomation can be provided by the manner in which the array power is sampled. To arrive at a figure for the array power it is necessary to sample array current and voltage and multiply the two. The result is the presence of another two parameters in the system, namely array current and voltage and it is possible to usethe values of either of these parameters in addition to the power values to provide the positional information about the operating point relative to the maximum power point.

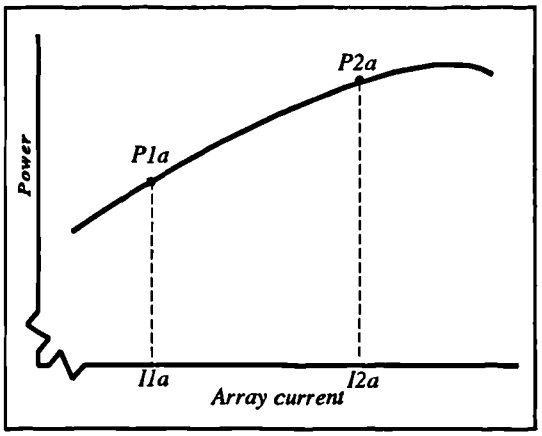

Figure 94 Sample points below MPP - operating point moving up curve.

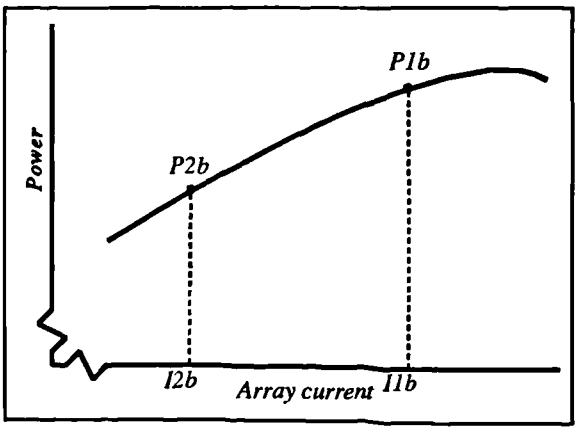

Figure 95 Sample points below MPP, operating point moving down curve.

Consider **Figure 94**. This shows a portion of an array power curve below the maximum power point with respect to array current with the two sample points, P1a and P2a taken at array currents I1a and I2a respectively, where the operating point is moving *up* the curve in the direction of increasing array current (sample distance exaggerated). **Figure 95** shows the same point on the curve with the same two sample points, with the operating point moving *down* the curve in the direction of decreasing array current. Likewise **Figure 96** shows a portion of an array power curve *above* the maximum power point with the two samples P1c and P2c, and the operating point moving up the curve in the direction of increasing array current, while **Figure 97** shows the sample points P1d and P2d above the maximum power point with the operating point moving down the curve in the direction of decreasing array current.

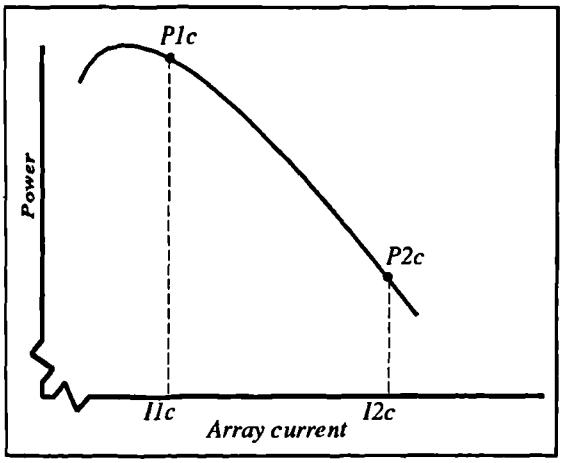

Figure 96 Sample points above MPP, operating point moving up curve

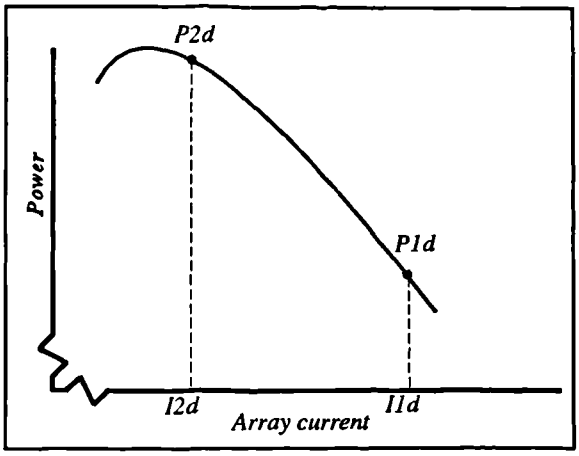

Figure 97 Sample points above MPP, operating point moving down curve.

It can be seen from these figures that the direction in which the operating point is moving may be obtained simply by taking the difference of the array currents at both the sample points as well as the powers. In the case of **Figure 94**, P2a-P1a is greater than zero, hence the operating point is moving towards the maximum power point. However I2a-I1a is also greater than zero, meaning that the operating point is travelling up the curve in the direction of increasing array voltage. The controller can then sense this and allow the operating point to continue moving in this direction. In the case of **Figure 95**, P2b-P1b is less than zero, indicating that the operating point is moving away from the maximum power point. However, I2b-I1b is also less than zero, indicating that the operating point is moving in the direction of decreasing voltage. The controller will thus cause the direction of motion to change.

In the case of **Figure 96**, P2c-P1c is less than zero, indicating that the operating point is moving away from the maximum power point. I2c-I1c is greater than zero, indicating to the controller that the direction of motion of the operating point is in the direction of increasing voltage, and would therefore cause the operating point to change direction of travel. In the case of **Figure 97**, P2d-P1d is greater than zero, indicating that the operating point is moving towards the maximum power point. I2d-I1d is less than zero, indicating that the direction of travel of the operating point is in the direction is in that of decreasing voltage and that the controller should not alter the direction of the operating point travel.

Since the shape of the curve of array power with respect to array current is similar to the shape of the curve of array power with respect to array voltage, there is no reason why the array voltage could not be used as the variable providing the information as to the direction in which the operating point is moving. In relation to the converter circuit of **Figure 34**, **Table 6** shows the desired variation of δ (the converter duty cycle) in order to intercept the maximum power point (either increasing, $\uparrow$ or decreasing, $\downarrow$) given the slope of the power curve at the sample points (given by P2-P1), and whether the difference between the array voltage samples at P2 and P1 (dV=V2-V1) and current samples (dI=I2-I1) is either negative or positive.

Table 6 Desired variation of δ with power, voltage and current.

	if below MPP	want	if above MPP	want
If P2-P1 > 0 (dP/dt +ve)	dV<0 dI>0	δ↑	dV>0 dI<0	δ↓
If P2-P1 < 0 (dP/dt -ve)	dV>0 dI<0	δ↑	dV<0 dI>0	δ↓

The sole purpose of this system is to use the samples of voltage or current to determine the current direction of travel of operating point and thus eliminate the need for a memory as required by the system described in section 3.14 - useful since the memory requires extra computation whereas the array voltage or current sensing is present by virtue of the requirement to sample array power.

3.9.6 Maximum power tracking using boost converter characteristics

Since for slope information it is necessary to have the converter operating point move, a new type of maximum power tracking controller was developed which rests on a characteristic of the boost converter - continuous input current with ripple, and this was one of the reasons for choosing this type of topology. In **Figure 34**, with a constant voltage source as input and the inductor value chosen for continuous inductor current it can be seen that the source current is the same as the inductor current and that the shape of this current consists of triangular ripple superimposed upon the nominal d.c. current. Such a signal makes an ideal dithering signal when the source is replaced by the photovoltaic array. The source voltage is not now constant with source current and the ramp will no longer be linear but this will not reduce the value of the dither signal. **Figure 98** shows the technique. The two-sample point method is still used to sample the array power and calculate dP_{out}/di, but now, since the direction of the operating point along the power curve during the dither is now fixed by the action of the inductor (in the direction of increasing current) only the difference between the two powers is required to determine the slope

of the power curve. This reduces the amount of computation over that required by other methods that need to sense the direction of movement of the maximum power point - or to use a memory. The two sampled values contain all the information required by a maximum power tracking controller to calculate dP_{out}/di. (from P2-P1) The basic controller is the same as **Figure 77** but the summing amplifier is removed along with the external dithering generator, and the samples are timed to coincide with the switch on-time: one just after the switch turns on and one just before the switch turns off.

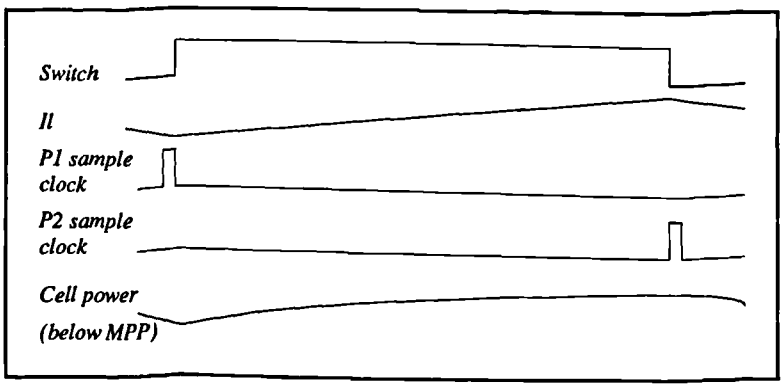

Figure 98 Technique for maximum power tracking using boost converter input current waveform.

Owing to the very slow speed of the changes in the environmental variables, it is not necessary to perform this sampling at every switching cycle. The sampling could be performed an integral number of switching cycles apart, with the new value of duty cycle being calculated and held for that number of cycles. There is ample time, therefore, for a microprocessor to calculate the new values of duty cycle and this obviates the need for an extremely fast microprocessor if maximum power tracking is the only task that it has to perform. For example the sampling could be organized with 10 switching cycles between each sample pair. The computational element would not necessarily have to complete the calculation within a single switching cycle.

Figure 99 shows in more detail the operation , at and below the maximum power point. Note that with this system as with the others, the average power throughput will be slightly below maximum power, this being due to the deviation of the operating point introduced by the ramp in I_L. The proximity of the average power to maximum power is given by the height of the ramp waveform of the inductor current, which is governed by the inductor value. If the inductor is increased in value the ramp height will be reduced, and the average power throughput will be

brought closer to maximum power: however the upper limit is brought about by both the physical size of the inductor together with the resolution of the system used for sampling the start and end values of the inductor current during the on-time (a much smaller ramp will demand high resolution).

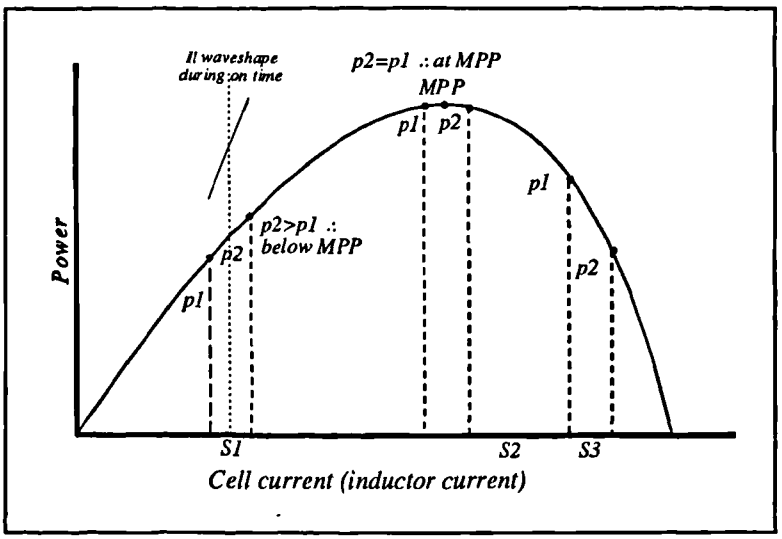

Figure 99 Operation of maximum power tracker using boost converter input characteristics.

3.9.6.1 Implementation

Figure 100 shows the block diagram of the system while **Figure 101** shows the associated sample timing. As can be seen from the block diagram, this approach is by far the simplest. The memory required by the running-sample methods is no longer required, neither is the summing amplifier and the dithering signal generator used by the dithering-signal methods. In a digital implementation, the reduced complexity of the system results in reduced demands upon the controlling microprocessor and this could be arranged to release processor time for other functions. It is not necessary to use specifically a boost converter if the transfer characteristics of

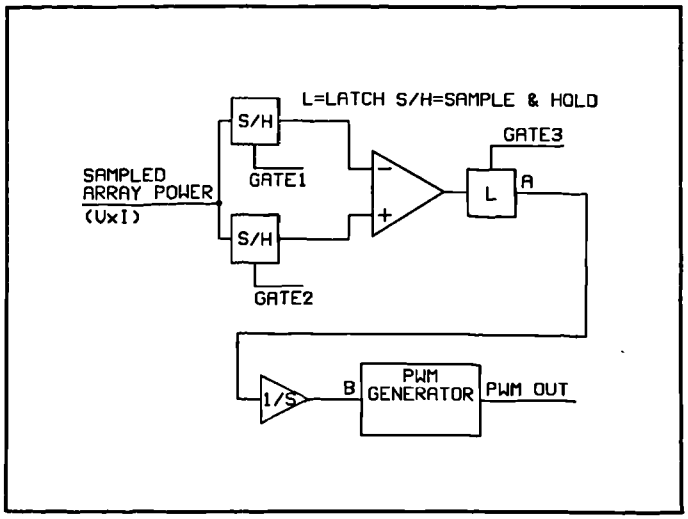

Figure 100 Block diagram of maximum power tracker using boost converter characteristic dithering signal.

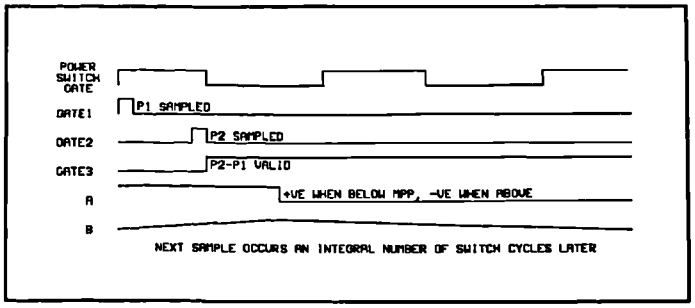

Figure 101 Timing for **Figure 100**

the boost converter are not required, but any converter that is used must have an input current characteristic consisting of continuous current with a ramp superimposed on it of sufficient amplitude not to cause the sampling A-D converter to run out of resolution. The current ramp need not be linear - indeed it will not be owing to the nonlinear characteristic of the array.

3.9.6.2 Implementation of simulation model.

The simulation model was again implemented as for the other algorithms, with the control algorithm embedded in a single template. The schematic is shown in **Figure 102.**

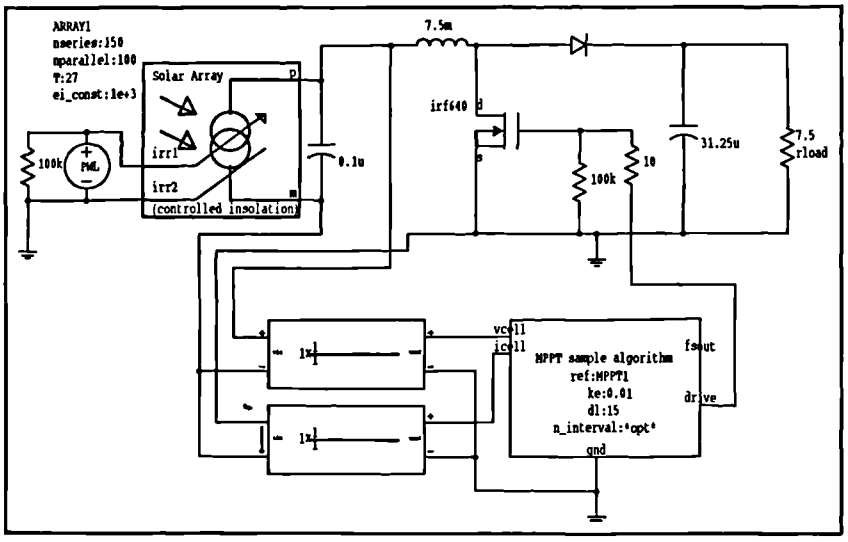

Figure 102 Schematic of maximum power tracker based on boost converter characteristic.

The template 'MPPT sample algorithm' in **Figure 102** embodies proportional integration as part of the algorithm, a listing of which is given in Appendix B. The template samples power at the start and the end of the switch on-time once every 'n_interval' cycles, where 'n_interval' is the number of cycles at the PWM frequency between each on-time where sampling occurs. The duty cycle value is updated only after each sampling - therefore the true integrator time constant is dependent upon both 'n_interval' and 'ke', the integrator δ step. As with the other proportional integration systems, there is both an upper and lower limit placed upon the size of the integration

step - the upper limit to prevent overflow in the computational element, while the lower limit prevents asymptotic approach to maximum power.

3.9.6.3 Operation of simulation model of boost converter method

The irradiance profile of **Figure 80** was used in a simulation run where the integrator constant ke was set to 0.001 and the sample interval to 8 cycles. The result, a power and insolation curve versus time is given in **Figure 103** where extremely good tracking, even of the discontinuities in the waveform, may be seen. Fast acquisition (seen by the startup curve during the first 18ms of the plot) is combined with excellent tracking. Pulling the integrator constant low (to 0.0001) gives rise to the power curve taking on the form of **Figure 104**, where it can be seen that the only result is that the acquisition and tracking is slowed down. For a slower irradiance profile the response would be adequate, and obviously for the type of profiles found in nature (slower with no discontinuities) a much slower integrator could be used. Speeding up the integrator, however, does not result in such dramatic effects upon the power curve as with the dither and running-sample methods. The plot of **Figure 105** shows the power curve for a system where the integrator constant has been increased tenfold over the nominal value. The only obvious difference in the power curve is during the startup portion where there is a level of transient behaviour - this is due to the integrator increasing Δ rapidly in response to the effective step input, overshooting maximum power and oscillating about the maximum power point. This is visible on the characteristic of load current and voltage (**Figure 106**) as decaying oscillations. To effect a realistic comparison, the load I/V curves are shown in **Figure 107** for the nominal integrator time constant. As can be seen there is no 'ringing' displayed in **Figure 107** and, apart from the switching ripple, the profile is clean.

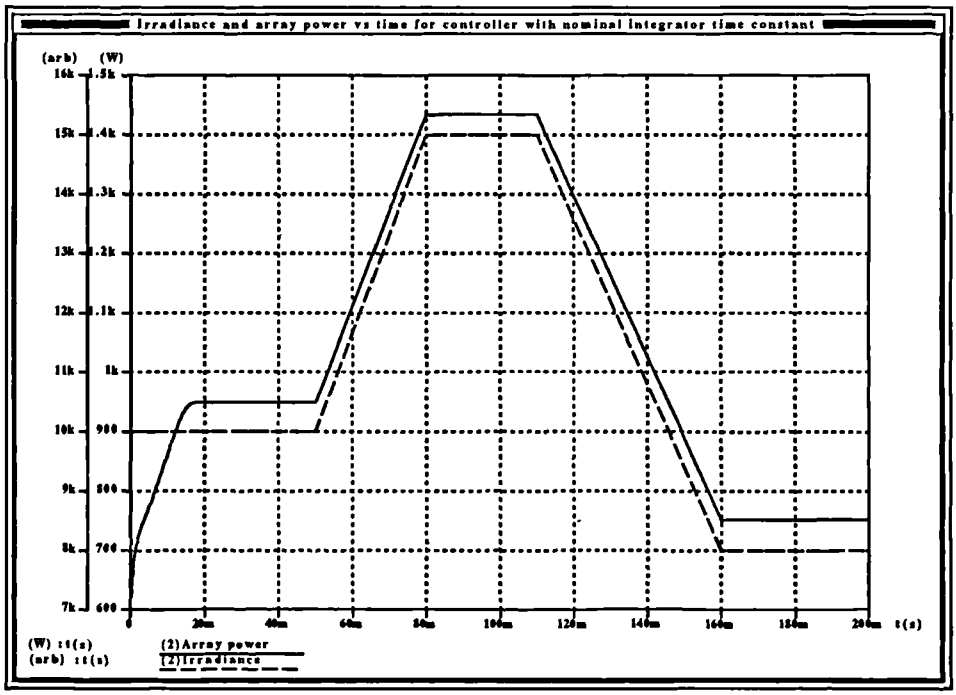

Figure 103 Power and irradiance curve using nominal integrator time constant for boost converter method..

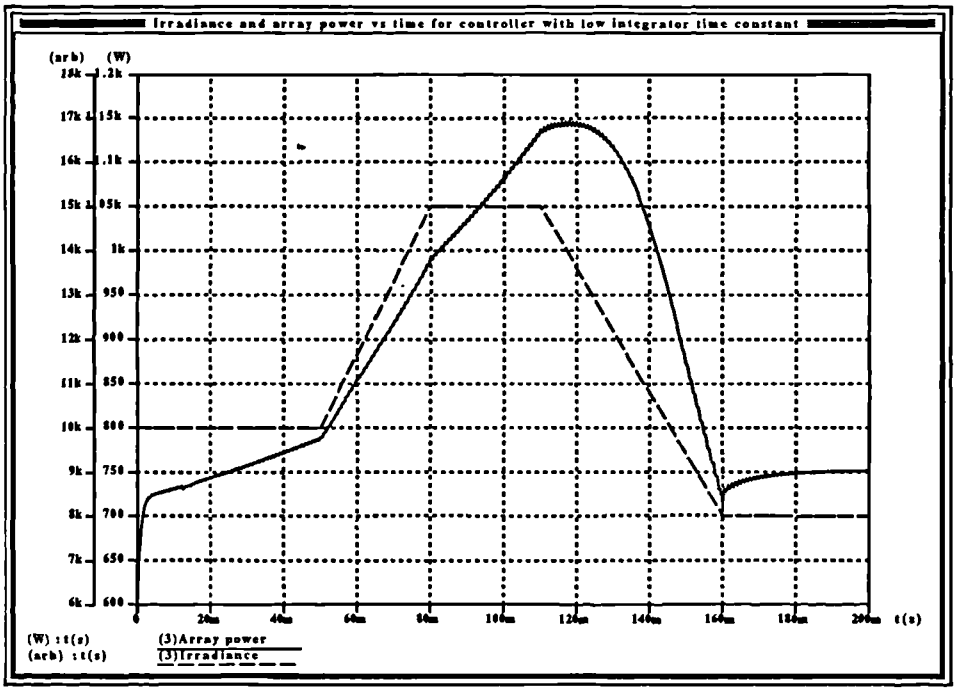

Figure 104 Power and irradiance curves using lower than normal integrator constant.

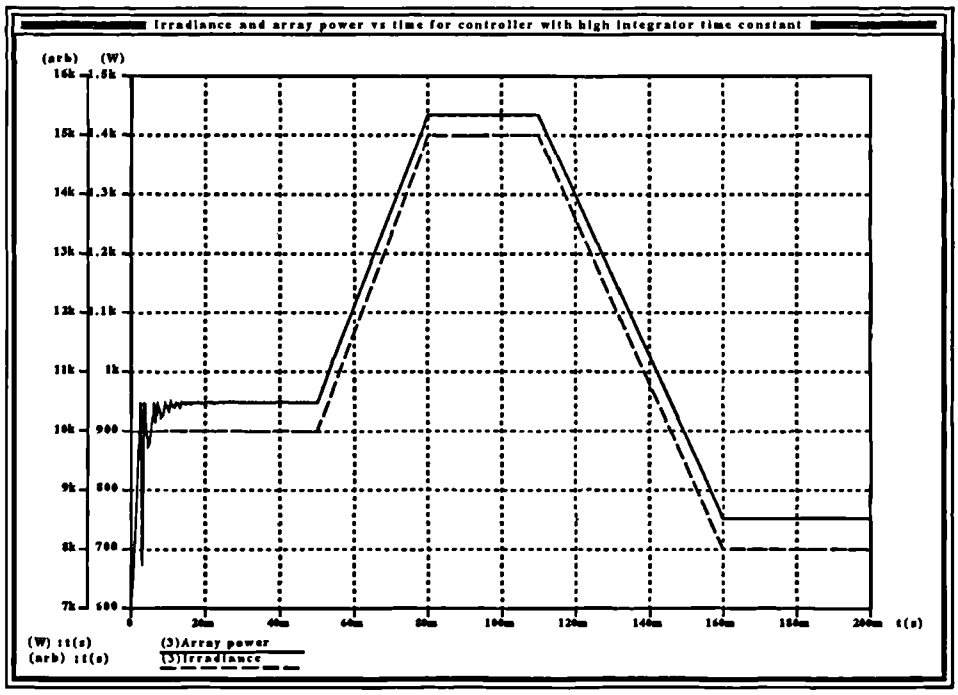

Figure 105 Power and insolation curve using high integration constant (0.01).

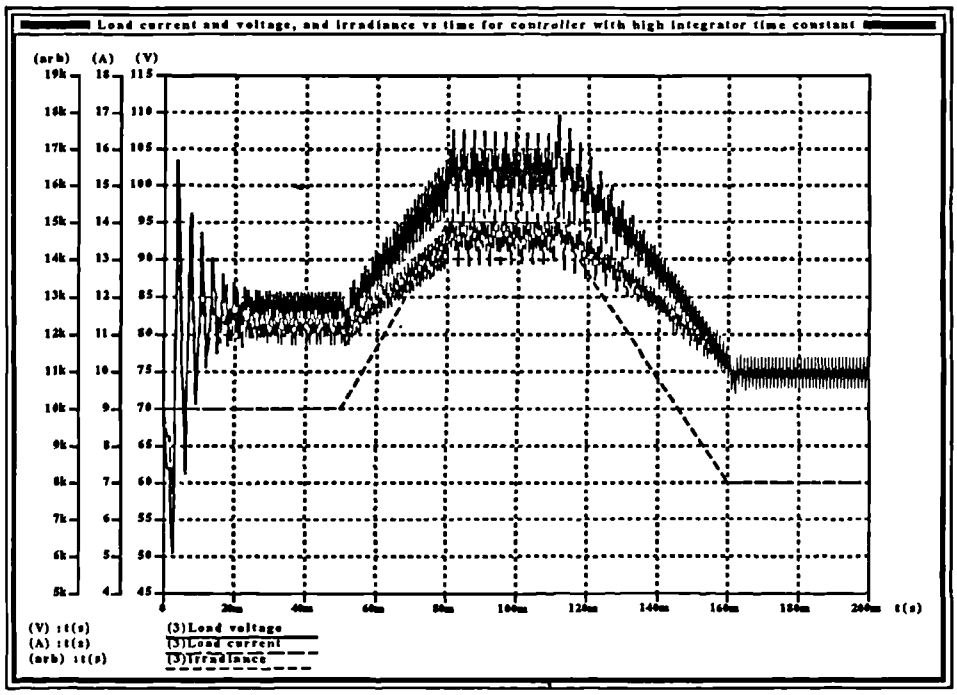

Figure 106 Load current and voltage curve for boost converter method with high integrator time constant.

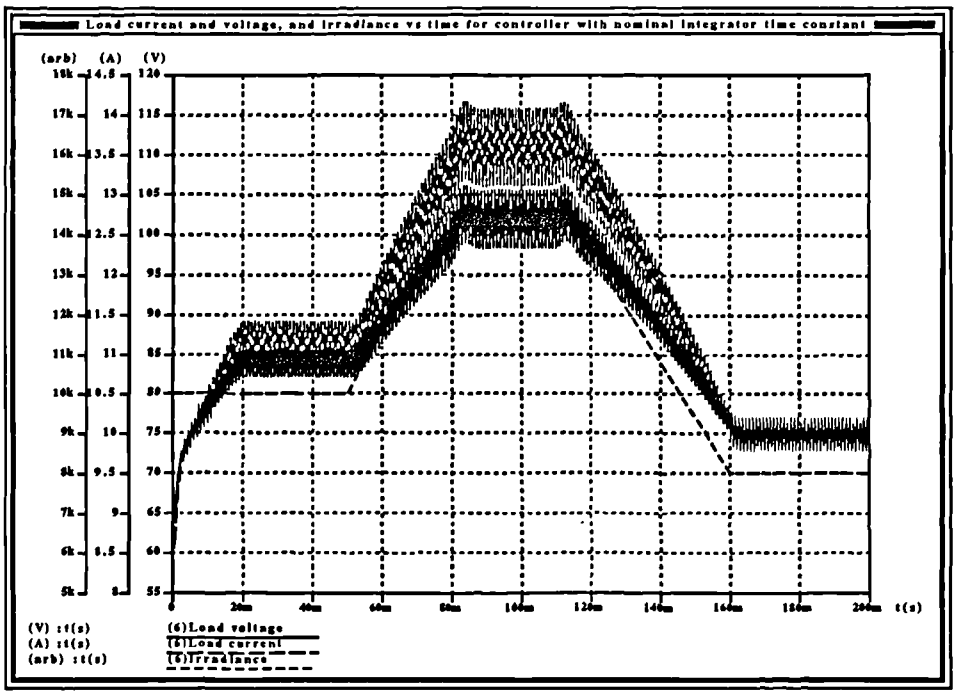

Figure 107 Load current and voltage profiles using nominal integrator time constant.

This system will track much slower movement of maximum power points and it appears that it is much less sensitive to changes in the integrator time constant. It makes an extremely good maximum power tracker.

3.10 Comparison of available maximum power tracking algorithms.

Of all the algorithms investigated, the boost converter characteristic method stands out as being by far the most insensitive to parameter values (ke, sample interval) and also seems to provide the best tracking. The dither-signal methods come a close second but could be quite sensitive to values of ke, and quite a large amount of time was spent actually getting the algorithm to track properly. Running sample methods have been implemented quite successfully in the analog domain, but again it was found quite difficult to implement a working simulation model of the system. Proportional integration makes quite a significant difference to fixed-integration algorithms and is clearly worth the very little extra computation that is necessary to implement

it. Given the simplicity of implementation of the algorithm in the digital domain, for converters with a continuous input current with ripple the converter-based algorithm would be the first choice.

3.11 Current mode control with embedded maximum power tracking

The elementary form of maximum power tracking provided by reversing the sign of the compensator gain as described in section 3.8.4 is similar to the running-sample methods described in section 3.9.4. The method relying on boost converter characteristics is superior and to gain the maximum benefit from both algorithms the boost converter method of maximum power tracking is used to provide the necessary maximum power tracking requirement of the complete converter control system.

3.11.1 Composite controller with embedded MPP, the operation.

The implementation of the controller can be seen in **Figure 108**. The conditions for the operation of the switch between PI and maximum power are also shown in **Figure 108** in pseudocode form. The final result is a system which operates conventionally up to the point where either the load or the controller demands a power from the PV array greater than maximum power for the given conditions. The converter will then switch to a maximum power algorithm until the demand is reduced. The result is that not only are such aspects of operation such as the rise time upon power-up and load changes improved over the PI-only system, but also loads less than array maximum power will be supplied with a fixed output voltage. Once the load rises above that which will draw maximum power at the fixed rail voltage, the rail voltage will fall in such a manner as to maintain maximum power into the load. Regulated rail voltage will be restored with an acceptable transient response once the load is shed. Unnecessary operation in the constant current region is prevented and the transient response is maintained. Maximum power loads do not use the PI controller, and thus there is no small-signal stability penalty associated with the lower load resistance values.

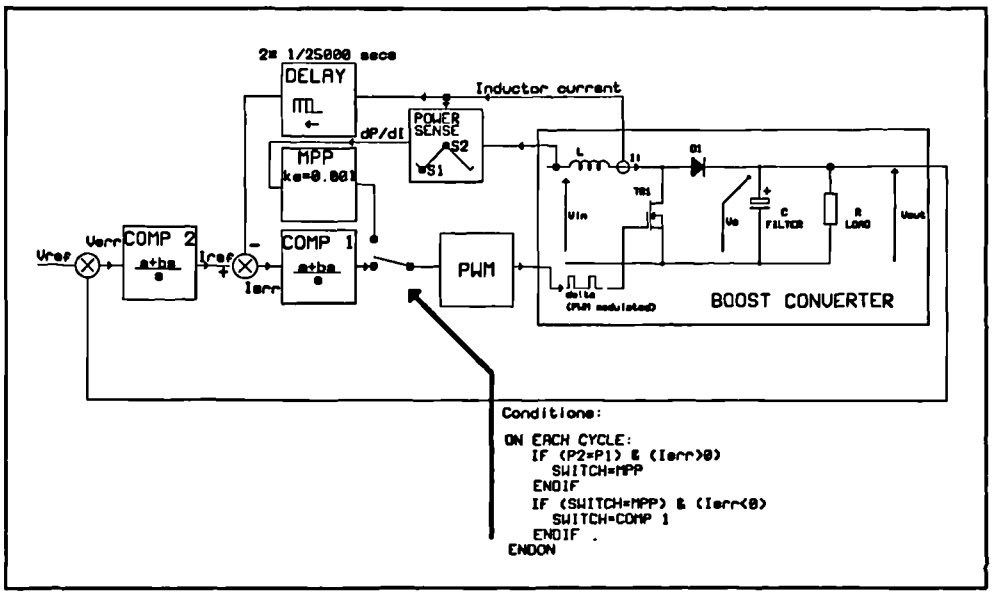

Figure 108 Implementation of controller algorithm.

3.11.2 Conditions for operation of the MPP/PI switch.

The conditions for the operation of the switch between the two modes of control are quite critical to the smooth and effective operation of the system as a whole. The condition for initiation of MPP operation is clear and has already been laid down as being the point at which the operation of the PI controller causes the power demand from the array to pass the maximum power point. This is easy to sense from dP_{array}/dI. However, the termination conditions are not so clear cut and to some degree are dependent upon transient conditions.

The first of the termination conditions will occur when the power demand from the array starts to drop below maximum power - that is when the value of the current demand signal input to the current loop drops to a point where it becomes equal to the actual sensed current flowing in the diode during MPP operation. When the MPP system is operational, unless the conditions of converter operation demand exactly maximum power from the array when the current error will be zero, the demanded current (output of the voltage loop compensator) will exceed the measured diode current. As the converter operating conditions change (for example it sheds its load) and the current demand drops, the PI controller may take over from the MPP controller

when the current demand value drops below the measured average diode current at maximum power, at this point operation will resume in the constant voltage region of array operation under PI control.

The second termination condition is largely due to transient behaviour, and is intended to speed up recovery after load changes. Depending upon the speed of the voltage loop (the output of which provides the current demand signal) it is possible for an undesirable condition to occur when a maximum power load is shed. A maximum power load is one which causes the converter to operate continually in the maximum power mode, the load is such that under the current environmental conditions (or even operating conditions in the case of drive to a grid-connected inverter) the array is unable to provide sufficient power for the converter to sustain the desired d.c. rail voltage as it would for lower loads. At the point of shedding such a load, the current demand will still be high as it is very likely that the voltage loop PI controller will have integrated up to its upper limit. At this instant, the maximum power tracker will still be operating as the current demand will take time to reduce. Now, if the load change was considerable, i.e. from a maximum power load to a very light load, the rise in converter output voltage will be rapid. If this rise is allowed to continue unchecked, it could result in considerable overshoot of the nominal d.c. output voltage before the current demand signal (output of the voltage loop) falls to the maximum power current and meets the first termination condition.

To prevent this behaviour a further termination condition is added: to revert to PI operation if the output voltage rises above the nominal. If the output voltage does rise above nominal then there is no requirement for maximum power operation as the load will not be drawing maximum power at nominal rail voltage.

These combined conditions are described below in **Table 7** in pseudocode form, from which they can be easily implemented both in MAST for simulation purposes, and also directly in code to run in the DSP controller used in the practical system. As stated earlier, it is also necessary to ensure that the integrator states are modified over the transitions between MPP and

PI and vice-versa, in order to prevent any discontinuities or glitches in the time response of the system during large load excursions and/or excursions of array environmental variables.

Table 7 Conditions for MPP/PI transition.

```
IF mpp_active == FALSE
        IF dP/dI<0
                mpp_active == FALSE
        ENDIF
ELSE
        IF (V_out >= V_nominal) OR (I_demand <= I_maxpwr)
                mpp_active == TRUE
        ENDIF
ENDIF
```

3.11.3 Saber simulation of the complete controller.

The controller of **Figure 109** was then implemented in the MAST modelling language to enable simulation of the complete system. The full listing of the template may be found in Appendix B.

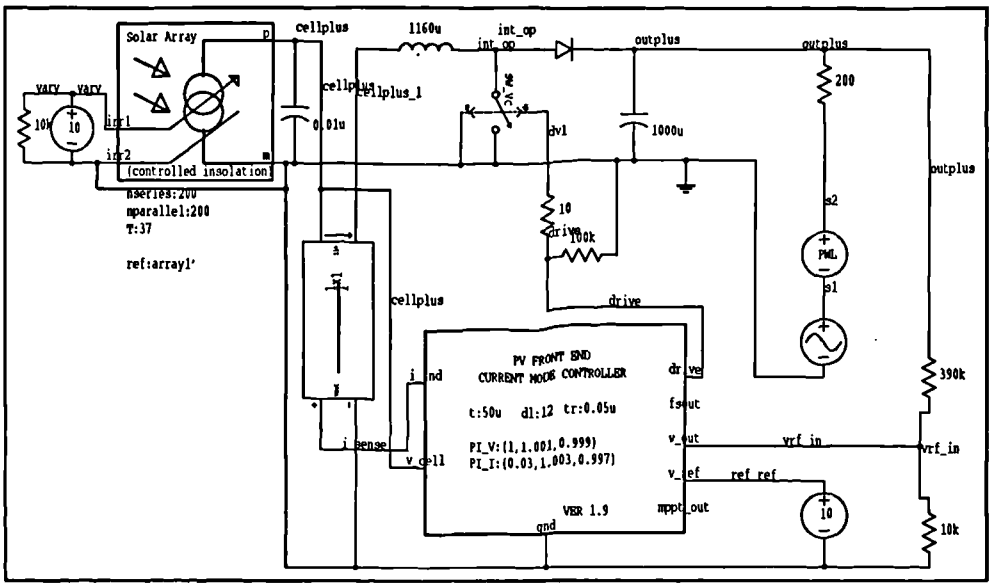

Figure 109 Schematic of simulation model of full MPP/PI controller.

The array size was restored to 200x200 as in section 3.8.1 to implement the same conditions as for the simulations run with the PI-only controller so as to allow a comparison to be made between the controller with embedded maximum power tracking and the PI-only controller. The maximum power tracker itself has been tested independently and is known to perform well.

A number of simulations were run and these are listed below in the order that they were run. For these simulation runs, each of which used the last one as its initial point to save simulation time involved in running the converter from startup, the following sets of plots were generated: output voltage vs time, input (array) current vs time, array power vs time and load power vs time. To avoid generation of large plot files and data files the results were sampled, not every point at every timestep was plotted so unimportant detail such as the switching ripple has been lost. A cross-reference between load types and presented figure numbers is given below:

1: Starting transient: from 0 to 130ms.

Output voltage:	**Figure 110**
Inductor current:	**Figure 111**
Array power:	**Figure 112**
Load power:	**Figure 113**

2: Transient response given load changes:

130ms: 200Ω-1000Ω

170ms: 1000Ω-100Ω

210ms: 100Ω-1000Ω

250ms: 1000Ω-100Ω

Output voltages:	**Figure 114**
Inductor current:	**Figure 115**
Array power:	**Figure 116**
Output power:	**Figure 117**

3: Response to 50Hz sinusoidal load change between 1000Ω and 100Ω effective load.

Output voltage:	**Figure 118**
Inductor current:	**Figure 119**
Array power:	**Figure 120**
Output power:	**Figure 121**

Due to an oversight the load change 100Ω-80Ω was omitted from this test, however these particular values are not critical to the presentation of the overall performance of the converter.

All of these show acceptable behaviour for use with either a fixed d.c. load or an inverter feeding a live load. The advantages of the embedded maximum power tracker is clear in the curve of output voltage during startup (compare **Figure 110** with **Figure 54**), the small glitch at 45ms is the point at which control reverts to the PI controller. This glitch is very small and caused by the presetting of the PI integrator state prior to transferring control from the maximum power system to the PI system - it is small enough to be of no concern. The array power curve of **Figure 112** shows the action of the maximum power tracker - the system is running at array maximum power between 25ms and 45ms, after which the switch to PI operation is clearly visible.

In the load change curves, the output voltage shows some oscillation at the point of transition between the 1000Ω and 100Ω loads, noticeable mostly in **Figure 115** and **Figure 116**. These occur only on the rising edge of the inductor current waveform, not on the falling edge. The exponential rise of the voltage waveform across the same period in **Figure 114** together with the exponentially-decaying shape of the oscillations in the inductor current waveform seem to suggest that the oscillation is in the current loop. However, the oscillations only occur upon transition to a heavy load; the curve when the heavy load is shed shows a small overshoot (0.5% of nominal rail voltage) and recovery consistent with correct operation of the controller. This is surprising in the light of equation (**51**), where the 1/R in the single s term in the quadratic denominator of the δ to diode current transfer function seems to suggest that damping will increase as load decreases. The oscillation is at about 500Hz (5 cycles across 10ms), or 3141rads

s^{-1}. The Bode plot of the compensated current loop (**Figure 45**) shows a phase response which rolls of quickly after the -180° point while the gain response flattens out. The oscillations die away quite quickly, so the system appears to be oscillatory, but not unstable and the narrow phase margin of the current loop may have some bearing on this. The absence of oscillation on the edge into the light load is unusual, however. A final possiblity as to the cause is an internal error in the simulator, possibly truncation of the controller variables and coefficients, or a problem with the time-step. The oscillations are quite small, however, the magnitude of the tallest spike is about 3V, 0.7% of rail voltage which is quite small, and the oscillations die away within 10ms.

The sinusoidal load results show no aberrations of any real concern, and the nominal 400V rail voltage is maintained to within 0.68%, which is quite acceptable.

The simulation model shows that the system is worth implementing in hardware in order that it may be investigated further.

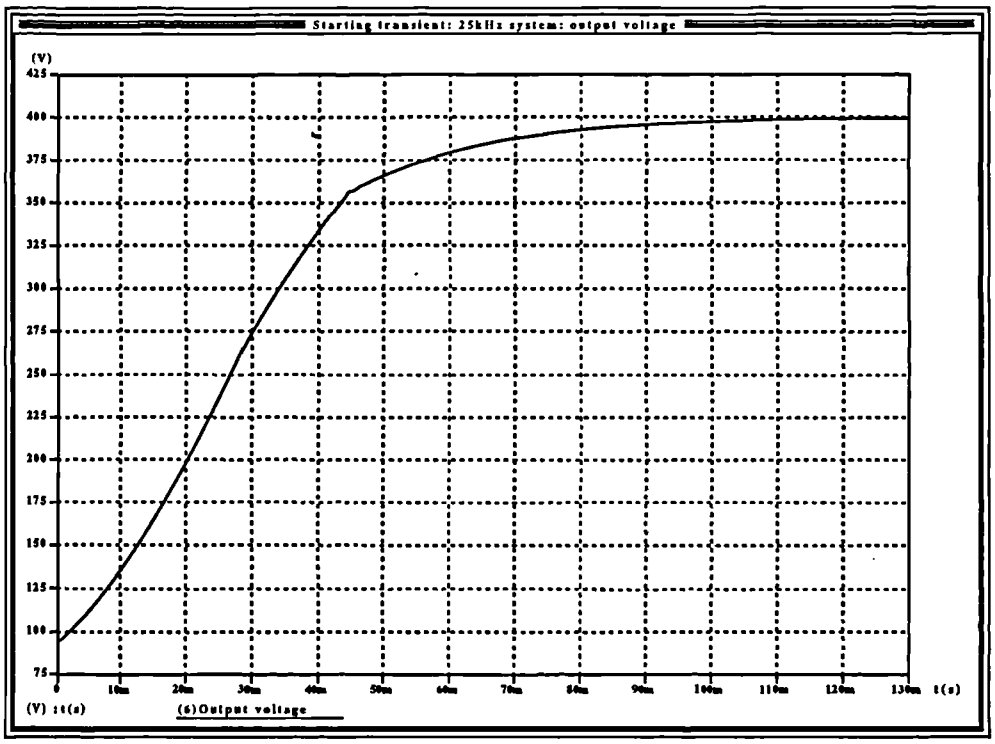

Figure 110 Starting transient: output voltage.

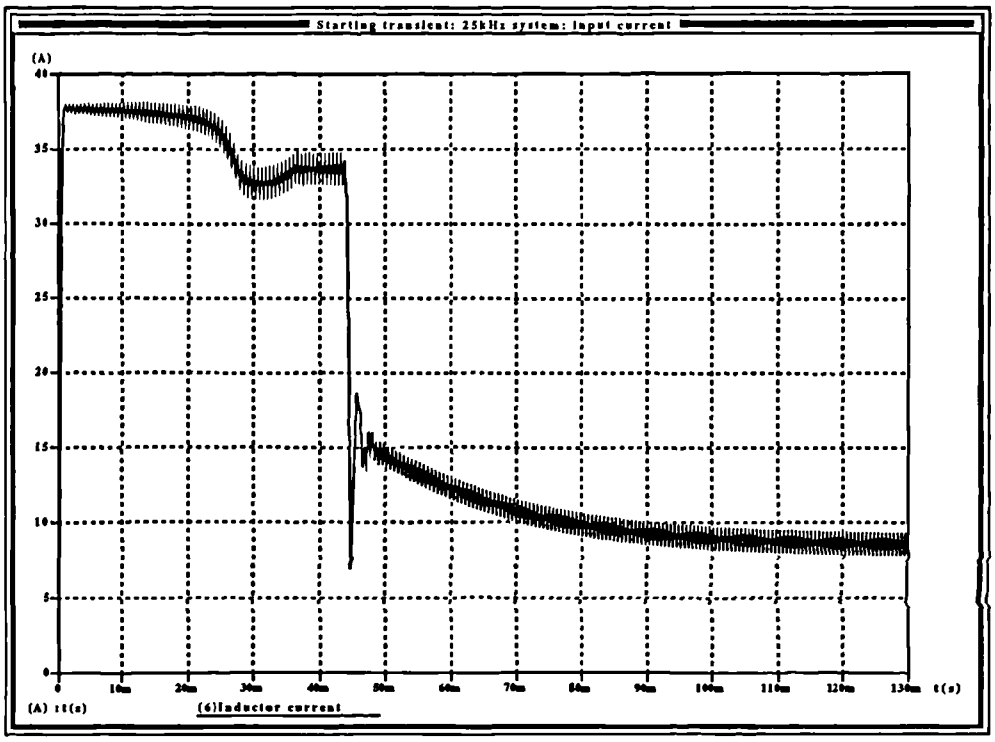

Figure 111 Starting transient: inductor current

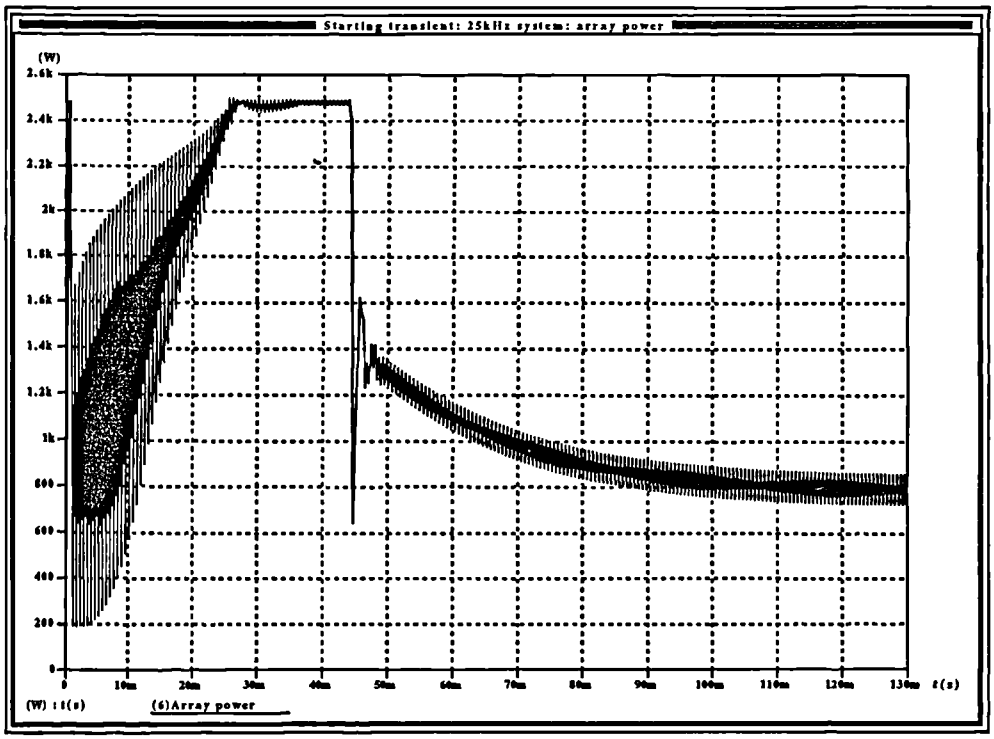

Figure 112 Starting transient: array power.

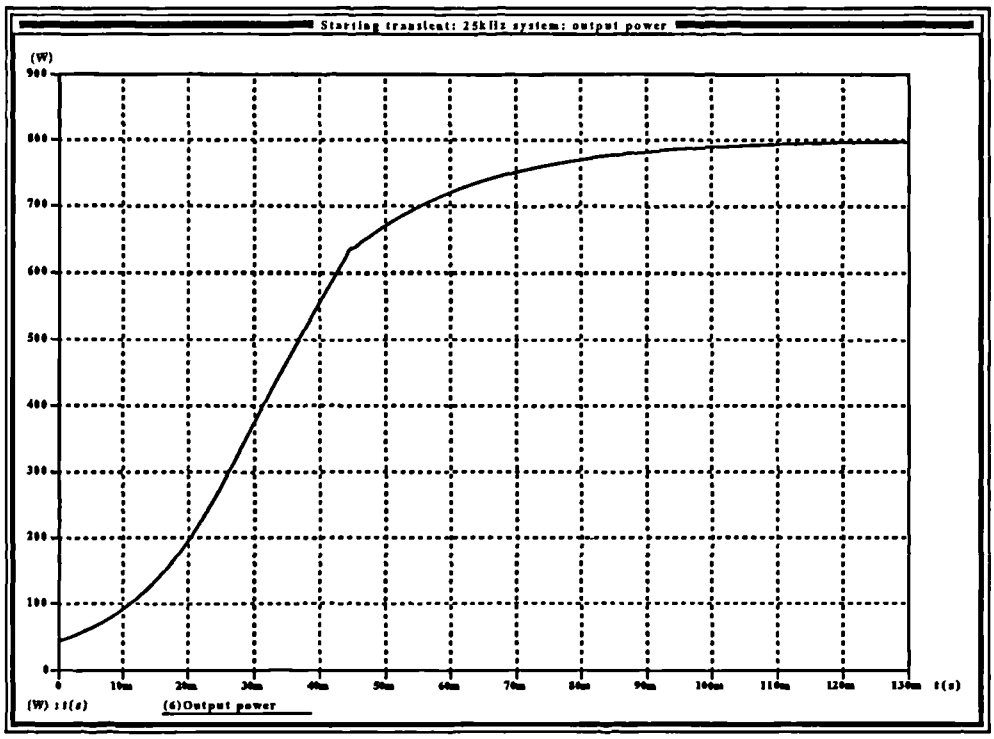

Figure 113 Starting transient: load power.

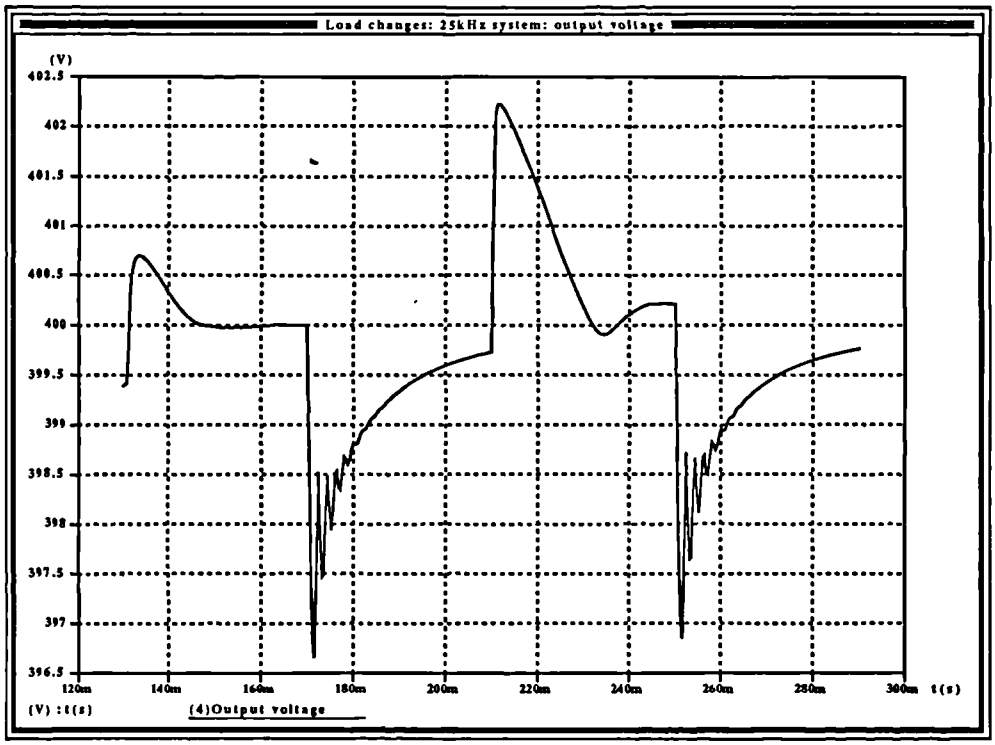

Figure 114 Load changes: output voltages.

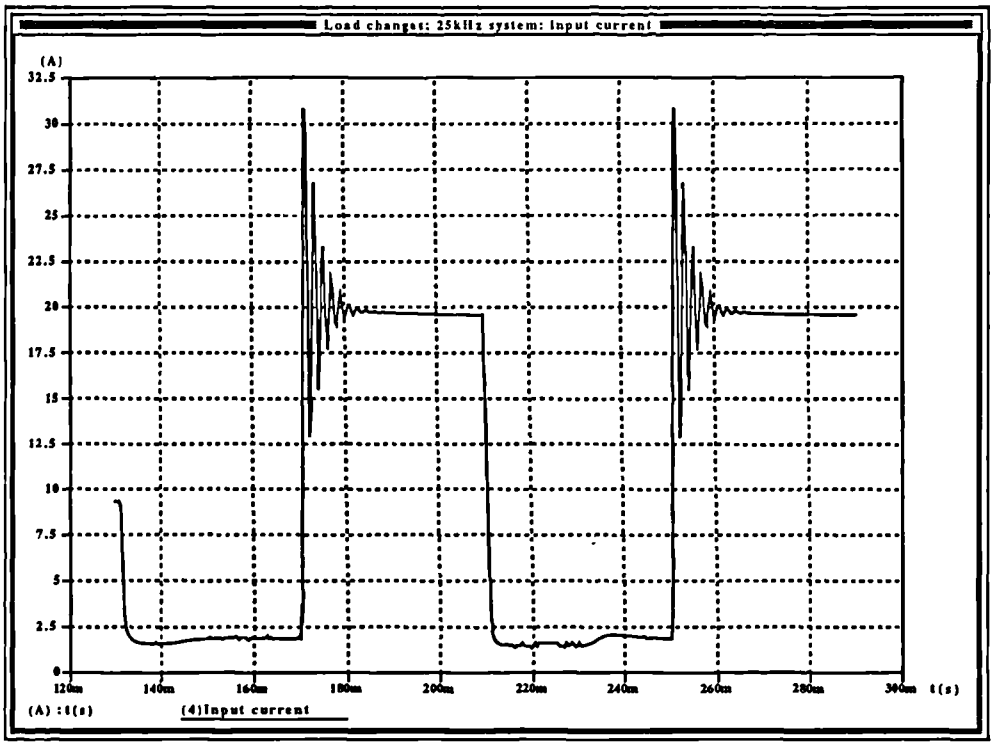

Figure 115 Load changes: inductor current.

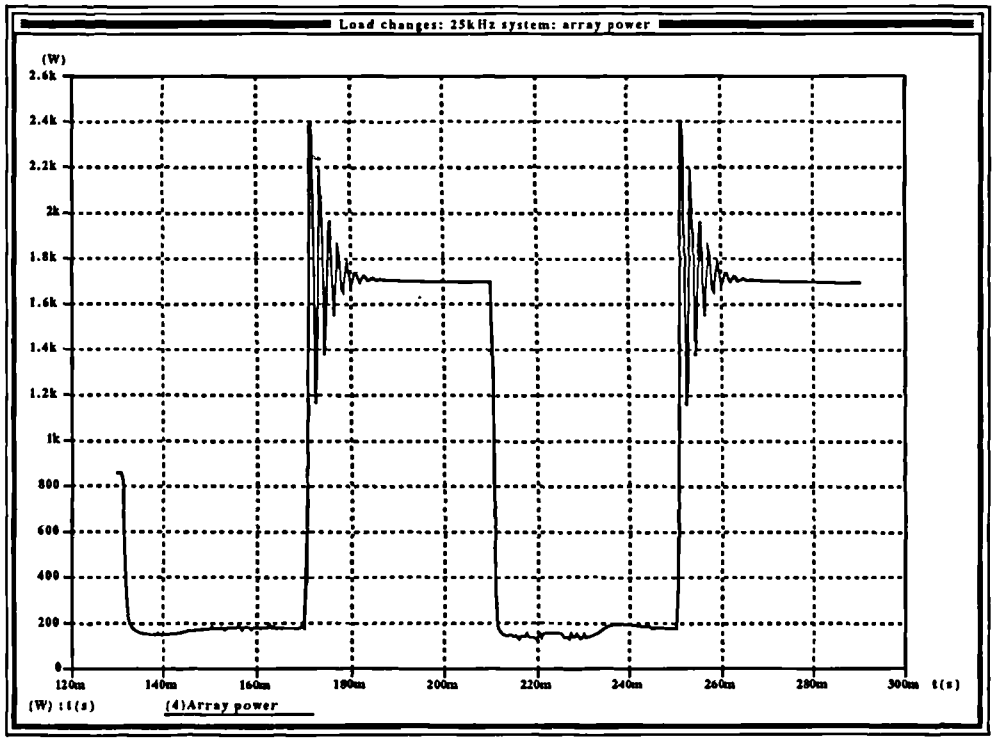

Figure 116 Load changes: array power

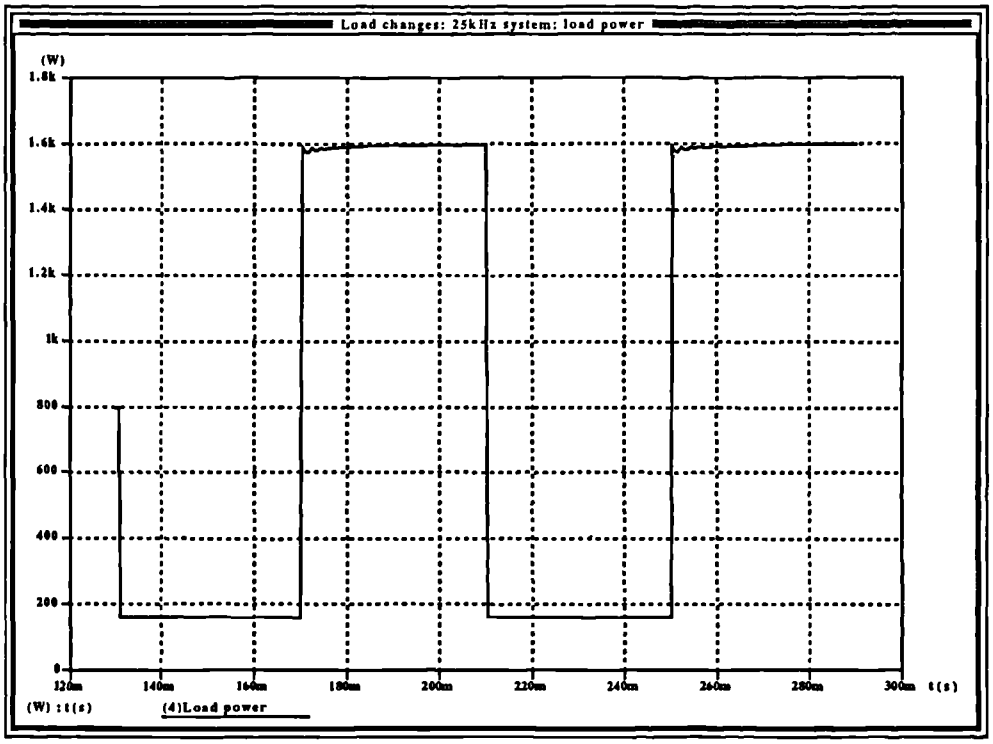

Figure 117 Load changes: output power.

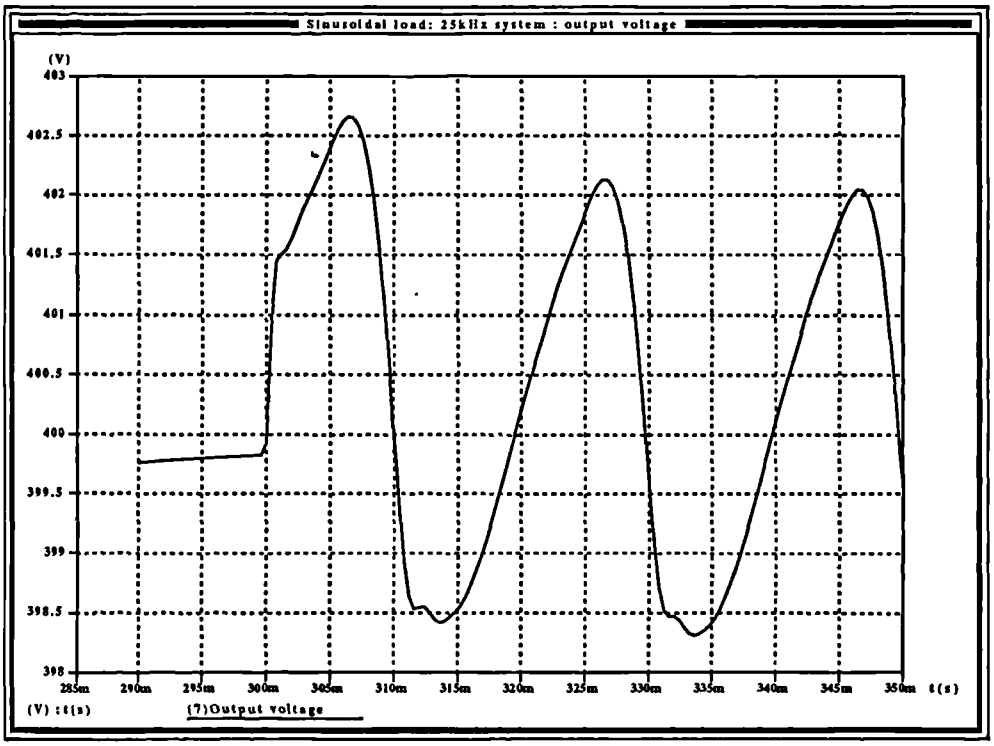

Figure 118 Sinusoidal load: output voltage.

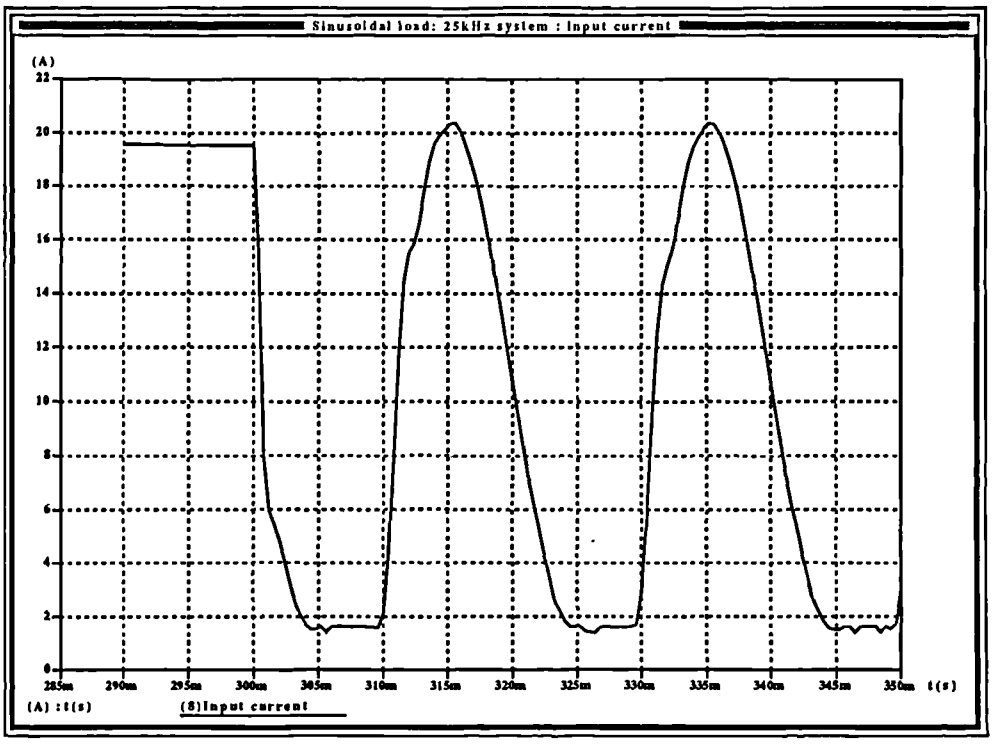

Figure 119 Sinusoidal load: inductor current.

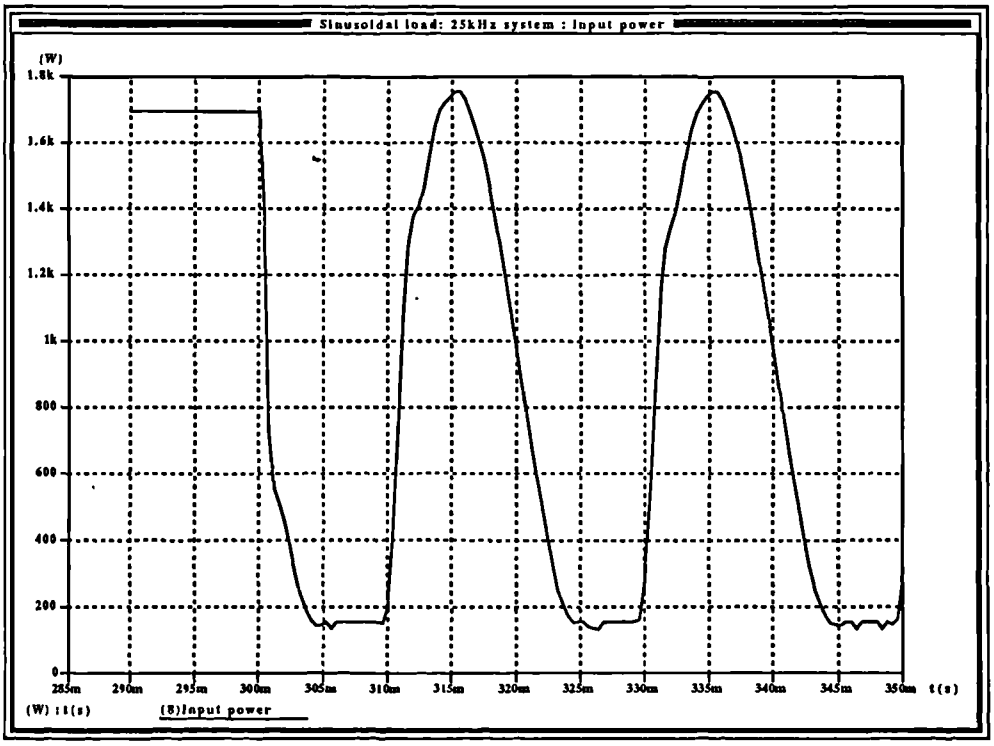

Figure 120 Sinusoidal load: array power.

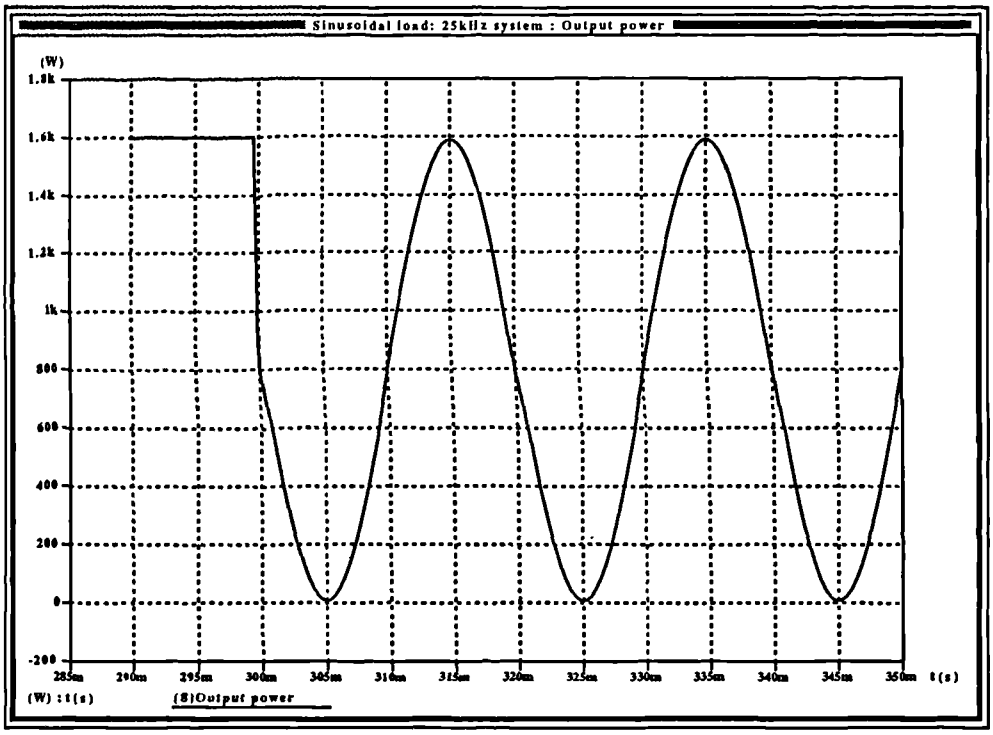

Figure 121 Sinusoidal load: output power.

3.12 Practical implementation of the system.

In the light of the expense of large scale photovoltaic arrays, as well as the amount of space required for them, it was decided initially to demonstrate the viability of the system by developing a low-power prototype which would embody all the operating characteristics of the full power version and use the same controller (with the signal-conditioning systems modified to suit the measurement of lower values). Two arrays were purchased, both of them supplied by Maplin Professional Supplies Limited [24]. Each array consists of two series chains of cells, delivering a nominal 6V at 250mA. These chains may be connected to deliver either 6V at 1A, or 12V at 500mA (or greater) with each array illuminated by 500W halogen floods of the type used during the development of the array characterization system. This will drive an inverter topologically identical to that of the proposed high power version, with the same inductance and capacitance values. Some modification will have to be made to the controller constants as with the lower voltages, the load resistances will be higher thus reducing damping and requiring

'stiffer' compensation to prevent oscillation. However, the operation of the small-scale system will certainly be sufficient to determine whether a large-scale 1-2.5kW implementation of this system in its present form will be successful.

Such a low power implementation will be sufficient to test the control algorithms and prove their validity. If high power arrays were available, it would be difficult to use them to establish the correct operation of the converter as the tests could only be run under solar illumiantion, which is variant and would not provide a fixed and known reference characteristic across the duration of the tests upon the converter. Once the correct operation of the algorithm is established at low power with an actual PV array, the high-power prototype can be implemented and tested using a simple, known maximum power source provided for by resistances in series with a voltage source.

SECTION 4: A practical implementation of a low-power boost converter

The preliminary boost converter front-end design consists of three subsystems. A block diagram of the design may be seen in **Figure 122.** The first of these is the power circuit containing the switching elements and energy storage passive components. The second subsystem is a signal conditioning, ADC and logic block which can both generate the necessary PWM drive signals, and also generate the timing to drive the ADC. The final subsystem, the computational element, consists of a Texas Instruments TMS320C50 DSP device. Its availability on a single card with the device bus brought out to header plugs, complete with an internal boot ROM allowing code to be downloaded from a PC greatly speeded the interfacing of the system to the device.

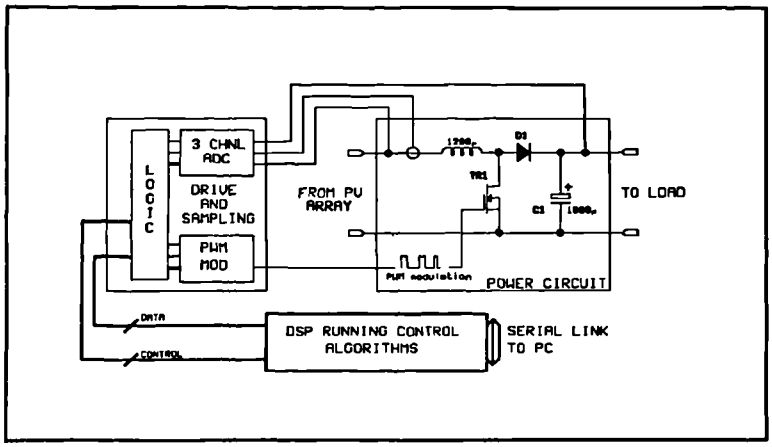

Figure 122 Block diagram of PV boost converter based front-end.

The above system emerged as a result of a decision made early on during the development of the project that the controller of the power electronics should be implemented digitally. This offers a number of advantages over an analog controller, particularly in the area of post-development modification where control algorithms may be modified or even completely rearranged simply by changing the software. The simulation models were developed to mimic the structure of a digital control scheme in order to facilitate direct transfer of the algorithms to the code required by a computational element such as a DSP. This design methodology certainly paid off, and the DSP implementation of the algorithm retained the structure of the MAST simulation

template to a significant level, thus providing a direct path between the simulation and the hardware.

It was further decided to develop a low power version of the system in order to verify the operation of the controller. There is nothing new about the boost converter, but the control algorithms have been tested only in simulation and it was felt to be prudent to test them in a practical sense in a fashion where any failures of the algorithm are unlikely to result in component breakdown. The use of a low-power system as an initial test bed in no way compromises the operation of the controller, and indeed it is possible to use precisely the same DSP, ADC subsystem and control logic to drive a power chain operating at the nominal design level of 1kW (with changes to the converter parameter sampling mechaninsm only). Once the operation of the front-end is proved, and the AC inverter section verified in simulation, it is intended that a complete 1kW prototype be constructed, quite possibly retaining a large part of the ADC and logic systems designed here.

4.1 Front end low-power boost converter: development.

A power source is required for the system, and available at the time was a pair of PV array panels, each panel consisting of a pair of series cell chains each delivering a nominal 6V at 250mA [24]. It is possible to connect these chains in either parallel or series, and it was decided to connect the chains on each panel in series, then the two panels in parallel to give a nominal output of 12V at 500mA. This is perfectly adequate for the purpose of testing the algorithm. One vital requirement of the development of a low-power test arrangement is that the control algorithm should not be modified any more than is absolutely necessary. To facilitate this, it was necessary to ensure that the power chain dynamics remain unchanged. To do this the inductor and filter capacitor must have the same value in the low power system as for the 1kW counterpart, as must the steady state boost ratio (V_{out}/V_{in}) when the system is operating in current mode.

In order to avoid having to recalculate the PI compensator parameters (Gi,Ki,Gv,Kv), as well as having to resimulate the low-power front end it was decided to retain the same values of

power circuit passive components as was used in the high power system, together with the values of PI compensator constants. An inspection of the small-signal transfer functions of equation **(51)** shows that the small signal dynamics are unaffected by input voltage or power allowing the use of the same PI compensator constants in this low power implementation. The steady state boost ratio, 1:4 in the high power system may be varied so as to allow the output voltage to be set at an appropriate value. Although the steady state duty cycle, Δ, to which boost ratio is directly related is present in **(51)**, it has been shown in section 3.7.2 that the system is stable across all practical values of Δ.

Although the input voltage is reduced, which will tend to reduce the inductor ripple current, this ripple current will be quite large in proportion to the array current at maximum power For a 12V array the specified 1mH inductor will result in a worst-case ripple current (at 12V and when δ=0.5) of:

$$di = \frac{Edt}{L} = \frac{\left(12\times0.5\times\frac{1}{20000}\right)}{1200\times10^{-6}} = 250mA \qquad \textbf{(64)}$$

assuming a switching frequency of 20kHz. Therefore if the existing value of L is used in a low power test bed, both the maximum power and the average current mode control algorithms can still be proved to work, but the converter power throughput at maximum power can be expected to be less than the actual array maximum power. This was anticipated during the analysis of the results.

The switching element was chosen to be a cheap run of the mill switching MOSFET of which there are a considerable number available. It is considerably over-rated, but this is of little consequence. Given that the topology of the boost converter allows the source of the MOSFET to be commoned, drive of the device is simple, and a fairly standard gate drive IC was selected to perform this.

An inductor of value 1.2mH, capable of sustaining a DC current of around an amp without saturating, was sourced from [24] as a ready made unit, while the output capacitor is made up from two 470μF low e.s.r. types. The diode is a standard fast recovery type.

4.2 Signal conditioning.

The control algorithm requires the measurement of PV array voltage, inductor current (from which average diode current may be calculated) and output voltage. The voltages may be sensed directly, and the reference rail used by the controller may be connected to the common rail of the power chain. However the sensing of the inductor current required some thought. Presently available are a number of Hall effect transducers consisting of a Hall effect device mounted in a small gap in a toroidal core, upon which a number of turns of wire are wound carrying the current to be measured. These are available as complete encapsulated units with on-board amplification for the output of the Hall effect device and designed to operate over a range of currents. These devices would be eminently suitable for the 1kW prototype, but the difficulty with the use of these devices at low power is that they will be operating at the very bottom end of the current range, where additional amplification would be required and noise may therefore become a significant problem as the signal-to-noise ratio is reduced. There may also be some question regarding the linearity of the devices at the very bottom end of the range.

Sensing the current with a resistor was the obvious choice. The value of the sense resistor has to be kept low in value to avoid upsetting the dynamics of the system. Placing it in the PV array return connection (the common rail) before the switch ensured that one end of the resistor was at ground potential without compromising the measurement of inductor current (which in this topology is identical to array current) and this eased the problem of amplification of the signal by removing a large common mode DC component.

An amplifier for the signal representing inductor current was designed around a standard monolithic differential instrumentation amplifier IC, but although giving a clean output signal, it could not slew fast enough at the gains required and was thus abandoned in favour of a simple

single-ended approach using an operational amplifier. This was a considerable improvement over the instrumentation amplifier, but was found to be quite critical as to choice of op-amp. A standard TLO71 device was found to exhibit similar slewing problems at high gains. Fast op-amps, such as the OP-07 and OP-37 were tried and found to work well with little noticeable noise on the output despite the single ended connection. The final schematic for the low-power chain is given in **Figure 123**, where its simplicity is evident. Topologically, the 1kW prototype will only differ in component types and the manner in which the converter parameters are sensed.

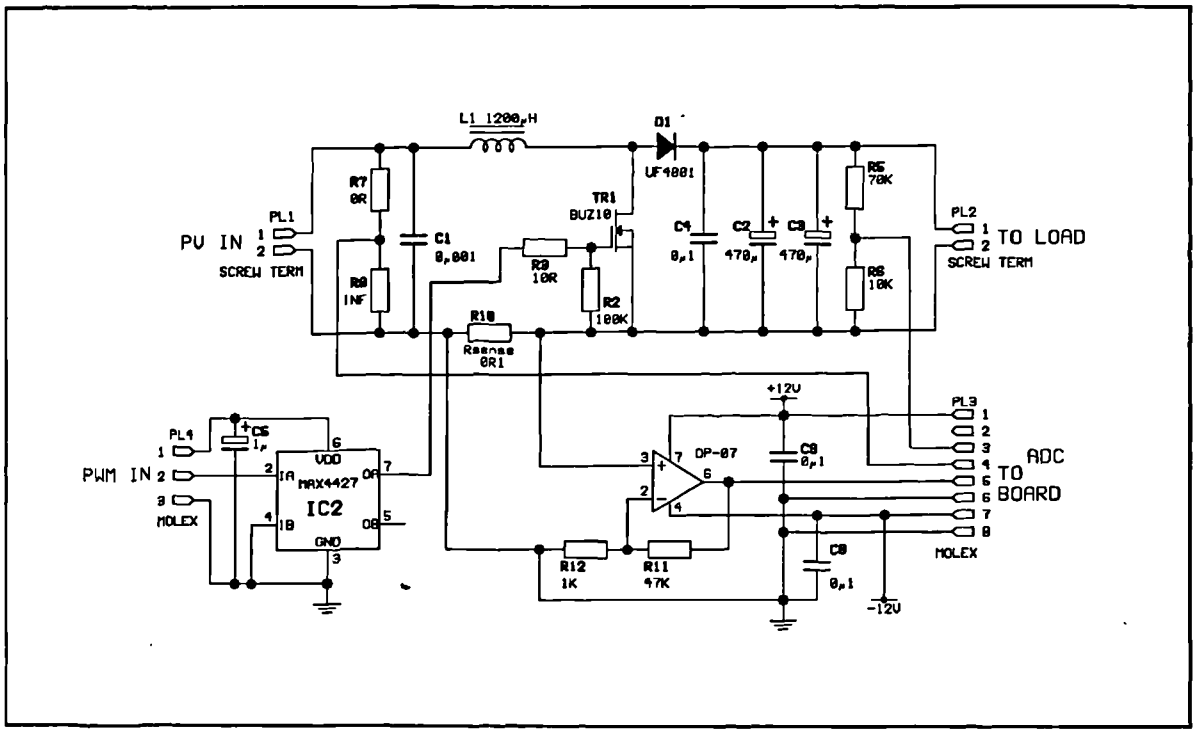

Figure 123 Low power prototype: power chain.

4.3 Sampling and conversion subsystem.

The sampling requirement of the control algorithms is that during each switching cycle, the values of PV array voltage, inductor current (from which diode current may be calculated) and output voltage are each to be sampled twice. The first of these samples is to be taken immediately prior to the switch turning on, the second prior to the switch turning off. At the

instant the switch changes state there may be some transient behaviour, thus sampling immediately before the switch changes state avoids any possibility of error in the samples.

4.3.1 Choice of ADC device

The DSP used in the system, a TMS 320C50, is a 16 bit device with a 16 bit external bus. Sufficiently fast 16 bit analog to digital converters are still somewhat expensive given the requirements of the system. It was desired that the ADC devices should interface to the DSP bus with a minimal amount of control and interfacing logic, but in addition, in order to maximize the time available to the DSP to process control algorithms the DSP should be relieved of having to generate the timing information. A considerable amount of external logic will be employed in the PWM generator, and timing information may easily be obtained from it. To facilitate this, the ADC subsystem must be able to sample and hold, and initiate the conversion independent of the data bus, i.e. without requiring a bus read or write. An interrupt may then be generated at the end of the conversion time to allow the DSP to read the valid sample data.

In addition, if the ADC has an on-chip sample and hold this will reduce the amount of analog signal processing required. A 12 bit successive-approximation device, the MAX122, was used. This has an on chip sample and hold and a voltage reference with a microprocessor-compatible bus structure and five different operational modes: a full controlled mode where the microprocessor controls every aspect of ADC operation except the conversion start which is a single logic input to the device, a stand-alone mode where the conversion control is by way of simple logic signals, two modes which are variants on the stand-alone and full controlled mode to enable direct memory access into fast or slow memory and a final mode allowing continuous conversions, one after the other with no convert start signal being required. The full controlled mode is of interest in this case (see Figure 124 for a timing diagram). Once the convert start signal is issued, the tristate bus remains

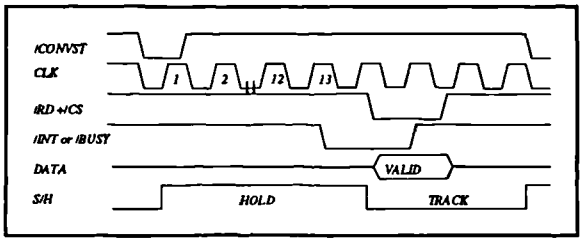

Figure 124 Timing of MAX122 in full-control mode

at high impedance until the conversion is complete, when an interrupt line is pulled low. To read the data the microprocessor simply executes a bus read at the location of the device in I/O memory. Interface logic is reduced simply to address decoding, while the timing generator has to provide a single pulse on the convert start line to sample at this point and initiate a conversion. Interrupt generation is handled by the ADC device itself.

At each sample point, it is required to sample three quantities, output voltage (V_{out}), inductor current (I_l) and PV array voltage (V_{arr}). This either requires three ADC devices, or a single device multiplexed accordingly. Examining the timing required by a multiplexed system it could be clearly seen that whichever form of ADC is used, it is necessary to initiate three seperate conversion cycles, one for each parameter. If three separate ADC devices are used, conversions can run simultaneously and the time delay before the samples are available to the DSP will be a third of that of a multiplexed system using the same ADC devices. The fastest clock that the chosen ADC may accept is 5MHz. Allowing 13 cycles for the conversion and two cycles (minimum) for the data read, the total conversion time is $15x1/(5x10^6)=3\mu s$. This corresponds to 100x3/50=6% of one switching cycle at 20kHz. This can be compared with the multiplexed system using the same ADC which requires 18% of the cycle time to sample the data not taking into account transition and settling times for the analog multiplexer switch etc. Considering the added cost and complexity of using a much faster ADC with multiplexing circuitry it was decided to use three separate ADC devices. With a conversion time of 3μs the MAX122 devices were adequate.

4.3.2 Analog signal preprocessing.

The analog input specifications of the MAX422 ADC is a bipolar signal with a range -5V to +5V giving an output in two's complement. All of the converter parameters being measured are unipolar signals with a varying range. **Table 8** shows the possible ranges of the low power converter parameters. It is necessary to buffer these to the input of the ADC using an amplifier with a gain set up to make full use of the resolution of the device. In addition a DC offset must be added in to offset the ADC input by -5V. This was done using a two stage system: scaling

followed by offset addition and buffering. Given that the current probe gain is adjustable and therefore only requires the addition of the offset, scaling is required only upon the two voltage parameters and this may be done simply by a pair of voltage dividers on the power chain board. This ensures similarity of the magnitudes of signals fed to the ADC board.

Table 8 Ranges of converter parameters for low-power prototype.

	Upper limit	Lower limit
V_{out}	15V (nominal) x2 (overshoot) =30V	0V
V_{arr}	12V (nominal) 8V (overshoot) =20V	0V
I_l (from amp)	Variable, dependent on current probe gain	0V

The ADC board was designed incorporating non-inverting amplifiers with a gain of 2 to buffer the inputs to the ADC. These amplifiers, the schematic of which is shown in **Figure 125** for one of the three channels, have the bottom end of the feedback divider tied to +5V generated from a dedicated voltage reference IC. The output of the amplifiers are offset by -5V and form the input to the ADC devices. Offset trim is provided for each channel, and fast precision op-amps were used which appear to have excellent stability and slew rate without requiring external compensation even at low closed loop

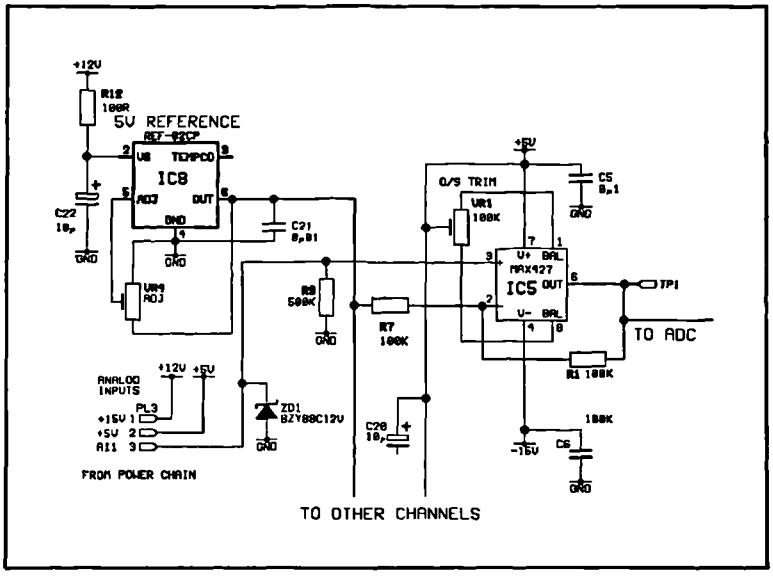

Figure 125 Schematic of one channel of the ADC buffering system

gains. The ADC board contains all the buffering required by the ADC devices, and the three ADC channel inputs to the board are specified as being unipolar analog signals with a range between 0 and 5V.

4.3.3 Sample timing

The timing required by the sampling subsystem is shown in **Figure 126**, where the relation of the ADC convert start signal (/CONVST) to the pulse-width modulated output (/PWM) can clearly be seen. The time t_{calc} is the time available after all the samples required to make the calculation of δ for the next switching cycle have been read for the DSP to execute one iteration of the control algorithm before having to write the new value of δ to the PWM generator. It is thus imperative to keep t_{cnvrt}, the conversion time, down as low as possible. The maximum ADC clock speed is 5MHz and the device requires 12 complete clock cycles after /CONVST goes low to execute the conversion. The ADC will assert the interrupt line a time t_{B1} later of nominally 150ns, so for worst case add an extra clock cycle to the conversion time. Using the maximum

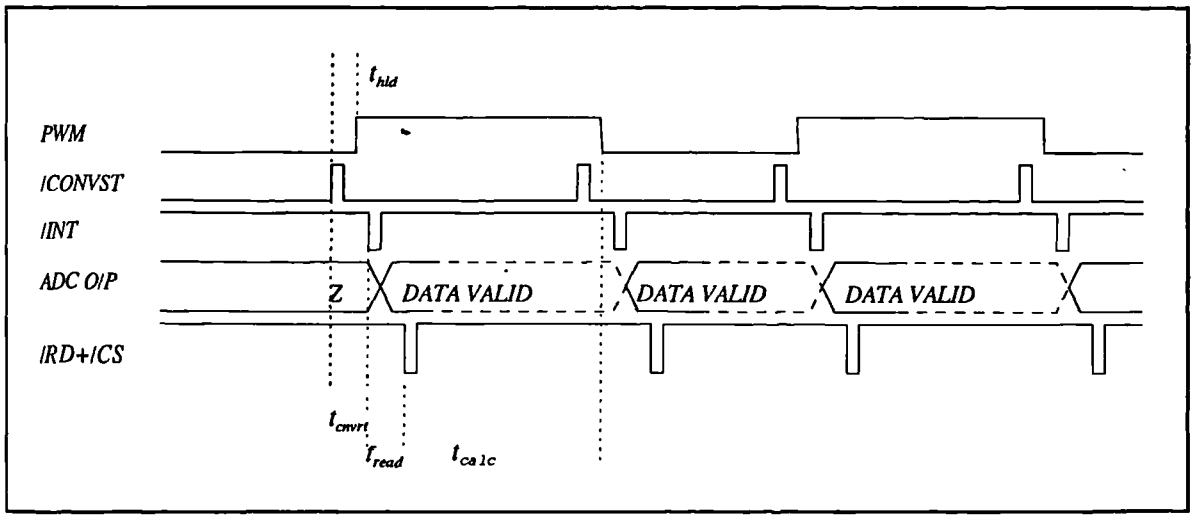

Figure 126 Timing of ADC subsystem (not to scale)

clock speed of 5MHz is convenient; as the DSP bus clocks at 20MHz the ADC clock may be derived by dividing the bus clock by 4. At a clock speed of 5MHz, the conversion time t_{cnvrt} is equal to $13x(1/5x10^6)$=2.6μs. This is fast enough. At a PWM clock speed of 20kHz, resulting in a cycle time of 1/20000=50μs, t_{calc}=50-(2x2.6)=44.8μs. In practice, /CONVST is asserted just

prior to the edge of the switching waveform to prevent transient behaviour being sampled. The 44.8μs of t_{calc} corresponds to $44.8 \times 10^{-6}/(1/20 \times 10^{6})=896$ instruction cycles. A large number of the DSP instructions are single-cycle, including the 16x16 signed multiply. This figure of 896 includes the I/O transfer instructions such as the ADC read and the PWM write, so the number of instructions available to the algorithm is somewhat less.

4.4 PWM generator subsystem

To generate PWM in the analog domain, the most common method is to compare either a triangle or sawtooth waveform of appropriate frequency with a modulating voltage lying within the range of the ramp. The resulting pulse train will have a δ equal to the modulating voltage divided by the height of the triangle. Use of a sawtooth ensures that the switch turn-on time is synchronized to the clock (turn on at clock time), whereas if a triangle is used both the turn on and turn off will vary.

Generation of pulse-width modulation in the digital domain is as straightforward as it is in the analog domain, and can be implemented in a similar fashion to the analog system. One such approach can be seen in **Figure 127** where a turn on at clock time approach is implemented. This system suffers from one apparent disadvantage in that the controlling microprocessor or DSP has to operate conditionally on the clock time. At the start of the PWM cycle the DSP must load the δ value into the down-counter, whereupon the SR latch is set and the PWM output goes high. As the counter counts down past zero the 'zero count' output is asserted, resetting the SR latch and the PWM output then goes low. The counter continues to count until the next value of δ is written to the counter. Therefore it is necessary to generate a DSP interrupt pulse once at the start of every switching cycle in order that a new δ may be loaded.

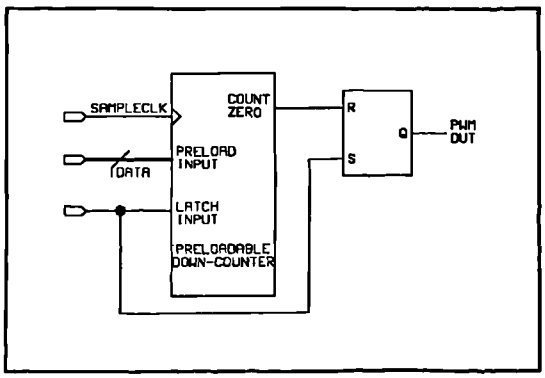

Figure 127 Simple digital PWM generator

In some systems this may not be a disadvantage. However in the PV front end system, where interrupts are generated by the ADC subsystem twice in each switching cycle once the conversion is complete, use of a simple PWM generator such as that described above would require the generation of a third interrupt at the exact start of the cycle in order to reload the PWM counter. This would not only require further processing overhead but could also reduce the number of instruction cycles available to the filter algorithm. The time between the start of the cycle, when the δ is written (time t), and the availability of the first sample data (at $t+t_{conv}$) would be unusable by the controller algorithm as no computation data would be available during this time. Some thought was then given to how this PWM generator could be modified in order to eliminate this problem.

4.4.1 Development of improved PWM subsystem

The solution to this timing dependency was to break the link between the DSP and the PWM subsystem, and develop a PWM generator that could operate asynchrously with the DSP in the sense that once a new δ is written to the subsystem, it will continue generating pulses at this value of δ without requiring DSP bus activity until a new δ is written - this will then take effect at the start of the next cycle. To do this, the system of Figure 128 was developed. The counter is free-running, and will generate one carry pulse every switching cycle (which is derived from the sample clock - the PWM frequency is equal to the sample clock frequency divided by the number of states in the counter). This carry pulse resets the SR latch and causes the PWM switching signal to be asserted. Once the count reaches the value of δ written into the latch, the comparator output is asserted resetting the SR latch and pulling the PWM output low. This operation continues until a new value of δ is written into the latch.

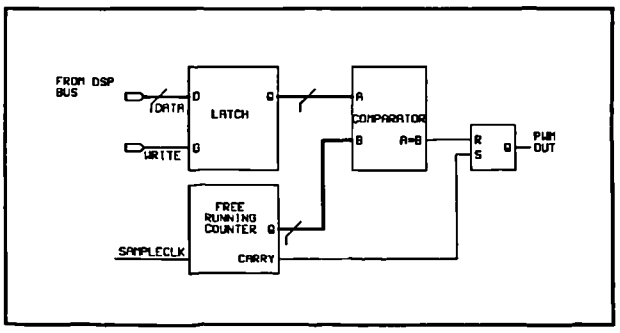

Figure 128 Improved asynchronous PWM generator.

The system thus operates independently of the DSP, which does not have to generate timing information for the switches. The system is not perfect, in that there are a number of restrictions upon the time at which a new δ may be written. This should occur during the switch off time or near the start of the on time, as if a value is written during the on time that is less than the current value, the output will change state at the instant that the value is written giving one switching cycle with an erroneous value of δ. Double-buffering the input would prevent this, but since a new value of δ is calculated every switching cycle this restriction does not really pose a problem. If there is a lower limit on δ (see section 4.4.2) it is possible to write the new value of δ during the interrupt service procedure for the ADC read of the sample taken at on-time. Since any calculated value of δ can never be less than the lower limit the new value of δ will take effect from this point onwards. This PWM system was sucessfully used in the low-power prototype.

4.4.1.1 PWM system resolution

The PWM system resolution is largely limited by the speed of available clocks. The DSP uses a master bus clock of 20MHz. If a PWM cycle time of 1/20kHz=50μs is required, the free-running counter must wrap around every 40μs. If the counter is clocked from the synchronous clock running at 20MHz the resolution available, i.e. the number of states required by the counter is $50\times10^{-6}/(1/20\times10^{6})=1000$. The number of bits required, therefore is 10, since $2^{10}=1024$. To design a 10-bit counter that will count modulo-1000 is not difficult, but in this instance, the modulation value byte would also have a maximum value of 1000, corresponding to a duty cycle of unity. For the DSP to relate the value of δ calculated by the control algorithm to the modulation value would require an extra multiplication by a constant. It was thought that if the PWM counter could be arranged to have integral bit resolution (i.e. if its maximum δ could be arranged to be a bit pattern consisting entirely of ones) this multiplication could be dispensed with and replaced by a simple truncation, effected by discarding the superfluous bits. In the low-power controller, due to the implementation used it was also thought better to reduce the amount of logic in the PWM generator to only that necessary to ensure fitting in the relatively small programmable logic device containing it.

Using 10 full bits of resolution with the 20MHz clock gives rise to a switching frequency of $1/(1024x(1/20x10^6))=19.5kHz$. This figure is very close to 20kHz anyway and the slight difference yielded by implementing a modulo-1000 counter is not really worth the extra effort required to implement it.

4.4.1.2 PWM status bit

The controller will need to know whether the interrupt just generated is at the switch on-time or at the off-time. To facilitate this, the state of the PWM output signal may be read back on the least-significant bit by the DSP via a tri-state buffer.

4.4.2 Duty cycle limitations

A maximum and minimum value of δ will have to be assigned to allow for the two samples at switch on and off time. Considering low values of δ, it can be seen that if the on-time is less than the time taken for the first sample to be latched, converted and read into the DSP there will be a collision between the two conversions, and correct sample data will not be available to calculate the next value of δ. The same can be seen to manifest itself during the off-time for high values of δ. The imposition of these limits upon the duty ratio will not interfere with the operation of the converter as it is undesirable for the converter to be operating at any length of time at the extremes of its possible range of operation. At high values of δ, where the boost ratio (V_{out}/V_{in}) is asymptotic to infinity, the efficiency of the converter is very low as with the high inductor currents and small conduction period, a significant amount of power is lost in the switching element. At low values of δ, where the boost ratio approaches unity, the implication is that the input voltage is approaching the output voltage. For this PV application, considering the 1kW system, this would imply that the array voltage is approaching 400V (or the output of the converter is approaching the array voltage), which will never happen in practice as this would be well outside the design range when the nominal array voltage has been set at 110-150V. - if the input voltage ever did get this high (or the output voltage this low) protection circuits would bring about a system shutdown. Initial limits on δ were set at 0.1 (boost ratio of 1.1) to 0.9 (boost ratio

10) which covers the expected converter operating range. The limits are imposed in software and did not require any extra hardware to implement them.

4.4.3 Generation of ADC conversion start pulses

The ADC conversion start pulses are generated directly from the PWM signal. **Figure 126** shows the required timing. The length of the /CONVST pulse required to ensure correct operation of the ADC device is specified as 30ns. It is simple to generate synchronous delays of integral multiples of the period of the synchronous clock, and, in this case using the 20MHz clock, it is convenient to obtain a pulse width of $1/20 \times 10^6$=50ns. If the /CONVST pulse is asserted for the duration of one clock cycle there will be a significant safety margin and the ADC is guaranteed to detect a valid /CONVST.

The /CONVST pulse is generated by a very simple, arrangement (**Figure 129**). The output of the PWM generator is delayed by a clock cycle by passing it through a synchronous D-latch to form the PWM output to the gate drive system. The /CQNVST pulse is formed by exclusive-ORing the delayed PWM with the original. The net result is that prior to every edge of the PWM output a pulse, of one clock cycle duration, appears on the /CONVST line.

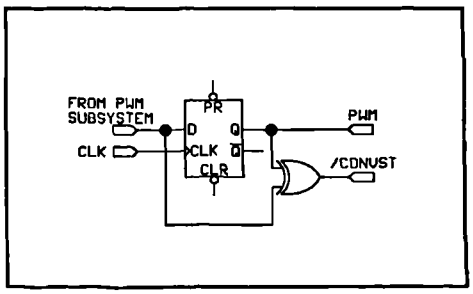

Figure 129 Conversion start pulse generator.

4.4.4 Reset logic

It is necessary to ensure that the PWM and interface logic powers up in a known state. To guarantee this the DSP /RESET line is sensed, and whenever a low is detected (i.e. the DSP is reset) the interface and ADC systems are also reset. The requirements are that the PWM counter is reset to zero, and the output is forced low. This condition is maintained for the length of time that the DSP /RESET is maintained, and once it is released the PWM system will start a

normal cycle. Note that the latch into which the PWM duty cycle is written is not reset, and thus it is the responsibility of software to zero this on or immediately after reset as part of its initialization routine.

4.5 DSP card

The DSP card is a TMS320C50 evaluation board available from Texas Instruments. It comes complete with a rudimentary assembler, and a powerful assembly-level debugging system allowing in-situ debugging of real-time code by way of a serial link from the board to the debugger software running on a PC. The card contains a DSP, a boot ROM (containing the serial communication code) and a simple audio ADC/DAC device. An on-board supply rectifier and regulator means that a 9V AC/DC power supply is all that is required for the DSP board, and the complete DSP bus system is brought out to header plugs facilitating ease of connection to additional hardware. The DSP itself is a 16-bit fixed-point device, with a 32-bit accumulator and product register. The one-deep hardware stack used for context save on interrupt does not allow interrupts to be nested without an additional software context save, but given that most instructions are one or two clock cycles in length the serial execution of interrupts is possible in most cases. The device is clocked at 40MHz, but an internal clock division by 2 results in the bus and core being clocked at 20MHz. This evaluation board saved considerable work in designing a suitable PCB for the DSP device, which comes in a 132 pin quad-flat pack (QFP). A seperate, more powerful macro assembler was used for the software development as the capabilities of the rudimentary assembler supplied with the board were insufficient.

4.5.1 Interface logic

Given the fact that the ADC devices are directly compatible with a microprocessor bus, and that the PWM subsystem may be written to by way of a simple latch, then the interface logic was simply reduced to a matter of address decoding. The three ADC channels were mapped into consecutive locations in I/O space in the DSP memory map, with the PWM subsystem being mapped into the next higher location. Partial decoding is used resulting in the four ports repeating

themselves throughout the I/O map, but given that the I/O map is free, this is of no consequence. A jumper on the PCB allowed any one of the four maskable interrupt channels (/INT1 to /INT4) to be driven from the ADC subsystem. The ADC devices are clocked at 5MHz, and their bus read cycle times will require the insertion of wait states into the DSP read cycle; this can be set up in software and does not require any additional hardware. The PWM generator is clocked using the synchronous 20MHz clock, and does not require wait states. Since three ADC devices will be sampling simultaneously the CPU interrupt signal was formed by ANDing the three interrupt lines from the ADC devices. This ensures that the CPU interrupt is not generated until all three ADC devices have finished their conversions. Each ADC will hold its interrupt line low until the read cycle is started, thus the CPU interrupt line will be released once the first value is read. The 320C50 requires the interrupt line to be asserted for three clock cycles before the interrupt is serviced as a guard against spurious interrupts. This will reduce the time available to the DSP for control calculations by $3x(1/20x10^6)=150ns$, which is not that significant an amount.

4.6 Hardware implementation

A double-sided plated-through-hole PCB carried the ADC and interface subsystem, while the power circuit, gate drive and inductor current signal amplifier was built on a small board. The DSP board connects to the interface and ADC board by way of three 24-way jumpers with IDC header plugs at each end.

The PWM generator, together with the interface logic was contained within a single *programmable logic device - an Altera EP1810 EPLD. The logic in this particular instance* was a tight fit within the 68 macrocell device. Considering the future hardware development surrounding the AC inverter section, which would involve at least one further PWM subsystem along with additional ADC channels it is going to be necessary either to move to a larger class of device, such as field-programmable gate arrays (FPGA), or to obtain more sophisticated programming hardware and software for the larger Altera devices. Although larger, and more easily reconfigurable, FPGA devices do have a number of disadvantages, one of which is that propagation delays through the device are not consistent and can cause timing criticalities.

Development software for these devices, although available, is workstation-based and does not have the speed, portability and flexibility of the PC-based Altera development software.

4.7 Software development.

The development of the controller software proceeded in two stages. Initially the interrupt driven ADC read, scaling and diode current calculations were implemented and tested, followed by the control algorithm code. The structure of the system was thus defined by the interrupt driven tasks and it is simple to add code to perform a single cycle of the control algorithm calculations at this point. Calculations that could not be reduced to single-cycle instructions were implemented using macros.

4.7.1 Internal variable and coefficient representation

In the implementation of any digital control algorithm within a fixed point processing core, the wordlength used to represent the fractional part of a number is important to the correct operation of the algorithm. Too few bits, and truncation after the multiplications becomes a source of error. Too many bits, and the computation time can increase significantly as the total word length used to represent a number requires more than one location in storage thus requiring shifting.

In this system, to simplify the design it was decided to represent all numbers in 16.16 32-bit format: each number has 16 integer bits, and 16 fractional bits. The lowest number that can be represented in this manner is thus 1/65536=0.000015. This format has sufficient accuracy for this application. Although 16 integer bits are unlikely ever to be used to the point of overflow, this format was retained through convenience. The DSP has a 32 bit accumulator and product register, while all other memory locations and registers are 16 bits. To effect a 32 bit add simply requires two single-cycle add instructions to add two consecutive memory locations containing the fractional and integer bits to the accumulator. No further shifts or truncates are required. The real advantage of retaining the 16.16 format is in the multiplications, where a macro effects a 32x32

multiply in 18 cycles. There are no awkward shifts involved, which would take up considerable time if the two portions of the number were not word-aligned. Finally, any format using less bits would still require two locations in memory to store it unless it could fit in a single word (and this would curtail accuracy) and so there would be no advantage in using a smaller format.

4.7.2 Timing and detail of interrupt handling functions.

The diagram of **Figure 130** shows the basic operation of the interrupt service routine (ISR), with the detail of what is required at the point of each interrupt expressed in pseudocode form. Basically the interrupt handler is an encapsulated function, asserting a DATA_VALID flag when the four variables required by the control algorithm have been obtained. These variables are P1 and P2 (the two array power samples at switch turn on and turn off), the converter output voltage V_o taken at sample 2, and IL_AVG, the average diode current which is calculated within the ISR from three inductor current samples. These four variables are valid at the completion of service of the interrupt at SAMPLE 1 in **Figure 130**, for the previous switching cycle. Once the DATA_VALID flag is asserted, one iteration of the control algorithm may be executed to calculate the duty cycle for the next switching cycle (thus the two switching cycle delay associated with average current mode control). The ISR is responsible for loading the new value of DELTA calculated by the control algorithm into the PWM subsystem at the start of the ISR at sample 1.

4.7.3 Controller algorithm, implementation requirements.

The overall controller algorithm developed may be seen in **Figure 131**. The implementation of the controller in MAST for use with the Saber simulator was relatively straightforward. The proportional plus integral (PI) compensators were implemented using the direct form of the z-transform, the conversion from the s-domain having been performed by way of the bilinear transform. With the simulator, this is a perfectly adequate method as the precision

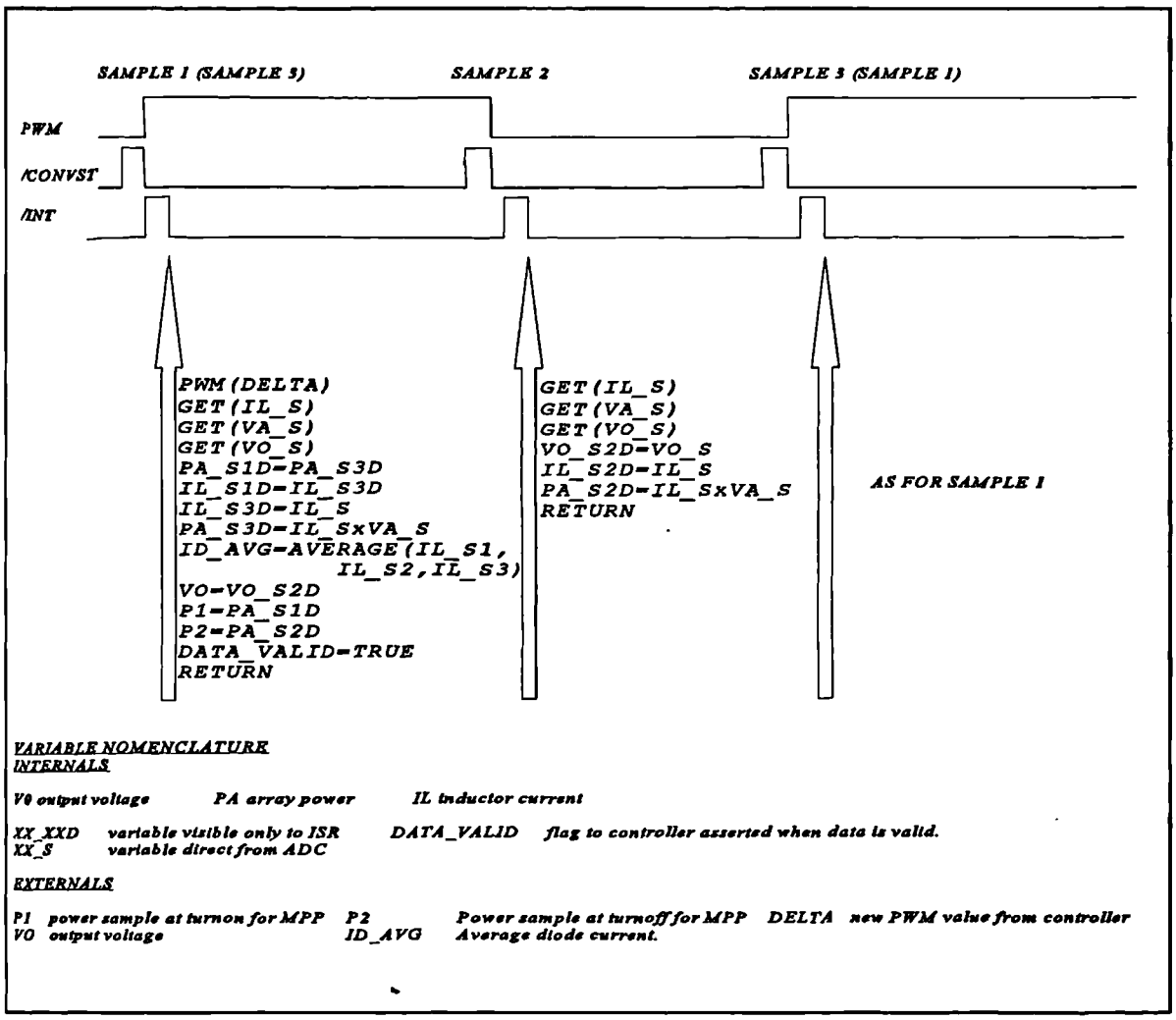

Figure 130 ISR timing and pseudocode

of the floating-point internal calculations performed within the simulator is very high (if they were not the simulator would generate very large errors during a run and be of little use at all as a simulator). The DSP implementation, however, is subject to truncation in multiplication and a finite representation for both the coefficients (gains) and the internal variables.

This can be problematic with the direct form of the z-transform. A PI compensator uses a pure integrator (the 1/s translates to $1/1-z^{-1}$) and thus the coefficient in the denominator of 1 can be represented accurately. However the same cannot be said for the numerator coefficients. The transfer functions, in the z-domain, for the controller in **Figure 131** are:

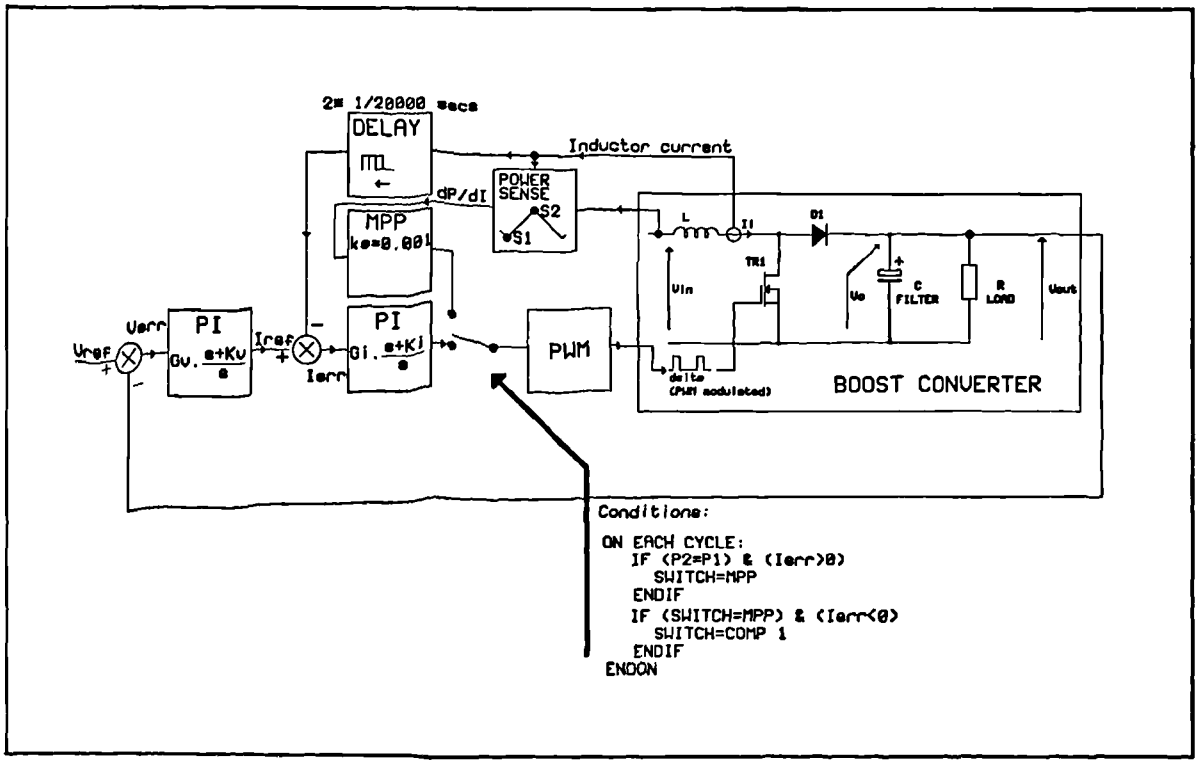

Figure 131 Basic PV converter controller algorithm.

$$\frac{i}{v} = 1\frac{s+50}{s} = 1\frac{1.001-0.999z^{-1}}{1-z^{-1}}$$
$$\frac{\delta}{i} = 0.03\frac{s+150}{s} = 0.03\frac{1.003-0.997z^{-1}}{1-z^{-1}} \qquad (65)$$

If the numerator coefficients are quantized to 16 fractional bits, the resulting coefficients will be in error. **Table 9** shows the difference between the original coefficients and the effective value of them when they have been quantized to 16 fractional bits.

Table 9 Coefficients quantized to 16 bits.

Original	Quantized
1.001	1.00992
0.999	0.998993
1.003	1.002991
0.997	0.996994

It may seem that this error is small, but it can still have a degradatory effect upon the operation of the compensator as for some combinations of sampling rate and compensator parameters the actual

value of the compensator parameters can be critical. As such, a small alteration in the value of the constant, say due to quantization, may cause a very large variation in the perceived position of the poles and zeros of the system as seen at the input and output of the compensator.

To overcome this, a different type of continuous-to-discrete transform was used. Known as the delta operator [47] (referred to here as δ_f to avoid confusion with switch duty cycle δ) it can be derived from the z-domain transfer function by the simple transform of:

$$\delta_f = z - 1 \tag{66}$$

therefore substituting into the bilinear transform to give s in terms of δ^{-1}:

$$\begin{gathered} s = \frac{2}{T}.\frac{1-z^{-1}}{1+z^{-1}} \\ z^{-1} = \frac{\delta_f^{-1}}{\delta_f+1} \quad \therefore \quad s = \frac{2}{T}.\frac{1+\delta_f^{-1}-\delta_f^{-1}}{1+2\delta_f^{-1}} \\ \therefore s = \frac{2}{T}.\frac{1}{1+2\delta_f^{-1}} \end{gathered} \tag{67}$$

and transforming the frequency-dependent portions of the equations of (65):

$$\frac{s+50}{s} \equiv \left(1.00125 + 2.5\times10^{-3}.\delta_f^{-1}\right) \tag{68}$$

$$\frac{s+100}{s} \equiv \left(1.00375 + 7.5\times10^{-3}.\delta_f^{-1}\right) \tag{69}$$

The first important thing to notice is the lack of a denominator in these transfer functions in δ_f^{-1}. This is one advantage as it removes one calculation from the implementation. In the direct form (difference equation) given by the implementation of (65), the denominator term generates an addition of a delayed feedback term (there is no associated multiplication as the system is a pure integrator). This term is non-existent in the δ_f form. The flow diagrams of the two

compensators are given in **Figure 132** where the differences in computation may easily be seen. The lack of a denominator in the δ_f filter results in the implementation posessing no feedback terms. The z^{-1} function is a one-sample delay and may be implemented using a data shift (load-store) instruction. The δ_f^{-1} function is an accumulation function, requiring an addition (load-add-store) and therefore is marginally more costly in computation time, however, only one δ_f^{-1} function is required in each PI compensator (load-add-store) whereas two z^{-1} functions are required in the direct z filter (load-store load-store). The delta filter thus, by one instruction, is the least computationally intensive.

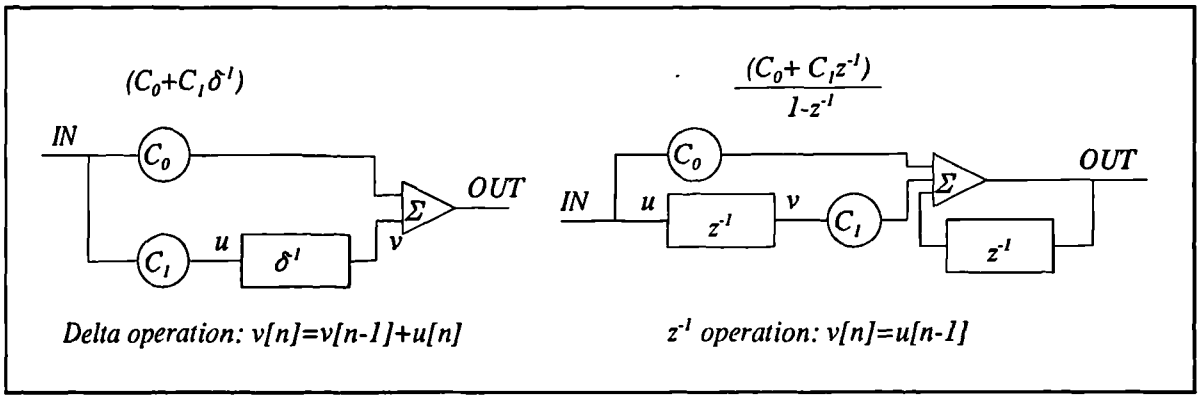

Figure 132 Comparison of δ_f PI compensator with direct z compensator.

In view of the lower sensitivities to error offered by the delta filter, the DSP implementation of the controller used delta-filters in both voltage and current loops, both of them in the form of **Figure 132**. The net effect is an implementation which is closer in performance to the desired analog transfer functions.

4.7.4 Sofware implementation

The software was developed to allow ease of modification of all aspects of the operation. All controller constants are declared in an include file, while all internal workspace sizes are calculated at assembly time allowing variables to be added or removed without having to modify several sections of code. All 32-bit arithmetic is declared as macros within a separate file as is the ADC read and scaling code; these macros are expanded by the assembler and do not incur the overhead of a function call. The basic operation of the system is once the workspace has been

initialized and the interrupt subsystem started, the code sits in an endless loop testing a flag from the interrupt subsystem. When this flag is found to be asserted the code first acknowledges by resetting the flag, then executes a call to a single function which contains the complete controller algorithm. One iteration is executed within: i.e. a new value of δ is calculated before the function returns to the loop. All sample values are read on interrupt and handled by the interrupt service code. For ease of legibility and future development the entire software package was constructed from three assembler files. The first of these contains the entry point for the code and simply calls the appropriate functions. The second of these contains the control algorithm function,. Finally, the interrupt service code forms the third file, and functions within this module are called only by a hardware interrupt (other than the initialization code called at startup). The basic flow can be seen in the pseudocode of **Figure 133** and **Figure 135**, with **Figure 134** showing the execution of the macro for bounds-limiting used within **Figure 135**.

```
FUNCTION RunControl:

LOOP:
      IF DATA_VALID;
            DATA_VALID==FALSE;
            CALL FILTER
      ENDIF;

GOTO LOOP:
```

Figure 133 Pseudocode of main loop

```
MACRO RANGECHECK(VARIABLE,LOWER,UPPER);

        FLAG=TRUE;
        VARIABLE=VARIABLE-LOWER;
        IF(VARIABLE<=0)
                VARIABLE=0;
                FLAG=FALSE;
        ENDIF
        VARIABLE=VARIABLE-(UPPER-LOWER);
        IF(VARIABLE>=0)
                VARIABLE=0;
                FLAG=FALSE;
        ENDIF
        VARIABLE=VARIABLE+UPPER;
        RETURN(FLAG);

END RANGECHECK
```

Figure 134 Bounds-limiting code.

The execution path of the controller sections of the MAST template describing the operation of the controller is almost identical to that of the pseudocode of **Figure 135**, and during the development of the DSP software it was found that the design philosophy of writing the simuation templates to be as close to a practical implementation of the system as possible paid off in the sense that the development of the DSP implementation progressed at a very rapid pace, and apart from some minor problems with the interrupt generator the system was found to work first time with little modification. This was brought about because most of the structure for the system was developed and put into place during simulation with a view to a forthcoming practical

implementation, and thus a lot of the implementation groundwork was carried out then. An 'idealized' approach to the simulation, using the 'control system' blocks and templates in the Saber libraries would have worked just as well in simulation, but considerably more effort would have been required to implement such a model as a practical system.

```
FUNCTION Filter;

% Set up voltage difference for MPP test

        V_DIFF_0=Vout-Vref;

% Voltage loop code

        Verr=Vref-Vout;
        UV=C1V*GV*Verr;
        Idmd=VV+C0V*GV*Verr;
        IF RANGECHECK(Idmd,IDMD_LOWER,IDMD_UPPER);
                VV=VV+UV;
        ENDIF

% Current loop code

        Ierr=Idmd-Iavg;
        UI=C1I*GI*Ierr;
        NI=VV+C0I*GI*Ierr;

% Maximum power tests

        P_DIFF=P2-P1;
        IF NOT MPP_ACTIVE
                IF(P_DIFF<0) AND ((Idmd-Iavg)>0)
                        MPP_ACTIVE=TRUE;
                ENDIF
        ELSE
                IF(Idmd-Iavg)<=0 OR ((V_DIFF_0 > 0 AND
                                        (V_DIFF_1 < 0))
                        MPP_ACTIVE=FALSE;
                        VI=δ-NI;                % reset integrator
                        SAMPLE_COUNT=MPP_SAMPLE_INTERVAL
                ENDIF
        ENDIF

        V_DIFF_1=V_DIFF_0;

        IF MPP_ACTIVE=FALSE
                δ=NI+VI;
                IF RANGECHECK(δ,DELTA_LOWER,DELTA UPPER)
                        VI=VI+UI;
                ENDIF
        ELSE
                DECREMENT(SAMPLE_COUNT)

                IF(SAMPLE_COUNT=0)
                        TMP=P_DIFF*KE;
                        RANGECHECK(TMP,DELTA_LOWER,DELTA_UPPER);
                        DELTA=DELTA+TMP;
                        RANGECHECK(TMP,DELTA_LOWER,DELTA_UPPER);
                        SAMPLE_COUNT=MPP_SAMPLE_INTERVAL;
                ENDIF
        ENDIF

END Filter.
```

Figure 135 Controller function pseudocode.

4.8 Result: testing of low-power system.

The primary reason for developing the low-power prototype was to determine the viability of the embedded maximum power tracking controller (PI-MPP) as an algorithm for solar photovoltaic converters. As such, the main areas of interest were the speed at which the maximum power tracking system would acquire and track, and the response of the system as the converter drops in and out of maximum power mode.

While it is possible, with the experimental facilities available, to accurately fix the array characteristic at a known value, it is difficult to generate a step change in irradiance (even more difficult a step change in array temperature) between accurately determined values. It is, however, possible to set up the arrays in such a manner as that the incident irradiance and array temperature will remain relatively constant during the period of experimentation, and thus provide a fixed array characteristic and maximum power point which can be measured. To establish the ability of the converter to track maximum power it is only necessary to allow the converter to make the transition from PI mode to maximum power tracking mode by increasing the load. The operating point at the input of the converter during PI mode will be well below the maximum power point, and by switching to maximum power operation it may be seen how quickly the system acquires maximum power, and whether it tracks it. This approach is equivalent to generating a step change in irradiance - at the instant of the step the controller is no longer operating at maximum power, therefore it must re-acquire the maximum power point.

Since the same controller constants have been used in the low power system as have been used in the high power system, it is expected that the transient response of the system in PI mode will not be as well damped as for the high power system, since the range of load resistances are likely to be higher. In addition, it is expected that the maximum power system will yield an average power during tracking of just below the maximum power point of the array itself while operating at low powers (**Figure 121**) due to the size of the current ramp during switching and this was considered when analyzing the results.

Steady state experimental values of current and voltage were taken using standard bench multimeters. The results were then plotted using MATLAB as a plotting aid. The oscilloscope traces presented here were generated using an storage oscilloscope with attached thermal printer, the hardcopy from which was then scanned after which the scale factors and axis labels were added.

4.8.1 Interrupt timing

To demonstrate the timing of the system, the trace of **Figure 136** shows how the interrupts are generated with respect to the pulse width modulation waveform. Note that the interrupts are generated just after the edge of the switching waveform (about 2ms delay) and it is at this point that the samples taken just prior to the switching are read into the DSP.

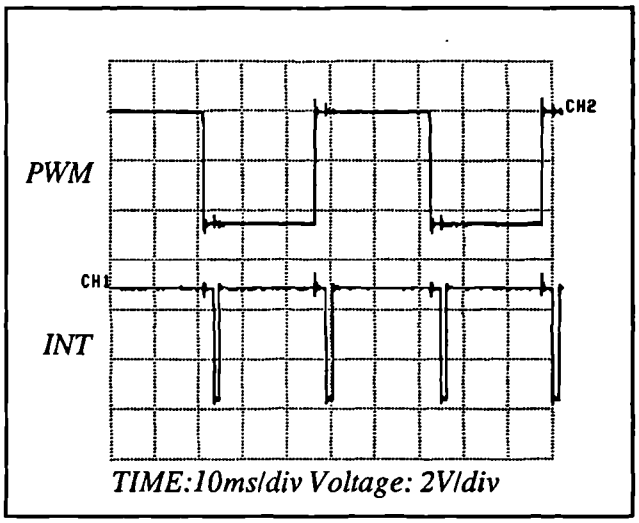

Figure 136 Interrupt timing of practical system.

4.8.2 Array I/V curve during testing of low power system.

The two PV array panels were illuminated using a 500W halogen bulb and reflector, and once the light source was switched on the system was left for 30 minutes for the array temperature to stabilize. Once thermal stability was confirmed (by watching the array open circuit voltage for any fluctuations) I/V data was generated for the array under these conditions, and from this a power curve (**Figure 137**), to yield a

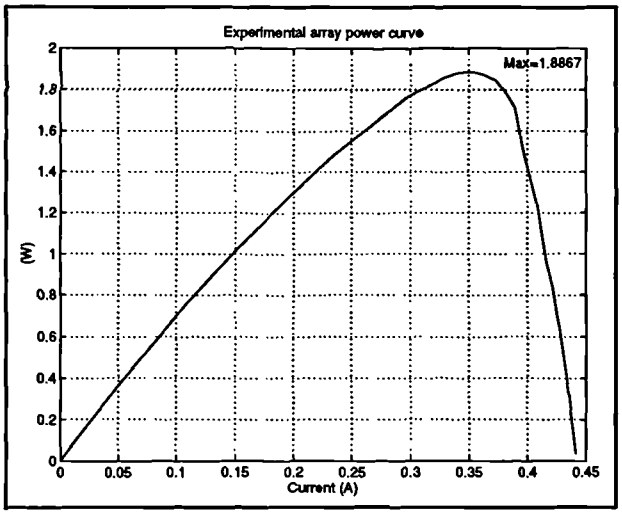

Figure 137 Array power curve during experimentation.

maximum power point of 1.886W. at an array current of 352mA, voltage 5.36V. It is possible now to calculate an estimate of the converter power throughput while tracking the maximum power point of this array. The array voltage at the maximum power point was measured as 5.36V. and from this the worst case current ripple (δ=0.5) can be calculated:

$$di = \frac{Edt}{L} = \frac{5.36\times0.5\times\frac{1}{20000}}{1200\times10^{-6}} = 111mA \qquad (70)$$

Using MATLAB, a numerical integration of the curve of **Figure 137** was performed across a 111mA region centered upon the maximum power point. The result was divided by 111mA to obtain an approximate average power throughput during maximum power tracking of 1.69W. With the position of the maximum power point now established, the extraction of experimental data could commence

4.8.3 Input: steady state and transient characteristics: an analysis.

The input power characteristics, as the converter load is swept, will show the steady state performance of the converter throughout the range of anticipated loads. It would be expedient, however, to show the effect of variations in the two parameters used by the maximum power tracker, if any, upon the characteristics. These parameters are the number of switching cycles between each sampling of the powers ('MPP_SAMPLE_INTERVAL'), and the gain of the integrator in the maximum power tracker (the duty cycle step multiplier 'ke').

To investigate the effect of variations in these parameters, five load sweeps were made. The first three of these had the sample interval MPP_SAMPLE_INTERVAL fixed at 4, while the integrator step size KE was assigned successive values of 1.953×10^3,0.5, and 128 respectively by modifying the constant file and reassembling between runs. The unusual values came about as these numbers form well defined hexadecimal (and hence binary) equivalents that can be

represented accurately in 16 bits of fraction. For each value an input power versus load current curve was obtained. A transient response was also obtained at each run by generating a step change in load from 700Ω to 10Ω, thereby causing the system to switch from PI to MPP operation. **Figure 138** shows the three steady-state curves. These show exactly what is expected. The first portion of the curve shows the array power rising linearly as the converter feeds a linearly increasing load. Once the maximum power point is reached so the maximum power tracker holds the array power at this level into the increasing load: i.e. output voltage starts to fall off. The final drop in array power is caused by the converter topology entering a region where it can not operate efficiently (high values of δ lead to higher inductor and switch currents), and thus the controller is unable to continue to track. This region is an area into which normal operation would not force the operating point. The average tracking power is less than the absolute maximum power as can be provided by the arrays - 1.76W against a maximum power from the array of 1.886W. The difference (0.12W) is due to the inductor current ramp being large in comparison with the array short circuit current than it would be in the high power system. The actual track power of 1.76W is actually better than the predicted approximate track power of 1.69W, and this is due to a combination of the fact that the duty cycle across the track region is not always 0.5, and also that the predicted value was only an approximation based upon numerical integration of experimental data where the spacing of the dependent variable coordinate representing current is quite coarse. It was intended only to show up major departures from the expected behaviour.

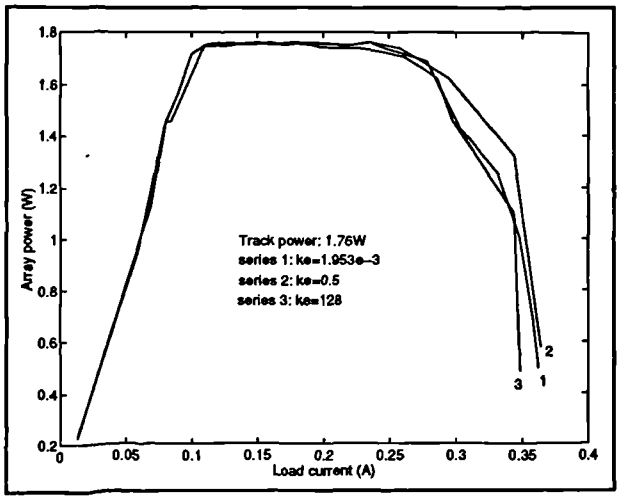

Figure 138 Family of input power characteristics as integrator step size is varied.

Variation of the integrator step size 'ke' can be seen to have little effect upon the steady state performance of the maximum power tracker. The transient responses show an improvement in settling time as 'ke' is allowed to rise from 1.953×10^{-3} to 0.5 (**Figure 139,Figure 140**). Output

voltage has been used to indicate the transient response of the tracker as this will include any transient effects due to the converter dynamics before settling down to the value giving maximum power to the load. It can be seen that increasing 'ke' above small values improves the transient response of the maximum power tracker, and hence its ability to follow a maximum power point. However, the difference between ke=0.5 and ke=128 is small (**Figure 145**), and it suggests that considerable increase in 'ke' brings about only marginal improvement.

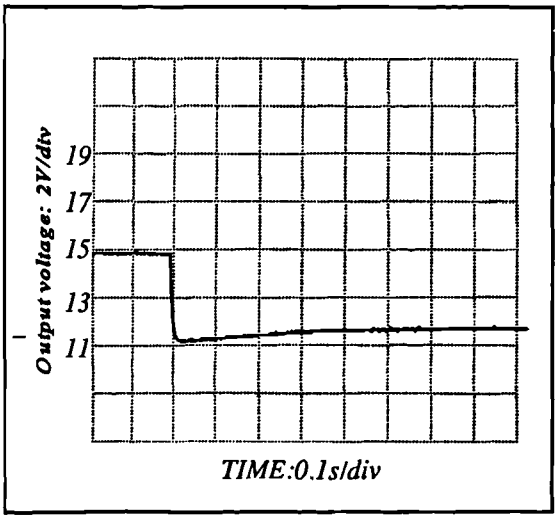

Figure 139 Output voltage transient over load change 700Ω-10Ω: KE=1.953x10^{-3}

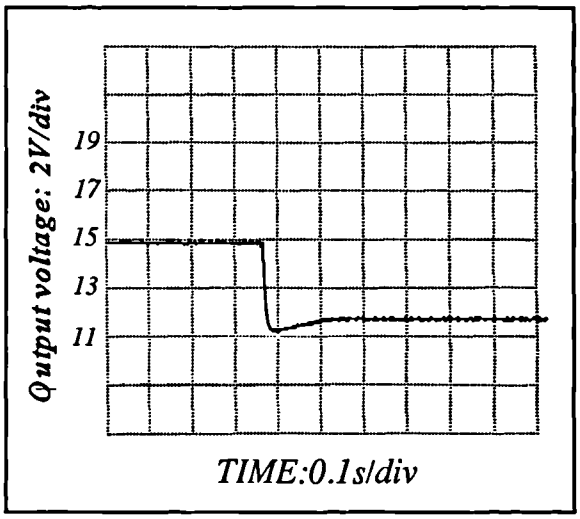

Figure 140 Output voltage transient over load change 700Ω-10Ω: KE=0.5

The nature of the 'proportional integration' ensures that as the maximum power point is approached, the integrator step size is lowered in a manner proportional to the difference between the two power samples. This ensures that the steady state tracking will not be affected significantly with variations in KE. However, when the MPP system is acquiring, the value of *KE is critical as large integration steps may cause* the maximum power point to be 'stepped over', bringing about a small overshoot of the operating point. Small integration steps will result in very slow acquisition. With the values of KE used here,

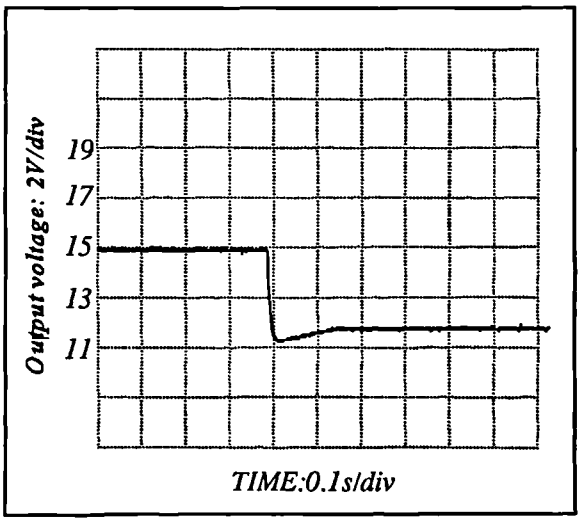

Figure 141 Output voltage over load change 700Ω-10Ω: KE=128

the fastest maximum power acquisition time is about 0.12s (**Figure 141**), and this is fast for a maximum power tracking algorithm. The small overshoot is of little consequence as a true step change in irradiance or temperature is unlikely to occur in the practical use of the system.

Variation of MPP_SAMPLE_INTERVAL was carried out at two different values. With KE fixed at 0.5, two sets of input power characteristics and transient responses were obtained (**Figure 142**,**Figure 143** and **Figure 144**). It can be seen that the variation in the sample interval has little effect upon the steady state tracking of the system. The transient response of **Figure 142** shows a much tighter response than that of **Figure 143**, and the reason for this is that with a sample interval of 2, the duty cycle is being updated every two switching cycles, whereas with a value of 20, the updates are ten times less frequent. The net effect is similar to varying KE, but the sample interval can be decreased (and the transient response improved) without fear of worsening the overshoot during acquisition as the step size per update remains unchanged.

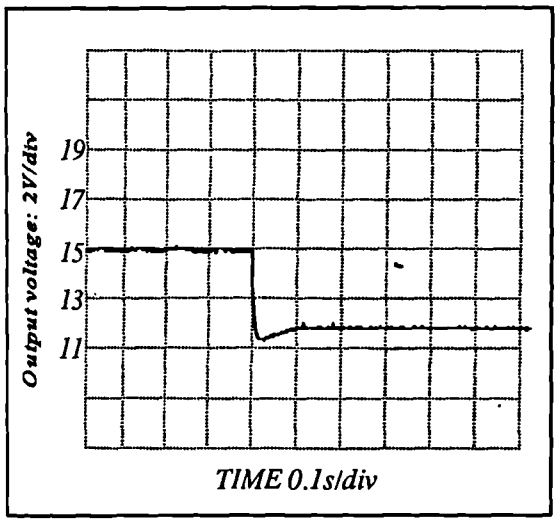

Figure 142 Output voltage over load change 700Ω-10Ω: MPP_SAMPLE_INTERVAL=2

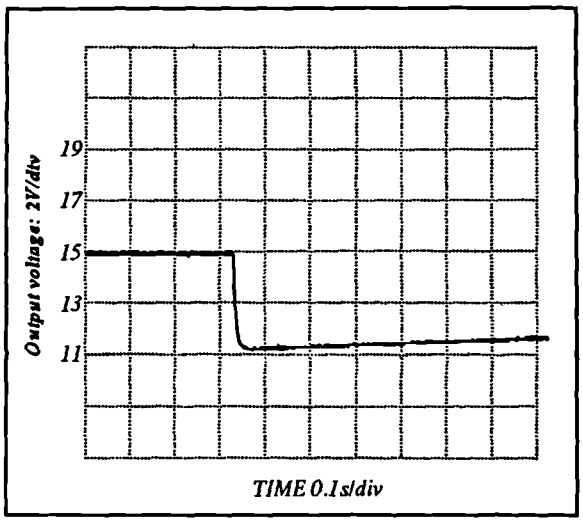

Figure 143 Output voltage over load change 700Ω-10Ω: MPP_SAMPLE_INTERVAL=20

4.8.4 Output: steady state characteristics

At light loads, the system will be regulating in the conventional manner. The regulated output voltage in this low-power system has been fixed at 15V+/- 0.5V by the reference constant in the constant include file. As the load is increased the maximum power tracker will eventually

engage, and the output characteristic will change from a constant voltage to a constant power characteristic. As the converter is loaded still more heavily eventually δ will become high enough that the converter is operating in regions where it is not at its most efficient, and, thus, the output voltage will fall off.

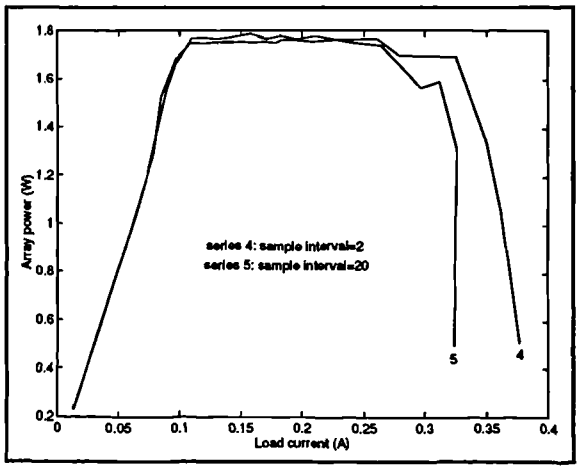

Figure 144 Array power characteristics with varied MPP_SAMPLE_INTERVAL

The curve of **Figure 145** shows the output voltage versus load (output) current for the converter under the condition of MPP_SAMPLE_INTERVAL=2 and KE=0.5. The three major sections of the curve can clearly be seen. The slight error in the output voltage during PI regulation is partly due to inaccuracies in the voltage divider generating the feedback signal. From this experimental setup, the output voltage measured was 14.65 to 14.85V, across the range of load variation in the region where the system was operting in voltage regulation mode.

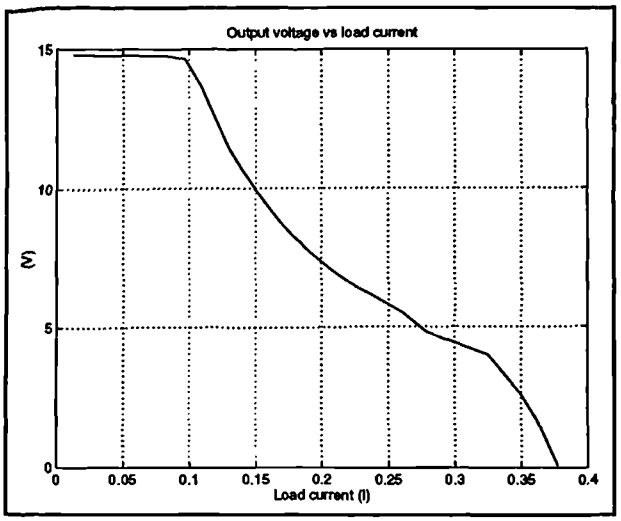

Figure 145 Output voltage versus load current.

4.8.5 Transient behaviour during an MPP-PI transition or step load change

In the region of PI regulation, the transient behaviour is important. For the low power system under consideration here it is expected that the transient response will be somewhat worse than with the high power system. To plot it a step load change was generated from 10Ω (which places the system in the maximum power tracking region) to 360Ω, a load roughly in the middle of the voltage regulation region. The resulting transient response is shown in **Figure 146.** There

is a slight ring after the initial overshoot, but only of about one half of a cycle before settling down to the steady state value. The peak of the ring is at about 15.5V, or 3% of the regulated voltage of 15V

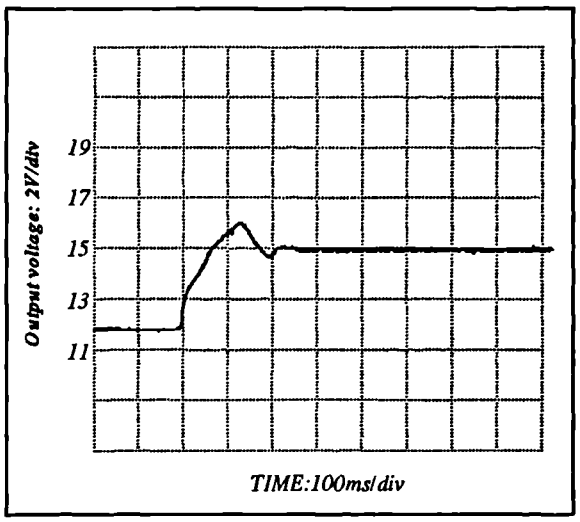

Figure 146 Transient upon MPP to PI transition.

4.9 Low power system: discussion

With the results that have been obtained, it can be seen that the control algorithm does indeed function in practice, as well as in the simulation. In view of the departure from the theoretical response at very high loads, it is advisable in the interests of efficiency to ensure that maximum power operation occurs at a point on the flat portion of the input power characteristic - if the system is driving an inverter which is utility-connected then this is a matter for the inverter control and is not excessively difficult to arrange. All transient responses are acceptable, the transition from MPP-PI and vice versa are satisfactory. The acquisition and tracking of the MPP algorithm is very fast, and perfectly adequate for the job in hand.

The system meets all of the criteria required by the front-end, and the development of a high-power version should simply be a matter of up-rating the converter power chain and using a larger PV array.

SECTION 5: INVERTER SECTION: DESIGN IN SIMULATION

A front end has successfully been developed which provides a fixed DC output from photovoltaic arrays, with a maximum power tracking characteristic into DC loads which would normally exceed the maximum power that the arrays can provide if the output voltage was retained at its regulated value. This output could conceivably drive any DC load.

The second class of loads that the system may be required to drive are AC loads, both live (a utility) and dead (e.g. an induction motor). The addition of an inverter to the DC front end would allow the system to drive all types of load thus making the photovoltaic power conversion system universal.

In the domestic environment, the primary design purpose for this system, the normal mode of operation would be as a utility feed. However, in the event of utility failure the system must immediately be disconnected from the utility so as not to cause a safety hazard to the utility repair engineers (or damage to the inverter through overloading). An advanced conversion system capable of driving dead loads could, in the presence of sufficient light, continue to drive loads while disconnected from the utility and thus keep central heating pumps, clocks and so on running during the utility down time. This is a significant advantage as much less energy is wasted compared with an inverter system that simply shut down with the utility. The block diagram of **Figure 147** shows the basic structure of the proposed conversion system.

The drive of AC loads does require some thought. Utility feeds will require a unity power factor supply which is locked in both phase and frequency to the utility, with protection if the utility is to fail. Dead loads can be even more difficult to drive as some may appear as a complex impedance and/or have a poor power factor, while others, particularly equipment containing offline switching supplies can present loads with a very high crest factor. To ensure robustness

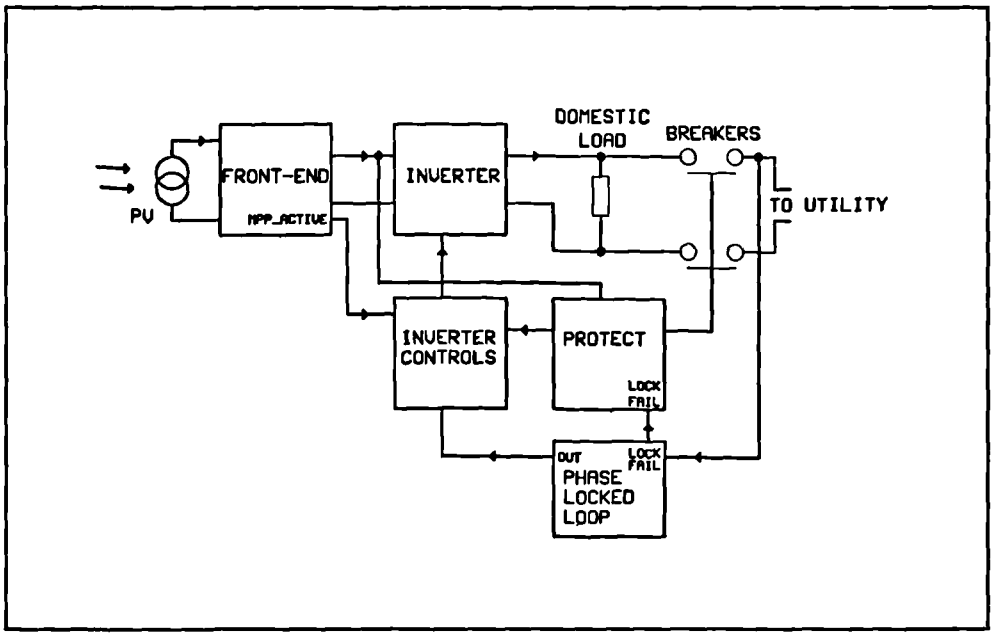

Figure 147 Block diagram of complete conversion system.

of the system all types of load must be handled. In view of the domestic application, a single phase system will be developed as if a three-phase system is desired for industrial use all of the control algorithms developed will function equally well in a three phase system.

5.1 Inverter design

The front-end provides a regulated +400VDC rail. This figure was selected in anticipation of the requirements of an inverter which could drive loads rated for UK mains. The nominal mains voltage in the UK is 240Vrms, giving a peak voltage of 340V. 400V provides a margin for inverter switch inefficiencies and any maximum or minimum limits on the duty cycle of the switches.

5.2 Inverter topology.

A four-quadrant conversion system is required that can produce an output ranging from -400V to +400V from a single-ended 400VDC rail. A full-bridge arrangement will do this (**Figure 148**) [48] but although ideal for driving dead loads it suffers from a disadvantage when the system

is driving a single-phase live load. The neutral line is at, or very near to earth potential. As a result, during the operation of the PWM switches the two DC input rails each alternate between earth and line potential. This is not a satisfactory state of affairs from the point of view of either safety or electromagnetic interference, and so an alternative approach must be found.

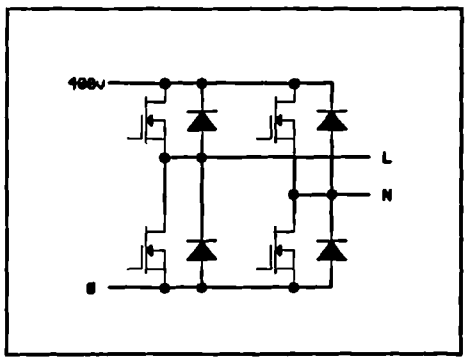

Figure 148 Full bridge arrangement.

A half-bridge arrangement (**Figure 149**) will not suffer from this problem. However, the disadvantage of this arrangement is that a split-rail supply is required, of -400-0-400V. To generate this from a single-ended supply is not difficult, but it does require the use of further switching devices. The inverter section itself, in terms of power-carrying silicon is two devices less than the full bridge however. A single additional smoothing capacitor is required, as the filter capacitor from the front end forms the top capacitor.

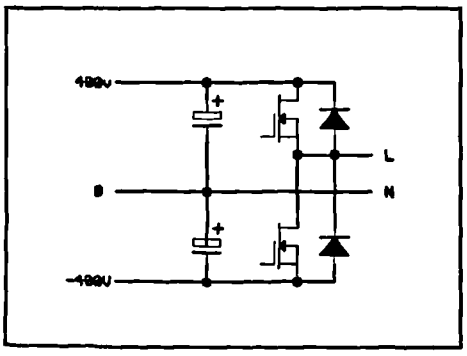

Figure 149 Half bridge arrangement.

The complete inverter power chain topology with output filter is shown in **Figure 150**. This power circuit is capable of driving all of the aforementioned loads when combined with the appropriate control.

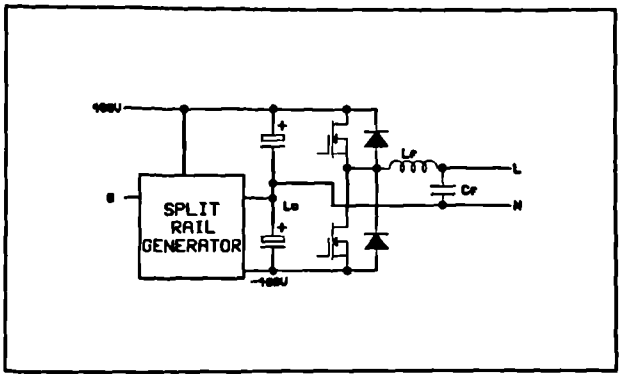

Figure 150 Complete inverter power chain.

Control of the inverter depends upon the type of load being fed. If the load is dead the inverter must appear as a voltage source. Into a utility, however, the converter output voltage is fixed by the utility and therefore the current fed into the utility must be regulated to ensure that

the front-end is within the bounds of maximum power tracking - the inverter itself behaves as a current source.

5.3 Negative d.c. bus drive: development.

To generate the split-rail supply, a number of techniques were tried in an attempt to avoid having to introduce another PWM and control channel to regulate it. One method tried was a simple up-down converter (**Figure 151**). If the inverter control algorithm does not require an absolutely rigid rail, it would be possible to operate this converter in open loop with a form of hysteresis control: if the negative rail voltage added to the positive rail voltage is positive by a fixed amount, start a 50% duty cycle pulse train to the switch; if the voltage difference is negative by a fixed amount, turn off the switch. The negative rail voltage will not be rigidly regulated using this approach. In a practical implementation, however, all the voltages required by a simple voltage-mode control system for the up/down converter are also required for the control of the inverter, and so the only extra hardware necessary for a simple voltage-mode control of the up-down converter is an extra PWM channel. A small amount of processor computation time (a PI compensator) will also be required to control it.

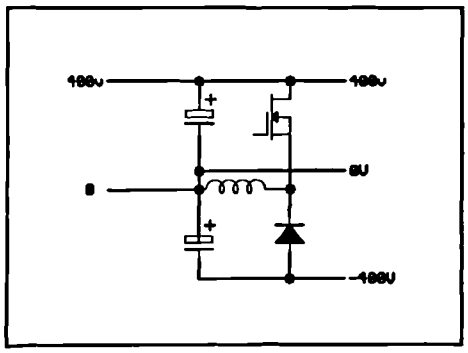

Figure 151 Up/down converter

Early tests showed that this approach, although successful when the system was driving most dead loads, failed when a maximum power load was being driven. This was due to the natural characteristics of an up-down converter.

Figure 152 shows the current profile in the positive supply rail for an inverter coupled to a perfect negative d.c. bus supply. The result is that the current, and hence power pulses drawn from the positive supply rail have a sufficiently low peak-to-average ratio in order that during maximum power tracking operation the filter capacitor in the front-end may keep the voltage

ripple within acceptable limits and the front-end in its region of efficient operation. Under these conditions it is possible to sustain maximum power operation over a complete cycle of mains without the danger of either the maximum power tracker dropping out or the positive DC rail voltage dropping significantly. If the peak-to-average ratio of the current profile in the positive rail is too high, the voltage across the filter capacitor in the front end will fluctuate between greater limits, and in order to sustain maximum power tracking across the entire cycle the positive DC rail voltage will have to be allowed to fall further at the peak of the current waveform, thus compromising the ability of the inverter to provide an unclipped voltage output and running the front-end into regions of relative inefficiency.

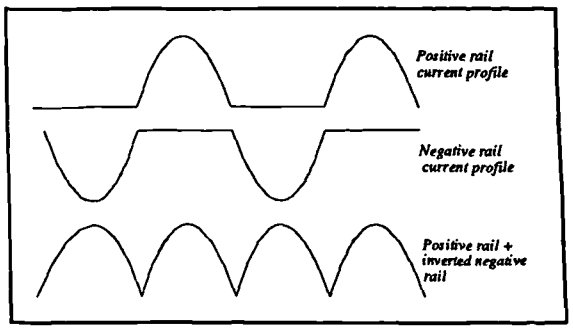

Figure 152 Current profiles using ideal rail invert drive system.

An up/down converter, in common with all continuous flyback topologies, has a right hand half plane zero in its control-to-output transfer function. The net result is that in order to bring about an increase in the output current, the duty cycle of the switch must first be increased, then reduced again. Such a characteristic makes the response of voltage mode control systems slow as to avoid instability the bandwidth must be reduced in order to allow for the lag induced by the right hand plane zero present in the small signal transfer functions for the up/down converter. As the negative half-cycle of the inverter starts and current is drawn from the negative rail, the up/down converter takes some time to respond, and the current drawn from the positive rail by the split rail supply lags the current in the negative rail drawn by the inverter. A sketch of the likely waveforms are shown in **Figure 153**, and it can be seen that the delay of the negative rail current reflected into the positive rail of the up/down converter split rail supply will result in a much higher peak-to-average ratio for the current in the

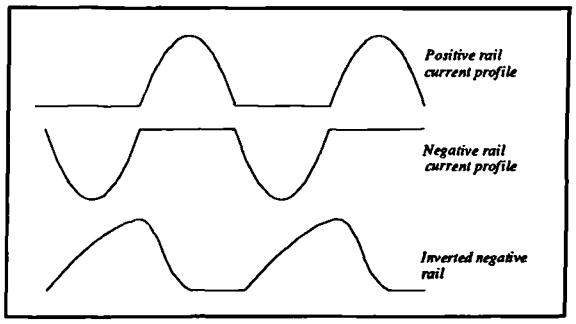

Figure 153 Current profiles in up/down converter type split rail supply.

positive supply rail. Current is still being demanded by the up/down converter when the inverter starts to demand current from the positive rail.

During early simulation tests it was found that the up/down converter, both in open loop and with voltage-mode control, would not allow the front end to stay in maximum power tracking mode across a complete 50Hz cycle - the front-end dropped out of maximum power mode and resumed voltage regulation for small portions of the cycle while the positive rail voltage fell quite considerably during the periods of high current demand.

One solution to this problem would be to go over to current mode control of the up/down converter - however this would mean an increase in the requirement for calculation time as well as yet another PWM channel to sample the inductor current. There are other topological disadvantages associated with the up/down converter. The inductor is bulky as it has to carry the large peak current without saturating. The switch carries the entire average current for the negative rail and will have to be adequately rated as inductor current will be greater than rail current. In consideration of how some of these problems could be addressed, a different approach was tried.

5.4 Resonant split-rail supply

The requirement is for a converter that will not only take a +400V rail and from it generate a -400V rail, but also accurately reflect the current profile in the negative rail into the positive rail with no significant delays. A charge-pump will do this, but the problem with a charge pump is the high peak currents involved, and such circuits are thus restricted to very low powers. However, experimentation with the charge pump using a resonant system to reduce the peak currents led to the system detailed in the schematic of **Figure 154**. A full and detailed mathematical analysis of the system including effects of system resistance is quite complex, and is given in Appendix C. The system is not without disadvantages, but simulation showed it to work well. It does not require any external feedback-based regulating control: the switches of **Figure 154** are operated in pairs, S1-S3 and S2-S4, switched with a duty cycle of 50% at a

frequency of f_s and a small deadband to prevent shoot-through. The system posesses a form of intrinsic feedback which uses the difference between the rails as a signal to determine the amount of current to feed to the negative rail.

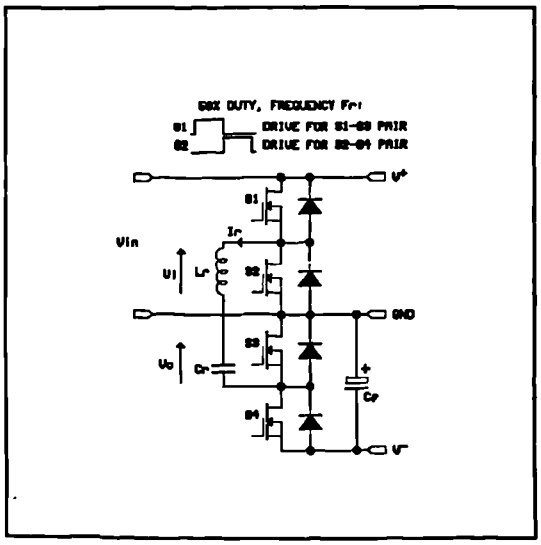

Figure 154 Schematic of proposed resonant split-rail drive.

The system is organized such that the frequency at which the switches operate is the same as the resonant frequency, f_r, of L_r and C_r in **Figure 154**. Consider the time period when S1 and S3 are closed. The schematic now appears as **Figure 155** where R is the lumped e.s.r of the capacitor, d.c. resistance of the inductor and on-resistance of the switches. Assuming R to be negligible, and if the initial voltage V_{cop} on C_r is less than the value of the positive rail voltage, then the resonant circuit current will form a sinusoidal pulse, starting at zero and ending at zero - if f_r is equal to the switching frequency the pulse will end at the instant that the S1-S3 pair open and the S2-S4 pair close. During this period the capacitor voltage will increase as a cosine function starting at V_{cop} and increasing to $2V^+-V_{cop}$

At the end of the S1-S3 on time, it can be seen that the resonant capacitor has charged up to a value higher than that of the positive rail, while the current through the series-resonant chain has fallen to zero. This is the first of the advantages of the system to be noted - zero current operation of the switches is employed thus eliminating switching losses which would certainly figure in the up/down converter approach.

At this point in time, the switch pair S2-S4 close, reducing the schematic of **Figure 154** to that of **Figure 156**. The initial voltage on the capacitor is now $V_{con}=2V^+-V_{cop}$, and the current through the resonant chain once again rises sinusoidally, although this time in the opposite direction. The current charges up the negative rail filter capacitor and supplies any current demand from the negative rail. The voltage across the resonant capacitor now falls as a cosine function

to a value less than the value of the negative rail; this value forming the starting value V_{cop} for the next cycle. The overall timing of the system with the expected waveforms is shown in **Figure 157.**

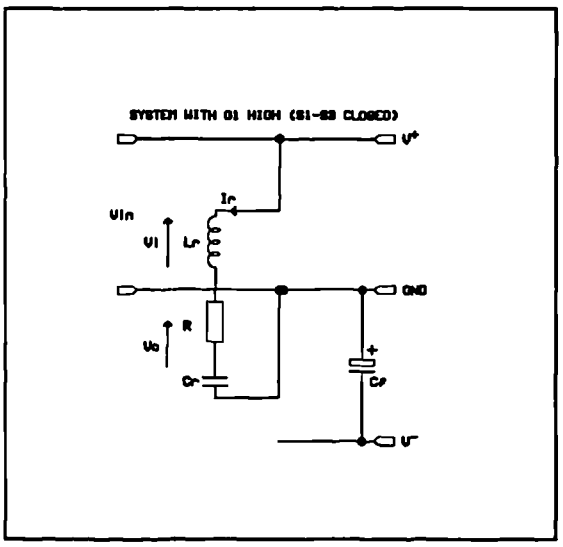

Figure 155 Resonant rail invert drive with S1 and S3 closed

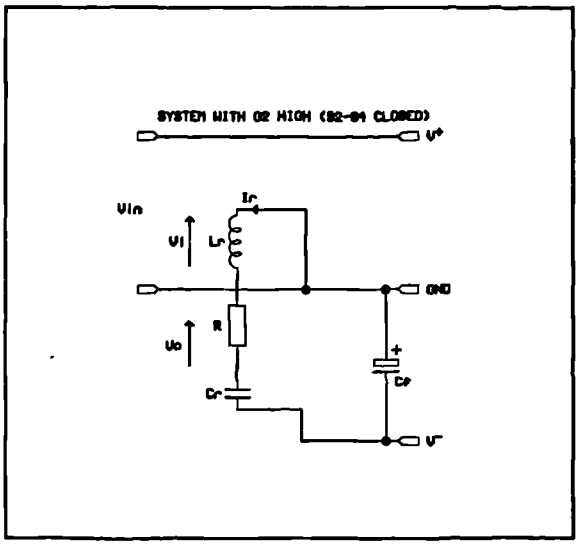

Figure 156 Resonant rail invert drive system with S2-S4 switch pair closed.

The first point of interest is that if the two rail voltages are equal and opposite, the starting voltage on the capacitor does not change. This implies that the resonant current fed to the negative rail during the S2-S4 on-time meets the demand from the inverter exactly, and therefore the rail voltage does not change.

Consider now if the inverter demands a step increase in load current from the negative supply. The negative rail voltage will drop as current is drawn from the filter capacitor C_f. The result is that the initial voltage V_{cop} will increase with sucessive cycles and this in turn implies that the current fed to the negative rail will also increase. This increase will continue above the

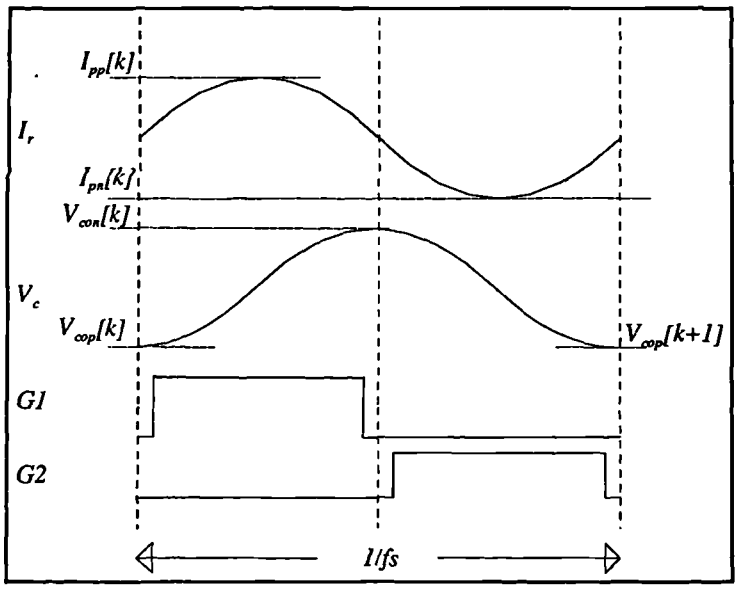

Figure 157 Basic timing of resonant split rail generator.

point at which the current demand from the negative rail is met to a point where the rails are once again equal in magnitude. The system thus displays integral action which will result in zero error in the steady state. Providing that this integral action is fast enough, it would therefore be expected that the tracking of the positive rail by the magnitude of the negative rail will be very good. It can be shown that the initial voltage on the capacitor follows: (assuming R to be negligible)

$$V_{cop} = 2f_s \int (V^+ + V^-) dt \tag{71}$$

where f_s is the switching frequency, providing that $1/f_s$ is small in comparison with any time constants associated with the load current and the value of C_f.

Since the current fed to the negative rail by the inverter is a function of the initial voltage on the capacitor at the start of the negative half cycle as well as the negative rail voltage, it can be seen that the system possesses a form of internal feedback. The analysis in Appendix C shows that transfer functions can be derived for the split-rail generator relating the negative rail voltage to the current drawn from the negative rail by a load. From these transfer functions a flow diagram can be constructed for the system and this is shown in **Figure 158** where I_{out} is the output current, V_{neg} is the negative rail voltage, I_{peak} and I_{avg} are the peak and average values of the current flowing in the resonant arm, V_{con} is the voltage across the resonant capacitor C_r at the start of the S2-S4 on-time and:

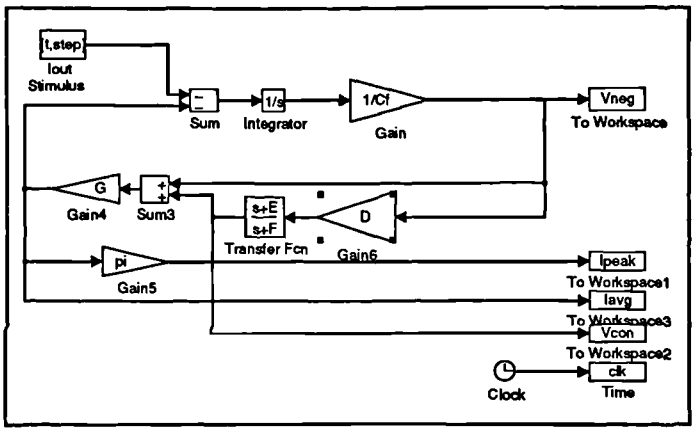

Figure 158 Flow diagram of resonant split-rail supply

$$\omega = \sqrt{\frac{4L - R^2C}{4L^2C}}\ ,\ A = e^{\left(\frac{R\pi}{2L\omega}\right)}\ ,\ D = \frac{A(1+A)}{1+A^2}\ ,\ E = \frac{2}{T}\ ,\ F = \frac{2(1-A^2)}{T(1+A^2)}\ ,\ G = \frac{C}{\pi} \tag{72}$$

The flow diagram of **Figure 158** incorporates the effect of R, and the feedback loop can clearly be seen. It is this effect that allows the system to provide a degree of regulation of the negative rail voltage. The symmetry of the system allows it to perform bidirectionally, in other words if an inverter is connected as a load which is in turn supplying a reactive load resulting in current being returned to the negative rail as opposed to being drawn from it, the energy returned to the negative rail will in turn be returned to the positive rail subject to the same dynamics as for a load drawing current - that is to say that the regulation will not be compromised.

The advantages of the system are as follows. Good rail tracking is provided across all inverter loads (even high crest factor), with a positive rail current profile which is much more amenable to correct operation of the maximum power tracker. The components, in comparison with the up/down scheme are a lot smaller, particularly the inductor which no longer has to carry low-frequency components of current. No control is required, simply two antiphase 50% duty cycle waveforms with a small deadband between them.

The disadvantages of the system, however, is that four switching devices are required, and high peak currents have to flow through the switches and resonant components. Current from the positive rail can only flow, with a sinusoidal shape, during half of the available time, the other half being spent passing that energy in to the negative rail (and vice-versa for regeneration). Peak currents will thus be high. If, for example a peak negative rail current I_n of 6A is required, this is drawn from the positive rail in a series of half-sinusoidal pulses, each with a peak value of πI_n, which in this case will be 18.84A. The capacitor and inductor must be able to handle this current without the inductor saturating, or the inductor and capacitor overheating.

The transfer functions for the system follow a standard second-order pattern, and as such it can be anticipated that the system may display a decaying oscillatory response. It is incapable of becoming unstable, but the maximum amplitude of the resonant arm currents and voltages may be of interest in terms of rating components. For correct operation of the system the resonant frequency of L_r and C_r must be equal to the switching frequency. The analysis of Appendix C suggests that the peak current in the resonant arm is a function of $\sqrt{(L_r/C_r)}$, and that increasing

C_r while adjusting L_r to maintain the same resonant frequency would cause the peak current to fall. However, the net effect, as shown by the analysis, is to trade off the rail tracking for lower peak currents - the current fed to the negative rail by the resonant system would be lower for a given rail imbalance. The integral action of the system would cause the initial voltage on the capacitor at the start of each resonant cycle to rise until the demand for current was met: the peak current would remain unchanged. There is thus a trade-off between the size of C_r (and indirectly L_r), the degree of rail tracking and the peak voltage across C_r. The selection of the type and value of C_r is a function of these parameters.

The degree of variation of the negative rail voltage is influenced additionally by the value of C_f - there will be less 'bounce' on the rail the higher the value of C_f. In this system, in the interests of symmetry it is desirable for the negative rail filter capacitor to be equal in value to that of the positive rail - and this is set at 1000μF by the design of the front-end (the analysis in Appendix C uses a value of C_f of 1500μF as when this work was carried out, a 1500μF capacitor rated at a suitable voltage was available - the effects of the reduction in value do not appear to cause a significant problem and results will be presented within this section from a system simulated with 1000μF capacitors).

The switching frequency indeed has very little effect upon the characteristics of the system other than to fix the product of L and C - its presence in the transfer functions and hence in **Figure 158** is due to the use of bilinear transforms to implement a conversion between the discrete and continuous domains, and if the time constants in the system are much lower than the period of the switching frequency its effect will be negligible.

The main effect of R is in the amplitude of the currents flowing in the resonant arm, and in turn it has quite a significant effect upon the dynamics of the system as a whole. As R is increased a point is reached above which the split-rail generator will lose its properties, and this occurs at the point at which the current in the resonant arm ceases to be sinusoidal. From this point of view, together with any consideration of dissipative losses in the system, R should be kept as low as possible. However, low values of R also result in the overall dynamics of the system

being less damped, and the transient response of negative rail voltage, resonant arm current and voltage to negative rail current demand will exhibit ringing of a higher amplitude, with correspondingly higher peak values. It is thus desirable to retain sufficient resistance in the resonant arm to allow a sufficiently damped response, while not allowing it to be so large as to significantly increase losses, or prevent the system from functioning. Some resistance is in the system is unavoidable, such as switch on-resistance and inductor d.c. resistance.

During the early development and simulation of this system using Saber, before the detailed mathematical analysis had been carried out, values of L_r of 24.3μH and C_r of 2.6μF were used, giving a resonant frequency of 20.023kHz. Once the analysis was completed, some numerical analyses were run using the expected worst-case load transition expected from an inverter. The results are presented in Appendix C as a set of graphs showing the maximum values of resonant circuit voltages and currents for different values of L/C and R. In the light of these, together with the Saber simulation results of the resonant rail drive with these values presented in Appendix C it was decided to retain these values of L and C, and if necessary, to adjust R to improve the response.

5.5 Inverter filter and switching parameters

The switches in the inverter section switch on alternately at a duty cycle of δ with a small deadband to prevent shoot-through effects. The filter at the output of the inverter reconstructs the sinusoidal voltage and current from this modulated signal. This is a pulse train alternating between 400V (V^+) and -400V (V^-), and the output voltage after one switching cycle can thus be calculated from :

$$V_o = \delta(V^+) + (1-\delta)V^- \tag{73}$$

or alternatively, the duty cycle can be found for a given output voltage from:

$$\delta = \frac{V_o - V^-}{V^+ - V^-} \tag{74}$$

Therefore the output voltage is a function of δ and the rail voltages. If the rail voltages are the same, the output voltage is proportional to δ-0.5 since at a duty cycle of 0.5, with both the rails equal in magnitude, the output voltage will average out at zero.

A filter is required to remove the high frequency components of the switch output waveform: this filter needs to provide significant attenuation at the switching frequency. Ideally it should attenuate at frequencies much lower than this in order that any control algorithm does not violate the Nyquist criterion; it should provide a sufficient degree of attenuation at and above half the switching frequency. In this application a single second-order section formed by a single inductor-capacitor pair will be sufficient. A higher order filter would prove difficult to use due to the larger group delays associated with such an arrangement causing the controller algorithms to become difficult to stabilize.

5.5.1 Filter inductor.

This is selected from Lenz' Law using a peak current ripple requirement. Assuming both DC bus voltages are identical in magnitude, the basic equation is thus:

$$L = \frac{V^{+}.t_{on}}{I_{ripple}} \qquad (75)$$

I_{ripple} can be anything up to 40% of the full load current. Maximum ripple occurs when the duty cycle is 50%, i.e. when the output voltage is zero hence t_{on} may be easily obtained as one half the switching cycle time. This inverter is to be rated at 1kW r.m.s and thus the peak load current is 1.414x(1000/240)=5.89A. Using a switching cycle time of 20kHz (identical to the front end to keep the timing simpler) from (75), the filter inductor was calculated to be 4.13mH at a ripple current of 2.4A.

5.5.2 Filter capacitor.

The filter capacitor is present to reduce the voltage ripple on the output. It must not be too large otherwise a considerable amount of reactive power will be circulated within the inverter. This inverter was designed to have a very low voltage ripple output to minimize unwanted harmonics on the voltage waveform as well as ripple in the current flowing into the load. Voltage waveforms in the simulation studies will also be cleaner and easier to analyze. The worst-case voltage ripple was arbitrarily set at 2V and the capacitor value can be calculated from:

$$C = \frac{I_{ripple}}{8fV_{ripple}} \qquad (76)$$

The switching frequency is 20kHz and the current ripple of 2.4A, and the maximum voltage ripple is calculated as 5% of the peak output voltage (17V) Substituting the values into **(76)** gives a capacitor value of 7.5μF. In the practical system this was rounded up to the conveniently available value of 10μF.

5.6 Inverter control approach

The front-end is self contained. During operation the output voltage will be fixed at 400V unless sufficient power is drawn from it to engage the maximum power tracker whereupon the bus voltage will drop and the front-end will assert a logic signal which indicates that the maximum power tracking system is operational (MPP_ACTIVE).

To drive dead AC loads, the inverter must operate in a fairly conventional manner. A voltage loop can ensure the regulation of the inverter output voltage, and below the maximum power point the front-end controller will look after the DC bus regulation.

When supplying a live AC load, or when a dead AC load is large enough to draw maximum power, the inverter controls will differ from the conventional. The output voltage is no longer a main concern being fixed by the utility, or allowed to drop if a dead load is being driven.

The required scheme in the maximum power mode is that the inverter current must be regulated so as to place the operating point of the front-end above the maximum power transition point, but below the point at which efficiency starts to drop (**Figure 159**).

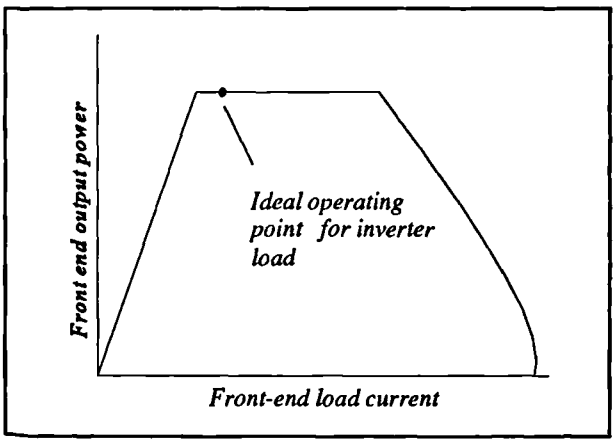

Figure 159 Ideal operating point on front-end output power characterisic.

To allow this, the inverter controller must use some type of current mode control where the inverter output current is proportional to a current input demand. Depending upon the region of operation this input is from one of two possible sources. While operating below the maximum power point into dead loads the input can be from a voltage loop. In maximum power tracking mode the current demand signal is generated by an integrator and a 'window' comparator. The window comparator tests two conditions. The first is the state of the MPP_ACTIVE flag from the front-end, the second is the value of the DC bus voltage. If the MPP_ACTIVE flag is not asserted the output of the window comparator is positive, and the integrator ramps upwards increasing the inverter output current and hence output power. If the DC bus voltage drops below a predetermined limit the output of the comparator is negative and the integrator ramps downwards reducing the inverter load current. If the MPP_ACTIVE flag is set and the DC bus voltage is above the limit the comparator output is zero and the integrator output does not change state, holding the inverter output current constant. The first condition ensures that the system operates always within the maximum power region, the second

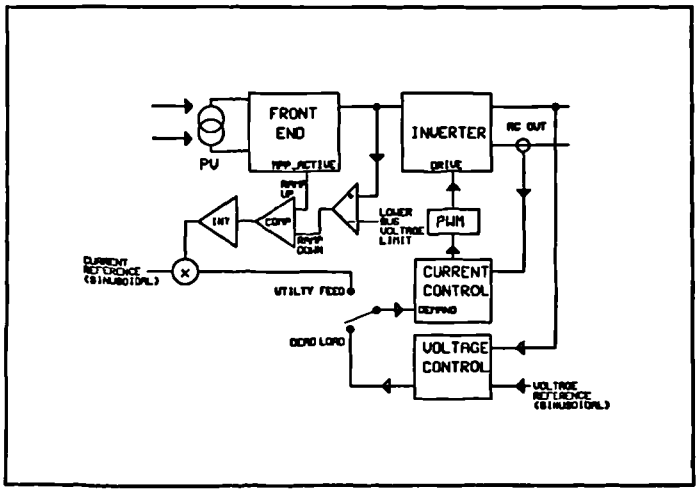

Figure 160 Block diagram of proposed inverter controller.

condition prevents operation in the regions of poor efficiency of the front end. A block diagram of this scheme is shown in **Figure 160.**

5.7 Current-mode controller

With the requirement for current-mode control of the inverter in order that under conditions of maximum power operation it can appear as a current source, two algorithms were experimented with. The first of these, average current mode control, is identical in operation to the average current mode control used in the front-end although a sinusoidal reference is used [49], [50], [51]. The second of these algorithms, the predictive current mode scheme, is much faster and inherently superior to average current mode control. This scheme, with a feedforward arrangement, was that which was used in the final system.

5.7.1 Average current mode control of inverter.

Average current mode control of an inverter is fundamentally the same as average current mode control in a DC system such as the front end. Classical control techniques are used throughout. An inner current loop, suitably compensated, regulates the average inductor current, where the input to this loop forms a current demand signal. To regulate voltage, a further loop can be closed around the current loop and a sinusoidal voltage reference at the required amplitude and frequency used as input. **Figure 161** shows the basic structure of the scheme.

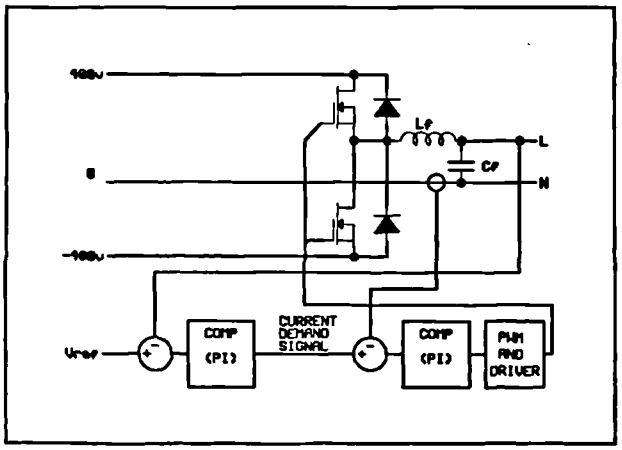

Figure 161 Basic average current mode control.

The problem with the scheme is one of dynamics. The dynamics of the inverter in open loop are much simpler than those of the boost converter, the transfer function of δ to inductor current consists of a single second order pole and first order zero (the characteristics of an LC

filter - there is no right-hand plane zero as with the boost converter), while the transfer function of inductor current to output voltage is a single first order pole. In spite of this, the average current mode controller is not a very robust performer when AC loads are being driven. It is desired that a 50Hz voltage reference (two loop, dead load) or current reference (single loop, maximum power mode) should result in an inverter output which accurately tracks the reference. To do this, the control must be arranged to give zero closed-loop phase shift and unity closed-loop gain at 50Hz. The requirement for one switching cycle to have been completed before the average inductor current can be calculated results in a two switching cycle delay within the feedback of the current loop as is the case with the DC converter of the front end. The result is that in order to maintain current loop stability its bandwidth must be reduced, and hence its speed. The integral action of a PI compensator ensures that there will be zero error in steady-state (DC), but this is not guaranteed for 50Hz and so to obtain the required gain and phase response at 50Hz some very careful selection of compensator parameters has to be made - and this does not allow a large margin for the generally high tolerances of power filter components. The result is a system which can not be relied upon to give a satisfactory response at 50Hz without sacrificing robustness.

Early simulation experimentation with an average current mode system was abandoned as it was indeed proving difficult to select suitable compensator parameters. A better current-mode system was employed, that of predictive current mode control which was first suggested in [53] as a proposed control method for boost rectifiers.

5.7.2 Predictive current mode control.

Predictive current mode control is basically very simple. In place of a classical feedback loop a system is established which for each switching period initially takes the value of a single sample of instantaneous inductor current taken at the start of

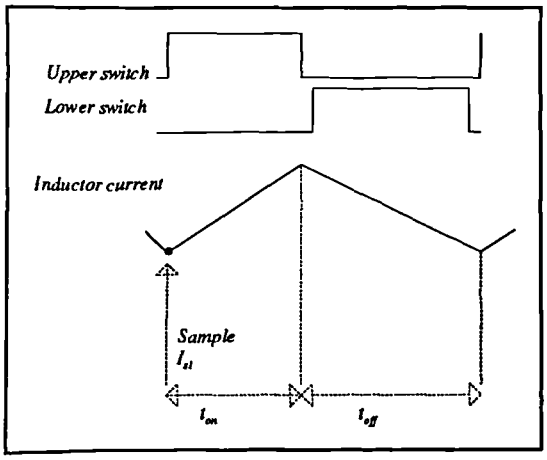

Figure 162 Sampling of inductor current in predictive control algorithm.

the current switching cycle and uses this, together with the corresponding value of δ, the known value of L and the DC bus voltages V^- and V^+ to calculate the average inductor current for the next switching cycle. **Figure 162** and equation **(77)** shows the method.

$$I_{avg} = I_{s1} + \frac{T}{2L}\left[\delta(2-\delta)(V^+ - V_o) + (1-\delta)^2(V^- - V_o)\right] \tag{77}$$

Using the value of L and samples of the DC bus voltages, the algorithm uses equation **(78)** to calculate for the next switching cycle the required value of δ to bring the initial average inductor current up to the level of the current demand signal.

$$\begin{aligned} \delta V^+ + (1-\delta)V^- &= \frac{L(I_{dmd} - I_{avg})}{T} + V_o \\ \therefore \delta &= \frac{1}{(V^+ - V^-)}\left[\frac{L(I_{dmd} - I_{avg})}{T} + V_o - V^-\right] \end{aligned} \tag{78}$$

The net result is a current mode controller which is very fast. There are no dynamics associated with a predictive mode scheme, and the transfer function of the controller reduces to a simple delay of one switching cycle. As there are no dynamics, there is no danger of the current regulator becoming unstable. Fluctuations in the DC bus voltages V^+ and V^- will not affect the algorithm as these quantities are measured on a per-cycle basis and the measured values used in the calculation, providing that the fluctuation is not so large as to preclude the generation of the required output voltage. This will happen if the bus voltage falls below the minimum voltage required by the PWM modulator. This minimum voltage can be derived from **(73)**. Assuming that the negative and positive bus voltages are equal in magnitude, and assuming also that δ is limited to a range between 0.1 and 0.9 (to allow time for the inverter parameters to be sampled) then for a maximum peak output voltage of 340V:

$$V_{rail}\Big|_{min} = \frac{V_o}{2\delta_{max} - 1} = \frac{340}{2\times 0.9 - 1} = 425V \tag{79}$$

This is larger than the anticipated 400V rail voltage. For the purposes of the simulation study it is a simple matter to decrease the limits upon δ in order to allow a 400V rail to be used,

or alternatively increase the output voltage from the front-end simply by increasing the reference voltage. In a practical implementation the limits on δ are fixed by the conversion time of the ADC devices and it is necessary thus to increase the rail voltage.

The input to the predictive current controller may be derived from a conventional PI-compensated voltage loop for voltage regulated operation, or alternatively the input may be used as a current control input in maximum power mode.

5.7.2.1 Slew rate limitation

The only main disadvantage of the predictive scheme (other than significantly more complex run-time calculations requiring a division) is that it is subject to a slew rate limitation. It is desired that the algorithm be able to change the inductor current to the demand value within a switching cycle in order for the dynamics of the system to reduce to a delay. For this to happen the rate of change of demand current between two successive switching cycles must not exceed the maximum possible rate of change of average inductor current between the two cycles.

Rewriting (78) in terms of the rate of change of inductor current yields:

$$L\frac{di_{avg}}{dt} + V_o = \delta(V^+ - V^-) + V^- \tag{80}$$

Rearranging for di_{avg}/dt gives:

$$\frac{di_{avg}}{dt} = \frac{1}{L}\left[\delta(V^+ - V^-) + V^- - V_o\right] \tag{81}$$

Now the inductor current will rise at its fastest level for a given set of bus and output voltages when δ is unity (or fall at its fastest level when δ is zero. Thus considering a rising current (for the falling current simply substitute V^- for V^+):

$$\left.\frac{di_{avg}}{dt}\right|_{max} = \frac{1}{L}\left[V^{+}-V_{o}\right] \tag{82}$$

The maximum speed at which the predictive controller can track currents is thus a function of the inductor value, the output voltage, and the bus voltage (normally fixed). Considering the output voltage rising across its range from the V^+ to V^-, the slew rate will worsen linearly as the output approaches V^+.

To consider how this limitation may affect the operation of this algorithm with respect to the mains inverter under development, it is necessary to consider the maximum possible slew rate of inductor current that may be required from the system.

If the load is linear, or live, the current drawn will be sinusoidal and the maximum slew rate, ocurring at the zero crossing, is simply given by $di/dt=\omega I_{peak}$. For a 50Hz sinusoid with an amplitude of 5.89A, the maximum slew rate will be $2x\pi x50x5.89=1850.3$ As^{-1}. At the current waveform zero crossing, the inverter output voltage will be zero for a unity power factor load giving a maximum inverter di/dt (from (82)) of $V^+/L=400/4.13x10^{-3}=96852.3$ As^{-1}. Therefore a unity power factor load will not present a problem. A zero power factor load, however, will have its current zero crossing at the peak of the voltage waveform (340V), making the inverter slew rate $(400-340)/4.13x10^{-3}=14527$ As^{-1}. As this is still greater than the maximum slew rate of the current waveform, such loads can be handled with no degradation in inverter dynamics.

Non-linear loads are a different matter. High crest factor loads (for example computer power supplies) may display high di/dt values at the instant conduction starts. The worst possible load for slewing, however, is a squarewave load (some motor drives). A squarewave load will exhibit step transitions between maximum negative peak current and maximum positive peak current, and it is necessary for the inverter to track this. It is possible to develop a relation to express the maximum amplitude of both a squarewave and sinusoidal load that can be handled by the inverter, versus its displacement in phase relative to the (sinusoidal) voltage waveform. This

enables the maximum loads for a given inductor, DC bus voltage and peak output voltage to be obtained.

The output voltage varies with angular displacement according to the relation $V_0=V_{peak}\sin\theta$. Substituting this into (82) gives:

$$\left.\frac{di}{dt}\right|_{max}=\frac{V^{+}-V_{peak}\sin\theta}{L} \tag{83}$$

The predictive control algorithm aims to bring inductor current up to the level of the demand current within a single switching cycle. For a squarewave current of amplitude I_{peak}, the maximum possible slew rate is $2I_{peak}/T$ where A is the height of a peak (zero to peak) and T is the period of one switching cycle (the minimum possible risetime in this system). For a sinusoidal load the maximum slew rate is ωI_{peak}. Thus:

$$\begin{aligned} &\textit{For sinusoidal load:} \quad I_{peak}=\frac{V^{+}-V_{peak}\sin\theta}{\omega L} \\ &\textit{For squarewave load:} \quad I_{peak}=\frac{T}{2L}\left[V^{+}-V_{peak}\sin\theta\right] \end{aligned} \tag{84}$$

It is useful to display these results graphically as a plot of maximum current waveform amplitude against displacement. From this the limits of the algorithm may clearly be seen. It is a simple matter to derive equations for any other load current waveshape, providing its derivative can be defined analytically. **Figure 163** shows the curves for the inverter under development (L=4.13mH, $V^{+}=V^{-}=400V$, $V_{peak}=340V$) across an angular displacement of -90° to +90 .° Note that, as expected, the squarewave limits are lower than those for the sinusoid. It can be seen that for

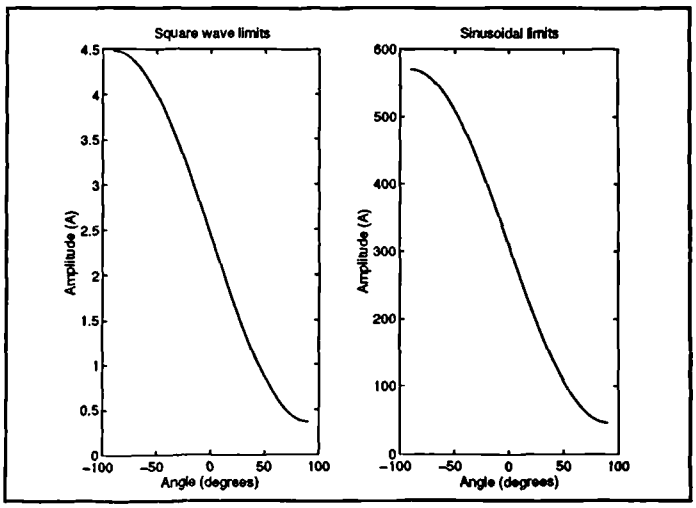

Figure 163 Slewing limits for a square and sinusoidal current load.

squarewave loads, the amplitude of the load currents may have to be limited in order to prevent a change in inverter dynamics.

The question of a step change in load such as would occur if a load was switched in at the instant of a peak in the voltage waveform has been neglected in this analysis as such a phenomenon would only occur for a single cycle and would be unlikely to compromise stability. However the results of the above analysis could be applied to such a step change in load, if desired, to show the maximum rate of change of load current before the inverter controller displays integral behaviour.

A final point to note is that in this analysis, only a rising slope has been considered - the graphs of **Figure 163** are assuming that zero displacement means that the current and voltage waveforms are in phase. The symmetry of the system ensures that for a current load waveform of the same frequency as the voltage waveform, the analysis will hold. It is interesting to note, however that at any instant in time, with the exception of the point where the output voltage is zero, the maximum slew rate in the positive-going direction is not the same as the maximum slew rate in the negative-going direction. This is brought about by the fact that the rate of change of inductor current is prportional to the voltage across it. If the output voltage is nonzero, the maximum voltage across the inverter inductor in one direction will be different to that possible in the other direction.

If the input demand current exceeds the maximum slew rate, so the dynamics of the current regulator will be altered. At the cycle following the demand change, so the algorithm will cause δ to rise to its upper limit. The inductor current can not change fast enough to supply the demand within one cycle, and so it simply ramps upwards over more than one cycle, with δ latched at its limit, until the output current enters the region of control once again. During this period, therefore, the current controller will possess integral behaviour.

This may not necessarily be a problem; where an outer voltage loop is used this should correct for this phenomenon providing that the period of integral activity does not dent the phase

margin of the voltage loop to a significant level. It could slow the system down slightly, however. When in current mode, such as when maximum power tracking is active, the problem may be greater although it is certain that the majority of loads fed under these circumstances will draw sinusoidal current, such as the utility. A designer has little control over the types of loads that may be used in the field, and therefore it is simpler to design the system with an inductor value that does not bring about a slewing problem across the anticipated operating range of the converter.

5.7.3 Filter capacitor voltage feedforward.

The basic predictive system regulates the inductor current as opposed to the output current. This is of little consequence when the system uses a voltage loop to regulate output voltage since the inductor current to output voltage transfer characteristic of the inverter (a single first order pole) is taken into account in the design of compensator parameters for the voltage loop. When a current demand is required in the maximum power mode only inductor current is regulated, and the filter capacitor will introduce some phase shift between inductor and output current which will not be corrected for. When driving the utility the feed current should be in phase with the voltage, and thus this error due to the filter capacitor must be corrected for.

A simple method would be to disconnect the filter capacitor when driving the utility, as in this case voltage ripple is not an issue. Current ripple, however may be an issue as the presence of the filter capacitor reduces current ripple into the utility. This method is crude, and would not make for ease of transition between load types (into a dead maximum power load the voltage ripple would be very high). A much better method is capacitor current feedforward and relies upon solving the current equation at the top of the filter capacitor at the input to the predictive control block. **Figure 164** shows the filter with the currents in question and from this diagram it can be seen that $I_o=I_f-I_c$. Rearranging this equation in terms of I_f gives $I_f=I_o+I_c$. Since the demand input to the predictive controller block is I_f, it is possible to solve this equation at the input to the predictive controller

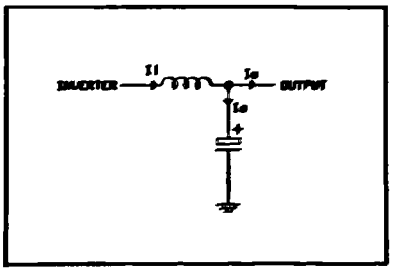

Figure 164 Inverter filter showing currents.

block and thus generate a demand input for I_o. The implementation of this is simple - the capacitor current is added to the demand signal, and the result of this calculation forms the input to the predictive control block (**Figure 165**). The capacitor current could be measured in its own right, but this would require the implementation of a further ADC channel and current probe. A simpler approach is to take a first derivative of the reference voltage, which can be obtained from the reference voltage by the simple expedient of generating a further waveform in quadrature with the main reference, and thereby calculating capacitor current from i=CdV/dt. This gives accurate feedforward information in the steady state, but results in a small error under transient conditions. The performance of the predictive scheme is good enough that the reference voltage is very close to the output voltage in both frequency and phase (it can be scaled for amplitude) and this system will work well without requiring a further current probe.

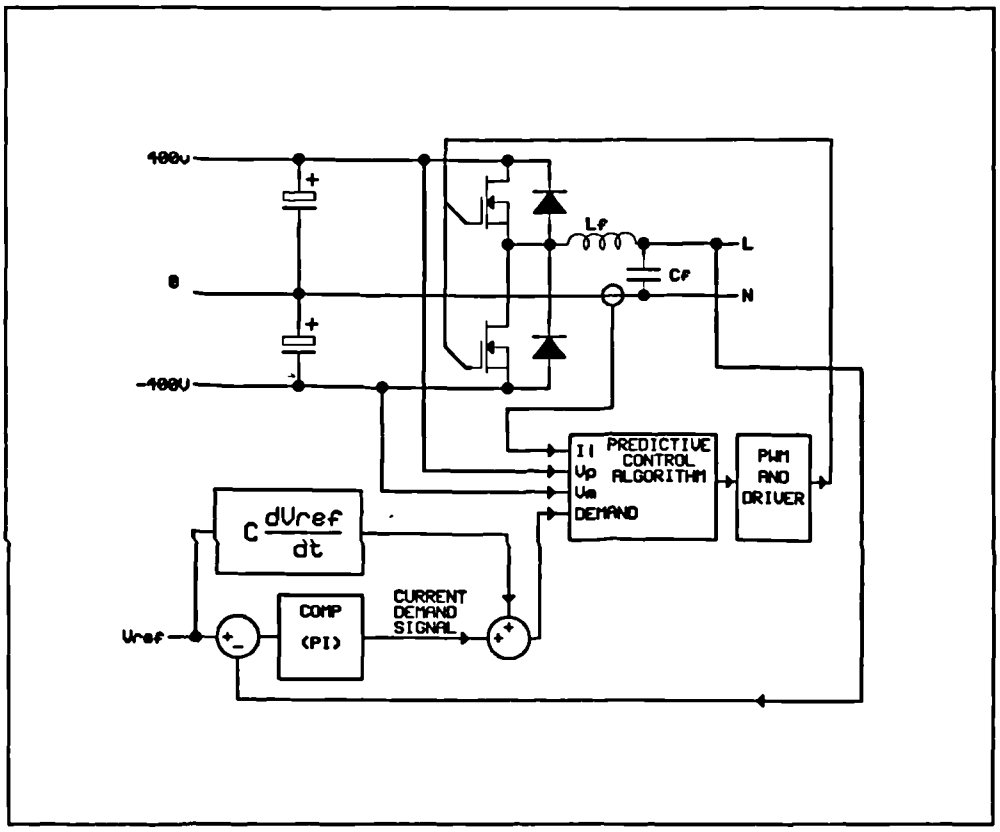

Figure 165 Predictive mode scheme with capacitor current feedforward.

Simulation studies of the system showed it to compensate very well for the capacitor current with no apparent change in inverter dynamics. Although this scheme has been applied

successfully to average current mode controllers [54] (and, in a more complex form, to [55]) to speed them up and overcome some of their shortcomings, the scheme has not before been applied to the predictive scheme. There is definitely merit in using the system, and in a digital controller the only penalty is a small amount of calculation time.

5.7.4 Load current feedforward

Load current feedforward is another example of a translation that can be applied at the input of the current loop in order to achieve an improvement in performance [56], [57]. In this case the load current is measured using a further ADC channel and the result is summed with the demand signal to form the input to the current loop. The scheme can coexist with capacitor current feedforward (**Figure 166**). The net result of the scheme is that the input signal to the current controller block is translated from a 'demand' signal into an 'error' signal, which corrects for the difference between the measured load current and the required load current. It is implicit that in steady state this error signal will be zero, and such an error signal can be directly provided by the output of a voltage loop compensator with an integral term. Thus load current feedforward can not be used if a current demand signal is what is required such as in the proposed system when a maximum power AC load is being driven. In a digital control environment the load voltage feedforward quantity is merely another variable, thus load current feedforward can be switched in and out with ease together with the voltage loop when the system is driving a live load.

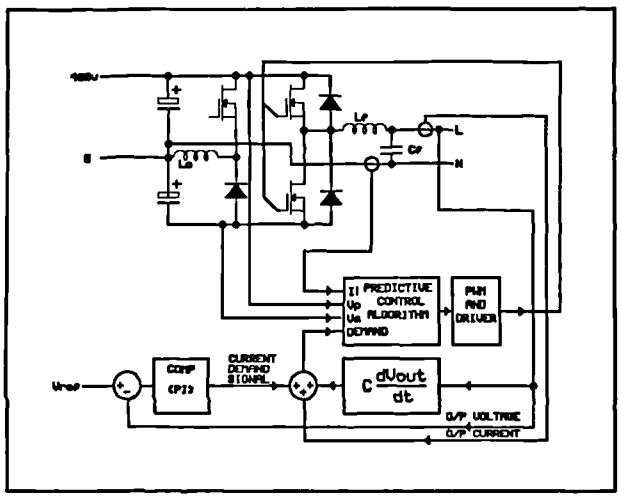

Figure 166 Predictive current mode control with capacitor current and load current feedforward.

When operating with an outer voltage loop, therefore, the addition of load current feedforward results in a considerable increase in the response speed of the current loop. This

scheme has been demonstrated with average current mode controllers again [54] with considerable success. Simulation studies of the scheme with the predictive controller showed that the main area of improvement was in the handling of loads with a high crest factor where the degree of clipping of the output voltage waveform was significantly reduced. Load current feedforward with linear loads showed a little improvement over the excellent response of the system with capacitor voltage feedforward alone although there are no disadvantages of using the scheme with such loads other than the requirement for an extra ADC channel and the very small amount of computation time. The improvement in performance with high crest factor loads could be sufficient to warrant use of the scheme since these loads form a significant proportion of the loads that may be encountered by such a system.

5.8 Implementation of simulation model

The complete inverter system was implemented in MAST through the schematic capture utility DesignStar. Full use was made of the hierarchical features of the system to facilitate rapid modification at any level without having to alter the levels above it. The controller templates for the inverter, the PV front end and the rail invert drive were written as primitives directly in MAST on a single level of hierarchy, with associated DesignStar symbols representing these sections to the schematic. Appendix B contains full listings of all the MAST code written during the development of the system.

The top level schematic for the inverter system is shown in **Figure 167**. Here the main functional blocks can clearly be seen: the previously developed PV array model followed by the

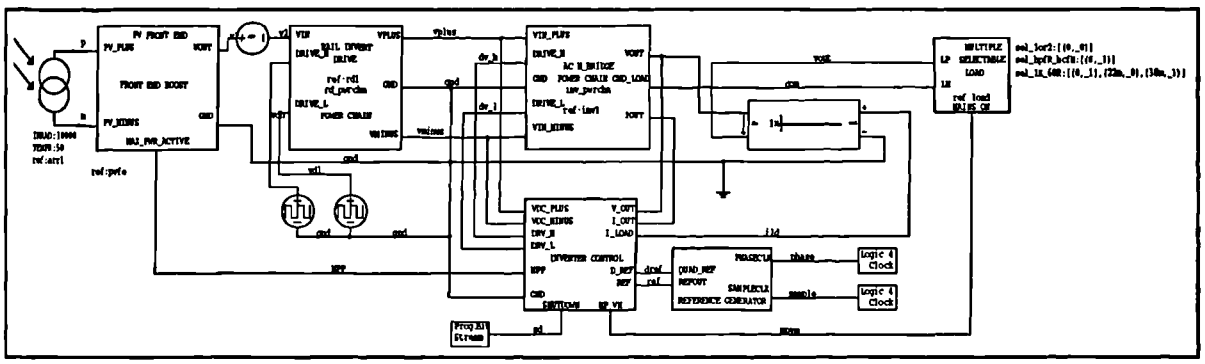

Figure 167 Top level schematic of inverter simulation model.

PV front-end driving the rail invert system and the inverter itself. The switchable loads are selectable by altering parameters to the 'multiple selectable load' block during simulation time. The 'reference generator' accepts a 20kHz and 50Hz logic clock and generates a 50Hz sinusoidal reference for the inverter controls, both in zero phase and quadrature (to enable the output voltage derivative to be calculated for capacitor current feedforward). The voltage source inserted in the positive feed to the rail invert drive system has zero amplitude and is purely a device to simplify the measurement of current in this rail.

Each of the blocks which form the schematic of **Figure 167** are now described in detail, showing the lower hierarchichal levels if appropriate.

5.8.1 Front-end boost converter block.

This block basically consists of the PV front end system as has been sucessfully developed in simulation and as a low-power prototype. The system has been rearranged (in layout alone) to facilitate use of DesignStar and Saber hierarchy. **Figure 168** shows the contents of the 'front end boost' block of **Figure 167**, while **Figure 169** shows the contents of the third-level block 'pv boost converter' of **Figure 168**. A slight modification from the original has been made to the switch drives in the sense that in this arrangement the outputs of the controller are single-ended. This has no effect upon the

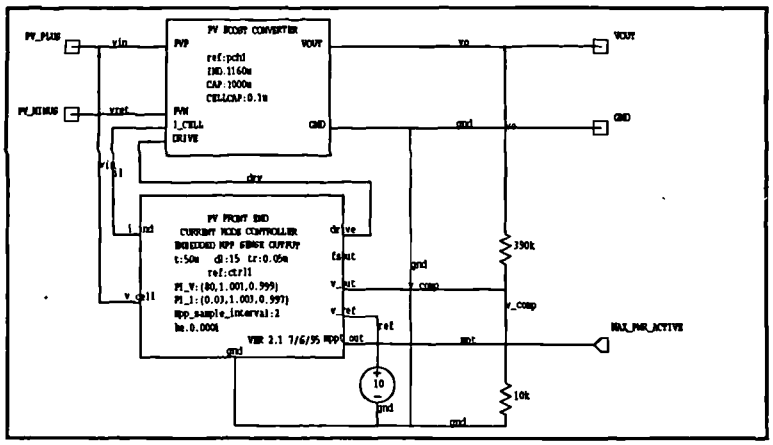

Figure 168 PV front end block.

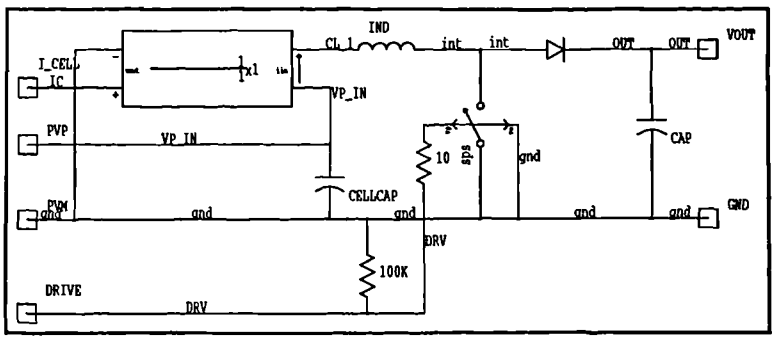

Figure 169 Power chain of PV front end.

operation of the circuit; it merely simplifies the templates somewhat. A full listing of the front end controller template is presented in Appendix B. It is the same as that previously designed with the addition of a logic output, 'mppt_out' which is asserted if the controller is operating in maximum power mode. The output divider and reference voltage together fix the DC bus at 400V while the system is operating in conventional current mode.

5.8.2 Negative rail drive.

The resonant rail drive system is shown in **Figure 170.** The switches are driven in pairs. The top switch in each leg are driven together and the bottom switch in each leg are driven together by a pair of pulse voltage sources from the Saber libraries (these are outside this template and may be seen on the top level **Figure 167**).

5.8.3 Inverter power chain and controller

The inverter power chain is basically a half-bridge (**Figure 171**). The component values used in the system are an output filter inductor (FILT_L_OUT) of 4.13mH and a filter capacitor (FILT_C_OUT) of 10μF, arrived at from the selected values of maximum inductor ripple current and output ripple voltage.

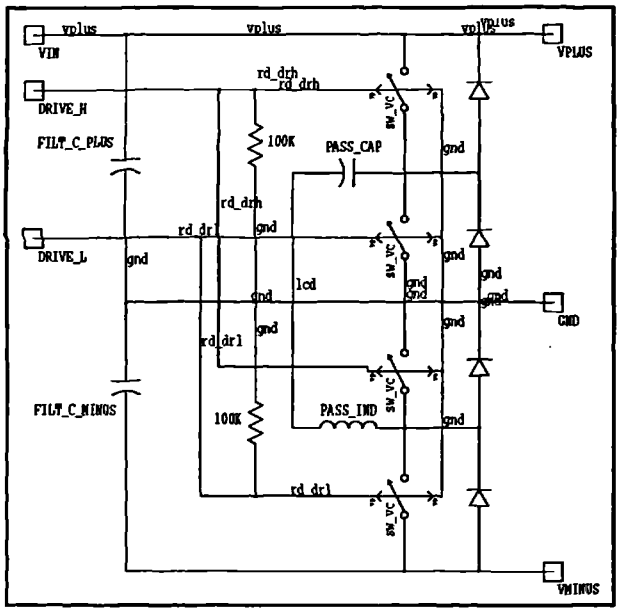

Figure 170 Resonant rail drive system

A full listing of the MAST template of the inverter control block may be found in Appendix B. The derivative of output voltage required in the calculation for capacitor current feedforward is calculated from a

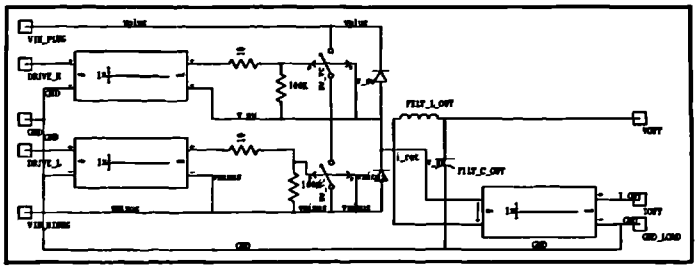

Figure 171 Inverter power chain schematic

prediction. The output voltage is sinusoidal, and therefore its first derivative will be a sinusoid in quadrature scaled in magnitude by a factor of angular frequency ω. This can be generated with ease from the refererence sinusoid, and forms a reliable method for predicting the capacitor current. The basic equations implementing predictive control are all present in this portion of the template.

The basic PWM generation section of the template is, in operation, the same as that for the front end. The only difference is that drives are required for both high and low side, and a deadband must be inserted to prevent shoot-through effects. The same structure of MAST code can be used, with duplication of some of the basic functionality, to implement this.

In addition, a shutdown feature was added to the template to allow the inverter system to be switched off. This was used during development to allow the DC bus voltages time to stablize before the inverter was switched on. A practical system would include such a facility as part of its 'soft start' algorithm.

5.8.4 Loads

The switchable load block 'multiple selectable load' in **Figure 167** was developed to allow different simulated loads to be applied to the system, and to be easily changed during a simulation run in order to simulate step changes in load value and type. The schematic of **Figure 172** shows the basic system, while **Figure 173** and **Figure 174** show the high crest factor load and the high power factor load respectively.

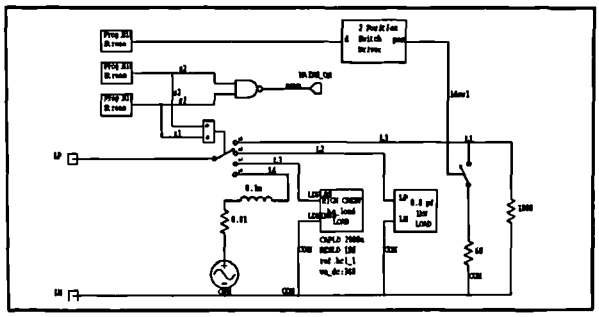

Figure 172 Selectable load schematic

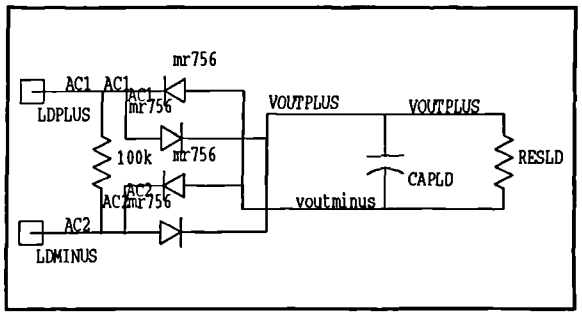

Figure 173 High crest factor load

The loads are selectable by modifying the values of the three programmable bitstreams, which control the position of the switch. The possible loads are:

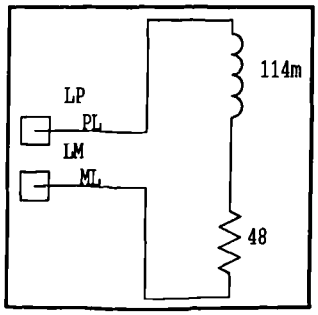

Figure 174 High power factor load

Resistive: 1K

Resistive: 60R

Reactive: 0.8 power factor

High crest factor: 2000μ/100R

Live load: 240V r.m.s.

When the live load is selected, a logic signal is asserted which simulates a 'loop in lock' signal from a phase locked loop and serves to inform the inverter controller to switch to current control. To simulate a complete line-lock phase locked loop would require a large amount of computation time resulting in a simulation which would take an unacceptable amount of time to run to completion.

5.9 Component values of final system.

The simulated PV array used in the inverter tests was a 120 (parallel) by 250 (series) cell array, irradiated at 10000 arbitrary units and at a temperature of 323K. The current-voltage characteristic of the array is given in **Figure 175**. Such an array has a maximum power point of 1800W. This is placed towards the upper limit of the design range of the converter as the greater number of the load tests on the converter will be using dead loads and for these the front-end will be operating in the constant voltage region of the array. This way a wider range of

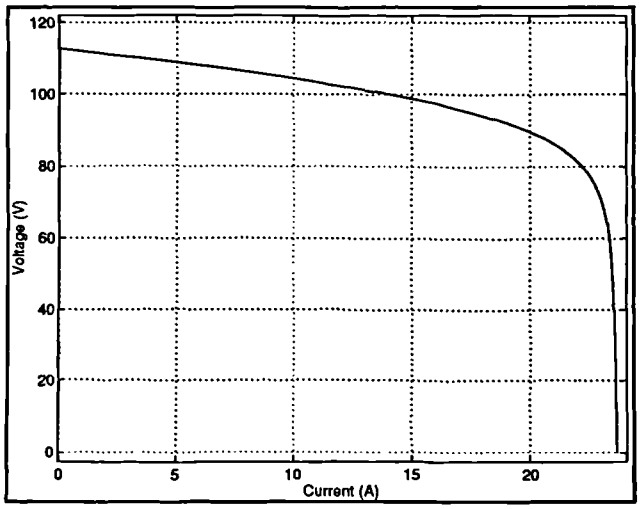

Figure 175 Current-voltage curve for array used in the inverter simulation tests.

powers in the constant voltage region is provided. Only a live load will require the front-end to continuously operate in maximum power mode. The front-end has been analyzed independently, and the emphasis in this section is to test the inverter section therefore here the array will be operated at a single value of temperature and irradiance.

The component values used in the final system are given in **Table 10.** This details all of the significant values and parameters used during the simulation run (these are not all printed in the schematic plots as they can clutter the diagrams and render them difficult to read. Most components whose values are not critical to the operation of the system (such as switch gate resistors) have been assigned fixed values at the position at which they appear.

PI compensator parameters are given in the table in the same form as which they are entered into the DesignStar symbol parameter fields, that is 'a,b,c' where:

$$H(s) = a.\frac{b-cz^{-1}}{1-z^{-1}} \tag{85}$$

See section 3.7.3 for the definition of the z-domain PI coefficients for the front-end.

Table 10 Component values used during the simulation of the complete photovoltaic power system.

Component designator		Description	Value
Front end power:	IND	Boost converter inductor	1.2mH
	CAP	Boost converter filter capacitor	1000μF
Front end control:	PI_V	Voltage loop PI compensator (a, b, c)	40,1.001,0.999
	PI_I	Current loop PI compensator (a, b, c)	0.03,1.003,0.997
	ke	MPP integrator gain	0.0001
	mpp_sample_interval	MPP sample interval	2
Resonant rail drive:	PASS_CAP	Resonant capacitor	2.6μF
	PASS_IND	Resonant inductor	24μH
	FILT_C_PLUS	Positive rail decoupling	0.1μF
	FILT_C_MINUS	Negative rail filter capacitor	1000μF
Inverter power chain:	FILT_L_OUT	Output filter inductor	4.13mH
	FILT_C_OUT		10μF

Most of the designators given in **Table 10** are brought through to the top level of hierarchy for ease of modification during the simulation run, except those associated with the front end which has been simulated previously and can be considered to be complete. The front-end has been encapsulated in a single block in the top level to enable work to be concentrated on the AC sections.

5.10 Simulation results of complete 1kW PV power conversion system.

A complete set of the simulation results for the entire inverter system with resonant rail drive are presented here. To assist in the evaluation of the effect of load current feedforward upon all types of load (except live loads where load current feedforward is not required) each simulation set was run twice, once with load current feedforward and once without. Capacitor current feedforward was used in all sets as this does not appear to significantly affect system dynamics. Four forms of load were used, resistive, high power factor (HPF), high crest factor (HCF) and live, and each of these is shown with its attendant parameter set.

The final group of curves are presented to show the effect of step load changes upon the transient behaviour of the resonant split-rail supply generator and demonstrate its viability as a means of achieving a split-rail supply in d.c. inverter feeds. The order is shown in the following sections.

5.10.1 Results of simulations of standard load groups

To simplify the analysis of the results, the curves are categorized into five main groups depending upon load type. In those groups where the effect of feedforward was investigated, the groups are further subdivided into sets, one of which corresponds to curves generated with capacitor current feedforward alone, and the other to curves generated with both capacitor and load current feedforward.

Group 1: Resistive loads.

Two values of resistance are used. From t=0 60R is used, with a 1K load being switched in at t=22.5ms and out at t=37.5ms in order to demonstrate the transient effects of a change in the value of the load.

Set 1: capacitor current feedforward only

Figure 176 (page 225): Output voltage and current.

Figure 177 (page 226): Maximum power tracking signal with voltage.

Figure 178 (page 226): Supply current envelope.

Figure 179 (page 227): Shape of supply current during negative half cycle.

Figure 180 (page 227): DC bus tracking error, resistive and high power factor load.

Set 2: capacitor and load current feedforward.

Figure 181 (page 228): Output voltage and current.

Figure 182 (page 228): Maximum power tracking signal and voltage

Figure 183 (page 229): Supply current envelope

Figure 184 (page 229): Shape of supply current during negative half cycle.

Group 2: High power factor (0.8 lag) load.

Set 1: Capacitor current feedforward only

Figure 185 (page 230): Output voltage and current.

Figure 186 (page 230): Maximum power tracking signal with voltage.

Figure 187 (page 231): Supply current envelope.

Figure 188 (page 231): Shape of supply current during negative half cycle.

Set 2: capacitor and load current feedforward.

Figure 189 (page 232): Output voltage and current.

Group 3: High crest factor load

Set 1: capacitor current feedforward only.

Set 2: capacitor and load current feedforward.

Group 4: Live loads, capacitor current feedforward only.

5.10.2 Results of simulations of transient load changes.

Group 5: Transient load changes.

Note all Group 5 transients were from a 1K resistive load to a fully-rated high crest factor load switched in at t=35ms, at the peak of the inverter output voltage waveform..

Figure 211 (page 243):	Complete transient: output voltage and load current.
Figure 212 (page 243):	Resonant capacitor voltage across complete transient.
Figure 213 (page 244):	Complete transient: load current, supply current and output voltage.
Figure 214 (page 244):	Resonant capacitor voltage at point of highest amplitude during transient.
Figure 215 (page 245):	Supply current at point of highest amplitude.

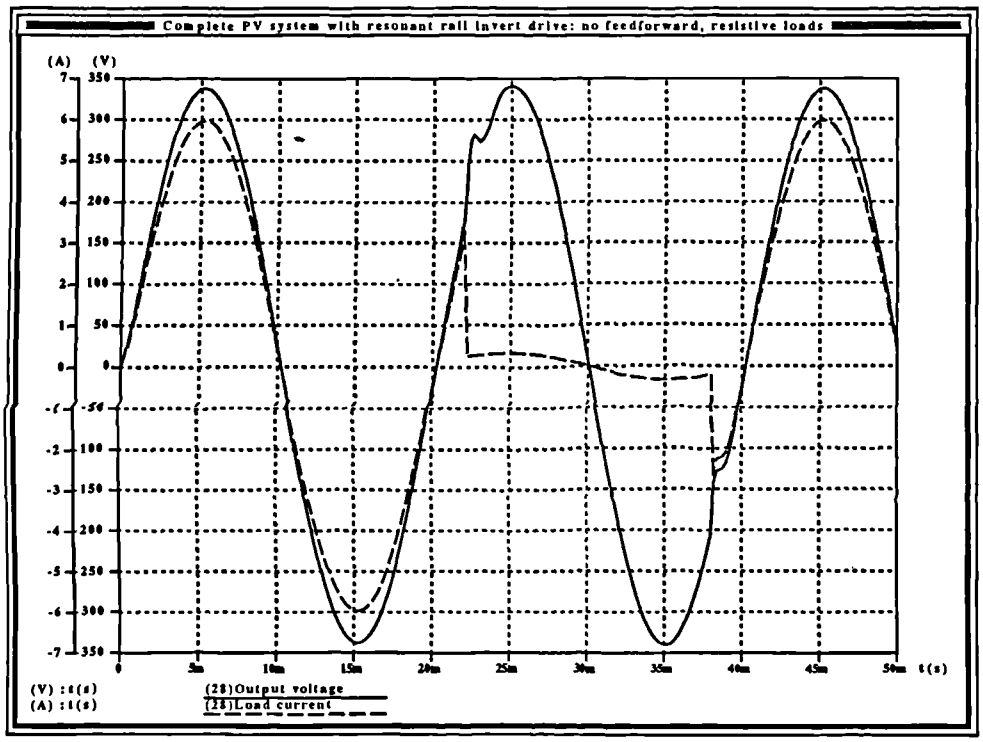

Figure 176 Group 1, set 1: Inverter output voltage and current for step load change; resistive load, capacitor current feedforward..

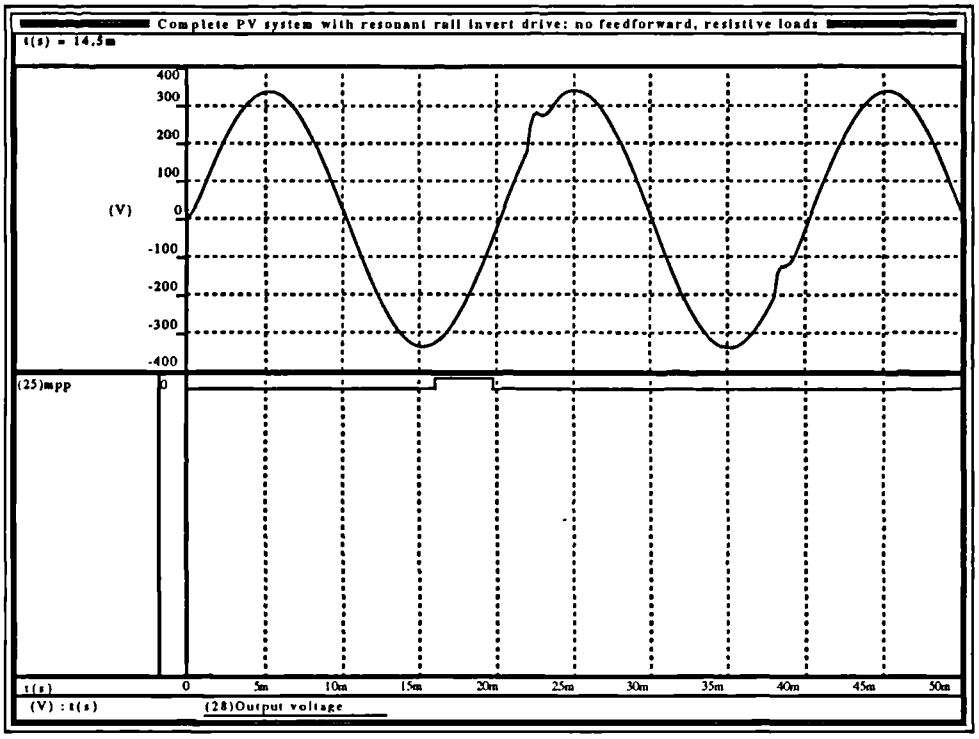

Figure 177 Group 1, set 1: Maximum power tracking signal and voltage for step load change; resistive load, capacitor current feedforward..

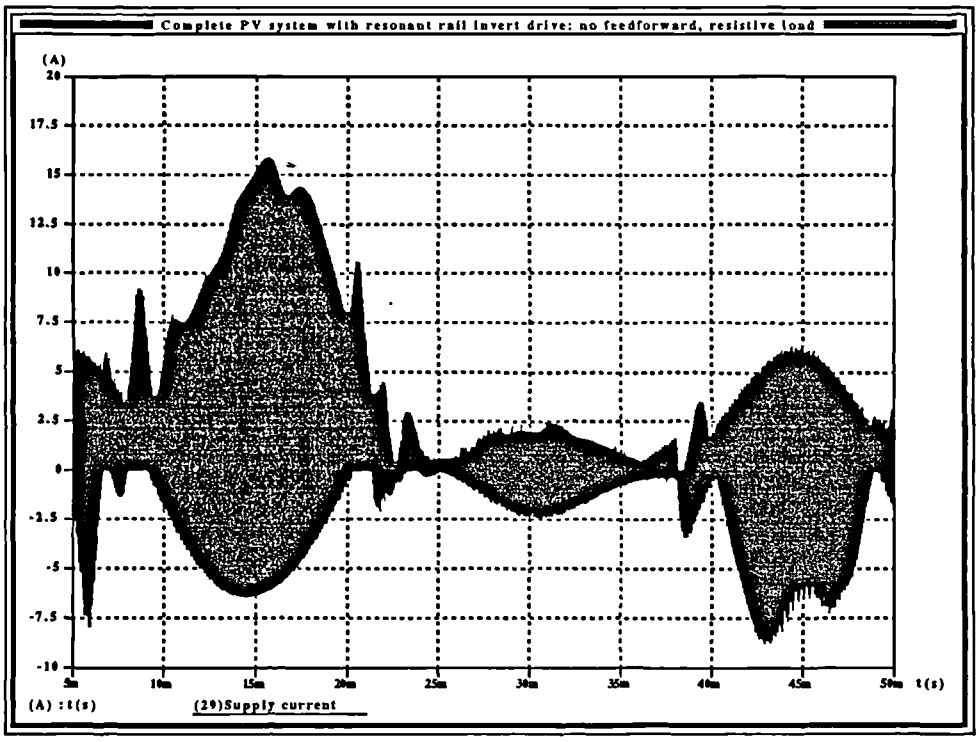

Figure 178 Group 1, set 1: Inverter supply current envelope for step load change; resistive load, capacitor current feedfoward..

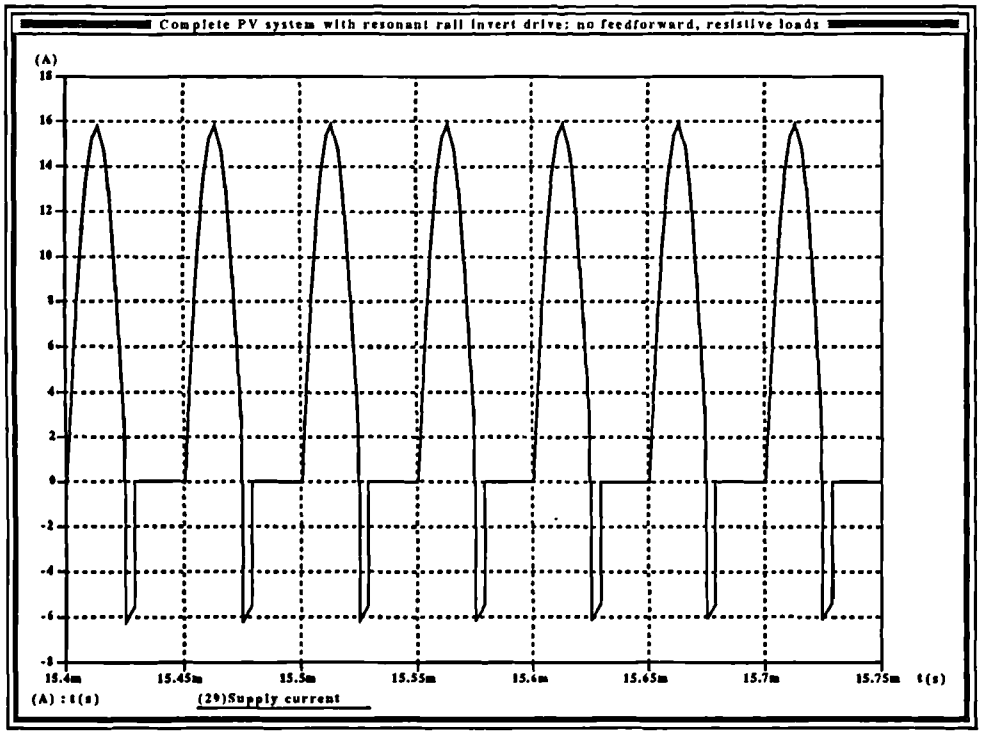

Figure 179 Group 1, set 1: Shape of inverter supply current during the peak of the negative half cycle of inverter current waveform; resistive load, capacitor current feedforward..

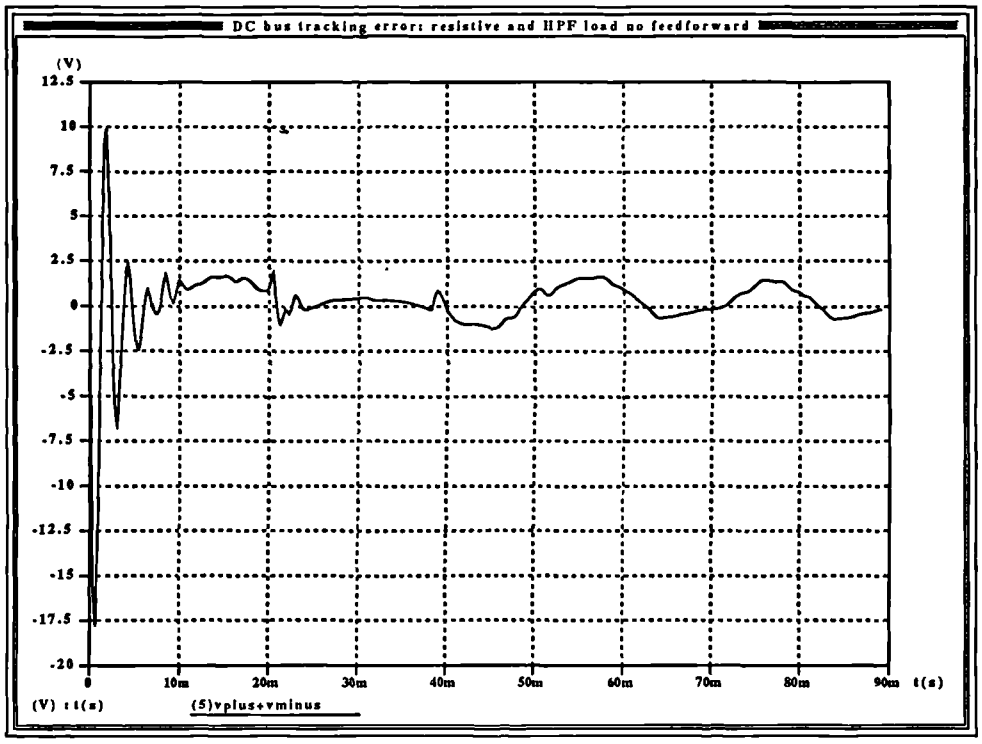

Figure 180 Group 1 set 1: d.c. bus tracking error for resistive and high power factor load; capacitor current feedforward..

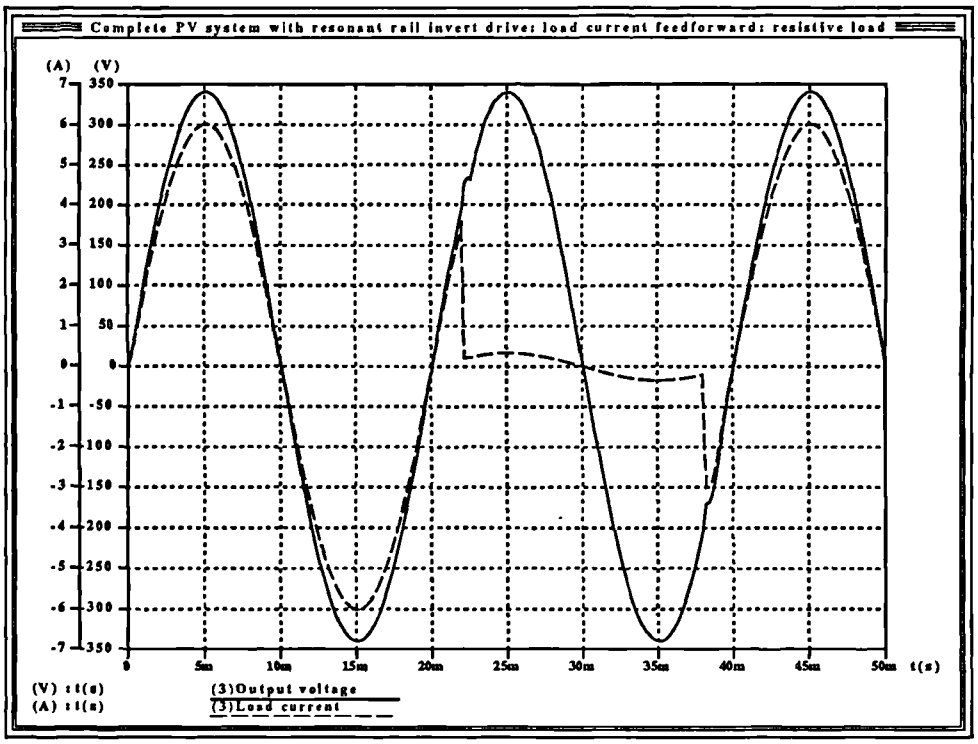

Figure 181 Group 1, set 2: Inverter output voltage and current for step load change; resistive load, capacitor and load current feedforward.

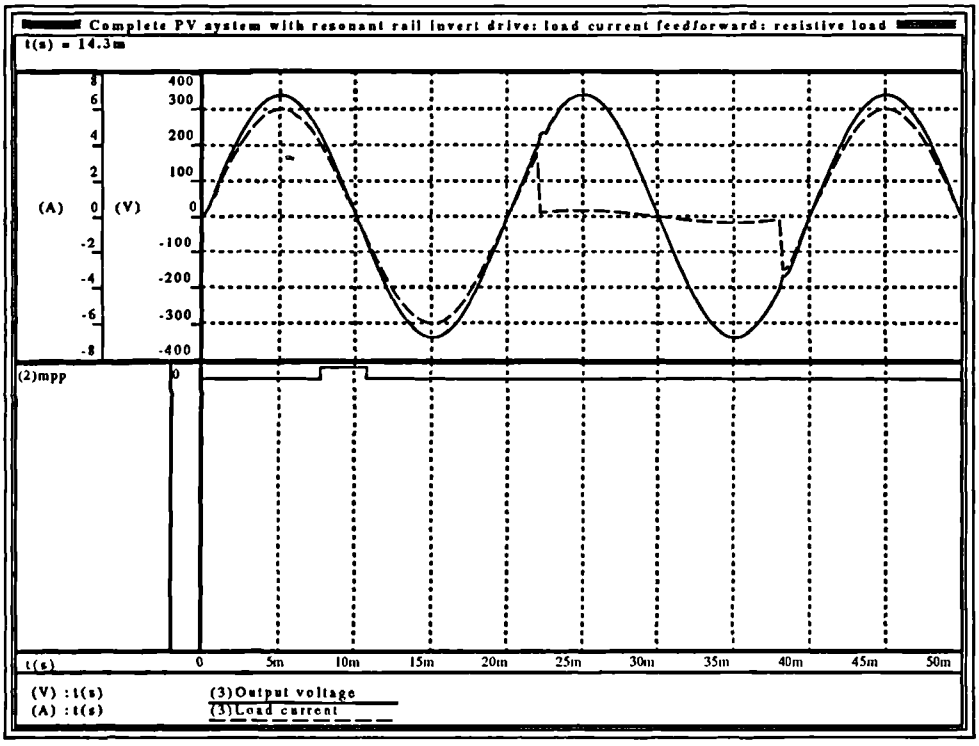

Figure 182 Group 1, set 2: Maximum power tracking signal and inverter output voltage for step load change; resistive load, capacitor current feedforward and load current feedforward..

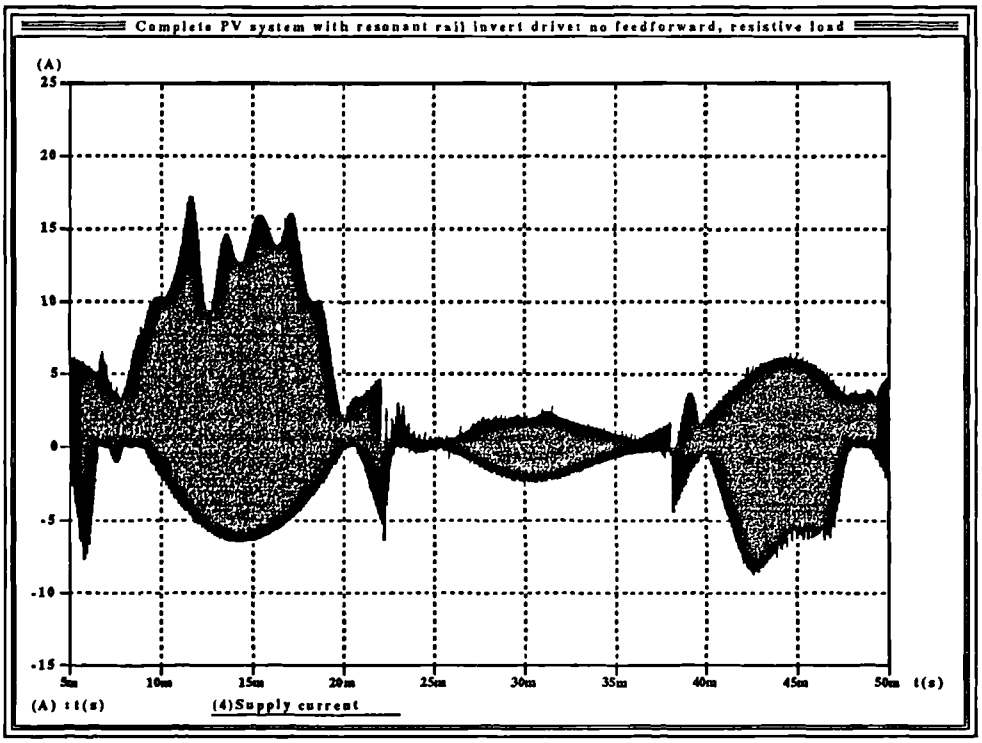

Figure 183 Group 1 set 2: Inverter supply current envelope for step load change; resistive load, capacitor and load current feedforward..

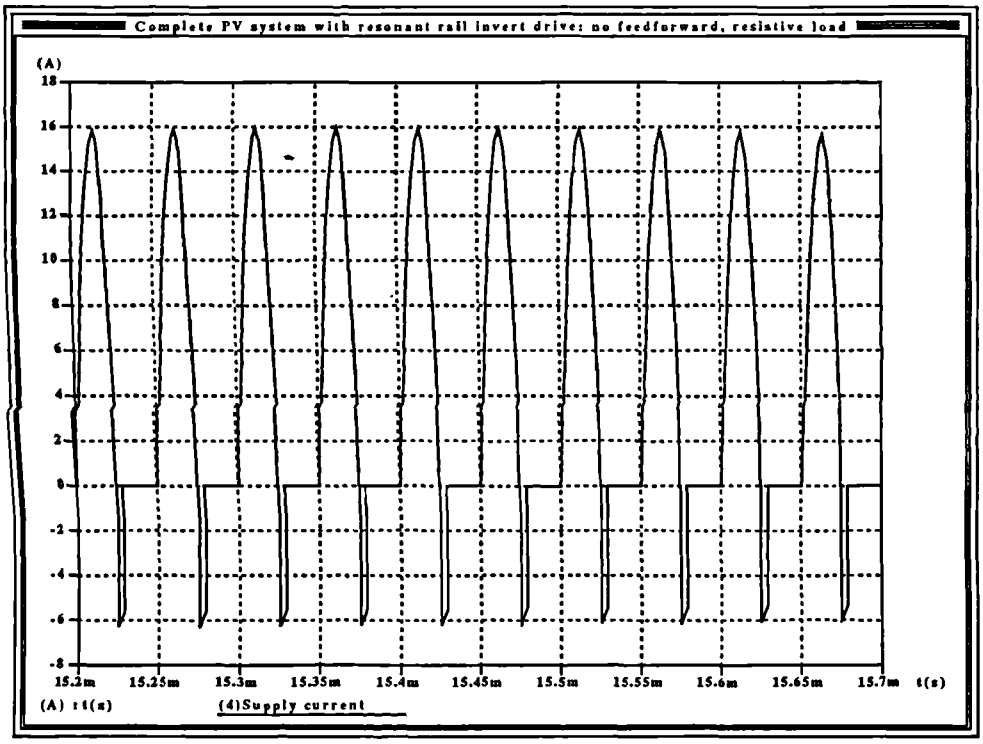

Figure 184 Group 1 set 2: Shape of inverter supply current during negative half cycle of inverter output current waveform; resistive load; capacitor and load current feedforward.

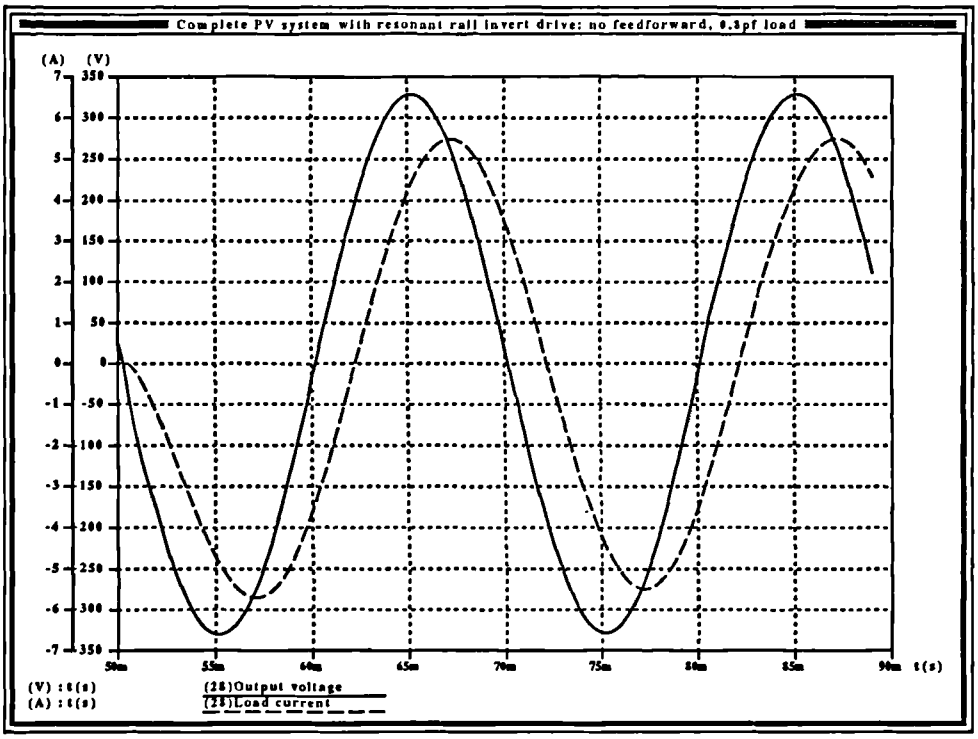

Figure 185 Group 2 set 1: Inverter output voltage and current, 0.8pf lagging load, capacitor current feedforward..

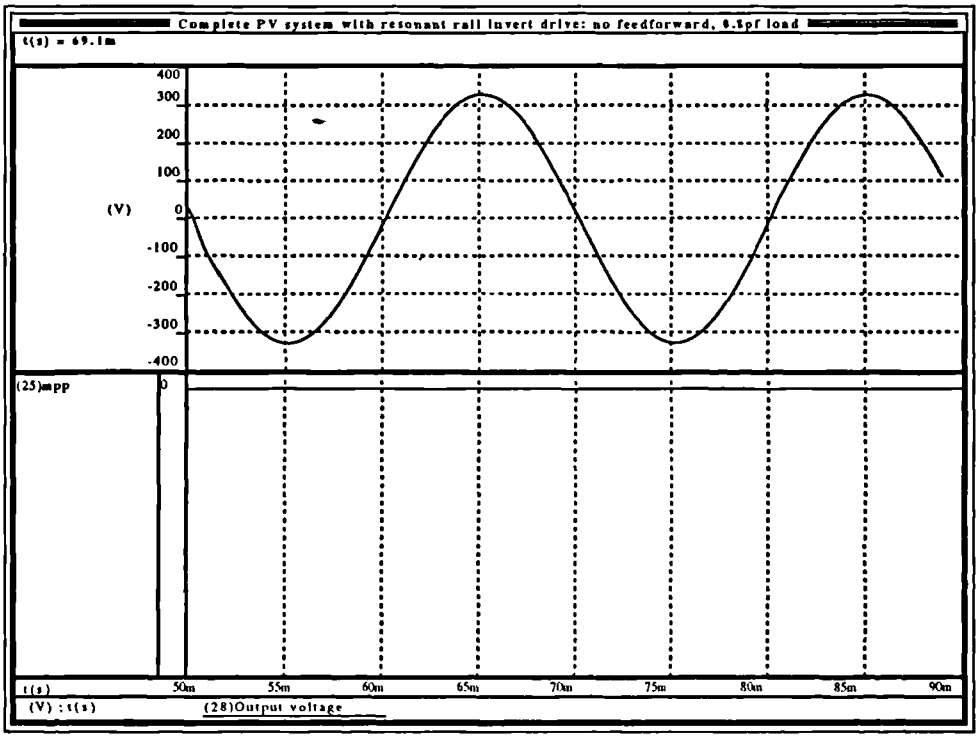

Figure 186 Group 2 set 1: Maximum power tracking signal and voltage, 0.8pf lagging load, capacitor current feedforward.

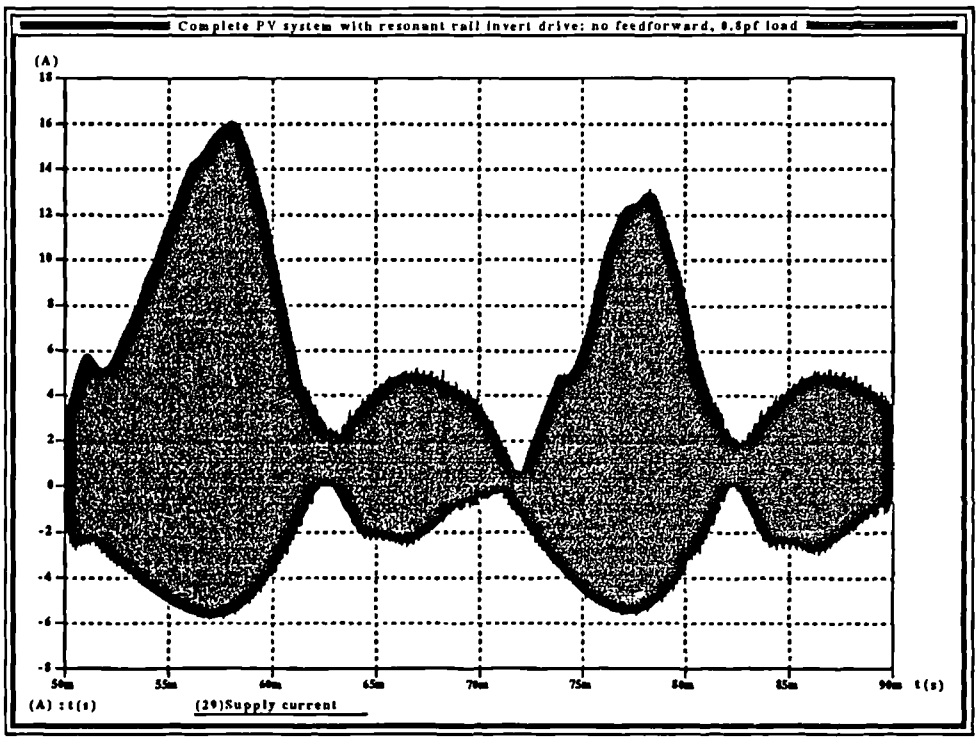

Figure 187 Group 2 set 1: Inverter supply current envelope, 0.8pf lagging load, capacitor current feedforward.

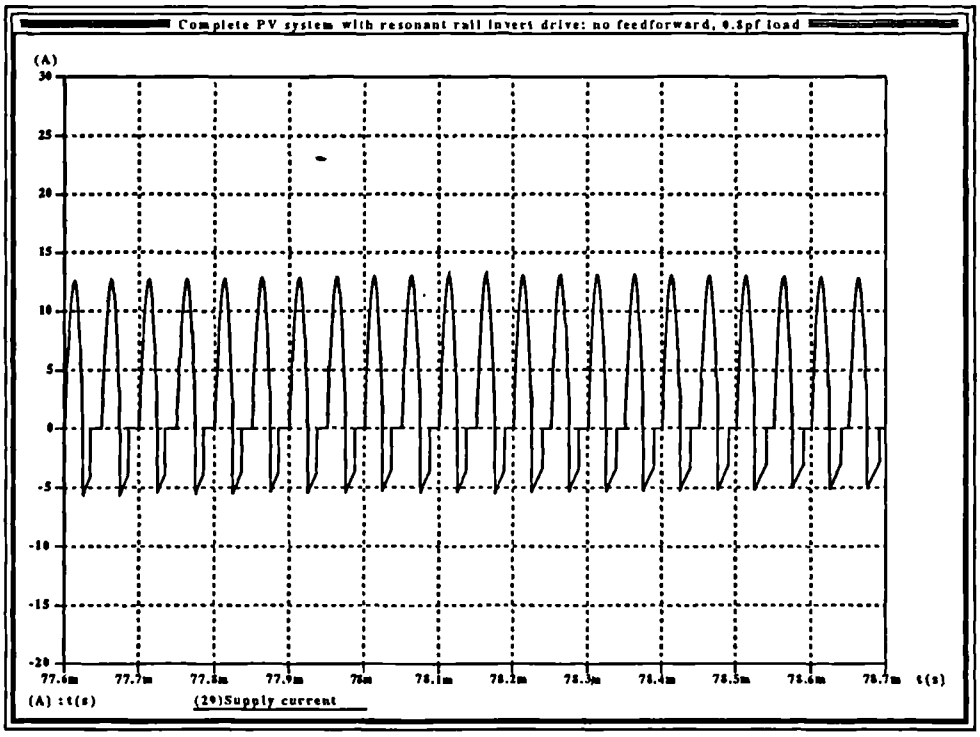

Figure 188 Group 2 set 1: Shape of inverter supply current during a portion of the negative half cycle of inverter output current waveform; 0.8pf lagging load, capacitor current feeforward..

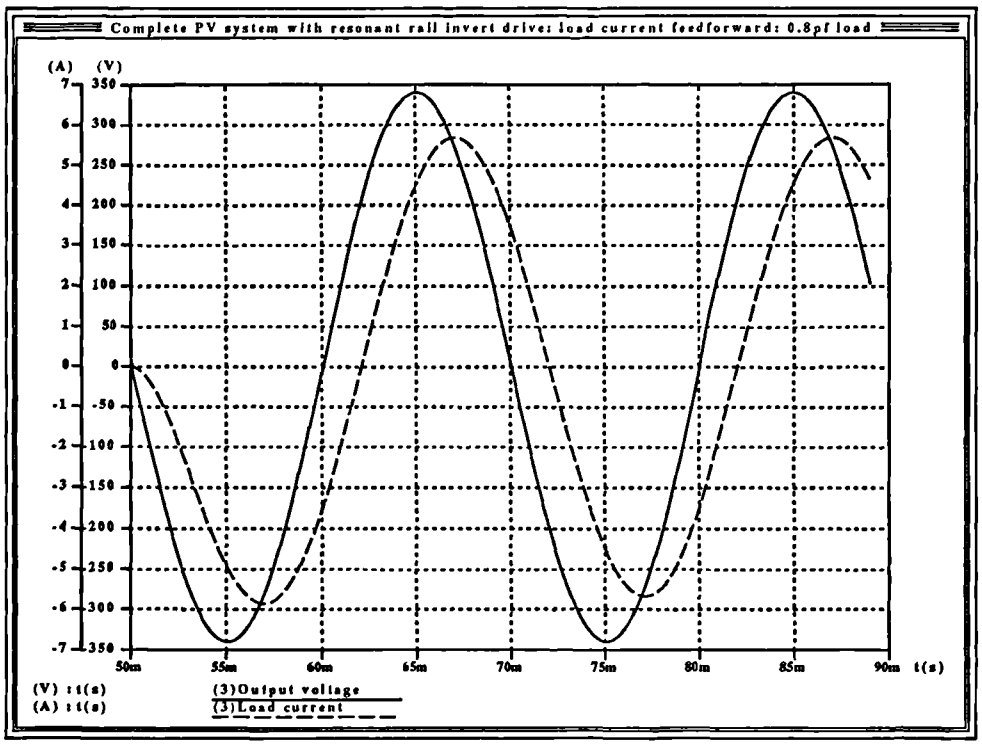

Figure 189 Group 2 set 2: Inverter output voltage and current; 0.8pf lagging load, capacitor and load current feedforward.

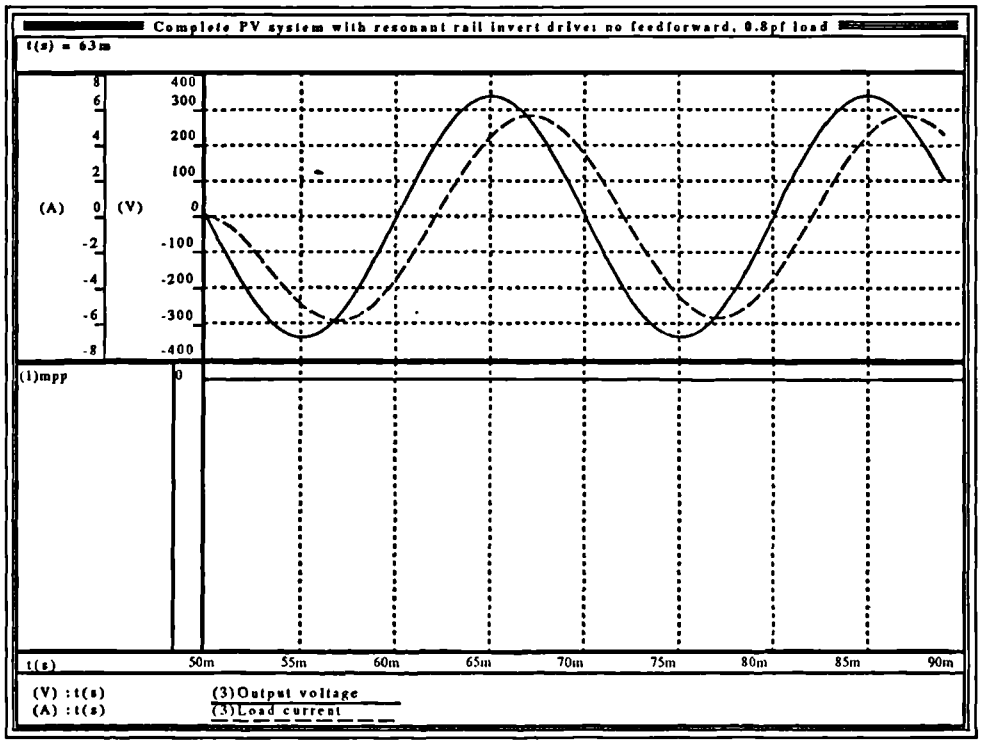

Figure 190 Group 2 set 2: maximum power tracking signal, inverter output voltage and current. 0.8pf lagging load, capacitor and load current feedforward.

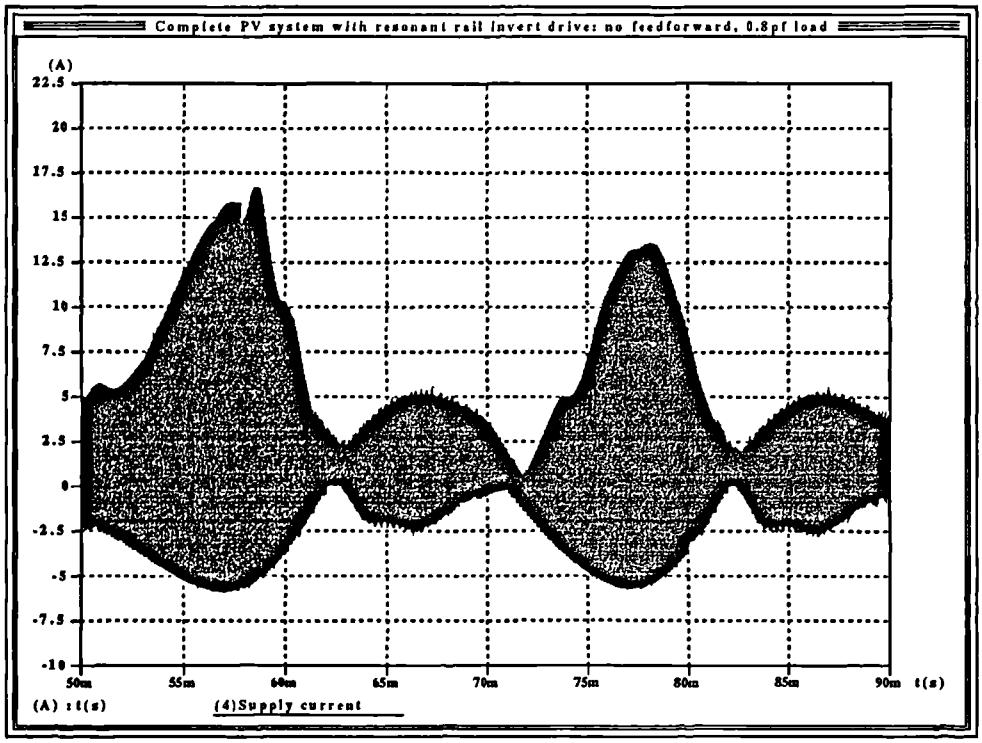

Figure 191 Group 2 set 2: Inverter supply current envelope; 0.8pf lagging load, capacitor and load current feedforward.

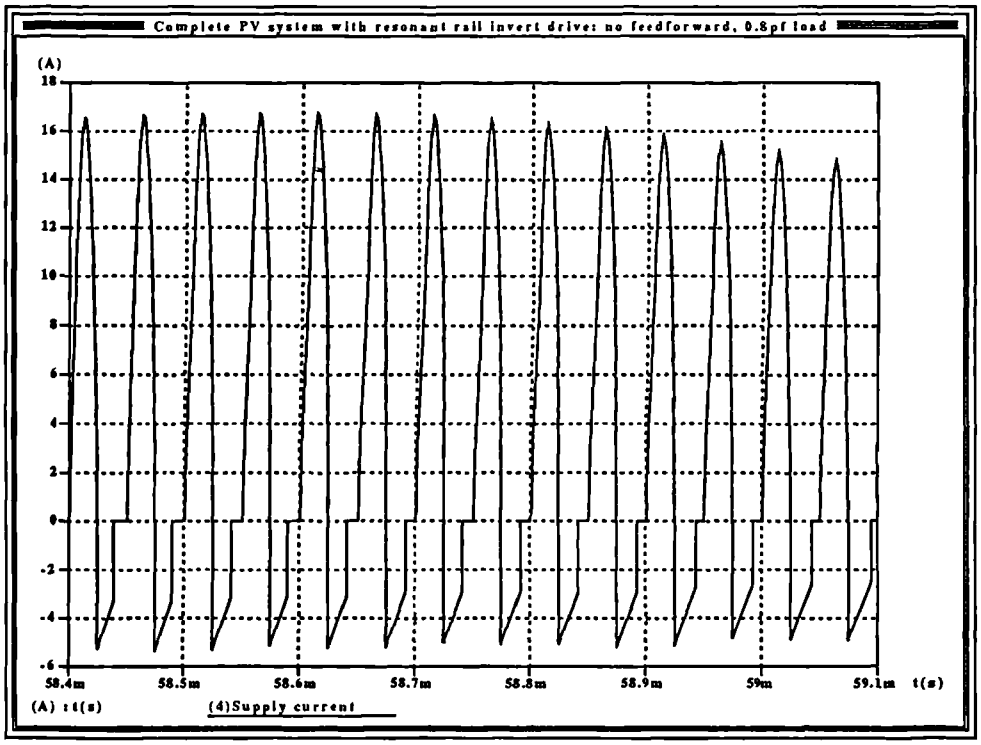

Figure 192 Group 2 set 2: Inverter supply current shape during a portion of the negative half cycle of the inverter output current; 0.8pf lagging load, capacitor and load current feedforward..

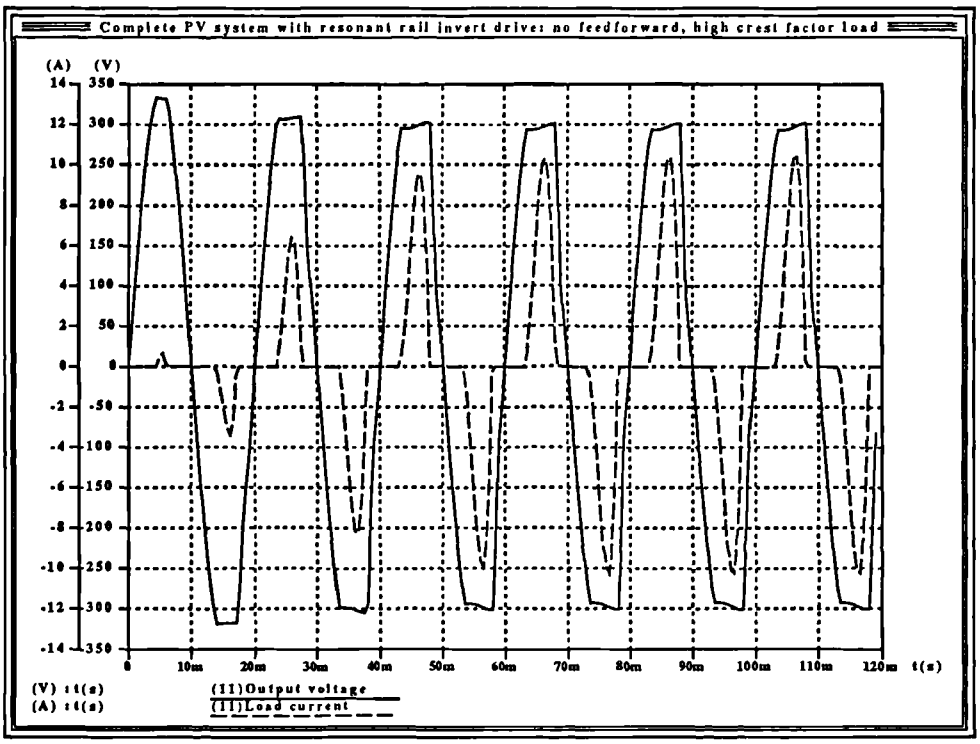

Figure 193 Group 3 set 1: Inverter output voltage and current; 3:1 high crest factor load, capacitor current feedforward.

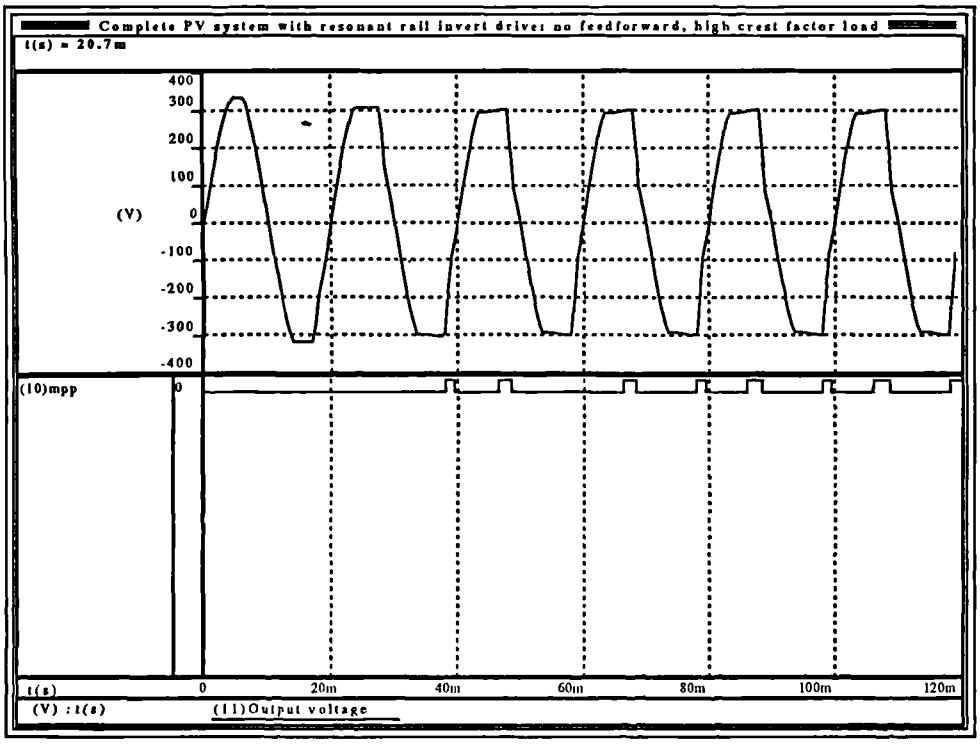

Figure 194 Group 3 set 1: Maximum power tracking signal and inverter output voltage; 3:1 high crest factor load, capacitor current feedforward.

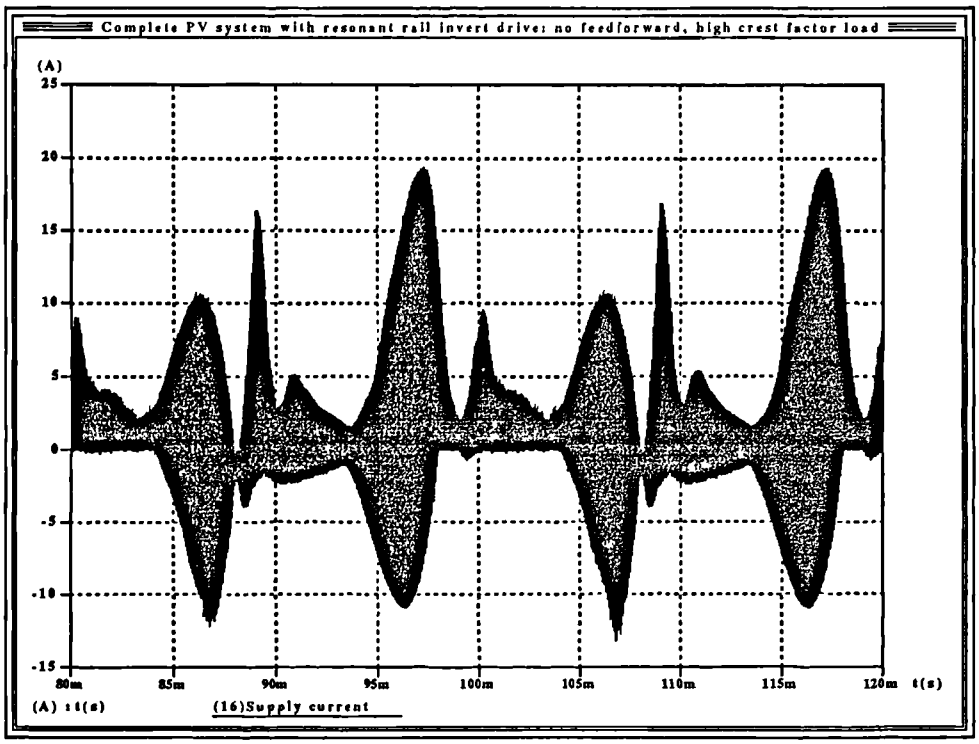

Figure 195 Group 3 set 1: Inverter supply current envelope; 3:1 high crest factor load, capacitor current feedforward.

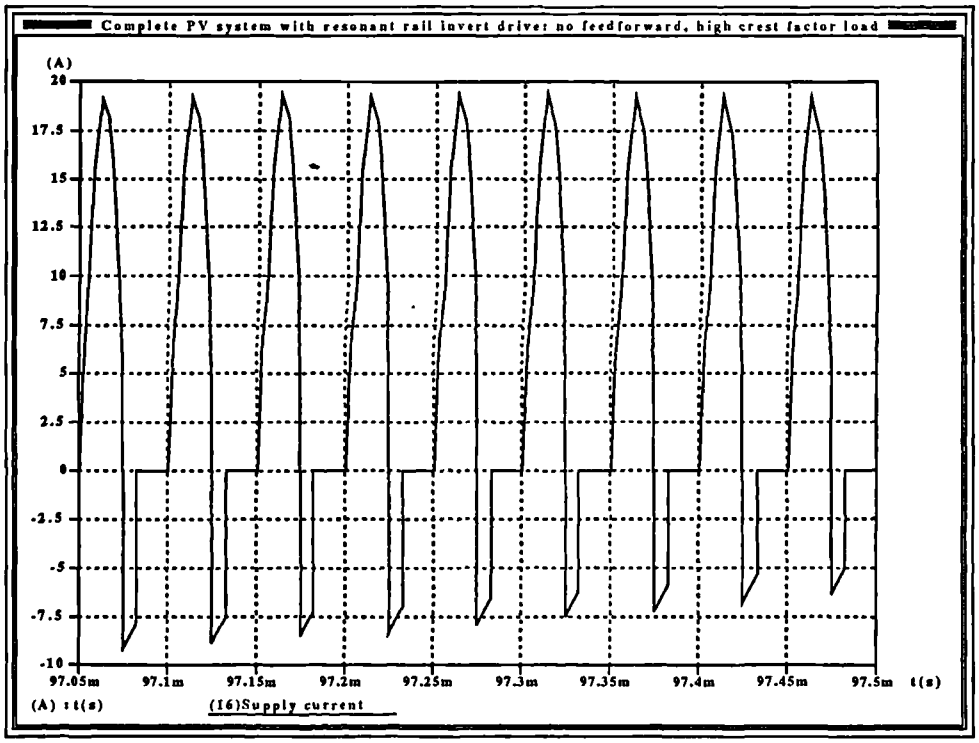

Figure 196 Group 3 set 1: Shape of inverter supply current during negative half cycle of inverter output current; 3:1 high crest factor load,capacitor current feedforward

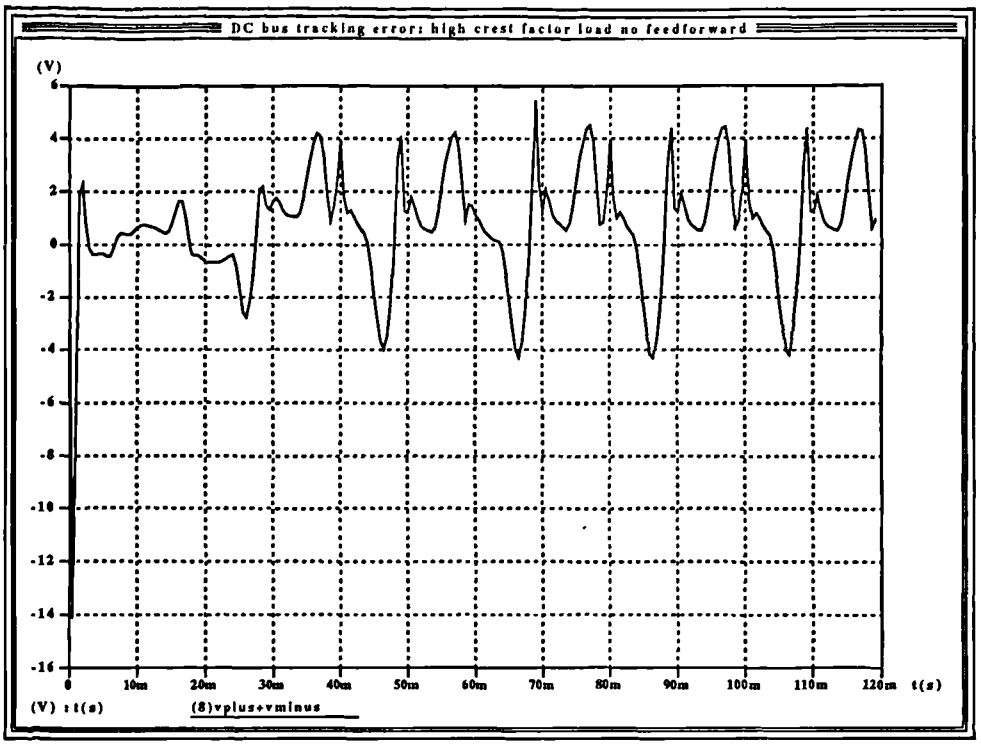

Figure 197 Group 3 set 1: DC bus tracking error; 3:1 high crest factor load, capacitor current feedforward.

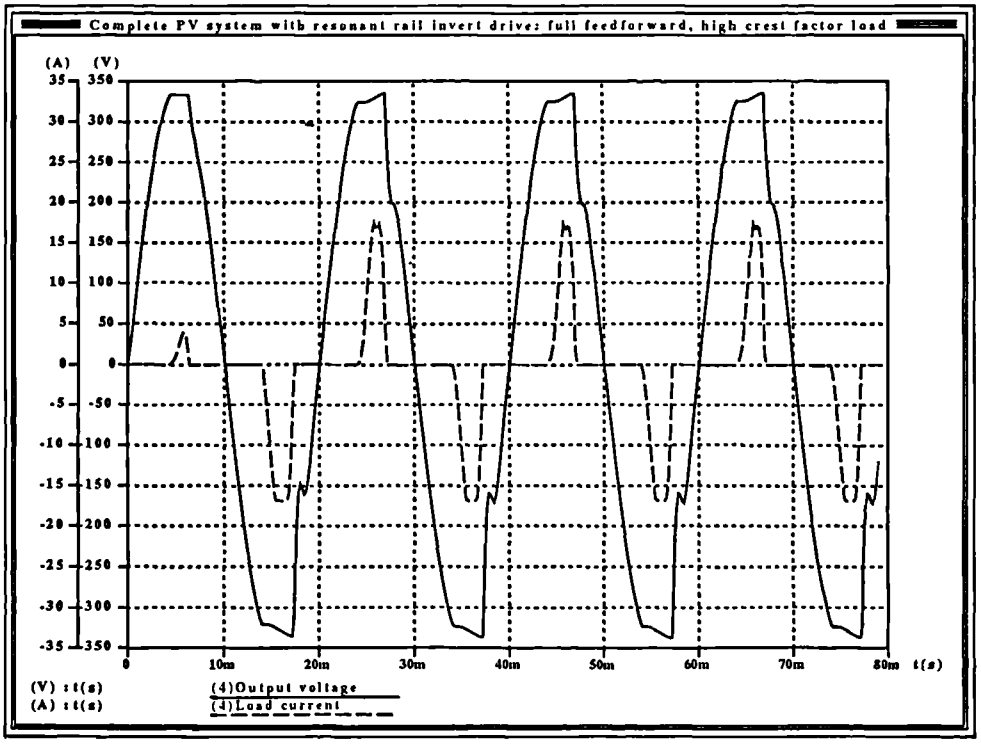

Figure 198 Group 3 set 2: Inverter output voltage and current; 3:1 high crest factor load, capacitor and load current feedforward.

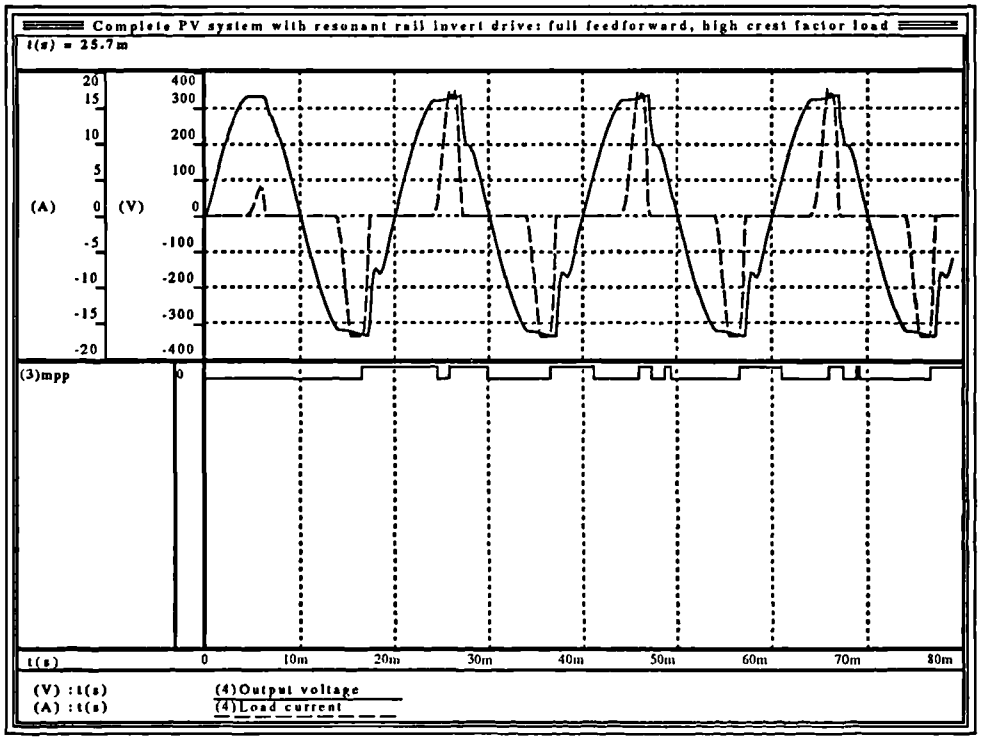

Figure 199 Group 3 set 2: Maximum power tracking signal with voltage and current; 3:1 high crest factor load, capacitor and load current feedforward.

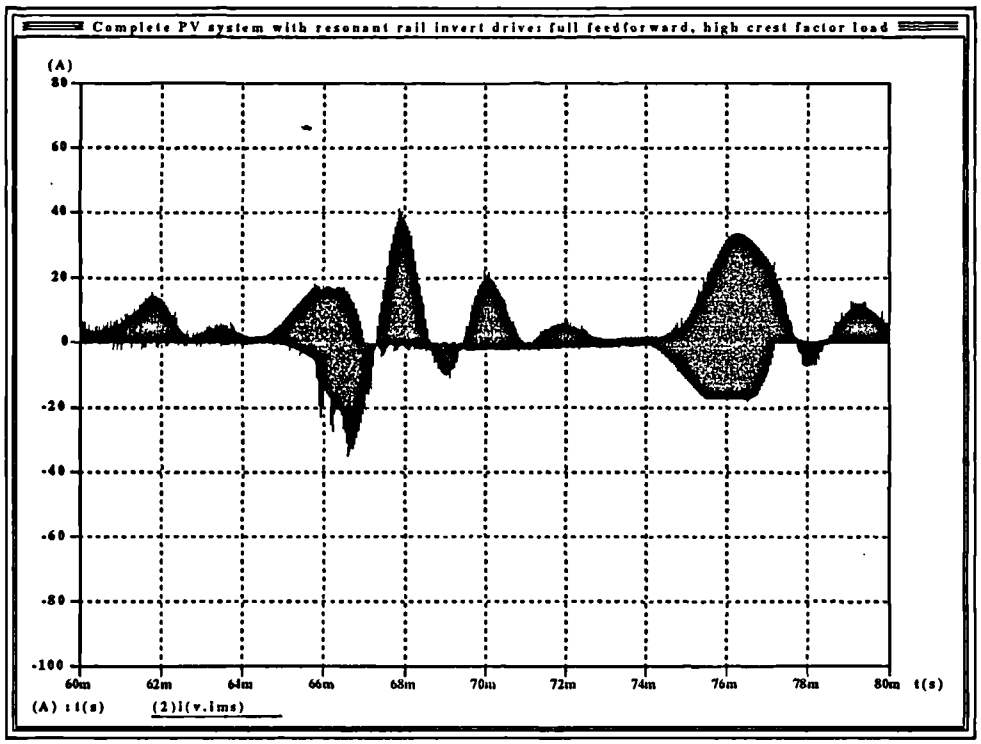

Figure 200 Group 3 set 2: Inverter supply current envelope; 3:1 high crest factor loaf, capacitor and load current feedforward.

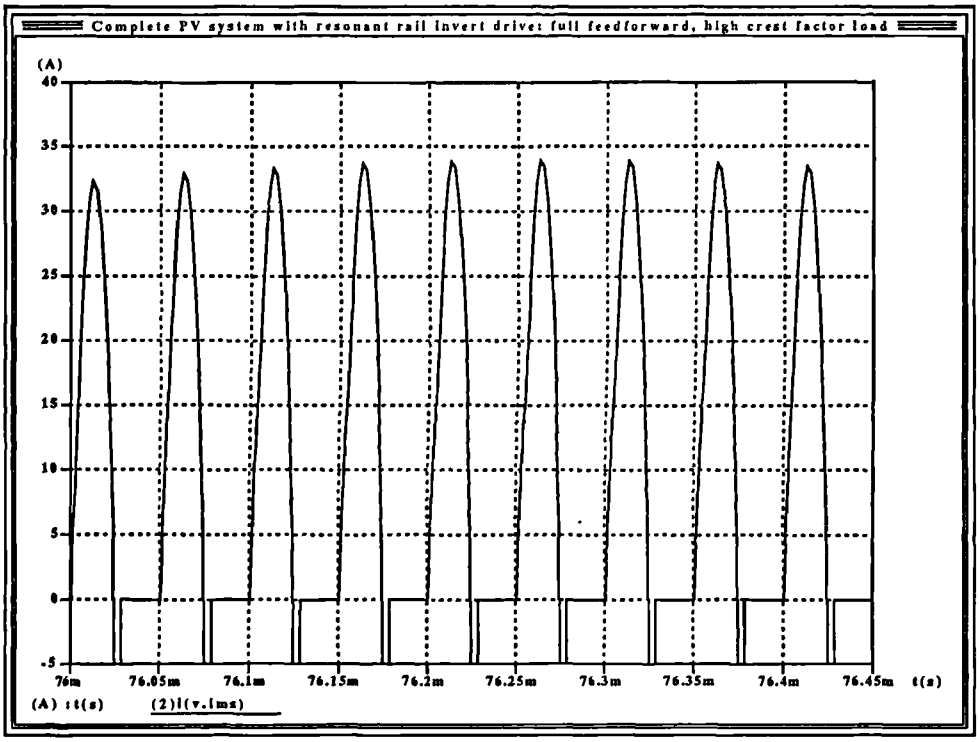

Figure 201 Group 3 set 2: Shape of inverter supply current during negative half cycle; 3:1 high crest factor load, capacitor and load current feedforward.

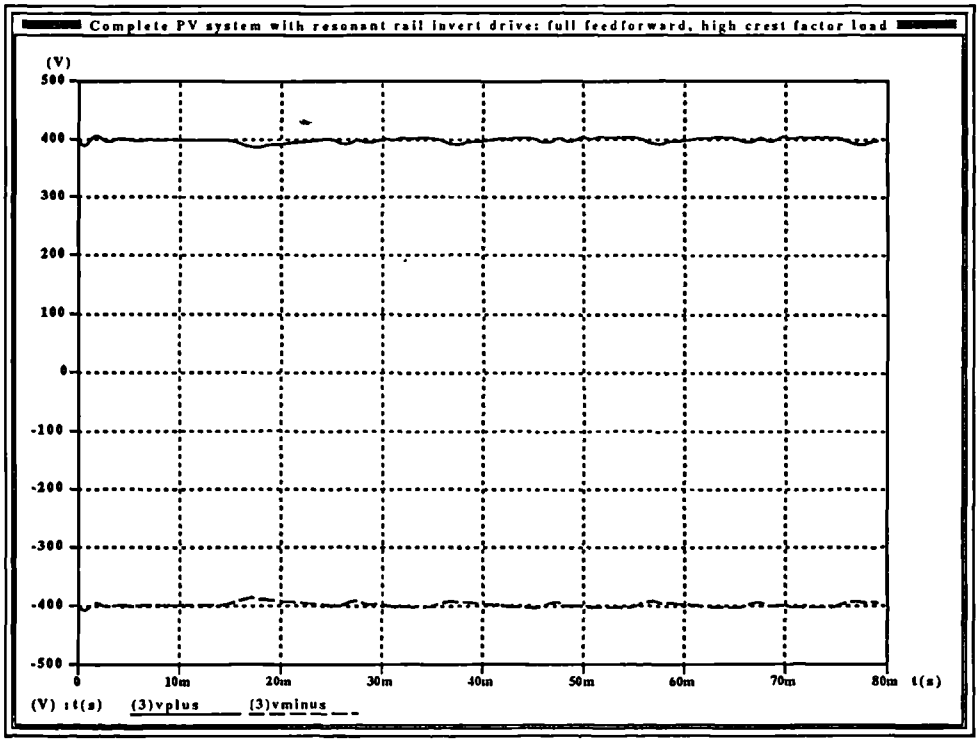

Figure 202 Group 3 set 2: DC bus tracking.; 3:1 high crest factor load, capacitor and load current feedforward.

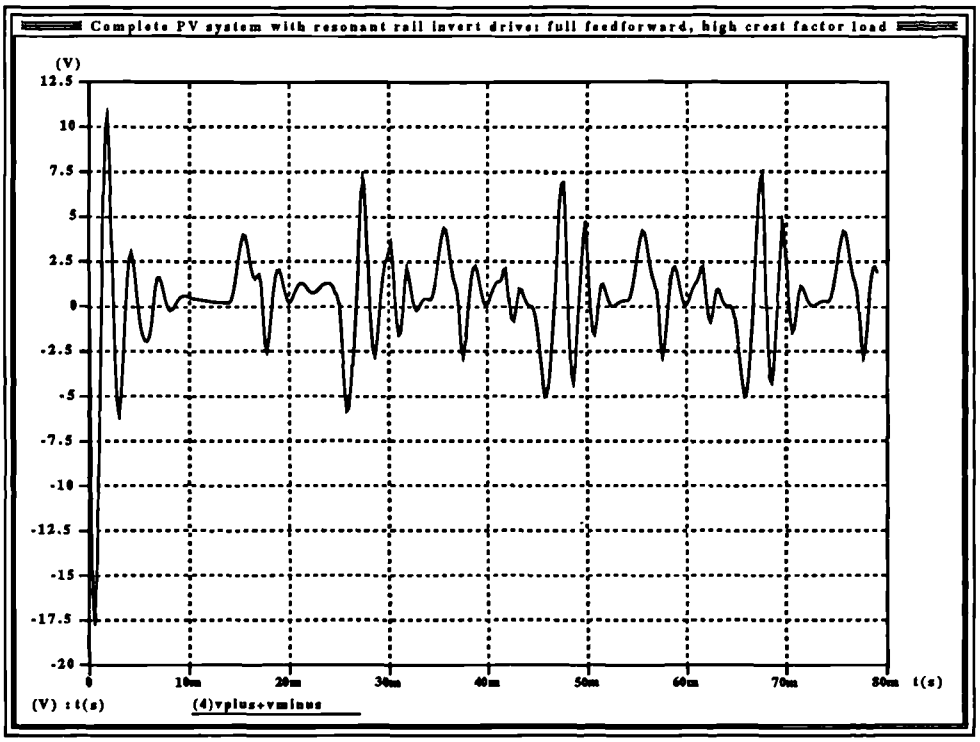

Figure 203 Group 3 set 2: DC bus tracking error; 3:1 high crest factor load, capacitor and load current feedforward.

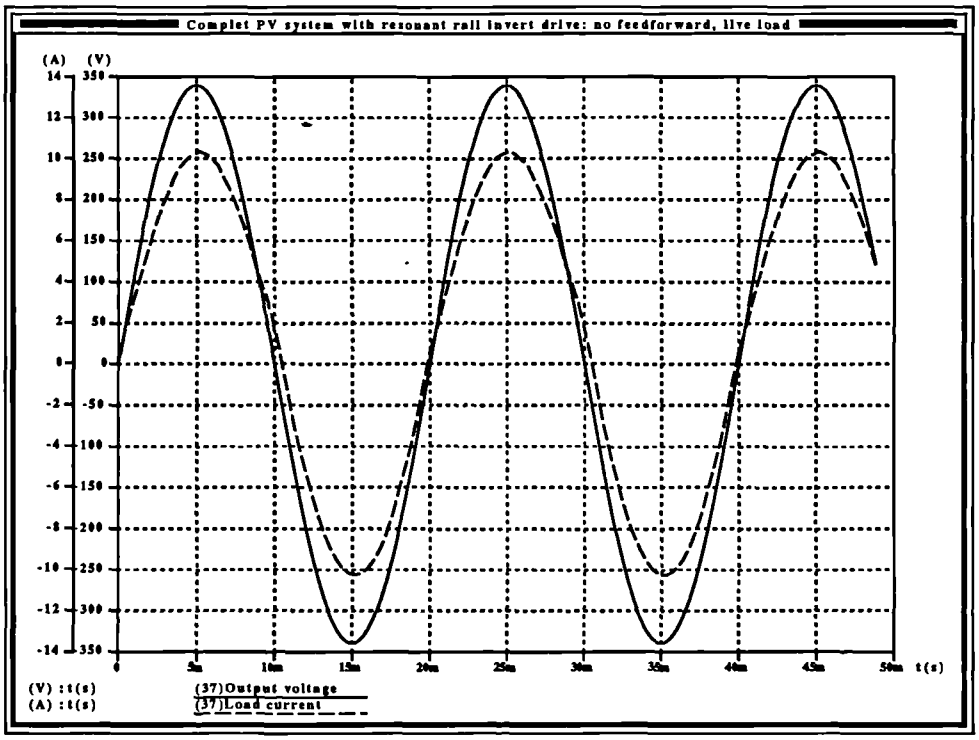

Figure 204 Group 4: Inverter output voltage and current; live load, capacitor current feedforward.

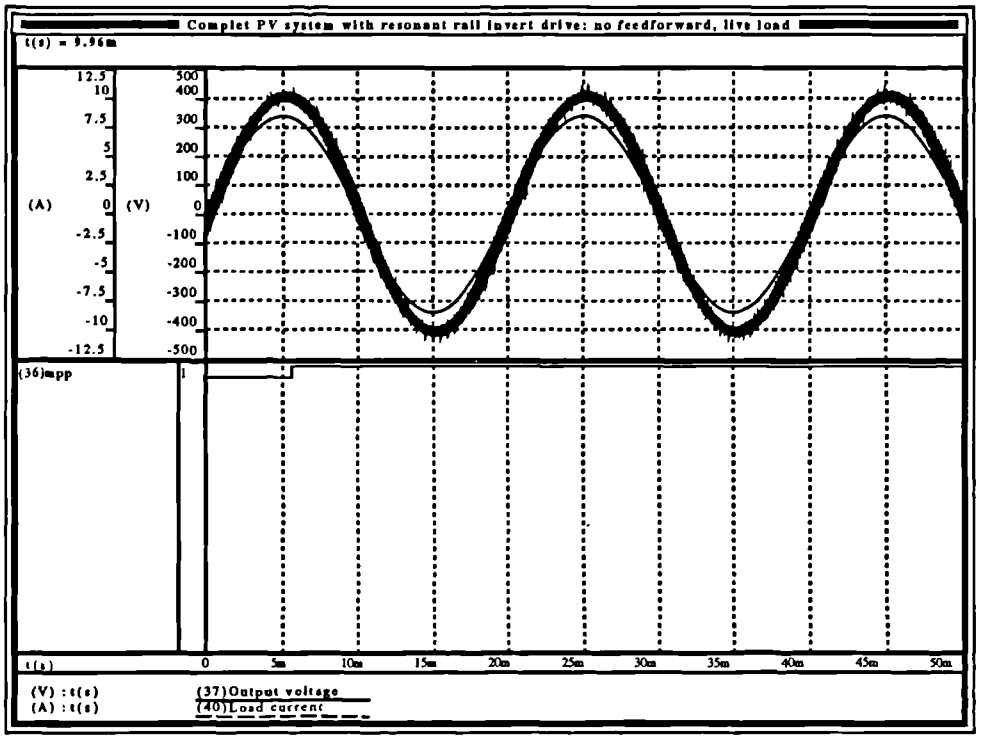

Figure 205 Group 4: Maximum power tracking signal, output voltage and load current; live load, capacitor current feedforward.

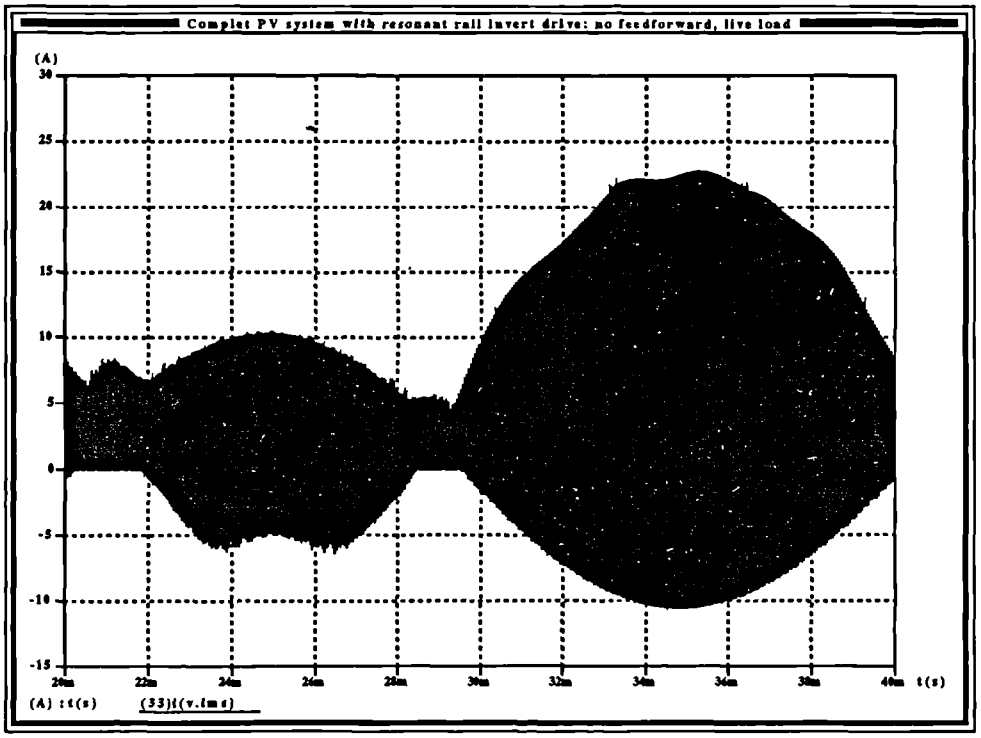

Figure 206 Group 4: Inverter supply current envelope; live load, capacitor current feedforward.

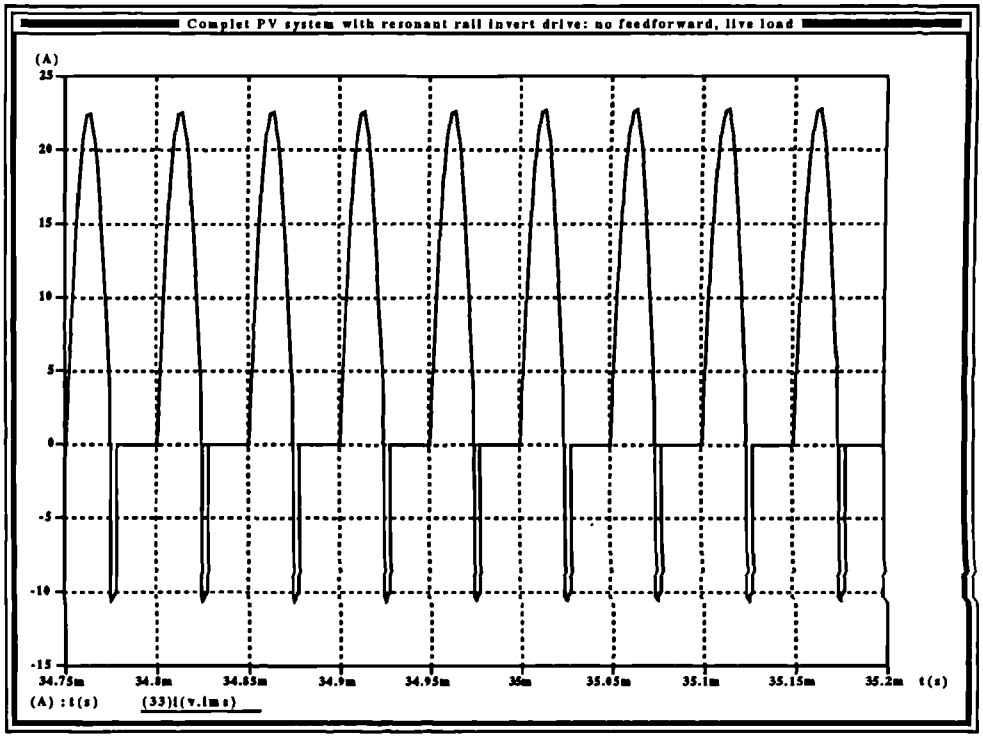

Figure 207 Group 4: Inverter supply current shape during a portion of the negative half cycle; live load, capacitor current feedforward

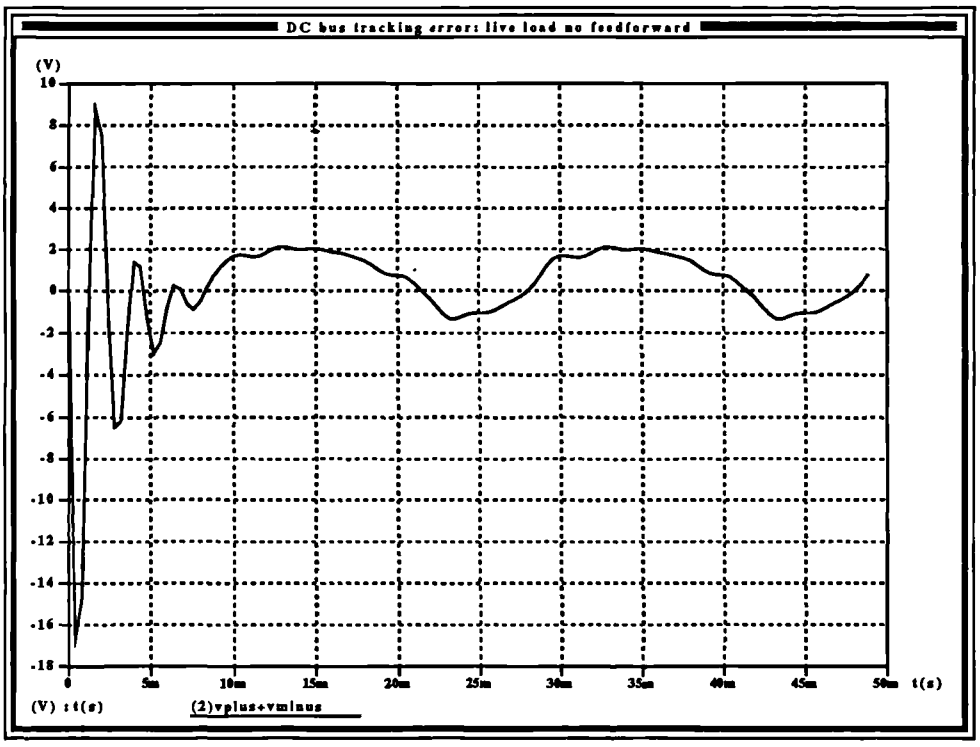

Figure 208 Group 4: DC bus tracking error; live load, capacitor current feedforward.

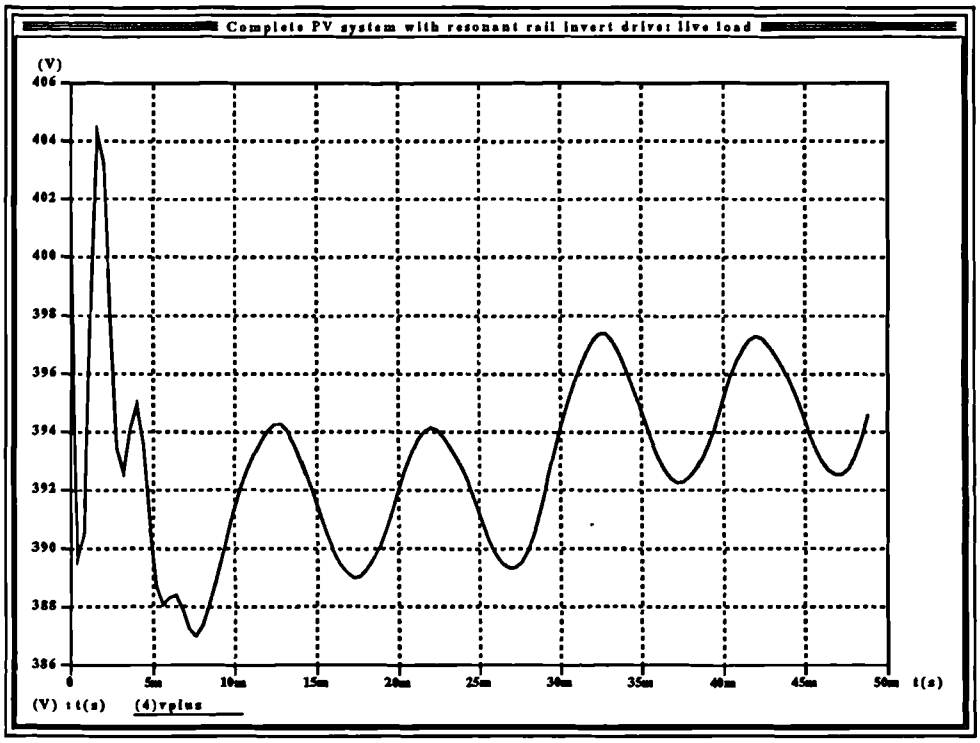

Figure 209 Group 4: Positive DC bus voltage ripple; live load, capacitor current feedforward.

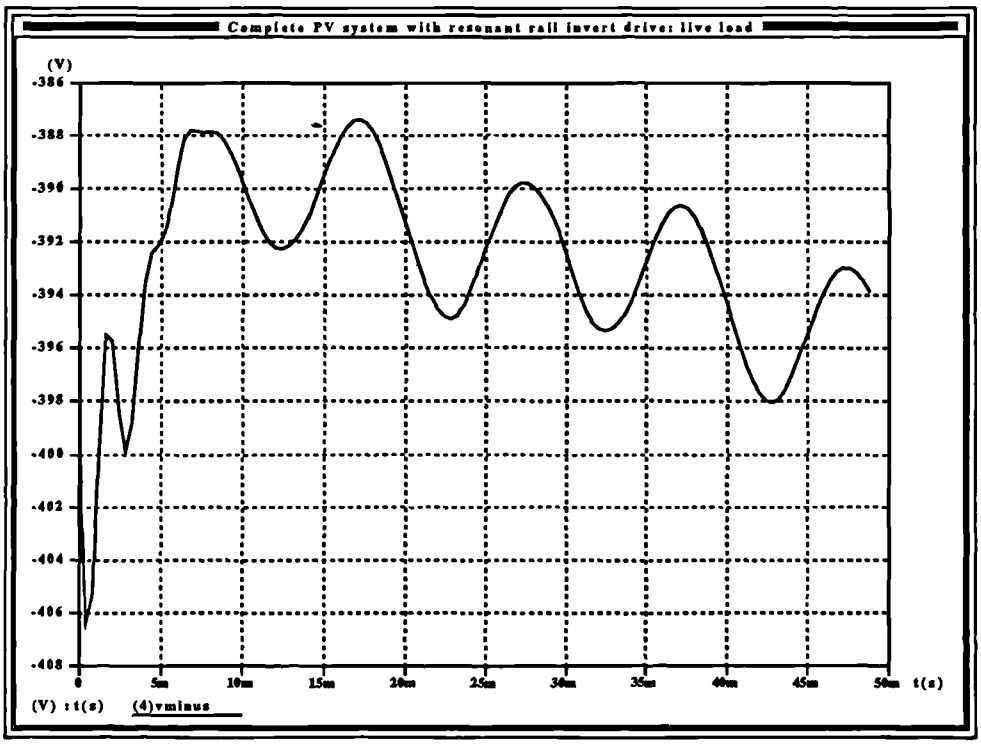

Figure 210 Group 4: negative DC bus ripple voltage; live load, capacitor current feedforward.

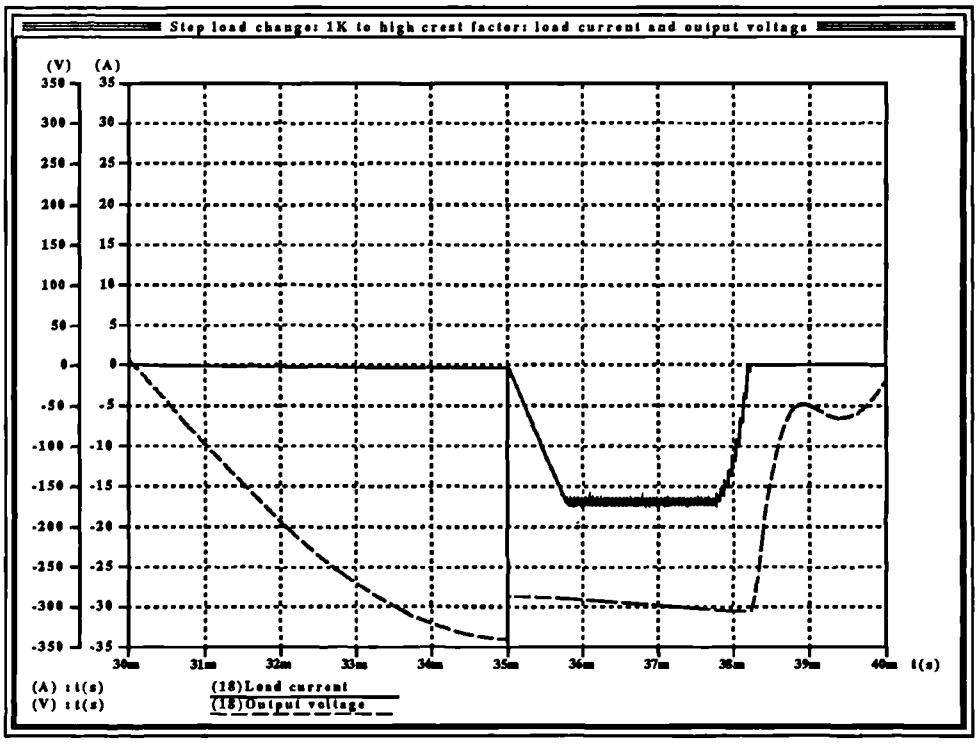

Figure 211 Group 5: Complete transient, load current and output voltage resulting from sudden application of high crest factor load.

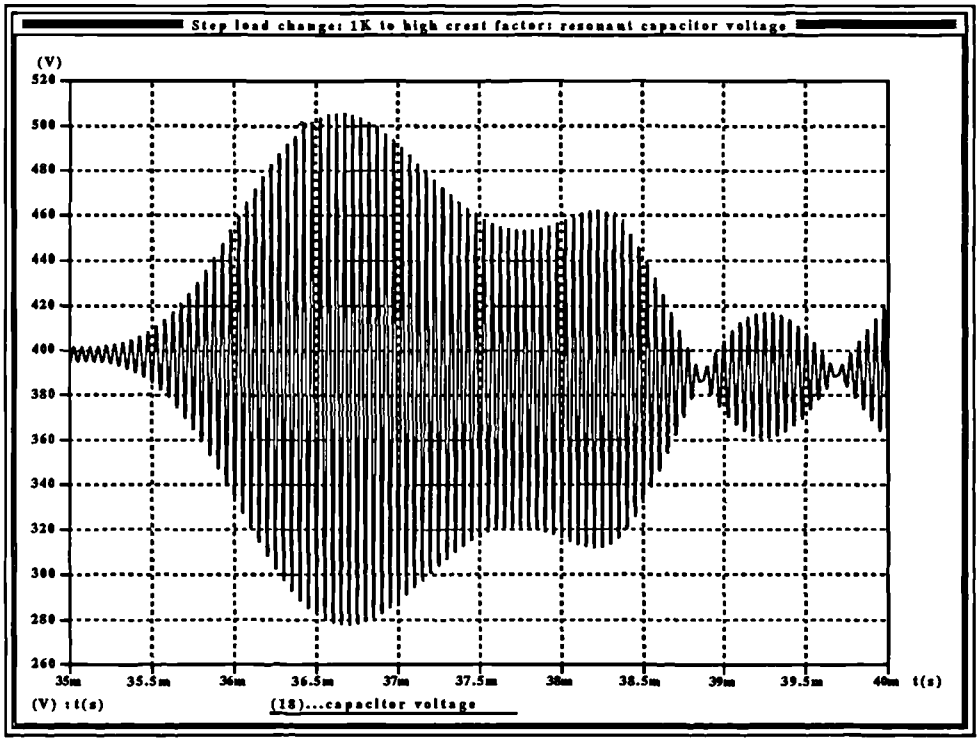

Figure 212 Group 5: Resonant capacitor voltage across complete transient resulting from sudden application of high crest factor load.

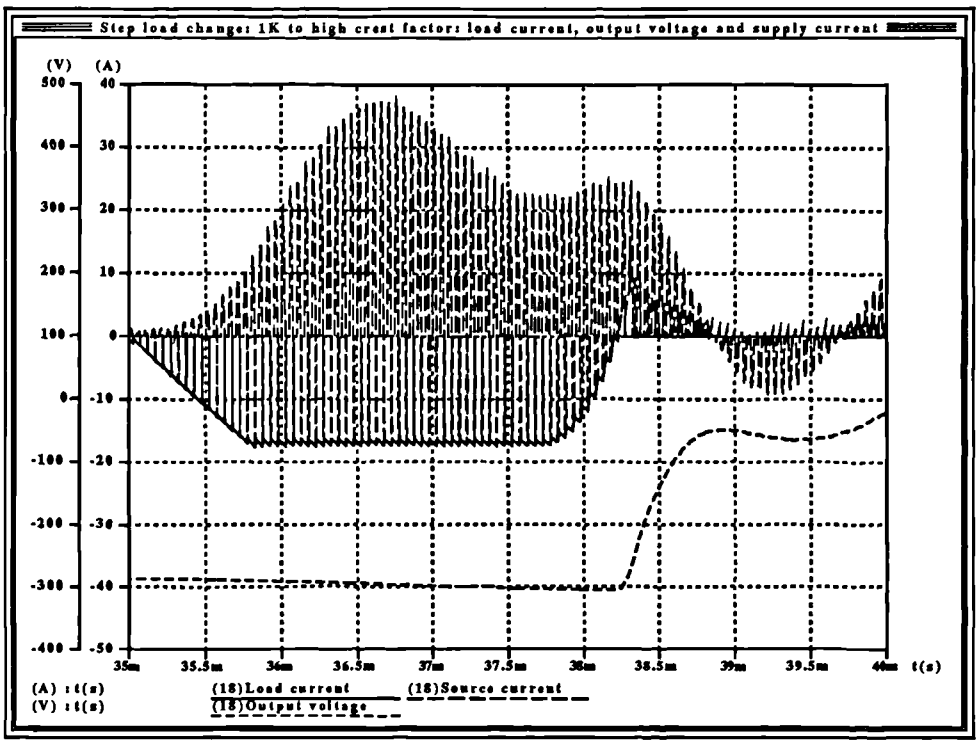

Figure 213 Group 5: Complete transient, load current, source current and output voltage resulting from sudden application of a high crest factor load..

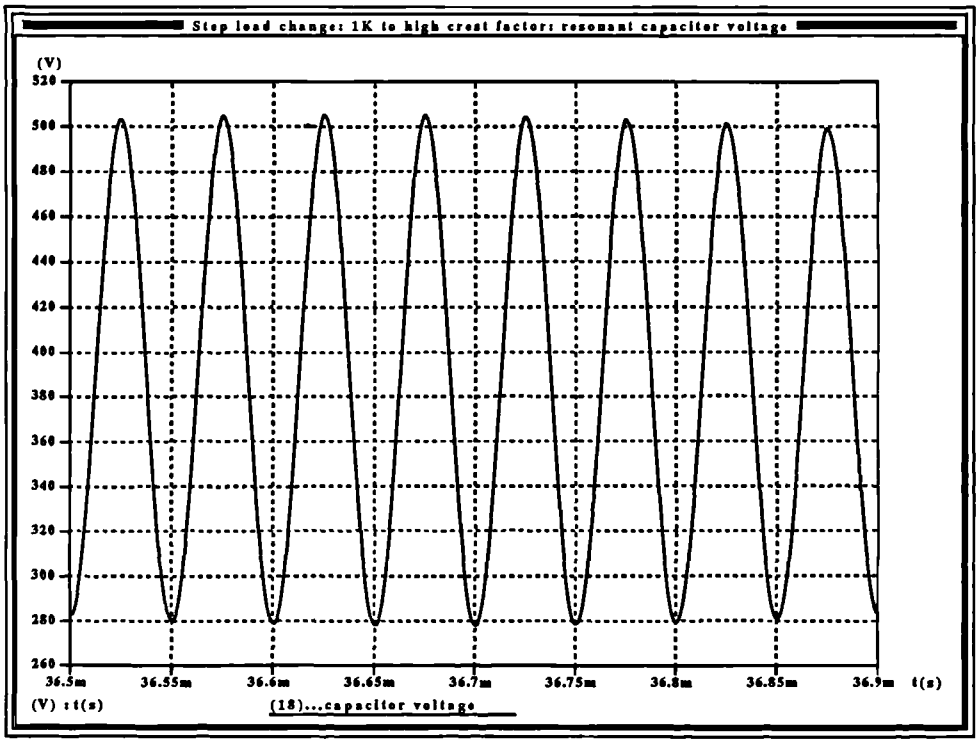

Figure 214 Group 5: Resonant capacitor voltage at point of maximum amplitude; sudden application of a high crest factor load.

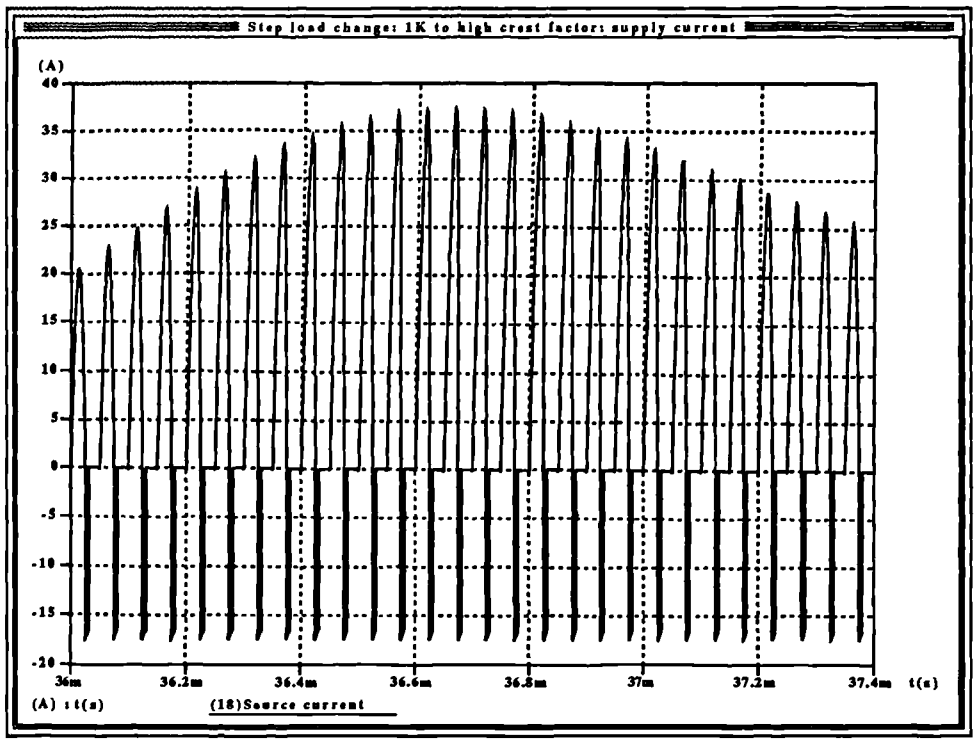

Figure 215 Group 5: Inverter supply current at point of highest amplitude during transient resulting from sudden application of a high crest factor load.

5.11 Results of inverter simulation: a discussion.

Considering the inverter results first, it can be seen that the system behaves remarkably well, both with load current feedforward and without. The simulation was performed as a single uninterrupted run, with the switchable load bank facilitating the switching in and out of the different loads. At the start of the run the initial voltage on the filter capacitors was set to 400V in order to minimize the length of the starting transient and avoid simulating the front-end over its power-up curve as it brings the d.c. bus voltage up from zero (see section 3.11.3 **Figure 110** for this transient). In a practical system, a soft-start arrangement will be used at power-up and so the starting transients on the resistive loads (particularly noticeable on **Figure 180** for the first 10ms) may be discounted. Each load type will be considered in turn.

5.11.1 Resistive loads

It may be seen from **Figure 176** and **Figure 181** that the load current feedforward tends to reduce the very small transient at the point of load change to an even smaller level. The very small phase error between the reference and actual output voltage (the reference zero-crossings are not shown and occur at 10ms, 20ms, 30ms etc.) in **Figure 176** is acceptable as it is, but the effect of load current feedforward is to reduce it still further. There is no obvious ringing anywhere, neither is there any distortion in the voltage and hence the current waveform. The use of load current feedforward with the predictive inverter control algorithm appears to have no serious disadvantages with a resistive load.

Figure 177 shows the inverter output voltage alongside the value of the digital flag signal indicating whether or not the front-end is in maximum power tracking mode (high for maximum power, low for voltage regulation). It can be seen that high loads drawing close to the maximum power which the array can supply at this point in time may result in the front end controller switching momentarily into maximum power tracking mode This is of no consequence as the average and RMS values of the load power do not exceed the array power (although the peak power might), and the DC bus voltage will not drop significantly and result in clipping of the voltage waveform.

At all times with all loads, the tracking by the negative d.c. rail of the positive d.c. rail (**Figure 180**) is good, tracking to within 2V (ignoring the starting transient) and thus the resonant split-rail supply is working as anticipated. **Figure 178** shows the overall envelope of the supply current as drawn from the front-end (for the system without feedforward) while **Figure 179** shows the shape of this current during the time when the inverter output voltage is at its negative peak (δ is close to 0.1) and current is flowing in the negative rail. It may be clearly seen that the resonant split rail supply is functioning as expected, and the basic envelope of the current in **Figure 178** does not exhibit any of the delay problems that were experienced with other forms of negative rail supply. Note that the amplitude of the envelope in **Figure 178** is higher during the negative half cycles (10-20ms and 40-50ms) than it is during the positive half cycles as current

can only flow from the supply into the resonant split-rail generator for one half of a switching cycle. **Figure 179** shows the positive d.c. rail supply current pulses lasting for one-half of the cycle time whereas during the positive half cycle of load current they are ramp-topped and last for the duration of the positive PWM modulation signal in the inverter, which can be up to 0.95 of the cycle time.

The negative going ramp-topped pulses in **Figure 179** are brought about during the time when the upper switch in the half-bridge is switched on, and inductor current is flowing into the positive rail during the time δT, or 0.1 of each switching cycle.

The presence of load current feedforward in the inverter control has little effect upon these waveforms (compare **Figure 178** with **Figure 183** and **Figure 179** with **Figure 184**).

The resonant split-rail inverter system works as expected with for a resistive load, and the response of the inverter is improved slightly by load current feedforward.

5.11.2 Reactive loads (0.8 pf lagging)

The voltage and current waveforms of **Figure 185** (without load current feedforward) and **Figure 189** (with load current feedforward) for a 0.8pf lagging load are very similar and show the characteristic effect of a load with a high lagging power factor - the current is lagging the voltage. The feedforward makes little difference in this case except to correct a very minute phase displacement of the voltage waveform, together with a noticeable reduction in output voltage error. The resonant rail drive system again performs as well as expected giving the characteristic shapes (**Figure 187** and **Figure 188** without load current feedforward, **Figure 191** and **Figure 192** with load current feedforward) and again load current feedforward has no visible effect upon the d.c. source to the inverter. DC rail tracking is good, being practically identical to that for the resistive loads and this is shown in **Figure 180**, the period of 50ms>t>90ms corresponding to the high power factor load. In this case, perhaps due to the slightly lower amplitude of current, the maximum power tracker does not engage, even momentarily (**Figure 186, Figure 190**).

5.11.3 High crest factor loads.

It is with this type of load that the effects of load current feedforward are more noticeable. The inverter control contains a current limit to prevent more than 17A being drawn from the system in order to protect the power chain from excessive loads. **Figure 193** shows the voltage and current waveforms into a fully-rated high crest factor load without feedforward, while **Figure 198** shows the same with load current feedforward. It is immediately obvious that the feedforward allows a greater inverter output voltage into the load than does the system with capacitor current feedforward alone. The current waveform also reaches its working amplitude much more quickly. The slight distortion of the falling edge of the voltage waveform during both half cycles occurs at the point where the output current drops to zero. This is caused by the discontinuity in the current waveform momentarily allowing the load current feedforward to generate a large current error signal at the input to the current-mode controller, before the PI compensator in the voltage loop is able to correct for it. This is of little consequence. The main disadvantage of the load current feedforward is that the voltage waveforms without load current feedforward are somewhat smoother than those with, and hence contain fewer harmonics. However the speed of response alone of the load current feedforward make it the better choice.

With the much higher pulse currents being drawn from the d.c.link when the inverter is feeding a high crest factor load, it would be expected that the front-end would momentarily switch to maximum power tracking mode at the peaks of the current waveforms, and indeed this is what happens (**Figure 194**). The cause of this is that although the d.c. link filter capacitor is designed to absorb the mismatch between instantaneous and average power in the case of the sinusoidal load, the much higher instantaneous currents appearing in the high crest factor load are sufficient to allow the capacitor voltage to drop. A d.c. link capacitor which could absorb the high intantaneous powers found with high crest factor loads would have to be much larger, and hence more expensive - the momentary drop into maximum power mode causes no problem for the converter. The speed of response and the larger amplitudes of current resulting from the load current feedforward would be likely to increase the duration of these excursions, and this may be

seen in **Figure 199** as expected. Note that as the load is below that which would draw maximum power continuously, the front end does not remain in maximum power mode and the DC rail voltage should not fluctuate significantly - as shown in **Figure 202** this is the case. The rail tracking is good, although worse than the linear loads as the current pulses are higher in amplitude and the maximum rail error is 7.5V, which is quite acceptable. The resonant chain current is appreciably higher, but providing the resonant split rail supply components are rated for it this should not be a problem - it may be seen from **Figure 200** that these currents flow for only a very short duration of time and their duty cycle is very low in consequence.

As with all the other load types, the use of load current feedforward in the inverter controls has no adverse effect upon the d.c. supply to the inverter and with this type of load its advantages are most profound. Given the various types of static loads likely to be encountered it appears that it is worth the cost of the extra ADC channel required to implement it as there are no noticeable disadvantages to this control approach where performance is concerned.

5.11.4 Live loads (utility feed)

This mode of inverter operation is unique in that a different control approach is required. Load current feedforward, by definition cannot be used in this mode as its effect is to transform the current demand signal at the input of the predictive control block into an error signal which is corrected by a voltage loop. In the live load mode the voltage loop is switched out as there is no requirement for it (the output voltage is fixed by the live load), and the current demand input signal to the inverter controller is used to determine the amount of power that will be fed to the load. The current fed to the load is adjusted by the controller to maintain the front-end just within the boundary of maximum power operation, but not so far in as to cause a significant drop in d.c. bus voltage.

Figure 204 shows the basic output voltage and current waveforms for the system operating into a simulated live load. Phase error is negligible. **Figure 205** shows the inductor current waveform with the output voltage and the maximum power tracking signal from the front

end. It can be seen that the controller quickly acquires maximum power tracking, and remains in this mode from then on. The operation of the controller in this mode may be better seen from **Figure 209**, which shows the magnitude of the d.c. rail voltage during the run. By way of an integrator the controller maintains operation between two boundaries: the first being the point at which the front end switches into maximum power mode, and the second when the d.c. rail voltage falls below a predetermined limit (in this case 380V). The d.c. rail voltage may fluctuate thus between this lower limit, and 400V thereby forcing the complete system to feed maximum power to the load. It effectively matches the live load to the array at its maximum power point, the integrator allowing response to changes in the position of the array maximum power point with environmental variables. As it can be seen from **Figure 209**, the variation in the positive d.c. bus voltage is of the order of about 4V and it clearly shows the presence of 100Hz second harmonic due to the current drawn from the front end supplying current for both positive and negative half cycles. The variation is quite acceptable.

Considering the operation of the resonant rail drive system, it can be seen from **Figure 208** that the tracking between rails is once again quite acceptable, the maximum error being of the order of about 2V (ignoring the starting transient). The envelope of supply current of **Figure 206** shows exactly what is expected from this system; the two half-sinusoids of current, one for each half cycle with the current pulse during the negative half cycle being larger due to the reduced duty cycle of the current (**Figure 207**). During this simulation run the maximum power supplied to the load was around 1.6kW and in all respects, performance is satisfactory.

5.11.5 Transient load curves

These curves are presented in order to show in some more detail the manner in which the resonant rail drive system operates. The load change under consideration is a step load change from a 1K (light) resistive load to a fully-rated high crest factor load at athe point of maximum amplitude during a negative half cycle. The sudden change in load conditions brings about a step demand in current at the output of the inverter causing the inverter controller to limit the current to a maximum of 17A (3:1 crest factor limitation). The action of the inductor in the inverter

›utput filter is such as to cause the current at the output to ramp up to this value as it can not :hange instantaneously, and hence the resultant current demand reflected into the negative DC ›us is a ramp. The current levels out at the limit level until the voltage falls off at the completion ›f the half cycle, where current falls off again. The load current and voltage waveforms may be ;een in **Figure 211**. The effect that this current profile has on the resonant split-rail generator :esonant capacitor voltage may be seen in **Figure 212**, and the source current envelope (for which :he positive amplitude is equivalent to the amplitude of the resonant circuit current) superimposed upon the load current and output waveform in **Figure 213**. The resonant capacitor voltage has a sinusoidal shape, as expected, and is shown in **Figure 214** in the region of the envelope peak. Likewise the shape of the positive rail supply current in the region of the envelope peak is shown in **Figure 215**. All waveforms suggest correct operation of the resonant split rail supply, and values obtained from them will be helpful in rating components during the development of the practical system for operation in a worst-case scenario.

The slight 'glitch' appearing on the load current curve of **Figure 211** at exactly 35ms is due to the simulator finite time-stepping algorithm predicting a large value at the instant that the HCF load is switched in - then backtracking to the correct value. Earlier on during the development of the system a single simulation was run with the minimum timestep set much lower in order to attempt to remove the glitch and determine whether this glitch resulted in the later portion of the curve being in error. The glitch was removed by this approach; however the time that the simulation took to run was protracted by an unreasonable amount and the simulator data files became extremely large - in one case too large for the plotter to handle. A comparison of the result of the run with the reduced timestep with **Figure 211** showed them to be identical except for the glitch and therefore later simulation runs were ran using the original timestep in the interests of speed and file size and the glitch may be simply ignored.

5.12 Development from simulation to practical system.

The result of the simulation is a workable converter system which meets the design criteria and provides a sound base upon which to develop a practical system. The control algorithms have

been tested and found to work very well; the predictive current controller has been successfully applied to a single-phase inverter and the use of load current feedforward as well as capacitor current feedforward has been proved to be a valuable addition to the algorithm where dead loads are to be supplied - its only disadvantage being the requirement for a further ADC channel to sample load current as well as inductor current.

The existing simulation work on the PV-aware d.c. to d.c. converter system has been successfully implemented as a practical system at low power, which operates in accordance with the expectations derived from the simulated system. In simulation, the front-end converter has been combined with the model of a unique resonant split-rail generator and a half-bridge inverter. Together with all of the control algorithms this has been implemented as a complete universal photovoltaic power conversion system, and has been shown to give a superb set of results for all of the conventional load types that such a system may encounter while operating in the field.

A practical implementation of the complete universal photovoltaic power conversion system will now be described in the next section. The basic design of the system has been retained, although some values have been modified slightly to take into account the parameters of components available at the time. The simulation shows that such a system is viable. A full set of specifications of the practical system will then be obtained, and used to determine the final uses and limitations of this scheme.

SECTION 6: Development of complete hardware prototype.

6.1 Introduction

With the simulation having shown that the design for the photovoltaic power conversion system was one which was worth pursuing and the tests at low power having proved that the unique embedded maximum power tracking system is effective, a complete high power (1kW) conversion system was developed and tested. Originally, it was hoped that the system could run at the 1kW power level, noise-related problems during early testing led to the reduction of the target power to 500W. Once the technology is proved, to increase the power is merely a simple developmental exercise, albeit time-consuming particularly in the eradication of noise from the power chain to prevent it interfering with the operation of the small-signal controller.

Although the target power of the complete system was reduced to 500W, the resonant split-rail supply was tested independently at load powers up to 1kW, at which power level it performed extremely well, somewhat exceeding expectations. This section of the system uses a much smaller inductor and did not appear to be subject to the same difficulty with saturation as the larger inductors in the inverter and front end were.

Despite the noise-related problems the system performed extremely well, proving the usefulness of the predictive current mode control scheme in systems such as these. It was unfortunate that owing to the (possibly electrostatic-discharge related) failure of one of the ADC devices and the lack of funds available to replace it, the channel sampling inverter load current was rendered inoperative, thereby preventing the demonstration of the control including feedforward. However, the performance of the system without feedforward was found to be very good indeed and it may be possible with predictive control in a production environment to

dispense with the feedforward completely and save the expense of an additional ADC and sample chain.

A full set of results are presented, with the inverter operating into all of the commonly-encountered loads including a live load. Performance was found to be very good, with the front-end operating in both voltage regulation and maximum power modes thereby enhancing the viability of this type of approach to photovoltaic power conversion.

The hardware consists largely of three discrete areas - the power chain, the control logic and the sampling chains. The control logic may be further broken down into two sections: the PWM/reference/timing and control logic block, and the DSP itself. **Figure 216** shows a block diagram of the complete system to show the basic interconnectivity. The design and development of each section of **Figure 216** will be described in detail in turn.

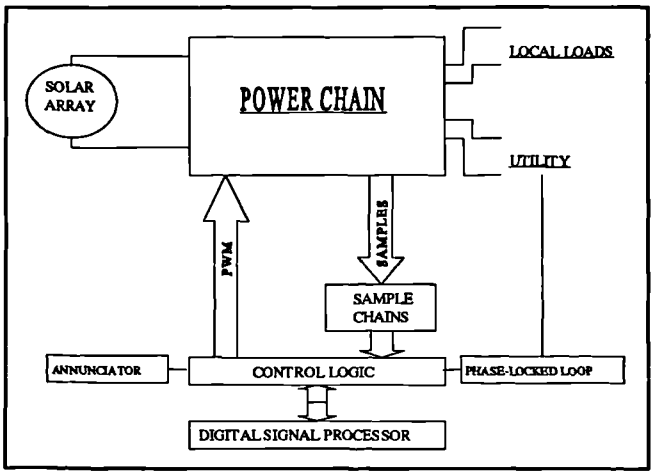

Figure 216 Block diagram of complete high power hardware.

6.2 Power chain

The power chain of the practical system is in essence identical to that of the simulated system. A schematic of the complete hardware power chain may be seen in **Figure 217**.

6.2.1 IGBT configuration

The IGBTs and parallel diodes are provided for by the use of four separate half-bridge IGBT modules with intrinsic reverse-parallel diodes arranged in the following configuration. One 600V 50A module provides TR1 and D1 (the upper device in the module is permanently

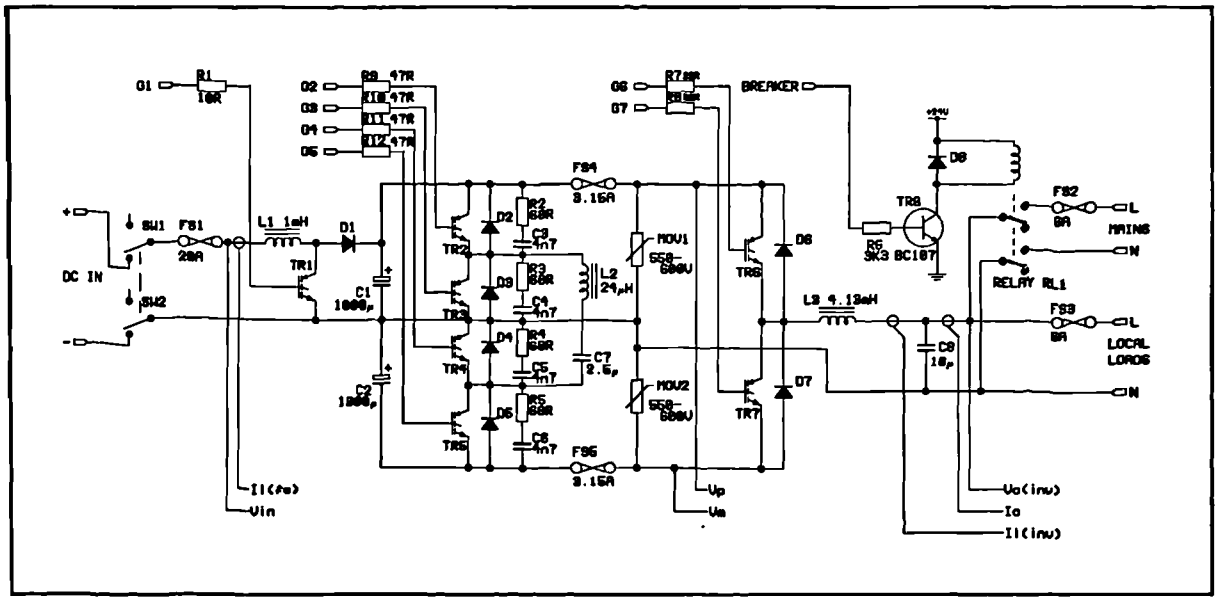

Figure 217 Complete hardware power chain.

gated off). The two arms of the resonant split rail supply are provided by two 600V 50A modules, one to provide the TR2/D2 and TR3/D3 combination and a second to provide the TR4/D4 and TR5/D5 combination. A final 1200V 50A module provides the TR6/D6 and TR7/D7 combination.

6.2.2 Gate drives

The gate drives to the IGBTs are proprietary units. They are relatively robust, and posess the ability to drive the gate negative during the off-time to aid noise suppression, and they also have a modicum of punch-through protection built into the drives. If the IGBT collector-emitter voltage starts to rise during the device on-time, the drive to the gate is shut down within a microsecond. It was found, however, that this protection was not always effective as a number of IGBT devices were destroyed during the early stages of the development before the robustness of the drive signals was established.

The gates of the devices are fed through a small resistor to damp any oscillation that may occur at the gate of the device, and also to give a measure of control over the rate of turn-on of the devices. 10Ω resistors were provided with the drive boards. However early experimentation with the resonant split-rail supply showed severe noise emissions which were sufficient to

corrupt the image on the digital storage oscilloscope used for the tests. The IGBTs in the split-rail supply were zero-current switching and it was found to be the high rate of turn-on that was responsible for the noise (discharging small device capacitances quickly). Increasing the gate resistances in the split rail supply to 47Ω cured the problem, and the residual noise was reduced still further by R/C snubbers. On the inverter side, noise was reduced to tolerable levels by increasing the gate resistances to 22Ω.

6.2.3 Snubbers

The main difference between **Figure 217** and the simulated power chain is the addition of the four snubber networks around TR2-TR5 (R2-R5/C3-C6). These were added to the system to help reduce the residual noise caused by the fast zero-current switching of TR2-TR5. Although this type of snubber is dissipative and wastes power, it is effective in reducing the noise, and is quick and easy to implement. Each snubber was designed to dissipate 7.5W thereby allowing the use of easily-obtainable 10W resistors. In a production version of this system a better layout would enable smaller snubber capacitors to be used resulting in a reduction of snubber power loss. Further reduction, if desired, could be achieved by the use of a non-dissipative snubber that would return the snubber capacitor energy to the DC bus filter capacitors C1 and C2.

Snubbers around the inverter devices were experimented with, but the simple RC snubbers used appeared to exacerbate a 100kHz 'ring' on the leading edge of the device current waveform as it switched on, and this increased the noise in another part of the system. Snubbers were not used on the inverter devices as they did not appear to bring about any worthwhile improvement in performance

6.2.4 Breaker

The function of the breaker is to provide a means of connecting and disconnecting the utility from the inverter under software control. In a domestic/small business application such

as this the normal mode of operation is (when sufficient light is available) for the breaker to be closed, and the converter to be driving both the local loads and the utility. When local loads are light, the converter will feed the excess energy generated by the solar arrays at the maximum power point back into the utility, while as the local load increases beyond that which can be provided by the converter, so power is drawn from the utility. In a real application, under conditions of insufficient light, or converter fault conditions, the inverter can be shut down and isolated allowing the local loads to draw all their power from the utility. To implement fully would require a second breaker not shown in **Figure 217** to isolate the inverter completely. A fuse provides a further line of defence against faults occurring within the inverter section of the system. In the laboratory prototype, with the breaker in the position shown, the utility may be disconnected from both the local loads and the inverter under such conditions. However, the system possesses a degree of UPS functionality in that the local loads are protected (in the presence of sufficient light) against utility failure - the inverter will disconnect the utility and revert to voltage-regulating mode, continuing to supply them (subject to the balance between load power and array maximum power) while the utility is off.

Under dark, or fault, conditions, however, when the converter is shut down, this configuration requires that the utility breaker be opened - otherwise there is a danger of the reverse-parallel diodes across TR6 and TR7 acting as rectifiers and causing a voltage to appear across C1 and C2. This single breaker system was adopted during development for simplicity and because a suitable relay was available, in a production version of this system it would be necessary to include a second breaker in series with the inverter output to allow the inverter to be physically disconnected from the utility whilst maintaining continuity of supply to the local loads.

6.2.5 Fuse protection

A 20A fast-blow fuse protects the input to the converter (FS1), while 6A fast-blow fuses (FS2 and FS3) protect the utility drive and the local load outputs (therefore providing quick identification of the faulty circuit by identification of the blown fuse). During development two

3.15A in-line fuses were connected in the main DC busses driving the inverter section to provide a further level of protection for the silicon.

6.3 Control logic

The control logic, apart from the DSP itself, consists of basically four main areas. Physically, and with the exception of some buffering, the control logic is implemented entirely within a Xilinx XC4003 field-programmable gate array (FPGA). This implementation allows for ease of modification of the logic without having to alter the PCB upon which the system is constructed simply by reprogramming a configuration EPROM. The FPGA contains all DSP bus interface logic and to the DSP appears as a set of registers which are mapped across to the bottom nine locations in the DSP I/O space. The block diagram of **Figure 218** shows the basic arrangement. The hardware arrangement contains tristate buffers to ensure that during power-up, when the FPGA is reading this configuration data from the associated EPROM, all IGBT gate drive signals and DSP bus signals are gated out in order to prevent contention. A soft power-up system is provided to ensure that FPGA configuration takes place cleanly at power up, and once the configuration is complete and the definable I/O pins of the FPGA have become active in their programmed state the buffers are enabled to allow operation. A detailed description of each block follows.

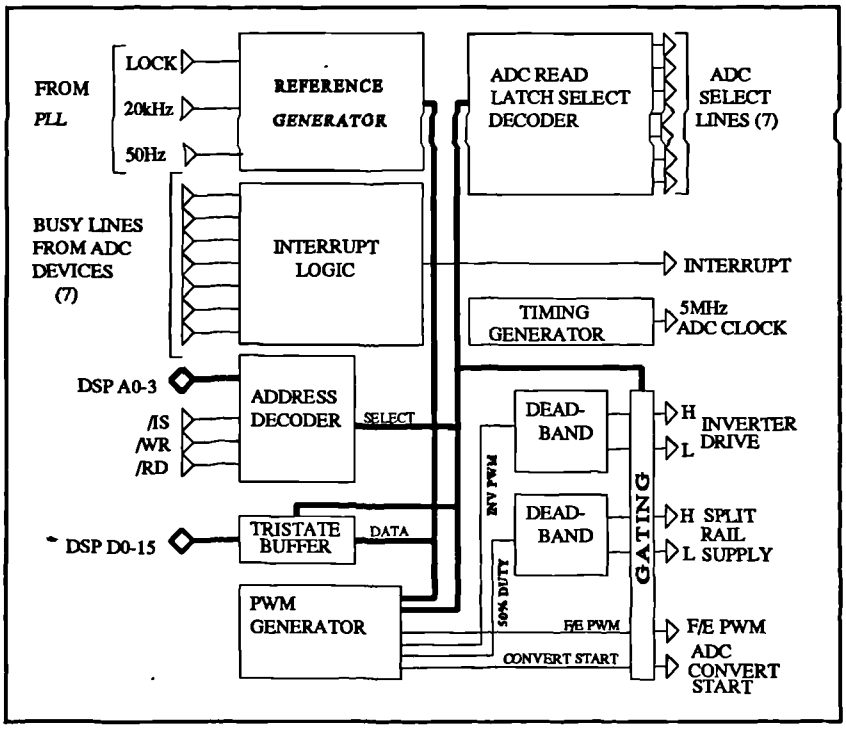

Figure 218 Block diagram of FPGA based control logic.

6.3.1 Pulse-width modulation generators.

The twin PWM generator block generates the base drive signals for both the front end and, through a deadband generator, to the inverter. Duty cycle (δ) is continuously variable from zero to unity, although limits are imposed upon this range in software in order to ensure that timing requirements are not violated. A simplified diagram of the twin PWM generator is shown in **Figure 219**. All registered logic is synchronous (hence the clock lines have been omitted from the diagram) and registered macros (for example, the latches) are controlled by way of an enable input, if required. The PWM generator block works as follows. The required value of pulse width is written to the first pair of latches. In the case of the first PWM channel (which drives the front-end), the output of this latch forms one input to a comparator, the other input being the result of a continuously running 10-bit counter. The complete system is clocked at 20MHz, the frequency of the DSP clock resulting in the counter wrapping around once every 1024 cycles. It will thus be generating pulses on its carry output at a frequency of $1/(1024 \times 1/20 \times 10^6)=19531$Hz. This is sufficiently close to the desired 20kHz switching frequency. These carry pulses are used to set what is effectively an S-R latch (although in practice this is formed from a J-K latch and some combinatorial logic in order to prevent 'glitches' occurring when the duty cycle written to the latch is equal to zero or unity). The result is that as the counter wraps around the PWM outputs go high; effectively 'turn on at clock time'. The S-R latches are reset by the comparator outputs when the counter value reaches the value written to the latch and thus the PWM outputs go low.

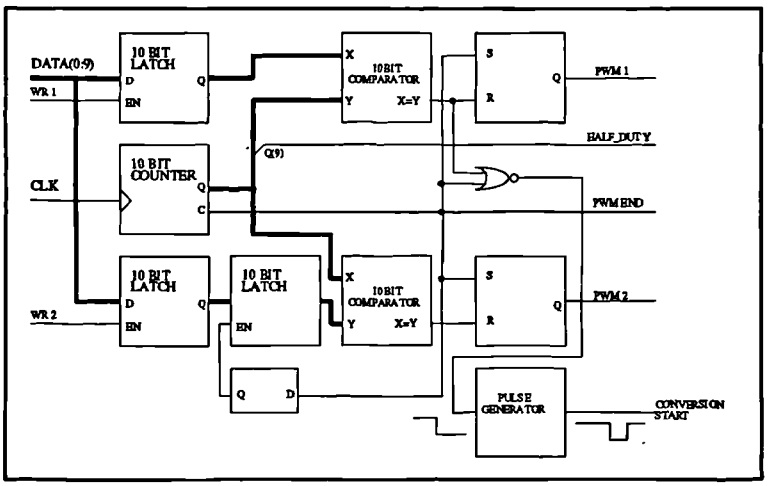

Figure 219 Simplified diagram of twin PWM generator logic.

Two further signals of importance are provided by the PWM generator. The requirement of the control for the front-end is that samples of inductor current are taken at the start of both the on and off time. The predictive scheme used in the inverter only requires samples to be taken at the start of the switching cycle. With this arrangement, the start of the switching cycle of both channels are coincidental - a convenient arrangement requiring only one counter and minimizing possible switching noise transients. An active low 'convert start' pulse is generated in the clock cycle immediately before both the rising and falling edge of the front-end PWM signal. This is derived by NORing the carry and comparator outputs, and a pulse generator is used to ascertain that the signal is active low for long enough to be recognized by the ADC devices (0.2μs). The second signal is a waveform with a 50% duty cycle at the same switching frequency. This is provided by the tenth bit of the counter and is used (via a deadband generator) to provide drive to the devices in the split rail supply. The basic timing of the PWM generators is shown in **Figure 220** with reference to the HALF_DUTY signal - essentially a 20kHz waveform.

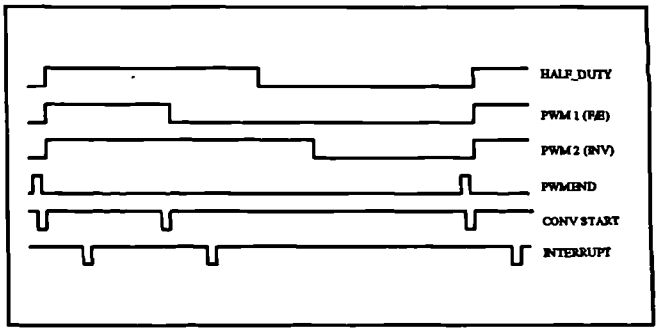

Figure 220 Basic timing of PWM generator.

The inverter PWM channel differs from the front-end PWM channel only in that a double-buffered arrangement is used to write the PWM duty cycle value to the comparator. This overcomes a criticality that would otherwise place a lower limit upon the permissible duty cycle that could be written to the latch. Without double-buffering, the new pulse width for each cycle can only be written to the latch in a period as soon as possible after the commencement of the on-time at the start of the cycle. If the write takes place during the off-time there is a danger that if the new value is less than the old value, the output may go low prematurely. If the write takes place too long after the start of the cycle the off time may be missed.

This is not a problem in the front end channel. Owing to the requirement for a clean sample of power chain parameters at the start and the end of the on time, it is necessary to

ıpose a lower limit upon the duty cycle in order to allow for the conversion time of the ADC ;vices. At the start of the cycle the PWM output goes high, a conversion is completed, the ıterrupt asserted (see **Figure 220**). The PWM output must not go low and initiate a new ADC ɔnversion until the interrupt has been serviced in software and the ADC samples from the turn-ı have been stored. Thus it is possible to perform the PWM duty cycle write within the ıterrupt service code. If the minimum PWM duty cycle is set to allow this to take place, there no danger of any spurious transitions in the PWM outputs - with the ADC devices being used ıe lower limit is δ_{min}=0.1. The same also applies to the upper duty cycle limit δ_{max}=0.9 - ɔnversion time must be allowed for. These limits have very little effect in reducing the perating range of the front-end boost converter as the very low and very high duty cycles ɔrrespond to regions of poor converter efficiency anyway.

The inverter does not require two ADC samples of power chain parameters during its on-ıme - it only requires the one at the start of the cycle. Using a single-buffered approach here and ;riting the duty cycle during the interrupt service would place the same lower limit upon the luty cycle as would be required by the front-end. A limit upon the extremes of the inverter duty ycle can result in a requirement for very high DC bus voltages in order to provide the necessary ıeak output voltages. The average output voltage at the center of the half-bridge is given by δV^+-1-δ)V^- where V^- and V^+ are the DC rail voltages, so if a requirement for a peak negative output ;oltage of 340V is required, and V^- and V^+ have equal magnitudes, then the required magnitude ıf rail voltage is 340/(2δ_{min}-1) or 425V. It is advisable, in the interests of component ratings to ;eep this as low as possible, and thus if duty cycle limits on the inverter can be avoided it is lesirable to do so.

The double-buffered approach allows the PWM duty cycle write to occur at any time *before* the start of the on-time. The second level latch is enabled by the carry output of the counter, and thus updates the comparator at the exact start of the duty cycle. The duty cycle then becomes continuously variable between zero and unity. The small penalty to pay is that the PWM write must now take place slightly earlier, requiring the inverter control calculations to be performed sufficiently rapidly to ensure they are complete before the start of the on-time. The

front-end control can use ADC conversion time to complete its calculations as the conversion process is transparent to the DSP.

6.3.2 Deadband generator.

The deadband generator is basically very simple in both design and operation - the timing diagram for the block may be seen in **Figure 221** from which the manner in which it operates may be seen. The function of the deadband generator is to produce two drive signals from the single PWM signal, one corresponding to the on-time, and one corresponding to the off-time. The system works by inverting the PWM signal in order to provide the low side drive, then delaying the leading edge of both the true and inverted signals. The two drive signals thus retain symmetry as the delay is subtracted from both leading edges and the duty cycle value is unaffected.

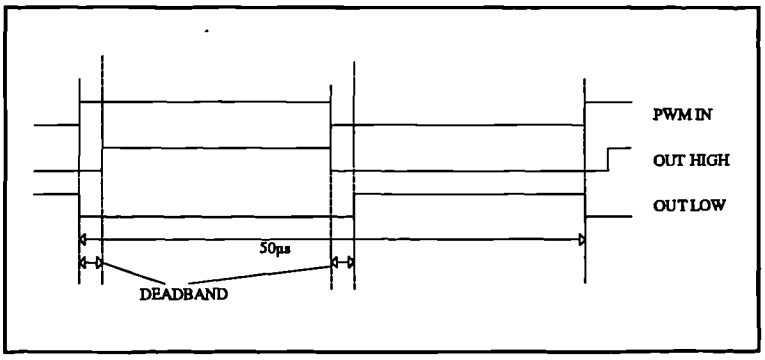

Figure 221 Timing diagram for deadband generator.

The value of the deadband is different for the split-rail supply and for the inverter. To reduce noise the split-rail supply requires a higher value of gate resistance to reduce dV/dt across the devices. Consequently a wider deadband is required than for the inverter with its lower value gate resistors. Measurement of the drive signals at the gate of the IGBTs led to values of 2.5µs and 1.5µs being established for the deadband of the split rail supply and the inverter respectively. The deadband is generated by way of a counter, and the value of the deadband may be altered (to a resolution of an integral number of system master clock cycles) simply by changing the count modulus otherwise the same basic design of deadband generator is used for both the split rail supply and for the inverter.

A minor aspect of operation is that at the extremes of values of δ, the actual on-time will get very small as the deadband is constant with δ. With the limitations of rise-times in the gate

drive modules it is necessary to be careful to avoid partial turn-on of the devices - to this end a small upper and lower limit of inverter δ is advisable. At the extremes of δ, if the current in the inverter filter inductor is in the same direction (i.e. positive for high δ and vice-versa) then as the IGBT with the low on-time turns on current will have commutated into the inverse-parallel diode associated with that device and partial turn-on of the IGBT may not be as critical. However, with some loads, noticeably poor power factor loads, it is not guaranteed that the current in the filter inductor will be in the same direction, and thus to remain safe it is inadvisable to permit partial turn-on in the interests of both efficiency and IGBT longevity.

The deadband generator contains additional logic at the output to ensure that at no time can both devices be turned on at the same time, thereby providing a further level of defence against shoot-through failures.

6.3.3 Reference generator

The function of the reference generator is to provide an 8-bit number between 1 and 200, which may be read by the DSP. In software this will form an index into a table containing values of the sine function at 200 points across one half of a cycle. The basic, simplified arrangement of the reference generator may be seen in **Figure 222.**

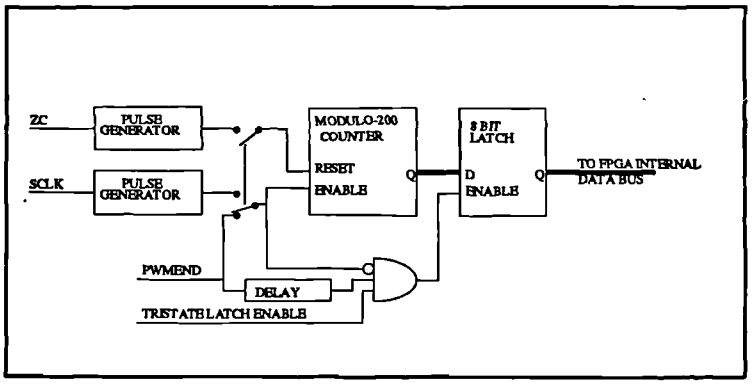

Figure 222 Simplified layout of reference generator.

The reference required is at 50Hz, which implies that the modulo-200 counter should wrap around every 10ms. There are two modes of operation depending upon whether it is desired to lock the reference signal to the mains. In the free-running mode, the switch of **Figure 222** (which is implemented in logic) is set so as to allow the PWMEND pulse from the PWM generator to enable the counter to advance once at the end of each 20kHz switching cycle. Under

these conditions the counter will wrap around once every 10ms. The zero-crossing signal from the phase-locked loop is gated out to avoid contention, while the information relating to the sign of the particular half-cycle is provided simply by using the effective 'carry' output from the modulo 200 counter to toggle a J-K latch, and gating the output of this latch into one of the status lines that can be read by the DSP (this is not detailed in **Figure 222**).

In the live load mode, where a reference locked to the utility is required, the system makes use of two signals that come from the phase-locked loop subsystem. This generates a 50Hz locked squarewave (ZC) and also a 20kHz clock which is phase-locked to the 50Hz (SCLK) giving exactly 200 rising-edges in each half-cycle of 50Hz. The rising edge of the 20kHz signal and both the edges of the 50Hz signal are converted to pulses synchronous to the master clock and then gated such that the 20kHz pulses become the counter enable, and the now 100Hz pulses are used to reset the counter. The counter now generates a 0-200 count which is locked to each half cycle of the mains. The sign information is obtained simply by gating the 50Hz squarewave from the PLL into the status line.

To synchronize the counter updates with the switching cycle the output of the counter is written to a latch shortly after the end of each switching cycle to ensure a clean update - that is so that the DSP does not try and read the value as it is being updated (which may cause bad data to be read). To improve the synchronization the latch write is suppressed both during a latch read and also a counter update. In this way, if the counter is updated at the exact instant that a latch read is taking place, the latch will not be updated at that time and the old counter value will be read. The latch will be updated at the next switching cycle. The fact that the switching frequency is not exactly 20kHz (19531Hz) prevents a 'lockout' condition occurring in which counter updates are always coincident with a latch read thus preventing latch update.

This slight discrepancy in the switching frequency means that the free-run (dead load) reference frequency will not be exactly 50Hz (48.82Hz), although this will be close enough for all applications except those which use the mains frequency for timing purposes e.g. clocks. The frequency of the reference when locked to the mains will be exactly 50Hz as this is governed by the PLL. A greater degree of frequency accuracy in dead loads could be achieved by changing

the modulus of the counter when out of lock to 195, to coincide with the slightly lower switching frequency. In the context of this project, particularly as there is very little space left within the FPGA for extra logic it was felt that the added complexity was not justified in this application.

6.3.4 Timing generator

The timing generator simply generates a 5MHz clock to drive the ADC devices. For the devices used the maximum clock frequency is 5MHz, giving a conversion time of 2.6μs. A counter and a latch generate a clock with a 50% duty cycle from the 20MHz master clock.

6.3.5 Interrupt generator.

The interrupt generator provides a single active-low pulse to the DSP, wide enough to allow at least three positive transitions of the master clock. The BUSY lines from the seven ADC channels are ANDed together and the resulting high edge, when all ADCs have finished their conversion, is inverted and converted to a pulse of sufficient length to use as the interrupt.

6.3.6 Decoder logic and FPGA registers within DSP address space.

The decoder logic is contained within the FPGA and defines the I/O map of the registers, status words and ADC channels within the DSP I/O space as well as controlling the bidirectional data bus within the FPGA configuration and providing enable signals for the ADC read buffers and the annunciator panel.

Nine I/O locations are required for use by the logic and ADC channels, and to facilitate ease of access to them sixteen locations are partially decoded into the DSP I/O address spaces (of which the bottom nine are used). These addresses repeat themselves across the entire I/O address space as 00-0fh, 10h-1fh and so on. This allows access to the I/O by the DSP in software either using the conventional I/O access instructions but also using memory-mapped register functions directed at the I/O port hole at memory address 50h (an area of memory addresses

which are mapped by the DSP to I/O space beginning at 80h). This allows a degree of flexibility within the software design.

Two status registers are used by the logic, separated into read and write functions and configured into separate memory locations. This allows the remaining bits of the 16-bit word that are not required as hardware status lines to be used within the software as additional flag bits. The first of these status words, coded as 'ST_STATUS' in the software contains the control bits for the logic. Only the bottom eight bits are used by the logic, leaving the top eight bits free for use by the software. As the status of these control lines can not be read back from the logic, a 'mirror' location must be maintained in software (this is required to enable the use of the upper eight bits as software flags). **Table 11** shows the bit-field definition of the bottom nine bits of this word as used by the hardware. All are active-high except those which are specified.

Table 11 Bit-field definition of system status word.

BIT	DEFINITION
0	INVERTER PWM OUTPUT ENABLE
1	FRONT END PWM OUTPUT ENABLE
2	SPLIT RAIL SUPPLY OUTPUT ENABLE
3	PWM GENERATOR (ALL SECTIONS) RUN/STOP HIGH->RUN LOW->STOP
4	REFERENCE COUNT SOURCE EXT/INT HIGH->EXT LOW->INT
5	FPGA INTERNAL LOGIC RESET
6	UTILITY FEED BREAKER
7	INPUT BREAKER

The final bit, INPUT BREAKER, was put in place to allow the input voltage from the array to be switched in and out under software control. The physical breaker was never implemented owing to the lack of a suitable breaker to hand, but the control line was left in place.

The second status word, coded as ST_HARDWARE in the software, contains the read status from the logic. Only the bottom three bits are used by the logic - the upper 13 bits are pulled

Table 12 Hardware status line bit field definition.

BIT	DEFINITION
0	FRONT-END PWM STATUS
1	PLL LOCK
2	REFERENCE ZERO CROSSING

low. The bit field definitions for ST_HARDWARE are shown in **Table 12.** All lines are active high. Bit zero is basically a copy of the front-end PWM output, while bit 2 is a copy of the 50Hz signal from the reference generator so that the correct sign of the reference may be determined. Bit 1 is an active-high signal from the phase locked loop which is used to detect an in-lock condition.

6.3.7 PLL and lock detect logic: considerations of islanding

The phase-locked loop section performs an important function within the framework of the inverter. From a 50Hz sinusoid, transformed down from the utility to provide isolation, the phase-locked loop must provide three signals: a 50Hz TTL level waveform at 50% duty which is locked in both phase and frequency to the mains, a 20kHz waveform, also at 50% duty which is phase-locked to the 50Hz output and an active high 'lock detect' signal. The PLL block must detect an out-of-lock condition and clear the lock detect signal appropriately.

The question of islanding arises - the condition in which the utility fails whilst the converter is still locked to it. The converter must disconnect from the utility immediately in order to protect the utility repair engineers. Detecting this condition is no easy task. The first consideration is an isolated instance of the converter, for example just one converter on a housing estate. If the local load experienced by the converter once the utility fails is either side of the maximum power point, or has a poor power factor, the converter output voltage and also the internal DC bus voltage will rise or fall and thus eventually be trapped by the over/undervolt detect. The converter will shut down, disconnect the utility and restore voltage regulation mode into the local loads. However the problem occurs when the loads have a good power factor and demand a power which is equal to the maximum power. Under these conditions the converter could conceivably continue running until either the load changes or the maximum power available from the array changes. Under these conditions the utility disconnect is not guaranteed.

A second consideration relates to the ideal goal for operation of this type of converter. If a large number of houses within an estate are fitted with this type of converter, the problems of islanded operation worsen. If the utility fails at this time it is more likely that no individual

converter will be able to detect the failure of the utility, and all converters will continue to operate.

A very elegant solution to the first consideration was proffered by [11]; this method used a delay to effectively destabilize the PLL in the free-run condition by introducing a right-hand plane pole into the PLL transfer function under the condition when the utility fails. A similar method involving careful choice of inverter controller parameters and sensing of line impedance has also been proposed [58]. Other methods include the use of a saturable reactor [59] to trap line faults These methods are very effective for a stand-alone converter operating under the conditions of the first consideration, but would provide very little protection against islanding when operating under the conditions of the second consideration, although methods involving the sensing of line impedance could be a better approach if the inverters are connected to a supply to which few other similar independent generators are connected.

The study of islanding is quite a complex one in itself, and there was insufficient time available to develop a complete solution to islanding under both conditions. A version of the destabilized PLL was not implemented within this system owing to the lack of availability of sufficient logic. A 20ms delay is required, equivalent to a single cycle at 50Hz, and with a 20MHz master clock a 400000 stage shift-register would be required. Even better methods involving the use of counters would require excessive logic. Analog delay methods would not be accurate enough unless very carefully designed. The FPGA is virtually full, and the small EPLD used to implement the lock-detect logic is also full. As available funds did not allow extra logic to be obtained, the solution used was very crude, but effective enough within the context of the development system. The capture and lock range of the PLL is very small, and the lock-detect logic is designed to drop the lock upon any sign of difference between the phase of the VCO and that of the utility - and not to restore it until after a suitable delay. Such an arrangement leads to the lock being dropped if sudden changes in the utility voltage are encountered, such as what would happen if the utility failed abruptly. Moreover, the system is glitch-sensitive and aberrations of the utility may also cause the lock to be dropped. It is appreciated that such a system is not ideal, but is what could be achieved quickly within the limited availability of time and hardware.

The conditions of the second consideration are very difficult to detect at the best of times by the individual converter systems. It may be of benefit here to employ a system of communication, perhaps based upon the establishment by the utility of a radio-frequency carrier signal superimposed upon the mains, which all converter systems could detect. Useful information could be modulated on to the carrier, but more importantly in the event of line failure the carrier would also be dropped, enabling the converters to detect line failure and disconnect themselves from the utility. Such an implementation would require the adoption of universal standards by both the utility companies and the manufacturers of converter systems: if solar power was to become a priority this method could easily become viable particularly in the wake of such schemes as demand-side power management.

The implementation of the PLL/lock detect logic was achieved using a standard CMOS PLL, an EPLD and a monostable with a time constant of about a minute. A simplified block diagram is given in **Figure 223**. The 4046 is configured in very much the standard manner. The VCO operates at 20kHz, and a divider within the EPLD reduces this to 50Hz, the frequency at which the phase detector operates. Incoming 50Hz from the transformer is clipped at ±6V8 before being squared by a comparator. The resulting 50HZ squarewave forms the phase detector input. Some experimentation was required to set the VCO resistor and capacitor values as those determined from curves in the PLL data sheet were found to be unsatisfactory.

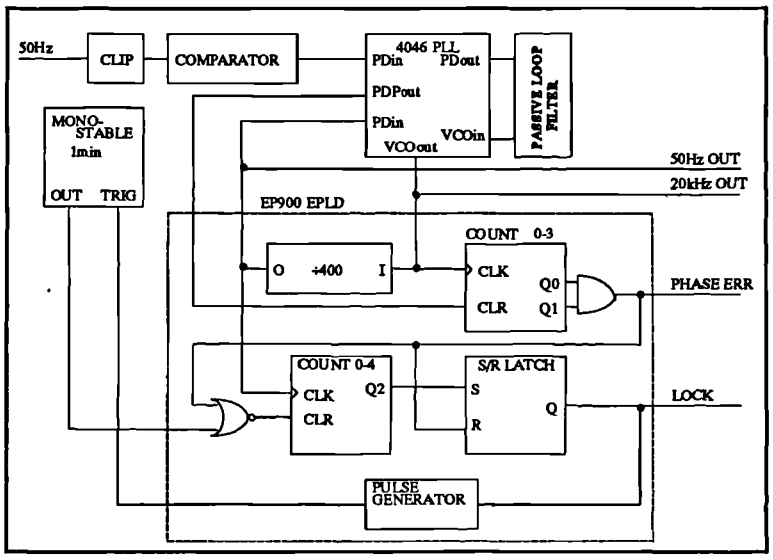

Figure 223 Simplified block diagram of phase-locked loop.

A pin on the PLL carries a logic-level pulse which corresponds in width to any phase error detected by the phase detector. The lock-detect logic operates by looking at the pulses on

this pin, and if they are wider than three cycles at 20kHz, in effect a phase error of 2.6 degrees, the lock detect pin is latched low and the 555-based monostable triggered. While the output of this is high (about a minute) a lock inhibit input to the lock-detect logic prevents the lock detect pin from being asserted, even if the lock is re-established within this time. This prevents the system from jumping in and out of lock. Finally, if lock is established and the monostable output is low, the system must retain the lock for four 50Hz cycles before the lock detect output is pulled high, enabling the utility feed mode of the converter.

6.3.8 DSP card

The DSP card used was the same Texas Instruments TMS320C50 evaluation card as was used in the low-power tests on the front-end. This card brings the complete DSP busses out to a set of header connectors from which it can be connected to the control logic.

6.3.9 Low-voltage housekeeping power supply

To supply the logic system with power, a small linear power supply was provided generating seven outputs: +5V regulated output for the logic, -5V regulated for the ADC devices, ±12V regulated for the ADC board op-amps and ±15V regulated for the transducers. A further 20V unregulated output was provided for the gate drives and the load change breaker.

6.3.10 Sample chains

The sample chains are based around Maxim MAX122 ADC devices, as for the low-power system. On the digital side the ADC devices are configured in the 'stand-alone' mode - although they are capable of direct interface to a microprocessor bus, this interface is too slow in this case using seven devices. The stand-alone mode of the ADC simply presents the results of the conversion at the ADC parallel data outputs once it is complete. The bus interface is provided by one pair of octal TTL tristate buffers per channel, the enable line being driven from the appropriate ADC enable line from the FPGA logic. The ADC also releases its 'busy' line

once the conversion is complete and these lines are used by the interrupt generator. On the analog side the topology differs slightly depending on whether the channel is sampling a unipolar signal such as the front end parameters and the rail voltages, or whether the signal is bipolar such as the inverter parameters. The ADC input voltage requirement is a bipolar signal of ±5V giving a two's complement output. Unipolar signals are offset by -5V and the difference added in software to provide a unipolar output, whereas bipolar signals are common-referenced. Each channel contains a fast op-amp buffer with a gain of 2 on each input.

The transducers providing the isolation from the power chain are incorporated within the screened enclosure containing the power chain circuitry. The currents are sensed using Hall-effect based current transformers. The voltage sensors fall into two types. For the inverter output, bandwidth limited by the LC filter, a Hall-effect based voltage transducer is used. However, these devices have a poor response time (40μs) which although acceptable for a 50Hz waveform, it will be of no use to the front end input voltage and rail voltages, both of which must be able to track a waveform with a 20kHz period. For these channels, unipolar transducers based upon a linear optocoupler and an operational amplifier were developed and found to be fast enough. The output of each transducer is a current; a proportional voltage is developed across a resistor and buffered at unity gain by way of an op-amp to drive the multicore screened cables between the sampling transducer board and the ADC board. **Figure 224** shows the basic layout of both the unipolar and bipolar channels. With a 5MHz clock the ADC devices achieve a conversion time of less than 3μs, and the data may be read as soon as the 'busy' line is released.

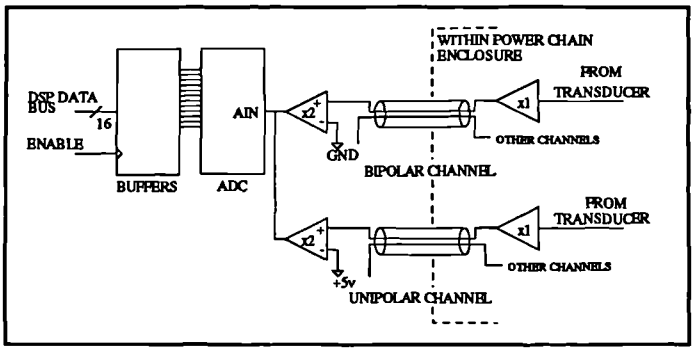

Figure 224 Basic layout of ADC channels.

6.3.11 Sample channel gains and scale factors

To maximize headroom within the ±2.5 or +5V (allowing for the x2 gain buffer) permissible at the input to the ADC board for the bipolar and unipolar channels, tracks were provided on the transducer PCB for a simple resistive divider to be implemented at the output of the unity gain buffer. This divider was required for some channels, particularly those using Hall-effect transducers in order to ensure that the transducer remained within its linear range of output currents and also that the output voltage remained within range. The range of the channel, and also the scale factor required in software to restore the value of the parameter is dependent upon the value of this divider as well as the transducer output resistor. The linear optocoupler based channels use a divider at the input to set the channel gain, and do not require this additional divider. **Table 13** lists the channels by name, and gives the forward gain (from power chain to ADC determined by measurement) together with the scale factor which is determined by multiplying the forward gain by 2048/5 (the gain of the ADC) and taking the reciprocal of the result.

Table 13 Table of sample channel gain, range and port number specifications.

CHANNEL	PORT	RANGE	GAIN inc. ADC	SCALE FACTOR
POSITIVE DC BUS	BASE+8	0-751.8V (opto)	5.464	0.183
NEGATIVE DC BUS	BASE+7	0-751.8V (opto)	5.464	0.183
ARRAY (INPUT) VOLTAGE	BASE+6	0-225.2V (opto)	18.214	0.0549
FRONT END INDUCTOR CURRENT	BASE+5	0-11A (Hall)	370.37	0.0027
INVERTER OUTPUT VOLTAGE	BASE+4	0-360V (Hall)	3.614	0.2767
INVERTER INDUCTOR CURRENT	BASE+2	0-16A (Hall)	128	0.0078
INVERTER LOAD CURRENT	BASE+3	0-16A (Hall)	128	0.0078

6.4 Hardware implementation and configuration.

The implementation of the complete hardware assembly was performed using clearly defined sections: the control logic and the power chain (incorporating the transducer board, the

gate drives and the low-voltage isolated housekeeping power supply). A diagram showing the basic implementation and connectivity configuration is shown in **Figure 225**. To avoid cluttering the diagram the low-voltage power rails have been left off the diagram,as have the input, utility and output connections to the power circuit.

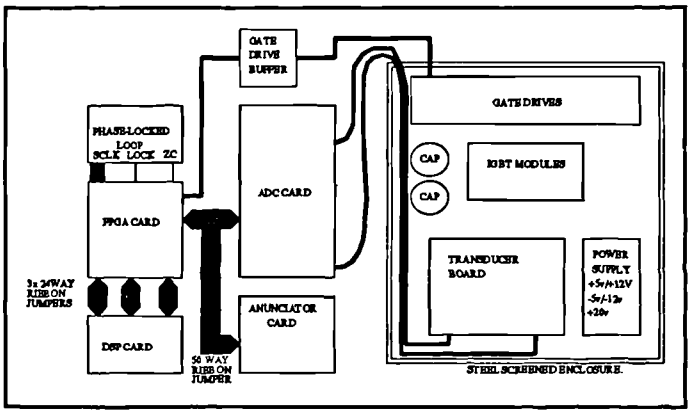

Figure 225 Hardware implementation block diagram.

6.4.1 Control logic implementation

On the digital side of the control, two plated-through hole (PTH) PCBs were manufactured. One of these carries the complete ADC subsystem and sample chain (except transducer and x1 buffer). The second, smaller board carries the FPGA, its configuration EPROM and associated power-up and buffering logic. The use of double-sided PTH boards allowed a greater packing density to be achieved and in turn a reduction in 20MHz bus line length over an equivalent non-PTH board. This leads to a reduction in the possibility of noise pickup, less degradation in the quality of fast pulses resulting in turn in better performance, and, in the case of the ADC boards, allows the correct board layout suggested by the ADC manufacturer to achieve best performance from the ADC devices.

Bus wiring between DSP and FPGA boards used three 24-way ribbon cables, with IDC PCB header sockets at each end. These mated with appropriate groups of pins on the PCBs. The bus between the FPGA, the ADC and annunciator boards used a 50-way ribbon cable terminated with similar IDC sockets, mating with quick-release plugs on the PCBs for easy removal during development. Most other signal wiring, including the transducer board to ADC board used Molex connectors. Care was taken with the earth arrangement to separate analog earths from digital earths and run them separately to a common earth point at the power supply. A small inductor/capacitor filter was also introduced to the +5v rail before being distributed to the logic boards in order to decouple it to HF noise still further.

Wiring from the transducer board to the ADC board is effected using two lengths of multicore screened cable, with the screens separately earthed at one end in order to reduce induced noise.

6.4.2 Power chain implementation

The power chain was wired using point-to-point wiring in 32/0.2 wire.. All connections between the power chain and systems outside the enclosure were made using 4mm shrouded plug/socket arrangements. The proprietary gate drive board consisted of a motherboard containing a power supply requiring +20V DC. This motherboard contained the six gate drive boards controlling devices in the resonant split rail supply and the inverter. A seventh, independent gate drive controls the single IGBT in the front end. The inputs to the gate drives are linked using a short ribbon cable to a buffer board containing a TTL buffer and resistors to drive the input optocouplers of the gate drives. This buffer is disabled during FPGA configuration in order to protect the IGBT modules during power up.

6.5 Software design and development

The complete controller software package consists of six individual files of TMS320C50 assembler code, which when assembled and linked produce about 1.7K of code in a common object file format. The basic functions of the software were separated into sections to simplify testing and development - in this manner each section of the complete system could be tested independently of the others. With this system, as with any other real-time system, timing is critical as all calculations must be completed within a single switching cycle in order to be able to update the hardware.

6.5.1 Development environment

Development of the code was undertaken using the production version of the PC-hosted Texas Instruments TMS320C50 assembler and linker as was used for the software written during

the low power tests, together with the debugger that came with the evaluation board. This debugger, although useful for verifying some of the calculation algorithms proved to be of little use in debugging interrupt-driven real-time code. The debugger uses interrupts as well and if a breakpoint is set it is impossible to disable the program interrupt independently of the debugger interrupt at the time of the breakpoint. As a result further executions of the program interrupt service code are not stopped. Most of the interrupt service code is quite straightforward and did not give rise to any severe problems.

6.5.2 I/O wait states

It was originally intended that with the use of the FPGA, clocked from the master 20MHz bus clock, zero wait state reads and writes could be used. However, one of the major disadvantages of the use of this type of FPGA is that the path timing is not guaranteed and is dependent upon the logic routing within the device. Owing to the approximate path delay being returned by the FPGA compiler software being 64ns it was necessary to insert wait states in order to obtain an error-free read/write from the FPGA. Experimentation showed that the insertion of a minimum of two wait states gave reliable operation of the FPGA-DSP interface.

6.5.3 Timing limitations.

The data requirement of the front-end is for samples of inductor current to be obtained at the start and the end of the on-time. This requires a minimum duty cycle limitation in order to allow for completion of the ADC conversion at turn-on, before commencing the next conversion. These ADC devices incorporate an internal sample/hold circuit so changes in the measured parameter will not affect the current conversion once it has been initiated. The front-end PWM write may thus occur as soon as the ADC conversion from the start of the cycle is over.

The inverter PWM channel requires samples of inductor current, rail voltage, output voltage and (for feedforward only) load current to be taken only at the start of the cycle. The double-buffered PWM generator must be written with the new duty cycle value before the start

of the cycle, and therefore must take place well before the interrupt generated once the ADCs have completed the conversion at the start of the cycle.

The complete timing requirement is shown in **Figure 226**. Note that the convert start signal is routed to all ADC devices. When a conversion is initiated, all seven channels will be sampled concurrently, but of the samples taken at the front-end PWM off-time, those relating to inverter parameters will be simply ignored.

It can be seen that to guarantee that the write of the new duty cycle for the inverter occurs before the physical start of the next cycle the write should take place early on in the computation time, suggesting that the control calculations should be ordered so those for the inverter should take place initially, followed by the duty cycle write, and finally the control calculations for the front-end. The front-end PWM write should occur between the start of the cycle and the completion of the ADC reads - placing it within the interrupt service code is satisfactory.

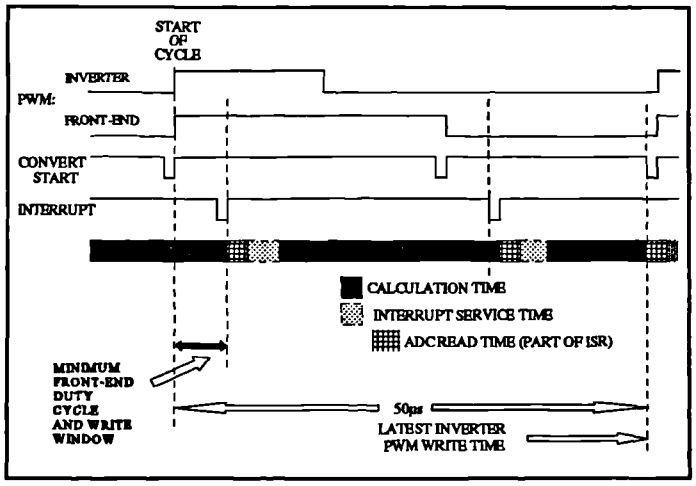

Figure 226 Timing of software against one cycle of PWM.

6.5.4 Software design.

The software was developed in six separate source files, each of which have a specific function within the complete controller. **Table 14** gives a cross-reference between the source file names and the function of the code contained within them. Two macro library files, ADC.MAC and ARITH32.MAC contain blocks of code which are used frequently throughout the software. Some simplified diagrams and a brief description of each section in turn follow.

Table 14 Software source-files/functionality cross-reference

SOURCE FILE	FUNCTION
ISR.ASM	Interrupt service code, ADC reads and scaling, front-end average diode current calculation, 50Hz reference lookup and sign determination
FE_SECT.ASM	Iterative (per-cycle) control code for front-end
INV_SECT.ASM	Iterative (per-cycle) control code for inverter
CONTROL.ASM	Control code. Calls front-end and inverter control code in turn after checking that all input/output parameters are within range. Performs shutdown if operating conditions are not correct and also supervises the transition between live (utility feed) and dead load operation.
MAIN.ASM	'Main' function. Provides an entry point, calls functions initializing workspace before transferring control to the code in CONTROL.ASM
SINEDATA.ASM	Contains the lookup table for the sine reference, does not contain any executable code.

6.5.5 Variable representation

As in the low power system, all variables and most constants are represented as 32 bit numbers arranged as 16.16 fixed point numbers - that is to say 16 bits of integer and 16 fractional bits. The exceptions to this are numbers which have only an integral, or a positive fractional value, such as the duty cycles. A 16-bit variable, depending upon arrangement, would either not allow sufficient precision or curtail the maximum integer value that can be represented.

6.5.6 Arithmetic macros

One of the macro libraries, ARITH32.MAC, was written containing macros for all the necessary 32-bit arithmetic functions including a 32 bit add and subtract, 32 bit by 32 bit multiply, and a 32 bit by 16 bit division which is required by the predictive algorithm. Initially a 32 by 32 bit division macro was developed, but this required a prohibitive amount of processing time (some 250 cycles, or 12.5μs at 20MHz). The 32 by 16 division code can make use of a conditional subtract instruction in the DSP instruction set which cuts the computation

time for this macro down to 41 cycles. The rounding of the divisor to the nearest integral value will not introduce a significant error as the divisor will be the sum of the rail voltages, a value around 800-900V of which a maximum error of 0.5V is a very small percentage of the divisor and can be ignored.

Another useful macro is the bounds checker. If the current DSP auxiliary register is set to point to a predefined limits table and the macro is called, the value in the accumulator will be limited accordingly and if the value exceeded the limits the zero flag will be set. An example of where this macro is used is in the duty cycle bounds limits.

6.5.7 ADC read macros

A further macro library, ADC.MAC contains two macros which perform ADC read and scaling. The port number, scale factor location and the result location are taken as arguments to the macro. The first of these macros reads the unipolar signals from the front-end. The 12 bit two's complement ADC output is converted to a unipolar number by complementing bit 11 before multiplying a (fractional) scale factor. A single 16 bit DSP multiply instruction performs this.

The second macro reads bipolar signals. Bit 12 is not complemented and the whole 12-bit number is shifted left by 4 to place the sign bit at bit 16. A 16 bit multiply by a fractional scale factor produces the 16.16 bit result which is shifted right by 4 with sign extension to compensate for the left-shift earlier.

6.5.8 Status flag bytes

As detailed in section 2.2.6, two status registers are used by hardware, and one 16-bit register forms the annunciator register. These three 16-bit registers map across to variables ST_SYSTEM for the system status word containing the lower eight bits to be written to hardware.

ST_HARDWARE contains the information read from hardware in the bottom three bits and ST_ANUN forms the annunciator status. The bit-field definitions of the bits of these lines are given in section 6.3.6. ST_SYSTEM, however contains additional software flags in the upper eight bits. The definition of these additional flags are given in **Table 15**. All flags are active-high except where specified as 'off/on' or 'live/dead' where the second value is the high condition.

Table 15 Definition of additional software status b in ST_SYSTEM.

BIT	DEFINITION
8	SOFT SHUTDOWN FLAG
9	HARD SHUTDOWN FLAG
10	DATA_VALID FLAG (SAMPLE 1 COMPLETED)
11	FRONT END MPPT ACTIVE
12	INVERTER LOAD DEAD/LIVE
13	INVERTER OFF/ON
14	FRONT END OFF/ON
15	UNUSED

6.5.9 Functions.

Table 16 gives a listing of each module in turn detailing the functions within them by name and purpose while **Table 17** lists the function imports and exports by source file.

Table 16 Definition of functions within the source files.

SOURCE FILE	FUNCTION NAME	PURPOSE
MAIN.ASM	_main	Acts as an entry point for the software. Calls all initialization functions from the other modules in turn to ensure that the workspace is initialized prior to transferring control to the 'CONTROL' function in CONTROL.ASM. _main does not return.
ISR.ASM	INIT_ISR	Zeros out workspace used by ISR.ASM, and transfers the initialized data used by the function from program memory to data memory. Sets the I/O wait states to 2 and initializes the two duty cycles to minimum for the front-end and 0.5 for the inverter. Annunciator is initialized to zero. PWM output is gated off

SOURCE FILE	FUNCTION NAME	PURPOSE
	ISR	Interrupt service routine. Called by hardware when ADC devices have completed conversion. Checks to determine whether sample is at start of switching cycle, or PWM off time. Reads ADC devices accordingly and writes front end PWM to FPGA register. If sample at start of switching cycle updates average diode current value, updates 50Hz reference for inverter before returning
FE_SECT.ASM	FE_INIT	Initializes workspace for front-end and copies initialized data from program memory to data memory.
	FE_START	Starts the front end control in an orderly fashion. Assumes interrupts are already initialized and that samples are being read. Enables front-end PWM after resetting the duty cycle to minimum and the outputs of the integrators in the control algorithms to zero.
	FE_STOP	Stops the front-end cleanly. Turns off the PWM generator to the front end and ensures that the utility is disconnected.
	FE_BLK_CONTROL	Front end control algorithm - one iteration. This must be called once for each cycle. Variables local to FE_SECT are maintained with the appropriate values between cycles. Identical to low power prototype in all but some of the constants. Will return without doing anything if FE_START has not been previously executed
INV_SECT.ASM	INV_INIT	Initializes inverter section and copies initialized data from program memory to data memory
	INV_START	Starts the inverter control in an orderly fashion. Assumes interrupts are already initialized and that samples are being read. Enables inverter PWM after resetting the duty cycle to minimum, the outputs of the integrators in the control algorithms to zero and ensuring the utility is disconnected. Will not allow inverter to start if front-end is not running
	INV_STOP	Stops the inverter cleanly. Turns off the PWM generator to the inverter but does not affect reference source
	INV_BLK_CTRL	Inverter control algorithm - one iteration. This must be called once for each cycle. Variables local to INV_SECT are maintained with the appropriate values between cycles. Identical to low power prototype in all but some of the constants. Will return without doing anything if INV_START has not been previously executed
CONTROL.ASM	INIT_CTRL	Initializes CONTROL.ASM workspace, transfers constants from program memory to data memory

SOURCE FILE	FUNCTION NAME	PURPOSE
	CONTROL	Main control function that contains the loop between interrupts. All functions except initialization are called from within this loop, which also contains bounds-checking code to ensure that the system does not run out of bounds. Checks include input voltage, DC bus voltage, excessive load current. CONTROL can shut down and restart the inverter as is necessary should any of these conditions be violated. CONTROL also supervises the transition between stand-alone and utility feed modes.
	S_CTRL	A cut-down version of CONTROL that does not perform any of the bounds-checking and only permits the system to run in stand-alone mode. Used for debugging, is redundant in the final system
	SHUTDOWN_H	Hard shutdown. Called by CONTROL in response to a possible fault or overload condition such as excessive load current. Drops all PWM signals, shuts down the system and loops forever. The code must be restarted and the system reset in order to resume operation
	SHUTDOWN_S	Soft shutdown. Called by CONTROL in response to a temporary condition such as input under/overvolt. The system can be restarted by CONTROL when the fault condition is lifted.
SINEDATA.ASM	No executable code	Contains the 200-word half-sinusoid lookup table. Values are from zero to 0.99 to enable them to fit in 16 fractional bits.

Table 17 Import/export listing by source file.

MODULE	IMPORTS	EXPORTS
MAIN.ASM	INIT_ISR (ISR.ASM) FE_INIT (FE_SECT.ASM) FE_START (FE_SECT.ASM) INV_INIT(INV_SECT.ASM) INV_START(INV_SECT.ASM) INIT_CTRL (CONTROL.ASM) CONTROL (CONTROL.ASM) S_CTRL(CONTROL.ASM) debug only	_main (entry point)
ISR.ASM	none	INIT_ISR
FE_SECT.ASM	none	FE_INIT FE_BLK_CTRL FE_START FE_STOP

MODULE	IMPORTS	EXPORTS
INV_SECT.ASM	none	INV_INIT INV_BLK_CTRL INV_START INV_STOP
CONTROL.ASM	FE_START (FE_SECT) FE_STOP (FE_SECT) FE_BLK_CTRL (FE_SECT) INV_START (INV_SECT) INV_STOP (INV_SECT) INV_BLK_CTRL (INV_SECT)	CONTROL S_CTRL INIT_CTRL
SINEDATA.ASM	none (data only)	none (data only)

6.5.10 Variables

The variables used by the system to represent samples taken from the ADC channels together with the status lines are defined in ISR.ASM. From here they may be imported and used by any other section that requires them. All other variables are local to the section that defines them with the exception of the average inverter inductor current. This is used by the CONTROL.ASM in bounds-checking and is calculated in INV_SECT.ASM. The variables are not modified by the importing code with the exception of the system status flag word and the hardware status flag word, and the ISR updates these variables at the beginning of each switching cycle. between which times they remain unchanged. Two further variables are exported from ISR, these being the duty cycle words for both the inverter and the front-end and these values are modified externally. The following list shows all of the system sample and status variables exported from ISR.ASM.

FE_P1	Array power sample at front-end on-time
FE_P2	Array power sample at front-end off-time
FE_P3	Array power sample at end of cycle
FE_ID_AVG	Average front-end diode current
FE_VO	DC rail voltage (used by FE_SECT)
FE_DELTA	Duty cycle input (front-end)
INV_REF	Inverter reference (sinusoid amplitude 0.999)

INV_VO	Inverter output voltage
INV_IO	Inverter load current
INV_IL	Inverter inductor current
INV_DELTA	Inverter duty cycle
DC_PV	DC positive bus voltage (inverter - identical to FE_VO)
DC_NV	Magnitude of DC negative bus voltage (inverter)

SINEDATA.ASM contains the lookup table for the sinusoid reference, and the start address of this table is contained in a single variable SINEDATA which is imported by ISR.ASM.

6.6 Control algorithm implementation

Three functions are involved with key aspects of the operation of the system. These are CONTROL with the operational bounds checking, FE_BLK_CTRL with the front-end control and INV_BLK_CTRL with the inverter control.

6.6.1 Front-end block control.

The front-end control code is almost identical to that which was used in the low power prototype. The only difference is that some of the delta-filter constants have been altered to make allowances for different steady-state values of duty cycle and to enhance stability. **Figure 227** shows the basic execution path. The code is basically a direct implementation within the framework of the DSP and hardware of the code that was developed in MAST during the simulation phase of the project. Relevant constants in the CONSTANT.INC include file are preceded with a 'FE_' prefix, and the most important ones together with their decimal values are listed below in **Table 18**.

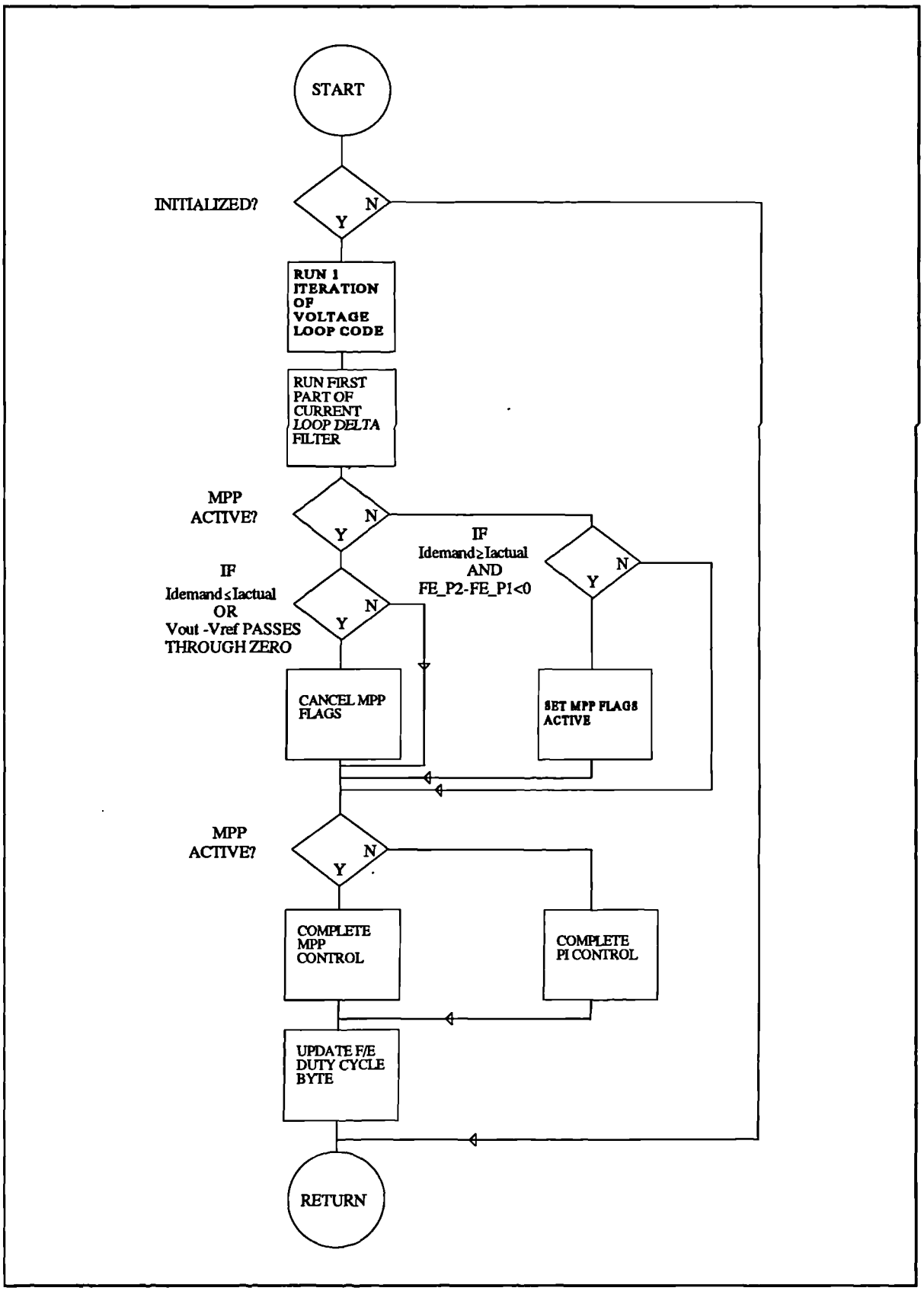

Figure 227 Execution path of front-end control.

Table 18 Table of controller constants used by front-end code

NAME	FUNCTION	VALUE
FE_GI_C	Current loop filter gain.	0.002
FE_A0I_C	Current loop delta filter parameter 1	1.005
FE_A1I_C	Current loop delta filter parameter 2	0.010
FE_GV_C	Voltage loop filter gain	64
FE_A0V_C	Voltage loop delta filter parameter 1	1.025
FE_A1V_C	Voltage loop delta filter parameter 2	0.05
FE_VREF_C	DC bus rail reference	450

6.6.2 Inverter block control

As with the front end, it has been directly coded from the MAST simulation template used during the simulation of the inverter sections - that is the algorithm is identical to that used in simulation. Once again some changes to the controller constants were found necessary in order to preserve stability in the noisy environment of the physical system, and to take into account some variation of component values that was found necessary. The predictive algorithm has been described in detail previously; and thus once again a simple diagram of the execution path of the inverter will be presented here in **Figure 228.** The reference count referred to in the diagram is simply a variable which is incremented or decremented according to the required change in operating point, and then the current demand input to the predictive controller is formed by multiplying this count value with the unit reference coming from the ISR. Relevant constants in the CONSTANT.INC include file are prefixed with the 'INV_' prefix and are listed below in **Table 19.**

Table 19 Table of controller constants used by inverter code.

NAME	FUNCTION	VALUE
INV_STEP_C	Reference count step	0.001
INV_T_ON_2L_C	The value of T/2L for the inverter, where T is the switching cycle and L is the filter inductor value in henries.	6.198×10^{-3}
INV_L_ON_T_C	The value of L/T	80.66
INV_PV_REF_C	Reference value for inverter output voltage (peak)	340
INV_GV_C	Voltage loop delta filter gain	0.039
INV_A0V_C	Voltage loop delta filter parameter 1	1.002
INV_A1V_C	Voltage loop delta filter parameter 2	0.004

The feedforward of filter capacitor and load current in the final system is slightly different to the approach used in simulation. The simulation used a quadrature version of the reference signal to calculate what the capacitor current should be. In the practical system it was found that to use this method would require more computation time than was available - the system is only just fast enough as is. However since inductor current and output current are measured, it is a simple matter to calculate the capacitor current by subtracting output current from average inductor current. An advantage of this method, other than speed, is that a measured value of capacitor current is used rather than a predicted value. The more measured parameters that are used in the system, the greater the accuracy of the system.

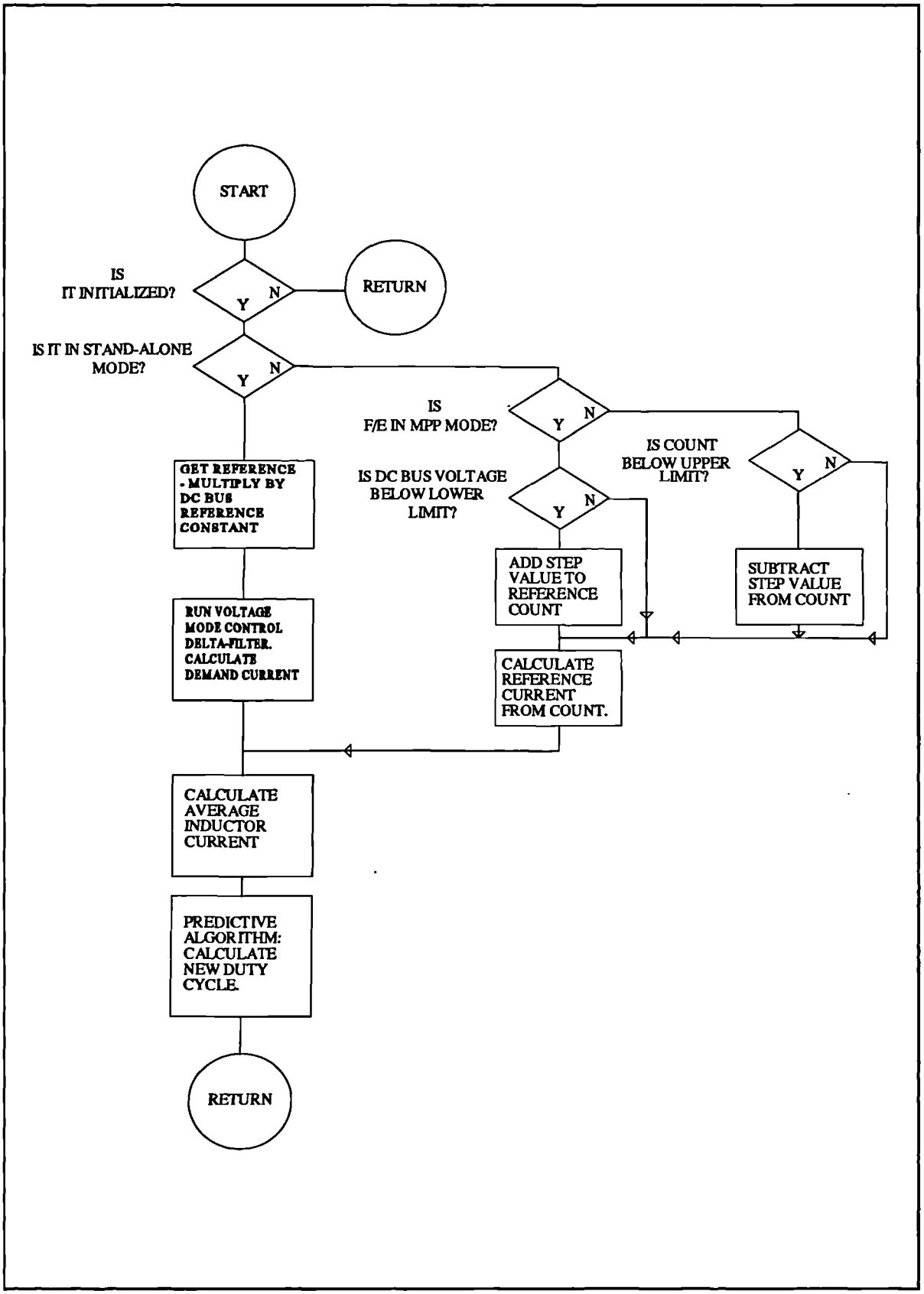

Figure 228 Execution path of inverter control.

6.6.3 Control function

The control function handles the error and fault detection, and supervises the transition between inverter modes. The basic execution path is detailed in **Figure 229**. This quite complex function is basically just an eternal loop, an iteration of which runs once each switching cycle on completion of the ISR at the start of the switching cycle and contains a group of condition tests. The second interrupt at the front-end PWM off time is transparent to the control code. All conditions that may result in a soft shutdown possess a hysteresis band (defined by a constant in CONSTANT.INC) in order to reduce the effects of noise causing the system to drop in and out of shutdown rapidly producing a 'spluttering' effect. All filter functions are called from within this function. Should a filter function be called when the appropriate shutdown flag in the status register is set, the call will have no effect and will not alter any variables. Most modifications to the annunciator status byte take place within CONTROL, the most notable exception being the MPP mode/voltage mode flag which is set in FE_BLK_CTRL.

Table 20 lists the faults that are trapped by CONTROL, whether they are recoverable and the value of the appropriate limit and hysteresis band. CONTROL constants in the include file are prefixed with 'CTL_', but some of the values in the limits tables are also used. **Table 21** lists these constants.

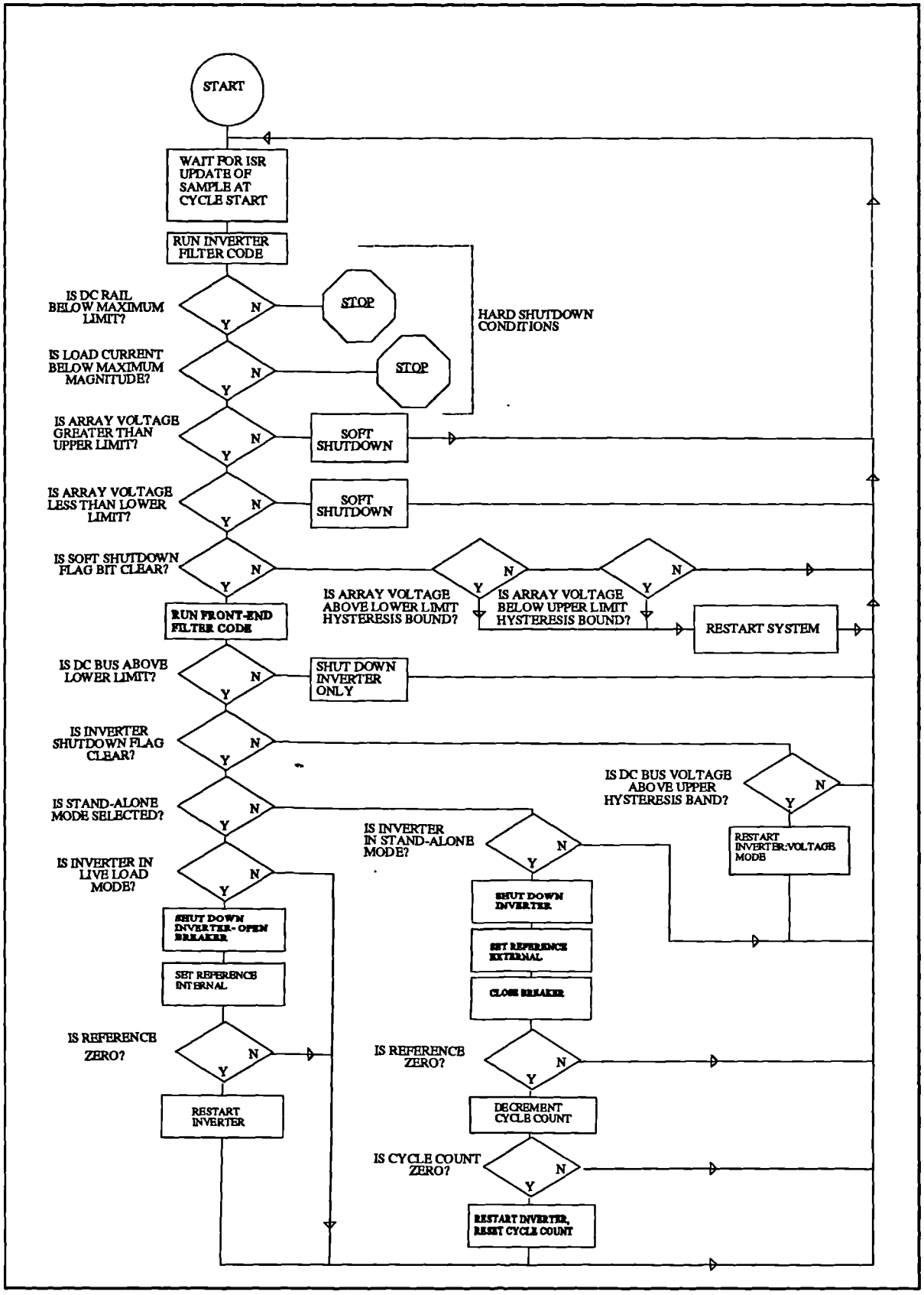

Figure 229 Execution path of control code.

Table 20 Fault condition and trap table.

FAULT	FAULT STATUS	LIMIT	HYSTERESIS BAND
DC bus overvolt	Non-recoverable	500V	N/A
DC bus undervolt	Recoverable: inverter shutdown only	370V	50V
Array voltage overvolt	Recoverable	220V	30V
Array voltage undervolt	Recoverable	50V	30V
Load current excess	Non-recoverable	12A	N/A

Table 21 Constants used in CONTROL.ASM

NAME	FUNCTION	VALUE
DC_PV_HLIM_C	DC bus upper limit	500V
INV_IO_HLIM_C	Output current limit	12A
FE_AV_HLIM_C	Array voltage upper limit	220V
FE_AV_LLIM_C	Array voltage lower limit	50V
CTL_AV_HLIM_HBAND_C	Array voltage upper limit hysteresis band	30V
CTL_AV_LLIM_HBAND_C	Array voltage lower limit hysteresis band	30V
DC_PV_LLIM_C	DC bus lower limit	370V
CTL_PV_LLIM_HBAND_C	DC bus lower limit hysteresis band	50V

It was originally intended to add two extra fault tests: to ensure that the DC rails were tracking within acceptable limits and to place an upper bound upon input current. The lack of available computation time prevented the addition of these tests to the code of CONTROL.ASM - errors associated with computation overrun occurred with even one of these extra tests. It was decided to leave out these particular tests for the following reasons. The input current is limited by the short-circuit current of the photovoltaic array, which if sized correctly for the inverter

should never cause excess current to flow - a short-circuit condition within the converter would lead to other conditions occurring which would bring about a shutdown. In addition, a bus tracking error is most likely to be caused by a fault condition - which, if serious, would be likely to be reflected into the positive bus and thus be detected by the front-end. The fault conditions that are detected are the ones most likely to result in damage to the converter if allowed to continue.

In conclusion, the code for the complete system has been written in a streamlined fashion, making use of the DSP delayed branch instructions wherever possible in order to speed up execution time and allow the controller software to complete an iteration within the boundaries of the switching cycle when executing along its critical (most time-consuming) path. The result is a complete controller program which worked well, and was found to function admirably within the framework of this project.

6.7 Testing of complete converter system.

The converter was tested in stages to ascertain that each stage functioned as desired before the next stage was tested. The first stage to be tested independently was the resonant split-rail supply.

Secondly the front-end was tested. This, being identical to the low-power prototype in all except the values of some of the delta-filter parameters, was not expected to display any unusual behaviour. It did indeed perform as well as the low-power prototype albeit at a higher power level once some minor design errors relating to the power device drive signals had been ironed out.

The inverter, being the first implementation of this scheme in hardware, was tested last, once the correct operation of the front-end and split-rail supply had been established. Once again, after some very minor (but time-consuming to locate) design errors in the reference generator the inverter did eventually function well, but in the course of testing provided some useful information relating to the performance of the predictive current mode control scheme

and this will be described in the following sub-sections. Unfortunately, tests of the inverter using feedforward of both capacitor current (and load current in the dead-load condition) had to be abandoned as the ADC device in the load current channel failed during testing. There was no additional hardware fault associated with that channel in particular, and as there had been some problems in the laboratory relating to static electricity it was suspected that a discharge had brought about the device failure. As there were no funds available to replace it tests continued with the feedforward calculations commented out of the control code. The result, however, shows excellent behaviour and it is quite possible that with careful development in a production environment feedforward may be dispensed with entirely, thereby reducing the requirement for sampling channels by one.

6.7.1 Preliminary predictive controller tests - a criticality

During the early testing and commissioning of the converter system, the predictive controller was tested independently of the front end and of the voltage loop. A 50Hz current demand signal was used as input, and a resistive load as output at a fairly low power level (about 100W). It was found initially to work, but a problem persisted in that the output current waveform, though sinusoidal in shape, contained a significant offset from zero which varied with load resistance. After considerable time this was finally traced to a small error in the scale factor of the sampling channel handling inductor current. The algorithm was found to be quite sensitive to errors in the reported value of inductor current, and the reason that this causes an offset is due to the manner in which the algorithm calculates average inductor current.

One sample is taken at the start of the switching cycle. To form the average current this sample is added to a calculated value which corresponds to the triangular portion of the inductor current throughout the cycle. This calculated value is based upon duty cycle and rail voltages as well as the (constant) inductor value and switching time. The diagram of **Figure 230** shows the effect of what will happen if the gain of the sample channel is out in a low direction, for the case when the current is not changing over the cycle. The calculated portion of the current remains

the same sign and magnitude, therefore for positive currents the average current is closer to the correct value; for negative currents it is further away resulting in asymmetry in the calculated average current. This results *in asymmetry in the output current* waveform in the opposite direction.

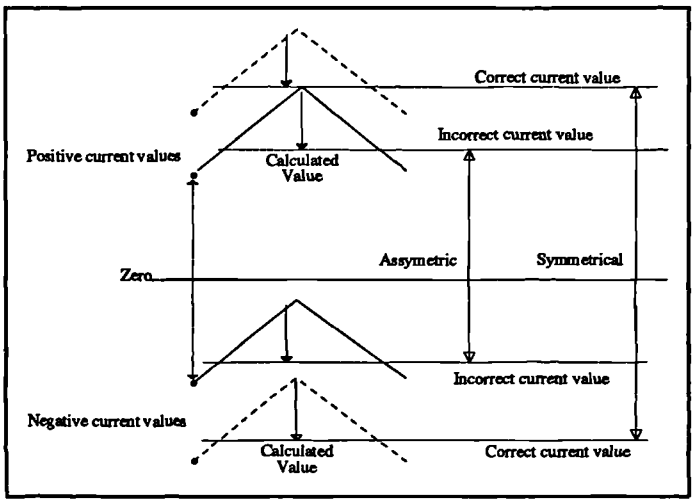

Figure 230 Source of asymmetry in predictive control algorithm.

If the channel gain is too high, the system can oscillate. When the duty cycle is set to provide the predicted value of inductor current in the next switching cycle, if the sample gain is too high the calculated average will be too high, with the result that the algorithm will try to reduce the current in the next cycle. This value will be reported too low, and the cycle repeats itself.

A recalibration of the current sample chain was undertaken, to a better degree of accuracy, and to further reduce the problem the scale factor for this channel in the software was trimmed to provide the best symmetry of output current waveform without any trace of oscillation. The result was a very well behaved predictive control system.

6.7.2 System test connections, power source and loads.

The complete converter system was wired as in **Figure 231** for all of the tests. Fuses within the converter itself, a smaller one in the branch to the utility feed and a further three in the input rectifier gave added protection to the silicon.

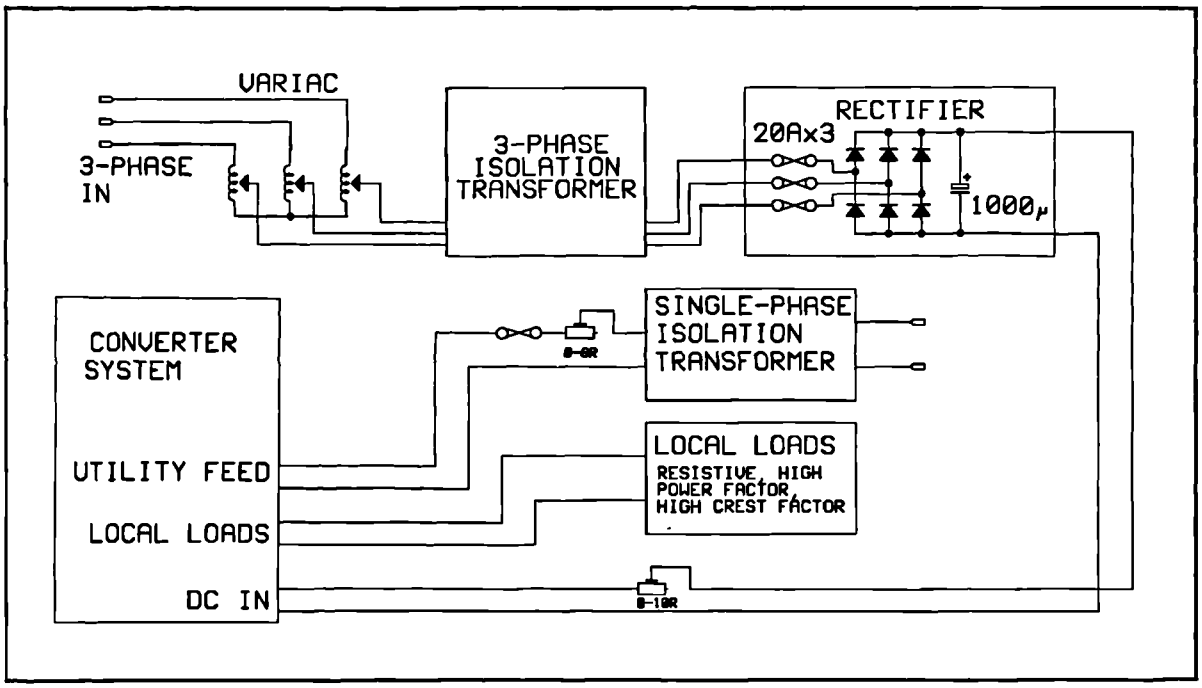

Figure 231 Converter wiring layout during tests.

6.7.3 Maximum power source.

As opposed to an actual PV array, a maximum power source was formed using a voltage source and a series resistor. This will, in fact have a worse characteristic than an array as the constant voltage portion below the maximum power point will not be as flat. There are some additional advantages to be gained from using this approach during testing. With a 500W solar array, apart from the problems of availability it is impossible to guarantee the operating point fixed during the time taken to perform the tests (the sun moves as do the clouds). As the front-end had previously been tested at low power with a PV array and found to function as expected, it is reasonable to expect an identical (even down to component values) high power version to behave similarly. Thus front-end tests were restricted to a check that the front-end could actually operate in both voltage mode and will operate at the maximum power point. Another advantage is the continuously-variable maximum power point, which could ensure that during the voltage-mode inverter load tests the system did not inadvertently run into maximum power mode because the light failed! The maximum power point is a function of the resistive divider value,

the variac position and both ohmic and non-ohmic resistances within the variac, rectifier and isolation transformer.

6.7.4 Loads - local

The local loads tested were those of the same type that was tested with the simulation model - resistive, poor power factor and high crest factor. The values and configuration of each of these loads will be described with the appropriate results. All of these loads were tested with the source set to ensure that the front-end stays in voltage regulating mode (with stand-alone mode, loads up to maximum power may be handled but to preserve the output voltage, the system does not track the maximum power point with load in stand-alone mode). The load power was set to around the 500W mark for each of these loads.

6.7.5 Loads - utility feed

The single phase utility feed (via the internal utility feed breaker) was fed to the utility via a very small resistor (0-6Ω) and an in-line fuse. The resistor is variable, and was placed there initially to provide a modicum of protection for the inverter IGBTs while preliminary tests were run on the utility feed/stand alone mode switching. Once this was perfected the resistor was reduced in value, and removed from the circuit. The small in-line fuse is at a much lower value, a 2A fast blow. This will allow the inverter to drive up to 480W into the utility, and its lower value will offer protection in the unlikely event of the DSP control software crashing and causing an uncommanded closure of the utility feed breaker, or if a short-circuit occurred at the breaker output for any other reason. This never happened during testing

An isolation transformer is the final link between the converter and the utility, and is present as a measure towards experimental safety. This transformer is a large one, capable of a throughput of over a kilowatt. The output of this is returned to the single-phase supply by way of a standard single-phase outlet.

6.8 Results and analysis

After an initial test of the front-end to determine that the maximum power tracking was functioning, the complete system was tested with the appropriate local loads in stand alone mode, and also with a utility feed.

6.8.1 Resonant split-rail supply.

The graph of **Figure 235** shows a set of traces taken from the resonant split-rail supply when it was tested at a power level of 1kW independently of the rest of the system in preparation for the publication of [52]. They show the rail voltages and the resonant arm current as both the envelope and the actual waveform as the 1kW load is switched in and out. The tracking can be seen to be excellent with no undesirable transient behaviour. The actual resonant circuit current waveform is a very clean sinusoid, except for a slight transient at the crossover point which is due to the deadband in the switching.

6.8.2 Front-end.

The system was started, and the variac set to deliver an open-circuit voltage of about 120V. A resistive load on the output of the inverter together with the supply series resistor was adjusted to force the embedded maximum power tracker of the front-end just into maximum power mode with the source power at 400W approx. The resulting trace of converter input voltage and input current may be seen in **Figure 236**. The current waveform shows the expected sawtooth at the front-end switch turns on and off. The small glitch on the voltage waveform happens to coincide with the switching transitions of the split-rail power supply and show that some noise is still emitted from this, although it appears not to have any effect upon the operation. The power at the inverter load, measured on a Holtek AC power analyzer, was 322W at 50Hz, with unity power factor. To show that the front-end is indeed tracking maximum power, the curve of **Figure 237** shows the instantaneous input power (the product of the input voltage and current) across the current rise-time portion of one switching cycle. This curve

shows a clear maximum, with the points at the start and end of the on-time straddling this maximum. The actual average operating power will be slightly less than maximum and may be found by calculating the area under the curve and dividing by the value of the on-time. MATLAB was used for this calculation and the average maximum operating power was calculated as 374W. The load power of 322W gives rise to a complete converter efficiency of 86%. However, 7.5W is dissipated in each of the four dissipative snubbers around the split rail supply, implemented in this manner for convenience and dissipating a total of 30W. If these snubbers were replaced with a non-dissipative design the efficiency could be improved to 94%. In a commercial environment the efficiency would be expected to be lower than this, possibly around 90-91% since lower rated and cheaper components would be used.

To improve on the proximity of the average power track to the true maximum power point, the front-end inductor value would have to be increased, or the switching period decreased in order to reduce the amplitude of the current ramp. An array with a less sharp maximum power point, such as one produced from amorphous silicon would track closer to the true maximum. The 1mH inductor was used due to availability, however the use of a larger inductor would mean modifying the delta-filter controller coefficients in order to accommodate the changes in converter dynamics that this would bring about.

6.8.3 Inverter load tests: resistive load.

In this test, the source was set up with a maximum power point in excess of the load power to ensure that the front-end remained in voltage regulating mode throughout the test. For a resistive load, a simple power rheostat was connected to the output of the inverter via a switch thereby allowing a heavy load to be switched in and out while the converter is running. With the rheostat switched out the only effective load that remains on the inverter is the output voltage sense transducer - this draws a current of approximately 10mA and forms a very light load. The system was started and the rheostat set to draw 545W when connected. Two traces were obtained of inverter output voltage and current (note inverter output current, not inductor current). The first of these traces (**Figure 238**) shows the inverter parameters as the heavy load is switched in,

and the second (**Figure 239**) when the load is switched out. The system can be seen to be very well behaved, there is no visible transient in the voltage waveform as the load is switched in or out, and the amplitude of the output voltage, a measured 238V r.m.s., does not change. The slight high frequency ripple that can be seen at the crest of waveforms when the load is switched in is slight oscillation due to the gain of the delta-filter controller parameters in the voltage loop of the inverter. This was found to be able to be eliminated by reducing the gain (G_v) of the voltage loop PI compensator, but at a penalty of output voltage regulation. This oscillation was not found to be a real problem, only occurring close to the maximum output power and it did not appear to destabilize the system significantly. The existing control parameters were thus retained in the interests of voltage regulation. Overall, the transient performance with a resistive load is very good, showing no unwarranted transient at the point of load transition. If feedforward was available it could not make a significant improvement to these waveforms.

6.8.4 Inverter load tests: poor power factor load.

A poor power factor load was formed using the simple L-R circuit of **Figure 232**. The inductor was air-cored, thus eliminating any problems associated with saturation at high powers. The resistor was the same power rheostat (0-300R) that was used in the resistive load tests. The inductor had quite a high series resistance, around 86R, and during the test it was found possible to reduce the rheostat to zero resistance in order to achieve the worst possible power factor. The system was started with the source set as for the resistive loads, and the rheostat reduced to give the worst possible power factor.

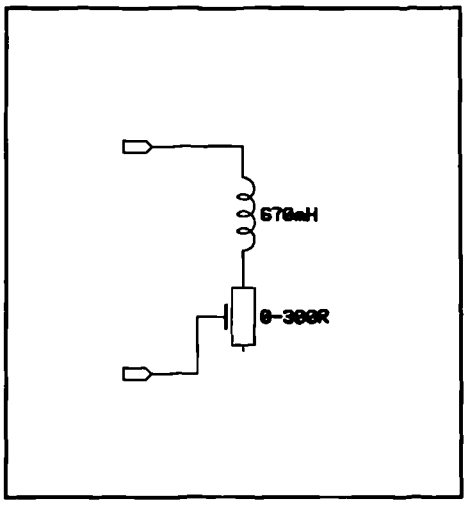

Figure 232 Poor power factor load.

The resulting trace of inverter output voltage and current is shown in **Figure 240**. The measured load power factor was 0.379, at a real load power of 96.2W and an apparent power of 252VA. The output voltage remained at 238Vrms and the trace shows no sign of distortion or oscillation

on either the current or the voltage trace. There is no reason to expect that the converter will behave differently with still worse power factors, or with heavier reactive loads.

6.8.5 Inverter load tests: high crest factor loads.

The high crest factor load is commonly found in linear and switch-mode power supplies, caused effectively by the capacitative filtering of rectified mains. To simulate this type of load the circuit of **Figure 233** was constructed and connected as a load. The system was started and the resistor, again a power rheostat, was adjusted to dissipate 300W and the trace of inverter output voltage and current is shown in **Figure 241**. The load power was set slightly lower than maximum owing to the appearance of oscillation once again on the crests of the current waveform. This is due to the fact that the instantaneous power at the crest is very much higher than the average power, in this case the peak current is 5.12A compared to a measured load current of 1.77A DC. This is a crest factor of 2.8:1, and a peak instantaneous power of 1740W. This peak is enough to destabilize the control algorithm slightly - once again it was found that changing control parameters in the inverter voltage loop could reduce the oscillation at the penalty of voltage regulation.

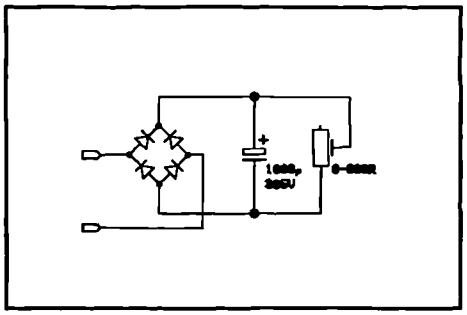

Figure 233 High crest factor load.

It is with this type of load that (in simulation) load current feedforward was found to be most effective at restoring the shape of the voltage waveform - and may have allowed control parameters to be redefined so as to reduce the oscillation without sacrificing voltage regulation. However the performance without feedforward is still quite good, the voltage waveform shows the expected squaring off but without significant reduction in the peak voltage. The r.m.s. output voltage as measured on the Holtek power analyzer was 235V - showing acceptable voltage regulation.

6.8.6 Inverter load tests: live load feed

It is with this type of load that the converter will run continuously in maximum power mode. During the tests the source was set to provide a slightly lower maximum power of around 300W as measured at the input. The first set of tests was carried out using a 240V feed through an isolation transformer. The output of the converter fed the utility, but also a small resistive local load dissipating 167W. The system was started up running in voltage regulation mode, the phase locked loop switched on and the converter allowed to switch over to live mode. The waveforms of inverter output voltage and output current may be seen in **Figure 242.** During the test the real power fed to the mains was measured as 109.3W.

The first thing to note is the quality of the voltage waveform. This is effectively the mains voltage, and this was measured at another outlet within the laboratory with the converter off-line to ascertain that this was not caused by the converter. The mains voltage waveform exhibits this clipping at the peaks, and is probably due to the presence of a large number of computers, low voltage power supplies and offline switch-mode converters within the building, some in the same laboratory as the converter and, all drawing loads with a high crest factor resulting in this rounding of the peaks due to line impedance, transformers and so on. Unfortunately there is little that can be done about this.

However, the current waveform shows a clear aberration at its peaks. This was investigated and traced to a problem relating to inverter duty cycle limits. An explanation follows.

It was initially intended in the design for the duty cycle to be continuously variable from a very low lower limit (0.05) to quite a high upper limit (0.95). However, it was discovered that if the duty cycle was reduced at the lower end much below 0.1 there was a problem with severe glitching and spiking on the lower edge of both the output voltage and inductor current waveforms which if allowed to continue at high voltages resulted in failure of the IGBT devices. Suspecting the presence of a shoot-through condition the system was started in open loop with

the control software stopped and the duty cycle set by hand using the debugger. At full power (c. 500W) there was no sign of a shoot-through on the waveform of the current flowing in either the positive or the negative DC bus supplying the inverter half-bridge for all duty-cycles between 0.05 and 0.1. However a 100kHz ring of very large amplitude was found on the leading edge of the current waveform flowing through the device that was switching on. At duty cycles of less than 0.1 this ring will occur within the time between the cycle start and the completion of the sample conversion in the ADC devices, marked by the assertion of the DSP interrupt line and it was suspected that interference from this ring was responsible for corruption of either the sample values, or worse, the gate drive signals. The presence of a snubber on the inverter devices appeared to worsen this ring and the snubber was eventually removed. Many attempts were made to suppress it including experimenting with snubber values, placing small low-inductance capacitors across the DC busses close to the inverter IGBT module but none appeared to be successful in allowing operation at low duty cycles and eventually the lower duty cycle limit was raised to 0.1. It is interesting to note that no glitching was present during the positive half cycle, indicating that there was no interference with the control algorithm at this point which ties in, as at the higher end of the duty cycle range the ring will not occur at the same time as an ADC conversion, or a duty cycle write.

Unfortunately the adoption of lower limits can cause a problem with a 240V live load. The predictive algorithm increases or decreases the output current by developing a voltage across the output filter inductor. At the peak of the voltage waveform while feeding a live load, the average voltage at the center junction of the two half-bridge devices must be sufficient to equal the sum of output voltage and the required inductor voltage in order to increase the current to the demand value (see **Figure 234**). The load current will actually start to fall if either the DC bus magnitude is insufficient or the duty cycle limits are too low, and this behaviour may be seen at the current peaks in **Figure 242**. For a waveform of 340V peak, and a DC bus magnitude of 450V per rail, to be able to pass current into such a load the average half-bridge output

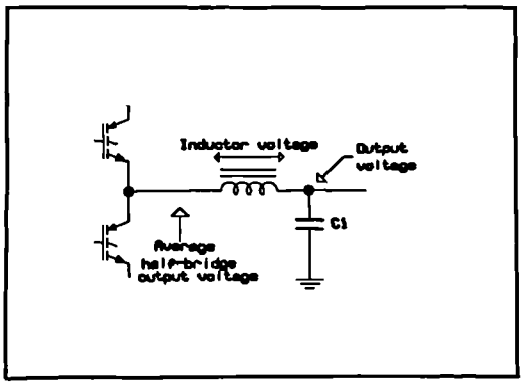

Figure 234 Inverter output voltage formation.

must be greater than 340V, i.e 450(2δ-1)>340. The duty cycle must thus be greater than ((340/450)+1)/2, or 0.88. For the negative half cycle the lower limit is 1-0.87=0.12. However this is the barest minimum, and does not take into account both the deadband and the voltage sustained across the inductor in order to allow the output current to increase. It was found that the 0.1 limit forced by the noise problem was insufficient for a 450V bus and a 340V peak utility voltage as can be seen in the waveforms.

To circumvent this problem the isolation transformer feeding the utility had two 125V secondaries which were connected in series to obtain a 1:1 ratio with the primary. The tests were run again at a live load voltage of 125V using one of the secondaries where all behaved as it should with a live load. The results of the tests may be seen in **Figure 243**. The slight rounding of the peaks of the current waveform is very likely due to the sudden increased current demand from the load at this part of the cycle from the large number of high crest factor loads - the clean nature of the current waveform when driving a dead load would suggest this. During the preliminary testing a test of the predictive control loop alone was made - the voltage loop was disconnected and a 50Hz current demand signal of a fixed amplitude was used as the input to the predictive block. The result here was a perfect sinusoid into a resistive load, and this would suggest that the aberration is a function of the poor utility voltage waveform. This rounding is only slight, however, the power analyzer reported a total power factor at the inverter output of 0.992 which is acceptable.

With live loads, when the inverter voltage loop is not used, load current feedforward has no meaning, and would be switched out. The presence of capacitor current feedforward would normally aid in correcting for the phase displacement brought about by the inverter output filter capacitor. However, the traces of **Figure 243** show no significant displacement between current and voltage, and this is backed up by the power factor reading of 0.992. The benefits of feedforward would seem to be very slight in this case.

6.9 Results: figures.

These may be seen below, in the order in which they are referred to in the text. In addition to the oscilloscope traces **Figure 244-Figure 248** show photographs of the actual hardware used.

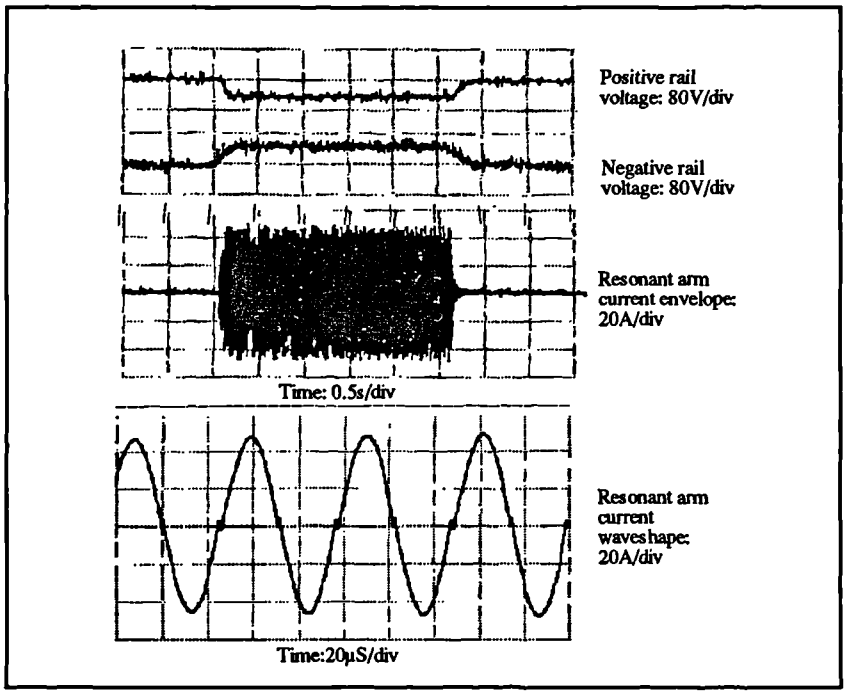

Figure 235 Resonant split-rail supply tests.

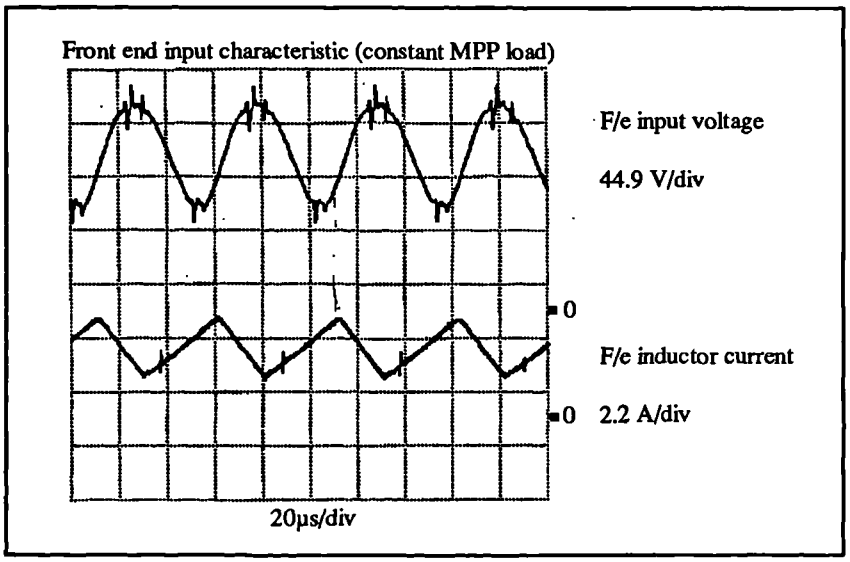

Figure 236 Front-end maximum power test: front end input voltage and inductor current versus time.

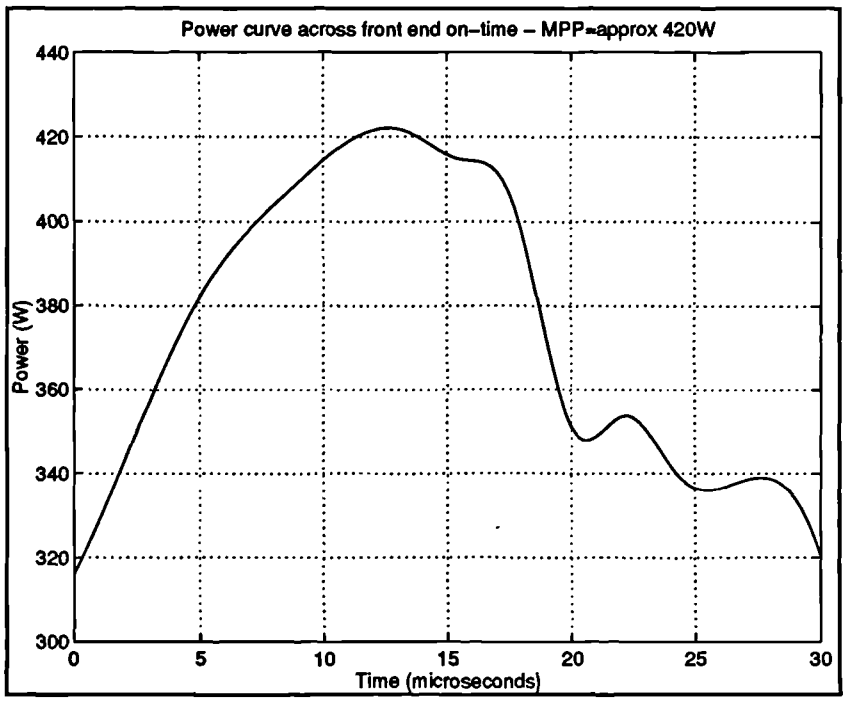

Figure 237 Input power curve taken across the duration of inverter switch on-time (current ramp rise).

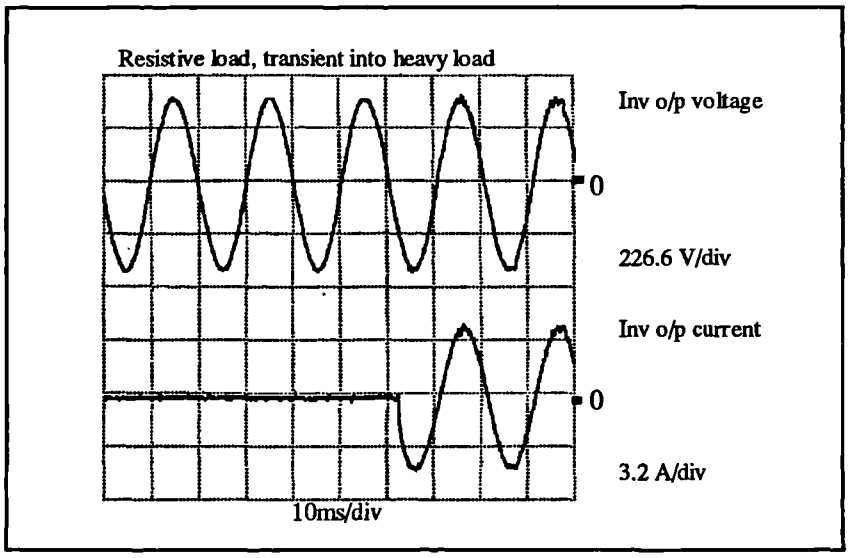

Figure 238 Inverter output voltage and output current transient - resistive load - light load to heavy load.

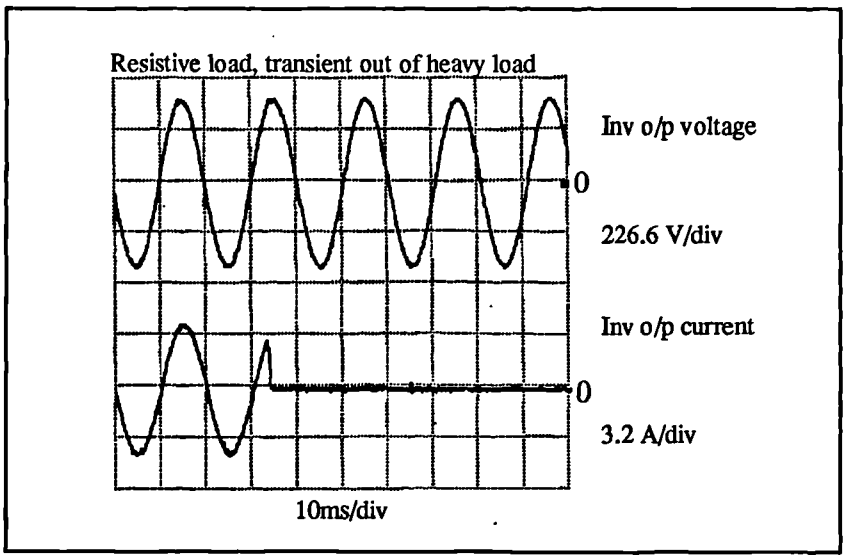

Figure 239 Inverter output voltage and output current transient - resistive load - heavy load to light load.

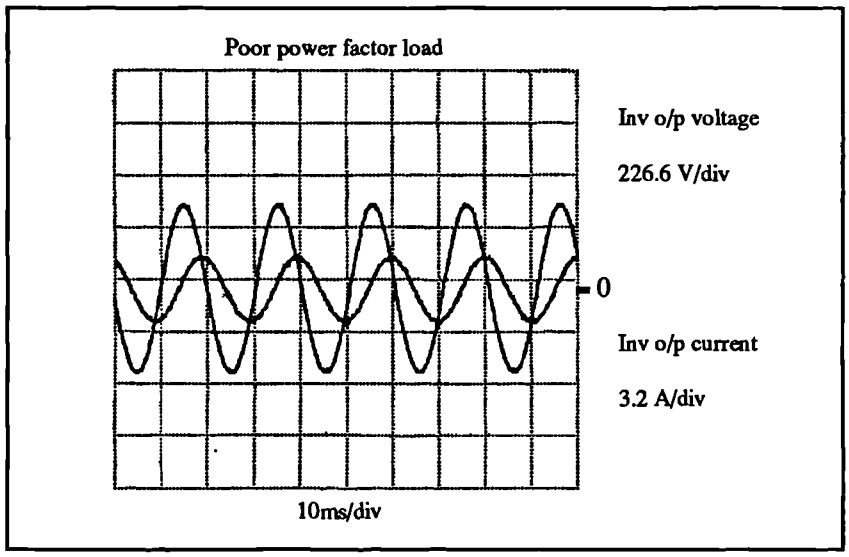

Figure 240 Inverter output voltage and output current - poor power factor load.

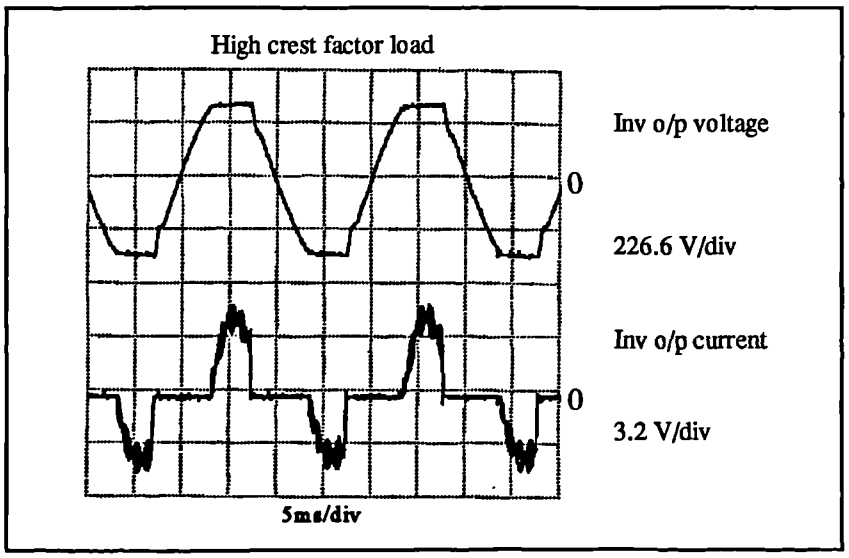

Figure 241 Inverter output voltage and output current - high crest factor load.

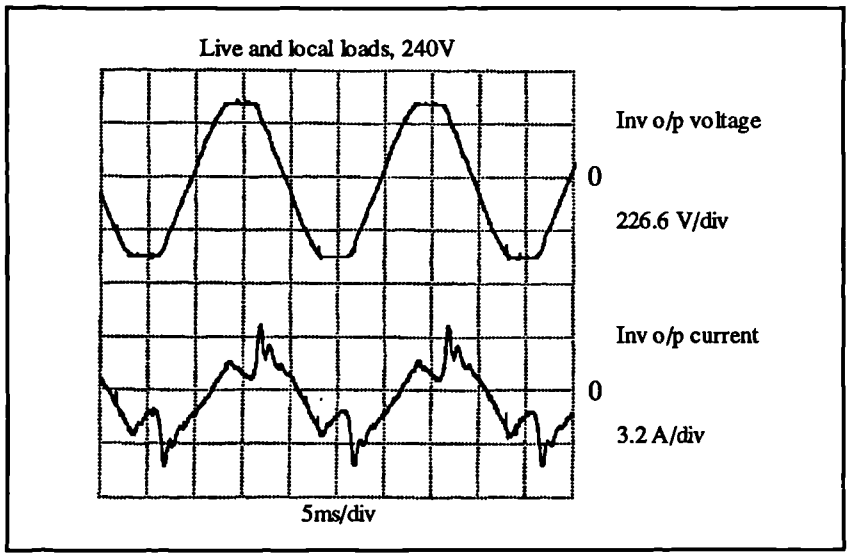

Figure 242 Inverter output voltage (utility voltage) and output current - utility and local load feed at 240V.

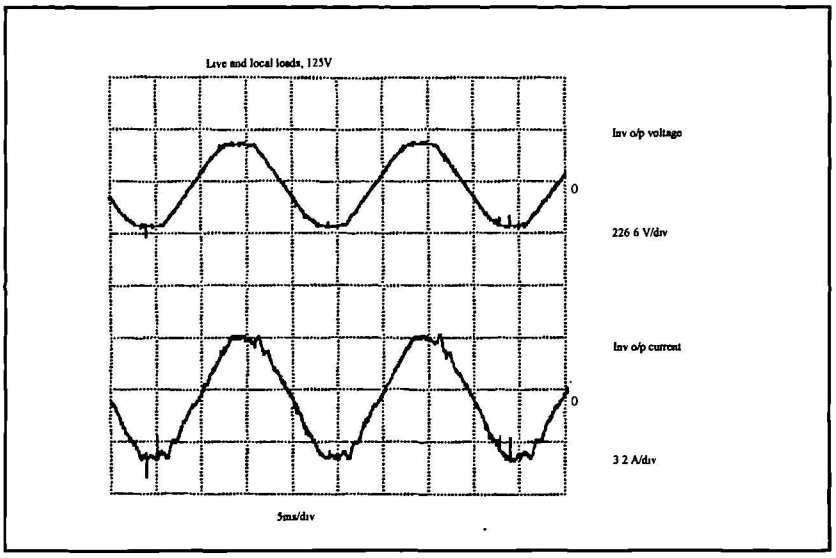

Figure 243 Inverter output voltage (utility voltage) and output current - utility and local load feed at 125V.

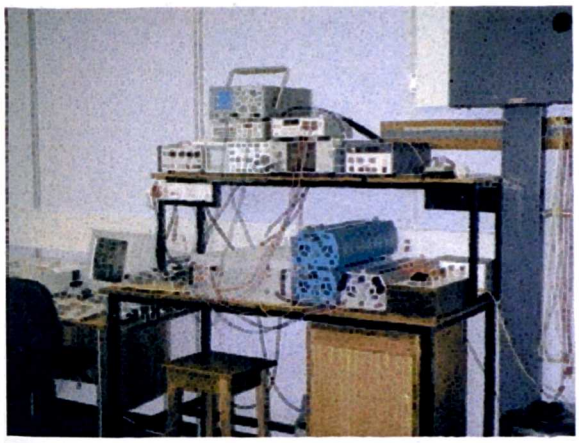

Figure 244 Complete high power system.

Figure 245 PC-hosted DSP development environment.

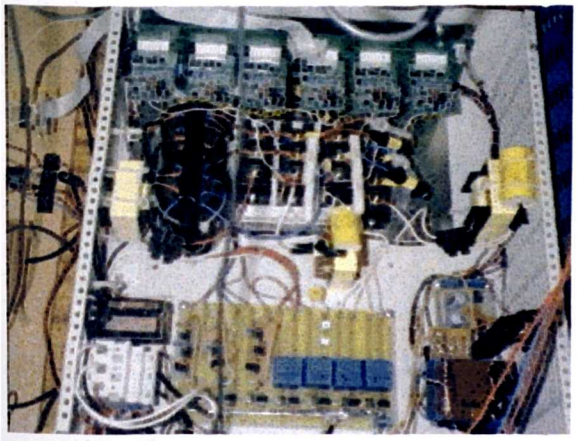

Figure 246 Power chain hardware

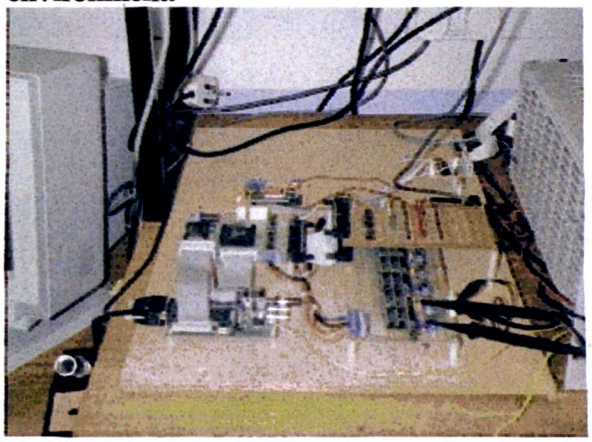

Figure 247 System controller including DSP card.

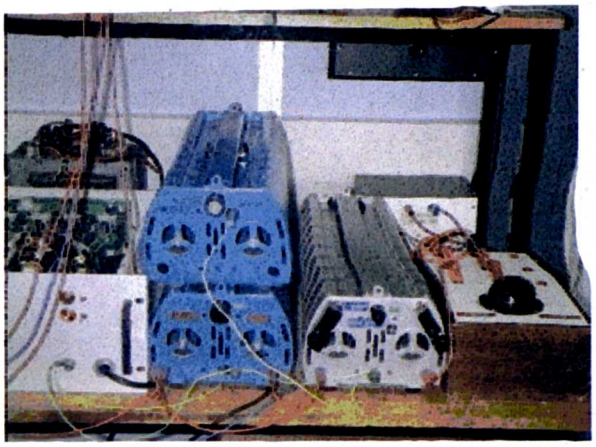

Figure 248 Rheostat load banks

6.10 Evaluation of results

In general comparison with the results obtained from simulation, it can be seen that the practical system performs very well, if not better in the light of the fact that there is no feedforward in the practical system. The simulation was only intended to verify that the technology was viable and worth prototyping, rather than for a direct comparison to be made on a trace-by-trace basis between the simulated system and the hardware using the simulation as a benchmark for the hardware performance. An exercise such as this only serves to demonstrate the accuracy of the simulator, which is not operating under the same conditions as regards noise, ADC characteristics etc - if these parameters were included in the simulation each simulation run would take a prohibitively long time to both implement and execute, and still would not be perfectly accurate.

The performance, judged exclusively upon the hardware, is very good and meets the expectation of the design. Efficiency figures, ignoring the power dissipated in the RC snubber networks which would not be present in a production version, are very good at 94%. The tracking of maximum power is good, but the system could be made to track closer to maximum power by increasing the inverter filter inductor value, or by increasing the switching frequency (this would require a faster DSP). Furthermore the noise problem relating to inverter switch turn-

on will require some attention (a development problem) to enable operation across a wider range of duty cycles and thus into a 240V load without requiring excessive DC bus voltages. The 125V load, however, demonstrates that the system can operate successfully into a live load.

SECTION 7: Conclusions, and recommendations for future work.

The converter system, as it stands, shows that the technology developed with a view towards producing a multipurpose photovoltaic power conversion system is quite viable. The basic front end is capable of driving fixed-voltage DC loads up to the maximum array power, or DC loads at maximum array power with an output voltage varying with load. With the addition of the inverter the system can drive both stand-alone AC loads as well as operate in a grid connected mode. To this end the overall goal of developing a flexible converter that was not in any way application specific has been achieved. Novel control techniques have been developed to overcome the limitations of conventional control arrangements when the converter is driven from a source with a maximum power point. The inverter uses a fast predictive current mode control scheme, recently developed and not widely used. The speed of this system has been shown to aid stability while driving various forms of load and its ease of implementation within the digital domain makes it an ideal choice in this type of system. A novel split-rail generator based upon resonant techniques allows the single phase inverter section to generate a true bipolar output and maintains the integrity of the common (ground) rail.

A comprehensive photovoltaic cell data acquisition and characterization system has been developed with a view to making the characteristics of photovoltaic cells available to power electronics engineers within a simulation environment. Such a system allows the power electronics engineer to develop converter systems that perform well across the full range of irradiances and temperatures experienced by the array without having to worry excesssively about the details of the manner in which the arrays are configured mechanically.

As to the operational aspect of the system, some developmental work would need to be undertaken in order to eliminate the noise problems - this could entail significant alterations to the layout. The controller would benefit from added protection and fault trap code - to

implement this either a faster DSP or a lower switching frequency would have to be used. However a large amount of time is occupied as a direct result of the requirement for two wait states on the FPGA based I/O accesses. If this could be reduced quite a significant amount of time could be freed for extra code. To do this would require a move away from FPGA technology and its attendant path delay problems. A better choice for logic implementation would be one of the larger EPLD devices made by Altera, some of which have greater capacity than FPGAs. In addition the development software is more readily available, is PC-hosted, and at the time of writing is much cheaper than the Xilinx 'XACT' software, as well as being considerably easier to use. In a production environment, depending upon volume it may well be worthwhile considering the logic implementation in a custom gate array, which would certainly be faster and cheaper over long production runs.

The DSP, a TMS320C50 fixed point unit, is already being overshadowed by faster DSP devices which have a floating-point core. Such devices, although still quite expensive will almost certainly drop in price with time. A DSP with a floating-point core would simplify the calculations in what is a calculation-intensive system considerably, and may even allow some of the time-intensive arithmetic macros to be dispensed with.

The power chain itself would benefit from slightly better gate drive arrangements. The gate drives used in this system were commercial units inherited from a previous project. During early testing of the system when the algorithm code was being perfected and some instabilities were present possibly generating noise, inverter IGBT damage was encountered which could not be explained given the manner in which the deadband generator operated (at no time could both devices in a half-bridge be on simultaneously). Checks with an oscilloscope at the gate drive outputs showed that there was no overlap, and it was felt that the failures were noise related, most likely resulting in interference with the operation of the gate drives. Although these gate drives had a form of built-in shoot-through protection which was designed to turn off the device if the collector voltage started to rise during the on time, failures still occurred. This suggested that the gate drives were being affected and the protection circuitry was not operating. Once the controller had been implemented fully, and the control algorithm perfected, no more failures occurred suggesting that noise caused by the instabilities was causing the gate drive corruption.

Extension of the inverter section to drive three-phase loads would be a matter of simply providing three sets of switches and tripling up the control algorithm using three 120° reference signals generated from the same lookup table in memory. If the grid-connected operation of this type of converter at higher powers was to become more widespread, a more detailed study of the effects of harmonics in the inverter output [60] may be necessary, and more effective methods of filtering [61] may need to be employed. With stand-alone loads the harmonic output only needs to be considered in terms of radio-frequency interference and whether or not the harmonics cause losses in the load (for example, rotating machines).

To sum up, the complete converter was found to be effective, relatively robust and the control technology would certainly form a useful basis for a commercial system. The novel control algorithms behave very well indeed, although a larger front-end inductor may be useful to provide tracking closer to the array maximum power point. The predictive control scheme works well, providing the gain of the current sampling channel is accurate, and the resonant split rail supply is very useful, particularly in the light of its open-loop operation even if it does require an extra two power switching devices.

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APPENDICES

APPENDIX A Full set of experimental and calculated data plots.

Below may be found a full set plots of each of the fifty experimental I/V curves as obtained from the polycrystalline solar cell used during the development of the model. The plots were those exported by the characterization system. On each set of axes may be found four curves. The first of these is the experimentally-determined data. The second set is the curve fitted to the experimental data by the curve fitting subsystem. The third is the power output from the cell obtained from the experimental data, while the fourth is the calculated power output from the cell based upon the fitted curve. The fitted curves have been back-calculated using the complete model from the values of temperature and irradiance at which the experimental data set was taken and the constant set extracted for the cell. As can be seen in all cases the fit is excellent, there is little deviation between the fitted curve and the experimental one exemplified by the fact that the obvious maximum power points from the fitted power curves are coincidental with the maximum power points from the calculated curves. The captions to the plots give the irradiance (arbitrary units) and temperature (Kelvin) at which the data set was taken. A legend may be found in the top left hand corner of the plots, but some of the plots are coincidental with each other and are thus hard to distinguish!

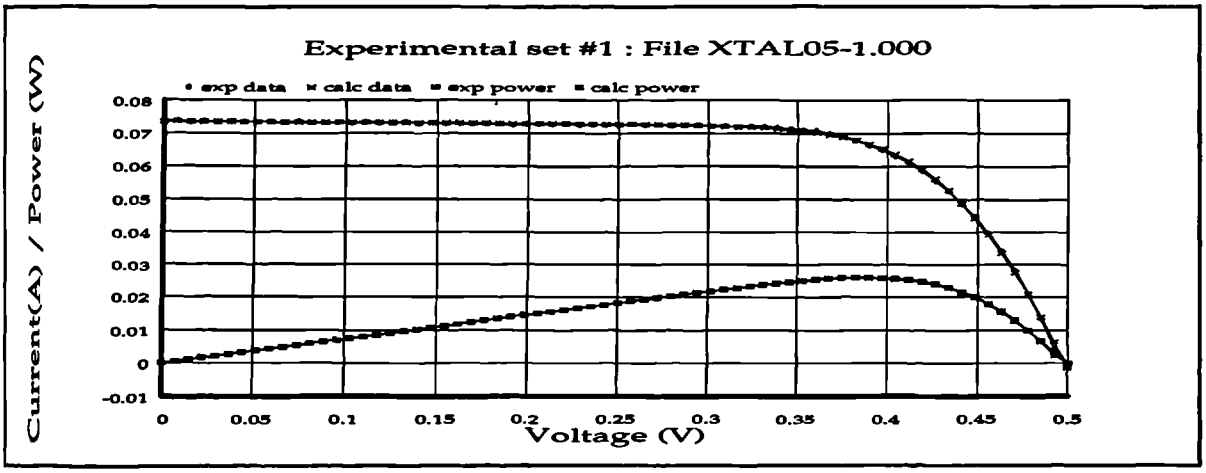


Figure 249 I/V plot: irradiance 4008.6 temperature: 300.2

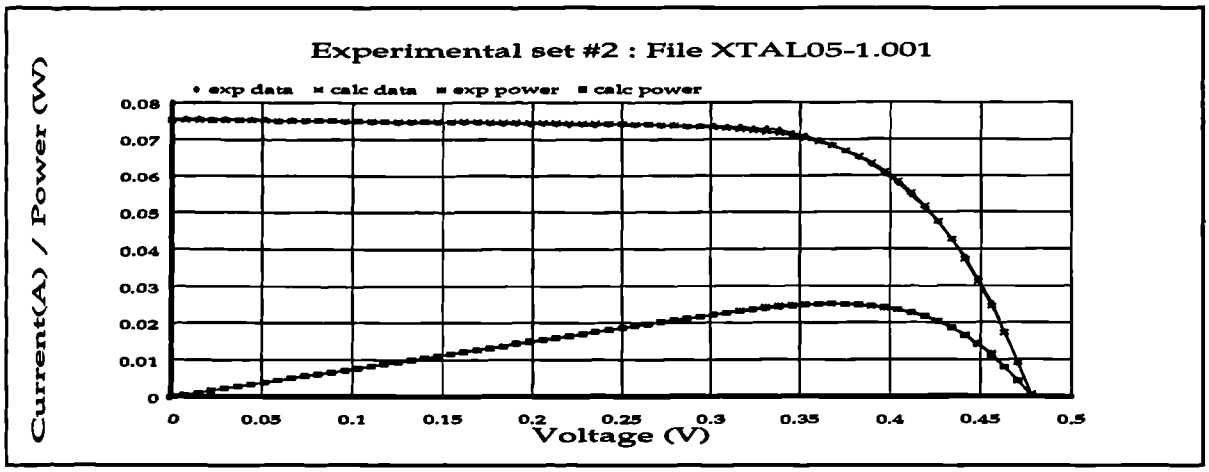


Figure 250 I/V plot: irradiance 4014.6 temperature: 305.1

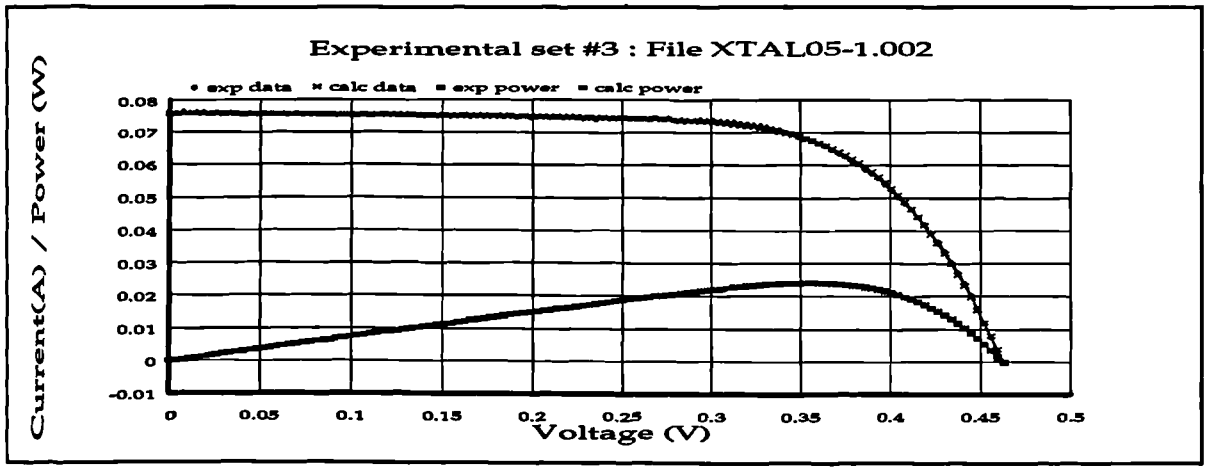


Figure 251 I/V plot: irradiance 3979 temperature: 310.1

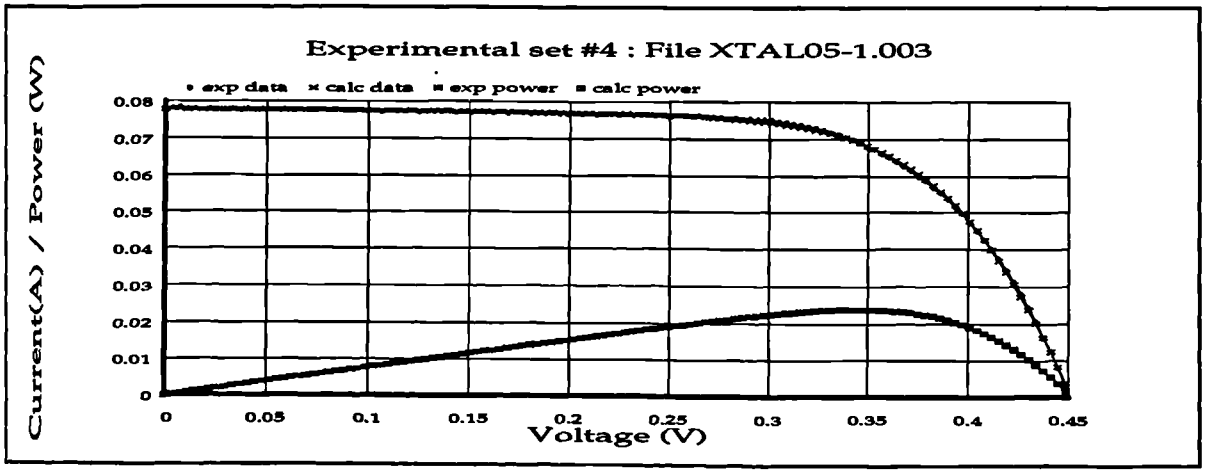


Figure 252 I/V plot: irradiance: 4039.3 temperature: 314.1

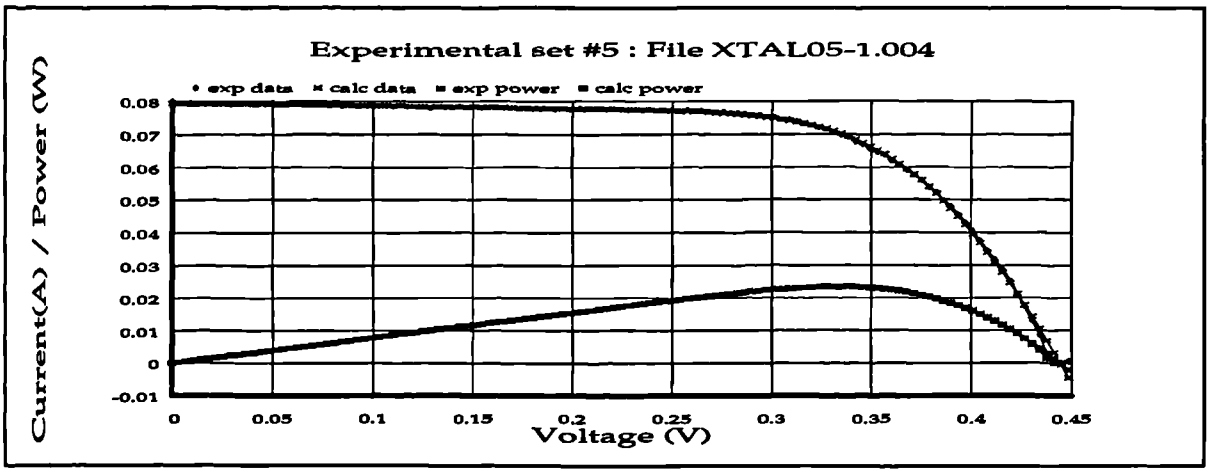


Figure 253 I/V plot: irradiance: 4035 temperature 317.9

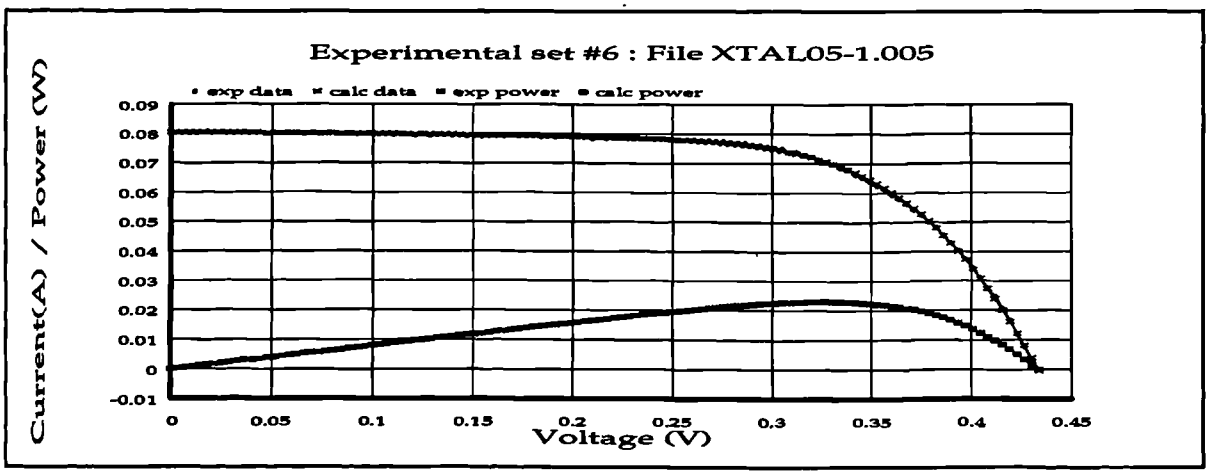


Figure 254 I/V plot: irradiance: 4046.3 temperature 323.7

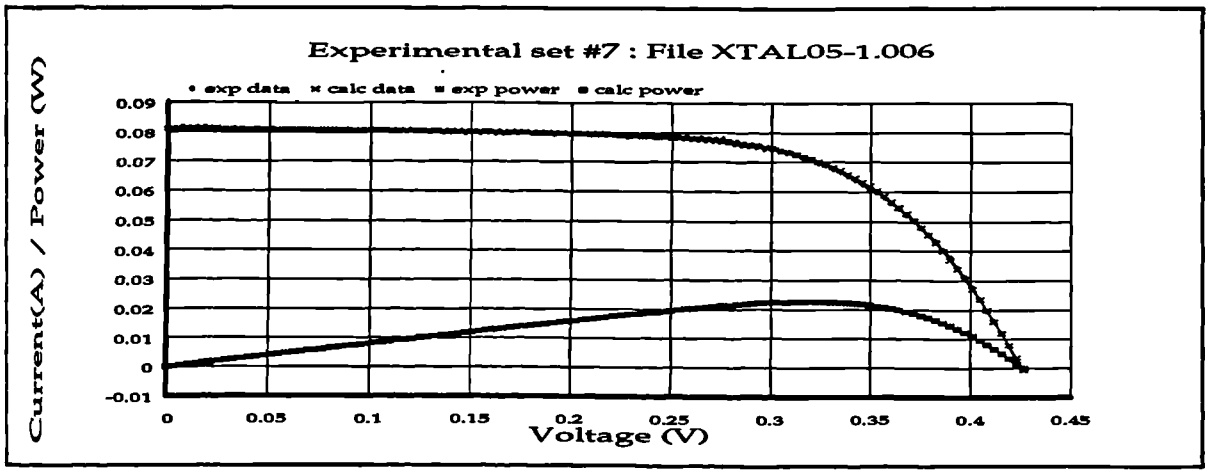


Figure 255 I/V plot: irradiance 4055.3 temperature 323.7

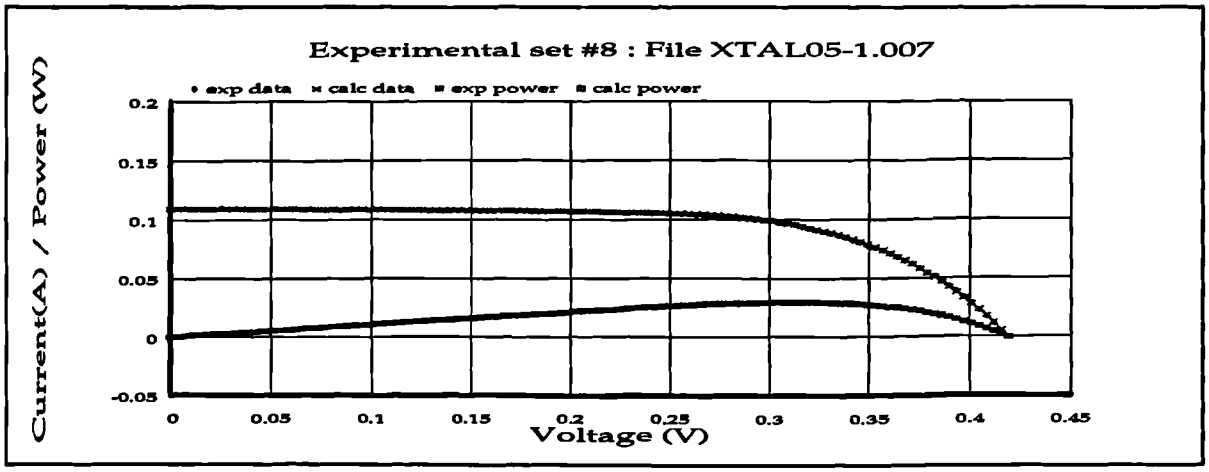


Figure 256 I/V plot: irradiance: 4051.6 temperature 326.1

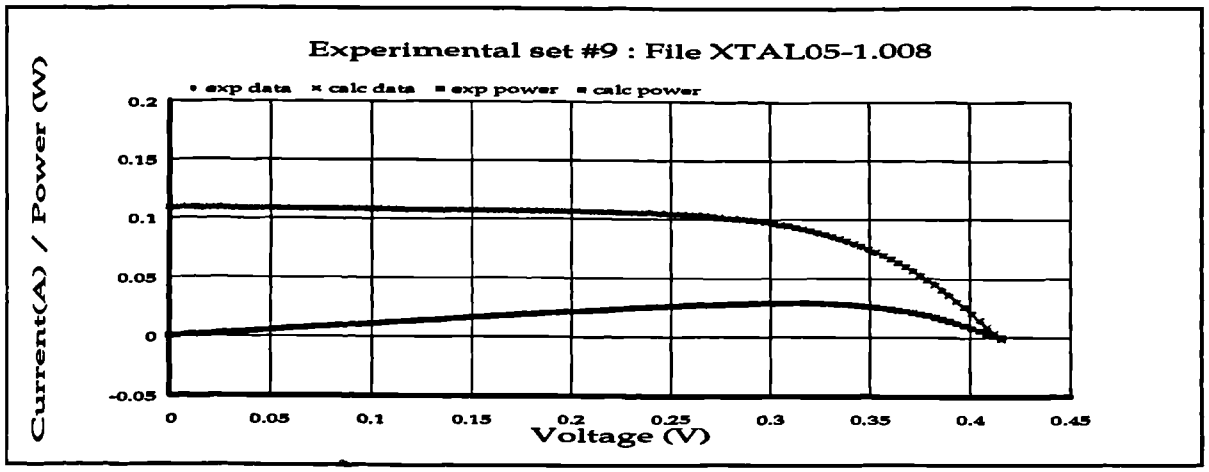


Figure 257 I/V plot: irradiance: 4034 temperature 328

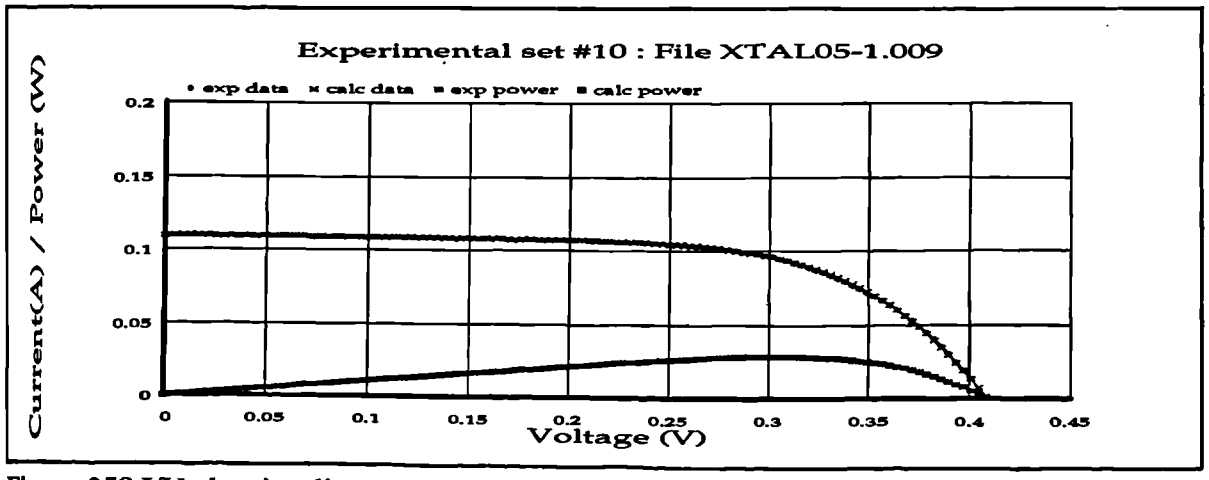


Figure 258 I/V plot: irradiance: 4036.3 temperature 329.9

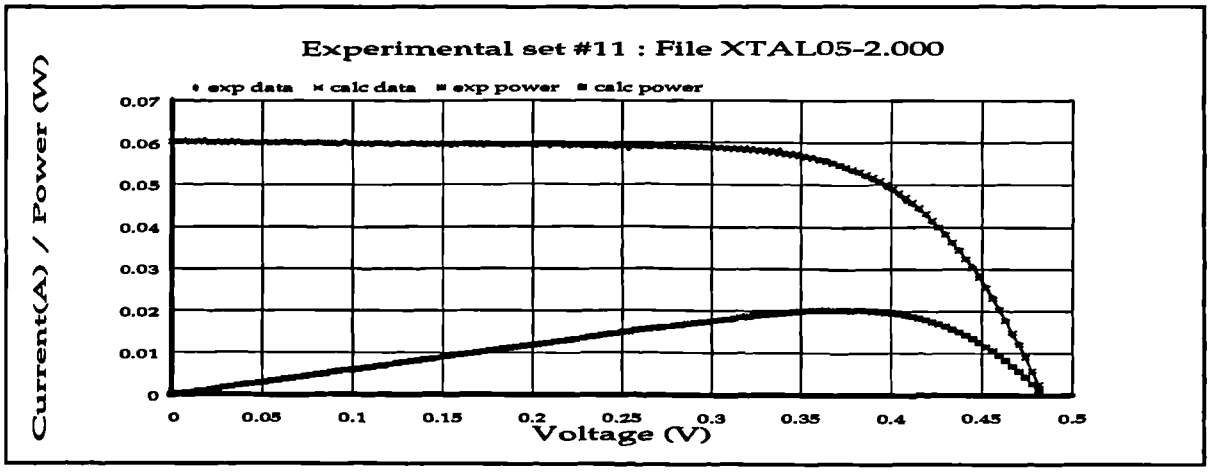


Figure 259 I/V plot: irradiance:3271.6 temperature 302.4

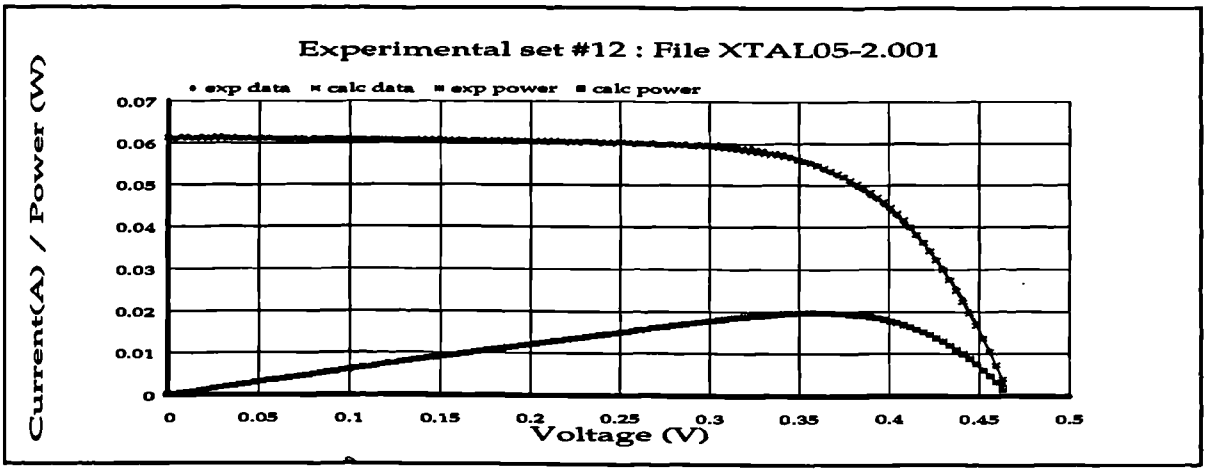


Figure 260 I/V plot: irradiance 3294.6 temperature 306.2

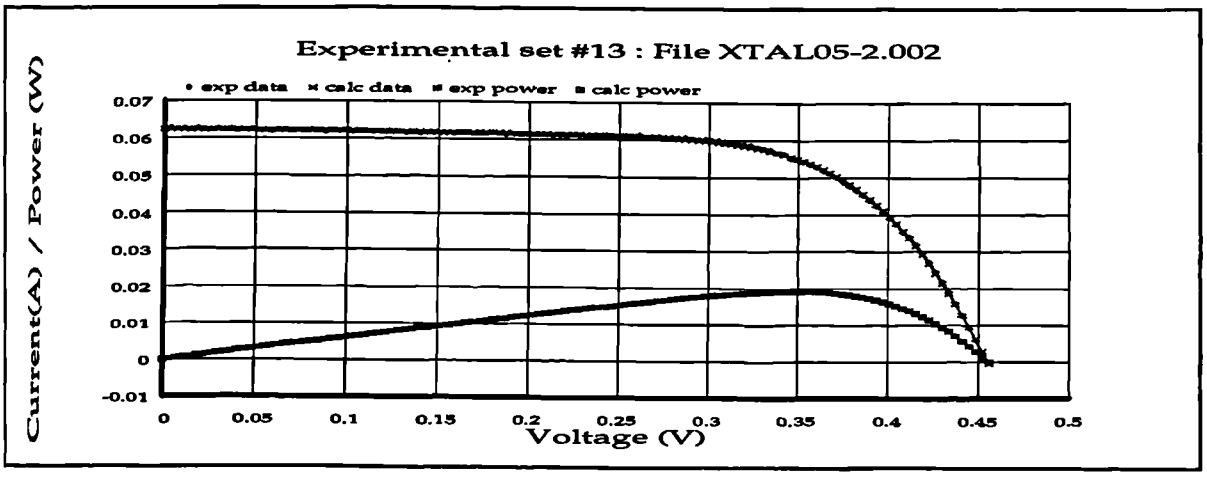


Figure 261 I/V plot: irradiance: 3304 temperature 310.4

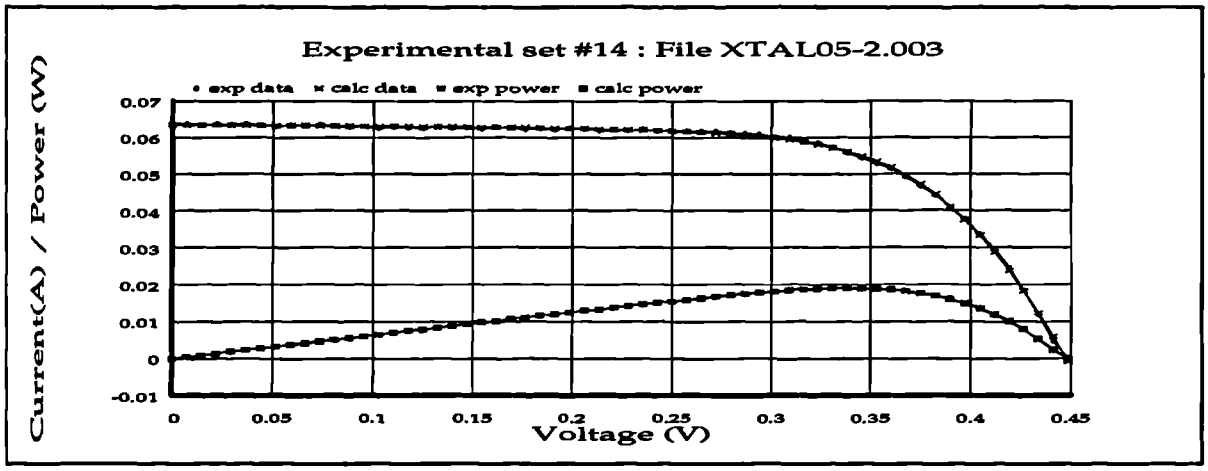


Figure 262 I/V data: irradiance: 3317.6 temperature: 313.8

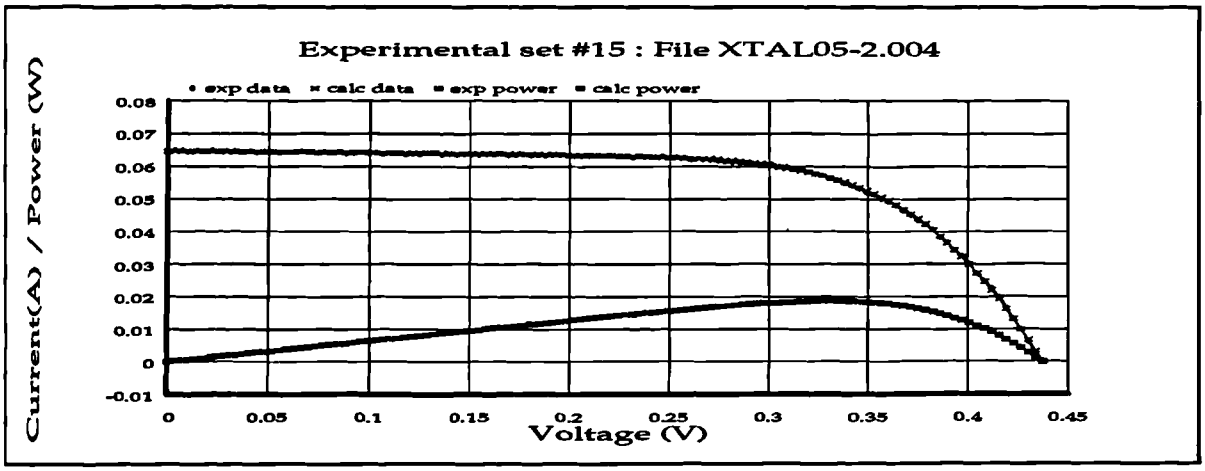


Figure 263 I/V plot: irradiance: 3358.6 temperature: 316.92

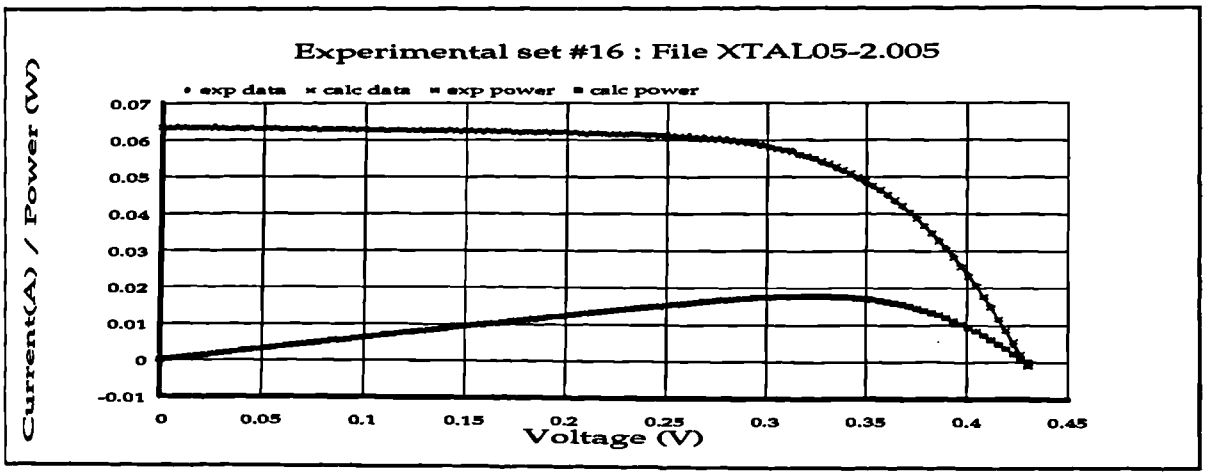


Figure 264 I/V plot: irradiance: 3262.6 temperature 319.5

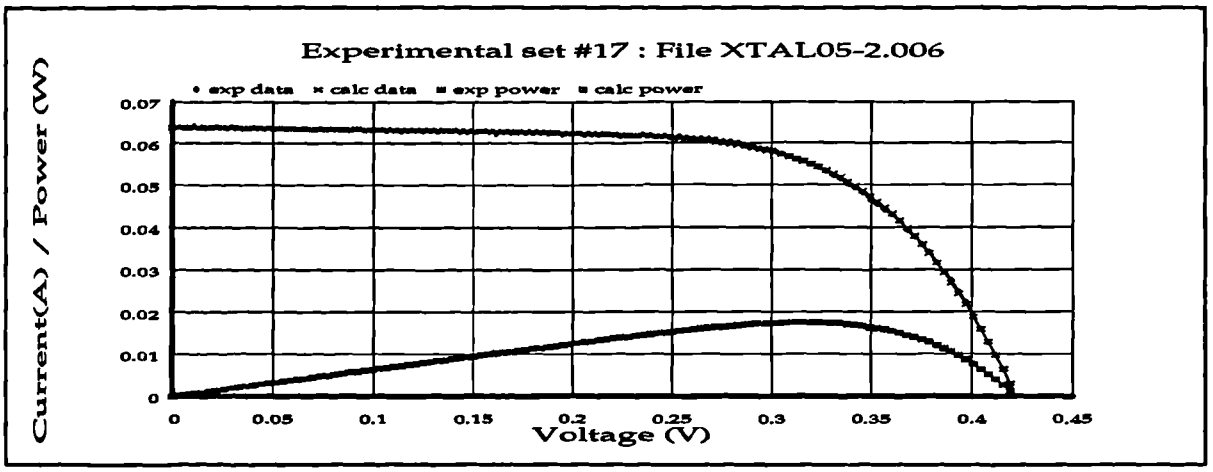


Figure 265 I/V plot: irradiance 3270.6 temperature 321.6

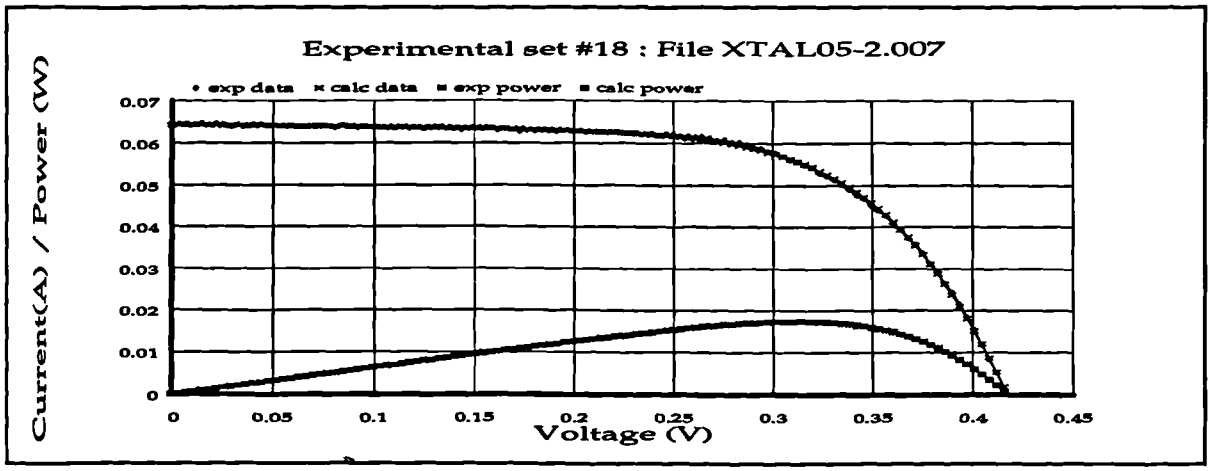


Figure 266 I/V plot: irradiance: 3280 temperature: 323.5

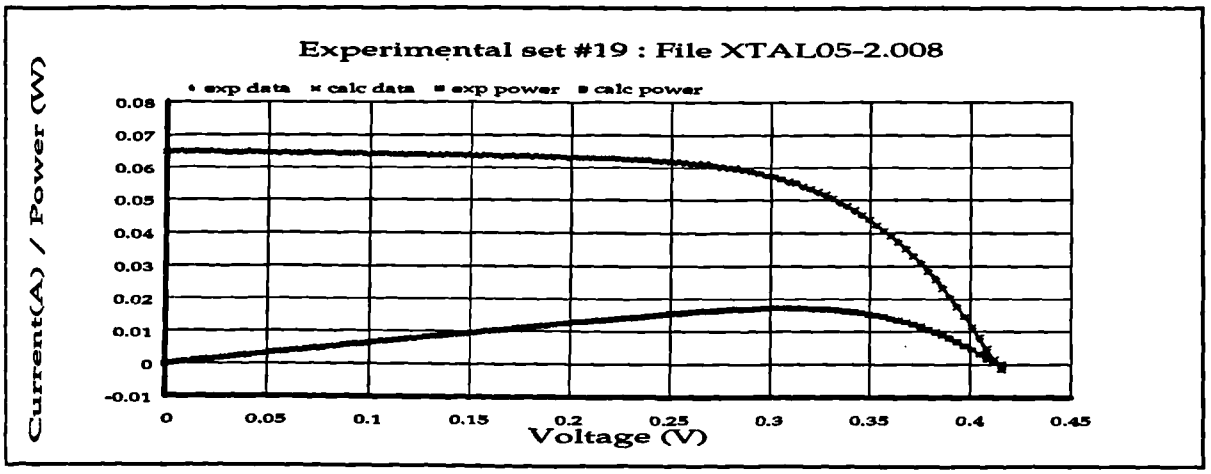


Figure 267 I/V plot: irradiance: 3284 temperature: 325.1

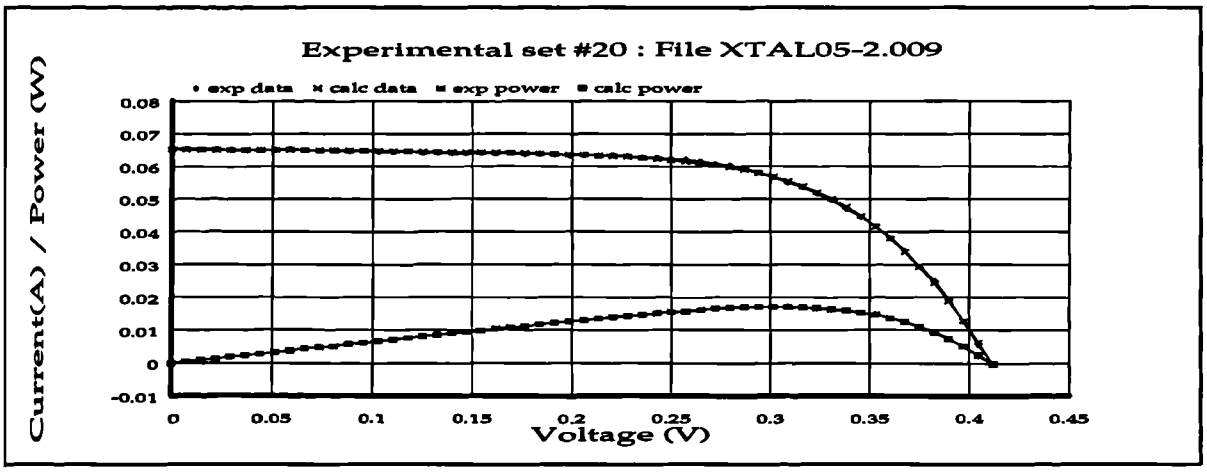


Figure 268 I/V plot: irradiance: 3291.3 temperature: 326.8

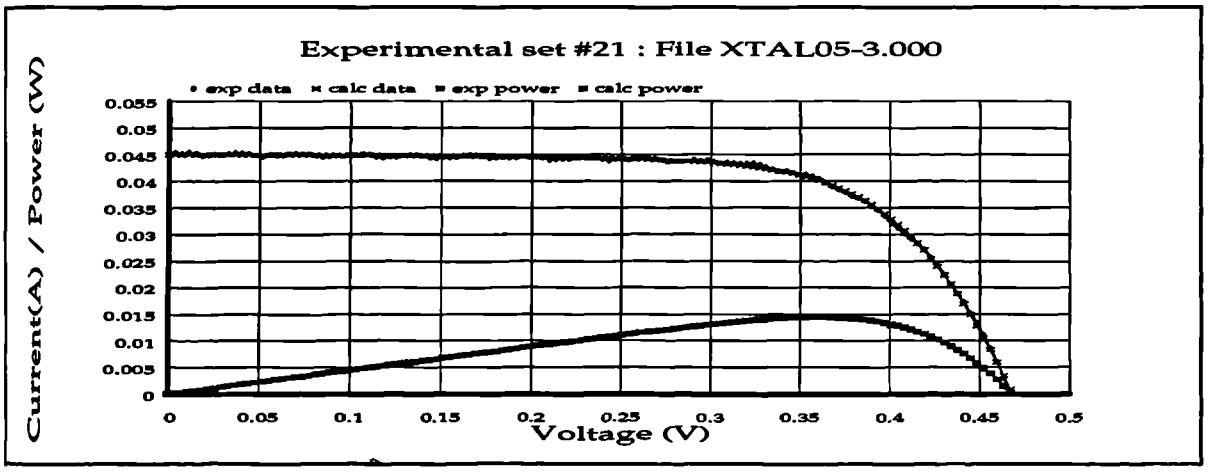


Figure 269 I/V plot: irradiance: 2480.4 temperature: 300.5

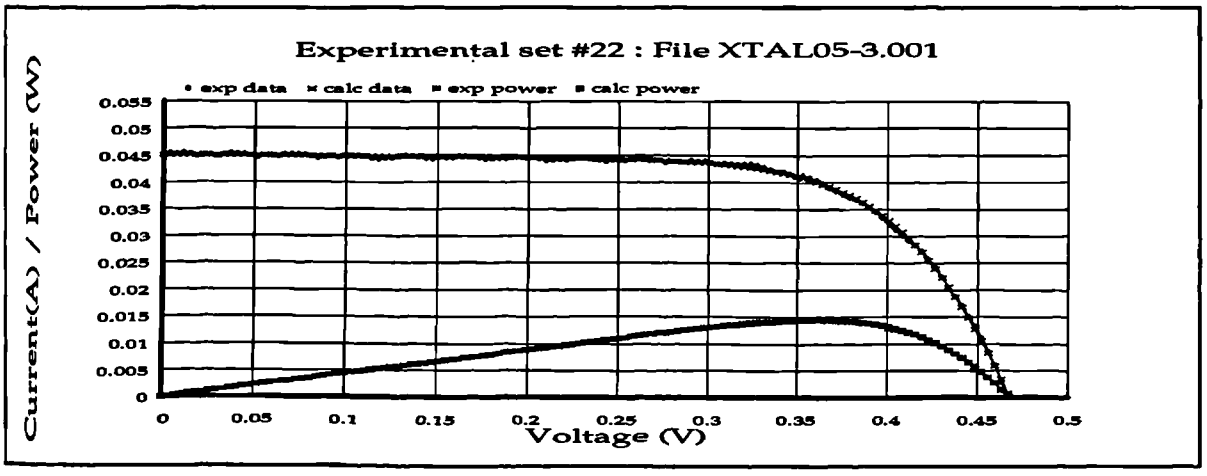


Figure 270 I/V plot: irradiance: 2480.4 temperature: 300.5

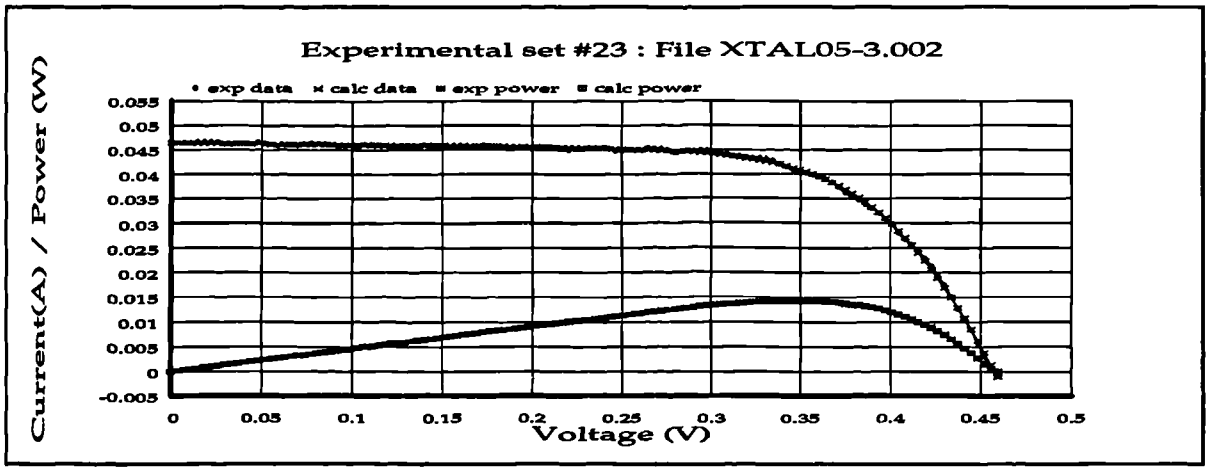


Figure 271 I/V plot: irradiance: 2495.2 temperature 304.5

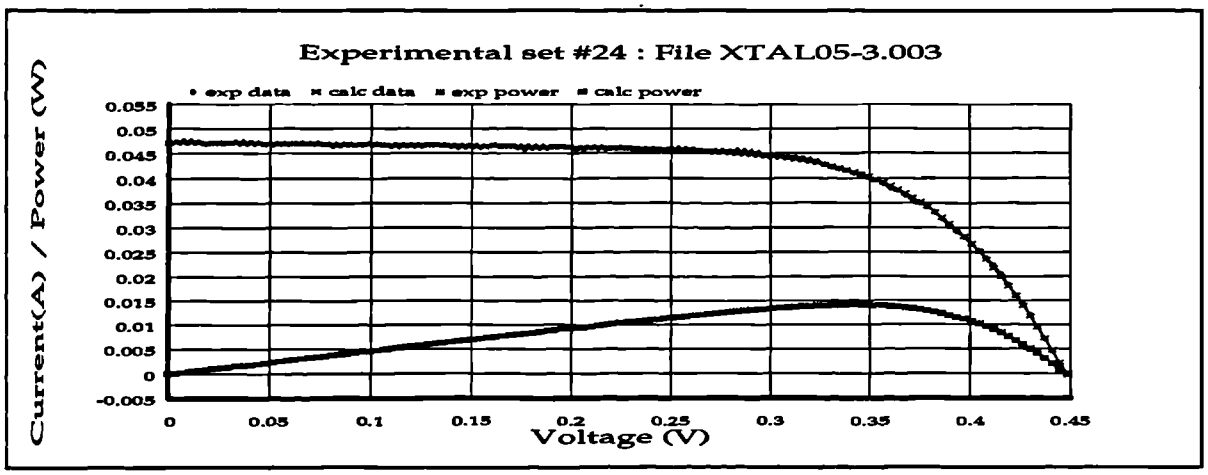


Figure 272 I/V plot: irradiance 2534.6 temperature 307.7

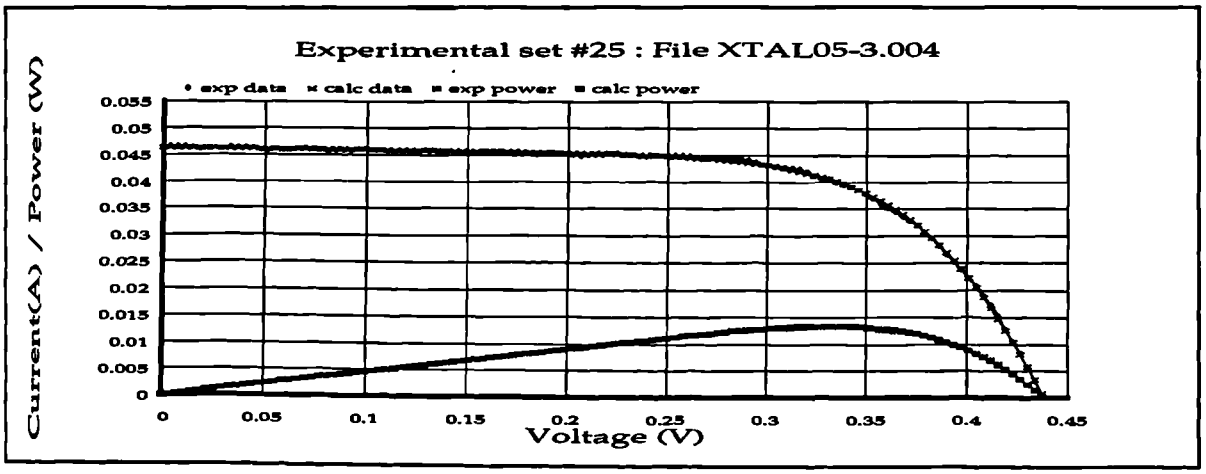


Figure 273 I/V plot: irradiance: 2474 temperature: 310.2

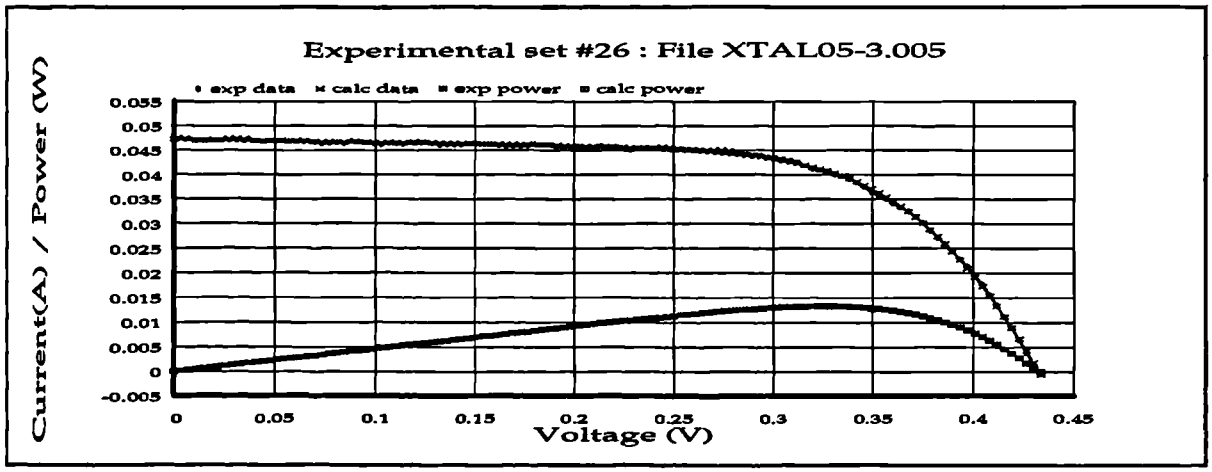


Figure 274 I/V plot: irradiance: 2499.2 temperature: 312.9

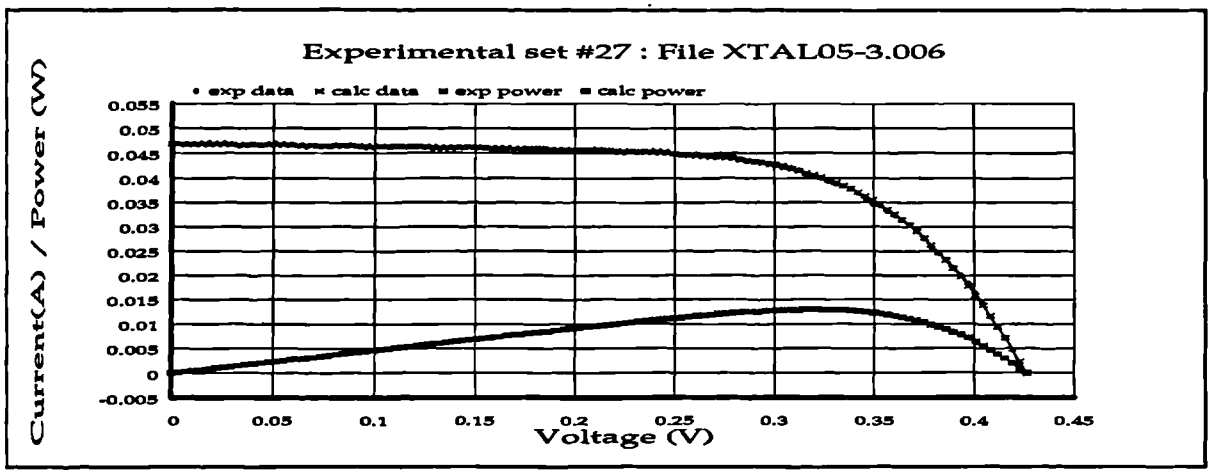


Figure 275 I/V plot: irradiance: 2450.6 temperature 314.8

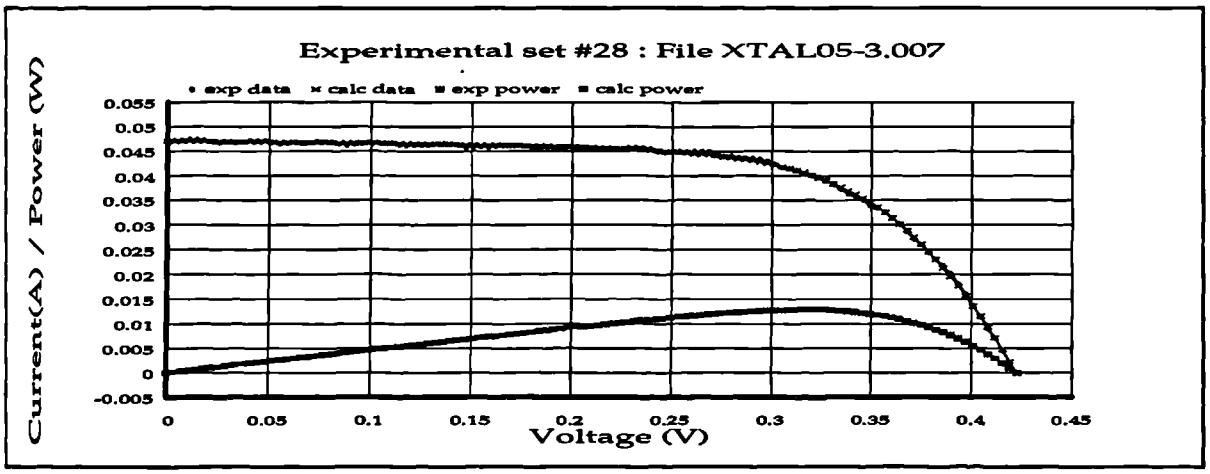


Figure 276 I/V plot: irradiance: 2447.6 temperature: 316.3

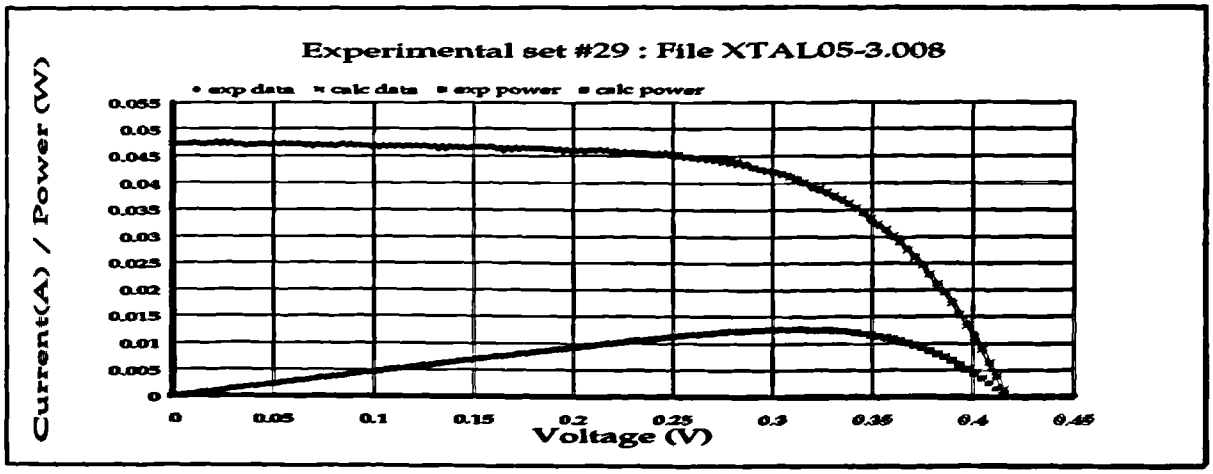


Figure 277 I/V plot: irradiance 2466 temperature: 318

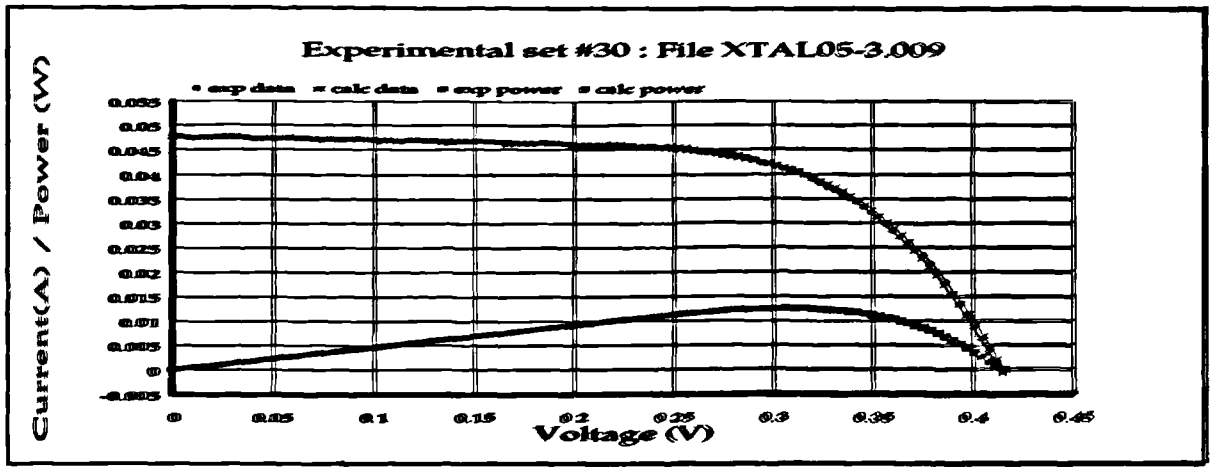


Figure 278 I/V plot: irradiance 2470 temperature 319.2

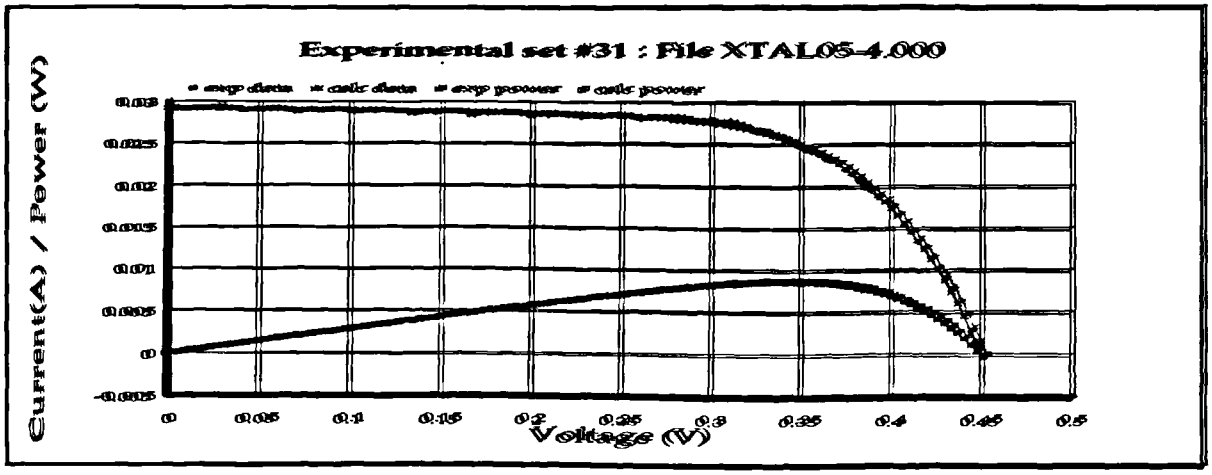


Figure 279 I/V data: irradiance: 1610.2 temperature: 299.0

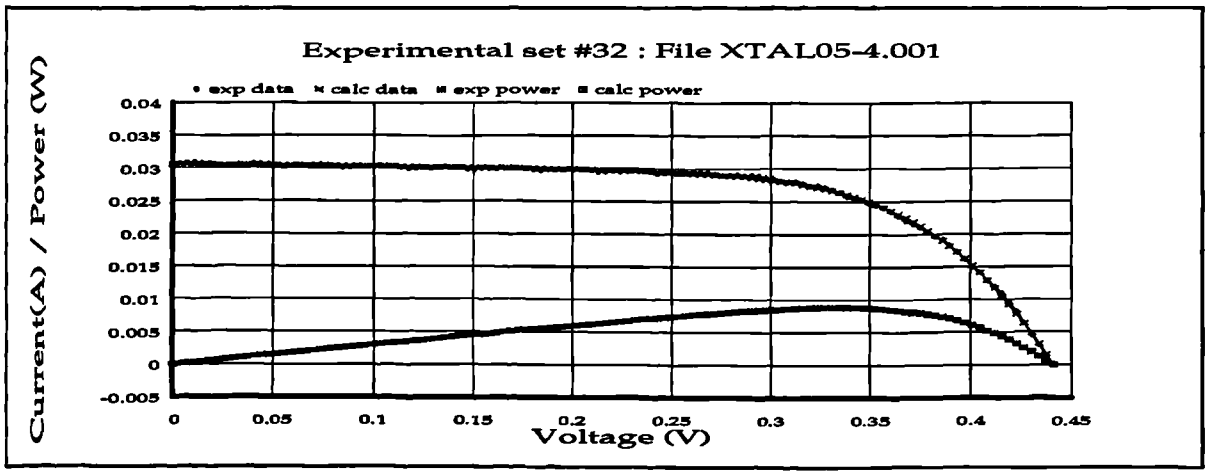


Figure 280 I/V plot: irradiance 1653.8 temperature 302.91

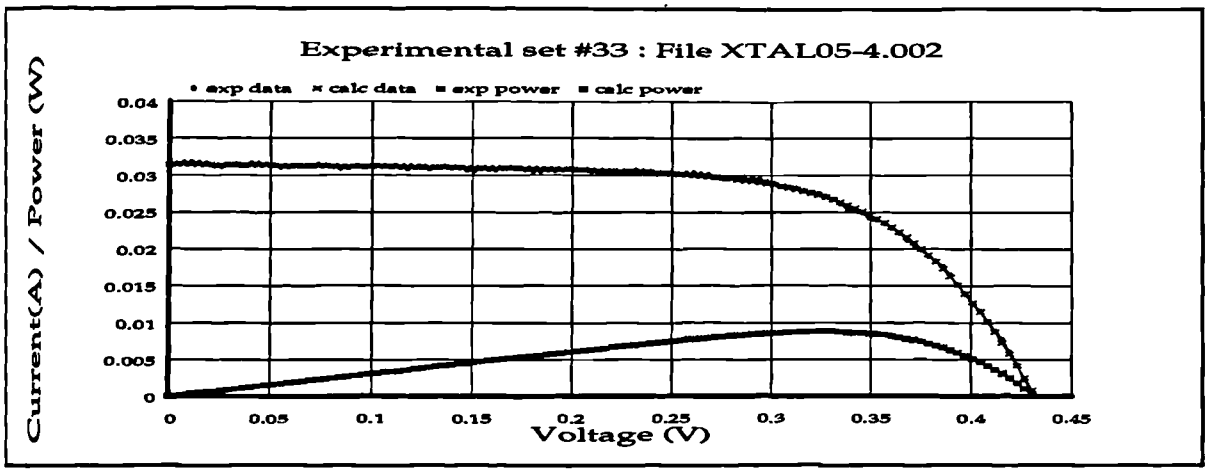


Figure 281 I/V plot: irradiance: 1688.8 temperature 306.0

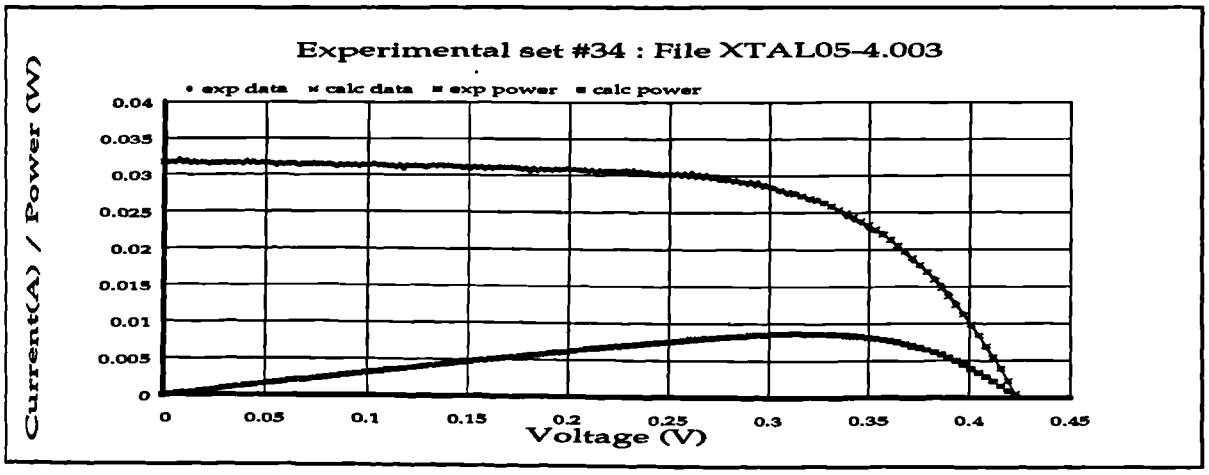


Figure 282 I/V plot: irradiance: 1685.8 temperature: 308.7

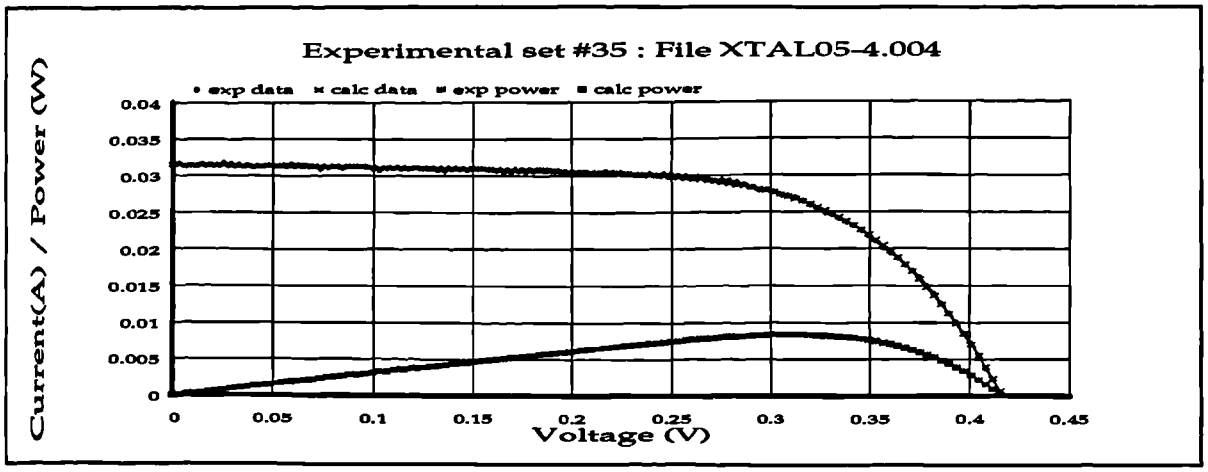


Figure 283 I/V plot: irradiance: 1672 temperature: 311.2

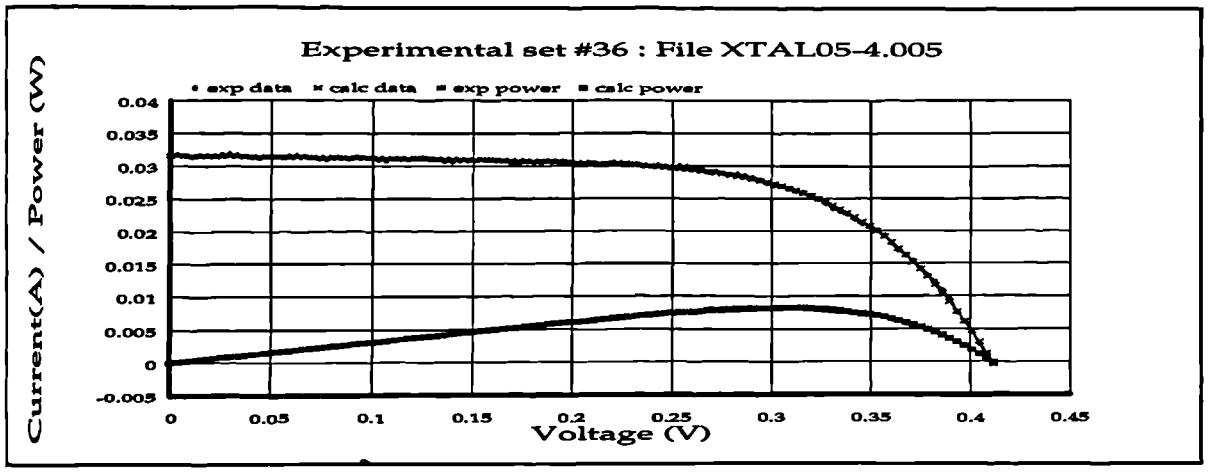


Figure 284 I/V plot: irradiance: 1664.8 temperature: 312.9

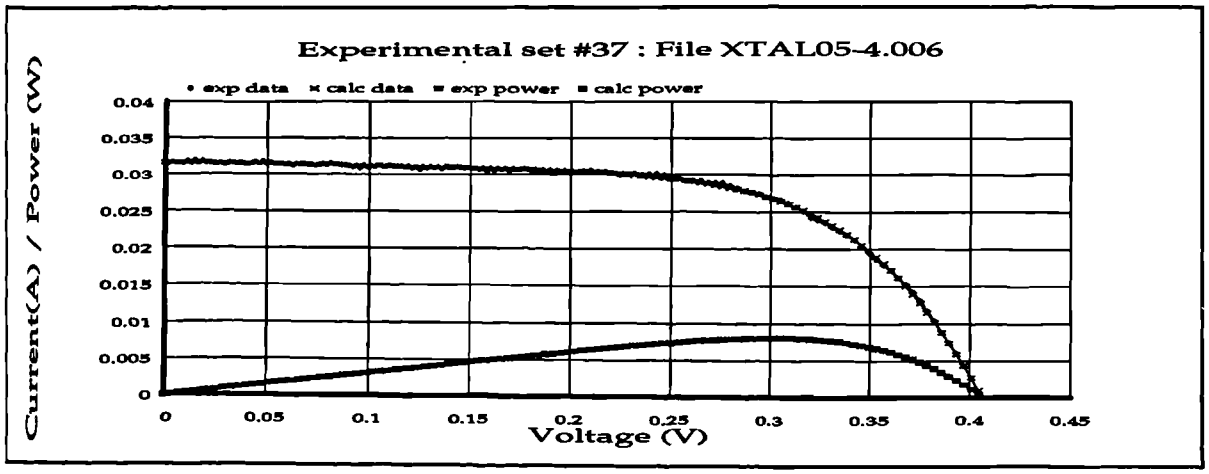


Figure 285 I/V plot: irradiance: 1658.8 temperature 314.4

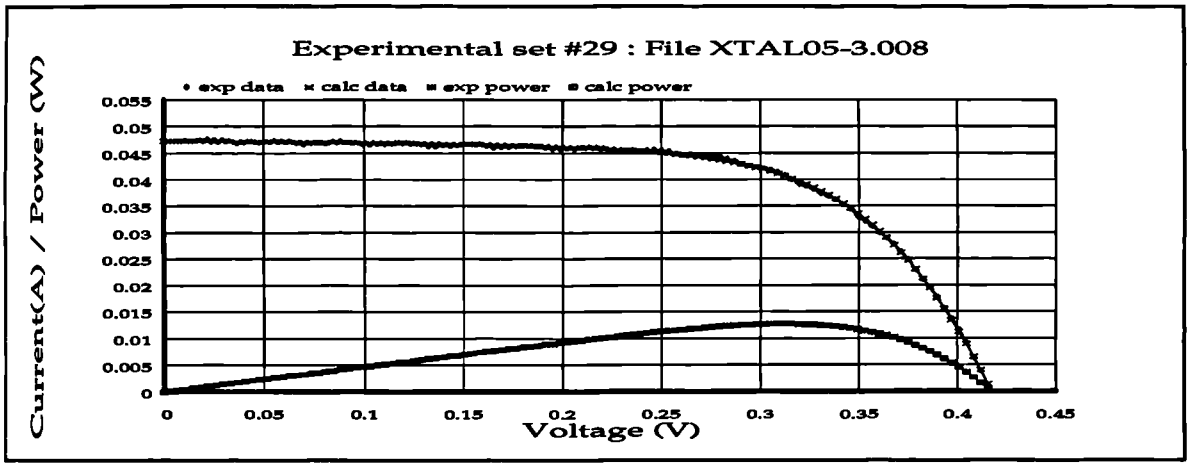


Figure 277 I/V plot: irradiance 2466 temperature: 318

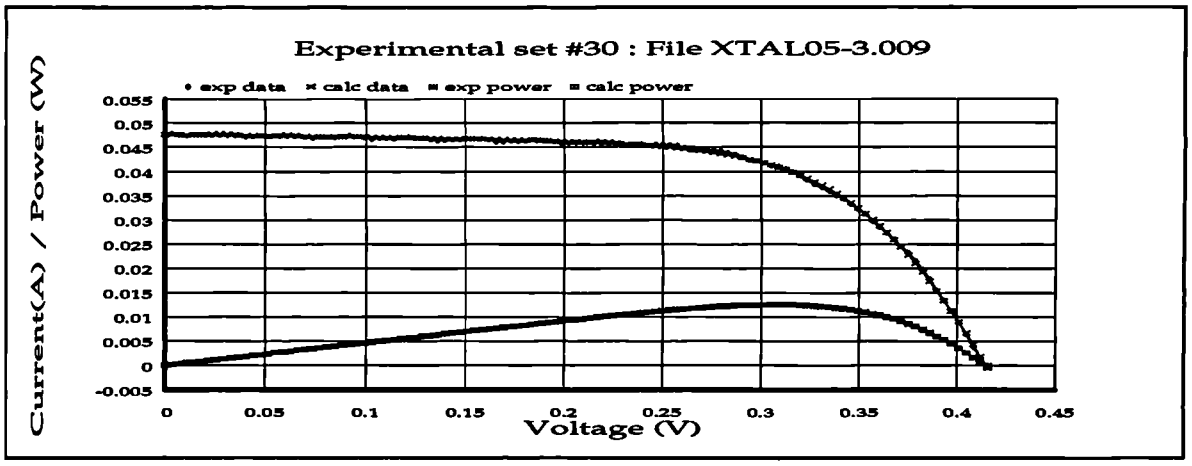


Figure 278 I/V plot: irradiance 2470 temperature 319.2

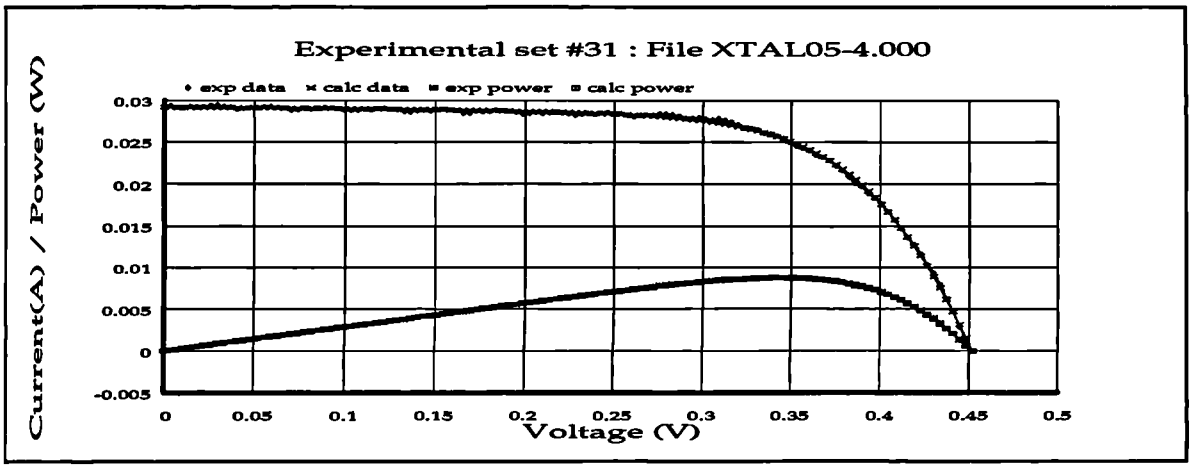


Figure 279 I/V data: irradiance: 1610.2 temperature: 299.0

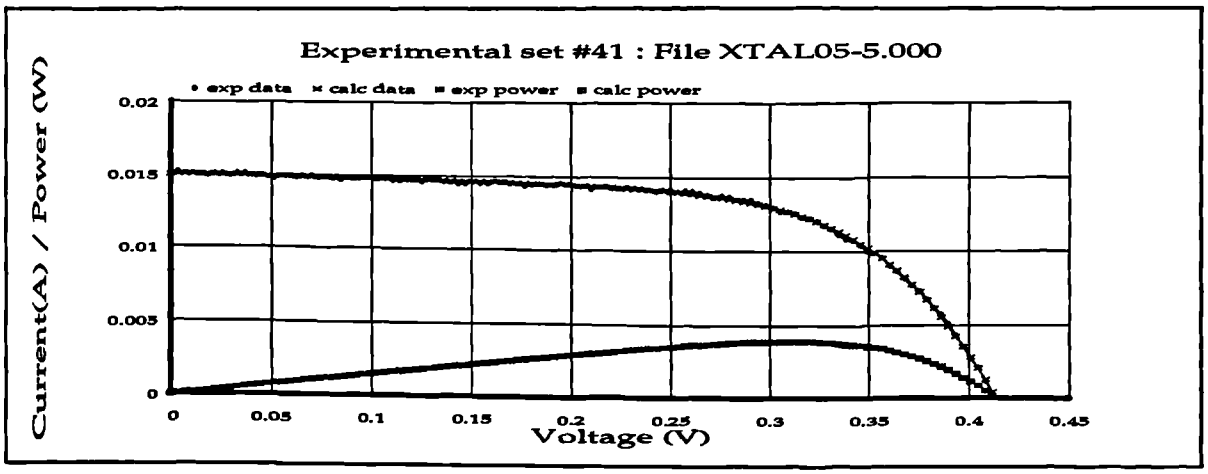


Figure 289 I/V plot: irradiance: 827.0 temperature: 298.6

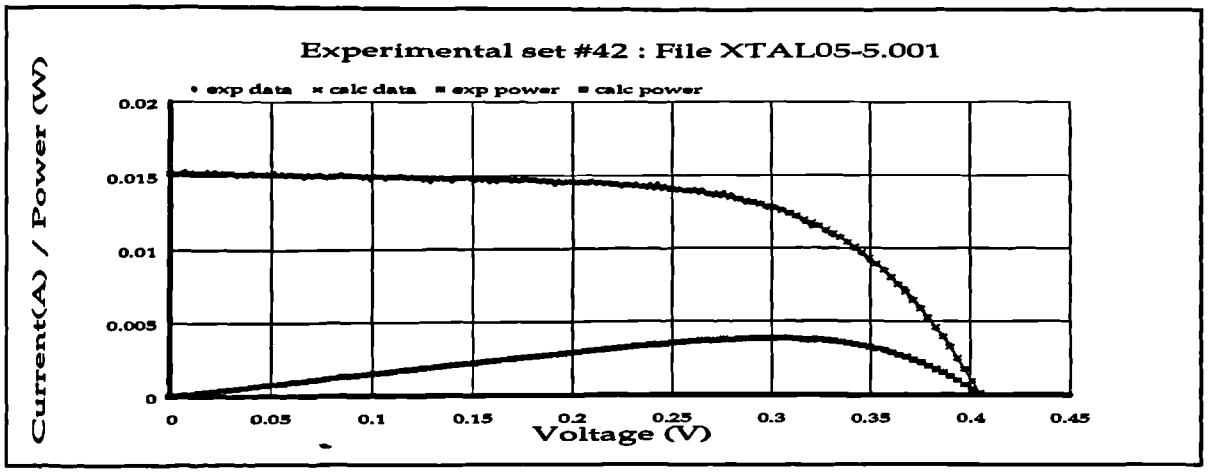


Figure 290 I/V plot: irradiance: 814.2 temperature: 301.12

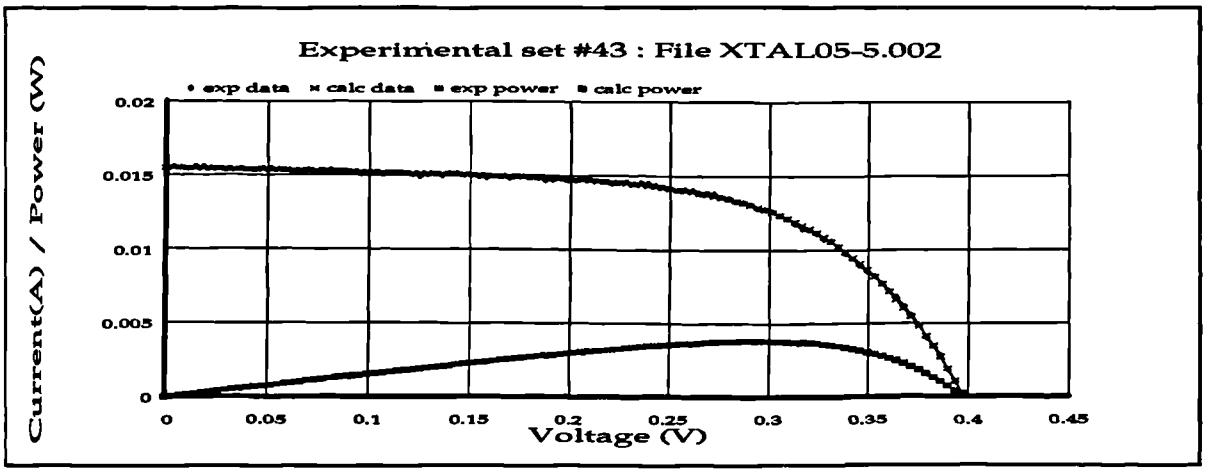


Figure 291 I/V plot: irradiance 827.2 temperature 303.54

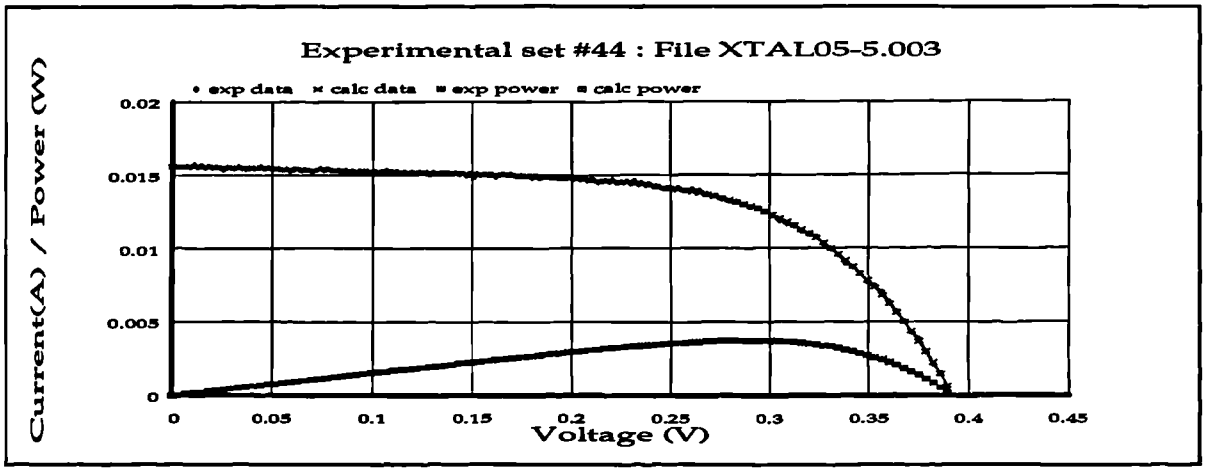


Figure 292 I/V plot: irradiance: 826.0 temperature 305.4

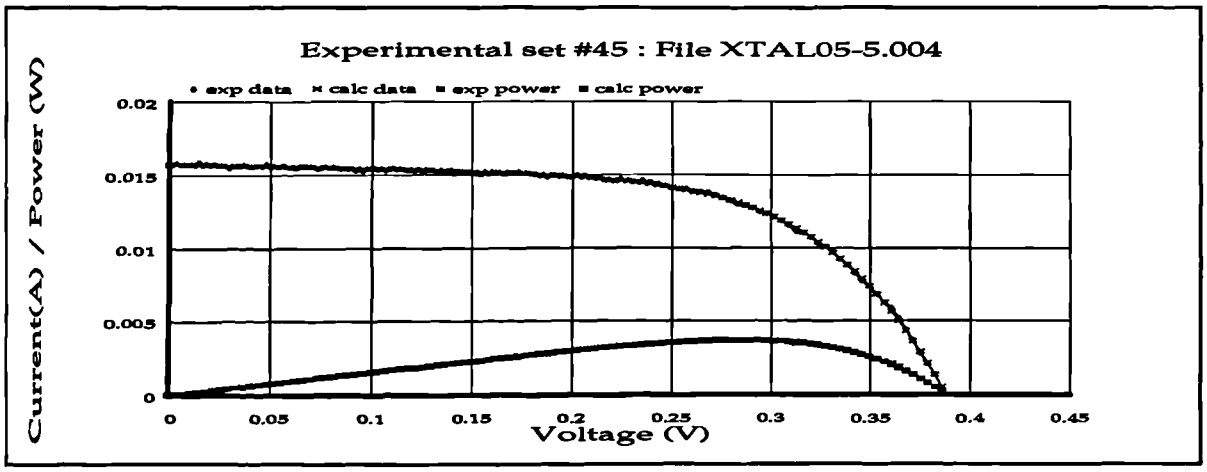


Figure 293 I/V plot: irradiance: 833.6 temperature: 307.0

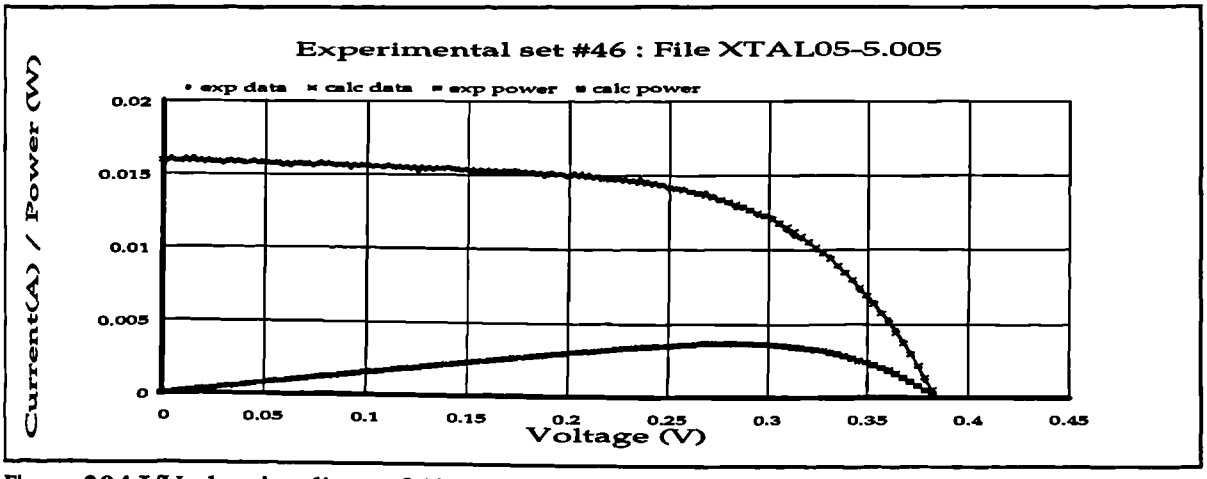


Figure 294 I/V plot: irradiance 842.6 temperature 308.3

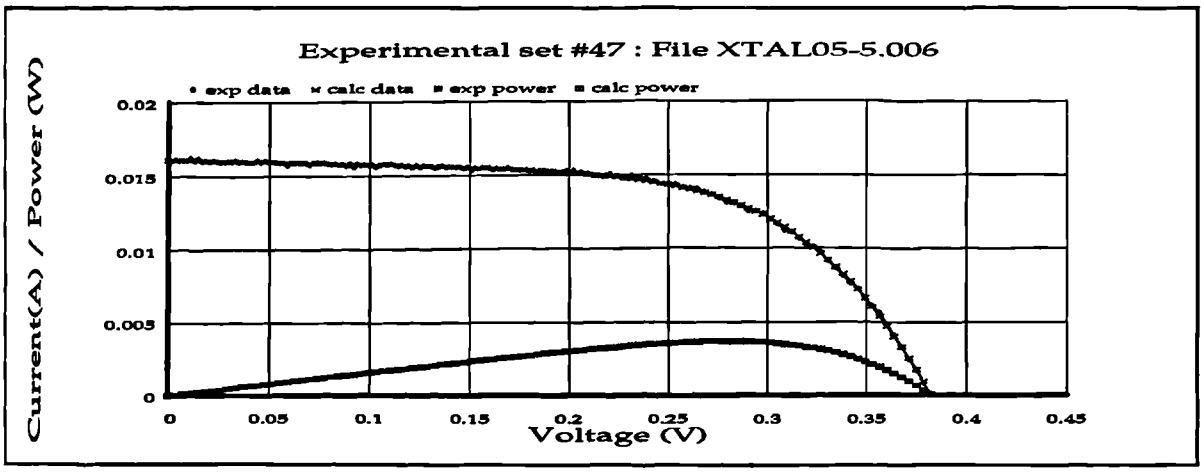


Figure 295 I/V plot: irradiance: 847.2 temperature 309.1

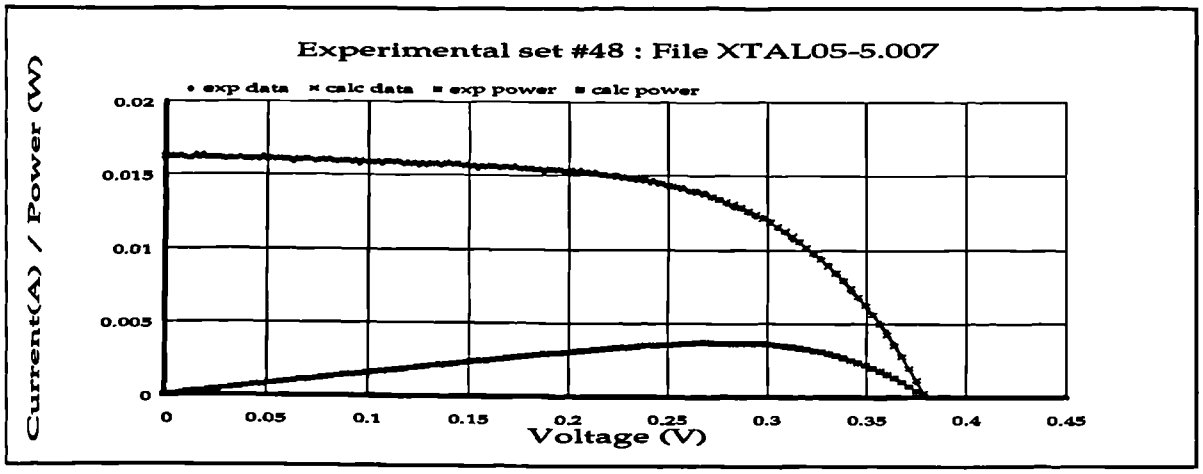


Figure 296 I/V plot: irradiance: 848.2 temperature: 310.0

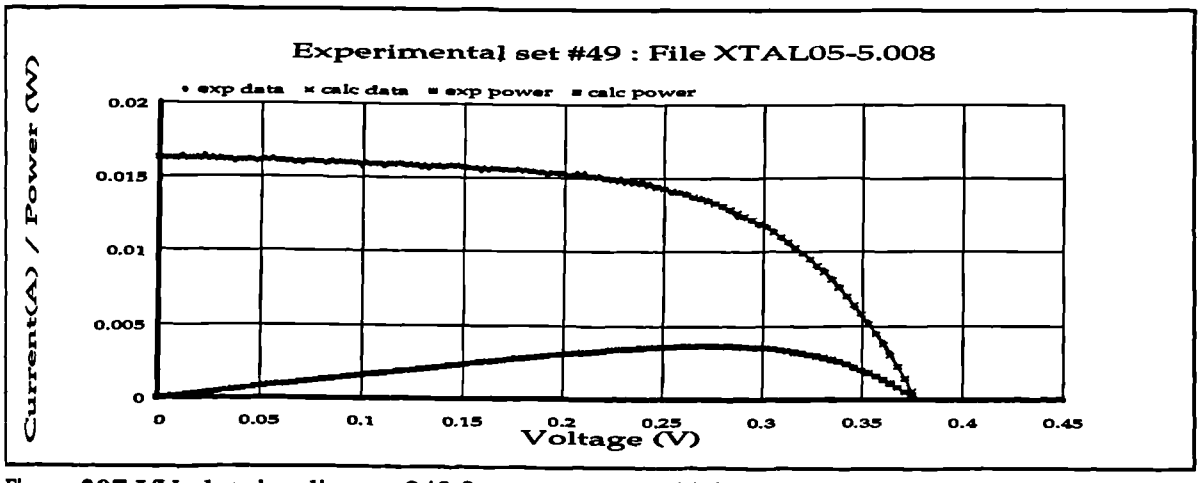
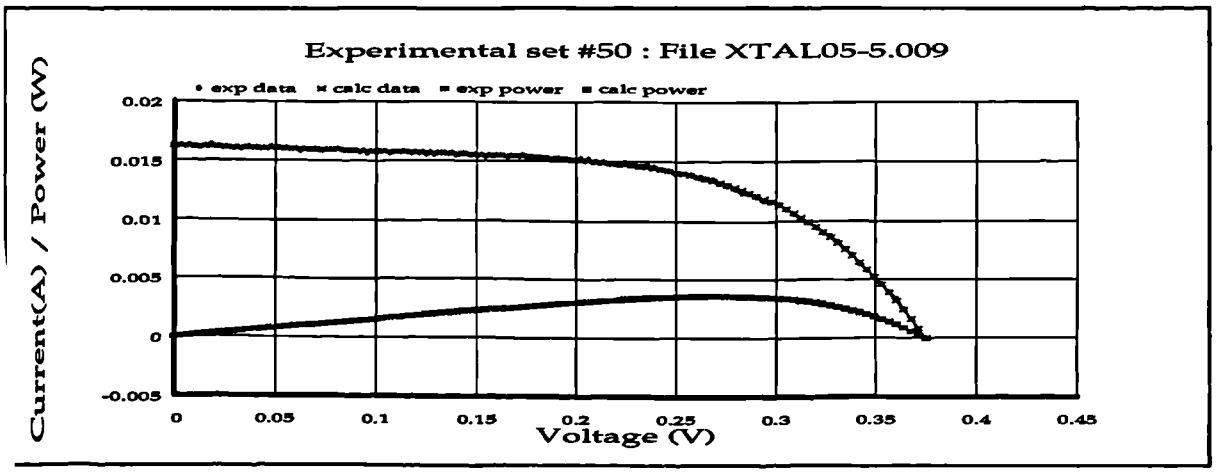


Figure 297 I/V plot: irradiance: 843.0 temperature: 311.2



'igure 298 I/V plot: irradiance: 839.8 temperature: 312.13

APPENDIX B MAST Scripts used during development

The MAST scripts are the template files used by the SABER simulation environment. This appendix gives listings of the main templates used that were written by hand (not generated from the schematic capture utility) The scripts shown are detailed below, and are followed by a list detailing page numbers for ease of location.

1. Array template:

   A1: MAST script for PV array template, version 3.0

2. Maximum power tracking controllers:

   Dither methods:

   A2: Maximum power tracker using fixed integration
   A3: Maximum power tracker using proportional integration

   Running-sample methods:

   A4: Maximum power tracker using fixed integration steps
   A5 Maximum power tracker using proportional integration

   Maximum power tracking using boost converter characteristic

   A6: Maximum power tracker using boost converter characteristic

3. Embedded MPP/PI controllers:

A7: Standard PI-only current mode controller

A8: Embedded MPP/PI controller

4. Inverter templates:

A9: Inverter main control script

A10: AC section reference clock generator

A11: Inverter protection logic

The following list cross-references scripts with page numbers for ease of location::

A1: MAST script for PV array template, version 3.0

```
##########################################################################
#
# Template for basic solar cell implementing the double-exponential model
# with single exponential model as subset.
# Insolation may be varied by varying voltage across irr1/irr2 pins.
#
# J.A. Gow 6/1/1994
# including temperature dependencies added 20/1/94
# revised temperature and irradiance dependencies added 1/9/94
# variable insolation added 15/11/94
# Version 3 with parametrized temperature added 5/4/95
#
##########################################################################

element template solar_cell_v p m irr1 irr2 = K0,K1,K2,K3,K4,K5,K6,K7,K8,K9,
                                              K10,K11,K12,nseries,nparallel,
                                              ei_const,T

################
# three terminals
################

electrical p,m,irr1,irr2

number        K0=undef,
              K1=undef,
              K2=undef,
              K3=undef,
              K4=undef,
              K5=undef,
              K6=undef,
              K7=undef,
              K8=undef,
              K9=undef,
              K10=undef,
              K11=undef,
              K12=undef,
              nseries=undef,            # no. of series cells
              nparallel=undef,          # no of parallel cells
              ei_const=undef,           # insolation muliplier for control voltage
              T=undef                   # temperature
{

      number  k=1.38e-23,                           # Boltzmann
              e=1.602e-19,                          # electronic charge
              vt,il,io1,io2,a2,rparallel,
              kelvin,                               # Kelvin temperature
              ns,np                                 # array dimensions

      val v vdiodes,ei
      val i idiodes
      val r rs
      val i photo_i

#     ### pull in the temperature from the system

      external number temp

#     ### one internal node

      electrical x


      struc {number bp,inc;} \
              svd[*] = [(-400,0.1),(0,0.0001),(0.3,0.00001),(400.0,0)],
              nvd[*] = [(-400,0.2),(400,0)]

 parameters {
              kelvin=T+273.15           # calculate temperature in kelvin
```

```
            vt=(k*kelvin)/e            # calculate thermal voltage

##########################################################################
# now calculate the changes in the ambient parameters due to temperature.
# and irradiance
##########################################################################

#      ### changes in il, the photocurrent


#      ### changes in the first saturation current

            io1=K2*(kelvin**3)*limexp(K3/kelvin)

#       ### changes in second (recombination) saturation current
#       ### allowing for SE model approach

            if (((K2==0)&(K3==1))|(K2==undef)|(K3==undef)) {

                  io2=K4*(kelvin**3)*limexp(K5/kelvin)

            }
            else {

                  io2=K4*(kelvin**(3/2))*limexp(K5/kelvin)

            }

#        ### changes in diode quality factor A

            a2=K6+K7*kelvin

#        ### changes in series resistance


#       ### changes in shunt resistance

            rparallel=K11*limexp(K12*kelvin)

##########################################################################
# now all parameters have their temperature and irradiance terms built
# in, as per J.A. Gow September 1994
##########################################################################

      if (nseries==undef){

            ns=1
      }
      else {
            ns=nseries
      }

      if (nparallel==undef){

            np=1
      }
      else {
            np=nparallel
      }
}

values {

      ei=(v(irr1)-v(irr2))*ei_const

      photo_i=K0*ei*(1+K1*kelvin)

      if(ei <= 0) {
            rs=K8+K9+K10*kelvin
      }
      else {
```

```
            rs=K8+(K9/ei) +K10*kelvin
        }

        vdiodes=v(x)-v(m)
        idiodes=io1*(limexp(vdiodes/(vt*ns))-1)+          \
                 io2*(limexp(vdiodes/(a2*vt*ns))-1)+      \
                     (vdiodes/(rparallel*ns))

}

control_section {

        sample_points(vdiodes,svd)  # set up the sampling
        newton_step(vdiodes,nvd)    # and the Newton-Raphson steps
}

equations {
            i(p->x) -= ((v(x)-v(p))/(rs*ns))*np
            i(x->m) += (idiodes-photo_i)*np
        }

}
```

A2: MAST script for maximum power tracker using fixed integration steps

```
##########################################################################
# Maximum power point tracking system for PV inverter
#
# Sample_point algorithm with external perturbation implementation v1.2 #
# FIXED integration steps
#
# J.A. Gow 1994
##########################################################################
template mppt_sample_2 vcell icell gnd drive fsout = t,ke,dl,ptb_width,
                                        ptb_ampl
electrical vcell,icell,gnd,drive
state logic_4 fsout
number t=40u
number ke=1
number dl=15
number ptb_width,ptb_ampl

{

        var i idrive
        state nu ft,sgn
        state nu drivestate
        state nu delta,p1,p2,ptb,e
        val v vdrive

        when(time_init) {

                schedule_event(time,ft,0)
                schedule_event(time,ptb,5)
                message("mppt_sample_2 v1.2: using FIXED integration steps")
        }

        when(dc_init) {
                delta=0.1
                p1=0
                p2=0
                drivestate=0
        }

        when(event_on(ptb)) {

                if(ptb==5) {
                        schedule_event(time+(ptb_width*t)/2,ptb,0)
                        schedule_next_time(time)
                        p1=v(vcell)*v(icell)
                        delta=delta+ptb_ampl
                        message("PTB +:%\n",ptb)
                }
                else {
                        schedule_event(time+(ptb_width*t)/2,ptb,5)
                        schedule_next_time(time)
                        p2=v(vcell)*v(icell)
                        e=p2-p1
                        message("PTB +:%\n",ptb)
                        message("----------------- e: %",e)
                        delta=delta-ptb_ampl

                        if(e>0) e=1
                        if(e<0) e=-1

                        delta=delta+ke*e
                        message("delta: %\n",delta)

                        if(delta>0.9) delta=0.9
                        if(delta<0.1) delta=0.1

                }
```

```
}

when(event_on(ft)) {

        if(ft==1) {
                schedule_event(time+(t/2),ft,0)
                schedule_event(time+(t/2),fsout,14_0)
                schedule_event(time+delta*t,drivestate,0)
        }
        else {
                schedule_event(time+(t/2),ft,1)
                schedule_event(time+(t/2),fsout,14_1)
                schedule_event(time+(t/2),drivestate,1)
        }
}


values {
        if(drivestate==0) vdrive=0
        if(drivestate==1) vdrive=dl
}

equations {

        i(drive->gnd) +=idrive
        idrive: v(drive)-v(gnd)=vdrive
}
```

A3: Maximum power tracker using proportional integration

```
##########################################################################
# Maximum power point tracking system for PV inverter
#
# Sample_point algorithm with external perturbation implementation v1.2a
#
# PROPORTIONAL integration steps
#
# J.A. Gow 1994
##########################################################################

template mppt_sample_2a vcell icell gnd drive fsout = t,ke,dl,ptb_width,
                                                      ptb_ampl

electrical vcell,icell,gnd,drive
state logic_4 fsout
number t=40u
number ke=1
number dl=15
number ptb_width,ptb_ampl
{

      var i idrive
      state nu ft,sgn
      state nu drivestate
      state nu delta,p1,p2,ptb,e
      val v vdrive

      when(time_init) {

            schedule_event(time,ft,0)
            schedule_event(time,ptb,0)
            message("mppt_sample_2 v1.2a: using PROPORTIONAL integration steps")

      }

      when(dc_init) {
            delta=0.1
            p1=0
            p2=0
            drivestate=0
      }

      when(event_on(ptb)) {

            if(ptb==5) {
                  schedule_event(time+(ptb_width*t)/2,ptb,0)
                  schedule_next_time(time)
                  p1=v(vcell)*v(icell)
                  delta=delta+ptb_ampl
                  message("PTB +:%\n",ptb)
            }
            else {
                  schedule_event(time+(ptb_width*t)/2,ptb,5)
                  schedule_next_time(time)
                  p2=v(vcell)*v(icell)
                  e=(p2-p1)*10
                  message("PTB +:%\n",ptb)
                  delta=delta-ptb_ampl
                  message("------------------ e: %",e)

                  if (e > 20) e=20
                  if ((e < 1)&(e >= 0)) e=1
                  if ((e < 0)&(e > -1)) e=-1
                  if (e < -20) e= -20

                  delta=delta+ke*e
                  message("delta: %\n",delta)

                  if(delta>0.9) delta=0.9
```

```
                if(delta<0.1) delta=0.1

        }
    }

    when(event_on(ft)) {

        if(ft==1) {
                schedule_event(time+(t/2),ft,0)
                schedule_event(time+(t/2),fsout,14_0)
                schedule_event(time+delta*t,drivestate,0)
                schedule_next_time(time+delta*t)
        }
        else {
                schedule_event(time+(t/2),ft,1)
                schedule_event(time+(t/2),fsout,14_1)
                schedule_event(time+(t/2),drivestate,1)
                schedule_next_time(time+(t/2))
        }
    }

    values {
        if(drivestate==0) vdrive=0
        if(drivestate==1) vdrive=dl
    }

    equations {

        i(drive->gnd) +=idrive
        idrive: v(drive)-v(gnd)=vdrive
    }
}
```

A4: Maximum power tracker using fixed integration

```
##########################################################################
# Maximum power point tracking system for PV inverter
#
# Autonomous sample_point algorithm implementation v1.3
#
# FIXED integration steps
#
# J.A. Gow 1994
##########################################################################
template mppt_sample_3 vcell icell gnd drive fsout = t,ke,dl,
                                sw_sample_interval
electrical vcell,icell,gnd,drive
state logic_4 fsout
number t=40u
number ke=0.01
number dl=15
number sw_sample_interval
{
        var i idrive
        state nu ft
        state nu drivestate,ncycles=0
        state nu sign,p1,p2,e,eold,ea,delta
        val v vdrive

        when(time_init) {
                schedule_event(time,ft,0)
                message("mppt_sample v1.3: using FIXED integration steps")    }

        when(dc_init) {
                delta=0.1
                p1=0
                p2=0
                drivestate=0
                ncycles=0
                e=1
                sign=1
        }

        when(event_on(ft)) {

                schedule_next_time(time)
                if(ft==1) {
                        schedule_event(time+(t/2),ft,0)
                        schedule_event(time+(t/2),fsout,14_0)
                        schedule_next_time(time+delta*t)
                }
                else {
                        schedule_event(time+(t/2),ft,1)
                        schedule_event(time+(t/2),fsout,14_1)
                        schedule_event(time+(t/2),drivestate,1)
                }
        }

        when(event_on(drivestate)) {

                schedule_next_time(time)
                if(drivestate==1) {
                        ncycles=ncycles+1
                        if(ncycles>=sw_sample_interval) {
                                ncycles=0

                                eold=e
                                p1=p2
                                p2=v(vcell)*v(icell)
                                e=p2-p1
                                if ((eold>0)&(e<0)) {
                                        sign=-sign
                                }
```

```
                        message("Evaluating powers: p1=% p2=% p2-p1=%",p1,p2,p2-p1)
                        if( ea > 15 ) ea=15

                        delta=delta+ke*sign
                        message("delta= %",delta)
                        if(delta > 0.9) delta=0.9
                        if(delta < 0.1) delta=0.1
                }
                schedule_event(time+delta*t,drivestate,0)
        }
    }

    values {
        if(drivestate==0) vdrive=0
        if(drivestate==1) vdrive=dl
    }

    equations {

        i(drive->gnd) +=idrive
        idrive: v(drive)-v(gnd)=vdrive
    }
}
```

A5: Maximum power tracker using proportional integration

```
##########################################################################
# Maximum power point tracking system for PV inverter
#
# Autonomous sample_point algorithm implementation v1.3a
#
# with proportional integration
#
# J.A. Gow 1994
##########################################################################
template mppt_sample_3a vcell icell gnd drive fsout = t,ke,dl,
                                sw_sample_interval
electrical vcell,icell,gnd,drive
state logic_4 fsout
number t=40u
number ke=1
number dl=15
number sw_sample_interval=5
{
      var i idrive
      state nu ft
      state nu drivestate,ncycles=0
      state nu sign,p1,p2,e,eold,ea,delta
      val v vdrive

      when(time_init) {
            schedule_event(time,ft,0)
      }

      when(dc_init) {
            delta=0.1
            p1=0
            p2=0
            drivestate=0
            ncycles=0
            e=1
            sign=1
      }

      when(event_on(ft)) {

            schedule_next_time(time)
            if(ft==1) {
                  schedule_event(time+(t/2),ft,0)
                  schedule_event(time+(t/2),fsout,14_0)
                  schedule_next_time(time+delta*t)
            }
            else {
                  schedule_event(time+(t/2),ft,1)
                  schedule_event(time+(t/2),fsout,14_1)
                  schedule_event(time+(t/2),drivestate,1)
            }
      }

      when(event_on(drivestate)) {

            schedule_next_time(time)
            if(drivestate==1) {
                  ncycles=ncycles+1
                  if(ncycles>=sw_sample_interval) {
                        ncycles=0

                        eold=e
                        p1=p2
                        p2=v(vcell)*v(icell)
                        e=p2-p1
                        if ((eold>0)&(e<0)) {
                              sign=-sign
                        }
```

```
                        message("Evaluating powers: p1=% p2=% p2-p1=%",p1,p2,p2-p1)
                        ea=abs(e)

                        if( ea > 15 ) ea=15
                        if( ea < 1 ) ea=1

                        delta=delta+(ea*ke*sign)
                        message("delta= %",delta)
                        if(delta > 0.9) delta=0.9
                        if(delta < 0.1) delta=0.1
                }
                schedule_event(time+delta*t,drivestate,0)
        }
}

values {
        if(drivestate==0) vdrive=0
        if(drivestate==1) vdrive=dl
}

equations {

        i(drive->gnd) +=idrive
        idrive: v(drive)-v(gnd)=vdrive
}
}
```

A6: Maximum power tracker using boost converter characteristic

```
#######################################################################
# Maximum power point tracking system for PV inverter
#
# Sample_point algorithm implementation using converter-generated # perturbation v1.1
#
# PROPORTIONAL integration
#
# J.A. Gow 1994
#######################################################################
template mppt_sample_1 vcell icell gnd drive fsout = t,ke,dl,n_interval
electrical vcell,icell,gnd,drive
state logic_4 fsout
number t=40u
number ke=1
number dl=15
number n_interval=5

{

	var i idrive
	state nu ft
	state nu drivestate
	state nu delta,p1,p2,e
	state nu count
	val v vdrive

	when(time_init) {

		schedule_event(time,ft,0)
		message("mppt_sample_1 v1.1: using PROPORTIONAL integration\n")
	}

	when(dc_init) {
		delta=0.1
		p1=0
		p2=0
		drivestate=0
	}

	when(event_on(ft)) {

		if(ft==1) {
			schedule_event(time+(t/2),ft,0)
			schedule_event(time+(t/2),fsout,14_0)
			schedule_event(time+delta*t,drivestate,0)
		}
		else {
			schedule_event(time+(t/2),ft,1)
			schedule_event(time+(t/2),fsout,14_1)
			schedule_event(time+(t/2),drivestate,1)
		}
	}

	when(event_on(drivestate)) {

		schedule_next_time(time)
		if(drivestate==0) {

			p2=v(vcell)*gain_iprobe*v(icell)*gain_vprobe
e=p2-p1
			if(e > 15 ) e=15
			if(e < -15) e=-15
			if(delta>0.9) delta=0.9
			if(delta<0.1) delta=0.1
			count=count+1
			if(count==n_interval) {
				delta=delta+ke*e
				message("evaluating powers: p1=% p2=% p2-p1=%",p1,p2,p2-p1)
				count=0
```

```
                }
        }
        else {
                p1=v(icell)*gain_vprobe*v(vcell)*gain_iprobe          }
    }

    values {
        if(drivestate==0) vdrive=0
        if(drivestate==1) vdrive=dl
    }

    equations {

        i(drive->gnd) +=idrive
        idrive: v(drive)-v(gnd)=vdrive
    }
}
```

A7: MAST diode current mode PI only controller

```
##########################################################################
# Current-mode control system for PV front end
#
# Implementation v2.0 23/2/95 with embedded current loop maximum power
# tracking.
#
# J.A. Gow 1995
##########################################################################

template cmcntrl v_out i_ind v_cell gnd drive fsout v_ref mppt_out = t,kv,dl,tr

electrical v_out,i_ind,v_cell,gnd,drive
state logic_4 fsout
electrical v_ref
state logic_4 mppt_out
number t=40u
number kv=1000
number dl=12
number tr=0.05u

{

      var i idrive
      state nu ft
      state nu drivestate
      state nu delta,i1,i2,p1,p2,iavg,e
      state nu iset,iset_k1,i_k
      state nu i_k1,delta_k1,idmd,idmd_k1,a
      state time slew=0
      val v vdrive


      when(time_init) {

            delta=0.1
            delta_k1=0
            i_k1=0
            iset_k1=0
            a=1
            idmd=0
            i1=0
            i2=0
            drivestate=0
            schedule_event(time,ft,0)
      }

      when(event_on(ft)) {

            if(ft==1) {
                  schedule_event(time+(t/2),ft,0)
                  schedule_event(time+(t/2),fsout,14_0)

# now work out average i1

                  iavg=(1-delta)*(i2+((i1-i2)/2))

# OUTER PI LOOP

#     simulate voltage loop amplifier

                  iset=(v(v_ref)-v(v_out))*kv
                  message("cmcntrl: iset (=vref-vout) : %",iset)

#     P+I compensator

                  idmd = 1.006*iset - 0.994*iset_k1 + idmd_k1
```

```
#       integrator limits on outer PI loop

                        if(idmd >  50) idmd= 50
                        if(idmd < -50) idmd=-50

#       z^-1 operations

                        idmd_k1=idmd
                        iset_k1=iset

                        message("cmcntrl: idmd : %",idmd)

# INNER PI LOOP

#       simulate current loop amplifier

                        i_k=(idmd-iavg)*9.5e-4


#       P+I compensation network

                        message("cmcntrl: i_k (=idmd-iavg) : %",i_k)
                        delta = 1.008*i_k - 0.992*i_k1 + delta_k1

#       integrator limits on inner PI loop

                        if(delta > 0.95) delta=0.95
                        if(delta < 0) delta=0

#       z^-1 operators

                        i_k1=i_k
                        delta_k1=delta

                        message("cmcntrl: delta : %",delta)

# now have new delta

                        schedule_event(time+delta*t,drivestate,0)
                }
                else {
                        schedule_event(time+(t/2),ft,1)
                        schedule_event(time+(t/2),fsout,14_1)
                        schedule_event(time+(t/2),drivestate,1)
                }
        }

        when(event_on(drivestate)) {

                schedule_next_time(time)
                slew=time+tr
                schedule_next_time(slew)
                if(drivestate==0) {

# turnoff point sample, both current and power

                        schedule_next_time(time)
                        i1=v(i_ind)
                        p1=i1*v(v_cell)

                }
                else {

# end of period sample, both current and power.

                        schedule_next_time(time)
                        i2=v(i_ind)
                        p2=i2*v(v_cell)
                }
        }

# analog values control - risetime additions.
```

```
        values {
                if(drivestate==0) {
                        if(time<slew) {
                                vdrive=((slew-time)/tr)*dl
                        }
                        else {
                                vdrive=0
                        }
                }
                if(drivestate==1) {
                        if(time<slew) {
                                vdrive=dl-((slew-time)/tr)*dl
                        }
                        else {
                                vdrive=dl
                        }
                }
        }

        equations {

                i(drive->gnd) +=idrive
                idrive: v(drive)-v(gnd)=vdrive
        }
}
```

A8: MAST diode current mode PI/embedded MPP controller

```
##########################################################################
# Current-mode control system for PV front end
#
# Implementation v2.0 23/2/95 with embedded current loop maximum power
# tracking.
#
# Implementation v2.1 7/6/95 with modified MPP section
#
# Implementation v2.2 21/6/95 with parametrized PI controller constants
#
# J.A. Gow 1995
##########################################################################

template cmcntrl2 v_out i_ind v_cell gnd drive fsout v_ref mppt_out = t,PI_V,
                                PI_I,dl,tr,mpp_sample_interval,ke

electrical v_out,i_ind,v_cell,gnd,drive
state logic_4 fsout
electrical v_ref
state logic_4 mppt_out
number t=13.3u                          # PWM time

struc {number gain,a0,a1;} \
      PI_V=(10,1.0006667,0.9993333),    # voltage loop
       PI_I=(0.06,1.0266667,0.973337)  # current loop

number dl=12                            # Output drive level
number tr=0.05u                         # Analog output risetime
number mpp_sample_interval=5            # interval between power sample pairs
number ke=0.001                         # MPPT integrator time constant

{

      var i idrive
      state nu ft                             # PWM clock
      state nu drivestate
      state nu delta,i1,i2,p1,p2,iavg,e
      state nu iset,iset_k1,i_k
      state nu i_k1,delta_k1,idmd,idmd_k1,a
      state nu mpp_active=0                   # Flag, nonzero for MPP
      state nu iavg_old,vref_old,vout_old     # Mimic delay in calculation
      state nu vref,vout
      state nu vdiff_k1                 # used in MPP termination
      state time slew=0
      val v vdrive

      when(time_init) {
            schedule_event(time,ft,0)
      }

      when(dc_init) {

            delta=0
            delta_k1=0
            i_k1=0
            iset_k1=0
            a=0
            idmd=0
            idmd_k1=0
            i1=0
            i2=0
            drivestate=0
            mpp_active=0
            iavg_old=0
            vref_old=0
            vout_old=0
            vdiff_k1=0
            message("cmcntrl V2.1:integrated PI/MPP PV front end controller\n")
      }
```

```
      when(event_on(ft)) {

            if(ft==1) {
                  schedule_event(time+(t/2),ft,0)
                  schedule_event(time+(t/2),fsout,14_0)

#       mimic calculation delay

                  iavg=iavg_old
                  vref=vref_old
                  vout=vout_old

                  vout_old=v(v_out)
                  vref_old=v(v_ref)

#       now work out average il and store for one cycle

                  iavg_old=(1-delta)*(i2+((i1-i2)/2))

# OUTER PI LOOP

#       simulate voltage loop amplifier

                  iset=(vref-vout)*PI_V->gain
                  message("cmcntrl: iset (=vref-vout) : %",iset)

#       P+I compensator

                  idmd = PI_V->a0*iset - PI_V->a1*iset_k1 + idmd_k1

#       integrator limits on outer PI loop

                  if(idmd >  50) idmd= 50
                  if(idmd < -50) idmd=-50

#       z^-1 operations

                  idmd_k1=idmd
                  iset_k1=iset

                  message("cmcntrl: idmd : %",idmd)


#       use condition to determine whether to use MPP or PI algorithms
#       MPP INITIATION CONDITION

                  if( ( p1 > p2 ) & ( idmd > iavg ) & (mpp_active==0) ) {

                        message("cmcntrl: EMBEDDED MPP ACTIVATED")
                        mpp_active=1

                  }

#       MPP TERMINATION CONDITION
                  if( mpp_active==1) {
                        if( (idmd <= iavg) | \
                              ( ((vout-vref) > 0) & (vdiff_k1 < 0) ) ) {

                              message("cmcntrl: EMBEDDED MPP TERMINATED")
                              mpp_active=0

#     reset outer and inner PI loop integrator initals to current values

                              idmd_k1=iavg
                              iset_k1=iset
                        }
                  }
                  vdiff_k1= vout-vref

# INNER LOOP: PI OR MAXIMUM POWER
# PI CONDITION
```

```
#       simulate current loop amplifier

                    i_k=(idmd-iavg)*PI_I->gain

                    if(mpp_active==0) {

#       P+I compensation network

                          message("cmcntrl: i_k (=idmd-iavg) : %",i_k)
                          delta = PI_I->a0*i_k - PI_I->A1*i_k1 + delta_k1

# END OF PI

                    }
                    else {

# MAXIMUM POWER CONDITION

                          a=a+1
                          message("cmcntrl: MPPSECT: a=%",a)
                          if(a==mpp_sample_interval) {

                                a=p2-p1
                                message("cmcntrl: MPPSECT: p2-p1=%",a)

#       limits on proportional integration

                                if(a > 10) a=5
                                if((a < 1)&(a > 0)) a=1
                                if((a > -1) & (a < 0)) a=-1
                                if(a < -10) a=-5

#       new duty cycle

                                delta=delta_k1+(ke*a)
                                a=0
                          }

                    }

# END OF MAXIMUM POWER

#       integrator limits on inner PI loop

                    if(delta > 0.90) delta=0.90
                    if(delta < 0) delta=0


#       z^-1 operators: held over MPP as well as PI to avoid significant
#       differences upon switching from MPP to PI

                    i_k1=i_k
                    delta_k1=delta


                    message("cmcntrl: delta : %",delta)

#       now have new delta

                    schedule_event(time+delta*t,drivestate,0)
              }
              else {
                    schedule_event(time+(t/2),ft,1)
                    schedule_event(time+(t/2),fsout,14_1)
                    schedule_event(time+(t/2),drivestate,1)
              }
      }

# PWM GENERATION FOLLOWS

      when(event_on(drivestate)) {
```

```
            schedule_next_time(time)
            slew=time+tr
            schedule_next_time(slew)
            if(drivestate==0) {

# turnoff point sample, both current and power

                  schedule_next_time(time)
                  i1=v(i_ind)
                  p2=i1*v(v_cell)

            }
            else {

# end of period sample, both current and power.

                  schedule_next_time(time)
                  i2=v(i_ind)
                  p1=i2*v(v_cell)
            }
      }

# ANALOG VALUES CONTROL - risetime additions.

      values {
            if(drivestate==0) {
                  if(time<slew) {
                        vdrive=((slew-time)/tr)*dl
                  }
                  else {
                        vdrive=0
                  }
            }
            if(drivestate==1) {
                  if(time<slew) {
                        vdrive=dl-((slew-time)/tr)*dl
                  }
                  else {
                        vdrive=dl
                  }
            }
      }
      equations {

            i(drive->gnd) +=idrive
            idrive: v(drive)-v(gnd)=vdrive
      }
}
```

A8: Inverter main control script

```
##########################################################################
# INV_CTRL.SIN
#
# Third generation (V3.0) controller for AC section of PV system. Uses
# predictive current loop sampling input voltages. Synchronized version,
# intended to be used in conjunction with protection and mode control
# modules. Switches two devices in a half-bridge arrangement in order that a
# 250V rms sinusoidal output may be achieved. System is PV-aware using an
# 'MPP' input to detect maximum power operation.
#
# Version 2.0 1/4/96  J.A. Gow: predictive controller algorithm by M. Fraser.
# Version 2.1 16/5/96         : updates DC rail voltages at each sample
# Version 3.0 5/7/96          : renamed INV_CTRL to maintain consistency in
#                               convention. MPP and mode-change system added
#                               and differential drive/input pins reduced to
#                               single ended. Back-calculation of inductor
#                               values present, but commented out in this
#                               version awaiting further trials. Note that
#                               'ref' is a state input, not an electrical pin
# Version 3.1 13/6/96 J.A. Gow: Experimental predictive capacitor current
#                           and load current feedforward added
#
##########################################################################

template inv_ctrl  v_out i_out i_load drv_h drv_l vdc_plus vdc_minus ref d_ref\
                   mp_vm mpp shutdown gnd = L,C,PI_V,t,tr,dl,dt,mp_astep, \
                                            vm_vout

electrical v_out,i_out,i_load,drv_h,drv_l,gnd,vdc_plus,vdc_minus
state logic_4 mp_vm,mpp,shutdown
state nu ref,d_ref

number L=4.1m                          # inductor value for prediction system
number C=10u                       # capacitor value for feedforward
struc {number gain,a0,a1;} \
      PI_V = (0.4,1.001,0.999)         # PI voltage loop
number t=50u                           # PWM cycle time
number dl=12                           # analog drive level
number tr=0.0                          # analog values risetime
number dt=0.0                          # deadband time
number mp_astep=0.1                    # amplitude step during MPP
number vm_vout=340                     # peak mains voltage for islanded op

{

      var     i       i_drive_h       # declarations: high side drive
      var     i       i_drive_l       # low side drive
      val     v       v_drive_h       # drive voltage: high side
      val     v       v_drive_l       # drive voltage: low side

      state   nu      clk             # system clock
      state   nu      drive_h=0       # drive condition: high side
      state   nu      drive_l=0       # drive condition: low side
      state   time    slew_h=0        # slewing time
      state   time  slew_l=0      # slewing time
      state   nu      vref            # sinusoidal reference
      state   nu      is1,is2,is3     # sampled output currents
      state   nu      il_n1,il_n2     # Average output current & delayed
      state  nu     iload         # Last cycle load current
      state   nu      vo_n1,vo_n2     # sampled output voltage & delayed
      state   nu      delta=0.5       # pulse duty cycle
      state   nu      idmd            # current demand
      state   nu      idmd_k1         # current demand*z^-1
      state   nu      err_v           # voltage loop error signal
      state   nu      err_v_k1        # voltage loop error*z^-1
      state   nu      Lcurr           # current value of inductance
      state   nu      Iavg            # predicted average current
      state   nu    st=1
```

```
# NEW IN VERSION 2.1, sampled output voltages etc.

      state   nu      Vdp             # positive DC rail voltage
      state   nu      Vdm             # negative DC rail voltage

# NEW IN VERSION 3, flags and control parameters.

      state   logic_4 run_stop        # running or halted
      state   logic_4 mode            # 14_1=voltage mode, 14_0=MPP
      state   nu      ref_ampl        # amplitude of reference
      state   nu    ic            # capacitor current

# DC initialization :
#   turn off the drive, zero analog signals and shifts.

      when(dc_init) {
          message("inv_ctrl: half-bridge inverter controller V3.0 for PV app")
         drive_h=0
         drive_l=0
         is1=v(i_out)
         is2=0
         is3=0
         il_n1=0
         il_n2=0
         vo_n1=v(v_out)
         vo_n2=0
         err_v=0
         idmd_k1=0
         err_v_k1=0
         delta=0.5
         vref=0
         Lcurr=L

         Vdp=v(vdc_plus)
         Vdm=v(vdc_minus)
         run_stop=14_0
         mode=14_0
         ref_ampl=0
         ic=0
      } #endwhen

# time-domain simulation initialization:
#   turn on the clock and start PWM generator state machine

      when(time_init) {
         Lcurr=L
         Vdp=v(vdc_plus)
         Vdm=v(vdc_minus)
         schedule_event(time,clk,0)
      } #endwhen

# test for a shutdown event.

      when(event_on(shutdown)) {
         if(shutdown==14_0) {
            message("inv_ctrl: INVERTER SOFTWARE SHUTDOWN AT %",time)
            run_stop=14_0
            drive_h=0;
            drive_l=0;
            schedule_event(time,drive_h,0)     # stop all drive signals
            schedule_event(time,drive_l,0)     # stop all drive signals
         } #endif
         if(shutdown==14_1) {
            run_stop=14_1
            message("inv_ctrl: INVERTER STARTED AT: %", time)
         } #endif
      } #endwhen

# test for a mode change and adjust accordingly

      when(event_on(mp_vm)) {
         mode=mp_vm
```

```
         if(mp_vm==14_0) {
            ref_ampl=10
         } #endif
      } #endwhen

# Sampling of analog signals and construction of sloped analog drive
# signal.

      when(event_on(drive_h)) {
         schedule_next_time(time)
         slew_h=time+tr
         schedule_next_time(slew_h)
         if(drive_h==1) {
            is1=is3
            is3=v(i_out)
            vo_n1=v(v_out)
            iload=v(i_load)
            Vdp=v(vdc_plus)
            Vdm=v(vdc_minus)
         } #endif
      } #endwhen

      when(event_on(drive_l)) {
         schedule_next_time(time)
         slew_l=time+tr
         schedule_next_time(slew_l)
         if(drive_l==1) {
            is2=v(i_out)
            vo_n2=v(v_out)
         }#endif
      } #endwhen


# MAIN TIMED LOOP:
#   events set up on rising and falling edges of CLK

      when(event_on(clk)) {
         if(clk==1) {
            schedule_event(time+(t/2),clk,0)
            if(run_stop==14_1) {    # check whether system run is desired


# RECALCULATION OF NEW DELTA:
#   PI compensator implemented using a direct implementation of the
#   z-transformed continuous PI controller.

# DEBUG INFO: calculate new average il for previous switching cycle
# note that in predictive system this is only for comparison and debugging
# it plays no part in the algorithm

               il_n1=(1-delta)*(is3+((is2-is3)/2))+ \
                  delta*(is1+((is2-is1)/2))

# CONTROL ALGORITHM SELECTION:
#    Alter control algorithm based upon selection of operating mode. This
#    distinguishes between utility feed and islanded modes of operation.
#    if 'mode' is high, voltage mode control is selected, if 'mode' is low,
#    utility feed operation is selected. Mode may only be changed over an
#    inverter shutdown.

               if(mode==14_1) {

# VOLTAGE LOOP
                  vref=vm_vout*ref                  # get reference
                  err_v=(vref-vo_n1)*PI_V->gain     # calculate error
                  idmd=PI_V->a0*err_v - PI_V->a1*err_v_k1 + idmd_k1
#                 if(idmd >  30) idmd= 30           # saturation limits
#                 if(idmd < -30) idmd=-30           # on demand signals
                  idmd_k1=idmd                      # z^-1
                  err_v_k1=err_v                    # z^-1

# Current loop voltage feedforward is only present when voltage loop is
```

```
# active.

                idmd=idmd+iload

             }
             else {

# MAXIMUM POWER REFERENCE GENERATOR
# For best efficiency of maximum power algorithm, all this system has to
# do is to cause MPP flag from front-end to be active, and to ensure that
# V+ drops only slightly: i.e. place some hysteresis in there

                if(mpp==14_0) {
                   ref_ampl=ref_ampl+mp_astep
                   message("inv_ctrl: RUNNING MAXIMUM POWER : increasing")
                }
                else {
                   if(Vdp < 360) {
                   ref_ampl=ref_ampl-mp_astep
                   message("inv_ctrl: RUNNING MAXIMUM POWER : decreasing")
                   } #endif
                } #endif

                message("inv_ctrl: RUNNING MAXIMUM POWER : ref_amp = %", \
                         ref_ampl)
                idmd=ref*ref_ampl

             } #endif

# CURRENT LOOP: active with all modes of
# PREDICTIVE CONTROLLER: DOES NOT USE CONVENTIONAL FEEDBACK APPROACH
# requires knowledge of L used in switching system and is topologically
# dependent upon the voltage across L during the switching cycles. idmd
# is demand current input to the controller.


# Controller average current calculation.

             Iavg=is3+(t/(2*Lcurr))*(delta*(2-delta)*(Vdp-vo_n1) +
                                     (((1-delta)**2)*(Vdm-vo_n1)))

# Capacitor current feedforward: Il=Iout+Ic : Ic=c*dv/dt
# used with all control algorithms.

             ic=C*d_ref*2*3.14*50*340
             idmd=idmd+ic

             if(idmd >  17) idmd = 17
              if(idmd < -17) idmd = -17

# Calculation of duty cycle using Lenz' Law, and averaging modulation voltage
# over one cycle

             delta=(((Lcurr*(idmd-iavg))/t)+vo_n1-Vdm)/(Vdp-Vdm)

# L back calculation commented out in this system pending operational
# simulation experimentation with the scheme

#                if((is2 ~= 0) & (is1 ~= 0)) {
#                   Lcurr=((Vdp-vo_n1)*delta*t)/(is2-is3)
#                }

             if(delta > 0.98) delta= 0.98
             if(delta < 0.02 ) delta= 0.02


# report the difference

             message("inv_ctrl: idmd = % : delta = %",idmd,delta)

# schedule the changes in delta and assign the drive states
```

```
                schedule_event(time+dt,drive_h,1)
                schedule_event(time+delta*t,drive_h,0)
                schedule_event(time+2*dt+delta*t,drive_l,1)
              } # endif
            } #endif
            else {
              if(run_stop==14_1) {
                schedule_event(time+(t/2),drive_l,0)
              } # endif
              schedule_event(time+(t/2),clk,1)
            } # endif
        } # endwhen

##############################################################################
# Analog sections:
##############################################################################
#
# Drive assignment:

        values {
            if(drive_h==0) {
              if(time<slew_h) {
                v_drive_h=((slew_h-time)/tr)*dl
              }
              else {
                v_drive_h=0
              } #endif
            } #endif

            if(drive_h==1) {
              if(time<slew_h) {
                v_drive_h=dl-((slew_h-time)/tr)*dl
              }
              else {
                v_drive_h=dl
              } #endif
            } #endif

            if(drive_l==0) {
              if(time<slew_l) {
                v_drive_l=((slew_l-time)/tr)*dl
              }
              else {
                v_drive_l=0
              } #endif
            } #endif

            if(drive_l==1) {
              if(time<slew_l) {
                v_drive_l=dl-((slew_l-time)/tr)*dl
              }
              else {
                v_drive_l=dl
              } #endif
            }  #endif
            if(time==0) {
                v_drive_l=0
                v_drive_h=0
            }
        } #endvalues

# Output through/across variable equations:

        equations {
                i(drv_h->gnd) += i_drive_h
                i_drive_h: v(drv_h)-v(gnd)=v_drive_h
                i(drv_l->gnd) += i_drive_l
                i_drive_l: v(drv_l)-v(gnd)=v_drive_l
        } #endequations
}
```

A9: AC section reference clock generator

```
##############################################################################
# REFGEN.SIN
#
# Reference waveform generator for PV inverter system. Uses a 50Hz (optional)
# and a 12.8kHz input (8-bit one cycle storage) to generate a sinusoid
# at 50Hz with 1V amplitude to be used as a phase and shape reference for
# the inverter. While free running, the generator requires only 'sampleclk',
# the 'phaseclk' (50Hz) input only required for mains synchronization.
# Note that the output, refout, is a number, not an electrical pin
#
# Version 1.0 5/7/96   J.A. Gow.  Initial version, simple in operation
##############################################################################

template refgen refout quad_ref phaseclk sampleclk

state nu refout,quad_ref
state logic_4 phaseclk,sampleclk

{
        state   nu      count                   # sample counter

# specify start-up conditions

        when(time_init) {
           count=0
        }

# generate the reference numbers.

        when(event_on(sampleclk)) {
           if(sampleclk==14_1) {
              schedule_event(time,refout,sin(2*3.141*50*count*7.8125e-5))
             schedule_event(time,quad_ref,cos(2*3.141*50*count*7.8125e-5))
              count=count+1
              if(count==256) {
                 count=0
              }
           }
        }

        when(event_on(phaseclk)) {
           if(phaseclk==14_1) {
              count=0
           }
        }
}
```

A10: Inverter protection logic

```
##############################################################################
# INV_PRTC.SIN
#
# Inverter and line protection module.
# Generates an inverter shutdown signal in response to dc rail anomalies
# and controls reference selection
#
# V1.0  6/6/96 J.A.Gow  :Initial version.
##############################################################################

template inv_prtc sd mp_vm breakers refsel lock gnd vo vp = t
electrical vo vp gnd
state logic_4 mp_vm breakers refsel lock

{
        when(event_on(lock)) {
           if(lock==0) {
              schedule_event(time,breakers,14_0)
              schedule_event(time,mp_vm,14_1)
              schedule_event(time,refsel,14_1)
           }
           else {
              schedule_event(time,mp_vm,14_0)
              schedule_event(time+10*t,breakers,1)
           } #endif
        } #endwhen

        when(event_on(threshold(v(vp),370))) {
           if(v(vp) <= 370 ) {
              schedule_event(time,breakers,14_0)
              schedule_event(time,sd,14_1)
           } #endif
        } #endwhen

        when(event_on(threshold(v(vo),260))) {
           if(v(vo) > 260 ) {
              schedule_event(time,breakers,14_0)
              schedule_event(time,sd,14_1)
           } #endif
        } #endwhen

        when(event_on(threshold(v(vo),220))) {
           if(v(vo) < 220 ) {
              schedule_event(time,breakers,14_0)
              schedule_event(time,sd,14_1)
           } #endif
        } #endwhen
}
```

APPENDIX C: A novel split-rail supply generator for use with medium power single phase inverter systems supplying live loads.

Paper presented at the Seventh European Power Electronics and Drives conference 1997 (EPE '97), Trondheim, Norway

J.A. Gow and C.D. Manning

Loughborough University, England

Abstract. Conventional single phase inverters, if supplying live loads, require a split-rail DC source to avoid the source voltage reference fluctuating with respect to earth. This paper proposes a method of generating a split-rail from a single ended DC supply with minimal components while maintaining good system dynamics.

Keywords: resonant converter, photovoltaic, split-rail generator.

INTRODUCTION

During the development of an advanced solar photovoltaic (PV) power conversion system, a requirement for a split-rail supply became apparent. The complete PV converter system consists of two parts; a front-end DC-DC converter, the control algorithms thereof designed with awareness of the requirements of the characteristics of photovoltaic arrays - and a single phase half-bridge inverter block which can supply either dead loads or feed a live utility (**Figure 299**).

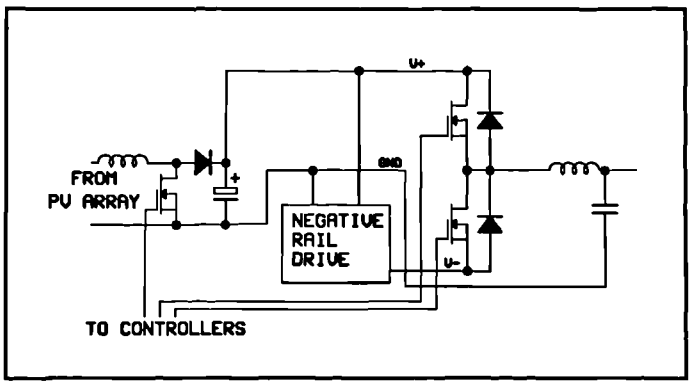


Figure 299 Basic power chain of photovoltaic power conversion system.

The control of both conversion blocks is effected in software running in a single digital signal processor, and available computation time is limited. The front-end converter control is aware of the characteristics of the PV array and can adjust its operational mode to compensate for the type of load being driven. When live inverter loads are driven the DC bus voltage may fluctuate with load changes as the converter maintains maximum power throughput. This converter has a single-ended positive DC output.

In order to maintain the integrity of the reference (GND) rail from input through to output, the single phase inverter block requires a split rail supply and a method thus had to be found of generating a negative rail from a single positive rail. The obvious method is to use an up/down flyback converter (Kassakian et al [1]). Such a scheme is workable, but is possessed of a number of disadvantages in operation. Most of these stem from the right-hand plane zero present in the small-signal control-to-output transfer function. If the flyback converter is placed under voltage mode control (this being the least hardware and computationally intensive method) due to the bandwidth limitations required in the controller imposed by the right hand plane zero there will be a lag in the current waveform (**Figure 300**). This lag will result in the total current drawn from the front-end converter appearing as a series of high amplitude pulses (although the RMS level will be consistent) between which little current is drawn. Using a conventional low impedance DC supply this is not a problem, however if the front end is operating in maximum power mode the large current pulses may result in excessive excursions of the positive rail voltage, even to the point where the pulse-width (PWM) modulator clips. The addition of a further PWM channel and control system is in itself a disadvantage in terms of computation time and added hardware complexity.

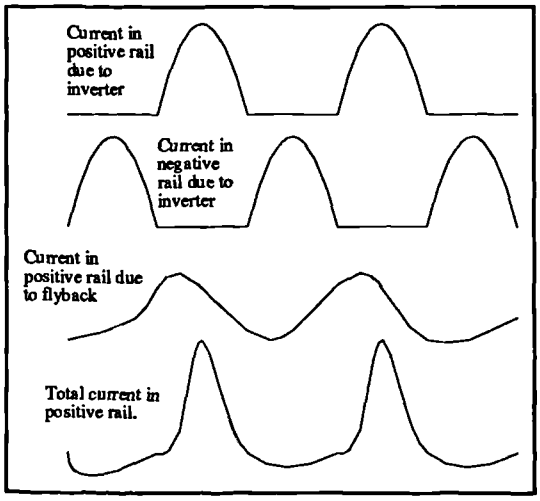


Figure 300 Current waveshapes when using conventional split-rail generator.

Current mode control will improve the current tracking, but it will also require a further current sampling channel adding to the complexity of the split rail supply still further.

One further alternative approach would be to use a forward converter with a transformer, but advantages are to be gained from removing transformers from the system due to the inherent bulk and cost associated with such items. It was desired to develop a split-rail supply that would address all of these criticisms.

It is worth noting at this point that the inverter control was implemented using a form of predictive control algorithm similar to that used by Fraser and Manning [2]. This algorithm has a property of good DC rail ripple rejection providing that the rail voltage is not allowed to fall below the clipping point of the PWM modulator, or that its rate of change is so high as to invalidate the sample taken by the controller at the start of the switching cycle. Therefore extremely tight regulation of the negative rail is unnecessary and it may fluctuate between reasonable limits, providing that the fluctuation is not too fast. To meet these requirements the following resonant rail drive system was devised. It requires no external control, it features good bus voltage tracking and also reasonably accurately reflects the current profile drawn from the negative rail into the positive rail without introducing any significant delays.

ANALYSIS.

Consider the system of **Figure 301.** The four switches are operated in pairs; S1 and S3 form one pair while S2 and S4 form the other. These switches operate in antiphase with a 50% duty ratio, and with a small deadband present to eliminate shoot-through effects. The resulting system can be reduced to one having two distinct states. The first of these states occurs when the S1-S3 pair are closed and the effective circuit is shown in **Figure 302.** The second state, giving the effective circuit of **Figure 303** occurs when the switch pair S2-S4

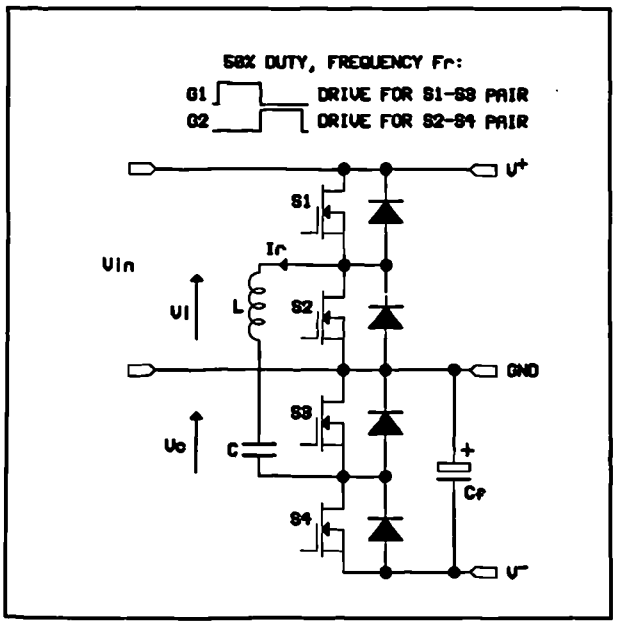


Figure 301 Proposed resonant rail inverter system.

are closed. The reverse-parallel diodes across the switching elements allow current in the resonant circuit to flow in both directions during both states making the circuit completely symmetrical and allowing the bidirectional flow of current between positive and negative rail. This allows current fed back into the negative rail (by, for example, a reactive load on the inverter) to be returned to the positive rail thus enhancing the bus voltage tracking. The resistance R in **Figure 302** and **Figure 303** is the lumped switch resistance (effectively twice the on-resistance of a single switch) and the series resistances of both the inductor and the capacitor.

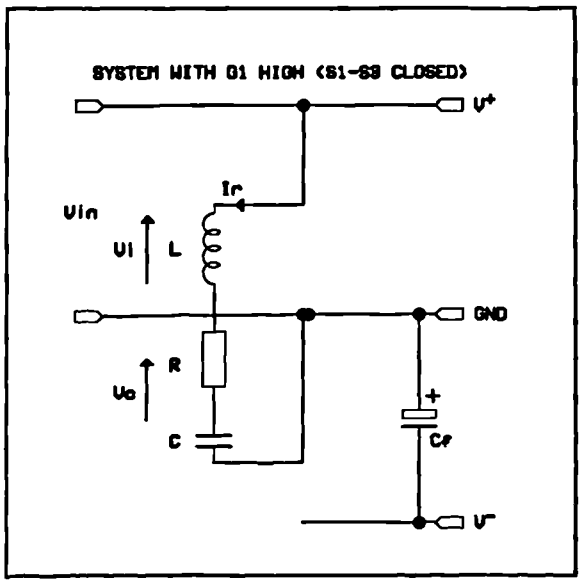


Figure 302 System in first state.

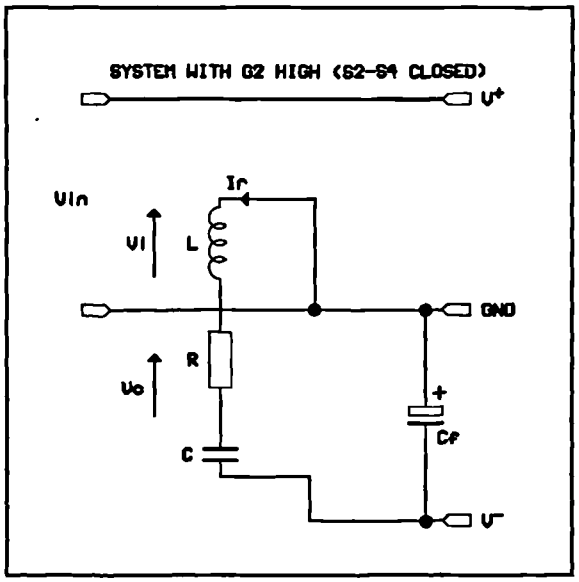


Figure 303 System in second state

An aspect of design of the system is that the resonant frequency of the series-resonant arm C and L is made equal to the switching frequency. This results in a half-cycle of resonance being complete at the instant that the switches change state (zero-current switching). The full timing of the system is shown in **Figure 304**. The switches thus always change state at a point of zero current, eliminating switching losses in the silicon. Although the resonant frequency will change slightly as R varies, the change should not be that great over most practical values of R

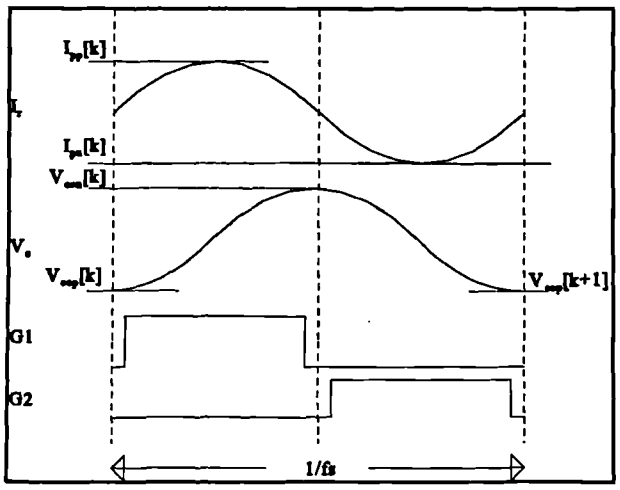


Figure 304 Timing of resonant rail invert system.

and thus this zero-current switching arrangement will not be violated sufficiently to cause a rapid increase in losses.

In a detailed analysis, the first consideration will be the currents flowing in the resonant circuit and the voltage across the capacitor during state 1. Given that the switching frequency has been made equal to the resonant frequency, then state 1 will last for one half of a cycle of resonance. The presence of R ensures that the resonance will decay exponentially. During state 1, the circuit current may be written as (86) where V_{cop} is the capacitor voltage at the start of state 1 and V^+ is the positive rail voltage.

$$I\left(sL+\frac{1}{sC}+R\right)+\frac{V_{cop}}{s} = \frac{V^+}{s} \tag{86}$$

Rearranging and inverse-Laplace transforming results in the expected time domain expression for the current in the resonant chain during state 1 (87) :

$$I = \left(V^+-V_{cop}\right)\frac{1}{L\omega}e^{-Bt}\sin\omega t$$
$$\text{where} \quad B=\frac{R}{2L} \quad \text{and} \quad \omega=\sqrt{\frac{4L-R^2C}{4L^2C}} \tag{87}$$

where the anticipated slight shift in frequency is obvious.

With an expression now available for the current waveform, which is valid during the length of state 1, it is now possible to derive a similar Laplace-domain expression for the voltage across the capacitor during state 1 in terms of time and the initial voltage (88):

$$V_c = \frac{V^+}{s}-I(sL+R) \tag{88}$$

and substituting for I from (87) and inverse-Laplace transforming gives:

$$V_c = V^+ - \left(V^+ - V_{cop}\right)e^{-Bt}\left[\cos\omega t + \frac{B}{\omega}\sin\omega t\right] \tag{89}$$

where B and ω have the same definitions as in (87).

Turning attention now to state 2, it can be seen that the expressions will be identical apart from the sign of the rail voltage: i.e. V^+ in (87) and (89) becomes $-V^-$ during state 2. Note that the sign of the initial voltage on the capacitor remains the same as the current is being considered with respect to the resonant chain itself. The current will therefore reverse direction from that in (87). The system is bidirectional and symmetrical. Although in this case consideration is being made of the effect of a load on the negative bus causing the negative rail voltage to fall (in magnitude) below that of the positive rail, the same equations will apply if the magnitude of the voltage on the negative rail should rise above that of the positive rail (such as if the inverter is driving a heavily reactive load) and the system will compensate accordingly. Therefore, for state 2:

$$I = -\left(V^- + V_{con}\right)\frac{1}{L\omega}e^{-Bt}\sin\omega t \tag{90}$$

$$V_c = -V^- + \left(V^- + V_{con}\right)e^{-Bt}\left[\cos\omega t + \frac{B}{\omega}\sin\omega t\right] \tag{91}$$

where V_{con} is the voltage on the capacitor at the start of state 2. To solve the system about the node at the lower end of C_f in **Figure 301**, it is necessary to know the average current that the resonant arm feeds to this node across a single cycle. This current will be half-sinusoidal and will flow for one half of a cycle - therefore its average may be found by dividing the peak value by π. This is valid providing the voltage at V^- does not change significantly across the time of a single switching cycle. For most practical values of C_f (1500μF in this system) any changes of V^- will occur at a rate much slower than one switching cycle. However, it is also clear from (87) and (90) that the current is dependent upon the initial voltage on the capacitor at the start of the

cycle. It therefore becomes necessary to develop a relation expressing V_{con} in terms of known system parameters.

Consider the half-cycle of current during state 1. V_c at the end of the cycle is equal to V_{con}. At the start of state 1, V_c at the end of the cycle is equal to V_{cop}. The switching period is constant, and so it is possible to develop a difference equation relating a current value of V_{con} to a previous value, one cycle earlier. From (91) for the current state 2, at the end of the cycle when $\omega=\pi$:

$$\begin{aligned} V_{cop} &= -V^- - \left(V^- + V_{con}[k]\right)e^{-B\frac{\pi}{\omega}} \\ &\quad let \quad A = e^{B\frac{\pi}{\omega}} \\ \therefore V_{cop} &= -V^- - A\left(V^- + V_{con}[k]\right) \end{aligned} \tag{92}$$

where $V_{con}[k]$ indicates the current value of V_{con}. Now, for the following period at state 1:

$$V_{con}[k+1] = V^+ + A\left(V^+ - V_{cop}\right) \tag{93}$$

where $V_{con}[k+1]$ indicates the next value of V_{con}. Substituting (92) into (93) gives rise to the desired relation:

$$V_{con}[k+1] = V^+(1+A) + AV^-(1+A) + A^2 V_{con}[k] \tag{94}$$

It is possible to rearrange (94) in the conventional form of a difference equation in terms of its two inputs V^+ and V^- and by use of the z-operator to denote a one-cycle delay it is possible to express it in the form of a transfer function multiplied by the 'input' $V^+ + AV^-$:

$$V_{con} = \frac{(1+A)}{A^2} \cdot \frac{1}{\frac{1}{A^2} - z^{-1}} \cdot (V^+ + AV^-) \tag{95}$$

A z-domain expression now exists (95) relating V_{con} in terms of the two system parameters V^- and V^+, and the decay parameter A. All direct reference to the cycle time interval has been

successfully eliminated from the expression and it is possible to use this expression in a time-domain analysis of the system.

If R=0, then A=1, and the denominator of the z-domain component of the expression in (95) reduces to $1-z^{-1}$, that of a pure integrator integrating the difference between the two rails. If R=0, and a difference should occur in rail voltage magnitudes, the peak capacitor voltage at the start of state 2 (the point at which it is at its largest) will ramp upwards, causing a corresponding increase in the current in the resonant arm. This will supply the current demand from the negative rail and continue to increase, charging C_f until the rail voltages are once again equal.

It is now possible to solve around the node at the bottom of the filter capacitor C_f (**Figure 305**) to obtain V^-. The current in this capacitor is the algebraic sum of the current from the resonant circuit and the load current. The peak of the current waveform occurs half of the way into the state, at $\omega t=\pi/2$, therefore substituting into (90):

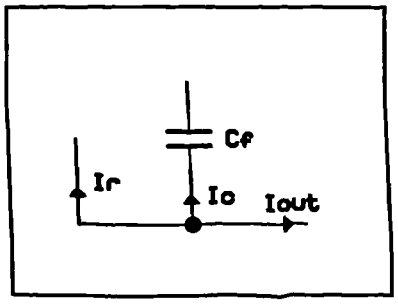


Figure 305 Node at V^-

$$I_{peak} = -\left(V^- + V_{con}\right)\frac{1}{L\omega}e^{-B\frac{\pi}{2\omega}} \tag{96}$$

therefore assigning:

$$C = \frac{1}{L\omega}e^{-B\frac{\pi}{2\omega}} \tag{97}$$

then

$$I_{avg} = -\frac{C}{\pi}\left(V^- + V_{con}\right) \tag{98}$$

The next stage is to solve the node equation at V^-:

$$C_f \frac{dV^-}{dt} = -i_r - i_{out} \tag{99}$$

Substituting (95) into (98) gives an expression for i_r:

$$i_r = -I_{avg} = \frac{C}{\pi}\left(V^- + \frac{1+A}{A^2} \cdot \frac{1}{\frac{1}{A^2} - z^{-1}} \left(V^+ + AV^-\right) \right) \tag{100}$$

and substituting (100) into (99) gives an expression which completely describes the resonant rail invert drive system, (101).

$$C_f \frac{dV^-}{dt} = -\frac{C}{\pi}\left(V^- + \frac{1+A}{A^2} \frac{1}{\frac{1}{A^2} - z^{-1}} \left(V^+ + AV^-\right) \right) - i_{out} \tag{101}$$

Transfer functions.

It is possible to derive a set of transfer functions from (101), relating I_{out} to V^-, V_{con} and I_{peak}. These parameters are the main ones of interest in selection of adequately rated components. Once this function is derived it is possible to convolve it with the appropriate 'worst-case' I_{out} profile by multiplying the Laplace-transform of the current profile by the transfer function, and inverse-transforming the result. Algebraic operations on the time-domain result will yield the quantities of interest.

In developing a transfer function for (101), the discrete term was first converted to an equivalent continuous term. Emulation using the bilinear transform (Forsyth and Goodall [3]), a common method which for high sample rates provides a good approximation was used. (102) shows the transformation:

$$\frac{1}{\frac{1}{A^2}-z^{-1}} \rightarrow \frac{A^2}{1+A^2}\frac{\frac{2}{T}+s}{\frac{2(1-A^2)}{T(1+A^2)}+s} \tag{102}$$

where T is the cycle time. Clearly as R tends to zero, A tends to 1 and the denominator of the frequency-dependent term in **(102)** tends to a single s, i.e. an integrator. Now substituting **(102)** for the discrete portion of **(101)**, we arrive at:

$$C_f\frac{dV^-}{dt} = -\frac{C}{\pi}\left(V^- + \frac{1+A}{1+A^2}\frac{s+\frac{2}{T}}{s+\frac{2(1-A^2)}{T(1+A^2)}}(V^+ + AV^-)\right) \tag{103}$$

Given this function, it is now possible to derive the s-domain transfer function that is required. The initial conditions on the system before any change in I_{out} are obtained from the assumption that the system has been running for a sufficient length of time when I_{out} is zero: this is that the magnitude of V^- is equal to that of V^+. In **(101)**, the initial condition on V_{con} is provided for by the V^+ in the $(V^+ + AV^-)$ term, while the initial value of V^- is the initial condition on the C_f integrator. If the worst case load on the negative rail is switched in during a negative half cycle on the inverter being driven, the system would have the positive half cycle to recover and thus a start from steady-state is a reasonable assumption. To simplify the system prior to calculation of the transfer functions we can normalize the system about V^+. This removes V^+ from the equations and results in functions whose outputs would be zero-referenced. It is then necessary to simply sum in the magnitude of V^+ into the voltage terms of the result to obtain absolute values. To do this it is realized that after full recovery, when $I_{out}=0$ and $V^+=-V^-$, then $V_{con}=-V_+$. Under these conditions current down the resonant chain is zero at all times, and the capacitor voltage does not change across successive switching cycles: i.e. $V_{con}=V_{cop}$. To implement this normalization, the initial conditions on the two frequency-dependent terms are set to zero. V^+ is removed from the equation.

It is possible to express the normalized continuous model as a block diagram (**Figure 306**, generated by SIMULINK [4]) in which the new constants defined are given in **(104)**.

$$D=\frac{A(1+A)}{1+A^2},\ E=\frac{2}{T},\ F=\frac{E(1-A^2)}{1+A^2},\ G=\frac{C}{\pi} \qquad \textbf{(104)}$$

From it some of the unique properties of this system may be seen.

Firstly, the system possesses an intrinsic feedback loop, which serves to regulate V^- against changes in I_{out}. This is a considerable advantage as there is no requirement for further forced regulation of V^- by way of external control and the only stimulus required by the system will be two antiphase 50% duty switching signals. The series resistance of the LC chain (including switch on-resistance) will clearly affect the regulation. As R tends to zero, so the denominator in the discrete portion of **(102)** will tend to that of an integrator. Integral feedback will reduce the steady-state error of the system to zero, conversely the further the pole in the feedback loop is away from $z^{-1}=1$ the worse the steady state error, flattening out at a value determined by the gain of the feedback path. Since this gain tends to zero as R tends to infinity (due to the A term in the V^- path) the regulation will worsen the larger the value of R. With low values of R the system will appear as two integrators 'chasing' each other, a system which can only be oscillatory. The decay term introduced by the V^- term summed in the equation for I_{avg} will ensure that the oscillations will never be continuous, that they will always decay, but for very low values of R it can be seen that the excursions of V_{con}, V^- and I_{peak} may be high.

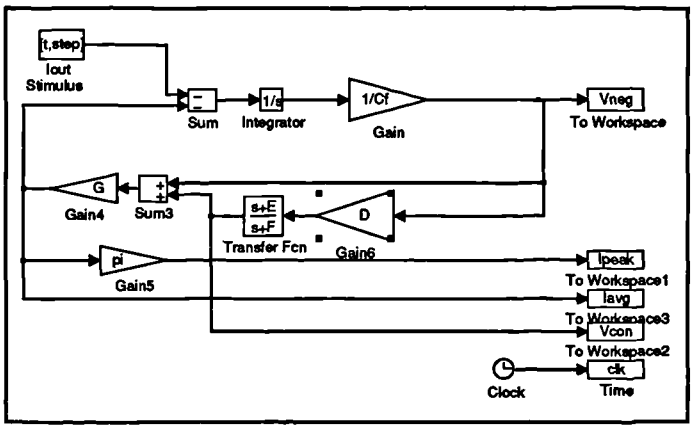


Figure 306 Normalized continuous model.

In a practical implementation, it is necessary to have knowledge of what the worst-case excursions of voltage and current may be in order to adequately size the components in the

system. To this end it would be useful to be able to solve the system of **(103)** given what would constitute a 'worst case' I_{out} profile in order to determine what effect the changes in the system components will have on the complete system. It is now possible to derive a transfer function. Starting with the characteristic of the feedback path:

$$I_{avg} = V^{-}G\left(\frac{(DE+F)+s(1+D)}{s+F}\right) \tag{105}$$

and that of the forward path:

$$V^{-} = -\frac{1}{sC_f}\left(I_{out}+I_{avg}\right) \tag{106}$$

Combining **(105)** and **(106)** rearranging gives the desired transfer function of V^{-} to I_{out}:

$$\frac{V^{-}}{I_{out}} = -\frac{s+F}{s^2C_f+s(FC_f+G+GD)+G(DE+F)} \tag{107}$$

Simplifying this by assigning two new variables:

$$H = FC_f+G+GD \ , \quad I = G(DE+F) \tag{108}$$

then

$$\frac{V^{-}}{I_{out}} = -\frac{1}{C_f}\frac{s+F}{s^2+s\frac{H}{C_f}+\frac{I}{C_f}} \tag{109}$$

It is possible now to derive two further transfer functions, one to relate V_{con} to I_{out}, and a second to relate I_{peak} to I_{out}. Combining **(109)** with **(105)** gives the I_{avg}-I_{out} transfer function, which only has to be multiplied by π to give I_{peak} **(110)**. To obtain V_{con}-I_{out} transfer characteristic, **(109)** is combined with D(s+E)/(s+F) to give **(111)**. It is important to realize that both of the two voltage transfer functions are normalized about the rail voltage magnitude, therefore to obtain absolute values it is necessary to add the steady-state values of V^{+} to **(111)**, and V^{-} to **(109)**. The resonant circuit current is based about zero and will not require any further manipulation.

$$\frac{I_{peak}}{I_{out}} = -\frac{\pi G}{C_f}\frac{(DE+F)+s(1+D)}{s^2+s\frac{H}{C_f}+\frac{I}{C_f}} \tag{110}$$

$$\frac{V_{con}}{I_{out}} = -\frac{1}{C_f}\frac{D(s+E)}{s^2+s\frac{H}{C_f}+\frac{I}{C_f}} \tag{111}$$

Transfer functions are now available for the complete system, and it is interesting to note that they are all of the standard second order form. From these, if the I_{out} profile is known, it is possible obtain a time response of the system from which the maximum values of each of the system parameters may be determined for a worst-case load transient at the output of the inverter which the rail drive system is supplying. To do this, it is necessary to know the effect of a step load change at the inverter output on the current demand from the negative rail.

For the inverter being driven, it can be determined that the worst-case load change at the negative rail will occur if a high crest factor load (such as a bridge rectifier driving a filter capacitor) rated at full load of the inverter is switched in half way through the negative half cycle. The inverter software current limit is placed at 17A in order to allow such high crest factor loads to be driven. The profile of this current will be a ramp whose slope will be governed by the output filter inductor value and the difference between maximum output voltage and d.c. rail voltage. Once the 17A limit current is reached the inverter will clamp the current and it will increase no further. At the instant of the load being switched in the inverter inductor voltage will be equal to the peak AC output voltage (the load rectifier filter capacitor is discharged at the time of switching)

To describe this characteristic in the s-domain is straightforward; a ramp from zero decreasing until -17A is reached, then a time-shifted ramp subtracted from it (equation **(112)**):

$$AMP\left(\frac{1}{s^2}-\frac{e^{\tau s}}{s^2}\right) \tag{112}$$

where

$$AMP = \frac{E}{L}, \quad \tau = \frac{I_{max}}{AMP} \tag{113}$$

E is the inverter inductor voltage, L is the value of the inverter inductor and I_{max} is the limit current. The time-domain expressions will take the form of the inverse-Laplace transform of (32) convolved with the form of (28)-(30). and the general form is given in **(114)**. All that remains is to calculate the appropriate constants a,b and c for the transfer function required and insert them. These are given in the substitution table **Table 22**.

Table 22 Constant substitution table:

$$A = e^{-B\frac{\pi}{2}}, \; B = \frac{R}{2L}, \; C = \frac{1}{L\omega_r} e^{-B\frac{\pi}{2\omega_r}}, \; D = \frac{A(1+A)}{1+A^2}$$

$$E = \frac{2}{T}, \; F = \frac{E(1-A^2)}{1+A^2}, \; G = \frac{C}{\pi}, \; H = C_{ff}+G+GD$$

$$I = G(DE+F), \; \omega_r = \sqrt{\frac{4L-R^2C}{4L^2C}}$$

$$For \; \frac{V^-}{I_{out}}: \; AMP=\frac{AMP}{C_f}, \; a=F, \; b=\frac{H}{C_f}, \; c=\frac{I}{C_f}$$

$$For \; \frac{V_{con}}{I_{out}}: \; AMP=\frac{D.AMP}{C_f}, \; a=E, \; b=\frac{H}{C_f}, \; c=\frac{I}{C_f}$$

$$For \; \frac{I_{pk}}{I_{out}}: \; AMP=\frac{\pi G(1+D)AMP}{C_f}, \; a=\frac{DE+F}{1+D}, \; b=\frac{H}{C_f}, \; c=\frac{I}{C_f}$$

$$F(t) = -AMP\left[\frac{1}{c}-\frac{a}{c}\frac{2z}{\omega^2+z^2}+\frac{a}{c}t + \left[\frac{a}{c}\left(\frac{z^2}{\omega(\omega^2+z^2)}-\frac{\omega^2}{\omega^2+z^2}\right)-\frac{z}{c\omega}\right]e^{-zt}\sin(\omega t) + \left[\frac{a}{c}\frac{2z}{\omega^2+z^2}-\frac{1}{c}\right]e^{-zt}\cos(\omega t)\right]$$

For $0<t<\tau$:

$$F(t)=F(t) \qquad \textbf{(114)}$$

For $t>\tau$:

$$F(t)=F(t)-F(t-\tau)$$

where $z=\frac{b}{2}, \omega=\sqrt{c-\frac{b}{2}}$

The form of **(114)** indicates that the response will be of exponential order, which for some values of L,C and R will be sinusoidal. The discontinuity present in this equation indicates that to reduce this into a form from which the maximum values may be determined would be analytically intractable. As a result it was decided that it would be more useful to develop a numerical solution of **(114)**, and plot the result as graphs showing maximum values as a function of system parameters.

MATLAB MODELLING

To assist in rating the components in the resonant rail drive system, MATLAB [4] scripts were written to solve the ramp responses given values of L,C and R. For the inverter under consideration with an inductor of 4.13mH and a peak output voltage of 340V, the rate of change (di/dt) of the ramp portion of the worst-case profile will be $0.0823A\mu s^{-1}$, with a limit of -17A.

In a practical system, it is simple to fix L and C, but R may vary as it contains the lumped resistances of the switches. It is useful to know what the optimum value of R is, and as it plays a large part in the damping of the response of the system it will also affect the maximum values of the parameters significantly.

To simplify the rating of the components required in such a system, the MATLAB scripts were developed to extend the characterization of the system and provide a simple set of graphs from which a suitable set of ratings for the components could be deduced quickly. There are initial requirements of the system which must first be satisfied.

Requirement 1. The frequency of resonance of the LCR series arm must be as close as possible to the switching frequency to ensure that zero-current switching occurs. The value of the LCR frequency will change with R, but the frequency of resonance may be allowed to deviate slightly from the switching frequency, and in most practical cases it will be acceptable to calculate values using the value of LC resonance (ignoring R). However, the difference between the LC value and the LCR value of resonant frequency is dependent upon the Q of the inductor, and it is advisable to ensure that the Q of the system is high. This ties in with the second requirement.

Requirement 2. The shape of the current in the resonant arm must be sinusoidal. If it becomes exponential, the system will cease to function correctly. The manner in which this requirement relates to the values of L and C may be expressed mathematically as follows. First, assume that the product of the values of L and C have been obtained from the switching angular frequency ω, i.e. $LC=(1/\omega)^2$. Then it is possible to define the ratio of L and C, L/C, as k. Now from LCR series resonance:

$$\omega_r = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \tag{115}$$

For the system to remain resonant, ω_r must be wholly real. The point of transition to an exponential system occurs when:

$$\frac{1}{LC} = \frac{R_{max}^2}{4L^2} \therefore R_{max} = 2\sqrt{\frac{L}{C}} = 2\sqrt{k} \tag{116}$$

$$\therefore \textit{for resonance } R \leq 2\sqrt{k}$$

We now have an expression which will give the largest possible value of R with which an implementation of the system will function for a given value of switching frequency and of k

(=L/C). It should be noted that at extremes of the ranges it is possible to violate requirement 1 for resistance values that satisfy the inequality of **(116)** as the frequency shift is too great. This is dependent upon the inductor Q value.

Using the MATLAB scripts, a set of families of maximum-value curves were plotted at the 25kHz switching frequency using nine values of k of 0.5,1,2,4,6,8,10,12 and 13 across a resistance range of 0-1 ohm and an output filter capacitance of 1500μF. The current profile used was the expected worst-case demand from a predictive-mode controlled inverter. The value of bus filter capacitor was chosen as the one used in the development of the photovoltaic inverter system - the MATLAB script can be run with any value desired. The start value of k=0.5 ensures that requirement 2 is not violated across the resistance range. Two further sets were plotted at switching frequencies of 10kHz and 15kHz, but these were identical to the set at 20kHz and thus confirm the fact that the system characteristics are independent of switching frequency other than that the LCR resonance must be identical to it - the appearance of the switching frequency in the discrete-to-continuous conversion of the capacitor voltage transfer function in the derivation of the model having negligible effect at power electronics frequencies. The MATLAB model compensates for the effect of R in that knowing L,C and R, it back-calculates ω (requirement 1 always met). The plots are shown in **Figure 308, Figure 307, Figure 309** and **Figure 310.**

Finally, using the Saber [5] simulation platform, the entire circuit of **Figure 302** was simulated at the circuit level, and the resulting waveforms shown in **Figure 312** and **Figure 311** show the expected inductor current, negative rail voltage and capacitor voltage from a workable system with resistance values of 0.04 and 0.2 showing the difference between a system with oscillatory response and tight rail regulation, or exponential response with slightly poorer rail regulation.

Figure 313 shows the results obtained from actual hardware where L=24.3μH, C=2.6μF and C_f=1500μF, with a switchable 1kW load. R is difficult to quantify as IGBT devices were used as the switching elements - there is an element of fixed voltage drop as well as ohmic drops. During the load on time, the positive rail dropped due to the supply impedance, but with the positive rail at 353V and the negative rail at 347V the tracking of the system can be seen to be

very good indeed for an open-loop system. At the time of writing the inverter code was not complete, and thus these results are obtained using a step load change (which is in effect worse than the ramp). It can be seen that with systems that do not require extremely tight rail regulation this approach has considerable merit.

CONCLUSION

A novel resonant rail drive system has been developed which operates in open loop while still providing reasonable rail regulation. It provides accurate reflection of current in the negative rail into the positive rail -it provides no current lag. It is very useful in the photovoltaic system under development, and will have other uses when driving inverter-type loads whose control system does not rely on tightly regulated voltage rails. An analysis for the rail invert drive has been carried out allowing ease of sizing and rating components.

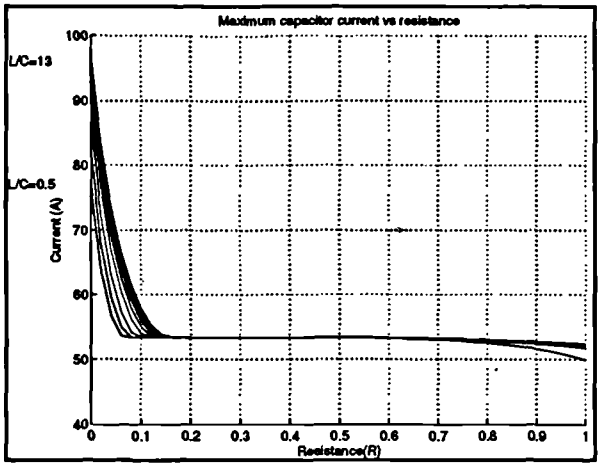


Figure 307 20kHz: maximum capacitor current.

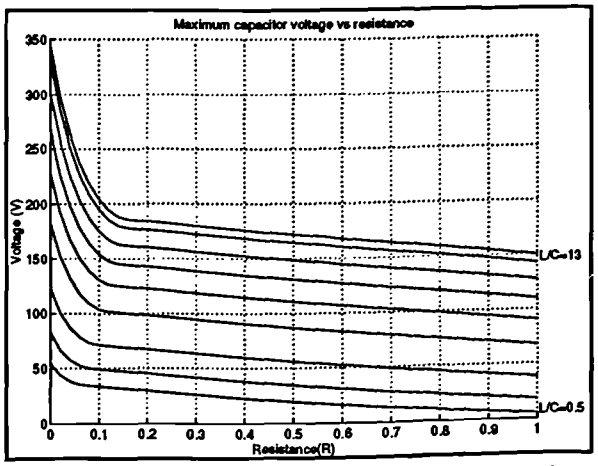


Figure 308 20kHz: maximum capacitor voltage change.

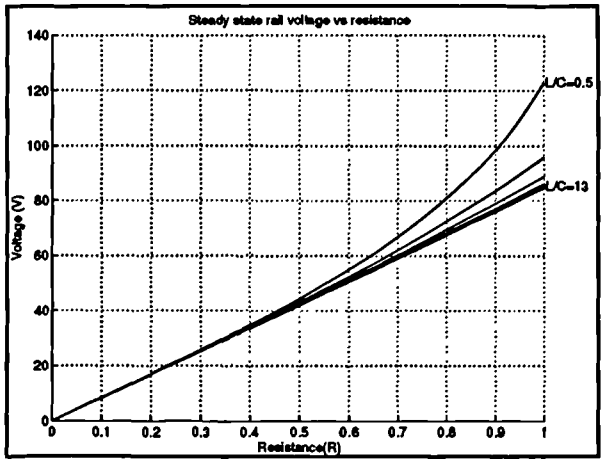


Figure 309 20kHz: steady state rail voltage.

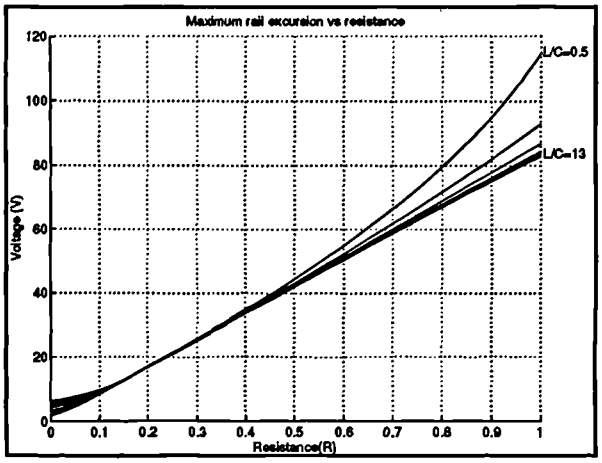


Figure 310 20kHz: maximum rail excursion vs resistance.

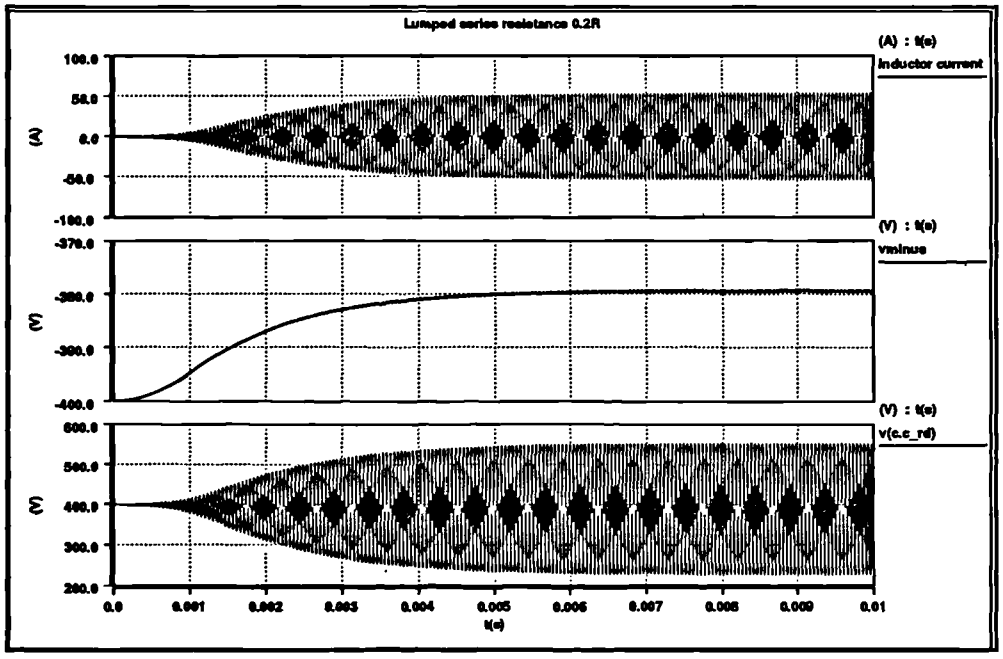


Figure 311 Saber simulation of complete resonant rail drive: R=0.20.

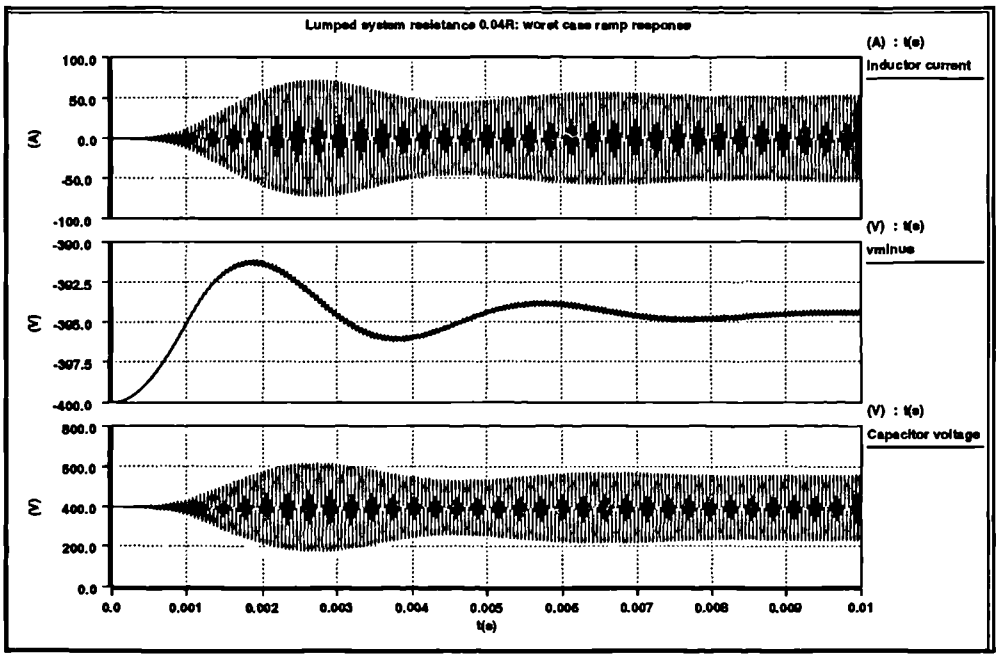


Figure 312 Saber simulation of complete resonant rail drive: R=0.04

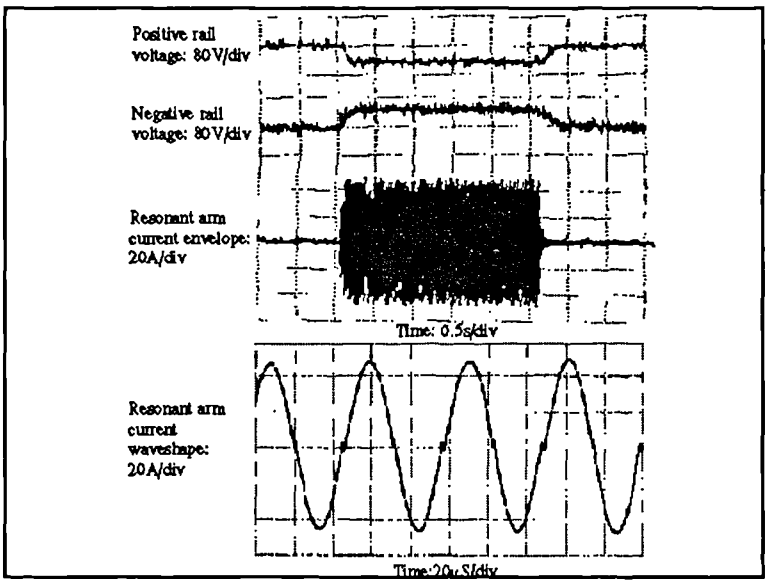


Figure 313 Results from a practical system - using step load change.

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