Thermo-mechanical Damage Accumulation during Power Cycling of Lead-Free Surface Mount Solder Joints

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Abstract

It is well known that in surface mount technology (SMT), thermal strains in electronic assemblies are induced in the solder joints by the mismatch between the coefficients of thermal expansion (CTE) of the components, substrate and solder, both during their processing and in service. Therefore, thermo-mechanical damage is likely to occur in the solder and the principle reliability hazard in SMT assemblies is the resulting fatigue cracking of the solder fillet, caused by cyclic thermal stresses. These stresses may be caused by both cyclic variations in power dissipation within equipment and by external environmental temperature changes. Most work reported to date has focused on the effects of environmental temperature changes, although for many types of equipment power cycling may result in significant stresses. The present paper describes the experimental determination of the actual temperature distribution in a chip resistor assembly when it is powered. The paper also discusses the significance of such experimentally determined non-uniform temperature distributions in electronic assemblies to fatigue damage accumulation due to both power cycling and to cyclic variations in the ambient temperature whilst the chip resistor is powered. This fatigue damage accumulation study is carried out using finite element analysis.

Introduction

The primary functions of solder joints in electronic assemblies are to achieve electrical connectivity and structural integrity, but structural integrity is a requirement for conductivity. The functional reliability of electronic products therefore depends on the structural reliability of the solder joints. Due to the ban imposed on use of SnPb solders in many electronic applications, most manufacturers have been forced to adopt lead-free solders. Eutectic and near eutectic SnAgCu solders have been widely adopted as replacements for the well established SnPb based solders. Any lead-free solder must have its reliability studied in the anticipated operational conditions before implementation in electronic products.

In typical applications, solder joints form a bridge between a substrate and the components. The difference in coefficient of thermal expansion (CTE) between the substrate and component may cause significant thermal stresses during operation. For the reliable functioning of electronic products, solder joints must accommodate the thermal strains caused in operation due to the mismatch in CTEs. The ability of solder to withstand considerable fatigue damage is critical for the reliable functioning of electronic products. Stronger solder materials that could resist these thermal stresses without fatigue damage could result in an unacceptable change in the failure mode, with failures occurring in the component or substrate rather than in the solder [1]. The most commonly used solders in electronic applications are Sn based. These are prone to thermal fatigue damage because the thermal anisotropy of the β-Sn phase causes intergranular fatigue damage upon thermal loading [2, 3].

Solder joints are subjected to thermo-mechanical fatigue damage during operation with the fluctuation of local temperature. The repeated heating and cooling of electronic devices induces cyclic strain in the solder joint resulting from the CTE mismatch between component and substrate. The operating temperature may vary between extremes as wide as 218K to 398K, depending on the application in which the electronic device is being used. This means typical lead-free solder joints, with melting points of around 217^{o}C (490K), operate at homologous temperatures (T_h) of between 0.45 and 0.81, which is sufficient for rapid creep deformation to occur under moderate loads. Hence, studies of the fatigue damage in solders must consider creep behaviour. Experimental methods such as shear or mechanical shock tests which may be used for solder joint bond strength determination do not provide any information about their fatigue behaviour. Hence, thermal cycling tests are commonly used to determine the fatigue damage due to cyclic variations in temperature, but it is laborious and time-consuming. Therefore, finite element analysis has been employed in recent years to simulate the damage phenomenon with consideration of different field operating conditions. However, most of the reported finite element simulations of thermal fatigue damage in solders have been carried out considering thermal cycling, which is application of a changing, but uniform temperature distribution across the electronic assembly, which is contrary to the actual temperature distribution [4, 5]. In applications such as automotive, aerospace etc., the ambient temperature can vary significantly when the electronic devices are in operation. This type of situation is very difficult to include in accelerated life testing to understand its influence on the fatigue damage. However, in finite element analysis such varying operating conditions can be readily included.

In this paper, the temperature distribution in a chip resistor assembly is determined using infrared thermography. These temperature distributions are then used as boundary conditions in a finite element creep analysis to replicate the infield thermal conditions during power cycling. A comparison of the resulting creep damage is made between application of a uniform and non-uniform temperature distribution within the chip resistor. Finite element analysis is also carried out for cyclic variations of ambient temperature with the chip resistor continuously powered.

Experimental Work

Procedure

Infrared (IR) thermography was used to determine the temperature profile in a typical chip resistor for power cycling. A schematic diagram of the temperature measurement set up is shown in Fig. 1. The experimental set up consists of a Thermosensorik camera, a 1206 chip resistor assembled on to a FR4 substrate, and a power supply. The details and background on these thermography experiments are given in [6].

Figure 2 shows the construction of the chip resistor used in the experiment. The chip resistor consists of an alumina substrate on which a thick film resistive element is printed. The thick resistive element is covered with a polymer resin based protective coating. The alumina substrate is covered with a solderable electrode termination at the ends. The chip resistor is mounted on a 1.6 mm thick FR4 substrate which has 35µm thick copper tracks used for powering the chip resistor. The 1206 chip resistor is rated to operate in the temperature range between 218K and 428K with a maximum power dissipation of 0.25W up to an ambient temperature of 343K, reducing to 0W at 428K. The resistor is reflow soldered to the copper tracks using Sn3.8Ag0.7Cu (SAC) solder with a melting point of 490K. The resistor assembly was sprayed with a thin layer of a matt black paint to provide a uniform high emissivity temperature measurement surface. The experiment was carried out for two different loading conditions: (A) the full rated load (0.25W) and (B) a derated load (0.15W). The chip resistor was powered and, after the temperature distribution had stabilised, the temperature profile was captured with the IR camera.

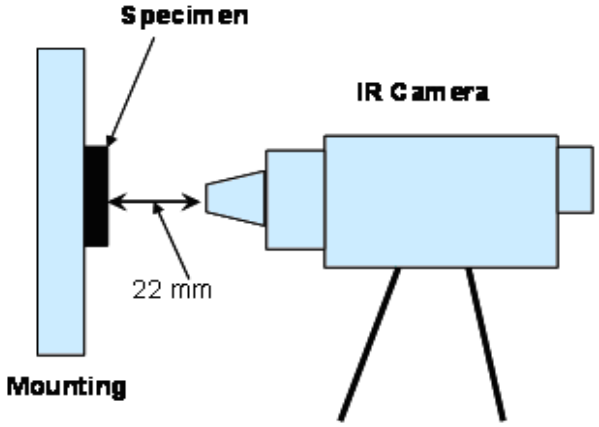


Fig. 1: Schematic diagram of experimental setup

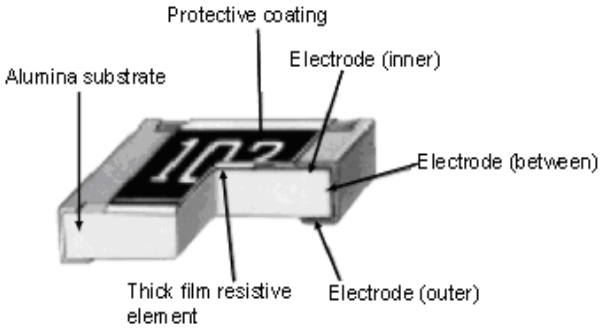


Fig. 2: Construction of a 1206 chip resistor [7]

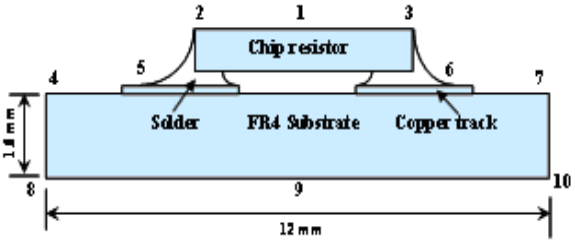
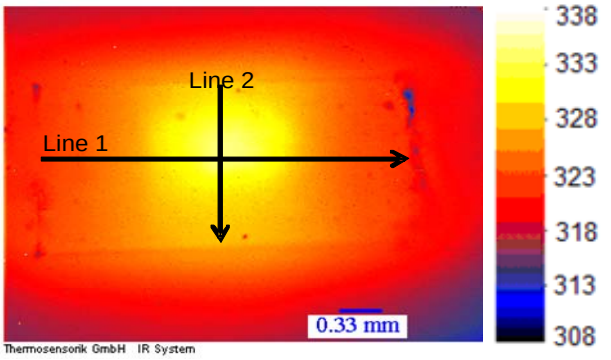


Fig. 3: Geometrical model of the chip resistor assembly

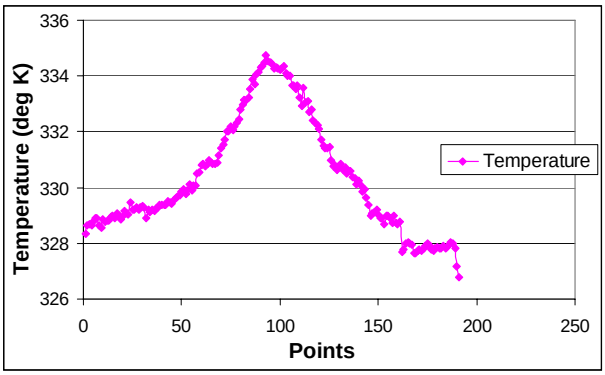
Results and Discussion

A. Full load (0.25W): The temperature distribution in the chip resistor at 0.25W is shown in Fig. 4(a). The maximum temperature of 334.5K was at the centre of the thick film resistive element, where the heat is generated, and decreased towards the boundaries of the chip. The temperature distribution was also evaluated across the length and width of the chip resistor. Figures 4(b) and (c) show the variation of temperature along lines 1 and line 2. The temperature distribution along line 1 is symmetrical, while that of line 2 is skewed towards one side. Manufacturing deficiencies wherein the heat generating resistive element is skewed towards one side may be the reason for the asymmetrical temperature distribution along line 2.

The temperature distribution obtained using the IR camera was validated by comparison with temperature measurements from thermocouples bonded to the sample at the locations indicated in Fig.3 on the central line. Calibrated K-type thermocouples with a wire diameter of 40 µm were used and these thermocouples were connected to a digital thermometer. Table 1 presents a comparison of the temperatures at these locations. The temperatures pretty well match for both measurement methods with a maximum discrepancy of 1K. The temperature gradient, which is the difference between the maximum and minimum temperature, in the chip resistor assembly is calculated to be 22.5K for the full load condition.



(a)



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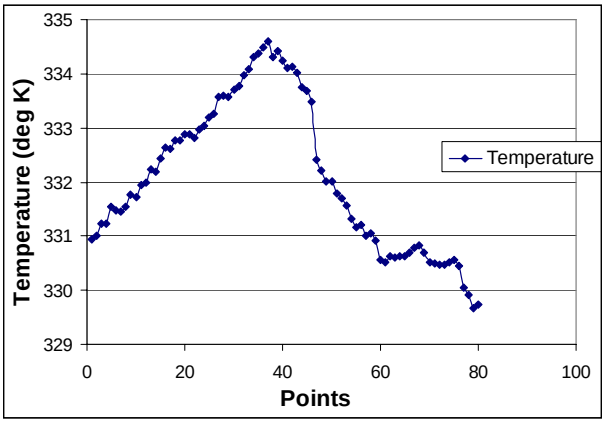


(c)

Fig. 4: Temperature distributions in the chip resistor: (a) over chip surface; (b) along line 1; (c) along line 2.

The full load experiment was repeated for a higher room temperature (297.5K) to understand its effect on the temperature gradient in the assembly. The temperature measurements for this condition are also shown in Table 1. The temperature distribution in the chip is similar to that observed at the lower room temperature (295K). The maximum temperatures in the chip increased marginally, while the temperature gradient in the assembly decreased by one degree. Again, the comparison of temperature between thermocouple and thermal camera measurement is good, with a maximum discrepancy of 3K at the chip centre. The drop in temperature gradient may not be significant; however, since the thermal strain in the solder joints is the direct effect of the temperature gradient in the assembly, and the temperature distribution at a room temperature of 295K was used in the subsequent finite element analysis.

Table 1 Measured temperature using thermocouples and thermal camera at full load (0.25W)

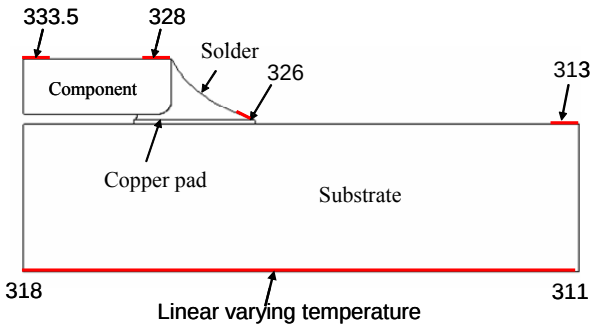
Location (Fig. 3)	Room Temperature 295K		Room Temperature 297.5K	
	Thermo-couple	Thermal Camera	Thermo-couple	Thermal Camera
1	333.5	334.5	335.5	338.5
2	329.0	328.0	330.0	328.0
3	327.0	327.0	329.5	326.0
4	312.0	311.0	317.5	316.5
5	326.0		328.0	
6	325.0		327.0	
7	312.0	311.0	317.0	316.0
8	311.0		314.0	
9	318.0		319.0	
10	311.0		314.0	

Thermal Finite Element Analysis

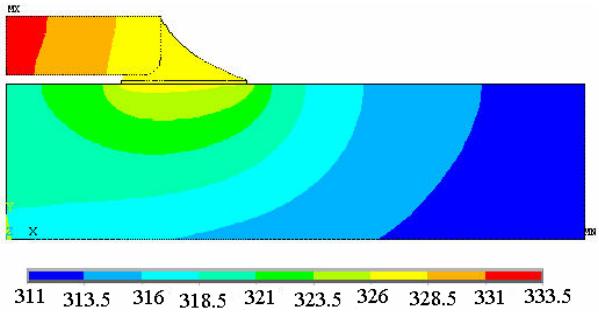
A 2D finite element thermal analysis was carried out, using the experimentally determined temperature distribution in the chip resistor as the boundary conditions, to obtain the full temperature distribution for use in the following creep analysis. Figure 5 (a) shows the temperature boundary conditions used at different locations on the assembly for thermal analysis. The locations of the boundary conditions are similar to those used for temperature measurement comparison. The symmetry plane is considered to be an adiabatic surface, i.e. without any temperature boundary conditions applied to it. A linearly varying temperature is applied only on the bottom surface of the substrate to replicate the experimental temperature distribution in the assembly. Material properties used for the thermal analysis are presented in Table 2. The obtained temperature distribution after thermal analysis is shown in Fig. 5(b).

Table 2 Material properties used in thermal analysis

Material	Density (gm/cm3)	Thermal conductivity (W/mK)
Alumina	3.97	25
Solder (SAC)	7.5	60.32
Copper	8.96	400
FR4	1.96	0.3



(a)

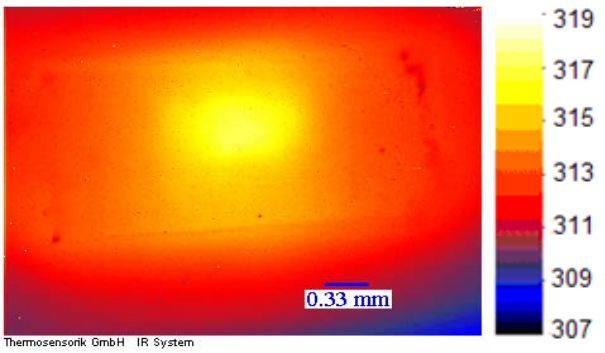


(b)

Fig. 5: Thermal analysis of chip resistor assembly at 0.25W: (a) temperature boundary conditions used; (b) predicted temperature distribution (K)

B. Derated load (0.15W): As the ambient temperature increases, the maximum allowable power dissipation in the chip resistor decreases. An experiment was carried out to establish the temperature distribution in the chip resistor while it is operating at an ambient temperature of 398K. At this temperature, the maximum load at which the 1206 chip resistor can be operated is 0.15W.

Figure 6(a) shows the temperature distribution in the chip resistor for the derated load of 0.15W, which resembles the temperature distribution for full load condition, but with a decrease in the magnitude of the temperature rise above ambient. The maximum temperature is again, as expected, observed at the centre of the chip and the variation of temperature along line 1 and line 2 is similar to that observed for full load. The thermal camera temperature measurements and those from the thermocouples again match very closely, as shown in Table 3. The temperature gradient observed in the assembly is 12.5K, which is proportional to the decrease in power input to the specimen.



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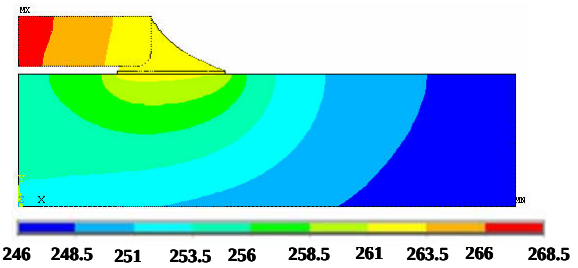

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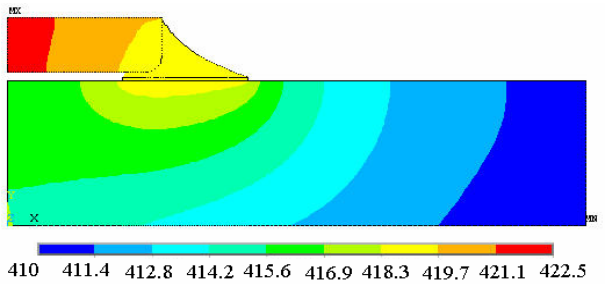


(c)

Fig. 6: Temperature distribution at 0.15W: (a) measured over chip surface (b) predicted for an ambient temperature of 218K; (c) predicted for an ambient temperature of 398K (K)

The thermal analysis was repeated for ambient temperatures of 218K and 398K, using both the full and derated load temperature distribution as boundary conditions respectively. This was carried out to establish the full temperature distribution in the assembly for continuously heat dissipating chip resistor with varying ambient temperatures between 218K and 398K. The locations (Fig. 5(a)) of the thermal boundary conditions are the same as used for the full load condition. Figures 6 (b) and (c) show the temperature distribution obtained after thermal analysis respectively for ambient temperatures of 218K and 398K, and these temperature profiles are later used in the cyclic creep analysis for variation of the ambient temperature between 218K and 398K with the chip resistor powered.

Table 3 Measured temperatures from thermocouples and thermal camera for derated load (0.15W)

Location (Fig. 3)	Room Temperature 295K	
	Thermo-couple	Thermal Camera
1	318.5	318.0
2	316.0	315.0
3	315.0	314.0
4	308.0	307.0
5	315.0	
6	314.0	
7	306.0	306.0
8	306.0	
9	312.0	
10	306.0	

Structural Finite Element Analysis

FE Model, Loads and Boundary Conditions

A 2D finite element (FE) model of the chip resistor assembly was built for the creep analysis. The FE modelling was done using plane strain elements, which have been shown to provide an accurate simulation of such chip resistor assemblies [9]. Only one-half of the geometry is considered in the finite element analysis, making use of the structure's symmetry. Figure 7 shows the quality of mesh used in the critical region of the solder joint of the chip assembly.

The majority of solder joints failures in electronic packaging are due to thermo-mechanical/creep fatigue. Therefore, only thermal loads are considered in the finite element analysis. The thermal history used in the power cycling simulation is detailed in Fig. 8. Creep analysis was carried out for three thermal loads:

Case 1: Non-uniform temperature distribution (Fig. 5(b)) in the chip resistor assembly at hot dwell (line DE in Fig. 8), which represent the power cycling simulation.

Case 2: Uniform temperature distribution in the chip assembly at hot dwell (DE) of the thermal history with the maximum temperature of 333.5K taken from the full load thermal simulation at room temperature. This represents the thermal cycling simulation.

Case 3: For the finite element creep analysis including cyclic variation of the ambient temperature with a continuously heat dissipating chip, the chip resistor assembly is cycled between the temperature profile obtained for ambient temperature 398K at hot dwell (line DE in Fig. 8) and 218K at cold dwell (line FG in Fig. 8).

A symmetry boundary condition is used to represent the structural symmetry of the assembly and to prevent rigid body motion in the X-direction. The lowest node on the symmetry plane is also constrained in the Y-direction to prevent rigid body motion.

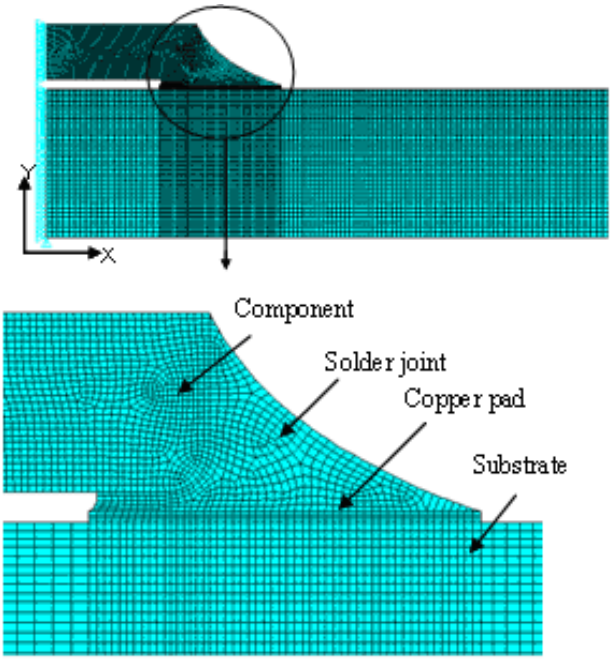


Fig. 7: Finite Element Model of 1206 resistor

Material Properties

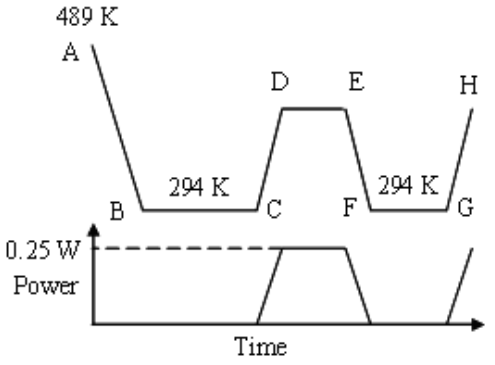
The finite element model consists of a component, solder joint, copper pad and substrate, which are modelled using published material properties for alumina, Sn3.8Ag0.7Cu, copper and FR4 respectively [8,9]. Since many material properties vary significantly with temperature, temperature-dependent material properties are used in the analysis. Most materials undergo rapid creep deformation at temperatures above $0.4T_h$. The solder, but none of the other materials in the assembly, operate well above 0.4Th ($0.55T_h$ and $0.68T_h$), therefore, a creep material model is introduced for the solder joint to capture the effect of creep and therefore allow estimation of fatigue damage during power cycling. Material properties for the SnAgCu solder joint are presented in Table 4 and a bilinear kinematic hardening (BKIN) material model is used for elasto-plastic modelling of the solder joint, which includes the Bauschinger effect due to cyclic loading. To reduce the model complexity and analysis time, only the solder joint is modelled using this elasto-plastic material model. The steady state creep behaviour of the SAC solder joint is modelled using the sine hyperbolic law:

$$\dot{\varepsilon}_{cr} = A[\sinh(\alpha\sigma)]^n \exp\left[\frac{-H}{RT}\right], \qquad (1)$$

where A = 277984, α = 0.02447, n = 6.41, H/R = 6500. $\dot{\varepsilon}_{cr}$ is a steady state-creep strain rate, σ is stress, T is absolute temperature [11].

Table 4 Material properties for SAC solder [8, 10]

Temperature (K)	Young's modulus (MPa)	CTE (ppm/K)	Yield Stress (MPa)	Tangent modulus (MPa)
298	32331	21.2	38	154
348	8285	21.7	30	134
423	6517	23.0	17	132



Cooling from 489 K (AB) = 48 sec

Dwell at room temperature (BC) = 3600 sec

Ramp DC = 300 sec

Ramp EF & GH = 360 sec

Hot & Cold dwell (DE, FG) = 300sec

Hot dwell peak temperature (DE) = 333.5 K

Temperature range = 39.5 K

Fig 8 Thermal history and power dissipation creep simulation

Results and Discussion

Case 1 & 2: This study is an extension to the work published in [8], where the same chip resistor assembly was cycled for five power cycles. The previous analysis work was performed with a similar set of boundary conditions, thermal history and material properties, but the stress-strain hysteresis loop had not stabilised after 5 power cycles resulting in a different strain range for each of the power cycles. Hence, the power cycling was continued for 10 cycles in this creep analysis. Since the solder joint is the main region of interest, a detailed study of stress and strain variation is carried out for the fillet of the solder joint, which is the location of both the maximum stress and strain.

The distribution of shear stress in the solder joint at the start of the hot dwell (point D in Fig. 8) and cold dwell (point F in Fig. 8) is shown in Fig. 9. It is clear from the stress distribution that both the thermal histories (Cases 1 & 2) predict similar stress variations in the solder joint. Evolution of shear stress in the solder joint is also studied and shown in Fig. 10. The figure shows the stress evolution for reflow, dwell at room temperature and two power cycles. Even though ten power cycles are simulated, the shear stress variation is shown only for two power cycles, since the stress cycle repeats for subsequent cycles due to thermal ratcheting. Simulation of reflow shows the considerable amount of residual shear stress (24 MPa) in the solder joint after reflow soldering.

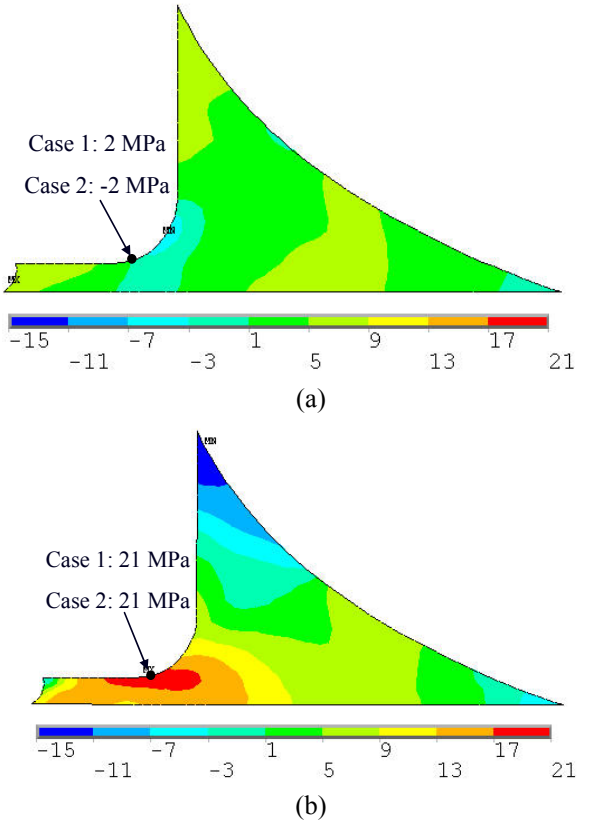


Fig. 9: Shear stress in solder joint: at point D (a) and F (b) of the thermal history (Fig. 9)

An hour dwell at room temperature, before the assembly is cycled, results in relaxation of the residual stress (reduction from 24 MPa at the end of reflow to 12 MPa) induced during manufacturing of the assembly. The maximum shear stress in each power cycle did not exceed the initial residual stress of 24 MPa, which indicates that stress levels induced in the solder joint during power cycling are within the new yield stress. The shear stress range was also studied and remained constant (24 MPa for Case 1 and 26 MPa for Case 2) over the power cycle, which is also evident from the stress evolution shown in Fig. 10.

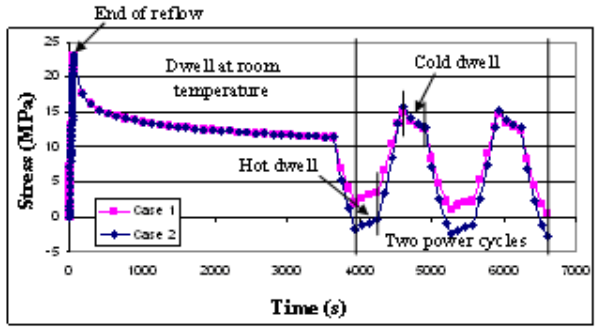


Fig. 10: Evolution of shear stress in the solder joint

The fatigue damage in the solder joint is studied by considering the inelastic strain accumulation during creep analysis. Figure 11 shows the accumulation of inelastic strain due to creep after reflow, dwell at room temperature and ten power cycles. The strain accumulation increases with time and Case 2 has a higher accumulation than Case 1. The difference in the inelastic strain accumulation at the end of ten power cycles is 5%.

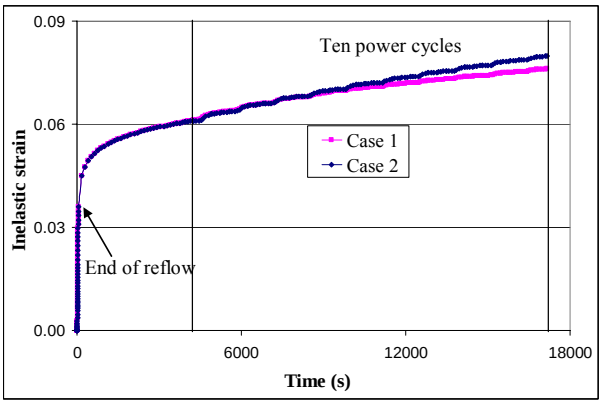


Fig. 11: Evolution of inelastic strain in solder joint

In fatigue life calculations using the strain based Coffin-Manson method, the inelastic strain range for a stabilised thermal/power cycle is used. Hence, the inelastic strain range for every power cycle is analysed. Table 5 shows the calculated inelastic strain range over each power cycle for both of the thermal histories (Cases 1 & 2). This shows an initial decrease in strain range as each cycle progresses, but unlike the authors previously reported creep study [9], the strain range reaches a constant value after the 9th power cycle, which shows the stabilisation of stress-strain hysteresis. Comparison of the inelastic strain range between cases 1 & 2 shows the importance of a non-uniform temperature distribution in the chip assembly. The uniform thermal history (Case 2) always shows a higher strain range than the non-uniform thermal history (Case 1). An inelastic strain range difference of 50% is observed at the end of the cycle stabilisation. This difference has a direct implication for the fatigue life on the solder joint.

Table 5 Inelastic strain range for power cycles

Power cycle	Inelastic strain range		% variation
	Case 1	Case 2	
1	0.0028	0.0028	0
2	0.0022	0.0024	9
3	0.0019	0.0022	16
4	0.0016	0.0020	25
5	0.0013	0.0019	46
6	0.0012	0.0018	50
7	0.0011	0.0017	42
8	0.0011	0.0016	45
9	0.0010	0.0015	50
10	0.0010	0.0015	50

Case 3: Finite element creep simulations were also carried out for powered chip resistor within an ambient temperature varying between 218K and 398K. The simulations were carried out for ten cycles and the shear stress variation is shown in Fig. 12. The shear stress distribution in the solder joint is similar to that in Fig. 9, but with slightly higher magnitude due to the higher thermal load. The stress variations were similar to Case 2 of power cycling, but also with increased magnitude.

The shear stress range and inelastic strain range for this simulation is tabulated in Table 6. The shear stress range is constant between cycles, which is similar to that for the Case 1 & 2 simulations. However, unlike the Case 1 & 2 simulations, the cyclic inelastic strain range increases initially and attains stabilisation earlier. The stabilised inelastic strain range is 38 and 25 fold higher than for Case 1 and Case 2 respectively, which is due to the higher range of cyclic temperature. This will greatly reduce the solder joint fatigue life.

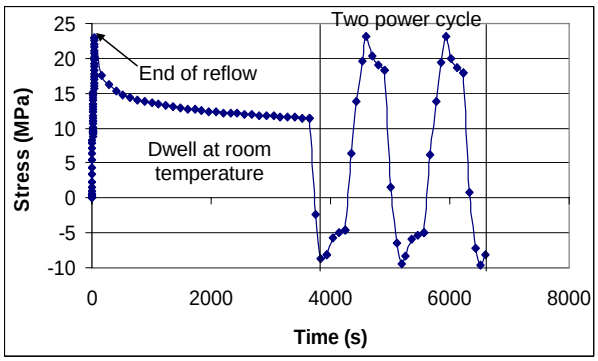


Fig. 12: Variation of maximum shear stress in the solder joint

Table 6 Inelastic strain range for cyclic variation of ambient temperature with chip resistor powered

Cycle	Shear stress range (MPa)	Inelastic strain range
1	32.6	0.0354
2	32.8	0.0363
3	32.9	0.0370
4	32.9	0.0375
5	32.9	0.0377
6	32.9	0.0379
7	32.8	0.0380
8	32.8	0.0380
9	32.8	0.0380
10	32.8	0.0380

Fatigue Life Estimation

The fatigue life for the solder joint was calculated based on the stabilised inelastic strain range. The commonly used Coffin-Manson relationship was used for the life estimation [11]:

$$N_f = (C'\varepsilon_{in})^{-1}, \quad (2)$$

where, N_f is the number of cycles to failure (fatigue life), C' is a constant, and ε_{in} is the accumulated inelastic strain range for a stabilised power cycle. For this study the value of C' used was 0.0468 [11]. Table 7 presents the calculated cyclic strain ranges used in fatigue life calculations, along with the predicted life for both power cycling and cyclic variation of ambient temperature with the chip resistor powered. As expected, there is a 50% improvement in the fatigue life of the solder joint with Case 1 in comparison with Case 2. However, in the case of cyclic variation of ambient temperatures, the fatigue life decreased drastically due to the higher level of stabilised cyclic inelastic strain.

Table 7 Predicted fatigue for solder joint

Thermal history		Inelastic strain range	Predicted fatigue life (cycles)
Power cycling	Case 1	0.0010	21367
	Case 2	0.0015	14245
Cyclic variation of ambient temperature		0.038	562

Conclusions

1. The experimental study shows that the temperature distribution in a powered electronic assembly is non-uniform, and consideration of a uniform temperature distribution for finite element analysis would result in an over estimation of the fatigue damage in the solder joints.
2. The creep study shows that the considerable amount of residual stress is induced in the solder joint by the reflow process but decays with dwell at room temperature. The stress cycle repeats with the subsequent power cycle because of thermal ratcheting.
3. The number of cycles before stabilisation of the stress-strain hysteresis loop in the power cycling analysis was 9, while for cyclic variation of ambient temperature analysis it was 7. This shows that the results of any simulations must be assessed on a case by case basis to ensure stabilisation has occurred.
4. Application of a non-uniform temperature distribution during the creep analysis results in a lower strain accumulation and a significant 50% difference in stabilized inelastic strain range has similar implication on the fatigue life calculation.
5. Creep analysis for cyclic ambient temperature variation significantly increases the stabilised strain range, which in turn affected the solder joint fatigue life.

The present study was carried out using published material properties for bulk Sn3.8Ag0.7Cu solder. In a future study, experimentally obtained material properties for solder within a joint will be used for modelling of both elasto-plastic and creep behaviour.

References

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