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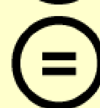

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FINITE ELEMENT ANALYSIS OF LEAD-FREE SURFACE MOUNT DEVICES

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Abstract

Transition to lead-free solder materials has raised concerns over the reliability of lead-free solder joints in the electronic industry. Solder joints provide electrical conduction and mechanical support for components and may operate over temperature extremes of -55°C to 125°C or greater. These temperatures are relatively high the melting point of the solder. A mismatch between coefficients of thermal expansion of the component, solder and substrate, combined with thermal variations during service, results in thermal fatigue that is a common failure mechanism for solder joints in electronic products. So far most of the studies of this issue have considered uniform temperature distributions in the electronic assembly. The main objective of this paper is to investigate the effect of the experimentally observed non-uniform temperature distribution in the electronic device on the structural response of solder joints in comparison with that for a uniform temperature distribution.

Keywords: Solder joint, lead-free, thermo-mechanical fatigue.

1. Introduction

Over many decades SnPb solder has been successfully used by the electronic industry. However, the recent ban imposed on the use of lead in electronic devices has raised reliability concerns due to the introduction of considerably less studied lead-free solders. Thermal stresses occur in a structure when any portion of thermal expansion or contraction is

constrained. Basically, there are two different sets of constraints, under which thermal stresses occur: external and internal [1]. Thermal stresses due to external constraints are obvious. However, the notion of internal constraints is less clear. A structure made of the material may be free to expand and yet have thermal stresses due to a non-uniform temperature distribution. On the other hand, a structure comprising components of different materials can demonstrate thermal stresses even in the case of uniform thermal conditions and absence of external constraints due to the difference in levels of coefficients of thermal expansion (CTEs). Usually electronic assemblies are manufactured from a range of materials with varying CTEs [2]. Since these assemblies experience temperature/power changes during their use (e.g. power consumption; switching equipment on/off; day/night temperature changes), the CTEs mismatch causes stresses in the assembly, which may then result in creep and stress relaxation with time.

The principle reliability hazard for surface mounting technology in microelectronics is fatigue cracking of the solder joints, caused by cyclic thermal stresses. Figure 1 demonstrates a crack in a solder fillet caused by thermal cycling. Under service conditions, these devices may be subjected to a cyclic temperature range from -55°C to 125°C or more depending on their application. Under such cyclic thermal loading, stresses due to the thermal-expansion mismatches are difficult to avoid. Even with matched levels of CTEs there is a possibility for stress initiation in the package due to the spatial temperature variations in the assembly. In many designs the imposed stresses exceed the elastic limit of the solder and produce plastic deformation. Under these conditions eventual failure by low cycle fatigue can be expected. The fatigue lifetime, which is required in service, typically considerably exceeds the duration of reliability tests. This means that service reliability must be estimated using some sort of extrapolation. The situation becomes complex because of the relatively high temperatures involved. Low cycle fatigue at more than half the melting point

of the solder will involve creep-fatigue interactions. Under these conditions, the number of cycles to failure depends on the cycle frequency and on the shape of a stress cycle [3].

Experimental evaluation of fatigue life consumes a considerable amount of time and is also expensive. Therefore, finite element analysis plays an important role in estimation of durability of solder joints. Within the framework of this approach a mathematical model is built, which incorporates both the constitutive equations and the actual geometry and different loading conditions can be simulated. So far, most of the finite element analyses in electronic assemblies have been conducted considering the spatially uniform thermal cycling, e.g. finite element simulation study of 5 x 4 chip scale packages (CSP) and flip-chip solder joint reliability under isothermal cycling [4, 5]. In this paper the effect of non-uniform temperature distribution on the structural behaviour of solder joints in a surface mount device is studied and compared with that of uniform thermal cycling.

2. Experimental procedure

A series of experiments were carried out to acquire the temperature distribution in an electronic assembly for power cycling condition, using an infrared (IR) Thermosensorik camera. It measures thermal radiation from the surface, which has a wavelength spectrum dependent on the temperature, structure and composition of the surface. The higher the temperature, the more radiation is emitted. This infrared radiation, not perceptible with naked eye, is made visible and measurable by infrared cameras. Analysing the infrared radiation it is possible to measure temperature as well as thermal conductivity, mechanical stress, material composition, defects and various kinds of inhomogeneities in the materials. IR-measuring technology is contactless and non-destructive and supplies information with a spatial and temporal resolution that is not achievable with other measuring techniques.

The Thermosensorik IR camera consists of a central processing unit with software

and an IR detector head with a focal plane array (FPA) detector sensitive in the range 1 μm – 14 μm. An infrared microscopic lens MWIR 2.5X, with a focus distance of 21-22 mm was used for this experiment. The camera is interfaced with software to control real-time acquisition and analysis of the infrared data.

The specimens used were identical flip chip assemblies attached to either a copper or FR4 substrate. They were placed in a wind tunnel where they were subjected to either 0.4 W or 1.2 W power levels. They were also cooled by either free or forced convection (airflow rates of 5, 10 and 15 m/s were used)

2.1 Specimen description

The flip chip specimens were silicon-on-silicon multi-chip modules (MCMs) that matched the description of those used in a previous experiment [7]. Both MCMs consisted of a 3 mm x 3 mm x 0.5 mm *"heater"* chip that bore a large central resistive element (the heater) in addition to small aluminium tracks and 36 connection pads. The *"carrier"* chip was larger at 6 mm x 6 mm x 0.5 mm that included larger ball grid array pads allowing for external connections to be made, as well as the corresponding pads to match those on the heater chip. The heater chip was attached to the carrier chip so that a standoff height of 35 μm was achieved (without underfill). The MCMs were subsequently attached to the corresponding substrate by a thermally conductive adhesive pad. A schematic of the assembled specimen is shown in Fig. 2.

2.2 Experimental set up

The experimental setup consists of a thermal camera, fitted with the micro lens, is mounted on the tripod, the specimen is powered on for a few minutes to stabilise the temperature distribution in the specimen, then micro lens is focused on the specimen and the temperature profile is captured.

2.3 Results and discussion

Free convection

The temperature distributions over the chip for 1.2 W power cycles are given in Figs. 3 and 4 for free convection; the path, which is used for temperature distribution analysis, is also shown. These figures demonstrate the effect of the substrate on temperature distributions in the chip: the copper substrate causes lower temperatures compared to the FR4 substrate.

Figure 5 shows the temperature distribution cross the width of the chip for both types of substrate. It is evident that these temperature distributions are non-uniform: the maximum temperature is observed at the centre of the chip, where there is a lower thermal mass, while its boundary has lower temperature. Another important result of this analysis is that the FR4 substrate induces higher thermal gradients in the chip than copper substrate. This can be explained by higher thermal conductivity of copper than FR4.

Forced convection

Figures 6 and 7 show temperature distributions in the chip for copper and FR4 substrates respectively, under forced convection 5 m/s. Forced convection can be seen to reduce the temperatures in the chip by increasing the heat transfer rate. Similar experiments were carried out for forced convection at levels of 10 m/s and 15 m/s.

So, the experiments vividly show that the temperature distribution in a power dissipating electronic assembly is non-uniform. They justify the necessity to study the structural response of solder joints and assemblies for cases where there is a non-uniform temperature distribution. Even though the experiments are carried out only for flip chip specimens, similar temperature distributions can be expected to occur in assemblies manufactured using other packaging techniques (BGA, SMT etc.) due to the comparable thermal mass distribution (more thermal mass at the boundary than the centre of the chip). The thermal data, used below in finite element simulations of surface mount resistor, is based

on these experiments.

3. Finite element analysis

Geometry

The reliability of surface mounted devices (SMDs) has been extensively analysed by means of finite element simulations. Surface mounting is the technique of attaching components directly to a substrate without the through-hole leads of a more conventional technology. The origins of this technique have been traced to 1952, but it is only in recent years that advances in robotics have allowed mass production, based on it [8]. The geometry of a 1206 resistor has been here used to study the effect of non-uniform temperature distributions on the structural response. The geometric dimensions of different components of this resistor assembly are shown in Fig. 10. In this finite element study only one half of the resistor assembly is modelled thanks to its symmetry.

The commercial FEA software ANSYS was used for both finite element modeling and analysis. A 2D model was built using PLANE 182 element type, which is a 2D plane stress with thickness element. A 3D finite element model with hexahedral elements was also used in simulation to study specific feature of a 3D stress distribution. A fine mesh pattern is maintained in and around the solder joint - a critical area - to accurately capture variations in the stress level. Finite element models with detailed views of the critical area are presented in Figs. 11 and 12.

Material properties

Temperature-dependent material properties are used in the FEA. The component is modelled with properties of alumina (Al_2O_3), while the material data given in Table 1 for as-cast SnAgCu is used for solder joint, and high-conductivity copper is considered for the pad. The data for FR4 substrate is taken from [9, 10]. The elasto-plastic analysis is carried out considering bilinear kinematic hardening (BKIN) model, which includes the Bauschinger

effect due to thermal cycling.

Loads and boundary conditions

Since most chip resistors fail due to thermo-mechanical fatigue, only a thermal load is considered for FEA. The FE study was carried out considering three different thermal loading conditions in two steps. In the first step, elastic analysis was carried out to identify the limiting temperature at which stress levels in solder joint reach the yield limit. Secondly, an elasto-plastic analysis was performed to estimate the residual stress induced in the solder joint during cooling from reflow soldering temperature as well as inelastic strains due to thermal cycling, and to compare stresses and plastic strains for three different types of thermal cycling. The following three cases of thermal loads were used:

Case A: Uniform temperatures ranging from +125°C to -55°C, where the entire resistor assembly is subjected to the same temperature.

Case B: Uniform temperature for the component, solder joint and copper pad ranges from +125°C to -55°C, and the substrate's temperature (T_{sub}) varies according to the following relation:

$$T_{sub} = 0.18*T_{comp} + 26.371, \quad (1)$$

where T_{comp} is the component's temperature.

The substrate material is FR4, and Eq. (1) for temperature on the substrate is derived from the experimental data, described in the previous Section.

Case C: In this case the temperature gradient in the whole assembly is considered. The gradient is obtained from the thermal analysis, for which temperature boundary conditions

are derived from the experimental data. The following thermal boundary conditions are used for different zones, as shown in Figure 13, for this thermal analysis:

Zone 1: The temperature varies from +125°C to -55°C.

Zone 2: This temperature boundary condition depends on temperature in Zone 1 boundary condition. The respective relationship is derived based on the experimental results for a specimen with a FR4 substrate and free-convection condition.

$$T_2 = 0.87*T_1 + 4.7, \quad (2)$$

where, T_1 and T_2 are the temperatures of Zone 1 and Zone 2, respectively.

Zone 3: The temperature in this zone, which is in the substrate, varies according to Eq. (1).

The temperature gradient in the resistor depends on the temperature in Zone 1, which controls temperatures in Zone 2 and Zone 3. Thermal analysis is carried out for different temperature levels for Zone 1 to obtain the thermal data that is used in structural analysis. The thermal load history and time steps used in elasto-plastic analysis are shown in Fig. 14.

The symmetry boundary condition and single node constraint on the symmetry plane were used for restraining the rigid body motion in the X and Y directions, respectively.

4. Results and discussion

Elastic analysis

A purely elastic finite-element analysis was performed for a component under thermal loading in the range from +125°C to -55°C to understand the level of stress induced in the solder joint and to estimate the area of applicability of this type of analysis. Plots of the equivalent stresses are presented for only one temperature step. Figure 15 shows the distribution of equivalent stresses in the solder joint for three different thermal load cases when the component's temperature is +125°C. It is evident that Case C results in lower stress

levels than the other two cases. The difference in the maximum equivalent stress between cases B and C is significantly higher than that between cases A and C. Also there is a shift in the maximum stress location from case A to cases B and C. Similar observations are drawn for the case T_{comp} = -55°C. The variation of the equivalent stress in the solder joint with temperature is studied for a single node (Node 551, Fig. 16(a)), located at the point with the maximum equivalent stress in case A. The obtained results (Fig. 16(b)) obviously demonstrate that the thermal load of Case C induces lower stresses in the solder joint compared to other two cases, with Case A resulting in the highest stress. The reason for this is that, in Case A the whole assembly is subjected to the same temperature leading to its higher global deformation. On the other hand, case B and case C have lower global deformation due to a low substrate temperature and temperature gradient, respectively. The maximum equivalent stress is observed in the solder joint, when the component is at +125°C for all three cases. The yield stress line for the solder (denoted YS in Fig. 16(b)) is used to find out the limiting temperature of the onset of plastic flow in the solder joint. In Case A 45°C and -25°C are limiting temperatures, while for cases B and C it is 50°C.

Elasto-plastic analysis

From this elastic stress analysis it is evident that thermally induced stresses in the solder joint exceed the elastic limit after a certain temperature excursion and confirms that a non-linear analysis is required. Before subjecting the resistor assembly to thermal cycling, the reflow process was simulated in order to determine the level of residual stresses induced in the solder joint by it. These manufacturing-induced stresses were then used as the initial stress state for the resistor assembly when subjected to two thermal cycles to study the evolution of plastic strains in the solder for the three different thermal load cases.

Figure 17 shows the predicted distribution of residual equivalent stresses in the solder

joint after cooling from the reflow temperature (217°C, i.e. melting point of the solder) for both 2D and 3D elasto-plastic analysis. The solder fillet, area of stress concentration, is the location of the maximum residual stress. From comparison of these two elasto-plastic analyses, a location of the maximum equivalent stress is found to be the same but the obtained magnitude in the 3D analysis is 20% higher than that in the 2D stress analysis. Distributions of the maximum and minimum principal stresses are shown in Figs. 18 and 19, the maximum principal stress is dominant in the location of maximum equivalent stress. A comparison of the equivalent stress in cases of 2D and 3D simulations is performed for the entire thermal cycling with Case A thermal loading. Figure 20 shows the variation for 2D and 3D stress for reflow and subsequent thermal cycles at the maximum residual stress's location. The equivalent stress variation is similar for both 2D and 3D analysis, with the difference in magnitude between them up to 8%. This study indicates that 2D finite element model provides a good approximation for the elasto-plastic analysis. Therefore, the 2D finite element model was used for remaining two thermal loading cases.

The reflow process also results in very high plastic deformation in the solder joint. The structural response of the solder joint to successive thermal cycles is presented in Fig. 21. The obtained results indicate that the stress and strain ranges are constant for conditions of purely thermal cycling. In Case A the maximum stress range per cycle is induced, compared to the other two cases, while case B results in the minimum stress range, which is about 6.4 and 2.5 times smaller than that of Case A and C respectively. Similarly, the elastic strain range per cycle is maximal for Case A and minimal for Case B. However, the range of equivalent plastic strain is quite different: their variations for Case A are similar to those of the equivalent stress/elastic strain and repeat with every thermal cycle. On the other hand, the levels of equivalent plastic strain for Cases B and C remain constant as, indicated in Fig. 21(c). Unlike Case A, Cases B and C show the increase in the equivalent plastic strain

despite the decrease in the stress level from residual stress state at the early stage of the first thermal cycle. This is due to the drastic decrease in the yield stress under heating from room temperature to +125°C. It is obvious that the thermal loads of Case A and C lead to maximum and minimum equivalent plastic strain in the solder joint. There is 8 and 16 percent decrease in the maximum plastic strain attained in thermal load Case B and C, respectively, compared to Case A.

5. Conclusions

This finite element study of a surface mount resistor under non-uniform temperature loads allows us to draw the following conclusions:

1. Elastic and elasto-plastic finite-element studies show that the non-uniform temperature distribution in the electronic assembly causes different responses of the solder joint to thermal cycling.
2. From the three studied cases, Case C (non-uniform thermal loads in the assembly) predicts lower plastic strain compared to other cases.
3. It is clear from results of the elasto-plastic analysis that stress/strain range is constant for thermal cycling between +125°C and -55°C. The further analysis should incorporate the relaxational effects as well as possible deterioration of material properties due to damage accumulation.
4. The solder joint has internal residual stresses along with high plastic deformation due to reflow soldering before the start of a thermal cycling. Since solder alloys generally operate at higher homologous temperature, the future work will include the effect of viscous behaviour on solder joints during reflow as well as thermal and power cycling.

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Figure Captions

Figure 1: Solder fillet cracking in -55 to +125°C test on 1812 size ceramic capacitors

Figure 2: Schematic of the flip chip specimens used

Figure 3: Temperature distribution in chip with copper substrate for power cycle 1.2 W

Figure 4: Temperature distribution in chip with FR4 substrate for power cycle 1.2 W

Figure 5: Effect of substrate on temperature distribution in the chip for free convection

Figure 6: Temperature distribution in chip with copper substrate for power cycle 1.2 W and forced convection 5 m/s

Figure 7: Temperature distribution in chip with FR4 substrate for power cycle 1.2 W and forced convection 5 m/s

Figure 8: Temperature distributions in chip with copper substrate for free and forced convection

Figure 9: Temperature distributions in chip with FR4 substrate for free and forced convection

Figure 10: Geometry of 1206 surface mount resistor

Figure 11: 2D finite-element model of a 1206 resistor assembly

Figure 12: 3D finite-element model of a 1206 resistor assembly

Figure 13: Thermal zones of 1206 resistor

Figure 14: Thermal load history and time step

Figure 15: Equivalent stresses (MPa) in solder joint (T_{comp} =125°C)

Figure 16: Location of Node 551 (a) and evolution of equivalent stress with in this node (b)

Figure 17: Residual equivqlent stress (MPa) in solder joint after reflow: (a) 2D simulations, (b) 3D simulations

Figure 18: Residual maximum principal stress (MPa) in solder joint after reflow: (a) 2D simulations, (b) 3D simulations

Figure 19: Residual minimum principal stress (MPa) in solder joint after reflow: (a) 2D

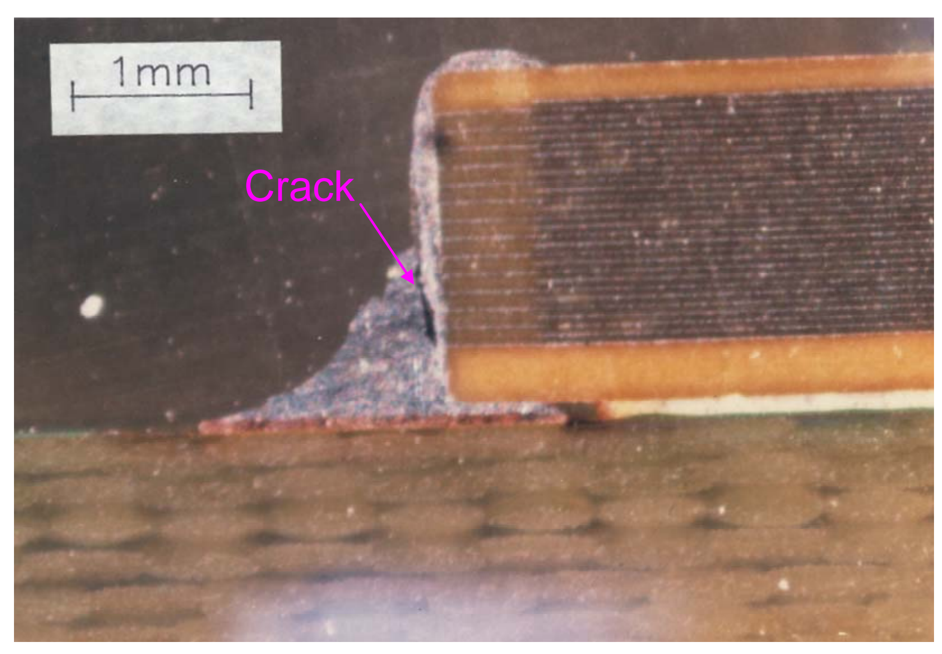
simulations, (b) 3D simulations

Figure 20: Comparison of evolution of equivalent stress between 2D and 3D stress analysis

Figure 21: Evolution of equivalent stress (a), equivalent elastic strain (b) and equivalent plastic strain (c) with thermal cycling

Table 1: Material properties of SnAgCu

Temperature (^oC)	Young's Modulus (MPa)	Yield Stress (MPa)	Hardening Modulus (MPa)	Poisson's ratio	CTE (ppm/^oC)	Density (gm/cm^3)
-50	57300	45	5650	0.4	12.7	7.5
-25	55800	41	5400	0.4	12.7	7.5
25	52600	32	5200	0.4	21.2	7.5
75	49300	21	4800	0.4	21.7	7.5
125	45800	13	4450	0.4	23.0	7.5



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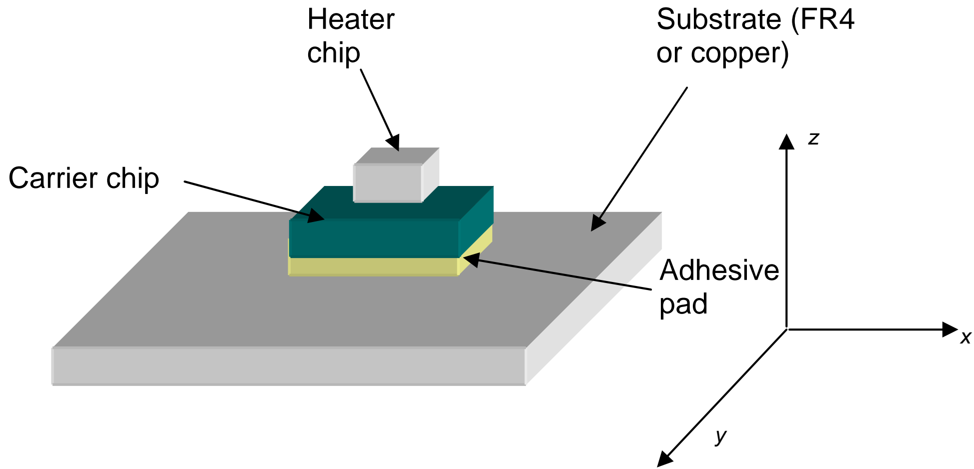

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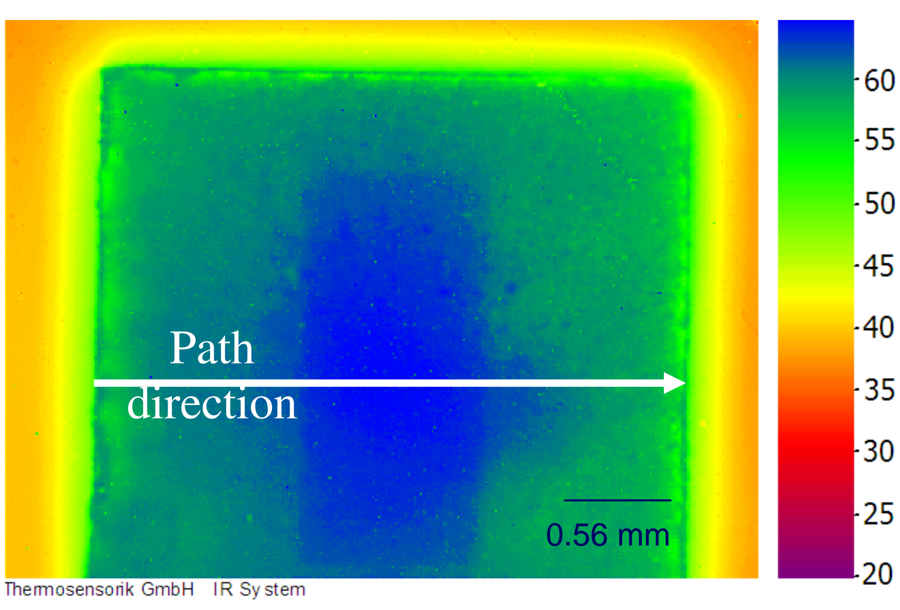

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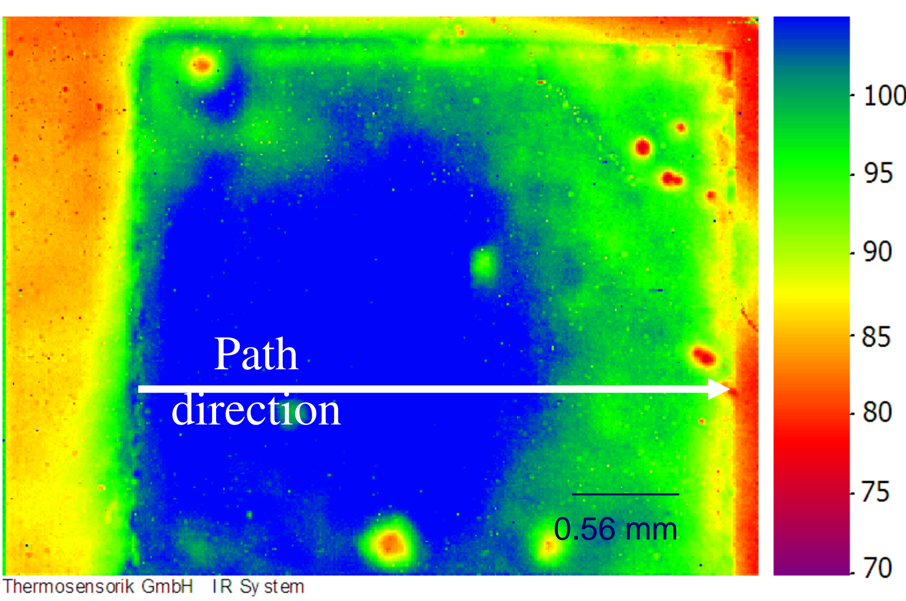

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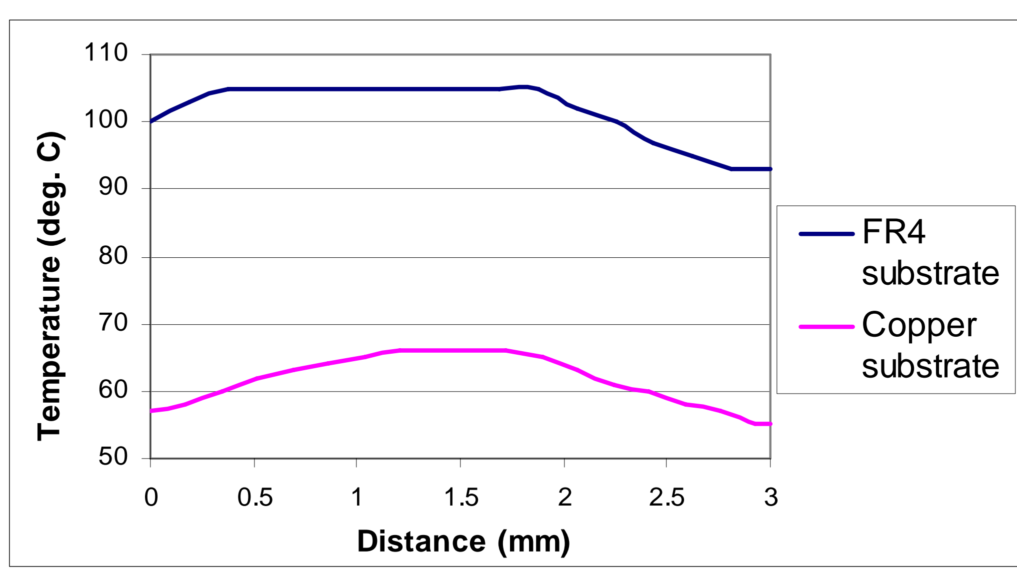

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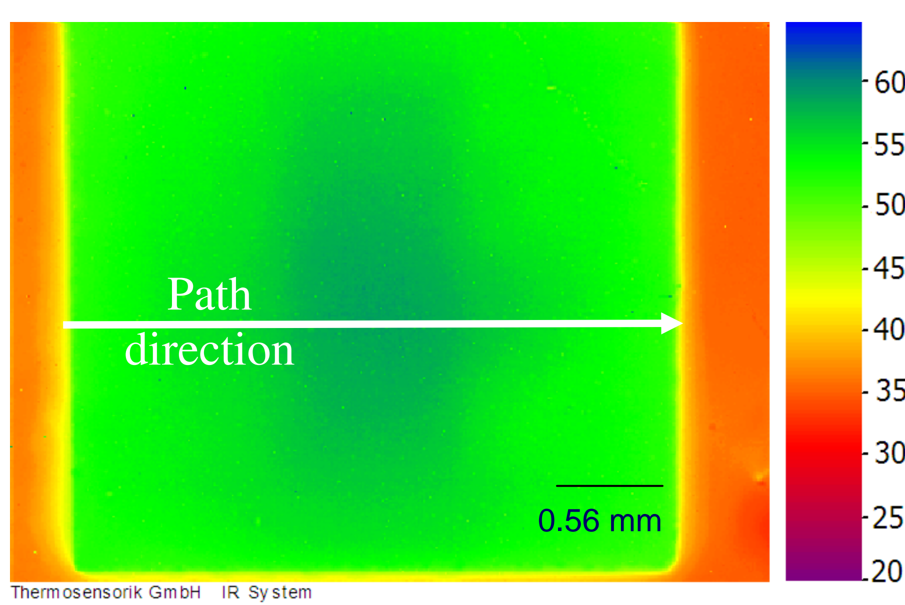

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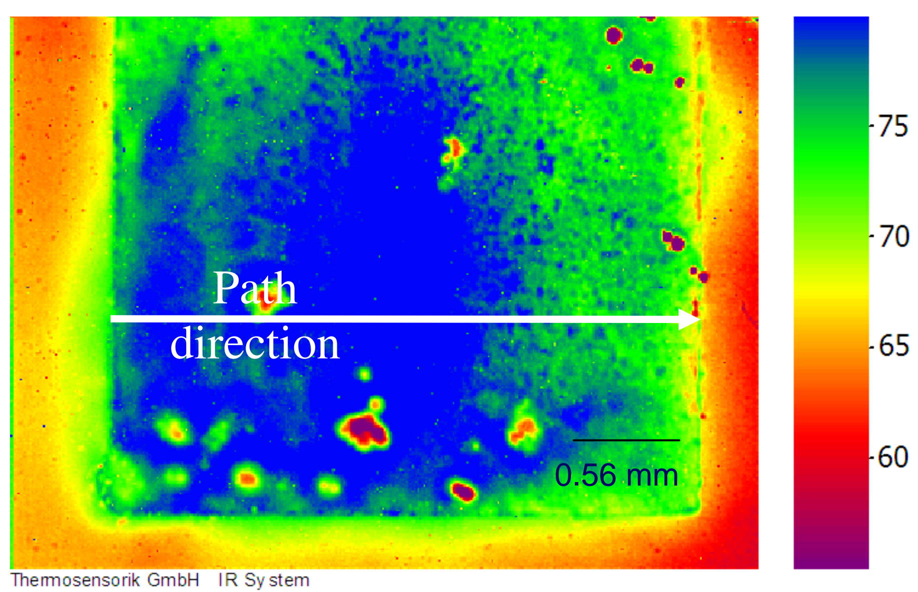

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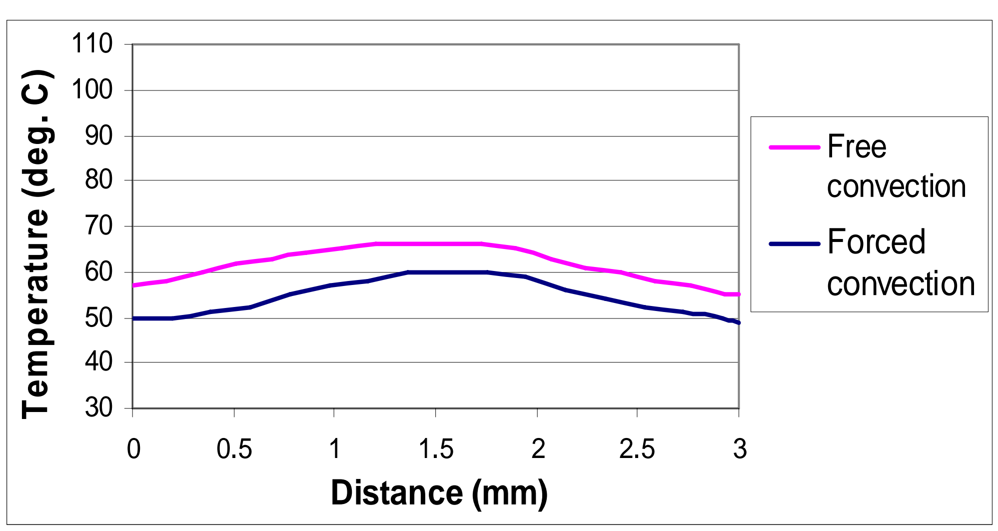

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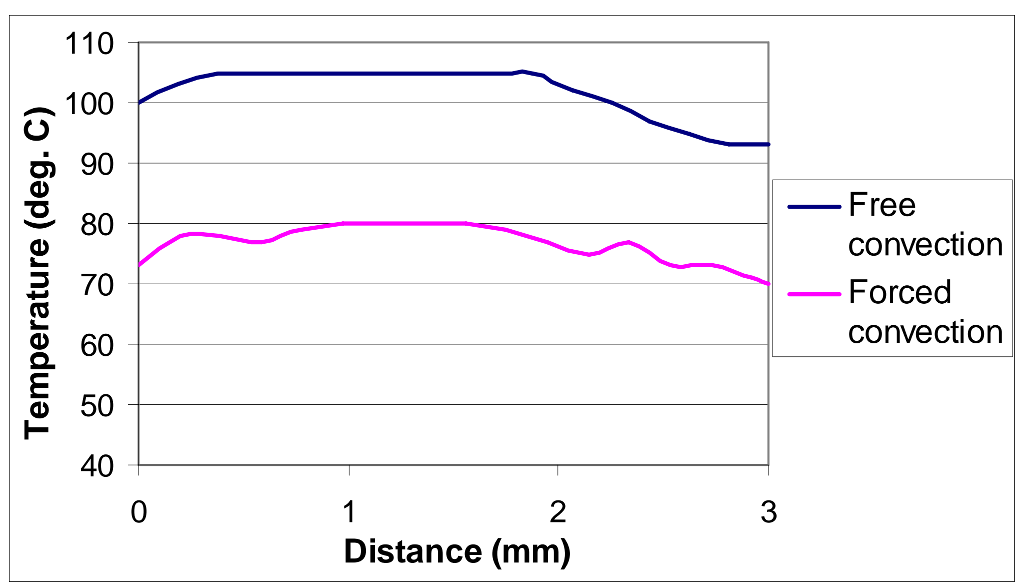

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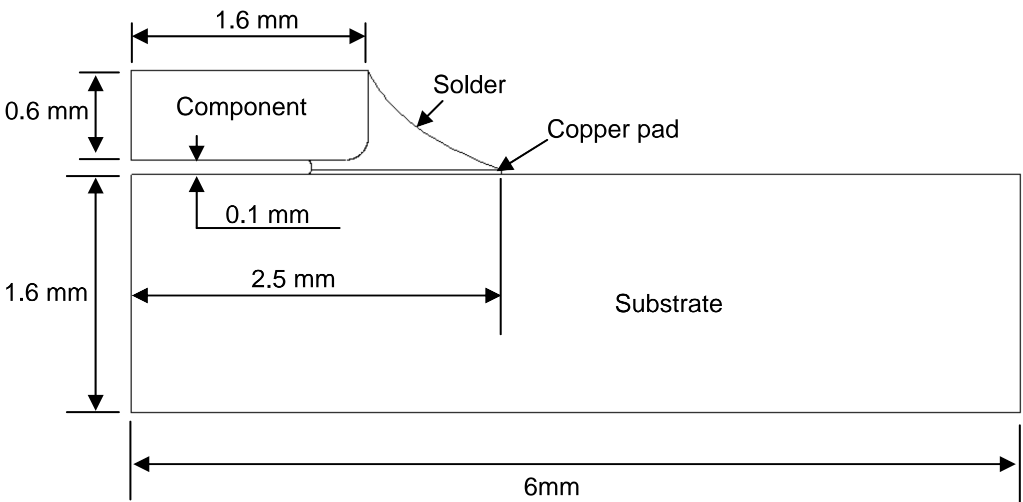

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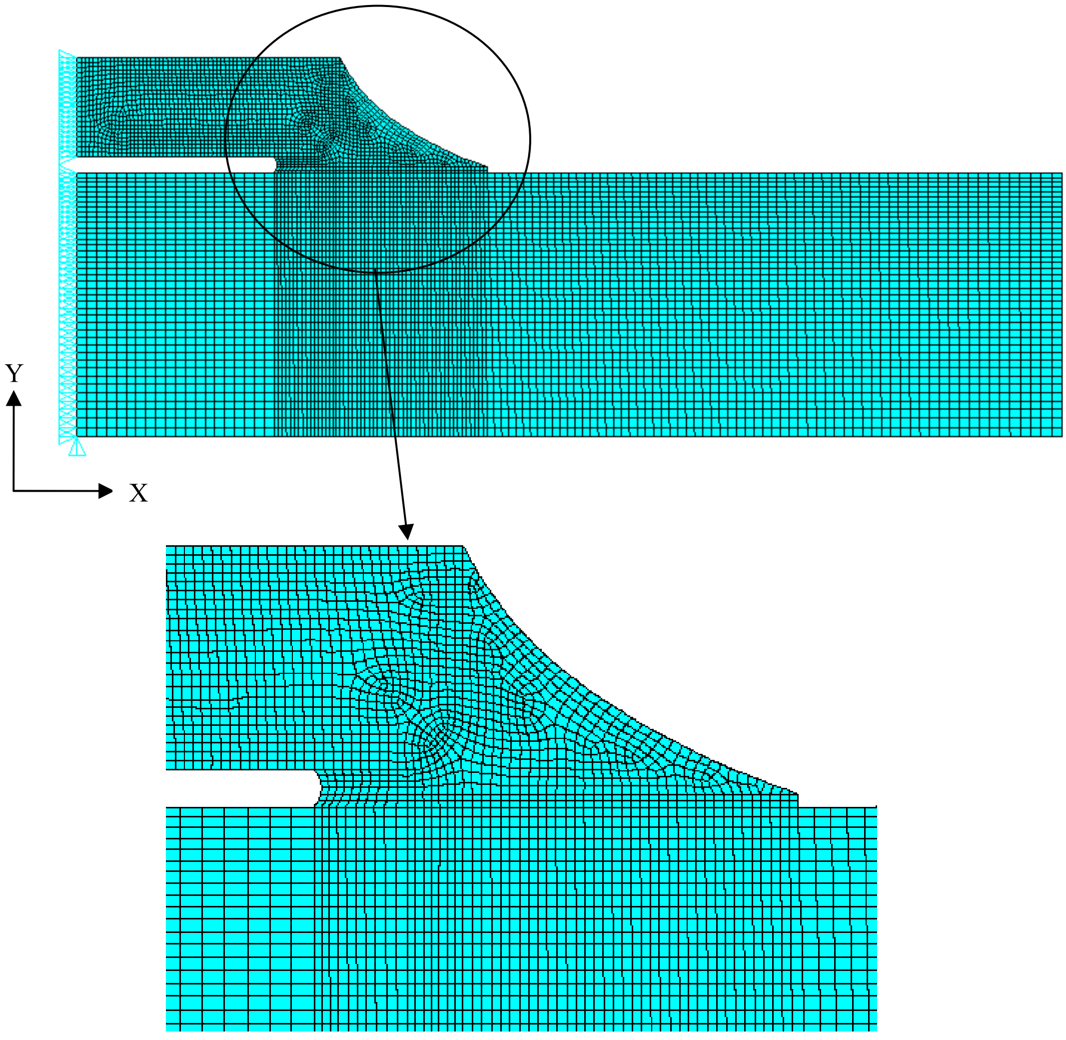

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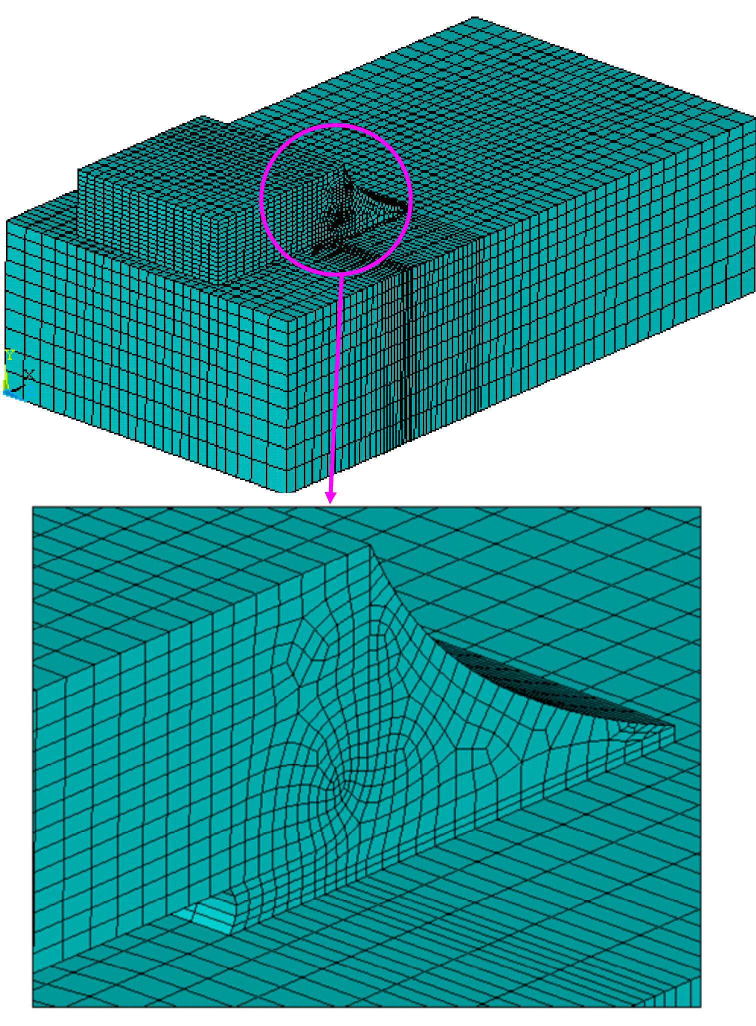

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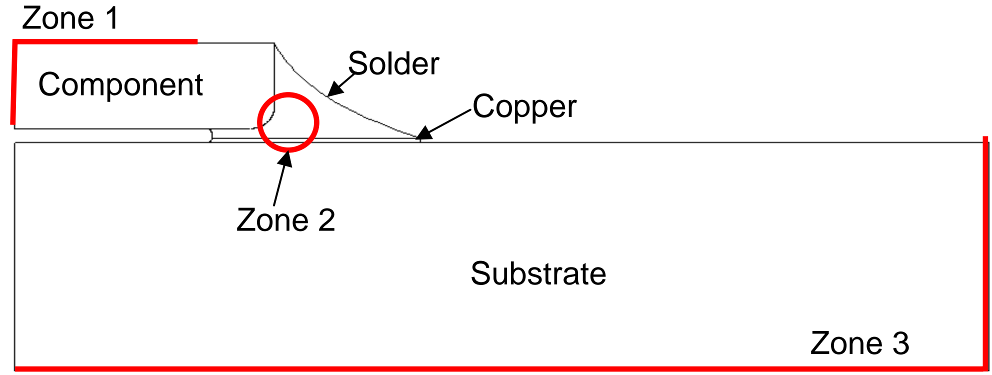

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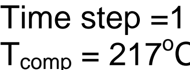

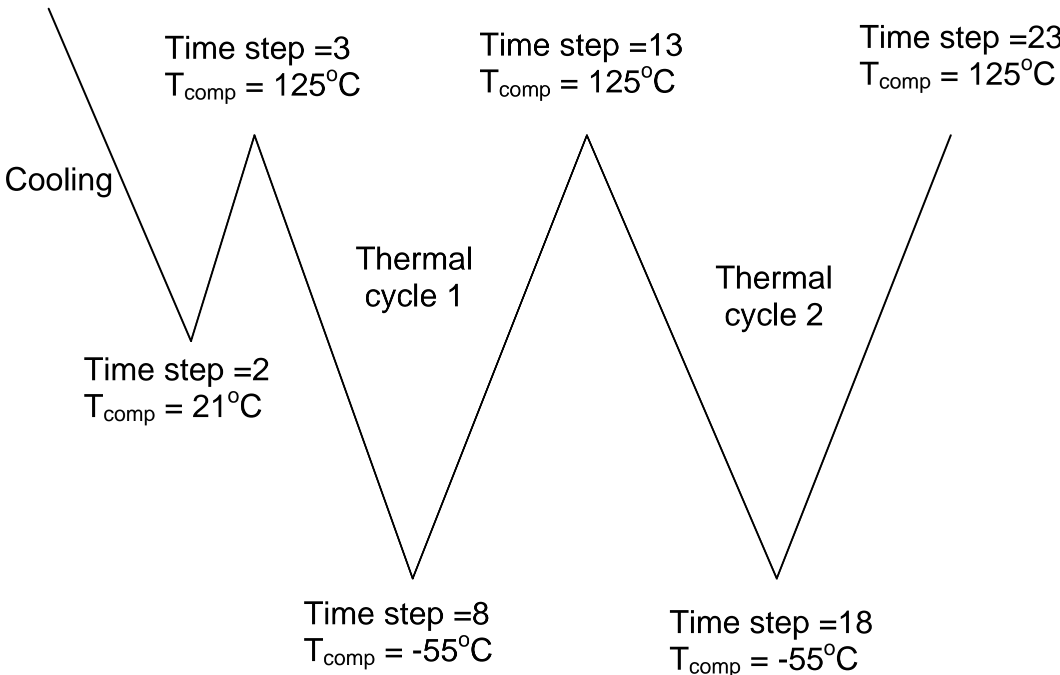

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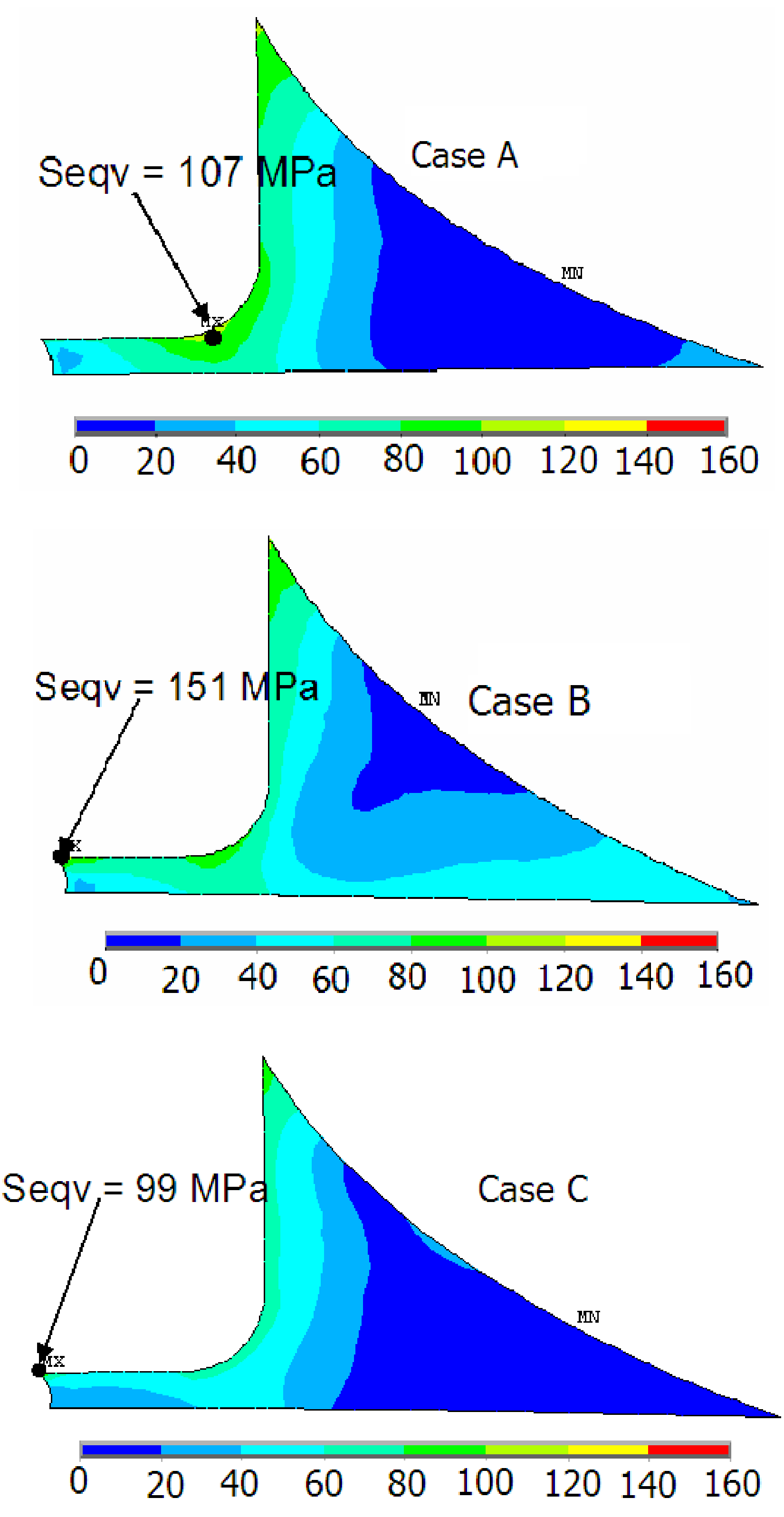

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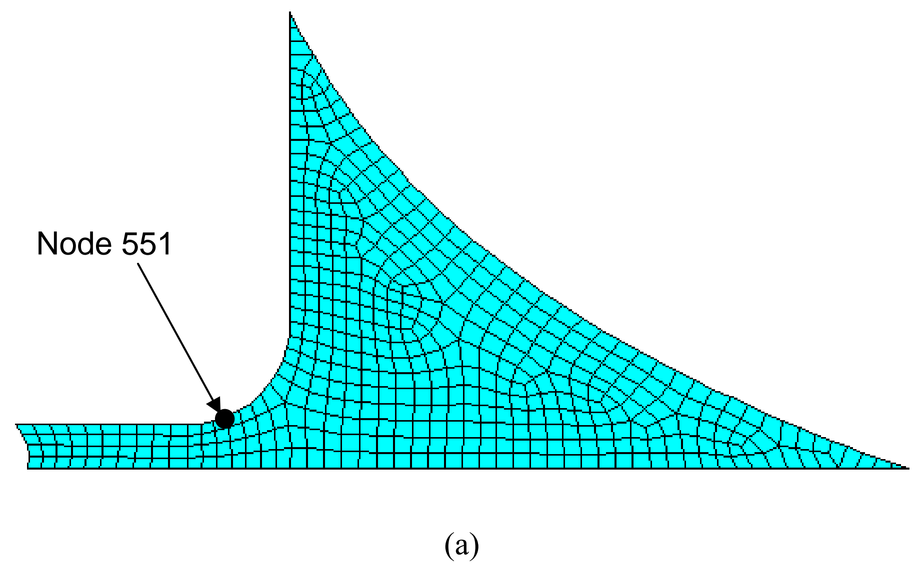

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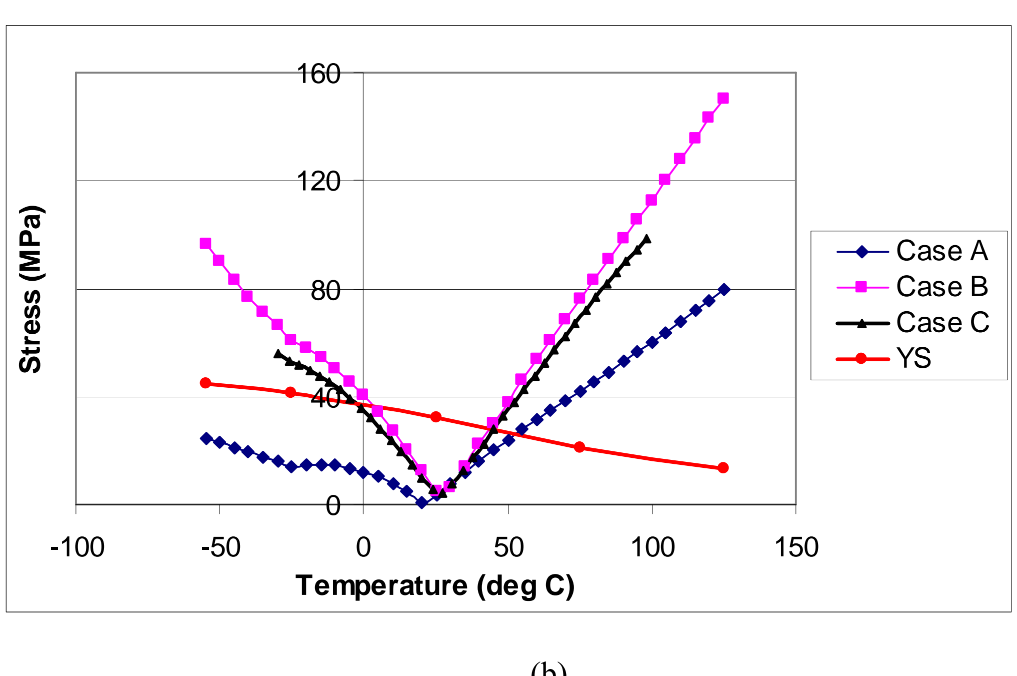
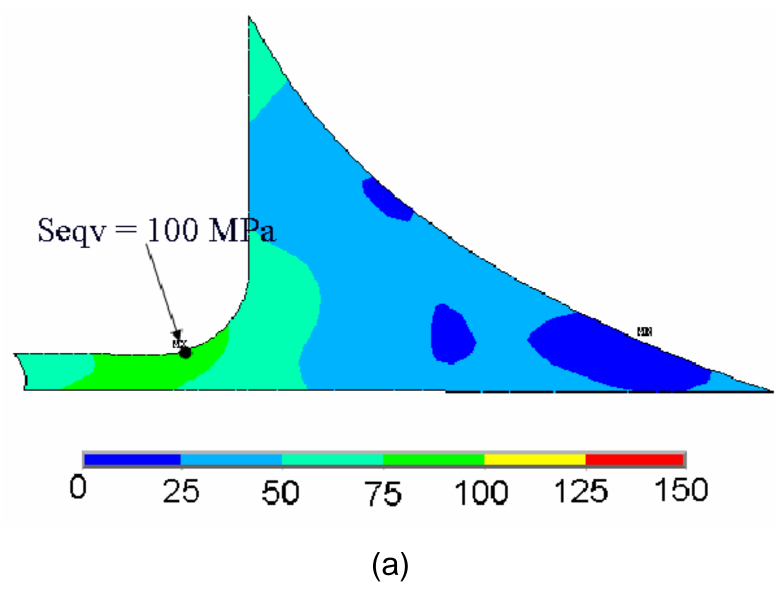


(b)

Figure 16



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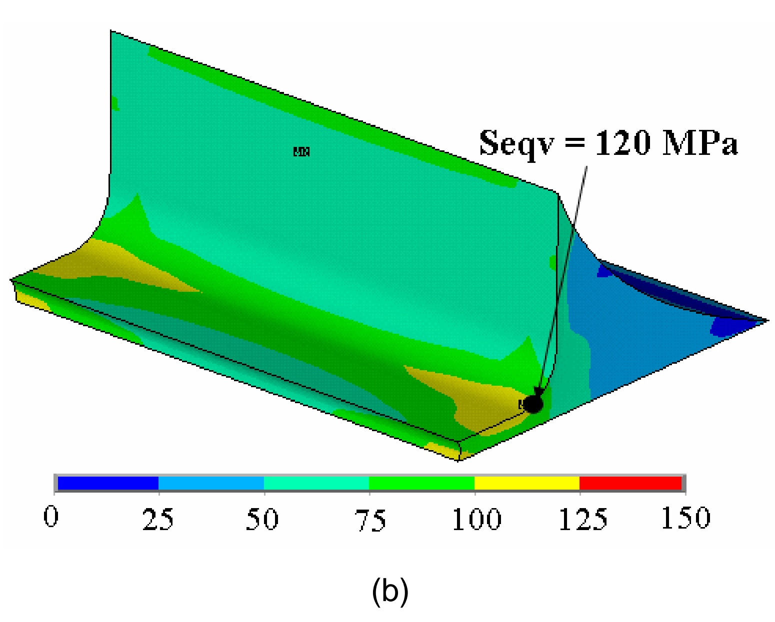

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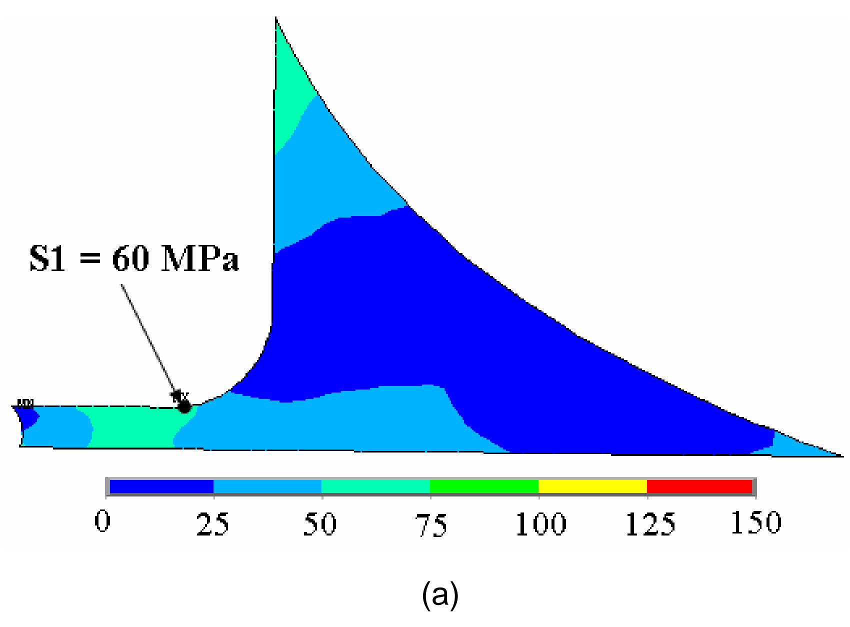
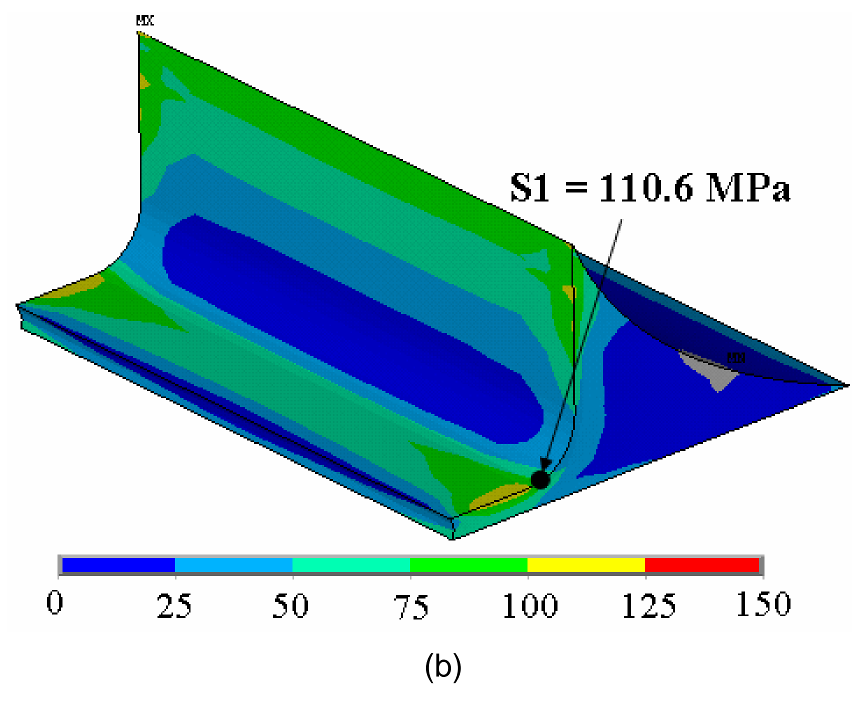
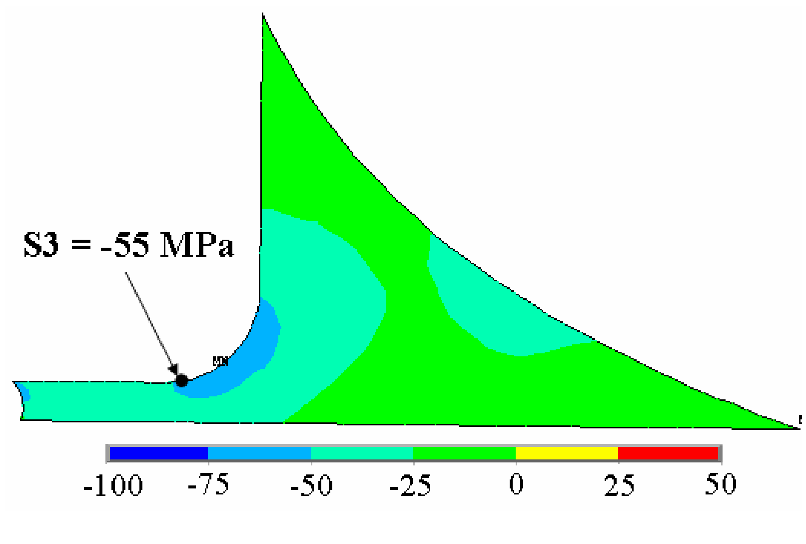


(a)

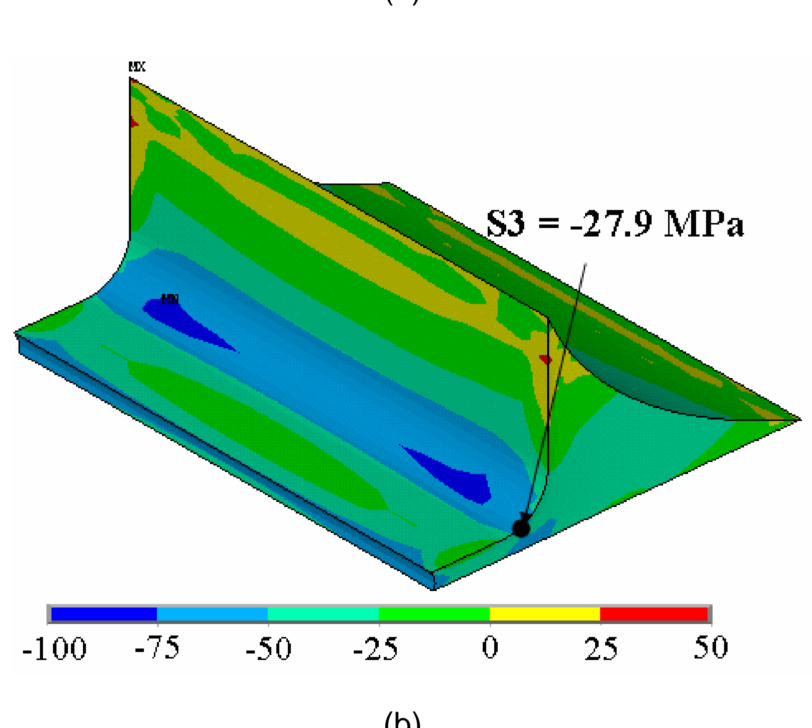


(b)

Figure 18



(a)



(b)

Figure 19

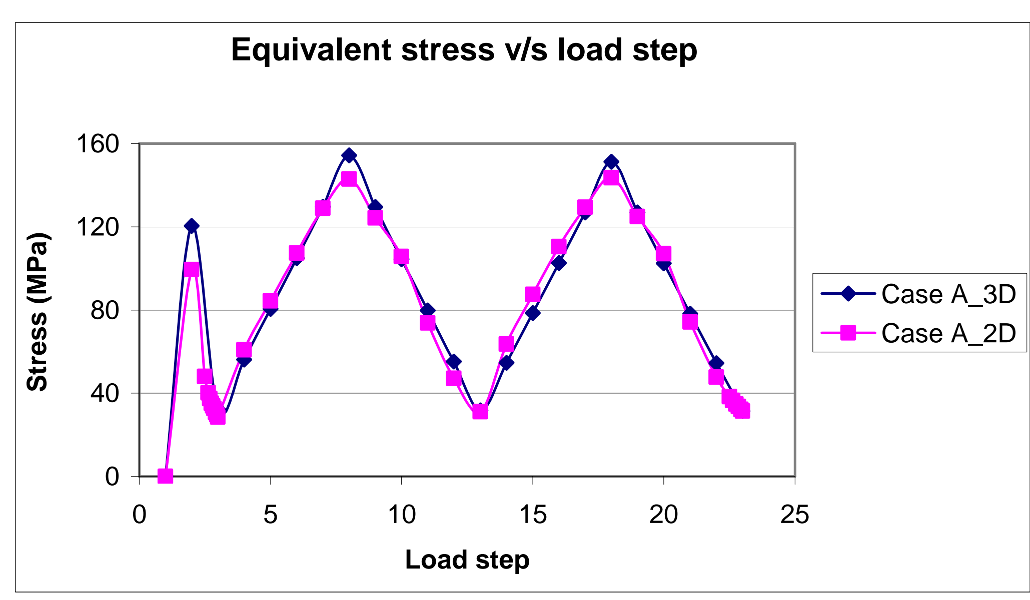
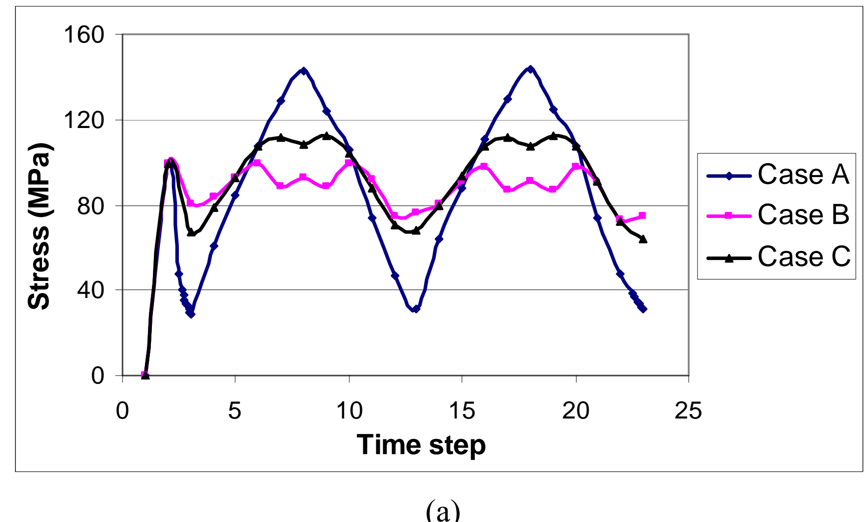
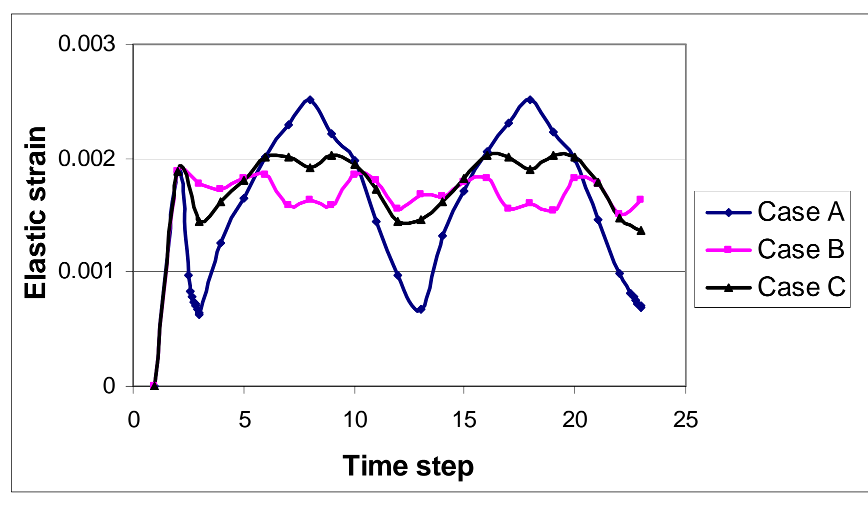


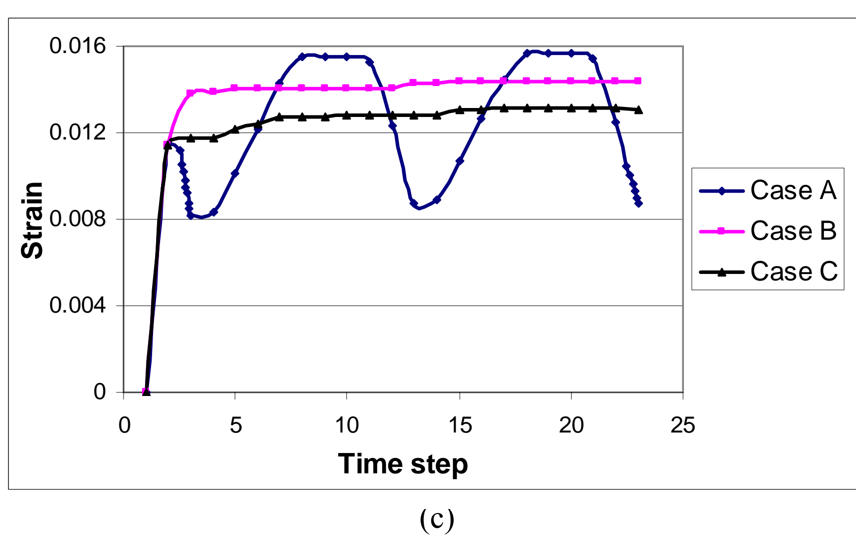
Figure 20



(a)



(b)



(c)

Figure 21