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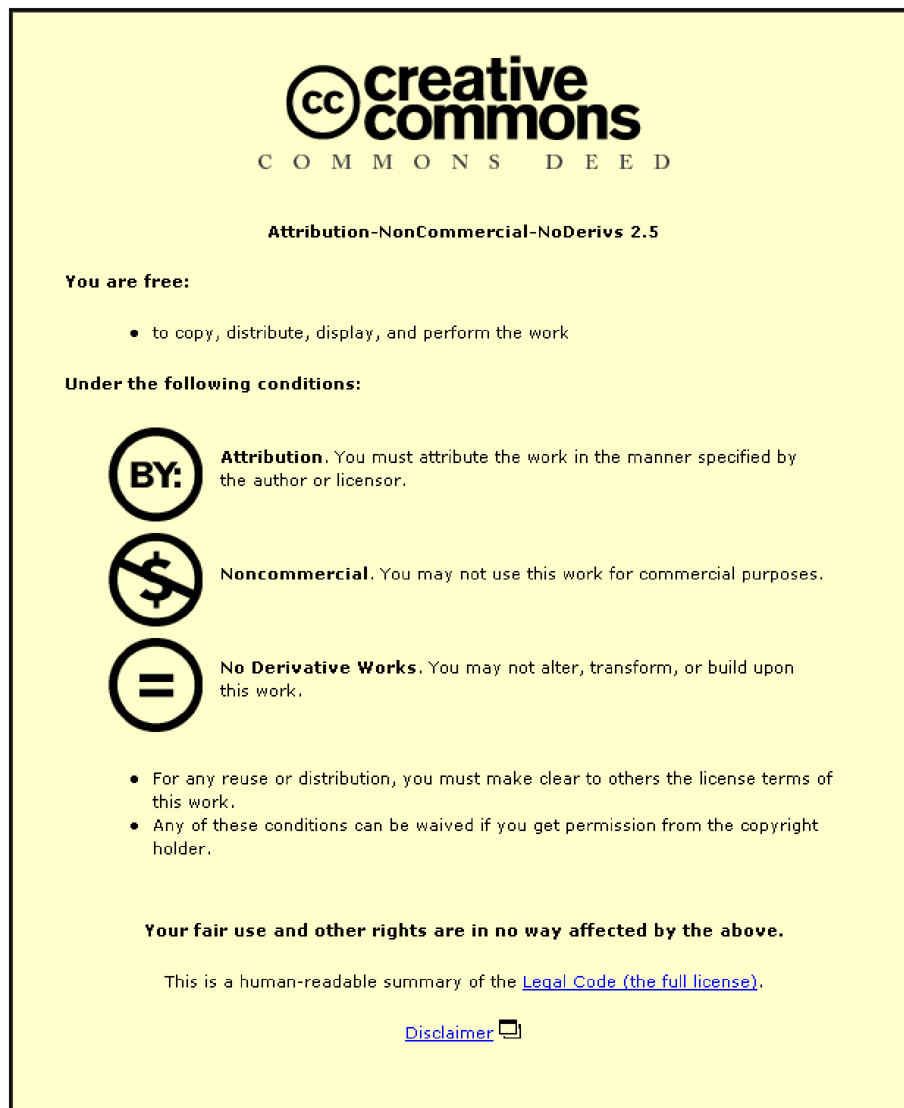

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CREEP DAMAGE STUDY AT POWERCYCLING OF LEAD-FREE SURFACE MOUNT DEVICE

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Abstract

Soldering is extensively used to assemble electronic components to printed circuit boards or chips to a substrate in microelectronic devices. These solder joints serve as mechanical, thermal and electrical interconnections, therefore, their integrity is a key reliability concern. However, newly introduced lead-free solders do not have a long history of applications in the industry and there is a lack of established material models of their behaviour over the wide temperature range experienced by electronics systems. Therefore, an extensive reliability study is required before introducing a new lead-free solder material in the electronic industries. Moreover, most of the solder materials have low melting temperatures, and are prone to creep in service. The cyclic temperature operating condition (powercycling) of the solder joint can result in the creep fatigue failure. Thus, a computational technique is used to investigate creep damage in solder joints. The present paper deals with creep damage of lead-free solder joints for powercycling using finite element analysis with the consideration of experimentally observed non-uniform temperature distributions in the 1206 surface mount chip resistor. In addition, a comparison is made for inelastic strain accumulation and fatigue life for creep damage study for spatially uniform and non-uniform temperature powercycling.

Keywords: PACS, 71.15.Dx, 85.40.Bh, powercycling, lead-free solder, creep analysis.

1. Introduction

Solder joints provide both electrical connection and mechanical support to electronic devices, which makes them indispensable in electronic packaging. Tin-lead (SnPb) solders were first used for metal interconnections about 2000 years ago [1]. In electronic industry, eutectic or near-eutectic Pb-bearing solder alloys, which meet most of the requirements for a good solder material, are extensively used. Research to replace the well-established Pb-based solder alloys with new lead-free solder alloys has gained importance due to the introduction of legislation on removal of lead from all electronic products in most parts of the world. Although several commercial and experimental Sn-based Pb-free solder alloys exist, none can be considered as a full substitute to traditional Pb-based solders. This is due to a relatively low melting temperature of the latter as compared to new lead-free solders. Nevertheless, new solders need to possess the desirable material properties, reliability and manufacturability.

Solder joints used in the electronic packaging operate under high homologous temperatures (T_h, a ratio of operating temperature and melting temperature on absolute scale) compared to its melting temperature. The typical operating conditions of solder joints are powercycling, vibration and impact (e.g. due to drops) loading and changes in environmental temperature. Integrity of solder joints is critical for reliable functioning of electronic components. The dominant type of failure in solder joints is creep fatigue due cyclic variations of load. Therefore, it is imperative to study the reliability aspects of new Pb-free solder joints in electronic packages before its broad use in various electronic packing. Accelerated temperature cycling (ATC) is a well-established experimental test used to study the reliability in the electronic industry. In this test, electronic components are placed in a chamber, in which temperature is cycled between extreme magnitudes. During this test, at each instant,

the oven operates quasi-statically, reaching a uniform temperature practically instantaneously.

The popularity of the accelerated thermal cycling is due to its simplicity in concept and operation. However, in recent years, there is an increasing debate on the applicability of thermal cycling tests for reliability studies since under the actual operating conditions, the heat is generated by a powered electronic device, and as a result, the package is under anisothermal conditions [2]. Thus, it is believed that powercycling accelerated tests, which result in uneven heating of electronic packages, represents service conditions more realistically. The typical temperature- and power-cycling tests are carried out in the range from -40ºC to 125ºC and 0ºC to 100ºC making both creep and fatigue a potential microscopic failure mechanism due to the high homologous temperature T_h, to which solder is exposed.

The present paper continues the previous work [3], where an elasto-plastic behaviour of the solder joint at thermal cycling was studied for assumed both uniform and non-uniform temperature distributions in the 1206 chip resistor assembly. This paper focuses on a creep behaviour of solders under powercycling. Initially, the experimental work carried out to establish the temperature distributions for powering of the surface mount chip resistor, which is actual representation of field use conditions, is described. These temperature distributions are used in the finite element creep analysis to study the creep damage accumulation in the solder joint of 1206 chip resistor for five power cycles. Creep analysis is carried out for both uniform and non-uniform temperature distributions (two cases of thermal loading) in the chip resistor that are explained below. Finally, fatigue lives are calculated for both cases of thermal loading based on the Coffin-Manson approach and comparison is made between them.

2. Experimental

To assess the non-uniformity of temperature distributions in the 1206 chip resistor due to powercycling, a series of experiments are carried out to acquire the temperature field using an infrared (IR) Thermosensorik camera. The temperature measuring technique is similar to the one described in [3]. Thermal radiation from the surface, which has a wavelength spectrum dependent on its temperature, structure and composition of the surface, is measured in the experiment. The higher the temperature, the more radiation is emitted; the temperature is measured by analysing thermal radiation. Infrared-measuring technique is contactless and non-destructive and supplies information with spatial and temporal resolutions that are usually not achievable with other measuring techniques.

Specimen description

The construction of the studied 1206 chip resistor is shown in Fig. 1. It consists of a thick-film resistive element mounted on an alumina substrate. The resistive element is covered with protective coating. The ends of the alumina substrate are covered with electrodes, which are used to power the chip resistor. This 1206 chip resistor can operate in the temperature range between -55ºC and +125 ºC. It has resistance 1.8 kΩ and the maximum power dissipation 0.25 W. As the ambient temperature increases, the power dissipation should be decreased to match the maximum power dissipation of the chip resistor. The required power supply to achieve the maximum power dissipation at room temperature is 21.3 V, which corresponds to the current with 0.01183 A.

The above described chip resistor is mounted on a FR4 substrate (width 3.2 mm) with 35 micron thick copper track (Fig. 2). The chip resistor is connected to the copper track with a lead-free eutectic Sn3.8Ag0.7Cu solder alloy. Electric connections are made to copper track

for powering the chip resistor.

Experimental set up

The experimental setup, used for acquiring the temperature data for the chip resistor assembly, is presented in Fig. 3. The chip resistor is painted with a matt black paint and mounted on a wooden block, which is placed over a variable lab jack. The camera, fitted with an infrared micro lens, is mounted on the tripod (not shown in Fig. 3). The specimen is powered on for a few minutes to stabilise the temperature distribution in the specimen, then the micro lens is focused on the specimen and the temperature profile is captured. The experiment is carried out to capture the temperature profile in the chip resistor assembly for two different power conditions – 0.25 W and 0.15 W. The results are presented only for maximum power condition due its relevance for the numerical simulations presented in this paper.

Experimental Results

A typical measured temperature distribution over the chip resistor is demonstrated in Fig. 4; it is evident that the maximum temperature 61.5ºC is at the centre of the chip where heat is generated due to resistance of the thick-film resistive element. This heat is conducted to other parts of the assembly. It is also observed that the temperature distribution decreases at the corners of the chip resistor, which is an indication of the temperature non-uniform distribution in the assembly. This is justified by Figs. 4b and 4c, demonstrating temperature distributions along two orthogonal lines. One of these distributions is more symmetric (Fig. 4b) than another; this is due to eccentricity of the resistive element's position along line 2.

The validation of the temperature distributions captured with the thermal camera is made by

comparing it with the temperature obtained by means of thermo-couple measurements. A very fine thermo-couple with diameter of 40 µm is used for the latter to avoid heat dissipation through it. The thermo-couple was calibrated by measuring temperature of boiling water. The comparison of temperatures at different locations of chip resistor assembly is presented in Table 1; the locations considered for are given in Fig. 2. A maximum temperature discrepancy 1.5ºC between two measuring techniques is observed at the centre of the chip, while at other locations it is about 1ºC. The temperature measurement in the afternoon estimates a slightly higher temperature level (65.5ºC) due to the increase in the ambient temperature; the discrepancy is also higher here. However, the temperature gradient in the chip resistor assembly remains nearly the same (23.5ºC). The obtained temperature distribution is used as input information for finite element creep analysis.

3. Finite element analysis

The complexity of the studied structure makes the use of analytical techniques cumbersome and presupposes employment of numerical simulation tools. The finite element analysis is an obvious choice to solve a thermomechanical problem for a complex behaviour of the multi-material assembly exposed to non-trivial thermal boundary conditions.. The use of numerical simulations can reduce the time and cost associated with the reliability study of solder joints, which otherwise include a time consuming and expensive experimental technique – ATC – used to assess the reliability of electronic product.

Geometry and material

Both 2D and 3D finite element models of the analysed assembly (see Fig. 2) are built to study the evolution of stresses and creep damage accumulation during powercycling. The geometry used for finite element analysis is the one used in the experiment. The geometric

dimensions for both 2D and 3D are similar to those used in [3].

Since material properties vary with temperature, temperature-dependent material parameters are introduced into the FEA. The material properties used to model a ceramic component, copper pad and FR4 are the same as in [3]. The undertaken studies showed that powercycling induces stress levels in solder joints beyond yield and temperature ranges between $0.55T_h$ and $0.68T_h$. When the operating temperature is more than $0.4T_h$, most of the materials undergo creep deformation. Therefore, the creep material model is introduced for the solder joint to capture the effect of creep damage during powercycling. Material properties for the SnAgCu solder joint are shown in Table 2 [4], and a bilinear kinematic hardening material model is used for elasto-plastic modelling of the solder joint, which includes the Bauschinger effect due to cyclic loading. To reduce the complexity and analysis time, only the SnAgCu solder joint is modelled with the elasto-plastic material behaviour. Its creep behaviour is described by the hyperbolic sine law used for the steady-state creep:

$$\dot{\varepsilon}_{cr} = A \sinh(\alpha\sigma)^n \exp\left[\frac{-H}{RT}\right], \quad (1)$$

where A = 277984, α = 0.02447, n = 6.41, H/R = 6500. $\dot{\varepsilon}_{cr}$ is a steady state-creep strain rate, σ is a stress level, T is absolute temperature [3].

Element selection and meshing

2D finite element modelling is implemented with plane strain elements to better represent the field problem and compared with the 3D formulation. Only one half of the geometry is modelled to make use of the symmetry of the structure. The commercial FEA software package ANSYS is used for both finite element modelling and analysis. A 2D model is built with 4-noded PLANE182 elements with the plane strain option. The 2D finite element model

contains 8058 elements with finer mesh at the solder joint area that is the region of interest. The 3D finite element model is built with 8-noded SOLID 45 element, and there are 33017 elements in this model.

Loads and boundary conditions

In the present creep analysis, only a thermal load is considered, which is a major cause for creep fatigue failures in solder joints. The thermal load for the 1206 chip resistor assembly is applied through powercycling. Research has been carried out to decide upon the dwell time used in the powercycling. Since most of the creep damage accumulation takes place during the hot dwell [2]. The longer hot dwell results in higher accumulation of inelastic strain and a shorter fatigue life. In contrast, shorter dwells do not allow a sufficient time for creep damage and result in a higher fatigue life. Further, according to previous research, the fatigue life is most sensitive to the hot dwell time that ranges between 5 to 10 minutes. Effect of hot dwell time on creep damage accumulation is insignificant when it is beyond 10 minutes [2]. Therefore, it is critical to select the proper dwell time in the powercycling to accurately represent the test condition. In the present powercycling used for creep analysis, 5 minutes hot and cold dwell time is used with total cycle time of 22 minutes. Details of temperature changes during the power cycle used in our simulations are given in Fig. 5.

Most commonly, creep analysis for powercycling is carried out considering a uniform temperature distribution in the chip resistor. This does not accurately represent the temperature distribution in the assembly when it is powered. Therefore, in the present creep analysis two different thermal profiles are used for powercycling: a non-uniform temperature distribution in the chip resistor assembly at hot dwell (**Thermal load case 1)** and a uniform temperature at hot dwell with the temperature corresponding to the maximum one I the

measured distribution when the chip resistor is powered on to its full power (**Thermal load case 2).** This enables us to compare the creep damage accumulated in the solder joint due to two assumed boundary conditions. The temperature in both thermal profile changes between 273 K and 333.5 K (which is the maximum temperature in the chip resistor assembly when chip resistor is powered to its maximum load). Figure 5 shows the power cycle used in creep analysis. Before the chip resistor assembly is subjected to powercycling, reflow (line AB) and a one-hour dwell period at room temperature (line BC) is simulated for creep. CD represents the ramp from room temperature to the hot dwell with a 5 minute dwell (line DE). Then the temperature is ramped down (line EF) to the cold dwell (0ºC) with 6 minutes ramp. After 5 minutes of the cold dwell (line FG), temperature is again ramped up (line GH) for the hot dwell to start powercycling again.

The structural boundary condition employed for creep analysis is similar to the one in [2] – a symmetry boundary condition is used for the finite element model to represent the symmetry and restrain the rigid body motion. In addition, a bottom node in the symmetry plane is also restrained in the vertical direction.

4. Results and discussion

Thermal analysis

A thermal analysis is carried out to obtain the temperature distribution for the 1206 chip resistor assembly when the resistor is powered on to its maximum power condition (0.25 W) at room temperature. The temperature distribution obtained from our experimental work is used as the boundary condition for the finite element thermal analysis. Figure 6a demonstrates the temperature boundary condition used for thermal analysis, while Figure 6b shows the temperature distribution in the chip assembly for maximum power condition. This

is the temperature distribution used at the hot dwell of the power cycle in thermal load case 1.

Structural analysis

4.2.1 Comparison of 2D and 3D finite element simulation

A comparative study is implemented to decide on the type of finite element modelling – 2D or 3D – for creep analysis. This study is carried out for the thermal profile with a uniform temperature distribution in the chip assembly. A creep analysis is conducted for both 2D and 3D models with similar loads and boundary conditions for three power cycles. The obtained distribution of shear stresses in the solder joint at the end of the dwell (point C in the thermal profile, Fig. 5) at room temperature is shown in Fig. 7. From comparison of 3D and 2D stress distributions, it is obvious that the stress magnitudes (between -6 MPa and 12 MPa) and positions of their extreme levels match very closely in both models.

Evolution of shear creep strain and stress is also studied for both 3D and 2D models over the dwell period at room temperature and three subsequent power cycles. The shear stresses calculated at a maximum stress location in the solder joint's fillet are compared in Fig. 8a. It is obvious that both schemes provide very close results over the cycle time, except for a slight discrepancy during the beginning of the dwell period. The evolution of shear creep strain over the dwell and subsequent power cycles is depicted in Fig. 8b for both types of dimensions. It is obvious from the graph that levels of shear creep are particularly the same in the initial period (till 285 seconds); thereafter a difference between the graphs appears. However, this difference between 3D and 2D models narrows as the powercycling progresses, changing from 6% in the first power cycle to 3% in the third power cycle. This indicates that 2D finite element simulations pretty well match 3D simulations, and further creep analysis can be carried out using the 2D model to reduce the computational time.

4.2.2 Creep analysis

A detailed creep analysis of the 1206 chip resistor assembly is carried out for five power cycles with two different thermal conditions corresponding to thermal load cases 1 and 2. The calculated distribution of the equivalent stress in the fillet of the solder joint at the start of the power cycle (location D in the thermal profile) is shown in Figure 9a. There is no significant difference in the stress distributions between non-uniform and uniform thermal load cases with the respective maximum stresses 15 MPa and 17 MPa. A similar observation can be made for the stress distribution at the start of the cold dwell (point F in the thermal profile, Fig.5). However, it is evident from Fig. 9b that the level of stresses in the solder joint is higher for the cold dwell compared to that for the hot dwell due to higher thermal strain. Figure 10 presents the shear stress distributions for the same moment of the thermal history. The analysis of stress distributions in the solder joint demonstrates that the solder fillet is the area of stress concentration that is the potential location for crack initiation.

A study of evolution for both equivalent and shear stresses for the location of the maximum stress in the solder joint's fillet over five power cycles is carried out for two thermal loading cases. In addition, the stress range in each power cycle is calculated and compared for these two cases. Figures 11 and 12 illustrate the variation of equivalent and shear stresses, respectively, in the solder joint's fillet over the dwell at room temperature and five power cycles. Both the maximum equivalent stress (42 MPa) and the maximum shear stress (24 MPa) are observed at the end of reflow. The magnitudes of both stresses decrease with relaxation representing the dwell at room temperature. The stress variation shows that stress cycles practically do not change the shape; there is a decrease in the magnitude for the lowest point; the decline of the maximum value with power cycle is significantly less pronounced. Difference between the stress ranges for cases 1 and 2 of thermal loading. From this study, it

is clear that stress range is nearly constant (24 MPa for the non-uniform temperature distribution case and 27.5 MPa for the uniform one) and the uniform temperature distribution case always results in the higher level of the stress range for both equivalent and shear stresses.

A study on creep strain accumulation is also conducted to find out the extent of creep damage caused by powercycling in the solder joint. It was shown in our previous work [3] that the critical temperatures corresponding to the onset of plastic flow are well within the range of thermal cycling of solder joints (presupposing the account for plastic strain component). In the conducted creep analysis accounting for the elasto-plastic material behaviour of SAC solder, the inelastic strain in the solder joint is calculated. This is due to both plastic and creep deformation. Evolution of this strain in the fillet of the solder joint is demonstrated in Fig. 13 for powercycling. It is obvious that accumulation of inelastic strain increases with time due creep. The inelastic strain contribution due to plasticity ceases at the end of reflow (point B in the thermal profile, Fig. 5) since the magnitudes of stresses induced in the solder joint in subsequent power cycles do not exceed the level attained at the end of reflow. The comparison of inelastic strains for Cases 1 and 2 indicates that strain accumulation is always higher in case of the uniform temperature distribution. The inelastic strain range for each power cycle is given in Table 5. Interestingly, this strain range is almost the same in the first power cycle for both cases. This range decreases as powercycling progresses, an indication for the stabilisation of the stress-strain hysteresis loop after few power cycles. The difference in inelastic strain ranges between Cases 1 and 2 increases from 0.42% in the first power cycle to 22.8% in the fifth power cycle. This difference has a direct effect on the corresponding fatigue lives.

4.2.3 Fatigue life estimation

There are various methods to calculate the fatigue life of solder joints. One among the most commonly used is the strain-range based Coffin-Manson method. The following Coffin-Manson equation [5] is used to calculate the fatigue life based on the inelastic strain range obtained from the creep analysis:

$$N_f = (C'\varepsilon_{acc})^{-1}, \qquad (2)$$

where N_f is the number of cycles to failure (fatigue life), C'= 0.0468 [5], ε_{acc} is the accumulated inelastic strain range per cycle. Fatigue life for both cases is calculated based on the strain range in the fifth power cycle (see Table 5). The calculated fatigue life of Case 1 – 6341 cycles – is 23% higher than that for Case 2 (5161 cycles). This indicates that consideration of the non-uniform temperature distribution has a significant effect on the estimate of the fatigue life of solder joints.

5. Conclusions

The finite-element creep study of a surface mount resistor under non-uniform temperature loads allows us to draw the following conclusions:

1. The experimental study of the chip resistor shows that the temperature distribution in the assembly is not uniform under the condition of powering.
2. An assumption of the uniform temperature distribution in the chip resistor assembly overestimates the inelastic strain accumulation. This overestimation results in the lower predicted fatigue life compared to the case of the non-uniform temperature distribution.
3. Accumulation of plastic strain in the solder joint ceases after the reflow making creep the main source of the inelastic deformation in the joint.
4. The range of inelastic strain stabilises with the increase in the number of power

cycles.

The next stage of finite element analysis of reliability of lead-free surface mount assemblies will be linked with direct introduction of interfacial crack initiation and growth, which will be implemented using cohesive zone elements at the interfaces.

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Figure Captions

Figure 1: Construction of a 1206 chip resistor

Figure 2: Mounting of chip resistor on FR4 substrate

Figure 3: Experimental setup (without infrared camera)

Figure 4: Temperature distributions in chip resistor: (a) over chip surface; (b) along line 1; (c) along line 2

Figure 5: Thermal profile used in powercycling: Reflow (AB) – 48 s; Dwell at room temperature (BC) – 3600 s; Ramp (EF, GH) – 360 s; Cold dwell (FG) – 300 s; Peak temperatures of power cycle (D, E) – 333.5ºC; Temperature range of power cycle 60.5ºC.

Figure 6: Thermal analysis for chip resistor assembly: (a) temperature boundary conditions; (b) calculated temperature distribution (in K)

Figure 7: Distribution of shear stresses in 3D (a) and 2D (b) after dwell at room temperature

Figure 8: Evolution of shear stresses (a) and shear strains (b) in 2D and 3D creep analysis

Figure 9: Equivalent stresses in solder joint: at point D (a) and F (b) of the thermal profile (Fig. 5)

Figure 10: Shear stresses in solder joint: at point D (a) and F (b) of the thermal profile (Fig. 5)

Figure 11: Evolution of equivalent stress in solder joint's fillet (Fig 10)

Figure 12: Evolution of shear stress in solder joint's fillet (Fig 10)

Figure 13: Evolution of inelastic strain in solder joint's fillet (Fig 10)

Table 1: Temperature magnitudes measured with thermocouple and thermal camera

Location (see Fig. 2)	Room Temperature = 22°C		Room Temperature = 24.5°C	
	Morning		Afternoon	
	Thermocouple	Thermal camera	Thermocouple	Thermal camera
1	60.5	61.5	62.5	65.5
2	56	55	57	55
3	54	54	56.5	53
4	39	38	44.5	43.5
5	53		55	
6	52		54	
7	39	38	44	43
8	38		41	
9	45		46	
10	38		41	

Table 2: Material properties of Sn3.8Ag0.7Cu [4]

Temperature (K)	Young's modulus (MPa)	Poisson's ratio	CTE (ppm)	Density (gm/cm^3)	Yield Stress (MPa)	Tangent modulus (MPa)
298	32331	0.4	21.2	7.5	38	154
348	8285	0.4	21.7	7.5	30	134
423	6517	0.4	23.0	7.5	17	132

Table 3: Range of equivalent stress in power cycles

Cycle	Range of equivalent stress (MPa)		Difference, %
	Thermal load case 1	Thermal load case 2	
1	22.8	25.5	11.8
2	23.0	26.5	15.2
3	23.8	27.9	17.2
4	24.8	28.9	16.5
5	25.6	29.6	15.6

Table 4: Range of shear stress in power cycles

Cycle	Range of shear stress (MPa)		Difference, %
	Thermal load case 1	Thermal load case 2	
1	21.8	25.3	16.1
2	22.6	25.9	14.6
3	23.1	26.2	13.4
4	23.4	26.5	17.2
5	23.7	26.8	13.1

Table 5: Range of inelastic strain in power cycles

Cycle	Range of inelastic strain		Difference, %
	Thermal load case 1	Thermal load case 2	
1	0.00622	0.00625	0.42
2	0.00467	0.00512	9.52
3	0.00402	0.00462	14.97
4	0.00363	0.00433	19.17
5	0.00337	0.00414	22.80

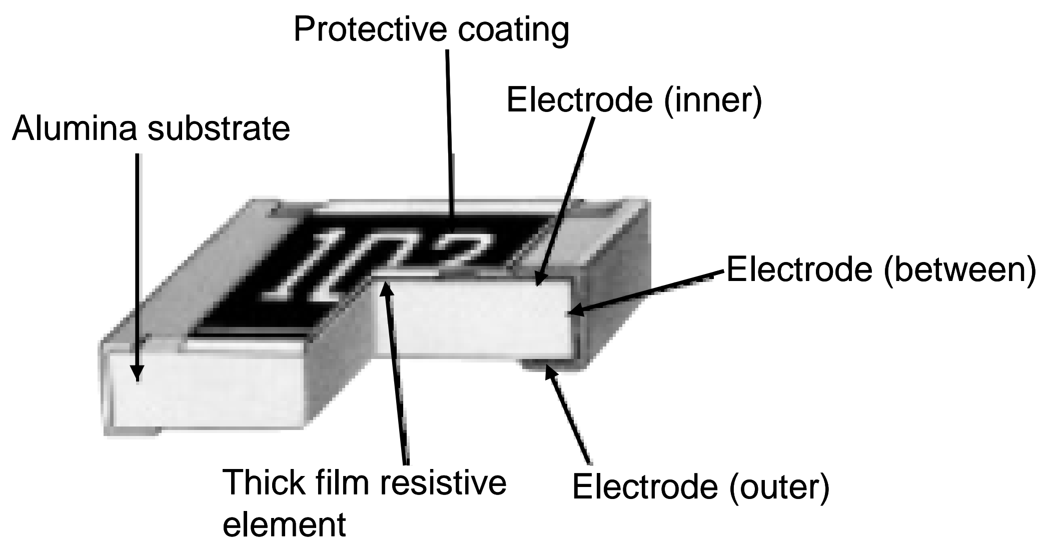


Figure 1

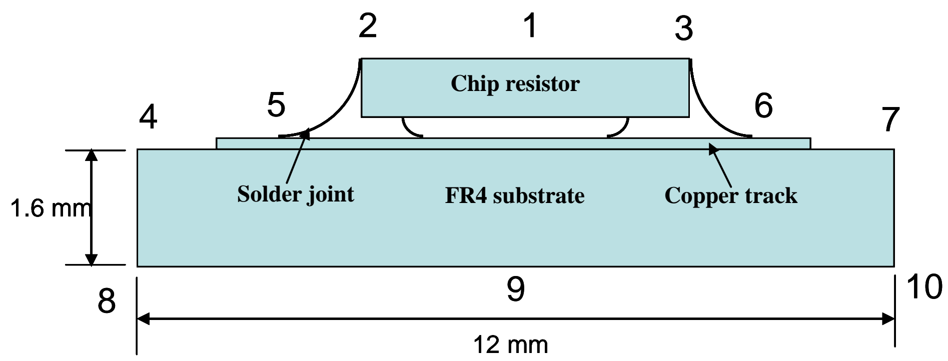


Figure 2

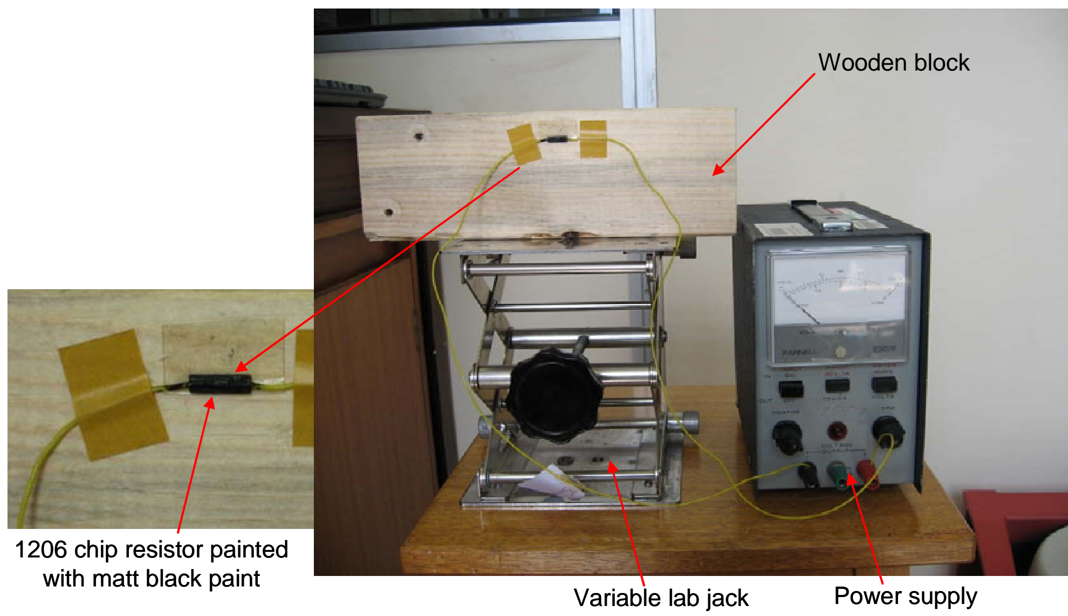
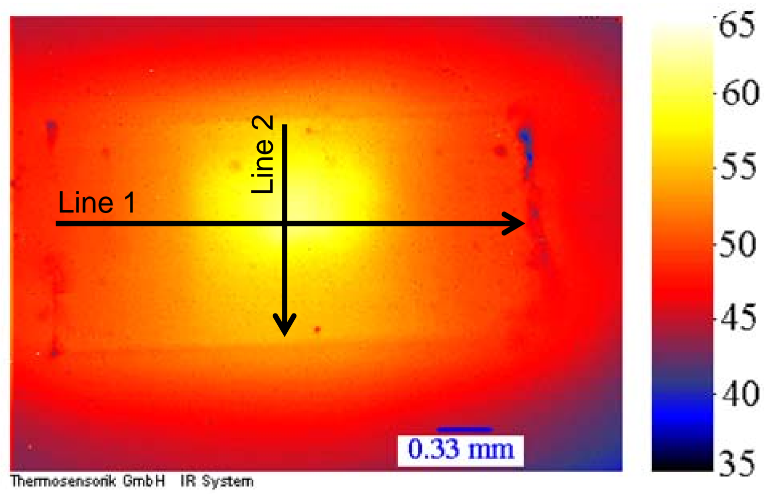


Figure 3



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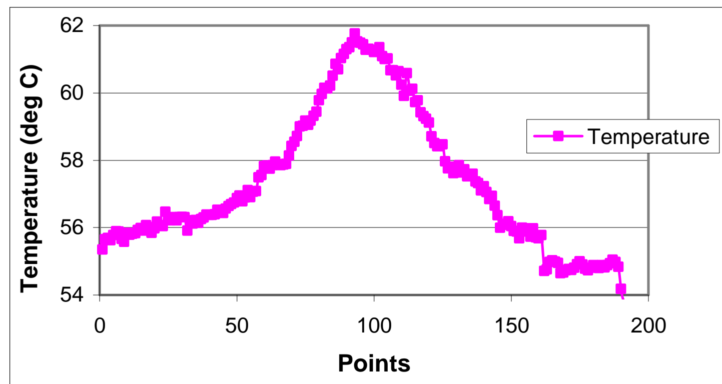

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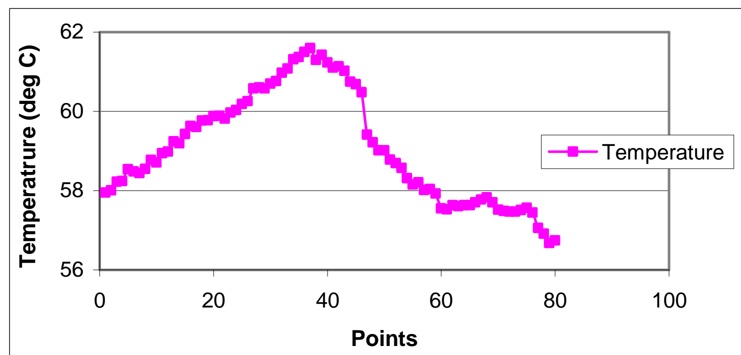

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Figure 4

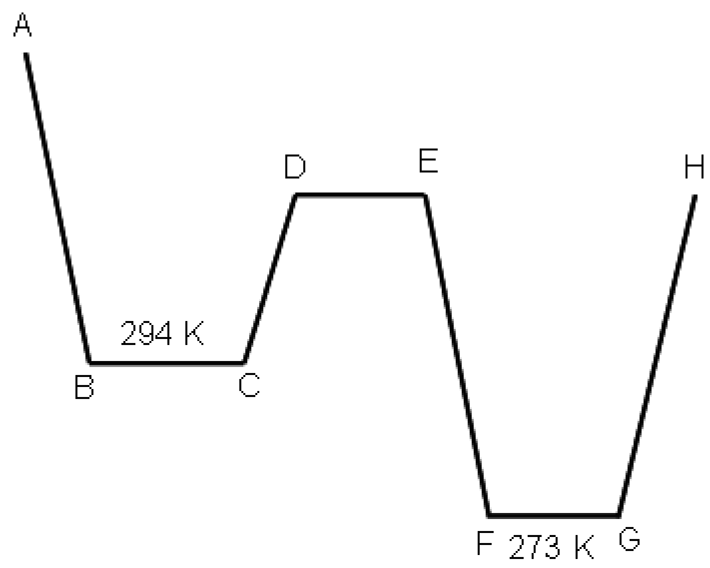
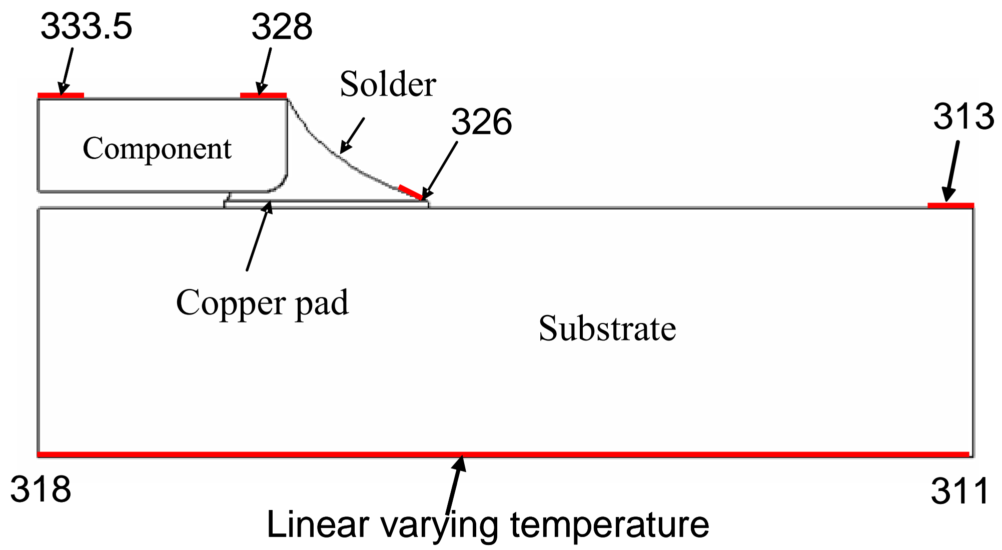


Figure 5



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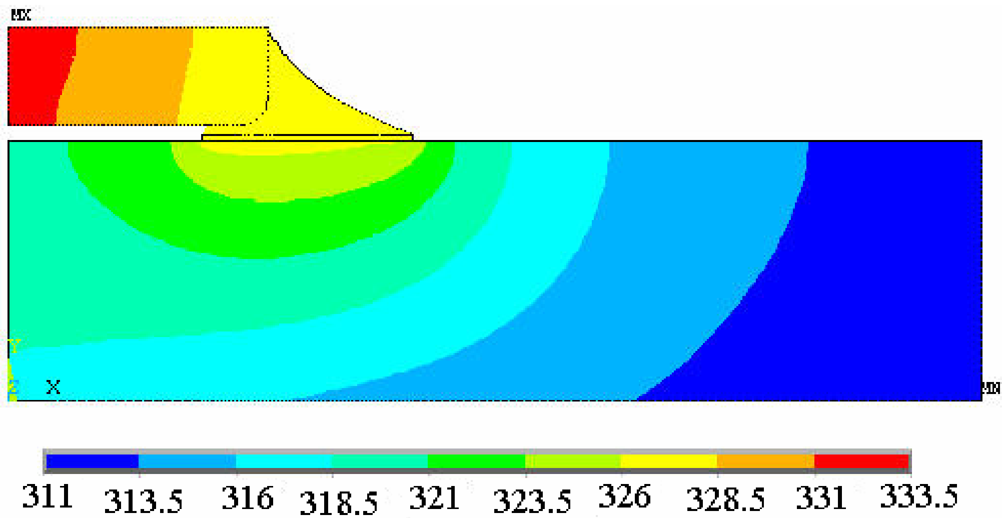

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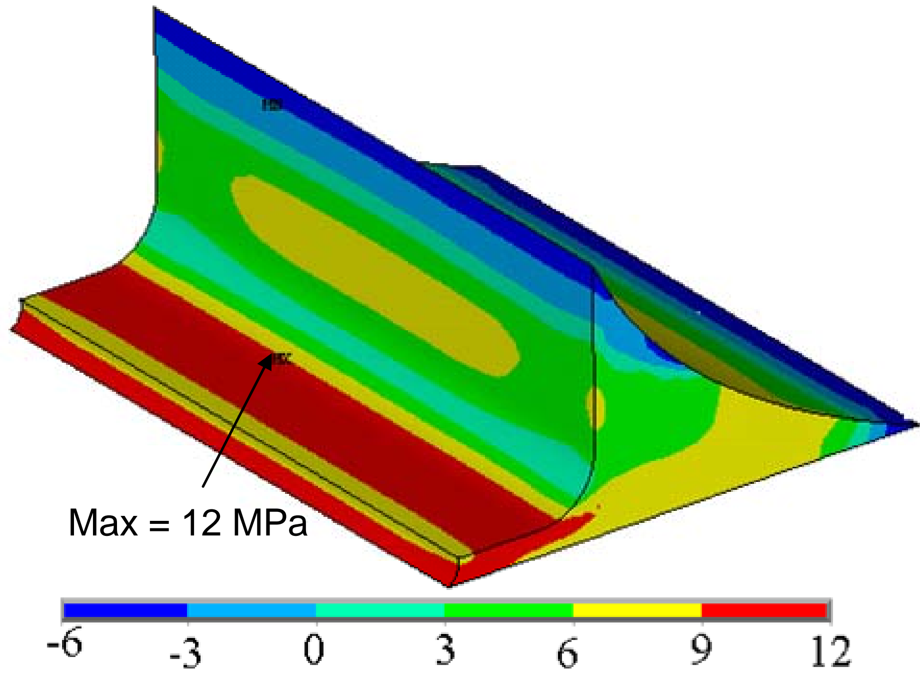
Figure 6



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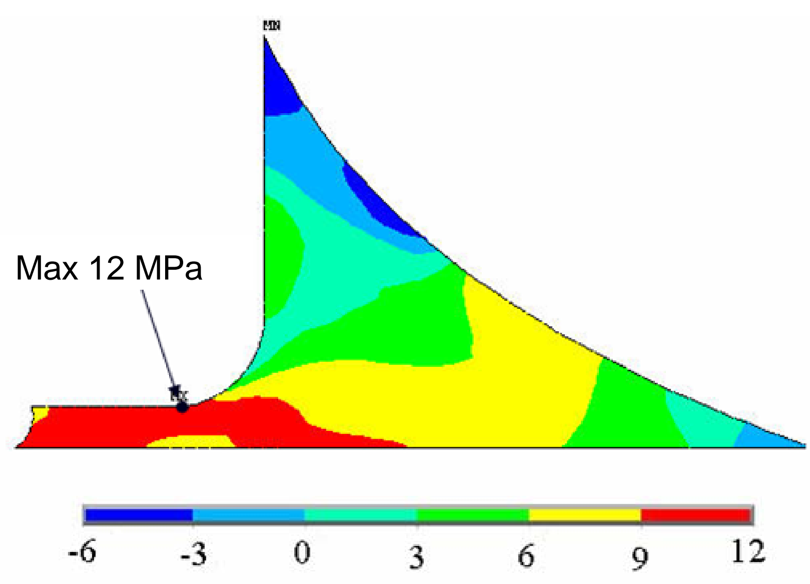

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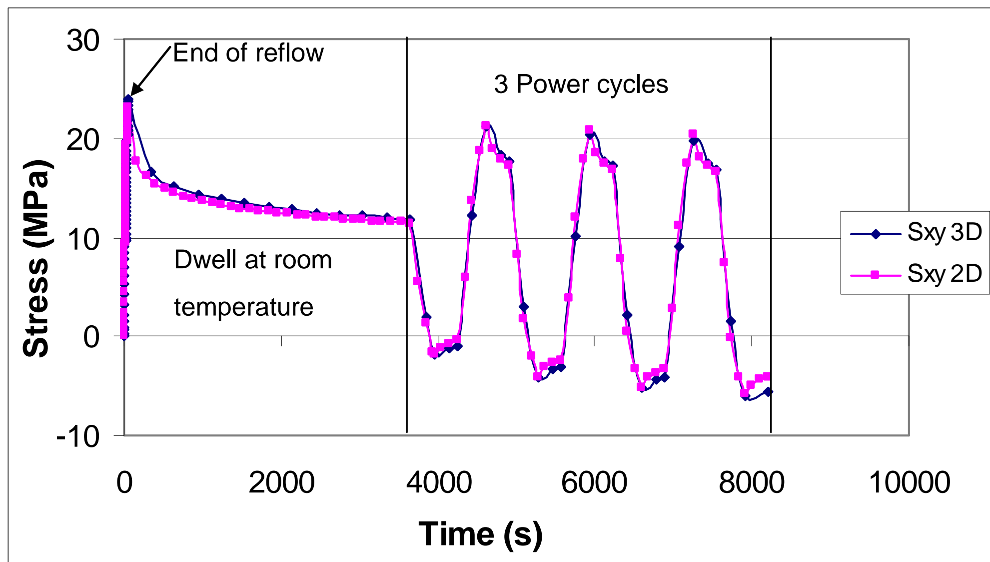
Figure 7



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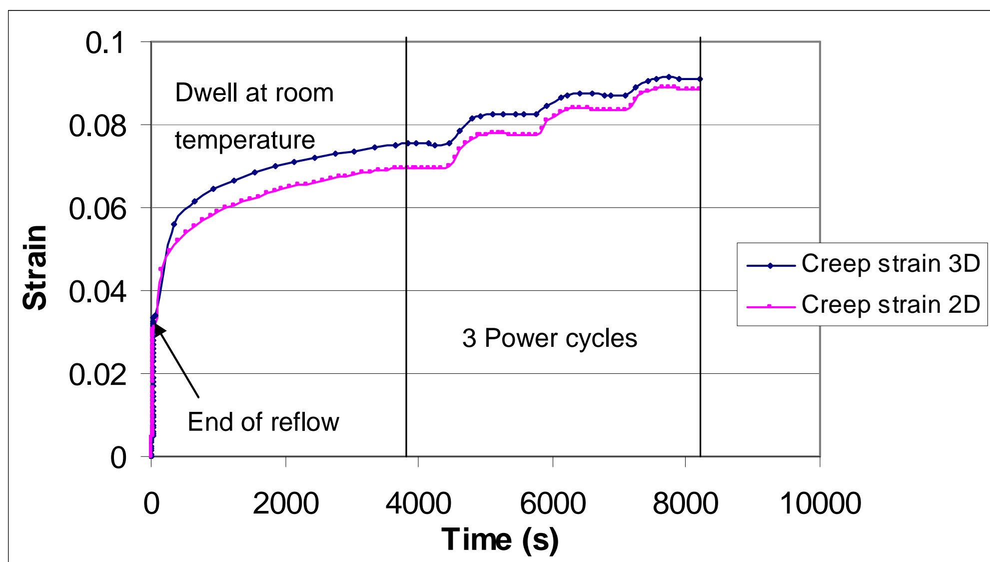
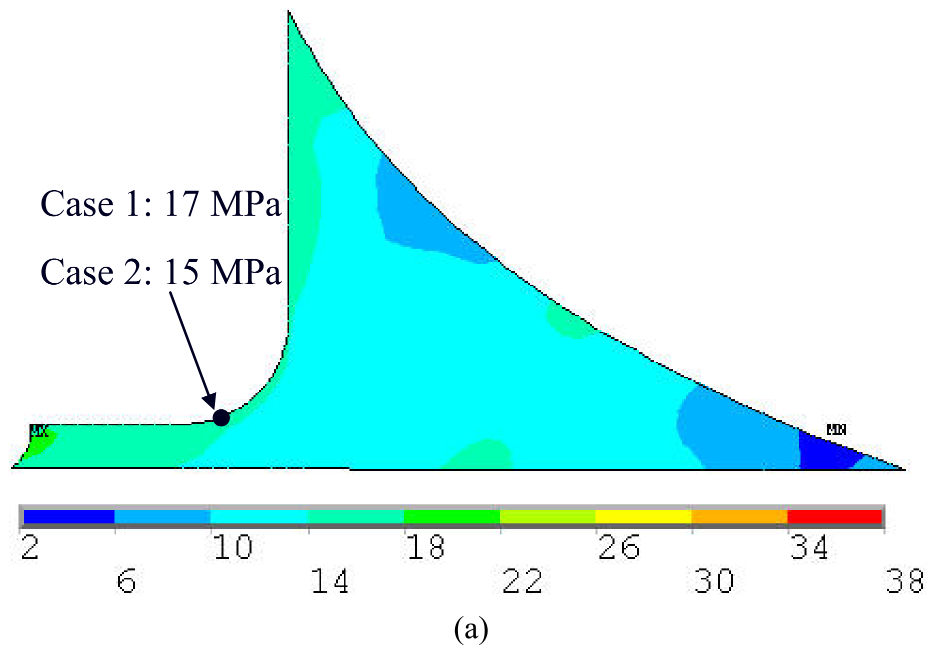
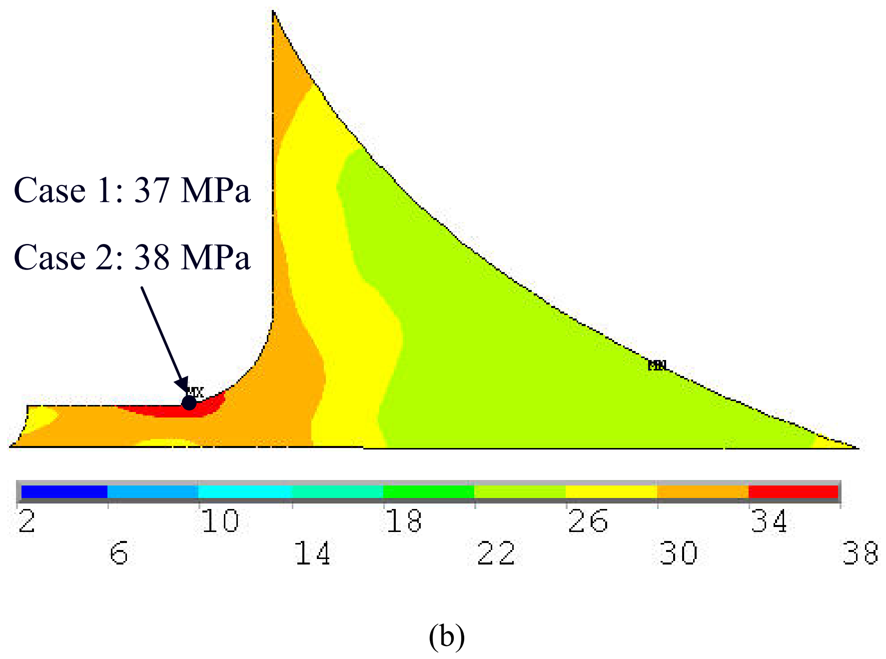


(b)

Figure 8

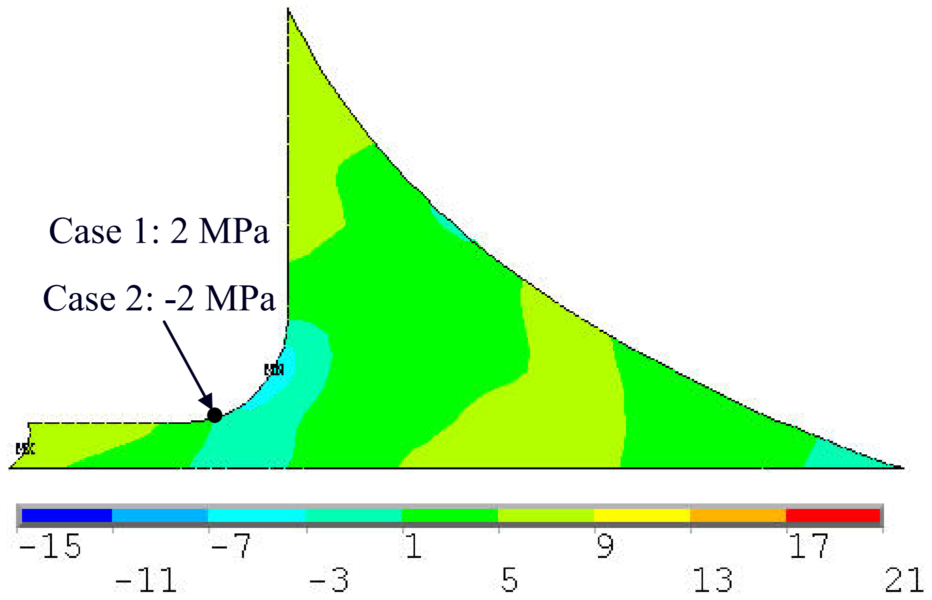


(a)

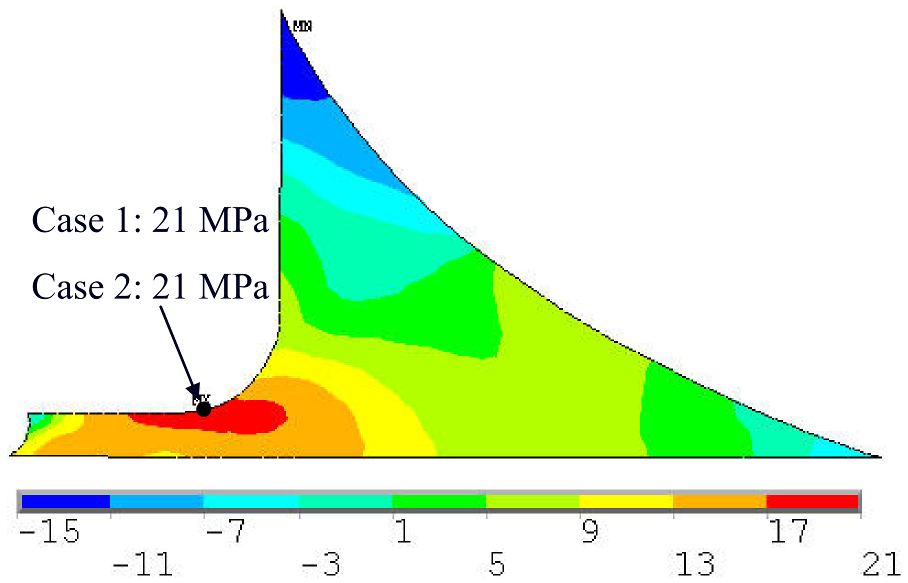


(b)

Figure 9



(a)



(b)

Figure 10

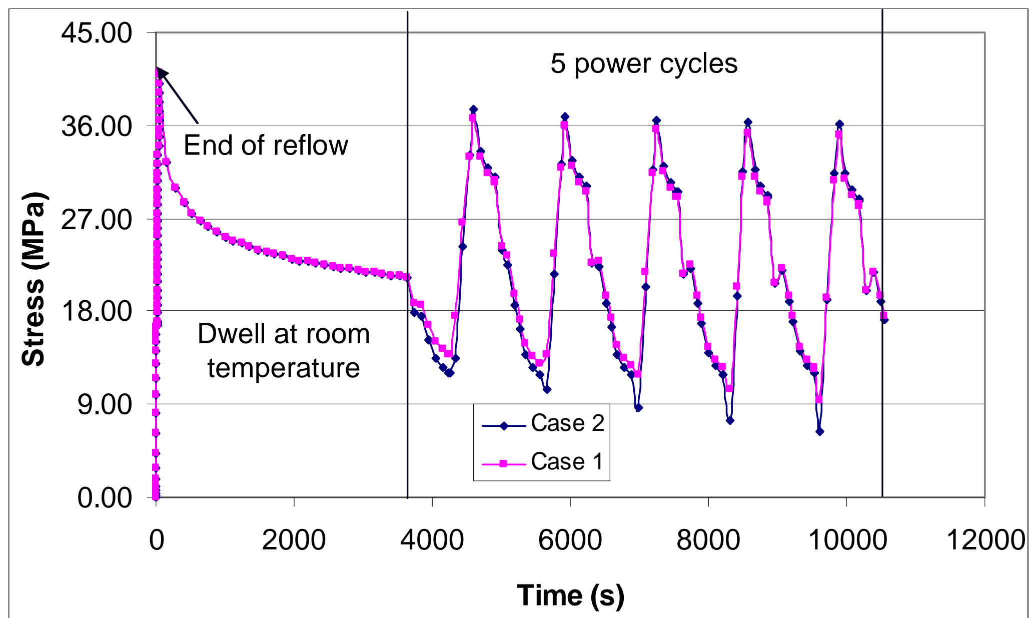


Figure 11

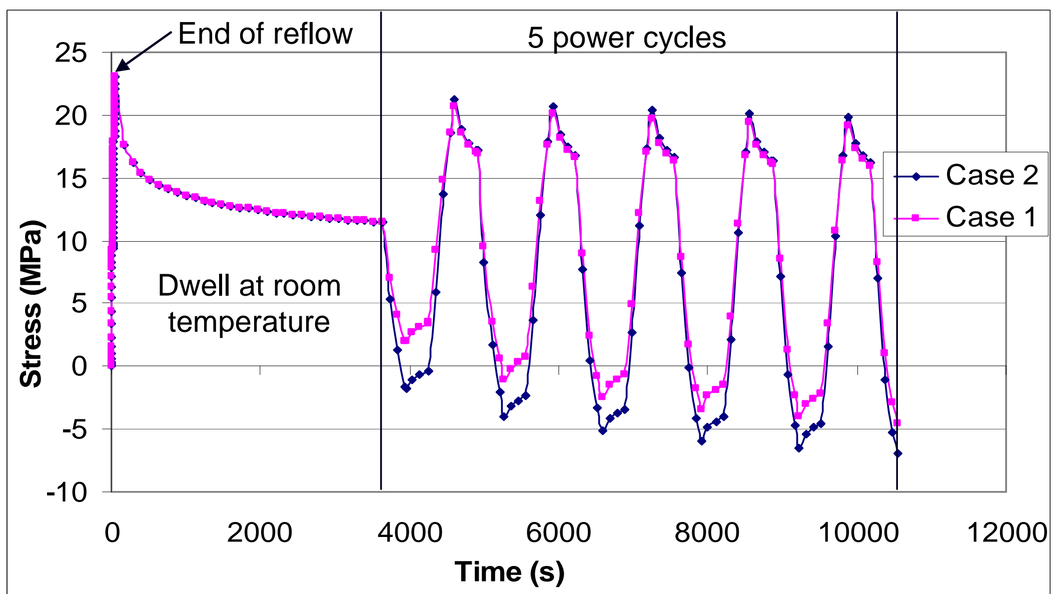


Figure 12

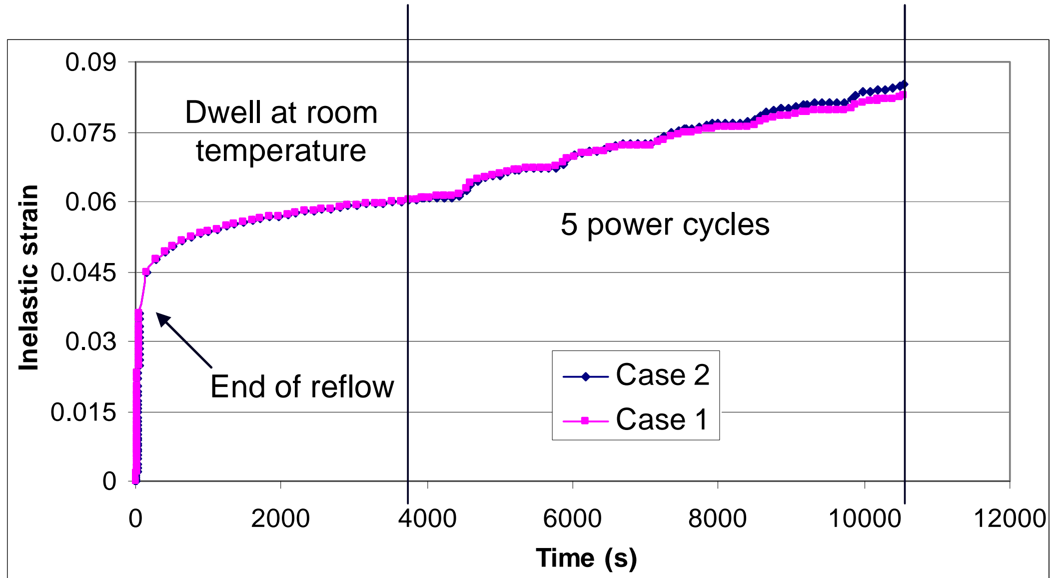


Figure 13