CORE

Metadata, citation and similar papers at core.ac.uk

Provided by Loughborough University Institutional Repository

This item was submitted to Loughborough's Institutional Repository (https://dspace.lboro.ac.uk/) by the author and is made available under the following Creative Commons Licence conditions.

COMMONS DEED

Attribution-NonCommercial-NoDerivs 2.5

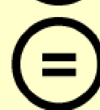
You are free:

- to copy, distribute, display, and perform the work

Under the following conditions:

Attribution. You must attribute the work in the manner specified by the author or licensor.

Noncommercial. You may not use this work for commercial purposes.



No Derivative Works. You may not alter, transform, or build upon this work.

- For any reuse or distribution, you must make clear to others the license terms of this work.
- Any of these conditions can be waived if you get permission from the copyright holder.

Your fair use and other rights are in no way affected by the above.

This is a human-readable summary of the Legal Code (the full license).

Disclaimer

For the full text of this licence, please go to:
http://creativecommons.org/licenses/by-nc-nd/2.5/

THERMAL DESIGN OF HIGH POWER SEMICONDUCTOR PACKAGES FOR AIRCRAFT ELECTRONIC SYSTEMS

Farhad Sarvar and **David C. Whalley**

Department of Manufacturing Engineering
Loughborough University, Loughborough, Leics
F.Sarvar@lboro.ac.uk, D.C.Whalley@lboro.ac.uk

ABSTRACT

The More Electric Aircraft is likely to require more extensive use of power electronics, for which thermal management will be a key issue. This paper will present an approach to designing integrated air cooled heatsinks which is being developed by Loughborough University as part of the CARAD funded Variable Frequency to Constant Frequency (VFCF) Converter project in collaboration with project partners TRW Aeronautical Systems, Mitel Semiconductor, AEA Technology and BAe Airbus.

The paper will show how simple models of the heat transfer from heatsink fins, which are based on well established empirical correlations, may be utilised in combination with either simple analytical models or two dimensional finite element models of the heat conduction from the semiconductor die through the multilayer package structure to the base of the fins. These models allow the generation of design curves which may be used to rapidly explore a wide range of design options before selecting potential designs for more detailed evaluation using 3D FE analysis.

In systems such as a VFCF convertor the semiconductor devices are switched at high frequency to ensure good input and output current waveforms. The power dissipated in the semiconductors, and therefore the heatsink weight, will however increase with the switching frequency, whereas the associated filtering components will be smaller and lighter at higher frequencies. The optimisation of the overall system weight therefore involves a tradeoff between the heatsinking and filtering requirements rather than just determining the optimum heatsink design for a specific power dissipation.

INTRODUCTION

Aircraft are increasingly using electronic systems to replace traditional mechanical and hydraulic systems in areas such as power conversion and actuation. In addition to the increased functionality and potential for weight saving that this offers there are a number of other drivers for the adoption of electronic systems such as reliability and serviceability. Such systems contain semiconductor devices such as Insulated Gate Bipolar Transistors (IGBTs) switching high currents and consequently having a high power dissipation. Because of the large size and weight of these systems and their high power dissipation such electronic systems may be inappropriate for installation in standard ARINC avionic electronic racking structures and application specific installation and cooling practices are having to be developed.

Power Semiconductor Package Structures

Traditional high power electronic applications, such as in locomotive traction control systems, are based on industry standard semiconductor package configurations. Heat is conducted from the semiconductor device through the various electrically conductive, dielectric and joining layers and then through a bolted interface into an air or water cooled heatsink. The bolted interface creates a significant resistance to heat-transfer and results in a large and heavy installation. In the example shown in figure 1 the die are soldered to a direct bonded copper (DBC) substrate which is in turn soldered to the package base. In air cooled applications the heatsink is typically extruded aluminium, although cast and fabricated heatsinks are increasingly being used in more demanding applications

An application specific package with an integrated heatsink has the potential to offer greatly reduced size and weight for more demanding applications. In an integrated heatsink design the heat is still conducted through various layers, which may be the same as those in a traditional package (although the opportunity exists to change or eliminate some of the layers), but the fins are attached directly to the package baseplate as

Authorized licensed use limited to: LOUGHBOROUGH UNIVERSITY. Downloaded on February 4, 2009 at 07:46 from IEEE Xplore. Restrictions apply.

is shown in figure 2. This type of structure offers the potential for substantial weight savings but the required finning will depend on both the use environment of the package and on the device power dissipation in the specific circuit design, so the device package will be application specific. In the package design discussed here the baseplate material chosen is an Aluminium/Silicon Carbide metal matrix composite (MMC) which has been developed to have a low density, low thermal expansion coefficient and high thermal conductivity [Young et.al., 1999].

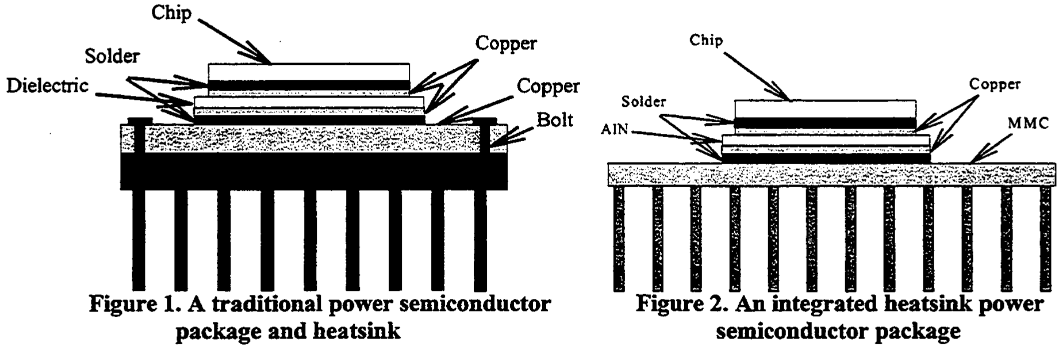


Figure 1. A traditional power semiconductor package and heatsink

Figure 2. An integrated heatsink power semiconductor package

FIN HEAT TRANSFER MODELLING

In the design of forced air cooling systems for electronic equipment such as computer workstations the air flow is unconstrained within the enclosure and complex 3D fluid flow models must be used to evaluate the air flow distribution within the enclosure and how it interacts with the individual semiconductor device heatsinks, e.g. [Rujano, 1998]. However, in the type of high power system being considered here, the cooling air flow will be ducted to the heatsink and therefore when designing the heatsink fins consideration need only be given to two things, i.e. the cooling fin dimensions must be selected to obtain sufficient cooling and at the same time the pressure drop through the fins must be kept to a level such that the required air flow can be supplied by the cooling air supply system. Simple empirical relationships have been derived by Scott [1974] for such ducted flow heat transfer, which can be used to greatly simplify the heatsink design process. The major simplifying assumptions made in deriving these correlations are that: the air flow is turbulent, that the ducts are narrow compared to their height above the base and that the fins are perfectly conducting. In spite of the approximate nature of the relationship, the equations are useful in estimating cooling capability for various potential fin degsins.

The temperature rise required to transfer a given amount of heat from the fins depends upon the velocity of the air moving past the fins, and the air velocity in turn depends on the fin geometry and dimensions and on the mass air flow rate. The temperature rise for the geometry of cooling fins shown in figure 3 is related to these variables by the following equation:

$$\frac{\Delta T_{fin-air}}{Q} = \frac{C_1 w}{n^{0.2} z^{0.2} f^{0.8} L} \quad (1)$$

Where $\Delta T_{fin-air}$ is the temperature rise of the fins above the air in the cooling ducts, C_1 is a constant depending on altitude and ambient temperature and Q is the total power being transferred, n and W are the number and width of ducts, z and L are the height and length of the fins and f is the total air flow.

The fin geometry and dimensions cannot be selected without considering their effect on the pressure required to force air through the fins. An approximate formula for estimating the pressure drop through cooling fins as a function of their dimensions is given below, Scott [1974]:

$$\Delta p \propto \frac{(\frac{f}{n})^2}{(wz)^2}[C_2 + 0.01\frac{L}{w}] \quad (2)$$

Where C_2 is a constant depending on altitude and ambient temperature and Δp the pressure drop through the fins.

Authorized licensed use limited to: LOUGHBOROUGH UNIVERSITY. Downloaded on February 4, 2009 at 07:46 from IEEE Xplore. Restrictions apply.

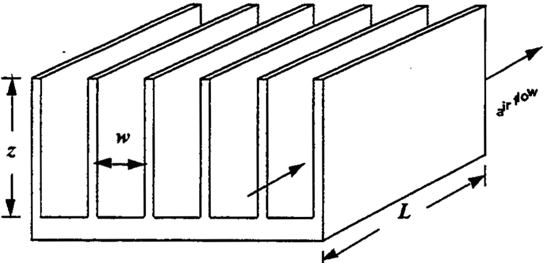


Figure 3 Diagram showing a typical plate fin heatsink

MODELLING OF CONDUCTION IN THE IGBT PACKAGE

A typical IGBT package will typically contain a number of individual IGBT devices plus their associated protection diodes. The exact temperatures of each device will therefore depend on the arrangement of the devices within the package. 3D modelling techniques are therefore necessary in order to evaluate the exact temperatures at which each die will operate at, but it is possible to estimate their temperatures fairly accurately using the highly simplified modelling approaches described in this section.

One-Dimensional Models

In structures encountered in electronic packages the area available for conduction along the thermal path is not normally uniform. Relationships have therefore been derived by, for example Ellison [1984], which allow calculation of thermal resistances in such cases. In this instance the thermal resistance, R, of an individual layer within the package is estimated by integrating the following expression:

$$R = \frac{1}{K}\int_0^L \frac{dx}{[t_1 + (t_2 - t_1)x/L][w_1 + (w_2 - w_1)x/L]} \quad (3)$$

Where t_1, w_1, t_2, and w_2 are the dimensions of the two faces of the layer, L is the layer thickness and K is the thermal conductivity of material.

The overall package thermal resistance can then be estimated by summing the individual layer thermal resistances. It is worth noting however that the one-dimensional representation of the heat flow using equation 3 only approximately represents the spreading of heat in the lateral direction, and some judgement must be used to decide how far spreading occurs through each of the layers of the package.

Two-Dimensional Conduction Models

The one-dimensional heat transfer models, although useful for a quick assessment of the design, are limited in their use as heat spreading within the different layers is only roughly approximated. It is also difficult to satisfactorily model transient situations. More detailed models are therefore required to carry out further analysis on potential designs and to study the effect of power transients on the die temperature. Two-dimensional axisymmetric FE models have therefore been developed which take into account conduction through the multilayer structure. Convective transfer to the environment from the base of the package is modelled using a uniform effective heat transfer coefficient which takes into account the effect of increased surface area due to the fins.

MODELLING CASE STUDY

A spreadsheet based analytical model of power semiconductor packages has been developed using the relationships given in previous section, thereby allowing a user to study the effects of different geometries, materials and air flow rates on the thermal performance. The spreadsheet model developed is divided into two sections. The first calculates the thermal resistances of each layer in the structure and uses these values to estimate the maximum allowable temperature at the base of the heatsink fins for the specified power and maximum junction temperature. The second part uses this information to calculate the fin height requirements. The number of fins and fin widths, etc. are parameterised so that the effect of different fin configurations can be studied. For each fin geometry, the pressure drop through the fins, and the weight and

Authorized licensed use limited to: LOUGHBOROUGH UNIVERSITY. Downloaded on February 4, 2009 at 07:46 from IEEE Xplore. Restrictions apply.

volume of the subsequent structure is also outputted in tabular and graphical form to allow the user to select the optimum design.

The spreadsheet program has been used to estimate the finning requirements for a proposed IGBT/heatsink structure. The total power dissipation is spread equally over a number of IGBTs and their maximum allowable continuous junction temperature is 125°C. The devices are mounted on the package baseplate using an alumina DBC substrate. The heatsink is assumed to be cooled by air at the worst case specified by ARINC-600, i.e. air at 70°C and with a flow rate of 220 kg/hr.kw and at an air pressure of 0.5 atmospheres. It is also assumed that the power is dissipated uniformly over the junction region on the top faces of the IGBTs.

Figure 4 shows how the required fin height to keep the maximum transistor junction temperature at 125°C varies as a function of switching frequency and for a number of possible fin geometries. Figure 5 is a plot of the resulting pressure drops through the fins as calculated from equation 3. Aircraft electronic systems are normally designed to meet the ARINC-600 [1987] specifications of a pressure drop of 50±30Pa at the specified air flow rate of 220 kg/hr.kw.

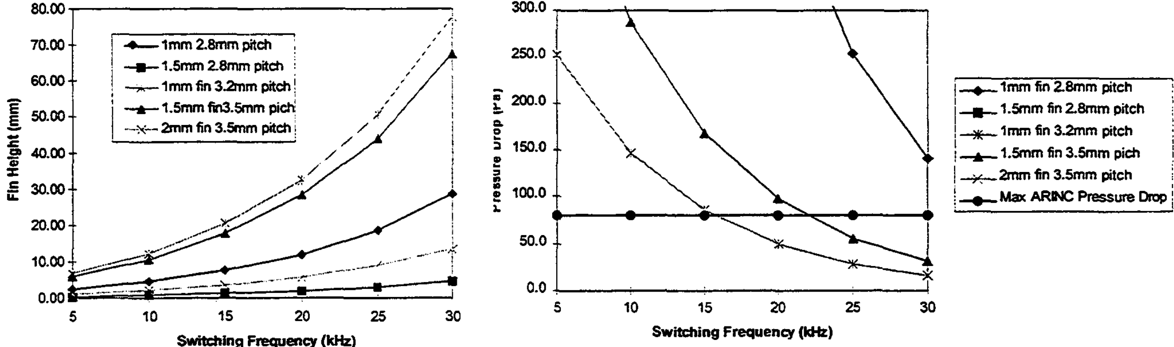


Figure 4. Fin height as a function of switching frequency and fin geometry

Figure 5. Pressure drop as a function of switching frequency and fin geometry

It can be seen from figure 6 that for this particular cooling system design, at switching frequencies above 15kHz only two of the chosen fin geometries satisfy the ARINC specification. The pressure drop axis has been limited to 300 Pa since for 2.8 mm pitch, 1.5 mm thick fins and 3.5mm pitch, 2mm thick fins, the pressure drop is far in excess of acceptable limits. Figures 5 and 6 clearly show that while a particular fin design may provide excellent heat transfer it may not be useable in practice due to the high pressure drop it will cause.

Axisymmetric models of similar structures have also been constructed. In this case the heat transfer coefficient calculated using the spreadsheet implementation of equation 1 was applied to the entire lower surface of the model. Figure 6 shows a contour map of the predicted steady state temperatures within this structure and, in this case, the predicted maximum junction temperature is 126°C in comparison with a maximum temperature of 125°C predicted using the analytical model. This model has also been used to perform transient simulations on package designs in order to evaluate the additional temperature rises occurring during potential overload conditions.

Figure 7 shows the predicted maximum junction temperature during a 5 second overload of approximately two times the normal, steady state, power dissipation. For this design the additional temperature rise of 50°C takes the peak junction temperature to well over the maximum allowable short term temperature of 150°C and design changes, such as the addition of further thermal mass, are being explored.

MODEL VERIFICATION

Two different designs of integrated heatsink module constructed by AEA Technology and Mitel were tested in a purpose built wind tunnel and the results compared with those from the spreadsheet model. The results are presented in table 1. For the 12 chip module the devices are well spaced out over the available baseplate area and the predicted temperatures are very close to the average temperature measured. For the 8 chip

Authorized licensed use limited to: LOUGHBOROUGH UNIVERSITY. Downloaded on February 4, 2009 at 07:46 from IEEE Xplore. Restrictions apply.

module however the devices are grouped closely together and the degree of heat spreading is therefore limited. There is therefore a greater difference between the predicted and measured temperatures.

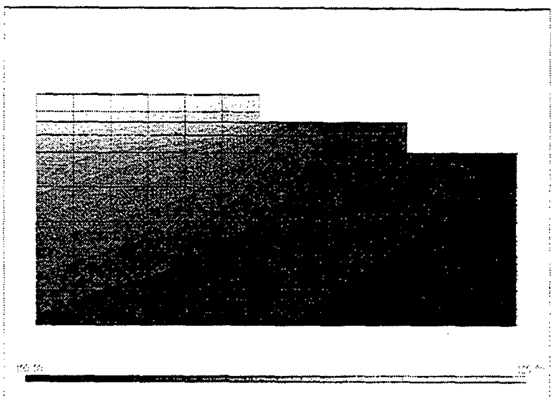


Figure 6. A contour map showing the steady state temperatures within the IGBT heatsink structure

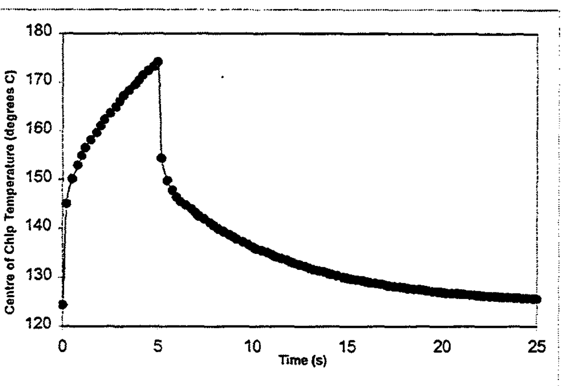


Figure 7. Predicted maximum junction temperature during a transient overload

CONCLUSIONS

It has been shown that simple analytical models can be effectively used to carry out rapid design studies on air cooled, high power electronics packages. The steady state results from these models compare favourably with those from wind tunnel testing on prototype modules. These analytical models do not however provide a detailed representation of the effects of package layout on individual device temperatures and more complex 3D models will be necessary in order to allow the detailed assessment of the effect of these factors on the actual junction temperatures achieved.

		Junction temperature (°C)	
		8 Chip Module	12 Chip Module
Measured	Max	80.3	72.6
	Min	74.3	65.7
	Avg	77.1	70.6
Predicted		74.9	71.5

Table 1. Comparison of measured and predicted junction temperatures

ACKNOWLEDGEMENTS

The authors acknowledge the financial support of the UK Department of Trade and Industry (DTI) under the More Electric Aircraft initiative of the Civil Aviation Research And Development program, and the financial and technical support of TRW Aeronautical Systems, Mitel Semiconductor, AEA Technology and BAe Airbus.

REFERENCES

ARINC Specification 600,1987, prepared by the Airlines Electronic Engineering Committee, Published by Aeronautical Radio Inc., Maryland.

Ellison G. N., 1984, "Thermal Computations for Electronic Equipment", Van Nostrand Reinhold Company, New York.

Rujano J. R. et. al, 1998, "Development of a Thermal Management Solution for a Ruggedized Pentium Based Notebook Computer", The Sixth Intersociety Conf. On Thermal and Thermomechanical Phenomena in electronic Systems, Itherm-98, Seattle, USA.

Scott A. W., 1974, "Cooling of Electronic Equipment", John Wiley & Sons, Inc, New York.

Young, R.M.K., Newcombe, D. and Sarvar, F., 1999, "Design Factors in Optimisation of IGBT Power Module Heatsinks", Power Conversion and Intelligent Motion Conference, June 22-24, Nuremberg

© 1999 The Institution of Electrical Engineers.
Printed and published by the IEE, Savoy Place, London WC2R 0BL, I

Authorized licensed use limited to: LOUGHBOROUGH UNIVERSITY. Downloaded on February 4, 2009 at 07:46 from IEEE Xplore. Restrictions apply.