Reflow Soldering Process Simulation: A Simplified Model

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Abstract

Established models of temperature development during reflow soldering have used general purpose, finite difference (FD) or computational fluid dynamics modelling tools to create detailed representations of both the product and the reflow furnace. Such models have been shown to achieve a high degree of accuracy, but are complex to generate and analysis times are long. With the move to adopt lead free soldering technology, and the consequently higher reflow process temperatures, optimisation of the reflow profile will gain a renewed emphasis. This paper will report a model of the process which uses simplified representations of both the product and the process which achieves an accuracy comparable with more detailed models. In order to establish an accurate representation of the specific reflow furnace being simulated, a reflow logger is used to make measurements of the temperature and level of thermal convection at each point along the length of the furnace for a small number of carefully chosen reflow profiles. The behaviour for any other reflow profile may then be extrapolated from these measurements.

1. INTRODUCTION

Reflow soldering is a non-equilibrium process in that the product temperature is never in thermal equilibrium with that of the heat source. The reflow furnace process settings must therefore be tailored to each individual product in order to ensure the optimum time/temperature profile for that particular PCB. The accelerating transition to lead free soldering processes will reduce the process window, requiring improved techniques for reflow profile optimisation.

The standard approach to reflow profile set-up has been to attach a number of thermocouples to an example of the product to be assembled, with the choice of thermocouple location being based on a combination of engineering judgement and experience. The product is then passed through the reflow furnace with a "first guess" set of process temperatures, while a data logger records the temperatures achieved. The initial process settings are then modified and the process repeated until the required time/temperature profile is obtained.

A computational model of the process has the potential to entirely eliminate this on-line set-up procedure through the construction of a detailed model of the product using the PCB CAD data, and could even be used to ensure the compatibility of a PCB design with the reflow process before it is released to manufacture. Such a model can also eliminate the risk that the chosen thermocouple locations do not cover the full spread of reflow profiles within the product, thereby ensuring that all solder joints on the assembly experience the correct process conditions. The feasibility of such models was demonstrated by Whalley et al. [1,2] and Sarvar and Conway [3] subsequently showed the high level of accuracy obtainable, provided accurate materials properties are available. Other approaches to simulation of the process has also been reported by e.g. Eftychiou et al. [4] and Kim et al. [5] who have developed two dimensional (2D) fluid flow models of the process and by Yu and Kivilahti who have developed a full 3D model of air flows within a furnace [6].

There are however a number of disadvantages to such modelling techniques. The principal of these disadvantages are the necessity of constructing a detailed physical description of the reflow furnace to be modelled and the long analysis time due to the large number of individual elements forming the model. The description of the reflow furnace has required detailed measurements of the geometry of each zone within the furnace and variations in the airflow velocities. The analysis time, even on a high performance workstation, is in the order of tens of minutes for even simple PCB designs, which is not compatible with algorithms designed to search for the optimum process settings, as these typically require a large number of iterations.

Whalley and Hyslop [7] reported a modified approach to the modelling of the reflow process, using a simple 2D model of the PCB assembly. This paper shows how the need to create a detailed physical description of the reflow furnace can be avoided in this type of model by using simple sensors to measure the furnace's heat transfer properties.

2. THE SIMPLIFIED SOLVER

The solver is based on a uniform rectilinear grid of elements in order to maintain simplicity, high execution speed and easy presentation of results. Each element contains a central node, to which all of the

thermal mass of that area of the assembly is assigned. The nodes are then interconnected by thermal conductances. It is assumed in the model that there is no variation in temperature through the thickness of the PCB or between the components and the underlying area of the PCB. If the time steps chosen are small enough that the boundary conditions and materials properties can be assumed to be constant over the time step, then the basic formulae to be solved at each node can be based on an explicit time integration approach and for each time iteration is:

$$T_{t+\Delta t} = T_t + \frac{Q}{C} \times \Delta t \quad (1)$$

where T is the nodal temperature (K), t is time (s), Δt is the time step (s), Q is the net heat flux into the node (W) and C is the heat capacity of the node (J/K).

The net heat flux into the node is the sum of the convective flux, F_C, and radiative flux, F_R, through the top and bottom surfaces, and the total conductive flux F_K from the four adjacent nodes, i.e.:

$$Q = F_C + F_R + F_K \quad (2)$$

The convective flux, F_c, at any location, x, within the furnace is given by:

$$F_C = (T_H(x) - T_t) \times H(x) \times SA \quad (3)$$

where T_H is the air/heater panel temperature (K), $H(x)$ is the convective constant for position x (W/m^2.K) and SA is the total surface area for the node (m^2).

The radiative flux, F_r, is given by:

$$F_R = (T_H(x)^4 - T_t^4) \times \varepsilon_H(x) \times \sigma \quad (4)$$

where $\varepsilon_H(x)$ is the effective average heater panel emissivity at position x, and σ is the radiation absorption constant for the node, i.e.:

$$\sigma = \varepsilon_E \times EA \times \varsigma \quad (5)$$

where ε_E is the effective average emissivity of the PCB assembly over the node, EA is the nodal plan area, and ς is the Stephan Boltzmann constant.

The solver is described in more detail in [8]. A programme to iteratively solve the above equations an to provide an animated graphical display of the predicted PCB temperatures has been implemented in C++. Input and output files use a comma separated variable (CSV) format for ease of export/import to/from other software such as spreadsheet programs.

3. GENERATION OF THE OVEN MODEL

A reflow furnace profile is often thought of as consisting of a number of zones of uniform temperature with step changes in temperature at the boundaries between zones as shown in Figure 1. Any real oven will however depart from this idealised view in a number of ways as is also shown in Figure 1. Firstly, there will be some degree of error between the oven set points and the actual heater panel temperature. There may also be some variation in heater panel temperature within a zone and the zones will interact to some extent, meaning that the transition from one zone to the next is not instantaneous. The sharpness of this transition between zones is dependant on various factors such as the tunnel height and the details of the air flow velocities. There are also areas of the furnace that are not under active temperature control, typically gaps between zones used for conveyor supports and the entrance and exit areas, which nevertheless may be significant to the overall reflow profile. A method to determine the real process temperatures as a function of the process recipe must therefore be established.

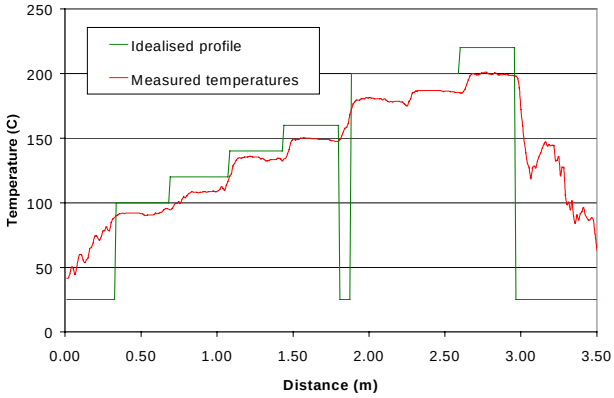

Figure 1. Comparison of an idealised furnace temperature profile with measurement

The oven model used in the solver consists of a set of the three parameters, heater/air temperature, T_H, heater emissivity, ε_H, and convection coefficient, H, at closely spaced intervals along the length of the conveyor (it is assumed that there is no variation in these parameters across the width of the conveyor). A method is therefore also required to measure H and ε_H, which generally will not change significantly from recipe to recipe, as well as to predict the parameters T_H for any recipe. The following section describes a procedure for deriving these parameters from measurements made using a calibration artefact, which is passed through the reflow process using a small number of carefully chosen recipes.

3.1. Equations for the calibration artefact temperature response

Any temperature sensor used to derive the required information will have a thermal mass, C, and will absorb heat at a rate Q. Assuming that the sensor is constructed such that there is no significant conductive heat flow to/from it and that it is thermally conductive enough that there is a negligible internal temperature gradient, then the rate of change of temperature, dT_s/dt, recorded by the sensor will be:

$$\frac{dT_s}{dt} = \frac{Q}{C} \quad (6)$$

The total heat flux, Q, is a combination of radiative and convective fluxes and will depend on the difference in temperature between the sensor and the

oven, the sensor area, the emissivity of both the sensor and of the oven components, and the convective heat transfer co-efficient between the oven atmosphere and the sensor:

$$Q = Q_C + Q_R \quad (7)$$

where, Q_C is the convective flux:

$$Q_C = (T_H - T_s) \times H \times A_s \quad (8)$$

where, T_H is the heater temperature, H is the convection coefficient and A_s is the sensor surface area.

And Q_R is the radiative flux:

$$Q_R = ({T_H}^4 - {T_s}^4) \times \varepsilon_H \times \varepsilon_s \times \zeta \times A_s \quad (9)$$

where ε_s is the sensor emissivity.

Combining equations 6 to 9 the overall temperature response of the sensor is therefore:

$$\frac{dT_s}{dt} = \frac{A_s \times [(T_H - T_s) \times H + ({T_H}^4 - {T_s}^4) \times \varepsilon_H \times \varepsilon_s \times \zeta]}{C} \quad (10)$$

If an appropriately designed sensor, which is well characterised for its thermal mass, area and emissivity, is used to measure T_s and dT_s/dt at three different temperature settings for each oven zone, then the three unknowns in equation 10, T_H, H and ε_H, should in principal be obtainable by assembling and solving a set of three simultaneous equations. However this approach, in addition to the complexity of solving these equations, is likely to require large changes in the oven set points in order to isolate the radiative heat transfer from the convective and would also make it more difficult to isolate interactions between adjacent zone set points during the transition between zones. A minimum of four, and possibly more, separate runs would therefore be necessary in order to fully characterise the process.

An alternative approach is to use three sensors, each with a different combination of C, A_s and ε with which the three parameters could be derived with only one run through the furnace. To simplify data analysis the three sensors could be chosen so that they each have a different combination of extreme values for their C and ε parameters, i.e.:

Sensor 1: Low C, high ε

Sensor 2: High C, high ε

Sensor 3: High C, low ε

Sensor 1 would closely track the oven air temperature, directly providing T_H, whilst the data from sensor 3 would, in combination with T_H, provide the H data by solving a version of equation 10 with the radiative term removed, i.e.:

$$\frac{dT_s}{dt} = \frac{(T_H - T_s) \times H \times A_s}{C} \quad (11)$$

The oven emissivity could then be obtained by solving equation 10 using the data obtained from sensor 2.

The disadvantage with this approach is the more complex sensor set-up and the number of data logger channels used, reducing the opportunity for measuring differences side to side and top to bottom within the oven.

Further runs through the oven for different process settings would then allow the relationship between the set-points and the effective heater temperature to be established as is explained in the next section.

3.2. Prediction of T_H as a function of x for any process recipe

Assuming that the oven emissivity does not vary significantly with the process settings, and that the convection coefficient also does not vary significantly, unless specifically controllable by a fan speed controller, then the values for them derived from the artefact should be directly usable for any process recipe. The T_H however will have to be predicted for any recipe not used for the calibration process. The calibration process will therefore have to be able to extract enough data to predict for every location *x* in the oven the relationship between $T_H(x)$ and the set points for the current and the nearest adjacent zones. This will have to also include "passive" zones, i.e. areas of the oven not within a controlled zone, but which will contribute to heat transfer. As noted earlier this includes gaps between zones, for example for conveyor supports, and the entrance and exit tunnels.

Rather than attempt to apply any more detailed knowledge of the design of the oven than is typically captured within reflow data logger software, i.e. the starting point and length of each zone, it is assumed that the influence of each zone extends half way into the next zone, except for the first and last (controllable) zones, whose influence are assumed to extend to the ends of the furnace tunnel. For two typical zones, Z_n & Z_{n+1}, with set points of SP_n and SP_{n+1} and which extend from x_n to x_{n+1} and x_{n+1} to x_{n+2} respectively, then T_H would be calculated as a function of SP_n and SP_{n+1} between $(x_n + x_{n+1} / 2)$ and $(x_{n+1} + x_{n+2}/ 2)$. At the extremes of this range it is expected that T_H would be almost entirely (linearly) dependent on the set point of one zone, but there may be differences in both scale and offset between the two, i.e.:

$$T_H(x_n + x_{n+1} / 2) = a \times SP_n + b \quad (12)$$

and

$$T_H(x_{n+1} + x_{n+2} / 2) = c \times SP_{n+1} + d \quad (13)$$

where a, b, c and d are the scale and offset errors for each zone.

For any point between these two extremes T_H would be a function of both set points i.e.:

$$T_H(x) = e(a \times SP_n + b) + (1 - e) \times (c \times SP_{n+1} + d) \quad (14)$$

where e is the proportionate contribution to T_H from the two zone temperatures.

However equation 14 can be reduced to:

$$T_H(x) = f \times SP_n + g \times SP_{n+1} + h \qquad (15)$$

where the constants f, g and h must be obtained from at least three runs through the oven for different combinations of SP_n and SP_{n+1} (although for some well calibrated ovens h may be very small).

If the oven has zones for which the level of convection is controllable, then this process will have to be extended to include a prediction of H at each location. Additional calibration runs would probably have to be made to capture this data.

3.3. Artefact construction and trials

For the purposes of testing the furnace calibration process described above, a calibration artefact was created based on a commercially available data logger carrier frame. This artefact consisted of a bare thermocouple projecting forward from the frame to act as sensor 1 and two further thermocouples attached to 18mm diameter nickel alloy disks to act as sensors 2 and 3. One of these disks (sensor 2) was given a matt black coating to give a high emissivity and the other (sensor 3) was polished to give a low emissivity. These sensors were supported only by the thermocouple wires, so there was negligible conductive heat transfer to/from them. This artefact was run through a Quad QRS7 furnace a total of four times, using the recipes listed in table 1. Figure 2 shows the measured T_H values for recipes A, B and C, and Figure 3 shows a comparison of the predicted values of T_H for recipe D with those measured. These results show that a reasonably good prediction of the T_H values can be obtained.

Zone Number	Recipe name/temperatures (°C)			
	A	B	C	D
1	100	100	80	90
2	120	100	100	120
3	140	140	120	150
4	160	140	140	150
5	200	200	180	190
6	200	180	180	200
7	220	220	200	230

Table 1. Process recipes used for the trials

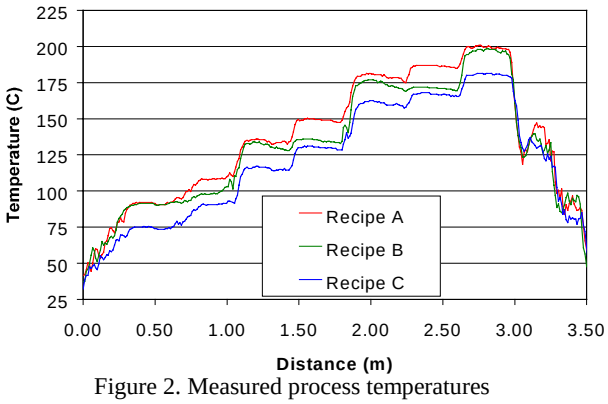

Figure 2. Measured process temperatures

Figure 4 shows the measured air temperatures and convection sensor (sensor 3) temperatures along the furnace length for recipe B. It was found that the values of convective heat transfer coefficient calculated using equation 10 appeared very noisy. This was initially believed to be primarily due to a combination of noise in the temperature measurements and their resolution. Averaging of the H values over several seconds reduced this noise, however comparison of the H values calculated from three runs through the furnace showed that the remaining "noise" was fairly repeatable from run to run and is therefore concluded to be due to real spatial fluctuations of the air flows within the furnace. Figure 5 shows calculated values for H including averaging.

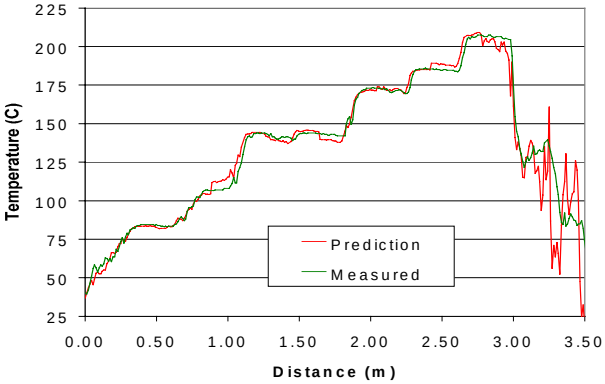

Figure 3. Comparison of measured and predicted process temperatures for recipe D

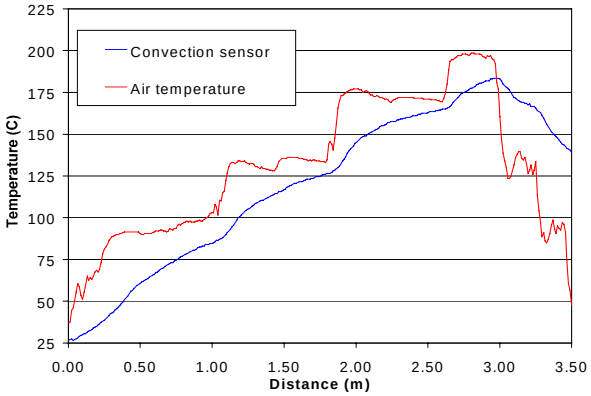

Figure 4. H sensor temperature measurements

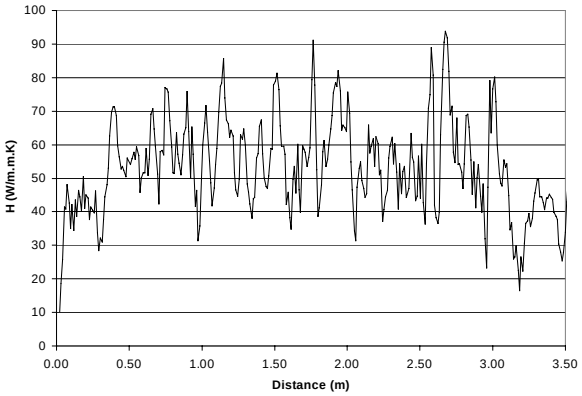

Figure 5. H values calculated from sensor data

Although a difference in temperature between sensors 2 and 3 could be observed, the extraction of oven emissivity data is based on the relative slopes of these two curves, which differ only slightly. The resulting calculated emissivity values were therefore so noisy that even after significant averaging they were not useful. In fact the calculated values fluctuated below 0 and above 1, which is clearly not realistic.

4. GENERATION OF THE PRODUCT DESCRIPTION

The data required for each thermal node within the product model are its effective in-plane conductivity, both in the X and Y directions, its thermal mass, average emissivity, and the convection area. Where there are no components these are straightforward to calculate, but where an area of the PCB is populated with components, calculation of the nodal properties is slightly more complex and the following modifications to the bare PCB properties must be made:

Conductivity: Components much smaller than the element size, such as ceramic chip capacitors and resistors, will have little effect on conductivity and can be safely ignored. Larger components, particularly those with a metal lead-frame, will however have a significant effect on the local in-plane thermal conductivity. An effective thermal conductivity was therefore calculated for each of the IC packages, taking into account the relative thickness of the lead-frame and package body. The thermal conductivity of each node under an IC was then modified taking into account the proportion of its area covered by the IC.

Thermal mass: The additional thermal mass of an individual component is the product of its volume, density and SHC and the total thermal mass of a node is therefore the sum of the PCB thermal mass and the individual component thermal masses. The components were however weighed so their volume and density did not have to be measured. Any component lying on the boundary of two or more elements was simply split between them in proportion to the component area within each element.

Emissivity: As noted in the previous section an accurate calculation of the effective emissivity of a node is quite complex. In most modern reflow ovens only a small proportion of the heat transfer is by radiative heat transfer and obtaining a precise value for the emissivity is therefore less important. Based on this it was decided to simply calculate nodal emissivity based on the (plan) area weighted average of the emissivities of the materials present within an element.

Convection area: The addition of components to a thermal node will increase the total surface area available to convective heat transfer. If the components sit close to the PCB, then there will be little airflow under the components and it can be assumed that the bottom of the component and the area of PCB underneath it only play a small part in convective heat transfer. The additional convection area due to a component is therefore only the area of its sides, i.e. the component height multiplied by the length of its perimeter. Where a component overlies an element border this additional surface area is split between the elements as for its thermal mass.

4.1. The test PCB

Figure 6 shows the test board used to test the model, which is about 20cm by 15cm and has a total of 37 components, including one 44 pin PLCC, and a mix of SO and chip components. In order to test the model a relatively coarse mesh of 20 by 15 elements was used, resulting in a total of 300 thermal nodes. Ideally the product description would be generated directly from the CAD data, but in order to test the new modeling approach this data was generated for an existing test PCB design using a spreadsheet.

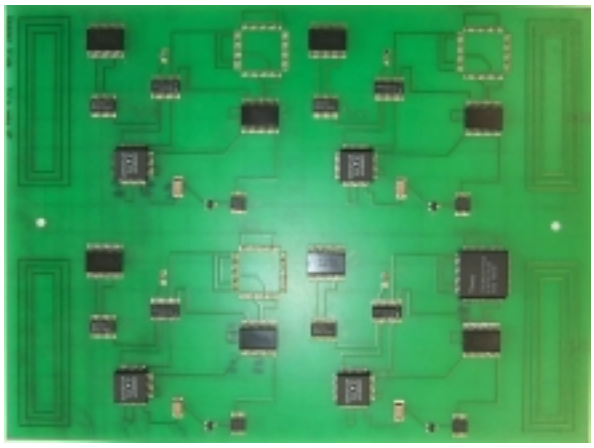

Figure 6. The test PCB

5. RESULTS

5.1. Experimental data acquisition

A sample of the test board shown in Figure 6 had thermocouples attached to an 1812 capacitor, a 20 pin SOIC, a 28 pin PLCC and to both the corner and centre of the 44 pin PLCC. To reduce thermal degradation of the test board, and any consequent changes in its thermal properties, the reflow furnace was set to a slightly cooler profile than would typically be used in production.

5.2. Modelling results

The model was run using the measured H data as presented in Figure 5, together with the predicted temperature/distance profile shown in Figure 3. Figure 8 shows the predicted distribution of temperatures in the PCB at a particular instant in time during the reflow process, and Figures 9 and 10 show a comparison of the predicted and measured time/temperature profiles for the five thermocouple locations. From figures 9 and 10 it can be seen that there is excellent agreement between the model and

experimental results throughout the entire reflow process. The average difference in peak temperature between model and experiment was 3.5°C and the maximum difference was less than 5°C. The analysis time was 0.44s on a 300MHz Intel Pentium processor with 64MB of RAM.

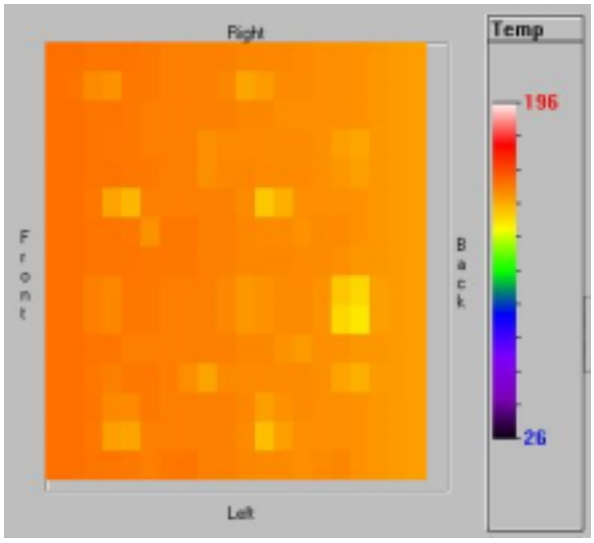

Figure 8. Predicted PCB temperature distribution

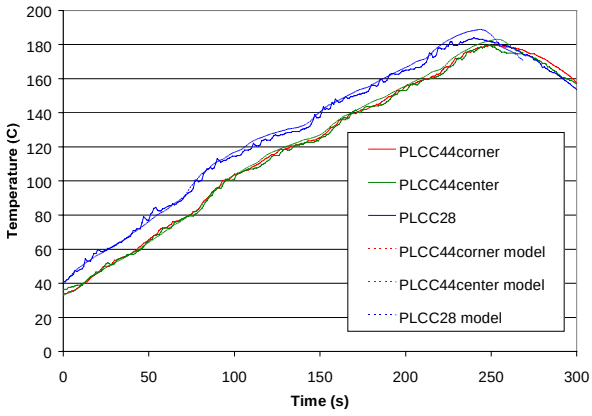

Figure 9. Comparison of measured and predicted temperature profiles for the QFP components

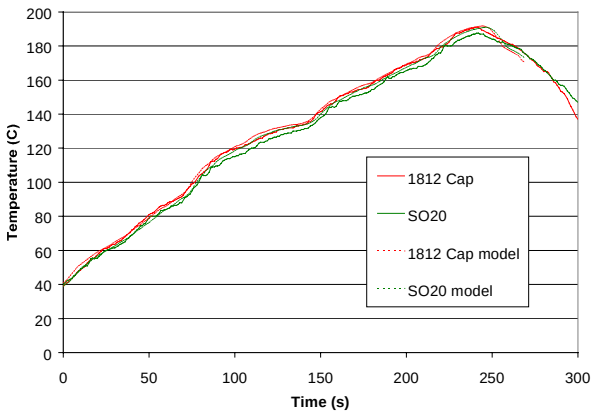

Figure 10. Comparison of measured and predicted temperature profiles for the 1812 capacitor and SOIC

6. CONCLUSIONS

It has been demonstrated that a very simple model of the reflow soldering process can provide extremely accurate predictions of the reflow profile for a given set of process settings. In this simulation process measurements are used to create a model which can predict the temperature at any point within the reflow furnace as a function of the process settings. These temperatures are then used as boundary conditions for a 2D model of the circuit board to be processed. This modelling approach greatly reduces the time required to create and run the simulation compared with models where boundary conditions are established from detailed process equipment geometry and either measurements or CFD predictions of the airflow velocities. Further work is required to test the limits of accuracy of the approach developed, both for other soldering furnaces, particularly those where heat transfer is IR dominant, and also for more complex PCB assemblies. In addition to its use in process optimisation during the new product introduction process, the modelling approach is simple enough to use during the PCB design stage to ensure compatibility of the design with available process hardware.

The process data acquisition and modelling approach described here is probably also applicable to other thermal processes where significant variations in product thermal mass require product specific process optimisation, such as in paint curing, ceramic kilning processes and in the food processing industry.

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