Reliability assessment of a digital electronic board assembly using the physics-of-failure approach: a case study

C N Oguibe and **D J Williams***
Department of Manufacturing Engineering, Loughborough University, UK

Abstract: An independent study has been carried out to assess the extent to which the physics-of-failure (PoF) technique can help in reliability enhancement and assessment of electronic assemblies. In particular, a specific case study has been conducted on a real, digital electronic board assembly with known failure modes. Results from the study include the simulation of substrate and component temperatures based on the knowledge of component power dissipation, board assembly materials and cooling methods of the board assembly. The fundamental frequencies and dynamic displacements of the board were computed from the vibration models. The thermal and vibration results were then used to model the damage accumulation at solder joints of the components to accurately predict failure trends and failure sites. These results are compared with field failure data and results from other computer aided engineering (CAE) tools.

Keywords: physics-of-failure method, reliability enhancement, fatigue life cycle, electronic assemblies, solder joint

1 INTRODUCTION

For many years, the defence and aircraft electronics industries have relied on military standardization when acquiring systems and equipment, requiring that electronic equipment contractors use mil-spec components rather than best commercial practices. The design and reliability practices embodied by these standards were often not firmly based on engineering science or physics. They created a need for costly test, analyse and fix programmes in order to ensure that reliability requirements were met, and inhibited the use of state-of-the-art, low-cost components. They were considered the best practices when they were developed many years ago but, today, the standards are outmatched by the rate at which product technology together with modelling and simulation is advancing. Also, the declining market in military and high-value electronic components and targets for reduced development periods of components mean that the emphasis on testing programmes with little engineering content is no longer affordable. Modern reliability technologies which use modelling and simulation and are based upon engineering science and physics offer distinct advantages in this regard.

One such reliability modelling technique is the physics-of-failure (PoF) method. The method helps to predict and evaluate potential failure causes, locate failure sites and evaluate their impact during the life cycle of an electronic product or its elements. It can also help to create an understanding of the effect of material properties on failure mechanisms through physically and scientifically informed models. These models, when used judiciously, would allow failure rates to the field failures to be estimated based on test conditions, design, material properties, geometric boundaries and across different technologies.

Recent investigations [**1**, **2**] have led to the development of a PoF-based reliability assessment tool, calcePWA, which can be used by engineers involved in the reliability of electronic parts. The calcePWA, developed by the Computer Aided Life Cycle Engineering (CALCE) Electronics Packaging Research Group of the University of Maryland, USA, is a simple and easy-to-use integrated, PoF-based reliability assessment tool. It has been developed to be a proactive design tool that allows the user to assess the

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**Corresponding author: Department of Manufacturing Engineering, Loughborough University, Loughborough, Leicestershire LE11 3TU, UK.*

thermomechanical integrity of a printed circuit board (PCB), and provides for four major analyses areas, namely thermal, vibration, fatigue and shock.

The thermal analysis module of the tool uses a three-dimensional finite difference approach to compute the temperature distribution within a PCB assembly, based on heat input and cooling design. The vibration analysis module uses the finite element technique to compute the first three natural frequencies, mode shapes and dynamic displacements of a PCB assembly. The shock analysis module, on the other hand, provides an ability to make multiple shock assessments of a PCB in order to determine whether a part attachment will survive in a shock environment.

As part of an industrially led reliability programme, a case study was conducted on a real, representative digital electronic board assembly using the PoF technique. The purpose of the study has been to assess the extent to which the PoF technique helps in the reliability assessment of electronic products through the simulation of thermomechanical failure mechanisms and prediction of life cycles of the board assembly. This paper discusses the modelling and analysis activities involved in the reliability assessment of the digital electronic board assembly. The results from the various simulation models, including those from the damage accumulation, are presented and are compared with field failure data and, where possible, with results from other computer aided engineering (CAE) tools. The concluding section describes the findings of the study and points out the benefits and limitations of using such a reliability modelling approach.

2 CASE STUDY

The study attempts to demonstrate how the PoF modelling technique can help in reliability assessment and enhancement of electronic assemblies. It was carried out for a consortium of UK-based industry partners who wished to understand the value of the approach. The simulation models are based on PoF deterministic models and first-order approximations of the life cycles of the PCB captured within the calcePWA tool.

The PCB assembly utilized in the study is an aerospace central processing unit (CPU) board assembly that is mounted between an analogue and a power supply board inside a digital electronics module (DEM). The CPU board assembly itself consists of seven layers of non-conductive material (FR4) with each layer sandwiched between 35 μm conductive layers and 28 devices mounted on a single side of the board. Details of the board configuration are shown in Figs 1 and 2 .

3 MODELLING METHOD

The most important aspect of the modelling is the construction of thermal and vibration models that act as input to solder joint failure models. The outputs of the failure models are then validated against field values. This process allows a judgement to be made on the value of the approach.

3.1 Thermal analysis

Thermal simulation was conducted to determine the temperature distribution through the board and to assess the effectiveness of the cooling design. The thermal model uses a finite difference approach to compute temperature distributions within printed circuit boards based on heat input and cooling design. The inputs to the thermal model include component, board and cooling data such as package dimensions, power dissipation, junction-to-case thermal resistance and material properties, all taken from the assembly's specifications. The outputs include node temperatures for each layer of the assembly.

There is no specific cooling method specified for the board in application. However, the mounting of the board inside the DEM shows that the board is cooled by conduction and natural convection on the top and bottom planar surfaces of the board (see Fig. 1). Based on this, heat conduction with a natural convection thermal model was constructed with the three sides of the board kept at an initial temperature condition equivalent to the applied ambient temperature. The top was insulated with a convection path gap of 2.54 mm.

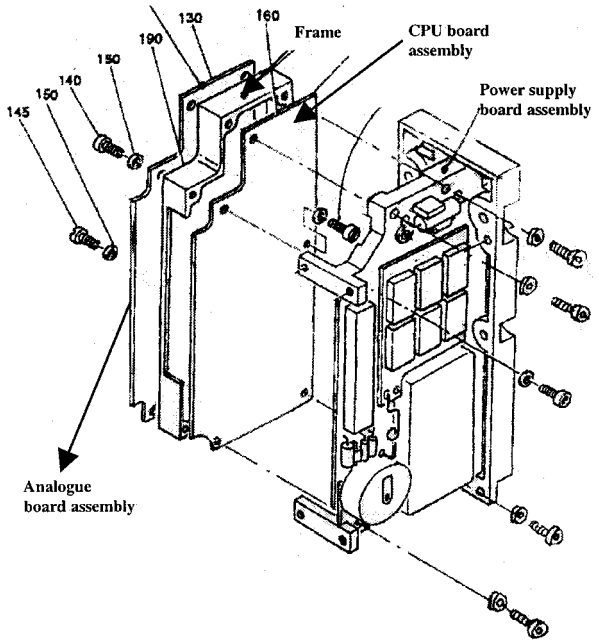

Fig. 1 The actuator digital electronics module (DEM) showing the board assemblies

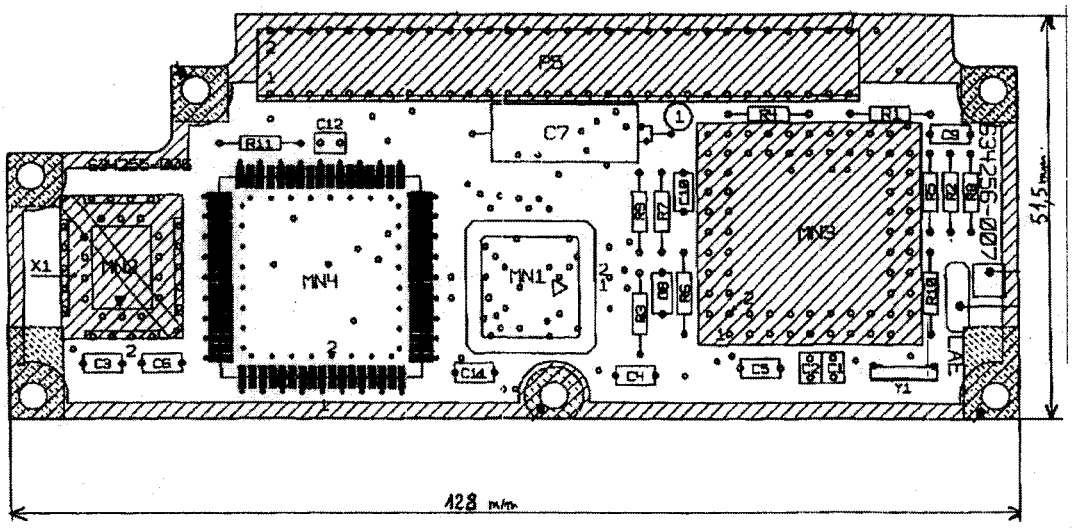

Fig. 2 Schematic layout of the CPU board assembly

The convection heat transfer coefficients are computed using the Bar Cohen and Rohsenow models [**3**]. The boundary conditions at the top and bottom planar surfaces of the board are defined based on an energy balance and Newton's law of cooling. Component case and junction temperatures are calculated using thermal resistance networks, by first calculating the substrate temperature directly below the component and then using the following equations:

$$T_c = T_s + qR_{cs} \qquad \text{and} \qquad T_j = T_c + qR_{jc} \tag{1}$$

where T_c, T_j and T_s are the case, junction and board surface temperatures respectively directly below the component and q is the heat dissipated by the component. R_{cs} and R_{jc} are the thermal resistance between the case and the substrate and between the junction and case defined as functions of component area, conductivity of the specified interface material, interface material distance and thermal resistance of leads.

Heat inputs on to the top and bottom surfaces of the board are based on the grid size, component actual power specifications, component positions and component sizes. From these initial conditions, the thermal analysis was conducted to compute the junction, case and board temperatures for each component and board location. Figure 3 shows the thermal boundary conditions.

3.2 Vibration analysis

The vibration analysis computes the fundamental mode shapes, dynamic displacement response and frequencies of the board. The vibration analysis involves creating a board model, setting the boundary conditions, specifying the input load and calculating the modal damping ratios.

The calcePWA vibration module uses a simplified finite element (FE) technique to determine the board

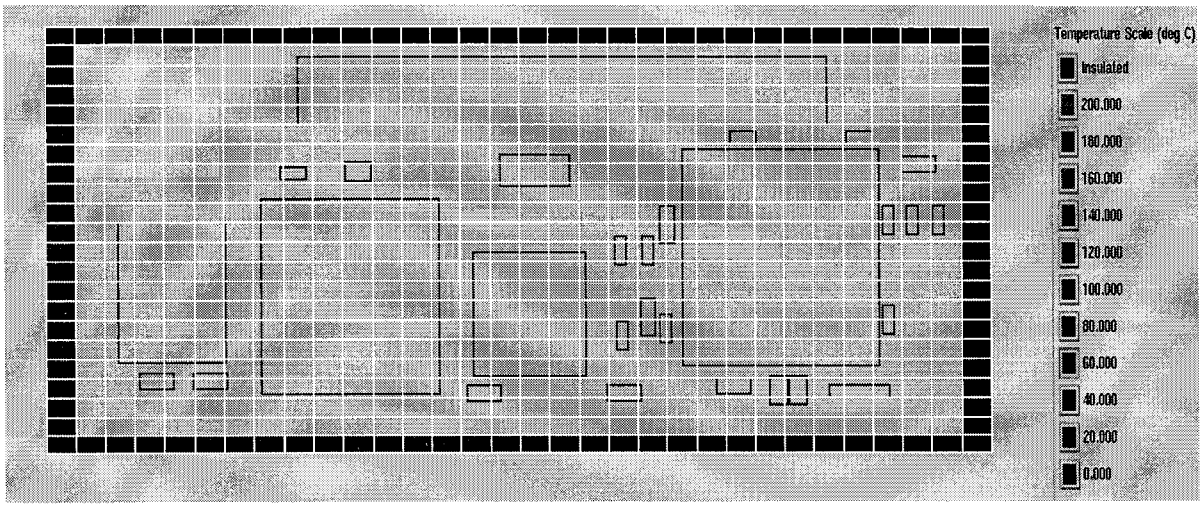

Fig. 3 Boundary conditions applied to the thermal model

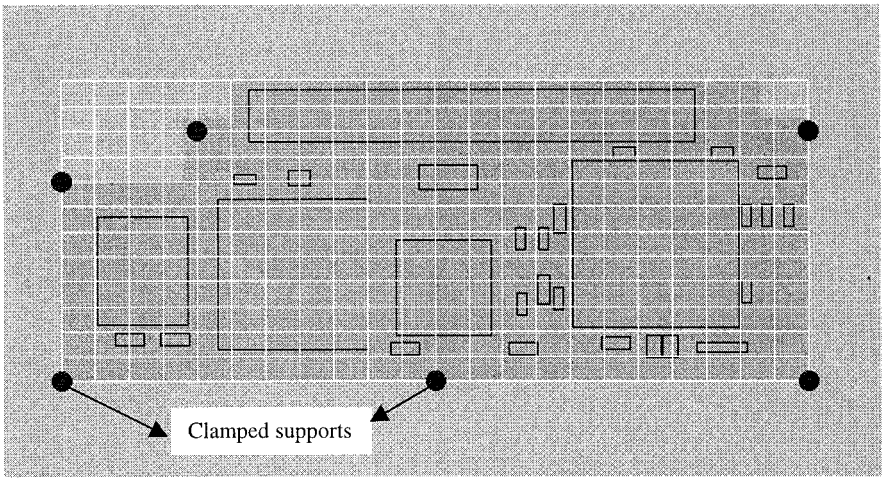

Fig. 4 Vibration boundary conditions

dynamic response to vibration mode—harmonic or random. The module treats the PCB as a flat plate and implicitly ignores component weights and positions. However, it is possible to consider the effect of components on the vibration response by modelling the components as stiffeners and by calculating an effective elastic modulus for each of the respective elements associated with each component. The modified Kirchoff plate element with three degrees of freedom (out-of-plane displacement and rotations about the orthogonal axes in the plane of the board) is implemented. Multilayer construction of PCBs is accounted for by using the laminate plate theory, which accounts for the bending stiffness of the plate.

The calcePWA tool provides for classical boundary conditions (simple and clamped) at a point as well as along any portion of an edge. In addition to the classical supports, the software provides for wedge lock supports that provide support somewhere between clamped and simple supports to model edge guides and connectors that behave differently from classical supports [**4**].

For the present analysis, random vibration was specified since experience and tests have shown that random vibration more closely represents the true environment in which the electronic equipment operates. The basic failure modes associated with this mode of vibration include high acceleration levels that would affect the operation of relays and crystal oscillators, and high stress levels that affect structural elements. Large displacement amplitudes would lead to collision between adjacent PCBs when too close together, resulting in broken and cracked components, circuit tracks and solder joints. Figure 4 shows the vibration model.

3.3 Solder joint fatigue reliability assessment

Fatigue analyses of the CPU board assembly were conducted to assess the impact of the thermal and vibration cycling on the fatigue life of the board, its components and interconnects. Computations were made for both the thermal and vibration fatigue failures, and the combined effects of the two were assessed. They were simulated for solder joints at the corners of large components because they would experience the greatest shear stress resulting from the thermal expansion mismatch between the package and the substrate.

There are two options for fatigue life assessment of solder joints: one due to device self-heating and the other due to an externally applied mission temperature profile. The latter was used in the study as the self-heating from the power input has such a small effect on the life cycle of the assembly. The thermal fatigue model is based on a Manson coffin-type damage law [**5**]. The stress state is formulated in terms of the maximum shear strain using the first-order Engelmaier models [**6**, **7**], while the vibration fatigue model is based on Steinberg's maximum displacement approach [**8**]. The Basquin relationship [**3**] is used to compute the life cycle due to vibration at solder joints.

Inputs for the solder joint fatigue analysis include the component position, diagonal length, lead/interconnection and case materials. Component case and board temperatures from the thermal analysis are automatically transferred to the solder joint fatigue analysis. Other inputs to the two cases of solder joint fatigue analysis of the CPU board are shown in Tables 1 and 2.

It is possible to compute the total damage to a component's solder joint when it is subjected to simultaneous vibration and thermal cycles by superposing the effects of vibration strain and thermal strain. This is achieved by using the Miner cumulative damage approach [**9**]. The cumulative damage approach assumes that every structural member has a certain fatigue life and that every stress reversal uses part of this life. It further assumes that the effective life is used up when enough stress cycles have been accumulated and

Table 1 Material properties of the CPU board assembly

Material	Density (kg/m^3)	Conductivity (W/m °C)			Elastic modulus ($\times 10^6$ lb/in^2)			CTE (ppm/°C)			Poisson ratio			Shear modulus ($\times 10^5$ lb/in^2)		
		k_x	k_y	k_z	E_x	E_y	E_z	α_x	α_y	α_z	υ_{xy}	υ_{yz}	υ_{zx}	γ_{xy}	γ_{yz}	γ_{zx}
FR4	1569.2	0.4	0.40	0.27	2.86	2.86	1.31	17.6	17.6	54.2	0.14	0.39	0.18	5.4	4.2	4.2
Copper	8911.5	401	401	401	12.0	12.0	12.0	16.7	16.7	16.7	0.34	0.34	0.34	0.0	0.0	0.0
Metal	2712.2	200	200	200	9.95	9.95	9.95	23.4	23.4	23.4	0.33	0.33	0.33	0.0	0.0	0.0
Plastic	1134.7	0.23	0.23	0.23	0.22	0.22	0.22	90.0	90.0	90.0	0.12	0.12	0.12	0.0	0.0	0.0
Ceramic	2601.5	39.7	39.7	39.7	10.4	10.4	10.4	6.20	6.20	6.20	0.17	0.17	0.17	0.0	0.0	0.0
Lead alloy	—	12.0	12.0	12.0	21.0	21.0	21.0	4.35	4.35	4.35	0.30	0.30	0.30	0.0	0.0	0.0
Tin–lead	8800.0	42.5	42.5	42.5	2.50	2.50	2.50	23.1	23.1	23.1	0.40	0.40	0.40	0.0	0.0	0.0

Table 2 Fatigue properties

Input description	Condition 1	Condition 2
Power-off temperature (°C)	−20	−20
Maximum case temperature (°C)	60	120
Vibration (h/day)	8.83/12.65	8.83/12.65
On/off cycle/day	2/3	2/3
Dwell time (min)	60	60
Maximum PSD (G^2/Hz)	0.1	0.1
Natural frequency (Hz)	530	530
CTE_x (ppm/°C)	17.23	17.23
CTE_y (ppm/°C)	17.23	17.23
Fatigue ductility	0.325	0.325

Table 3 Thermal analysis results

Load case	Maximum temperature (°C)			
	Ambient	Board	Case	Junction
Case 1	30	31	33	35
Case 2	50	51	53	55
Case 3	60	61	63	65
Case 4	120	121	123	125

the member will fail. Miner suggested the use of a ratio, R_n, to determine the fraction of the life that is used up. The ratio compares the actual number of stress cycles, n, at a specific stress level to the number of cycles, N, required to produce a failure at the same stress level, i.e.

$$R_n = \frac{n_1}{N_1} + \frac{n_2}{N_2} + \frac{n_3}{N_3} + \cdots + \frac{n_n}{N_n} = \sum \frac{n_i}{N_i} \tag{2}$$

When $R_n = 1$, the part is considered to fail.

Results from the solder joint fatigue analysis are given in terms of on/off cycles-to-failure for thermal, vibration and combined fatigue.

4 RESULTS AND DISCUSSION

4.1 Thermal analysis

The results from the thermal simulation are presented in terms of the temperature profile of the board assembly. The temperature distributions include those of the substrate, junction and component case for the different load cases simulated. Table 3 gives the maximum case, junction and board temperatures. The resulting temperature distribution highlights the 'hot' spots on the board, indicating where temperature gradients are high. An examination of the results shows that the maximum junction and substrate temperatures occur in device MN3, while the maximum case temperature is in device MN1. It should be noted that device MN3 dissipates the largest heat within the board assembly. The case material and the small size of device MN1 may account for the relatively high case temperature observed. The results further show that heat dissipated into the PCB from the components caused a small temperature rise of less than 2 °C above the specified ambient temperature. Again, this is due to the small power rating of the board assembly (0.350 W).

In order to validate the simulation results from the calcePWA thermal model, a further thermal analysis was performed using another CAE tool, MELTAN. The results from this other analysis compare well with those from the calcePWA PoF model, thus providing a degree of confidence in the validity of the thermal model. The component case temperature for each microelectronic package and temperature at all locations on the PCB were inputs to the solder joint fatigue assessment.

4.2 Vibration analysis

The first three natural frequencies, mode shapes and dynamic displacements, considered adequate for the present study, were computed from the random vibration simulation model. The first three natural frequencies of the CPU board assembly are 530, 1034 and 1212 Hz respectively, while the maximum dynamic displacement is 0.03 mm. The results show that the maximum board displacements are sensitive to the natural frequency. Thus, a slight increase in the natural frequency rapidly decreases the board deflection, and hence the stresses and strains in the components. The modal shape, natural frequencies and dynamic displacements give an indication of the relative motion between the PCB and the components.

Table 4 Summary of results

Component type	SJ H (mm)	Fatigue life cycle						Temperature (°C)		
		Thermal		Vibration		Combined				
		calce	*Analytic*	*calce*	*Analytic*	*calce*	*Analytic*	*Junction*	*Case*	*Substrate*
Case 1: −20 to 60 °C										
MN1	0.076	22	29	7×10^9	11×10^9	15	20	61.12	60.5	60.5
Leadless	0.127	74	97	7×10^9	11×10^9	51	62			
MN1	0.076	2×10^7	NA	2×10^{10}	NA	1×10^7	NA	64.63	64.02	60.51
J-lead	0.127	5×10^7	NA	2×10^{10}	NA	4×10^7	NA			
MN4 J-lead	0.102	4×10^6	NA	2×10^{10}	NA	2×10^6	NA	60.47	60.31	60.31
Case 2: −20 to 120 °C										
MN1	0.076	5	7	7×10^9	11×10^9	3	5	121.2	120.5	120.5
Leadless	0.127	16	22	7×10^9	11×10^9	11	15			
MN1	0.076	6×10^5	NA	2×10^{10}	NA	4×10^5	NA	124.6	124.1	120.5
J-lead	0.127	2×10^6	NA	2×10^{10}	NA	1×10^6	NA			
MN4 J-lead	0.102	2×10^5	NA	2×10^{10}	NA	1×10^5	NA	121.4	121.3	120.3

The fatigue failure of many electronic components is related to the dynamic displacements that are experienced by the PCBs housing the components. When the PCB resonant frequency is excited, the plate structure is forced to bend back and forth. When the displacement amplitudes are high, the relative motion between the PCB and the components can be high, which often results in cracked solder joints and broken electrical leads. Reducing the dynamic displacements would reduce the fatigue life of many different types of components. Vibration analysis results show that the board displacement is small because of the high first natural frequency. It is unlikely that fatigue problems due to vibration would occur. This is further confirmed from fatigue analyses.

4.3 Fatigue analysis results

The simulation of the thermal fatigue failure was conducted for two different conditions. The first is for the temperature range −20–60 °C representing the operating condition of the board assembly, while the second represents the qualification condition having a temperature range of −20–120 °C. The results from the solder joint fatigue simulation are presented in terms of the on/off cycles-to-failure for corner solder joints, because the corner solder joints experience the highest fatigue stresses. Table 4 shows the results for microelectronic devices with low fatigue life cycles-to-failure; other devices produced high fatigue life cycles and are considered not to influence the CPU board assembly's life and hence are not presented here. Table 4 also includes the results of simple analytical models that took no account of product detailed geometry.

An examination of these results shows that the fatigue life of the board assembly was greatly influenced by the thermal stresses produced at the solder joints. The predicted vibration fatigue life cycle estimates are orders of magnitude higher than the thermal fatigue, indicating that thermal fatigue is the primary loading that causes the device solder joints to fail. These thermal stresses are a result of mismatch between the TCE of the component and board materials. The thermally induced displacements at the solder joints produce a complex stress system distribution at the solder joint, resulting in high shear stresses near the bonded edges of the solder joint–substrate interface or solder joint–chip interface. The consequence of these high shear stresses is crack initiation at the bonded edges which may propagate along the interface or into the solder, leading to failure of the solder joint.

The first-order fatigue models used in the present analyses predicted very low fatigue life cycles for the leadless device compared to the leaded components. The shear force experienced in leaded devices is distributed between the leads and the solder joints, thus reducing the force experienced at the joints. In devices where solders are used, a significant amount of shear force is produced at the joints from any relative expansion difference between the board and the leadless device. Adding leads to the leadless chip carrier (LCC) device would produce an improvement in the life cycle of the same component. Indeed, this was the case, when, for example, changing the device MN1 interconnect to the J-lead saw the life estimates jump from 22 cycles to 20 million cycles for the same solder joint height and temperature cycle range.

A comparison of the fatigue results with the field failures of the board assembly shows that the first-order fatigue simulation models predicted ultra-conservative life cycles for leadless devices while overpredicting life cycles for the leaded device. The predicted life cycles for the leadless device are more than one order of magnitude lower than the field values and those for the leaded device are from experience several orders of magnitude higher than field values. However, the fatigue simulation models accurately predict the trend of failures and failure sites to those observed in the field.

The fatigue empirical factor for the leadless device was modified, following discussion with CALCE, to a value that has been found to give good results in other applications. An improvement in the predicted thermal life cycle was observed; there was no effect on the vibration life cycle. For example, changing the empirical factor from 1.0 to 0.42 improves the fatigue life of the leadless device from 22 to 163 thermal cycles. The exact criteria for selecting correct values of empirical factor have not been clearly established.

5 CONCLUDING REMARKS

An aerospace electronic board assembly has been analysed using a first-order, PoF based, model to independently assess the capabilities and areas of application of the PoF-based reliability assessment tool. The study has helped identify some of the benefits and limitations of this technique.

From the thermal analysis, it can be seen that the board and component case temperatures rise due to internal heating of 0.35 W and heat dissipation within the board is small. It appears that the thermal fatigue is driven by an externally applied mission temperature profile. Vibration analysis results show that the board displacement is small because of the high first natural frequency. Fatigue problems due to vibration of the board assembly are unlikely to occur, as shown by fatigue analyses. The solder joint fatigue analyses predicted the failure sites and the trend of failure within the board assembly.

The results from this study have further shown that the simple first-order PoF models used in evaluating the solder joint fatigue is ultra-conservative when applied to leadless electronic devices, and overpredicts the life cycles for leaded components. These indicate that the phenomenological deterministic models that make up the tool depend crucially on the quality of the physical relations contained in the models and the trustworthiness of the input data, including the empirical fatigue factors. It is important that the user of such a reliability assessment approach should have a good understanding of the models on which the PoF technique is based. Second-order models for joint fatigue life predictions for leadless and leaded components have been reported to give better results than the first-order model [**6**]. These are, however, yet to be properly validated for industrial usage.

An effective use of the first-order reliability assessment models as implemented in calcePWA for reliability assessment of electronic assemblies requires a good understanding of the models, their limitations and their particular areas of application. Even though the tool could be improved, e.g. by improving the interface and damage models, it seems that even relatively simple modelling as carried out in this case study can provide first-order guidance in reliability assessment of electronic products.

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