Materials and Processes Issues in Fine Pitch Eutectic Solder Flip Chip Interconnection

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Abstract

New product designs within the electronics packaging industry continue to demand interconnects at microscopic geometry, both at the Integrated Circuit (IC) and supporting board level, thereby creating numerous manufacturing challenges. Flip Chip On Board (FCOB) applications are currently being driven by competitive manufacturing costs and the need for higher volume and robust production capabilities. One of today's low cost FCOB solutions has emerged as an extension of the existing infrastructure for Surface Mount Technology (SMT) and combines an Under Bump Metallisation (UBM) with a stencil printing solder bumping process, to generate mechanically robust joint structures with low electrical resistance between chip and board. Although electroless Ni plating of the UBM, and stencil printing for solder paste deposition, have been widely used in commercial industrial applications, there still exists a number of technical issues related to these materials and processes as the joint geometry is further reduced. This paper reports on trials with electroless Ni plating and stencil paste printing and the correlation between process variables in the formation of bumps and the shear strength of such bumps at different geometries. The effect of precise control of the tolerances of squeegees, stencils and wafer fixtures was examined to enable the optimisation of the materials, processes and tooling for reduction of bumping defects.

Introduction

Compared with peripheral leaded package styles Ball Grid Array (BGA) and Chip Scale Packaging (CSP) formats provide increased circuit density capability coupled with a reduction in real estate coverage on the supporting board. However, as the inexorable drive towards miniaturisation and higher operating speeds continues, the need to completely eliminate even the minimum of chip packaging becomes evermore critical. Flip chip interconnection involves the assembly of naked, unpackaged chips directly to a supporting board, requiring products to be manufactured with solder joints at geometries similar to those of the semiconductor chips. Further reduction in the scale of flip chip geometries is expected, to ensure the technology keeps abreast of future product applications and IC designs [1, 2]. Such demands are also reflected at the board level, where microvia technologies (sub 50μm diameter) have been developed, that are capable of supporting FCOB interconnection [3].

Various hybrid processing techniques have been explored and adopted within the electronics manufacturing industry in order to provide FCOB solutions [4-7]. Electroplating, evaporation, solder jetting, stud bumping, stencil printing and "squeegee bumping" [7] have been employed, with each having its own merits, but their technological capability in terms of joint geometry, metallurgy, reliability, and processing cost (equipment, production yield) are critical factors to be considered. Extending existing SMT, i.e. process capabilities, equipment and soldering materials, offers a cost-effective solution for flip chip interconnection that is attractive to manufacturers having an existing SMT infrastructure. Solder joints formed by reflow of a bumped chip onto a supporting board (usually with the assistance of a flux) are capable of achieving flip chip interconnects by coupling the stencil printing technique with an electroless Ni Under Bump Metallisation (UBM): a cost-effective approach for providing a wettable surface finish to the Al bondpads on the chip. The electroless Ni-P UBM process has already been thoroughly investigated [8-11] and the existing industrial Ni-P plating processes and bath formulations for providing corrosion or wear resistance to engineering components have proven unsuitable for the UBM of fine pitch flip chip, which requires selective deposition onto the bond pads. Although improvements to this process have been made by several groups, and potentially commercialised to achieve a quality UBM satisfying a variety of wafer specifications and manufacturing details (e.g. pad registration, passivation etc.), there still exists a number of issues regarding the plating quality and technical specifications with respect to the initial bondpad characteristics (e.g. Al alloy composition, microstructure, thickness, properties and passivation defects).

The materials and processing variables in stencil printing also critically affect the quality and yield of solder deposition to produce consistent, reproducible and uniform bumps for fine pitch flip-chip prior to final assembly [12-20]. The Ishikawa cause-and-effect diagram generated by Pan et al. [14] summarises these variables. There are eight major categories identified (operator, environment, printing parameter, printer, stencil, wafer, squeegee and solder paste) that could influence the solder paste printing. Pan et al showed that, apart from the rigid control of the parameters related to the materials and systems

used, the operator's skills and experience need to be included. In this paper, FCOB trials have been undertaken with fine pitch flip chips (in the range of 300 to 90μm) with both peripheral and full array bond pad layouts. The issues related to materials and processing variables are addressed to provide guidance in the further enhancement of FCOB for high volume production.

Experimental Details

A. Flip Chips for Trials

Two types of test chip, having different feature dimensions, were used to investigate the effects of size in relation to the materials and processes. Test chips were processed in a 4 inch wafer format prior to dicing for bump analysis and assembly. Wafer type A (Figure 1a) was a peripheral I/O daisy chain design with Al-Cu (Cu 1Wt%) alloy bondpads (3μm thickness) on pitches of 225μm and 300μm. The circular openings in the silicon nitride passivation over the bondpads had a diameter of 75 μm. The type A chips were 6mm square with a thickness of 500μm.

Wafer type B (Figure 1b) included chip designs with both peripheral and full area array patterns of pure Al bondpads (1μm thickness). For the purposes of this experimental evaluation, chips with an I/O pitch ranging from 90μm to150μm, in a daisy chain format, were used. The bondpads had a circular passivation opening of 50μm for the 90μm pitch, but 60μm for the other pitches. The type B wafer was laid out as an array of 12x12mm repeated patterns, where each 12x12mm die was subdivided into a further 16 smaller 3x3mm die areas. Figure 1b shows the bondpads on these 3mm square sub-die which are laid out on four different pitches. Each pitch was laid out as a peripheral design, an array in a square pattern and a staggered array where the bumps were packed the closest that they could be for that pitch. Table 1 summarises the details of the two types of wafer used for this work.

Table 1. Comparison of the two types of wafer used for the trials

Wafer	Type A	Type B
Bondpad material	AlCu (1 wt % Cu)	Pure Al
Bondpad thickness	3μm	1μm
Passivation	Si_3N_4	SiO_2
Defects on passivation	None	Fine particles and pits
Die size	6x6mm	3x3mm
Pitch	225, 300μm	90, 100, 125, 150μm
Bondpad shape	Octagonal	Octagonal
Bondpad opening	75μm circular	50, 60μm circular
Bondpad layout	Peripheral	Peripheral, full array

B. Under Bump Metallisation (UBM) and Solder Bumping Trials

Both types of wafer were processed to generate an UBM layer on the bondpads for subsequent solder bump formation, using an electroless nickel plating process, developed previously [10, 21-22]. The process included pretreatment and activation of the Al bondpads by a single or double zincate treatment followed by plating in an acidic hypophosphite bath that deposited a layer of Ni-P containing 4-5 Wt% P.

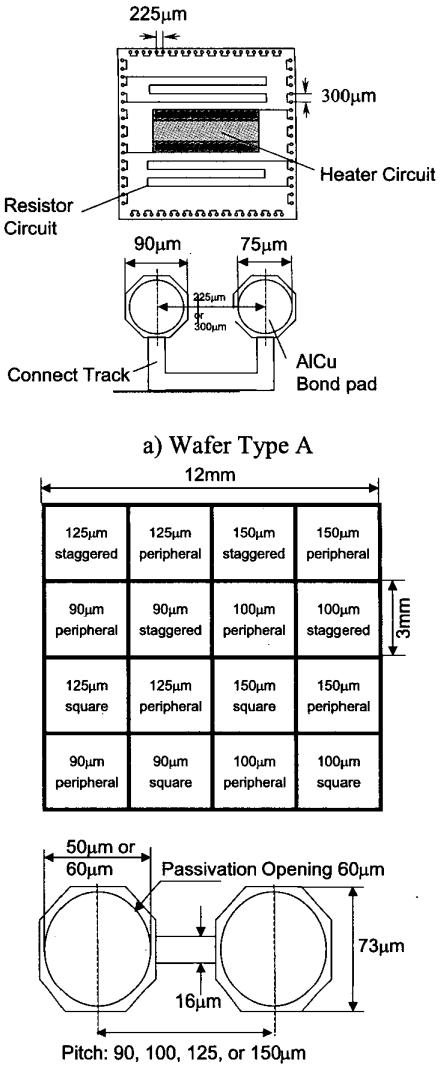


Figure1. Details of test chip designs: pad pitch, layout, materials and passivation opening

Following the electroless Ni UBM plating, solder paste deposits were created by stencil printing onto the bondpads to form eutectic Sn/Pb bumps for subsequent reflow soldering. A recently developed paste that contained an 89 wt.% content of SnPb eutectic solder alloy particles (diameter 5-15μm) and formulated with three different flux systems (Rosin Mildly Activated (RMA), no-clean (NC) and water soluble (WS)) was used for the printing trials. Stencil aperture sizes in the range of 175μm to a minimum of 75μm in diameter were assessed with two electroformed Ni stencils that were 50 μm and 75μm thick. Both metal and rubber squeegees were employed to compare their effects. The length of the metal blade was 300mm, and the

ruber squeegees are 168mm long and 7mm thick. Using a DEK 265 printing machine, stencil printing parameters such as squeegee speed and applied pressure were optimised to achieve suitable quality solder paste deposits for both the A and B type wafers. The printing speed: 10mm s^{-1}; snap off (separation gap between stencil and wafer surface): 0.00mm; normal load on squeegee: 30-80 N; separation speed: 0.5-2.0 $mm.s^{-1}$.

Finally, reflow of the paste deposits in an N_2 inert atmosphere was carried out to form the solder bumps. A Scanning Electron Microscope (SEM) with Energy Dispersive Analysis of X-rays (EDX) was utilised to investigate the surface morphology and for materials analysis.

C. Laser Surface Profiling

Since the wafer was too fragile to be handled by the standard printed circuit board carrier, a wafer fixture (or 'holder') was needed to support the wafer during printing. Two wafer fixtures (I and II) were used for the trials, which had different tolerances for the recessed pocket where the wafer was held by vacuum. Fixture I was machined from an aluminium alloy with a recessed circular pad made from porous ceramic. Fixture II was machined from mild steel with a precision recessed pocket with minimum surface variation. The surface planarity of the wafer when held in the pocket using both fixtures was evaluated using an ISO Surf laser surface profiler, which utilised a Rodenstock RM600 laser stylus capable of non-contact measurement between 0.01μm and 600μm.

D. Bump Micro-shear Testing

A micro-shear strength study of the mechanical integrity of the eutectic Sn/Pb bumps was conducted using a Dage Series 4000 Multi-purpose Bond Tester with a BS250 Ball Shear cartridge. This low deflection cartridge enabled precision shearing at pre-set heights above the chip surface. The width of the shear tool was 100μm, sufficiently wide to cover the bump diameter but not so wide as to interfere with adjacent bumps during the shear testing. A shear speed of 100-300μm/sec and shear height of 25-50% of the bump height were employed. During each test, the peak shear force and the corresponding displacement of the shear tool through the bump structure were recorded. For each shear test protocol, 20 solder bumps were sheared from individual chips which were randomly chosen from each test wafer.

Results and Discussion

A. Under Bump Metallisation

The Under Bump Metallisation (UBM) provides a solderable surface as well as protection for the Al pads from flux and solder dissolution during the solder reflow processes. A process that has received considerable interest as a maskless low cost wafer UBM technique is electroless nickel deposition, which is also suitable for large volume production [12]. However, plating defects can occur when finer pitch chips are processed, which are related to the pad microstructure and plating process variables. Several issues in connection with the pretreatment of Al bondpads are highlighted here including the influence of the first sodium hydroxide etching step and the zincate activation processe. Figures 2 a-c show the surface morphology of the Al pads on wafer type B after pre-etching in 5% NaOH solution for 10, 20, and 30 seconds respectively. Clearly, due to the localised preferential etching, the Al pads became more porous after 30 seconds etching, which led to poor Ni-P morphology in the subsequent plating. Figure 2d shows an EDX analysis from these etched surfaces. A dramatic decrease in their Al content was seen for 30s etching, indicating that damage to the pads had occurred.

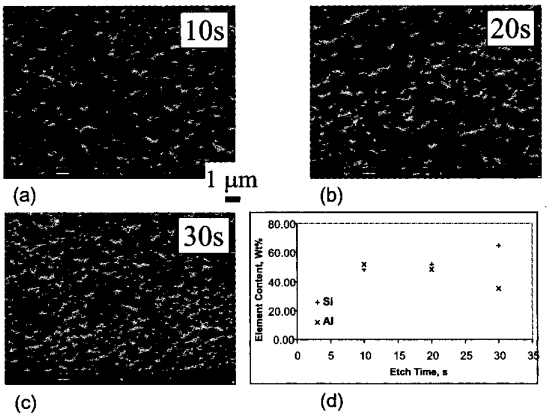


Figure 2. Etching of Al pads on wafer B in 5% NaOH solution: SEM surface morphology after a) 10s, b) 20s, c) 30s, and the EDAX elemental content analysis d)

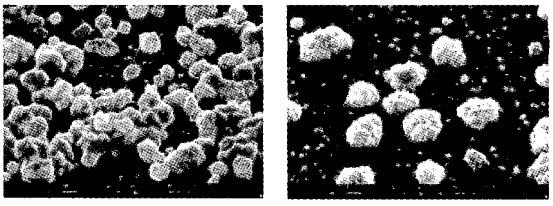


Figure 3. Zincate treatment of Al pads on wafer B: a) 20 s single zincate; b) 20 s double zincate, following 20s etch in 5% NaOH

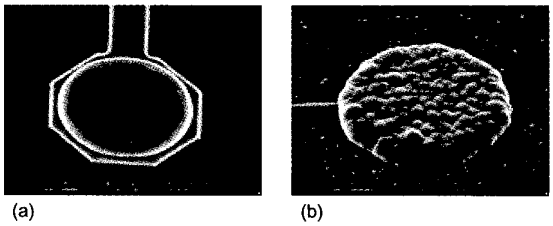


Figure 4. Electroless Ni-P UBM bump formation: a) Ni-P bump on pads of wafer type A; b) Ni-P bump on pads of wafer type B

The zincation process, which is conventionally used to activate the Al pads prior to Ni deposition, may also be thinning the Al pads due to the highly alkaline characteristics of the zincate solution. This could substantially reduce the interfacial bonding strength (adhesion) of the deposited Ni layers [10]. Figures 3a, and 3b are SEM micrographs of the Al pads of wafer type B after 20 seconds single and double zincation, respectively. In comparison with the porous Al pads from single zincation (Figure 3a), the Al pads after double zincation had been entirely removed (Figure 3b). This led to a radical reduction of the adhesion for the Ni layer [10]. Furthermore, the electrical resistance of the contact increased dramatically due to the thinning of the Al pads. For wafer type A, the thicker Al-Cu alloy pads allowed a wider processing window for etching and zincation to produce a finer and smoother zincate layer prior to Ni plating. Figures 4a- and 4b show the typical surface morphology of the Ni-P coating on the bondpads of wafer A and B, respectively. A number of issues related to the type B wafer and process specifications were identified for finer pitch flip chips, as shown in Figure 5 – an SEM image of a 5μm Ni-P UBM for a 100μm pitch staggered full array chip. The defects observed in the passivation resulted in the deposition of Ni nodules over tracks and between pads. This may cause short-circuits between pads; therefore, caution must be taken to avoid such faults at wafer manufacture to eliminate defects in passivation and to ensure accurate registration of pad openings.

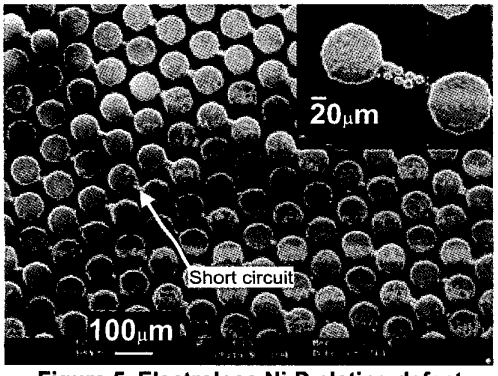


Figure 5. Electroless Ni-P plating defect identification: 5 μm thick Ni-P layer on 100 μm pitch staggered full array chip

B. Stencil Solder Bumping of Flip Chips

1. Solder paste deposition by stencil printing

Production of consistent, reproducible and uniformly distributed paste deposits over an entire wafer by stencil printing presents numerous challenges in finer pitch flip-chip applications. The solder paste used is composed of solder alloy particles, flux, viscosity controlling agents and a solvent system. Modelling and experimental work has demonstrated that the ratio of the aperture size to the solder particle diameter should be around five [20]. Depending upon the pitch size of the flip chips, a solder paste containing fine particles (e.g. 5-15μm) is therefore usually required to enable sufficient stencil aperture fill and acceptable release characteristics. In the printing process, solder paste sheared off by a squeegee blade rolls and subsequently fills the apertures in the stencil ahead of the squeegee as it moves over the stencil. On completion of the print stroke, the wafer is separated from the stencil, generating freestanding paste deposits on the bondpads beneath the stencil. Typical printing defects include bridging of adjacent pads, slumping, poor shape-definition and skipping (insufficient or no solder deposited) [19]. Optimised printing needs to consider variables including: paste rheology (e.g. viscosity); squeegee pressure and speed; stencil separation speed; print direction and environmental considerations such as temperature and humidity. According to Zou et al [17], the print temperature and humidity could significantly affect the printing quality using the squeegee method; it is therefore advantageous to use an enclosed, environmentally controlled print system [17]. The printing trials in this work were however performed in uncontrolled ambient environment on two types of wafer (A and B) to investigate both the attributes and consistency of the paste deposits, without consideration of the external environment (e.g. temperature and humidity and air flow). The critical factors affecting paste flow during the printing were thought to be aspect and area ratio, with paste transfer efficiency being improved if the aspect and area ratio were higher than 1.25 and 0.6, respectively [24]. There has been some experimental work combined with computational study (i.e. CFD approaches) to understand the printing process and the variables at macroscopic and microscopic scales [20, 23, 24].

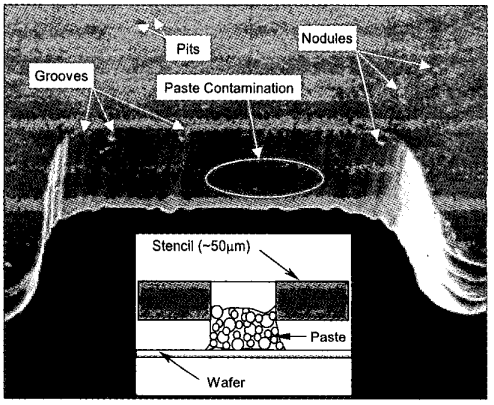


Figure 6. Stencil manufacture and definition: SEM image of the aperture wall texture from a nickel electroformed stencil cross section

Figure 6 shows a SEM view of a 100μm square aperture from the Ni electro-formed stencil. A number of features are apparent on the stencil surface (e.g. pits, nodules and scratches), and along the wall of the apertures (e.g. grooves). As these features were equivalent to the size of particles in the paste, it is likely that filling of the aperture was affected by the interactions between paste and stencil. Macroscopic studies on the bulk motion of paste ahead of a squeegee have indicated Non-Newtonian behaviour during the rolling of the paste and numerous process

parameters may therefore play important roles in determining the paste deposition [23]. Meanwhile, the microstructural dynamics of individual particles suspended in the carrier fluid could be critical to the printing consistency and quality [20]. In this study, the wave-like groove texture along the aperture wall (see Figure 6) is likely to have affected the flow, filling and release behaviour of the paste. In particular, adjacent to the corners of square apertures, the paste packing and subsequent release during the 'snap-off' (separation of stencil from wafer) can be substantially affected as indicated by microstructural modelling by He et al [20]. The stencil surface texture that contained features (e.g. pits and inclusions) at the microscopic scale can also influence the rolling of the paste and the interaction of paste with the stencil, which also impacts on the print quality. The relationship between the motion of solder particles and the paste rheology and the tendency for paste to adhere to the aperture walls during stencil withdrawal requires further study into the microstructure of paste transfer dynamics. However, the behaviour of a dense suspension at a plane wall boundary is different to that at the interior. Therefore, the paste deposition can be largely determined by the localised properties and interactions between the solder paste and stencil wall texture [23].

2. Tolerance of tooling (stencil, squeegees and wafer fixture) in fine pitch solder paste printing

The stencil used for printing plays a significant role in the quality and yield of solder paste deposition. Currently, stencils for SMT assembly are usually fabricated by chemical etching, Ni electroforming, or laser cutting processes. The materials used to make a stencil should meet various requirements in terms of their processability, durability, plastic/elastic deformation properties, wear and corrosion resistance, and cost effectiveness. Electrochemical Ni formed stencils have been often used for fine pitch flip chip wafer bumping (e.g. for the ~100μm pitch on wafer type B) due to their high hardness, excellent creep and fracture resistance and rapid manufacturability. However, the challenge still remains to reduce the manufacturing costs and to optimise the microstructure of the surface finish and precision aperture definition [18]. In particular, for finer pitch chips, the relationship between the aperture shape and size, and the aspect and area ratio has to be considered to achieve the highest packing efficiency. The stencil surface friction and elastic and plastic characteristics are also important parameters to achieve high alignment accuracy and a suitable 'snap-off' characteristic.

Squeegees are the blades used to shear and propel the solder paste to fill the apertures in the stencil. The contact between squeegees and the stencil surface, and paste rolling due to the shear process, were both found to significantly affect the final bumping quality (consistency and defect rates). The squeegee materials and properties (e.g. hardness, stiffness, and straightness) are of particular concern. Printing trials in this study showed that the quality and yield of paste deposits were dramatically improved with a rubber squeegee, in comparison to a metal squeegee. To explain this, Figure 7a and7b schematically illustrate the deformation of a stencil with two types of squeegees: stainless steel and rubber, respectively. The closer contact along the curved stencil surface that is attributed to the better elastic characteristics of rubber materials results in a narrower crevice between the squeegee and stencil, whilst the stainless steel squeegees were unable to co-locate the deformation with the stencil surface, so that larger contact gaps resulted. The larger the crevice, the lower the packing efficiency obtained, because of the localised lower levels of shearing and pressure. Therefore defects such as partial or incomplete deposits (skipping) and missing bumps were observed after the stencil was removed. Visual inspection confirmed that the distribution of the paste deposits when using metal squeegees was less uniform, and many missing or skipped bumps occurred.

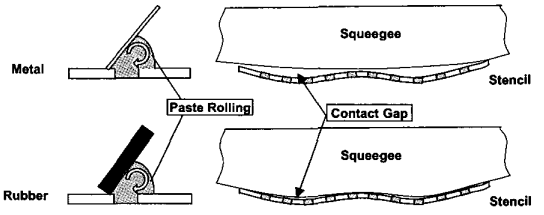


Figure 7. Squeegees in action to roll the paste and fill the stencil aperture

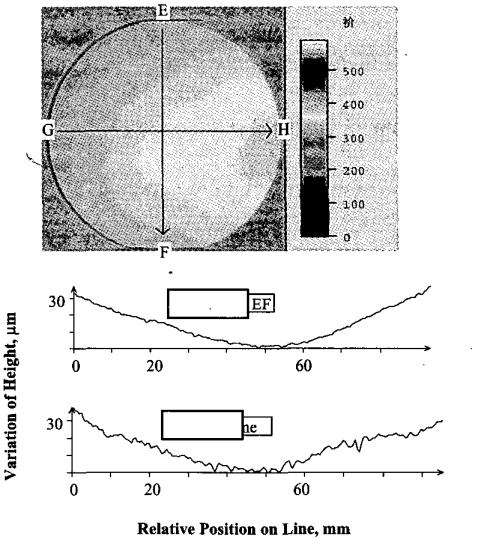


Figure 8. Laser surface imaging profile of wafer fixture I: Surface variation of wafer in pocket drawn down by vacuum

The dimensional tolerance or accuracy of the wafer fixture (holder) is also critical to the printing quality (e.g. consistency) and yield. Two types of wafer fixtures (I and II) were used in this work to investigate the effect of their surface co-planarity tolerance. Figure 8 provides the laser surface topography when the wafer was drawn into the pocket of fixture I by vacuum during the printing process. The line profiles EF and GH from

the scans show a variation in height of over 40μm, measured from the edge to the centre of the wafer, owing to the poor planarity of the pocket surface. Zou et al [17] proposed the estimation of substrate (e.g. wafer) distortion degree using H/L%, where H is the maximum vertical variation due to bending, L the substrate length or diameter. Accordingly, using fixture I the wafer distortion degree is estimated to be 0.04% for the 4 inch wafers that were used (40/101600)*100%=0.039%). This is well below the critical value of 0.1% that was proposed by Zou et al to enable acceptable quality by squeegee printing in the case of PCBs with pitch size bigger than 300μm. However, in this study, for printing on wafers with pitch size smaller than 300μm, the trials showed that printing with rubber squeegee was unable to cope with distortions as small as 0.04% using fixture I. This resulted in a solder paste 'smear' area that appeared near the centre of the wafer after printing, and consequently, the occurrence of a number of print defects such as slumping, skipping, missing or displaced bumps where the paste 'smear area' was observed.

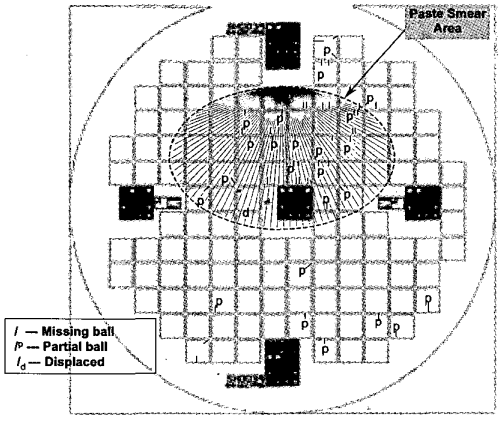


Figure 9. Evaluation of bumping by stencil printing on wafer type A with wafer fixture I: A smear paste area was identified causing poor quality of paste deposition

Figure 9 shows a typical result of the evaluation selected from a number of trials on wafer type A. This indicates that the rigid wafer fixture is required to ensure the flatness of the wafer surface to be printed. Using wafer fixture II, the resulting variation on the wafer when it was drawn down in the pocket by vacuum was around 5μm (see the line profiles of EF and GH in Figure 10). This variation can be converted into a distortion degree of approximately 0.005%. Unsurprisingly, when using fixture II, there was no observable 'smear' area after printing, printing trials showed an excellent quality and uniformity of paste deposit distributed throughout the entire wafer surface, with a dramatic reduction of the defects. Improvement of printing quality due to the smaller distortion of the wafer surfaces to be printed is likely to lead to a significant increase of paste packing efficiency and a neater release motion of the paste from the apertures. The stencil conforming closely to the wafer surface resulted in uniform squeegee pressure and a controlled "snap-off" when withdrawing the stencil from the wafer surface, enabling the paste deposits to be released uniformly over the entire wafer surafce. The smeared paste area occurred where the squeegees could not remove the paste from the depressed areas, such that the paste residues remained on the stencil surface. In these areas, on withdrawal of the stencil, the paste in the apertures could be completely or partially lifted up along with the paste residues on the stencil, thereby causing slumping, skipping and missing or displaced bumps. In addition, the paste packing efficiency was significantly decreased due to less shear and squeegee pressure in the depressed areas.

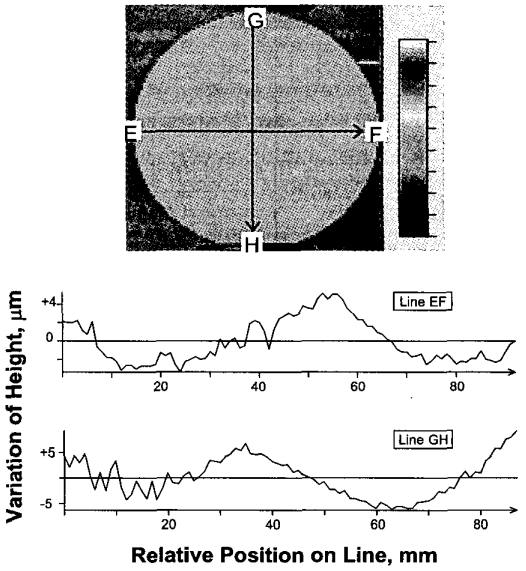
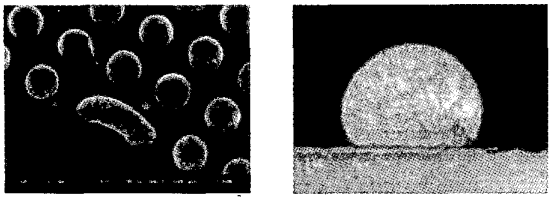


Figure 10. Laser surface imaging profile of wafer fixture II: Surface variation of wafer in pocket drawn down by vacuum

C. Formation and Shear Strength of Solder Bumps

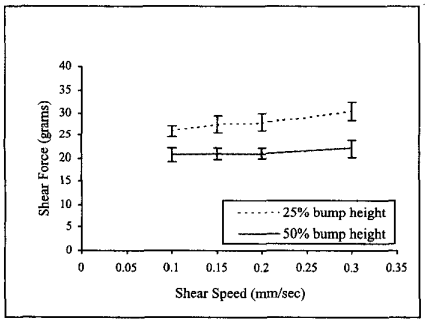
After a reflow process in a nitrogen atmosphere the solder paste deposits formed solid solder bumps. Figure 11a shows the solder bumps for a 150μm pitch full array chip, which included a bridging defect. This type of failure was the result of adjacent oversized deposits merging together during reflow when the pitch size was close to the pad openning. The small balls formed between the bumps in Figure 11a are thought to be formed at the defects on the passivation layer where the small Ni nodules were generated in the Ni UBM processes (Figure 5) and could later have become the sites for solder attachment. The microsectional image (Figure 11b) confirms the excellent wetting of solder to the Ni-P UBM and the formation of the intermetallics along the interface between the solder alloy and Ni-P layer, producing a typical bump with a 60μm height 80μm diameter at 150μm pitch.



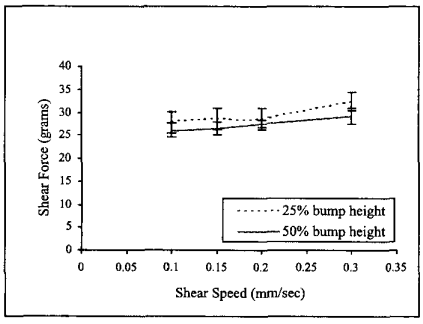
(a) (b)

Figure 11. Solder bump formation: a) SEM micrograph of solder balls on Ni UBM of 150 μm pitch; and b) Cross-sectional view of a 80μm diameter bump

Shear tests were carried out in this work to evaluate the mechanical strength of bumps, and to understand the failure modes. From previous BGA and CSP shear studies, and the lack of shear strength information at small-scale geometries, the shear study was conducted to understand the effects of testing parameters on bump integrity. Figures 12a and 12b show the effects of both shear speed and shear height at 80μm and 100μm bump diameters, respectively. The error bars around the data points, for all the graphs in this text, represent one standard deviation. The results, for the varying bump diameters, indicate two trends clearly visible from the shear study. Firstly, increasing the shear speed yields apparently higher shear strengths for the bumps. Secondly, reducing the shear tool height also appears to



(a) 80μm bump diameter



(b) 100μm bump diameter

Figure 12. Bump shear results: the effects of varying the bump diameter and shearing height

increase the bump shear strength. The variation in shear height was investigated in light of the shear height tolerance specified within the JESD22-B117 standard, which states a maximum shear height of 25% of the bump height. These shear study trends reflect similar work reported by Huang et al [25], albeit at BGA geometries. Further shear testing was conducted at a shear speed of 150μm/sec and corresponding height of 25%. The average shear strength was found to be greater for the 100μm bump size (28.6g ±2.3g), compared to the 80μm size (27.5g ±1.8g). This is attributed to an increase in the sheared cross sectional area.

Conclusions

A number of technical issues related to the materials and process variables have been presented, in order to produce quality bumps and thus reliable solder joints for fine pitch FCOB interconnection. In electroless Ni plating for the UBM, the pre-treatment steps including the etching (in NaOH) and zincation, are critical to ensure a Ni-P layer with adequate adhesion to the Al pads and low electrical resistance. The elimination of Ni nodules generated at the defects in passivation is crucial to prevent bridging and as such wafer manufacture should ensure a defect free passivation with accurate registration of the pad openings.

The stencil printing trials identified issues of stencil fabrication (e.g. the need for high quality aperture definition), and dimensional tolerances of the squeegees and wafer fixtures used in printing. The filling, release and distribution characteristics of the paste material through the small apertures determine the quality and consistency of the bump formation. Therefore, not only the print parameters, but all of the related mechanical components (e.g. stencil, squeegees, and wafer fixture etc.) and their dimensional tolerances need to be carefully considered to achieve the maximum reduction of bumping defects. Significant reductions in solder bumping defects by stencil printing have been achieved by optimising the materials and processing variables in relation to the precise manufacture, definition, rigid design and control of the stencil apertures, wafer fixtures and squeegees. A Ni formed stencil with finely defined aperture geometries, coupled with the use of rubber squeegees, rigid wafer fixture and optimised printing parameters has been employed to produce consistent, reproducible and uniform paste deposits with high yields and quality for flip chip wafer bumping with the pitch size around 100μm.

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