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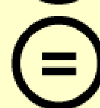

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Scanning Acoustic Microscopy Investigation of Engineered Flip-chip Delamination

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Abstract

The rapid uptake of flip-chip technology within the electronics industry, is placing the reliability of such assemblies under increasing scrutiny. A key feature of the assembly process is the application of underfill to reinforce the attachment of the die to the printed circuit board. This has been identified in numerous studies as one of the major ways in which the reliability of the devices can be improved, by mitigating the coefficient of thermal expansion mismatch between chip and board. However, in order for the underfill to be effective in coupling the die to the circuit board, its adhesion to the passivation layer of the die and the solder mask layer on the PCB must be maximised. There is a growing body of literature that indicates that poor adhesion at either interface (delamination) as a result of contamination can result in premature failure of the assembly through stress fracture of the solder joints.

In order to investigate further the effect of delamination on the reliability of flip-chip assemblies, surface chemistry has been used to control the adhesion of the underfill to the die passivation. This paper reports how modification of the die surface by the application of a low surface energy coating, which prevents the strong adhesion of the underfill, has enabled the selective delamination of the device at the chip-to-underfill interface. Using scanning acoustic microscopy (SAM) the effectiveness of this treatment in creating controlled delamination before and after thermal cycling has been monitored. The ability to engineer delamination, can enable experimental studies of the mechanics of flip chip assembly failure, which complement current finite element modelling work.

Introduction

With the increasing utilisation of flip-chip technology in electronics manufacture, the requirement for high speed assembly processes is becoming more important. One part of the assembly process that has attracted considerable interest as an area in which improvements can be made is the dispensing and curing of the underfill. The application of underfill is essential to maintaining the reliability of flip-chip assemblies by reducing the impact of the coefficient of thermal expansion (CTE) mismatch between the chip and the board which otherwise would lead to rapid fatigue failure of the solder joints during operation.

The drive to increase the throughput of flip-chip assembly lines has led to extensive research in the areas of pre-deposited underfill, fluxing (no-flow) underfill, snap-cure underfill and fast flow underfill. The introduction of these new materials has required extensive investigation of their ability to maintain the reliability of the assemblies, which is traditionally monitored through thermal cycling studies. The key underfill properties that determine its effectiveness for reliability enhancement are its modulus of elasticity, CTE and its adhesion to the PCB, solder ball and die surfaces. Through extensive modelling studies and experimental trials it has been shown that the CTE of the material should be between that of the PCB and the die to ensure the maximum lifetime of the device. However, the integrity of the underfill to chip or underfill to PCB interfaces is also seen as essential to enable the underfill to provide effective coupling of the chip to the board. Through reliability studies of flip-chip assemblies there is increasing evidence that failure at these interfaces (delamination) leads to early failure of the device. The origins of delamination are varied, but it is often attributed to surface contamination due, for example, to flux residues. The non-destructive technique of scanning acoustic microscopy (SAM) is gaining extensive use for quality control in the electronic packaging industry and has been applied by researchers to investigate flip-chip packages. The technique is able to identify delamination in flip-chip devices due to the strong reflection of sound energy at internal interfaces between the package materials and air or vacuum.

In order to enhance the adhesion of the underfill to the chip surface, new underfill material formulations have been examined [e.g. 1,2]. All of these rely on the formation of a strong chemical bond between the die passivation and the underfill epoxy resin through the introduction of chemical species that make bonds directly with both materials. The work of C.P. Wong [2] is a good example of this: he has incorporated silane species into the underfill material that have a chemical head group that bonds selectively to the passivation of the die and a tail group that interacts strongly with the epoxy species in the adhesive. An example of this is shown in figure 1a. The use of silane materials in this way, is reminiscent of the formation of self-assembled monolayers which have received

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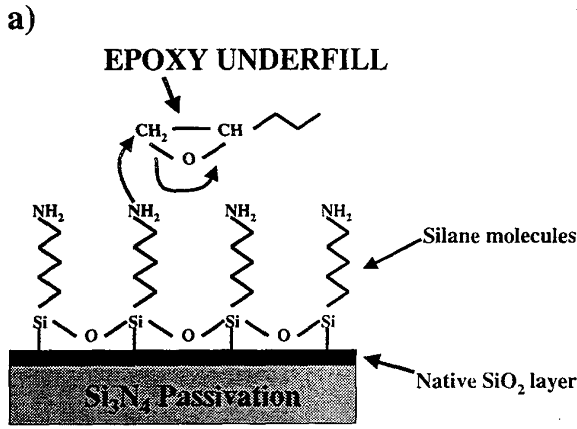
considerable interest in recent years. Figure 1b shows an example of the formation of a self-assembled monolayer of octadecyltrichlorosilane (OTS) on a SiO_2 surface. In this example, the monolayer would be formed by immersing the sample that has a thin native layer of SiO_2, into a dilute solution of OTS in a solvent. The OTS molecules adsorb onto the material surface by forming strong chemical bonds between the silane species and the silica surface. The long carbon chain backbones then align themselves away from the surface, maximising the van der Waals interactions between them and exposing the tail group, in this case CH_3, at the surface. It is the ease with which surfaces with different chemical properties can be prepared by adsorbing molecules with different chemical species in the tail group that has generated interest in these materials.



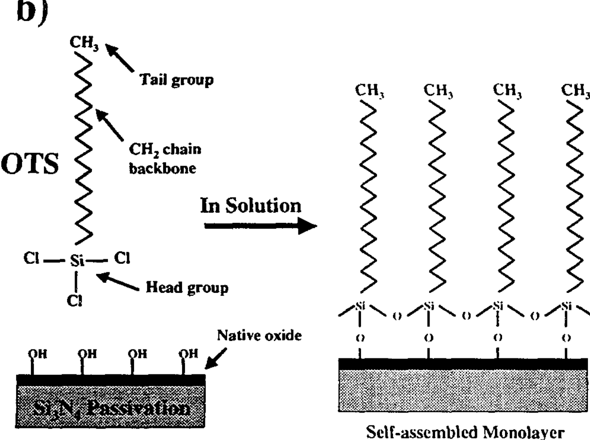


Figure 1: a) mechanism of adhesion promotion using silane additives in underfill; b) formation of a self-assembled monolayer of octadecyltrichlorosilane (OTS) on silicon nitride.

In the preliminary experiments reported here, delamination in flip-chip assemblies has been engineered through the deliberate minimisation of the adhesion between the die and the underfill. To achieve this, self-assembled monolayers of OTS on solder bumped die were prepared as shown in figure 1b to produce a low energy die surface composed of methyl (CH_3) species that would not bond covalently to the underfill. The aim of these experiments was to develop a tool for the understanding of delamination mechanisms and their effects on package reliability, and to use scanning acoustic microscopy to monitor the development of delamination during thermal cycling. This engineered delamination of flip-chip assemblies will in the future enable the validation of the results of computer simulations of device reliability. In addition, these preliminary experiments could lead to further studies where selected areas of the die are delaminated through the formation of patterned adhesion inhibitor layers, leading to a greater understanding of the mechanisms of device failure and the critical areas where adhesion should be maximised.

Experimental

As these were trial experiments, only two boards were assembled, each populated with 9 die. The first board (board 1) used a mixture of assembly techniques, including fluxing underfill, and presented some interesting preliminary results which were further investigated by the assembly of a second board (board 2) using a more limited range of technologies. The following sections describe the test devices used in this study and the assembly techniques employed. All wafer bumping and board assembly operations were performed in the UK, while thermal cycling and SAM analysis were conducted in Hong Kong. There was therefore a transportation operation between assembly and testing and the effect of this on the assemblies will be discussed further.

Test Devices

For these trials, 6mm x 6mm test chips were used which included a daisy chain test structure of 75μm diameter Al bondpads at 300 and 225μm pitch. Bumping of the die was carried out on a wafer scale starting with the plating of an electroless nickel under bump metallisation (6μm thick) together with a gold flash. Following this, solder paste was printed and reflowed to produce solder bumps around 70μm high. Further details of the electroless nickel bumping process can be found elsewhere [3]. After bumping, the wafer was cleaned to remove flux residues before being diced into individual chips.

The printed circuit boards used for these studies were FR5 material with 25μm thick copper tracks and pads which were finished with electroless nickel and immersion gold. The nine electrically testable sites on the board matched the daisy chain configuration of the die and were divided into three groups based on the pad geometry and the method used to define the solderable area. Table 1 lists the range of sites available on the boards and figure 2 shows an image of one of the microvia in pad sites (no.s 6-9). The pads for sites 1-3 consisted of straight tracks with no solder mask, while sites 4 and 5 used a carefully applied solder mask to define a small wettable area on the track surface for joint formation. The microvia in pad sites did

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not use solder mask to define the solder wettable area as there was no exposed track along which the solder could run. Each site had an array of daisy chained pads around the periphery of the die that enabled the majority of the joints to be tested for continuity by one resistance measurement. These can be seen as the square array in the centre of figure 2. Further test points were provided running from each side of the die to allow failed joints to be located. In addition, eight larger test points were provided around the site to enable the four point measurement of two resistor structures on the die surface. These test pads can be seen clearly in figure 2 to the top and bottom of the bond site.

Table 1: PCB site type and dimensions

Site No.s	Pad Type	Pad / track width
1-3	Bare track	110μm wide
4-5	Solder mask defined	110μm diameter
6-9	Microvia in round pad	140μm diameter

Application of Low Surface Energy Coating to Die

The passivation on the die was Si_3N_4, which has been shown [4] to possess a native SiO_2 layer onto which

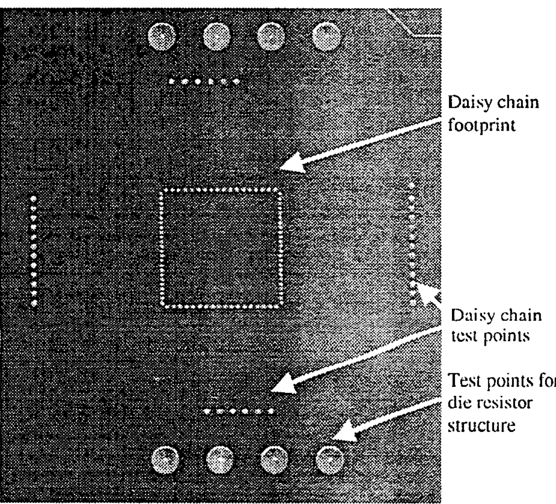

Figure 2: Site number 9 on PCB showing microvia in pad connections (central square). Small arrays of pads around the outside are for probing of daisy chain individual joints and large pads are for probing of die resistor structures.

silane species can adsorb. Octadecyltrichlorosilane (OTS) coatings were applied to the die using a traditional procedure for the formation of self-assembled monolayers [5]. This involved immersing the individual solder bumped die into a dilute solution of octadecyltrichlorosilane in cyclohexane (~10mM concentration) for between 1 and 1.5hrs followed by rinsing with cyclohexane and iso-propyl alcohol and then drying.

Board Assembly and Underfilling

Die were assembled onto the sites on the boards in pairs i.e. a coated die next to an uncoated die on the same type of site, so that direct comparison between them could be made. Table 2 lists the assembly configurations used for these trials. Die were assembled to the board by applying flux to the die, followed by die placement. Flux was applied by using a doctor blade to produce a thin layer of tacky flux on a metal plate into which the die were placed face down. For the die used on board 2 this provided a small quantity of flux on each of the solder balls that was sufficient to form good joints during reflow, however for the die used on board 1, some additional flux became attached to the surface of the chip which remained in the assembly after reflow.

Following reflow, the die assembled onto board 1 using the no-flow underfill were found to have moved and were not conducting. Further detailed investigation of these devices was therefore not pursued. For the die assembled using tacky flux a much higher assembly yield was achieved and these devices were underfilled without any cleaning treatment applied. A commercially available underfill was used for all assemblies and was dispensed manually along two sides (L shape) of the die, which was heated to 80-90°C. Material was continually added until it was seen to flow out of the other two sides of the assembly, after which, additional underfill was dispensed to form fillets all around the device. The underfill was then post-cured in an oven at 150°C for 30 mins.

Table 2: Board assembly parameters

	BOARD 1		BOARD 2	
Site No.	Coated / Uncoated Die	Assembly Technique	Coated / Uncoated Die	Assembly Technique
1		Tacky flux	Coated	Tacky flux
2		Tacky flux	Coated	Tacky flux
3		No-flow		Tacky flux
4	Coated	Tacky flux	Coated	Tacky flux
5	Coated	No-flow		Tacky flux
6		Tacky flux		Tacky flux
7	Coated	Tacky flux	Coated	Tacky flux
8		No-flow	Coated	Tacky flux
9	Coated	No-flow		Tacky flux

Thermal cycling

Thermal cycling of the assemblies was conducted using an air-air system. The profile used was –40°C to +125°C with a hold at each temperature of 30mins for board 1, and a hold of 15 mins for board 2. Board 1 was exposed to 111 thermal cycles, while board 2 received 430 cycles in the time available. The different hold times and limited number of thermal cycles for the two boards were used for reasons of time pressure on the cycling chamber.

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Scanning Acoustic Microscopy (SAM)

The scanning acoustic microscope used was a Sonix Inc. system [6]. For analysis, the sample is immersed in water and a sonic transducer emitting sound wave pulses is scanned over the surface by a highly accurate translation stage. Sound energy is reflected by internal interfaces in the sample and detected by the same sonic transducer. The depth at which the reflection occurs may be estimated from the time at which the reflected sound pulse is received. Total reflection of the sound pulse occurs at the interface between solid materials and air or vacuum, for example at a void or delamination. An image is built up from the scan by gating the reflection signal from the transducer to cover the layer or layers of interest in the device. The magnitude of the largest reflection between the gates is mapped to a greyscale value to form a pixel of the image. Because total reflection of the sound pulse occurs at the interface between solid materials and air or vacuum, voids and delaminations usually cause the largest reflected signal and hence appear white within the image. In this work a transducer frequency of 230MHz was used and the gates set to cover both the chip to underfill and the underfill to board interfaces.

Laser Profilometer Measurements

In order to measure the extent of curvature of the die at various stages of assembly, a laser profilometer system was used. This consisted of an infra red laser and focus detector that was mounted in a frame above an X-Y translation table. To record data from the back surface of the die, the PCB was mounted on the table and scanned beneath the laser, the reflection of which was used to build up an image of the sample height as a function of the X-Y position. The profiles shown in this paper were extracted from complete scans of the back surfaces of the die and display the curvature across the die width from left to right.

Results

Die Curvature Measurements

The difference in the coefficients of thermal expansion of the silicon die and the FR5 PCB, together with the high temperature cure of the underfill material, means that the die attached to the PCB are expected to be curved following assembly [7]. Figure 3 shows laser profiles obtained from the back surfaces of a number of devices at various stages of the assembly process. Figure 3a shows a profile obtained from a bare die before assembly onto the circuit board. This profile shows no curvature, as expected, and forms a control from which the other assemblies can be judged. Figure 3b shows a profile obtained from a die that had just been reflowed onto the PCB and allowed to cool to room temperature. Again there is no curvature observable in the data. This is unexpected, as at 183°C when the solder solidifies, the die should be in a stress free condition (i.e. planar) and cooling to room temperature is likely to induce curvature as the board contracts more than the silicon. The absence of any curvature in the profile of figure 3b even only 15 minutes after the reflow process indicates that the solder joints are able to relax (creep) sufficiently to relieve the stress and remove the curvature from the assembly.

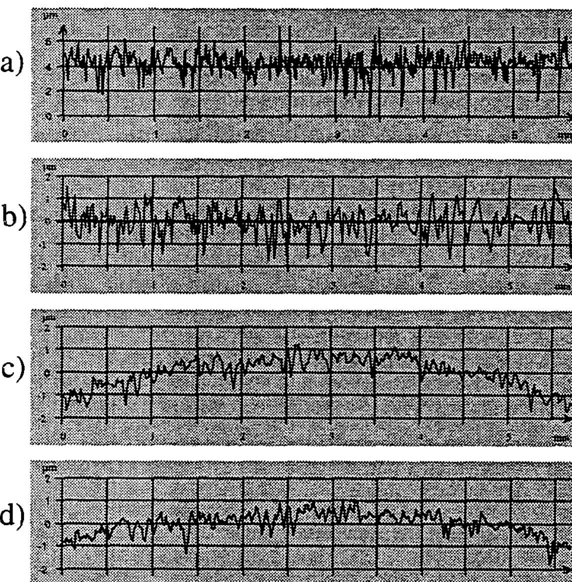

Figure 3: Laser profilometer data obtained from die at different stages of assembly. a) bare die not attached to PCB; b) after die reflowed onto PCB; c) after underfill dispense and cure of assembly (uncoated die); d) after underfill dispense and cure of assembly (OTS coated die).

For die with no coating, following underfill dispensing and then post-curing of the devices, the die were found to have a significant degree of curvature as shown in the profile of figure 3c. This indicated that the edges of the die were deflected by around 2-2.5μm compared to the centre of the die. This result was found for several assemblies produced in this way using the conventional underfill material and this agrees with model calculations made by Wheeler and Bailey [8] based on these devices. These results indicate that the solidification of the underfill during the post-cure at 150°C, locks the die to the PCB so that during cooling to room temperature, the greater contraction of the PCB compared to the silicon chip causes extensive bowing of the latter.

For the die treated with OTS (Figure 3d), a similar curvature profile was obtained as for the uncoated die (Figure 3c). However, closer inspection of the data revealed that the deflection of the OTS coated die was only 1.5μm at the edge of the chip with respect to the centre. This would appear to indicate that the application of the coating reduces the interaction of the underfill with the die surface, leading to less curvature on cooling.

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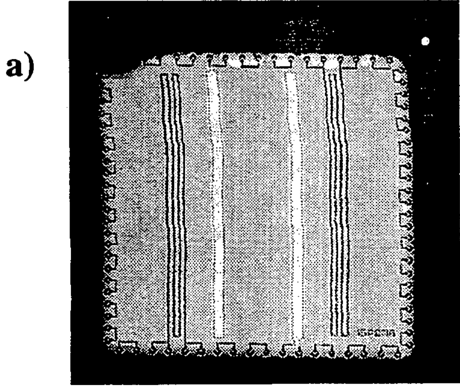
Following assembly, board 2 was electrically tested to measure the resistance of the daisy chain connections around the whole die and the shorter four point resistance chains situated on either side of the assemblies. All daisy chains of the uncoated die were conducting immediately after assembly and after underfilling. However, the OTS coated die generally formed higher resistance daisy chains compared to the uncoated chips.

Table 3: Number of thermal cycles to electrical failure for die assembled onto board 2

Site No.	Die Type	Full daisy chain	Four point edge test sites
1	OTS coated	Transportation	<117 cycles
2	OTS coated	Transportation	<117 cycles
3	Uncoated	>430 cycles	>430 cycles
4	OTS coated	Transportation	<220 cycles
5	Uncoated	>430 cycles	>430 cycles
6	Uncoated	>430 cycles	>430 cycles
7	OTS coated	Transportation	<220 cycles
8	OTS coated	Transportation	<220 cycles
9	Uncoated	>430 cycles	>430 cycles

a)



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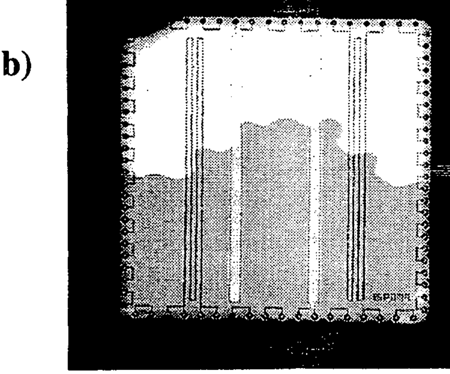

Figure 4: SAM images of OTS coated die assembled onto board 1: a) before thermal cycling; b) after 111 thermal cycles.

Subsequent cross-section analysis showed that the majority of solder joints were well formed, but for the OTS coated die, one or two dry joints had occurred leading to only a pressure contact between the solder and the copper track. After transportation to Hong Kong, the full daisy chains of the assemblies formed from the OTS coated die had all failed, presumably due to the separation of these dry joints. This left only the shorter four point resistance chains operational for testing which were used to monitor the effects of thermal cycling on the devices.

Resistance measurements were performed at room temperature after 117, 220 and 430 cycles. Table 3 summarises the results of the electrical tests as a function of the thermal cycling for board 2. From these results it can be seen that two of the die with the OTS coating had failed before 117 cycles, while the remaining die with the OTS coating failed before 220 cycles. In contrast, die without the OTS coating were all still conducting with little change in joint resistance after 430 cycles.

Scanning Acoustic Microscopy Measurements

SAM measurements were performed on the two assembled boards before and after thermal cycling. Figure 4 shows the SAM images obtained from one of the two OTS coated die assembled onto board 1 using tacky flux. Before cycling, this die showed some delamination in the vicinity of the joints across the top of the die. However, following 111 thermal cycles, this device displayed severe delamination in the SAM image and some delamination was also found for the other OTS coated die. For die that were uncoated, no delamination was observed following this thermal cycling regime. The substantial delamination observed for the coated die was consistent with our expectations based on the poor adhesion of underfill to chip surface induced by the OTS coating. The poor adhesion was further demonstrated by the complete detachment of the die from the PCB during handling of the assembly for cross-section analysis.

In order to repeat the experiment, board 2 was prepared and assembled, this time successfully avoiding tacky flux reaching the die passivation. As described above, the OTS coated die assembled onto this board all failed the daisy chain electrical continuity test following transportation to Hong Kong, and following limited thermal cycling, all the remaining electrical connections on the die became open circuit. Figure 5 shows representative SAM images obtained from an OTS coated die assembled onto board 2 before and after thermal cycling. In contrast to the coated die assembled onto board 1, none of the OTS coated die on board 2 showed any delamination even after 430 thermal cycles (the maximum time allowed for these trials).

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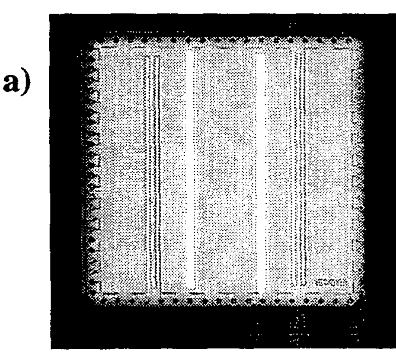
a)



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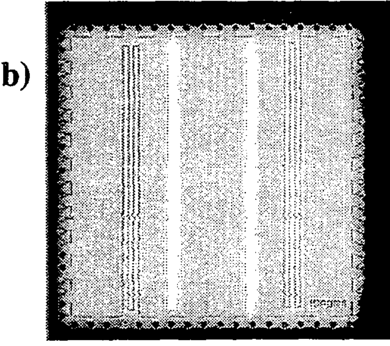

Figure 5: SAM images of OTS coated die assembled onto board 2: a) before thermal cycling; b) after 430 thermal cycles.

Cross-section Analysis

Following thermal cycling and SAM examination, the boards were returned to the UK for further die curvature and cross-section analysis. Laser profilometer measurements of the assemblies prepared without the OTS coating still indicated significant curvature of the back face of the die comparable to that observed before thermal cycling. This would indicate the die were still firmly attached to the board supporting the conclusion from the SAM and electrical measurements. A cross-section of the die bonded to site 5 of board 2 is shown in figure 6a. This shows clearly the integrity of the solder joint between the circuit board and the electroless nickel bump on the die as expected from the electrical continuity of the daisy chain connections.

For the die that had been coated with OTS and reflowed onto site 4 of board 2 (matching site to number 5 described above), a very different picture emerged of the die condition. The laser profilometer measurements indicated no curvature of the die at all after 430 thermal cycles and the cross-section (figures 6b and 6c) showed clearly a substantial separation between the die and the underfill. The presence of a large separation between die and underfill in the cross-section is unexpected as the SAM images did not indicate any delamination. At present, it has not been possible to determine whether this separation occurred as a result of sample preparation for cross-section analysis or damage in transit of the board from Hong Kong to the UK. The absence of any die curvature after receipt of the board in the UK could indicate that this separation did take place in transit leading to the die reverting to its planar, stress free condition. The nature of the joint failure observable in the cross-sections of figures 6b and 6c is interesting, as a mixed mode of failure appears to have taken place. In some joints, fracture of the solder near the electroless nickel bump surface can be observed, however in others, the electroless nickel bump has been pulled from the Al bondpad. This later failure mode is rarely observed in normal assemblies and it is unclear whether these fractures were the cause of the electrical failures or whether they have been induced later on by the substantial separation of the die from the underfill. Remember the SAM images did not indicate delamination even though the joints had failed. The surrounding of the solder ball by the underfill during separation could have produced a solder ball pull effect which resulted in the fracture of the electroless nickel – aluminium interface. Alternatively, the weak adhesion of the underfill to the die surface could have led to a shearing action of the cured adhesive across the die surface during thermal cycling, again resulting in the fracture at the NiP-Al interface.

Die Pull-off Testing

For the die that had been coated with OTS, the complete non-adhesion of the underfill to the chip surface was further demonstrated by pulling off the die from the boards. For the coated samples this was extremely easy and an example of the result obtained from this is shown in figure 7. This shows a die that has been pulled off the board leaving behind the underfill with an impression of the chip in it. Analysis of the solder joints showed that these had successfully formed during assembly, but had been fractured either before or during the pull-off test. The clean surface of the die and the smooth underfill left behind indicated that there was no adhesion between the two surfaces. There was no evidence of any voids.

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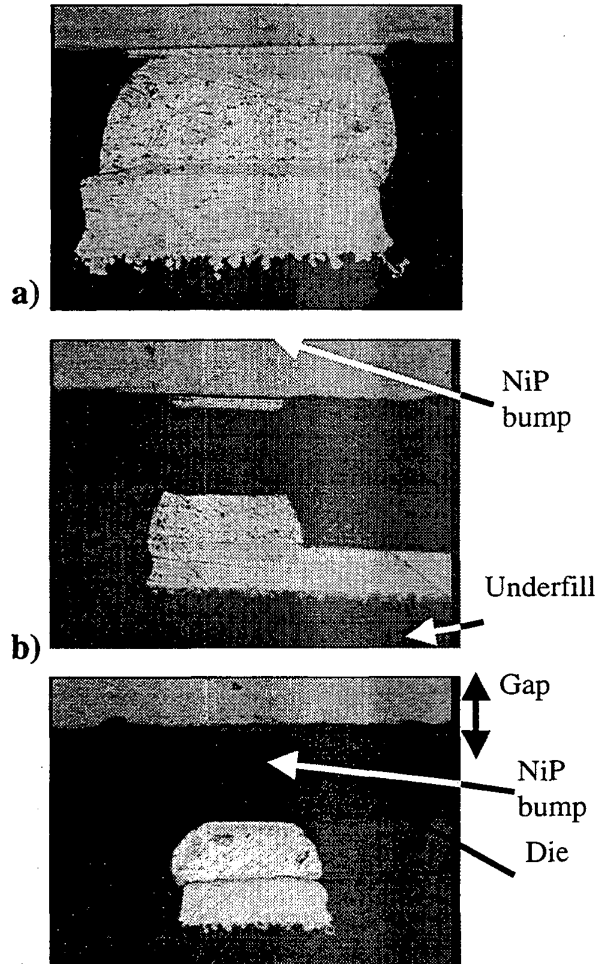

Figure 6: Cross-sections of assemblies on board 2 after 430 thermal cycles. a) site 5, no coating on die surface; b) site 4, OTS coating on die, fracture at electroless nickel - solder interface; c) site 4, OTS coating on die, fracture at e electroless nickel – aluminium interface.

Discussion

The rapid electrical failure during thermal cycling of die coated with OTS is in line with expectations regarding the delamination of the underfill – die interface. The extensive delamination observed in the SAM images of the die assembled onto board 1 is to be expected considering the poor adhesion of chip to underfill engineered into the assembly. However, the intriguing issue is the lack of evidence of delamination observable in the SAM images of the OTS coated die on board 2, despite the complete failure of the die after 220 thermal cycles. Clearly, at this stage there was no appreciable adhesion between the die and the underfill as indicated by the ease with which the die could be removed from the board surface.

The answer to this contradiction between the two boards may lie in the different accuracy of the flux application. In order for SAM to observe delamination, a separation must occur between the die and the underfill. This "void" will be either a vacuum or will contain air or other vapour produced by outgassing of the surrounding materials. It is the total reflection occurring at the interface between the chip underside and this void material that produces the strong signal in the SAM images. Sound wave transmission across an interface at which there is intimate contact between the die and the underfill, despite the absence of strong chemical bonding, is enough to produce a SAM image that does not show delamination. This is demonstrated by the images obtained before thermal cycling treatment of the die. For the die on board 1, the poor accuracy of the flux application before die placement and reflow may have provided a reservoir of material to outgas during the thermal cycling process. This gas could then create a void between chip and underfill leading to a strong reflection in the SAM image. For the die assembled onto board 2, the more accurate fluxing of only the solder balls led to far less residue being left behind in the assembly before underfill application.

Conclusion

In this paper we have demonstrated the use of low surface energy coatings to control the adhesion between the die surface and conventional underfill materials in flip-chip assemblies. These experiments have shown that it is possible to substantially reduce the adhesion of the underfill to the die surface by applying a self-assembled monolayer of octadecyltrichlorosilane (OTS) to the die before reflow and underfill application. The non-adhesion of the underfill to the die surface leads to early electrical failure of the devices. In this work, scanning acoustic microscopy has been used to monitor the delamination of the die with the surprising result that despite the almost complete non-adhesion of the die to the underfill, in certain circumstances no delamination is observable. This may be significant in that SAM has been used as an indication of the quality of device assembly, including underfill – die interface integrity, but is clearly not always able to indicate substantial regions of poor adhesion.

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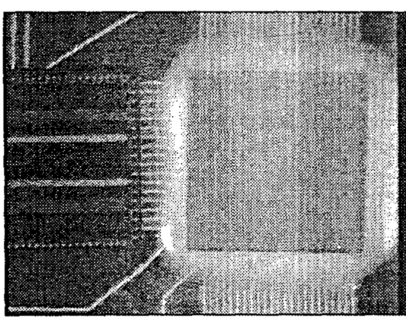

Figure 7: Underside of chip and indentation in underfill left behind after removal of die from site 1.

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