



This item was submitted to Loughborough's Institutional Repository (<https://dspace.lboro.ac.uk/>) by the author and is made available under the following Creative Commons Licence conditions.



CC creative commons
COMMONS DEED

Attribution-NonCommercial-NoDerivs 2.5

You are free:

- to copy, distribute, display, and perform the work

Under the following conditions:

BY: **Attribution.** You must attribute the work in the manner specified by the author or licensor.

Noncommercial. You may not use this work for commercial purposes.

No Derivative Works. You may not alter, transform, or build upon this work.

- For any reuse or distribution, you must make clear to others the license terms of this work.
- Any of these conditions can be waived if you get permission from the copyright holder.

Your fair use and other rights are in no way affected by the above.

This is a human-readable summary of the [Legal Code \(the full license\)](#).

[Disclaimer](#) 

For the full text of this licence, please go to:
<http://creativecommons.org/licenses/by-nc-nd/2.5/>

The Effect of Temperature Ramp Rate on Flip-Chip Joint Quality And Reliability Using Anisotropically Conductive Adhesive on FR-4 Substrate

Katrin Gustafsson¹, Samjid Mannan², Johan Liu³, Zonghe Lai³,
David Whalley² and David Williams²

¹ Department of Engineering Metals, Chalmers University of Technology,
SE- 412 96 Göteborg, Sweden

² Department of Manufacturing Engineering, Loughborough University,
Loughborough LE11 3TU, UK

³ IVF - The Swedish Institute of Production Engineering Research, Argongatan 30,
SE- 431 53 Mölndal, Sweden

Abstract

In this work, the effect of temperature ramp rate on flip-chip anisotropically conductive adhesive joint quality and reliability has been studied. The experiments were performed on bumped and unbumped die. They were assembled onto bare ITO-glass and FR-4 substrates. The reason for using the transparent glass substrate is that the particle deformation and settlement can be visualised without destroying the assembled module. The temperature ramp rates studied ranged between 8.1 and 65.7 °C/s. The experiments show that the best joint quality is obtained when a slow temperature ramp rate is applied to unbumped dies. A good joint is achieved when many particles have been entrapped on the die pad and when there is a significant degree of particle deformation. A large degree of deformation of particles results in a large contact area for the electrical conduction path. When a high temperature ramp rate is applied, there is a risk that the adhesive is already cured before full compression is reached. This will prevent the particles in the adhesive from contacting the bonding surface. When assembling bumped die, the temperature ramp rate does not seem to have a significant influence on the result.

The joint quality evaluation has been performed using Scanning Electron Microscopy (SEM) and Optical Microscopy (OM). Furthermore, temperature cycling between -40 to +125 °C, 1000 cycles, has been performed to characterise the joint reliability under the optimum temperature ramp rate conditions. The electrical resistance has been measured continuously.

A theoretical simulation of the influence of the temperature ramp rate on the adhesive joint quality has been performed using the same test module conditions as for the experimental work. The results coincide with the experimental results, particularly in the range of low bonding pressure values.

Introduction

The driving forces of achieving smaller, lighter, faster and cheaper electronics products make flip-chip joining technology one of the most important packaging technologies in the nearest future. Today, the most common flip-chip joining material is solder. Recently, there has been an increasing interest in using anisotropically conductive adhesives (ACAs) for flip-chip bonding. Compared to

soldering, ACA flip-chip joining offers the following advantages and features:

- Capability to cope with extremely small pitch, down to 70 µm pitch, which has already been demonstrated on glass substrates [1].
- Simpler processing and thereby a low-cost technology.

Today ACA flip-chip joining on glass substrates is used in digital cameras and lap-top computer applications [1], [2]. Also, recent publications investigate the feasibility of using this technology on printed circuit boards [3-10].

ACAs are generally composed of an adhesive polymer matrix and conductive fillers, where the fillers are metallic particles or metal-coated polymer spheres. When the component is attached on the substrate, some of the particles are trapped between the die pads and the pads of the substrate. The purpose of these particles is to create conductive paths between the contact areas on the chip and the metallization on the substrate. Bonding quality, reliability, and failure mechanisms during flip-chip bonding using anisotropically conductive adhesives on FR-4 and rigidified flexible circuitry have previously been reported [3], and it has been shown that the best joint reliability is obtained when all filler particles are uniformly deformed, forming a strong interatomic bond [3] through atomic diffusion. To obtain a good joint, the following factors are critical:

- Curing temperature and time of the ACA
- Bonding temperature and time,
- Temperature ramp rate
- Alignment accuracy
- Pressure value, pressure distribution and pressure application rate.
- Bump height and uniformity
- Board coplanarity

Some of the parameters above have been studied in [3]. The purpose of the work presented in this paper has been to study the effect of temperature ramp rate on ACA flip-chip joint quality and reliability on FR-4 substrates.

Experimental procedure

To study the effect of temperature ramp rate on bumped, Chip 1, and unbumped dies, Chip 2, chips have been assembled to ITO-glass and FR-4 substrates. The characteristics of the

Table I
Characteristics of test chips

Bumping condition	Test chip	Chip size (mm)	Pad size (μm)	Passivation	Pitch (μm)	No. of bumps
Bumped with electroless Ni & Au	Chip 1	4.4 x 4.6	104 x 105	Silicon dioxide	380	41
Bumpless with under bump metallization of Ni-V/Cu/Au	Chip 2	4.5 x 4.5	100 x 100	Silicon oxynitride	508 (horizontal) 381 (vertical)	32

chips used in the study are shown in Table I. Transparent glass substrates were used to visualise the particle deformation and the settlement after assembly. The adhesive used in the experiments was an anisotropically conductive adhesive of thermosetting epoxy type containing nickel particles with a size distribution of 2-10 μm and an average size of 3 μm . Two different forces were used during assembly, 15 N/chip and 140 N/chip. Four different ramp rates have been studied. These are 8.1 $^{\circ}\text{C}/\text{s}$, 9.2 $^{\circ}\text{C}/\text{s}$, 13.4 $^{\circ}\text{C}/\text{s}$ and 65.7 $^{\circ}\text{C}/\text{s}$. Flip-chip bonding was performed using bonding equipment with a beam-splitter vision system, heating and pressurisation unit as needed for flip-chip assembly. The following bonding parameters were kept constant during the experiments:

Bonding time: 30 seconds
 Bonding temperature: 180 $^{\circ}\text{C}$
 Bonding machine accuracy: $\pm 5\mu\text{m}$
 Pressure application rate: $\approx 1\text{ mm/s}$
 Bump height for the bump die: $20\pm 1\mu\text{m}$

A temperature ramp rate curve is shown in Figure 1.

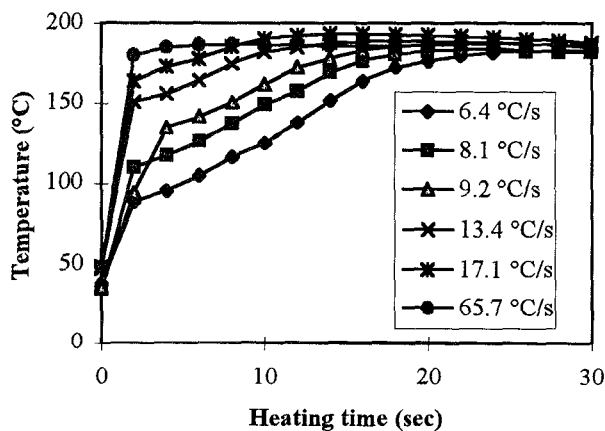


Figure 1. Temperature ramp rate curve.

The temperature cycling test was performed in a temperature cycling cabinet, from -40 $^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$ for 1000 cycles with 30 minutes dwell time at peak temperatures and 3 minutes temperature transition time.

Continuous electrical resistance values were recorded simultaneously.

Results

For Chip 1, the bumped die, the experiments showed that a good quality joint could be obtained for both a low and a high ramp rate together with both low and high pressures. For Chip 2, the unbumped die, the experiment showed a good quality joint for low ramp rate and both high and low applied pressures. The results are given in Table II. Figures 2 - 9 show the assembled joints on glass substrate. The white-looking particles have been deformed during assembly and the dark particles have not been deformed. Figures 2 - 5 are micrographs showing bumped die, after assembly. As can be seen all the particles trapped on the bumps of the chip have been deformed. This can also be seen in Figures 10a, b and 11a, b, where cross-sections of the same joints are shown. Figures 10b and 11b show a deformed particle in a higher magnification. The conclusion is that neither the temperature ramp rate nor the pressure used when assembling should make a difference regarding the quality of the joints. When looking at Figures 6 and 7 showing the unbumped dies, deformed particles are found on the pads of the chip after assembly using a slow temperature ramp rate and both high and low pressure and should therefore be a good quality joint. Cross-sections of the joints are shown in Figures 12a and b, where 12b shows a deformed particle in a higher magnification. For a high temperature ramp rate and both low and high pressure the particles in the unbumped die assembly have not been deformed (see Fig.8 and 9). The reason for this is that when too high a ramp rate is used, the adhesive is already cured before full particle compression has been reached. Cross-sections of these joints can be seen in Figures 13a and b, where 13b shows the joint in a higher magnification. Chip 1 and Chip 2 were assembled to FR-4 substrates using low pressure on Chip 1 and both low and high pressure on Chip 2. A low temperature ramp rate was used for both of the two chip types. After temperature cycling for 1000 cycles, the bumped die (Chip 1) shows stable electrical resistance as can be seen from Figure 14, with a reliability yield of 100%, (in total, 6 modules were assembled and tested), while the bumpless die (Chip 2) shows instability in electrical resistance especially in the low temperature region (-40 $^{\circ}\text{C}$), during the temperature cycling. At high temperature the joint resistance is rather stable, as can be seen from Figure 15.

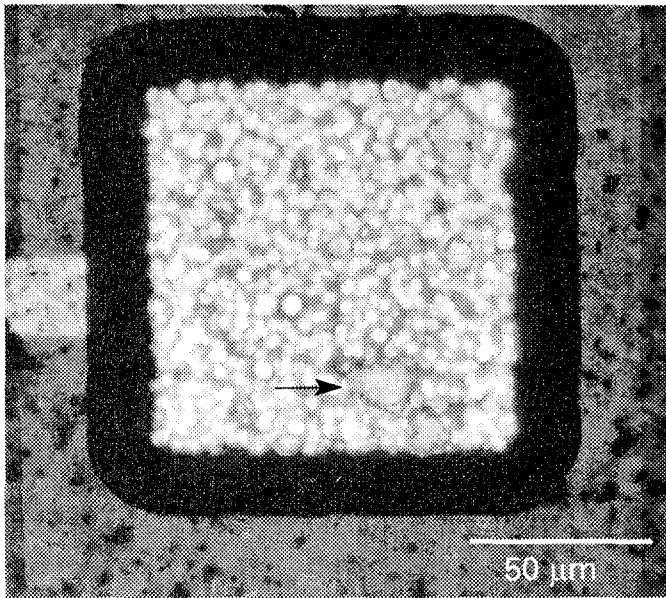


Figure 2. Bumped die (Chip1) assembled on glass substrate with a temperature ramp rate of 8.1 °C/s and an applied force of 15 N/chip. A deformed particle is indicated by an arrow.

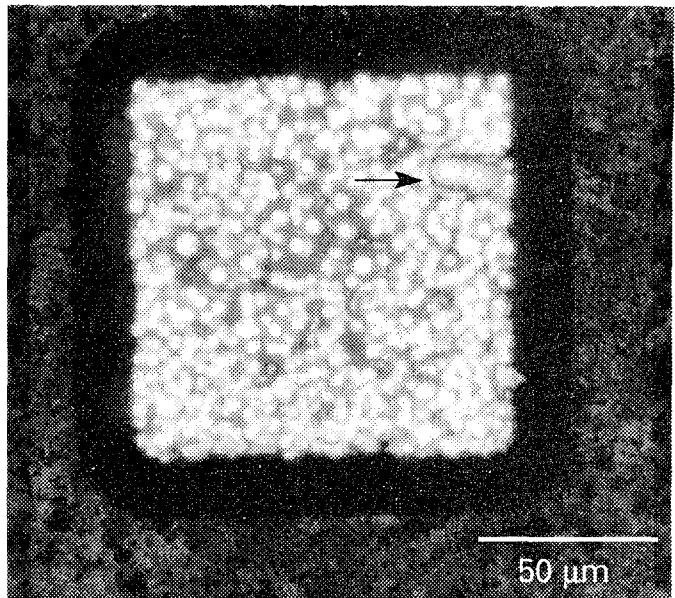


Figure 4. Bumped die (Chip1) assembled on glass substrate with a ramp rate of 65.7 °C/s and an applied force of 15 N/chip. A deformed particle is indicated by an arrow.

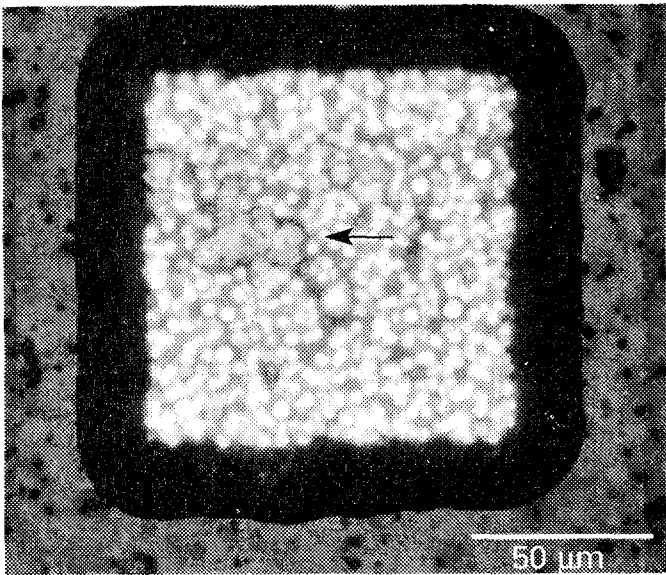


Figure 3. Bumped die (Chip1) assembled on glass substrate with a ramp rate of 8.1 °C/s and an applied force of 140 N/chip. A deformed particle is indicated by an arrow.

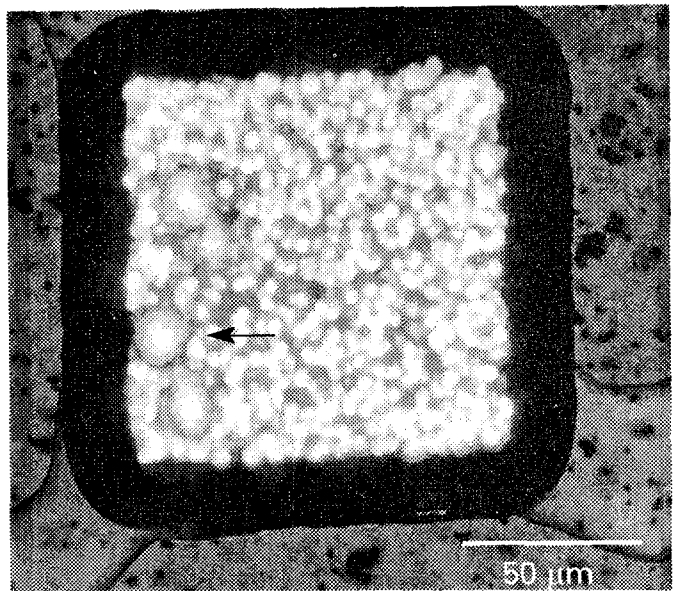


Figure 5. Bumped die (Chip1) assembled on glass substrate with a ramp rate of 65.7 °C/s and an applied force of 140 N/chip. A deformed particle is indicated by an arrow.

Table II
Results from assembly on glass substrates.

		Ramp rate (°C/s)				
		8.1	9.2	13.4	65.7	
Quality	Chip 1	15N	good	good	good	good
		140N	good	good	good	good
	Chip 2	15N	good	good	good/bad	bad
		140N	good	good	good	bad

This means that the joint failure is of type 3 [3], i.e. that the failure results from shape or height variations of the contact areas. The conductive particles are not deformed uniformly and a failure at low temperature can be caused by the undeformed particles contracting more than the deformed particles. This will result in poor conductivity preferentially at low temperature instead of at high temperature. This result differs from the result obtained after joining on glass substrate. Apparently, when working with non-linear deformable substrate such as FR-4, the substrate behaviour is an important parameter to consider.

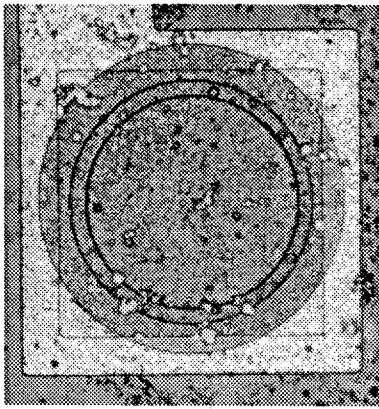


Figure 6. Unbumped die (Chip2) assembled on glass substrate with a ramp rate of 8.1 °C/s and an applied force of 15 N/chip.

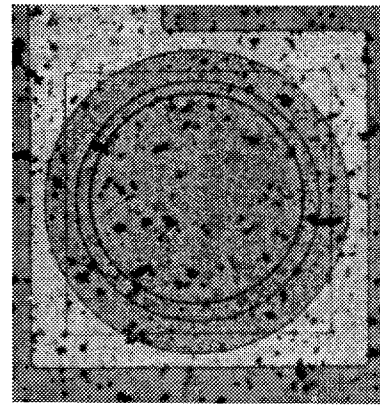


Figure 9. Unbumped die (Chip2) assembled on glass substrate with a ramp rate of 65.7 °C/s and an applied force of 140 N/chip.

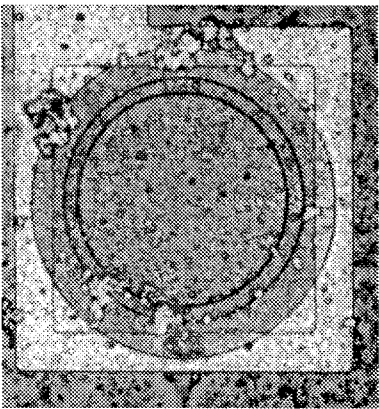


Figure 7. Unbumped die (Chip2) assembled on glass substrate with a ramp rate of 8.1 °C/s and an applied force of 140 N/chip

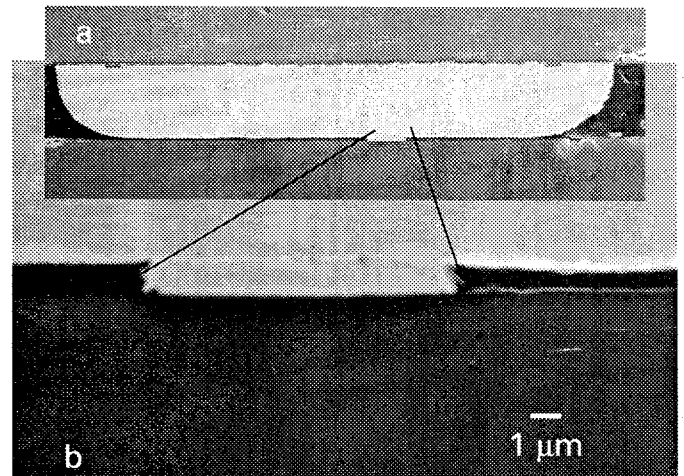


Figure 10. a) Cross-section of bumped die (Chip1) assembled with a ramp rate of 8.1 °C/s and b) a deformed particle in a higher magnification.

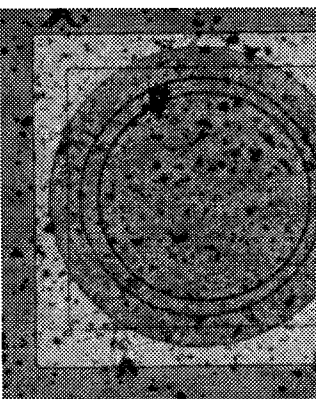


Figure 8. Unbumped die (Chip2) assembled on glass substrate with a ramp rate of 65.7 °C/s and an applied force of 15 N/chip.

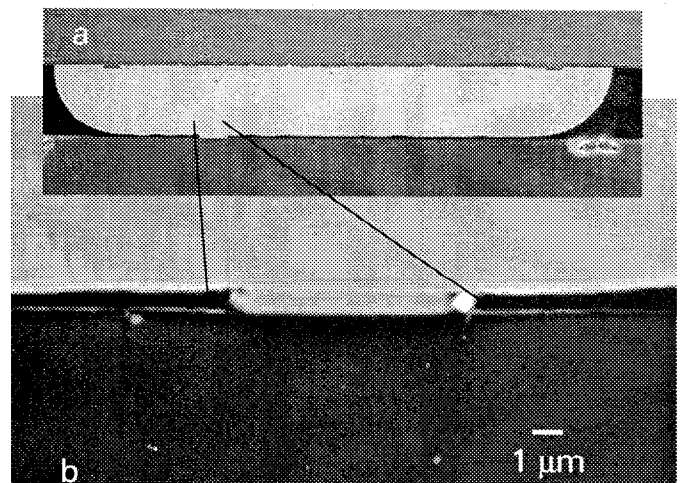


Figure 11. a) Cross-section of bumped die (Chip1) assembled with a ramp rate of 65.7 °C/s and b) a deformed particle in a higher magnification.

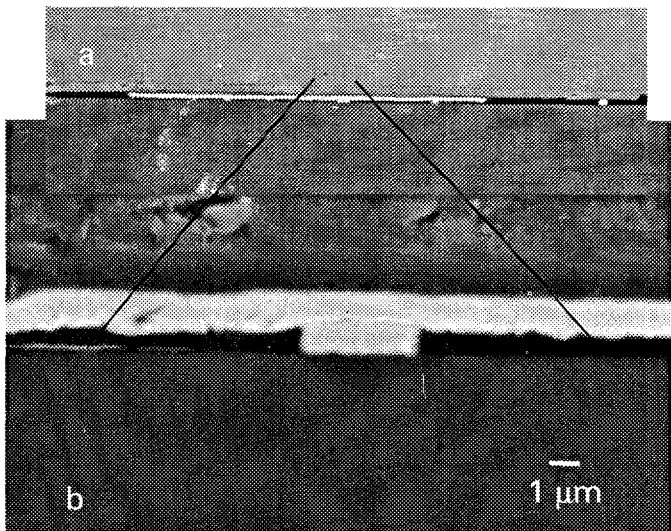


Figure 12. a) Cross-section of unbumped die (Chip2) assembled with a ramp rate of 8.1 °C/s and b) a deformed particle in a higher magnification.

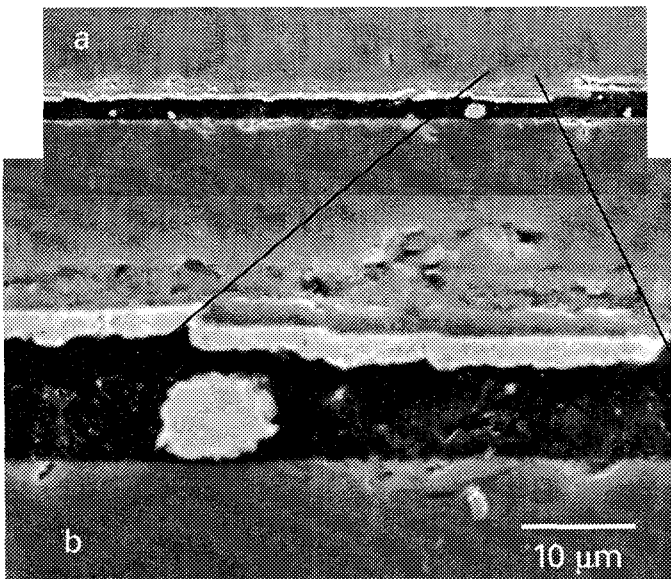


Figure 13. a) Cross-section of unbumped die (Chip2) assembled with a ramp rate of 65.7 °C/s and b) nondeformed particles in higher magnification.

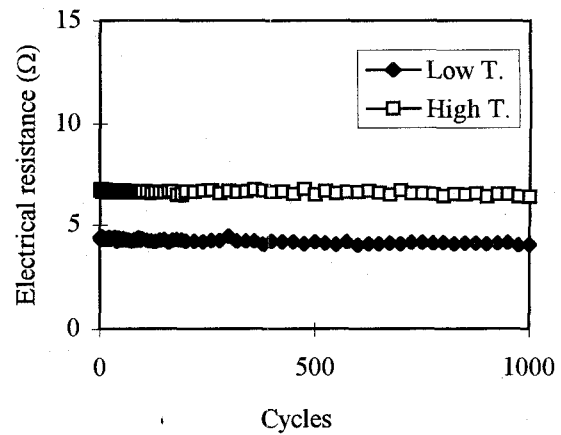


Figure 14. Electrical resistance vs. temperature cycles for bumped dies.

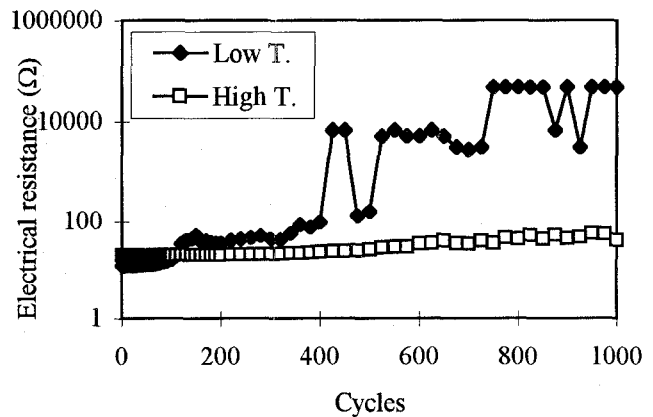


Figure 15. Electrical resistance vs. temperature cycles for unbumped dies.

Theoretical analysis

Theoretical simulations have been performed using the fluid flow models developed and reported earlier [11] for the test module configurations given in the experimental work. The results from the simulations coincide with the experimental results except in one aspect. According to the simulation it should not make any difference what temperature ramp rate is used if only a high enough pressure is applied. As can be seen in Figure 13a and b, this was not the fact in the experimental study. This could however be true for assembling on FR-4 substrates, where there are pads on both the chip and the substrate and not a flat surface as when assembling on glass substrate. On the other hand, the model developed so far does not take into account the curing effect on the fluid flow. Hence, the thermo-setting ACAs were treated as if they were thermoplastic ACAs and the results are not reliable above the region where cure is taking place. The model does however show that at low temperature ramp rates the flow will be complete before significant curing occurs.

Discussion

During the work, all the process parameters were kept constant in order to eliminate the influence of other parameters. However, when bonding on non-linear

deformable substrate such as FR-4, deformation of the substrate is a significant parameter that must be taken into account. In fact, deformation up to 2 μm during ACAs bonding has been estimated [12]. This is a rather significant value in the context that the average filler particle size is 3 μm with a variation between 2 μm and 10 μm and the bump height variation is $\pm 1\mu\text{m}$. In this work, the pressure application rate has not been varied. It has been noticed that for conventional ACA flip-chip assembly with 20 μm high bump, a much higher pressure application rate (3 cm/s) is used [13]. A higher pressure application rate for the assembly of unbumped die is therefore worth further investigation.

Conclusions

The influence of temperature ramp rate on the joint reliability has been studied in this paper. The conclusions are that when using flip-chips with bumps, the temperature ramp rate does not influence the quality and reliability of the joints. When assembling bumpless flip-chips on FR-4, the electrical resistance of the joint increases in the low temperature region during the temperature cycling test as a result of nonuniformly deformed filler particles. The non-linear deformable FR-4 substrate is another important factor that can cause joint failure. Hence, a bumped die is necessary to obtain a good electrical reliability.

Acknowledgements

This work has been financially sponsored by the participating companies within the multiclient research program "Flip-chip joining using conductive adhesives, phase II": Ericsson Telecom, Ericsson Components, Alfa Laval Automation and Mydata Automation, Sweden; Delco Electronics Delphi Packard Electric Systems and Epoxy Technology, USA; Hitachi Chemicals and Namics, Japan; Schneider Electric, France; Robert Bosch, Deutsche Thomson-Brandt, Germany; Philips CFT, The Netherlands. Financial support has also been received from the National Swedish Board for Technical and Industrial Development (NUTEK).

References

- [1] T. Kubota, T. Kimura and S. Ushiki, "COG(Chip-on-glass) Mounting of Si and GaAs devices," Proceedings of 1991 Japan international electronic manufacturing technology symposium, June 26-28, Tokyo, Japan, 1991, pp. 188-191.
- [2] J. Liu and L. Ljungkrona, "Reliability of thermo-setting anisotropically conductive adhesives in Chip on Glass application," *Microsystem Technologies*, Springer-Verlag, Vol 2, 1995, No 17, pp.32-37.
- [3] Lai Z-H. and Liu J., "Anisotropically Conductive Adhesive Flip-Chip Bonding on Rigid and Flexible Printed Circuit Substrates", *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B*, vol 19, no. 3, August 1996, pp.644-660.
- [4] Bela Rösner, Johan Liu and Zonghe Lai, "Flip-Chip bonding using isotropically conductive adhesives," Proceedings of the 46th Electronic Components and Technology Conference (ECTC), May 28-31, 1996, Florida, USA, pp.578-581.
- [5] Johan Liu and Zonghe Lai, "Flip-chip joining for solderless multi-chip modules assembly using anisotropic and non-conductive adhesives," *Journal of Surface Mount Technology*, pp.37-42.
- [6] Johan Liu, Katarina Boustedt and Zonghe Lai, "Development of Flip-chip Joining technology on flexible circuitry using anisotropically conductive adhesives and eutectic solder," *Circuit World*, Vol.22, No 2, 1996.
- [7] Markus Dernevik, Rolf Sihlbom, Zonghe Lai, Piotr Starski and Johan Liu, "High-frequency measurements and modelling of electrically conductive adhesive flip-chip joint, to be published at the Interpack '97, The Pacific Rim / ASME International, Intersociety Electronic & Photonic Packaging Conference, Sheraton Orchid Hotel, Hawai'i, USA, June 15-19, 1997.
- [8] N R Basavanahally, D Chang, B Cranston and S G Segar, "Direct chip interconnection with adhesive conductor film", *IEEE Transactions on Components, Hybrids, and Manufacturing technology*, Vol.15, No 6, December 1992, pp 972-976.
- [9] N Shiozawa, K. Isaka and T. Ohta, "Electrical properties of connections by anisotropic conductive film", *Journal of Electronics Manufacturing*, Vol. 5, No. 1, (March 1995), pp 33-37.
- [10] A. M. Lyons, E. E. Hall, Y. H. Wong and G. Adams, "A new approach to using anisotropically conductive adhesive for flip-chip assembly", proceedings of the 45th Electronic Components Technology Conference, Las Vegas, USA, May 21-24, 1995, pp 107-113.
- [11] S.H.Mannan, D.C.Whalley, A.O. Ogunjimi and D.J. Williams, "Modelling of the initial stages of the anisotropic adhesive joint assembly process," proceedings of 1995 Japan IEEE IEMTS, Omiya, December 4-6, 1995, pp.142-145.
- [12] S.H. Mannan, D.J.Williams, D.C. Whalley and A.O. Ogunjimi, "Models to determine Guidelines for the Anisotropic Conducting Adhesive Joining Process" in "Conductive Adhesive Joining in Electronics Packaging" edited by Johan Liu, to be published by Electrochemical publications, September 1997.
- [13] Itsuo Watanabe, Hitachi Chemicals, Private Communication, December 1996.