Modelling of realistic annealing behaviour of amorphous silicon photovoltaic devices

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Abstract

Long-term degradation and annealing behaviour of a-Si mini-modules is investigated in this paper. Four devices were firstly degraded by light and then annealed in the dark at temperatures ranging from 65-85°C. Dark annealing rates were obtained for each temperature. Further annealing with light bias was carried out for two of the devices in order to study the interaction between the light-induced degradation and thermal annealing process. Results demonstrate that the annealing in the dark is strongly influenced by the operating temperature but also dependent on the history of the devices. Annealing is a self-limiting process and is significantly influenced by the light intensity in the short-term exposure, giving rise for a balance-equation for modelling purposes.

Introduction

Amorphous Silicon (a-Si) photovoltaic (PV) modules suffer from light-induced degradation [1], which can be recovered by annealing modules at elevated temperatures. The annealing process is triggered by the device operating temperature. Typically, this is a temperature threshold for the process. Devices with temperatures below the threshold see hardly any or no annealing, whereas devices with temperatures above the threshold can be annealed enough to affect device's performance.

This paper investigates annealing behaviour of degraded amorphous silicon (a-Si) devices under temperatures occurring in the field. The long-term aim is to model the device's seasonal and lifetime ageing behaviour in dependence of realistic operating conditions. The paper compares annealing at different temperatures, with and without the presence of light that undertaken in indoor controlled irradiance and temperature environments. This is to investigate the impact of annealing and degradation on the device electrical performance and get a better understanding of the physics of the annealing process in general.

The rate of annealing is largely determined by the temperatures above the threshold. In the literature [2,3], most of the research studies the annealing at elevated temperatures, e.g. 120°C or higher, where the annealing rate is relatively fast. In this work, the normal field operating temperatures, which is lower than 85°C typically, is the focus and much slower annealing rates are expected. The aim is to identify eventual saturation and to identify annealing rates. This is the reason that up to 3600 hours of annealing was implemented to see the change in device power.

The annealing is expected not to be indefinite. The saturation of annealing process depends on a number of factors such as device operating condition and device history. Light complicates the situation as two processes, i.e. degradation and annealing, work in parallel against each other. This is studied in terms of indoor light annealing tests. The influences of operating temperature and device history on the annealing behaviour are investigated. The knowledge gained from the observations will be the basis of an ageing model for a-Si devices to be developed at CREST.

Indoor degradation and annealing stress test

Indoor controlled degradation and annealing tests up to 4800 hours have been carried out at CREST for four a-Si mini-modules in order to investigate the device ageing and annealing behaviours.

The four mini-modules have been firstly degraded for 1000 hours under the conditions of 250-350 W/m^2, 15-44°C, respectively. Different irradiance and temperature conditions led to different degradations. The power at maximum power point (P_{MPP}) of the four devices degraded between 27-36% during the light soaking. The temperatures for the four mini-modules have been kept below 45°C so

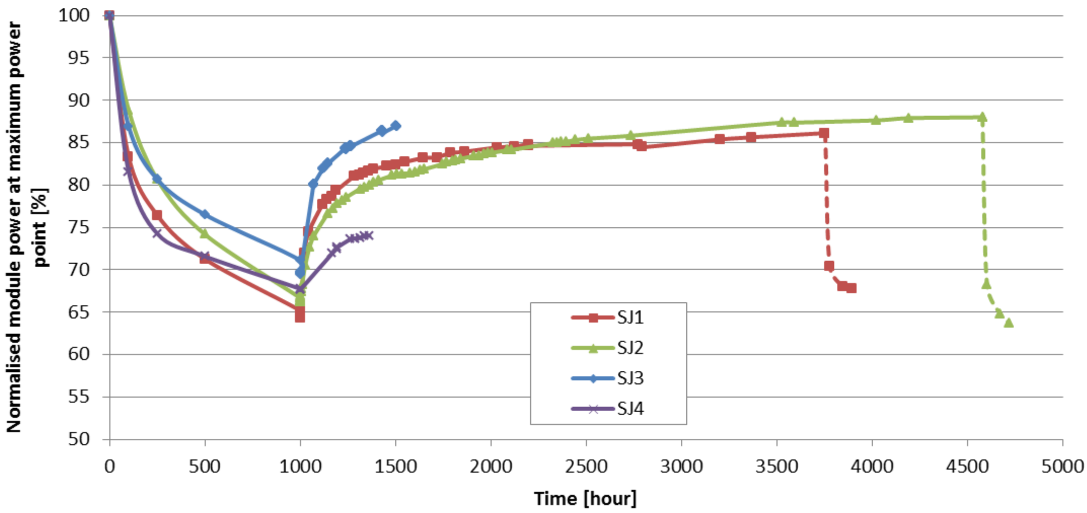

Figure 1: Overview of power variation during the light soaking, dark annealing and light annealing (dashed lines) of a-Si mini-modules

that no annealing effect on degradation is assumed.

Thermal annealing at different temperatures, i.e. 65°C, 75°C and 85°C, in the dark condition has been applied to the four devices after the light soaking. Device SJ1 and SJ3 have been annealed at 85°C for 2800 hours and 500 hours respectively. Device SJ2 has been annealed at 75°C for 3600 hours and device SJ4 has been annealed at 65°C for 400 hours. The recoveries of P_{MPP} were observed for all of the devices as shown in Figure 1. Different annealing temperatures led to different power recovery rates.

After the dark annealing, two of the devices with longest annealing exposure SJ1 and SJ2, have been exposed to light again, but kept at the annealing temperatures. This is to investigate how the light degradation and thermal annealing process works against each other.

An overview of the P_{MPP} variation for the four mini-modules during the light soaking, dark and light annealing is demonstrated in Figure 1.

Dependency of annealing on operating temperature

The rate of annealing a-Si devices is largely determined by the temperature. Operating temperatures over 85°C, which may accelerate the annealing process significantly is not the interest of the work. This section investigates the annealing rate at realistic outdoor operating conditions.

Device SJ1, SJ2 and SJ4, which have been annealed at 85°C, 75°C and 65°C respectively, are studied in this section. As light-induced degradation only can be annealed and recovered, the percentage of power recovery is used to evaluate the device annealing rate and defined in Eq (1):

$$Recovery\ percentage = \frac{\Delta P_{rec}}{\Delta P_{deg}} \quad (1)$$

where ΔP_{rec} is the recovered power by the thermal annealing and ΔP_{deg} is the degraded power by the light soaking. The calculated power recovery for the three mini-modules are plotted in percent versus the annealing time in Figure 2.

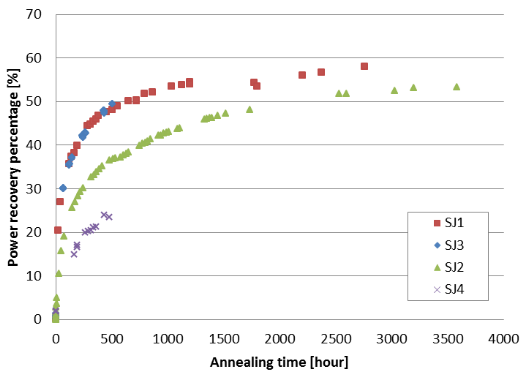

Figure 2: Percentage of power recovery of devices annealed at different temperatures

Figure 2 shows that the power recovery due to annealing is fast at the first 500 hours and becomes slow and saturates afterwards, though the absolute saturation was not observed yet after 3600 hours. The behaviours follow a stretched exponential style. Power recovery rate at higher temperatures is faster than that at lower temperatures as expected. Taking the derivative of the results shown in Figure 2 with respect to the annealing time, the averaged annealing rate per hour can be calculated at and plotted versus the annealing time in Figure 3.

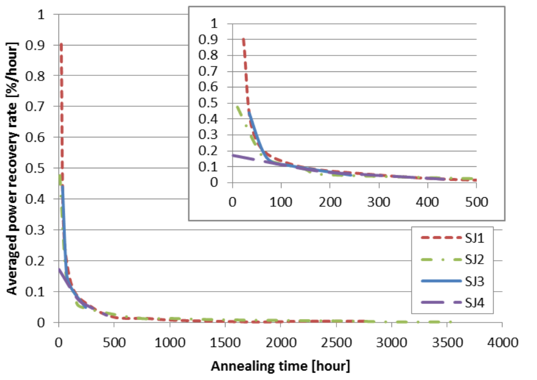

Figure 3: Averaged power recovery (annealing) rate per hour versus annealing time

The device annealed at 85°C (SJ1) has an averaged annealing rate of 0.9%/hr at beginning, which decreases to 0.14%/hr after 100 hours. It keeps at 0.02%/hr after 500 hours. The device annealed at 75°C (SJ2) has the annealing rates of 0.5%/hr at initial stage, 0.12%/hr after 100 hours and retains below 0.02%/hr after 500 hours. The device annealed at 65°C (SJ4) has the lowest annealing rate of 0.17%/hr at initial stage. It decreases to about 0.1%/hr after 100 hours and to 0.02%/hr after 500 hours. Significant differences in the annealing rates at different temperatures were observed in the first 100 hours and the differences became less significant after 100 hours of annealing and after 500 hours the differences were tiny.

Dependency of annealing on degradation history

The device SJ1 and SJ3 have different light-induced degradation history. SJ1 degraded 36% in power while SJ3 degraded 27% over 1000 hours light soaking. According the defects pool theory [4,5], the larger degradation means more light-induced defects are generated, which in term means that more available defects can be annealed.

The two devices were annealed at the same temperature of 85°C. By calculating the percentage of power recovery versus the annealing time as shown in Figure 4, one can observe almost no difference in the recovery curve between the two devices. However, the same recovery curve (same indicates that the two devices recovered different absolute power ΔP_{rec}, i.e. SJ1 recovered 21% of its initial power and SJ3 recovered 16% of its initial power. Thus, the ΔP_{rec} of a-Si devices investigated in this paper depends on the light-induced degradation history, i.e. degraded more, and thus recovered more. This needs to be taken into account when developing the device ageing model.

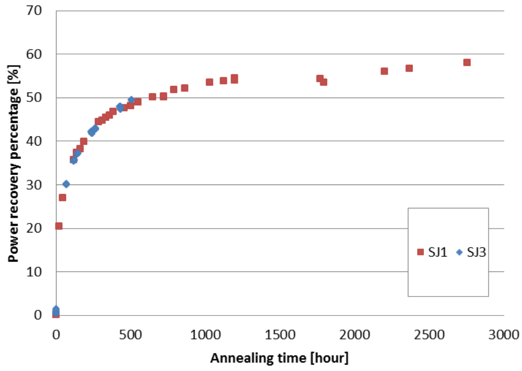

Figure 4: Percentage of power recovery of devices with different degradation histories

Annealing in the presence of light

Two devices SJ1 and SJ2 annealed in the dark have been exposed to the light for 100 hours, but kept at the annealing temperatures of 85°C and 75°C, respectively, as shown in Figure 5. Referring to the result of power variation in Figure 1, it shows that device SJ1 degraded by 18.5% and SJ2 degraded by 24.3% of their initial powers respectively after 100 hours light exposure. The degradation rates are even faster than their initial light-induced degradation rates, which may be due to the stronger light intensity (500-530W/m^2) received by the two devices.

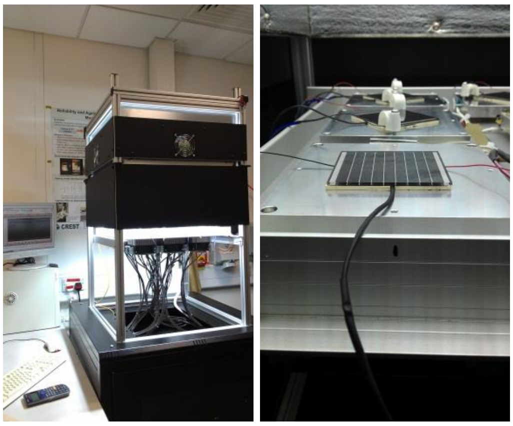

Figure 5: Light annealing of a-Si mini-modules

The light significantly degraded the devices though they were annealed at temperatures up to 85°C. The two devices will be further light-annealed and monitored continuously. Once the light-induced degradation effect becomes less significant, the annealing effect may start to affect the device long-term ageing.

Modelling of a-Si annealing

The modelling of a-Si annealing and long-term ageing is based on the theory of the so-called 'defects pool' model [4]. The light generates defects in the pool, whereas the annealing recovers these defects. The annealing rates in the dark and under light are investigated and the knowledge gained is used in model development. The dark annealing rate (R_a) can be modelled by the stretched exponential function:

$$R_a = e^{-(t/\tau)^{\beta}} \quad (2)$$

where the t is the annealing time, τ and β are parameters depending on the annealing temperature and saturation behaviour. A good fitting of τ=22 and β=0.44 is obtained for the annealing at 75°C, whereas τ=77 and β=0.84 for 85°C and τ=4 and β=0.28 for 65°C. The fitted values of τ and β are thus plotted versus the annealing temperature in Figure 6. Clear trends show that both of the τ and β increase with increasing annealing temperature.

The absolute power recovered by annealing depends on the amount of power degraded by light and can be expressed by Eq (3):

$$\Delta P_{rec} = \Delta P_{deg} \int R_a t dt \quad (3)$$

The modelling of light annealing needs more data. But the initial observation of SJ1 and SJ2 confirms the light intensity largely determines the device behaviour, though the spectral and loading conditions may influence it too.

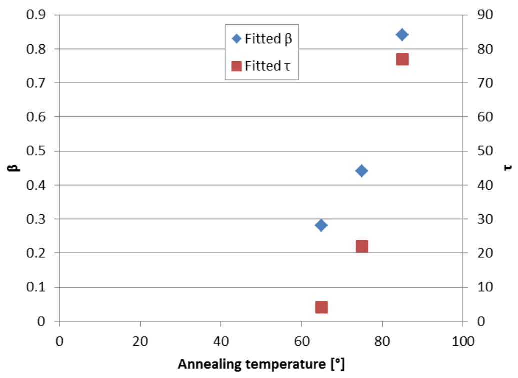

Figure 6: Fitted τ and β versus annealing temperature

Conclusions

The long-term indoor degradation and annealing test for a-Si mini-modules was carried out and is continuing at CREST. Dark annealing effect depends on the annealing temperature significantly in the first 100 hours of annealing and becomes almost independent of temperature after 500 hours. The annealing also depends on the operating history of devices. A model based on the stretched exponential function is developed for modelling the dark annealing rate. The effect of light-induced degradation outreached the effect of annealing at realistic field temperatures during the short-term exposure. Further test will investigate the long-term interaction between the two processes.

Acknowledgements

This work has been supported by a joint UK-India initiative in solar energy through a joint project "Stability and Performance of Photovoltaics (STAPP)" funded by Research Councils UK (RCUK) Energy Programme in UK (contract no: EP/H040331/1) and by Department of Science and Technology (DST) in India.

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