Effect of varying process parameters on CdTe thin film device performance and its relationship to film microstructure

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***Abstract* — The performance of CdTe thin film photovoltaic devices are sensitive to process parameters. In this study efforts are made to further understand the effects of process parameters like process temperature as well as variation in cadmium chloride passivation treatment on CdTe films deposited using closed space sublimation (CSS). Here the effects on film microstructure and electrical performance are studied using electrical measurements and advanced microstructural characterization methods. Electrical performance is studied using current density vs. voltage and electroluminescence. Transmission Electron Microscope, Scanning Electron Microscope and Secondary Ion Mass Spectroscopy are used for material characterization. The aim of this study is to provide new insight into the understanding of device performance and its relationship with thin film microstructure.**

***Index Terms* — Cadmium Chloride, Cadmium Telluride, Closed Space Sublimation, Photovoltaics, Solar Cell, Thin Film Photovoltaics.**

I. Introduction

CdTe thin film Photovoltaics is an important technology for production of utility scale solar electricity. With recent improvements research scale small devices have recorded efficiency of 19.6% [1] while modules with up to 16.1% efficiency [1] has been produced. CdTe is a p-type absorber layer in such films. Band gap of CdTe is 1.45 eV which is optimum for photovoltaic conversion. It also has a high coefficient of absorption which implies that a very thin film (~2 μm) is required for absorption of most of the solar spectrum. CdTe may be deposited using various methods including but not limited to Electroplating, Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD), Metal Organic Chemical Vapor Deposition (MOCVD), Closed Space Sublimation (CSS) and Sputtering. Studies have shown that cells made from as deposited films exhibit poor efficiency which is attributed to high density of stacking faults present in grains of the film [2].

An important process step in the fabrication of high efficiency CdTe photovoltaic devices is the cadmium chloride ($CdCl_2$) passivation treatment. This passivation treatment radically improves film microstructure and electrical characteristics of CdTe photovoltaic devices [3]. Cells made from as deposited CdTe films exhibit under 1% efficiency while passivation treatment improves the efficiency to ~13%. An earlier study has shown that annealing treatment in absence of $CdCl_2$ reduces the density of stacking faults in CdTe grains [4]. However, the treatment time and temperature without $CdCl_2$ does not have substantial effect on electrical performance and cell efficiency persists to be low. Use of cadmium chloride helps completely remove the stacking faults [2,5]. Studies carried out on closed space sublimation have also shown that the recrystallization process initiates preferentially at the CdTe/CdS interface [6]. This study concentrates on variation of deposition temperature as well as varying passivation treatment of CdTe films. The change in electrical performance and respective microstructural changes are reported here. Goal here is to provide a further insight into the microstructural changes that occur due to change in process parameter and in turn relate them to the changes in electrical performance of CdTe thin film photovoltaic devices.

II. Experimental Details

CdTe thin films are deposited at CSU using closed space sublimation on NSG-Pilkington TEC 12 soda lime glass that is coated with Fluorinated Tin Oxide (FTO) that acts as a Transparent Conducting Oxide (TCO) to reduce sheet resistance. A continuous vacuum process is carried out to deposit the films in a superstrate configuration. Graphite vapor sources are heated to the sublimation temperatures of the respective materials. The superstrate is passed thorough different chambers under 40 mTorr vacuum while the substrate is kept a few millimeters above the vapor source. A ~ 120 nm layer of cadmium sulfide is first deposited onto FTO layer with the superstrate inverted followed by ~2 μm layer of CdTe. Cadmium chloride passivation treatment at 400 ˚C in 2% oxygen atmosphere is then carried out followed by annealing. The optimum passivation treatment time for these kind of films is 120 seconds that is considered as the standard here. Following this a copper doping process is carried out [7,8].

For electrical characterization current density vs. voltage, open circuit voltage, short circuit current, fill factor and percentage efficiency data are collected using a JV tester that was fabricated and optimized in the Department of Physics at Colorado State University. Electroluminescence (EL) images are collected and studied using an EL setup that was fabricated and optimized in the Department of Physics at Colorado State University [9].

In depth microstructure characterization of the CdTe film is carried out using Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM) and High Resolution Transmission Electron Microscopy (HRTEM). TEM samples are prepared using Focused Ion Beam (FIB) milling using dual beam FEI Nova 600 Nanolab. A standard in situ lift out method is used to prepare the cross section sample through the film stack into the glass substrate. A platinum overlay is deposited on the top of the film to define the area of interest on surface of the sample, homogenize the final thinning of the samples and to avoid damage to the CdTe film surface from ion beam. STEM bright-field images and high resolution TEM images are captured using a FEI Tecnai F20 (S)TEM operating at 200 kV. TEM studies are performed at University of Loughborough, UK. Scanning Electron Microscope images are obtained using Jeol JSM-7000F SEM at Colorado State University's Central Instrumentation Facility.

III. Cells with Standard Process Conditions

Standard samples are prepared by baking the substrate at 620 °C. Thereafter a 120 nm CdS layer is deposited at 617 °C followed by deposition of the CdTe layer. Entering the CdTe source the temperature of the substrate is 445 °C. This is followed by $CdCl_2$ deposition where the substrate temperature when it enters the $CdCl_2$ source is 406 °C. The temperature of the substrate at each stage is determined using advanced thermal modeling software that is designed using LabVIEW.

As mentioned earlier, grains of CdTe layer have very high density of stacking faults before $CdCl_2$ passivation treatment is carried out. The difference between the internal structures of such grains can be observed in the HRTEM images in fig. 1.

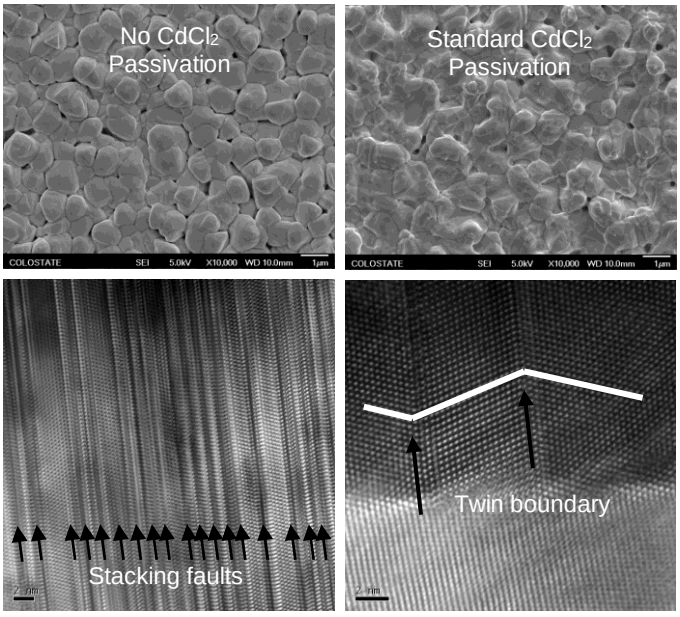

Fig. 1. HRTEM micrograph showing effect of $CdCl_2$ passivation on stacking fault in CdTe grains in standard samples.

TABLE I
Electrical Performance of Standard Devices

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	%Π
Standard Sample, No Passivation	531	8.5	34.3	1.5
Standard Sample, Standard Passivation	790	20.6	72.2	11.8

Table 1 shows the electrical measurements of the standard CdTe cells with and without $CdCl_2$ treatment to help understand the effect on device performance. As can be observed in Table I, there is a dramatic improvement in cell device performance after standard $CdCl_2$ treatment is performed as compared to cells fabricated from as deposited CdTe films without any passivation treatment.

IV. Cells with Lower Substrate Temperature

To understand the effect of deposition temperature, cells are fabricated with CdTe deposited at 100°C lower than the standard substrate conditions. The cells are analyzed before and after the $CdCl_2$ treatment.

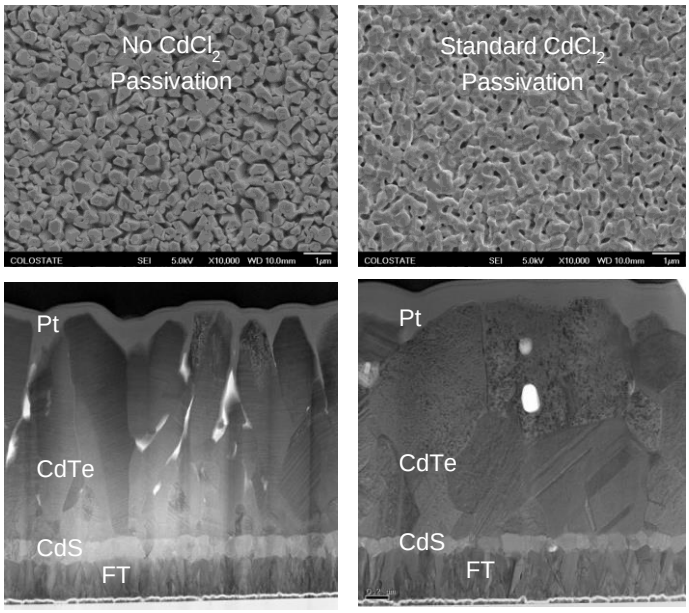

Fig. 2. Surface SEM (top) and cross section BF-STEM (bottom) micrograph showing effect of $CdCl_2$ passivation on stacking fault and grain structure in CdTe grains in low temperature samples.

Films without the passivation treatment show highly columnar CdTe grains, as well as a high density of smaller grains nucleating above the CdS layer. Also, it must be noticed that the voids at the CdTe free surface go deep between CdTe grains which can act as sites for chlorine accumulation when $CdCl_2$ passivation is carried out. This is highly undesirable. On carrying out the standard $CdCl_2$ treatment on the same films show recrystallization and elimination of stacking faults. It is

also observed that there are CdTe grains stacked one over the other which would potentially increase the resistance to the movement of electrons as they travel through the grain boundaries. It is desirable to reduce stacking of grains to reduce this resistance and have large grains that grow from CdTe/CdS interface all the way to free surface of the film.

Electroluminescence image of cells deposited at low substrate temperature that underwent a standard $CdCl_2$ passivation treatment show lower intensity and substantial non-uniformity. Cells without $CdCl_2$ passivation have very low signal intensity under electroluminescence test and therefore does not produce an image on a logarithmic scale. The dark spots observed in the standard cell are dead spots in the cell. Cell deposited at lower substrate temperature shows some regions that are bright and have darker center. Such regions suggest higher electron flow around the darker center that provides greater resistance to their flow.

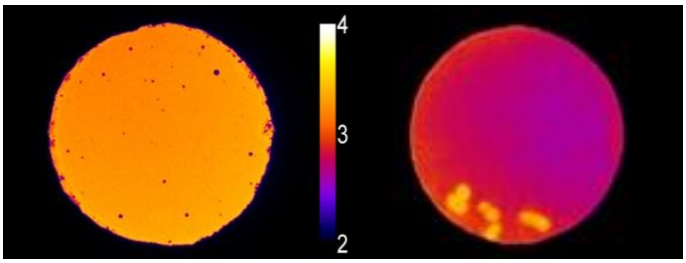

Fig. 3. Electroluminescence image of standard CdS/CdTe cell (left) as compared to cell with absorber CdTe deposited at lower substrate temperature (right).

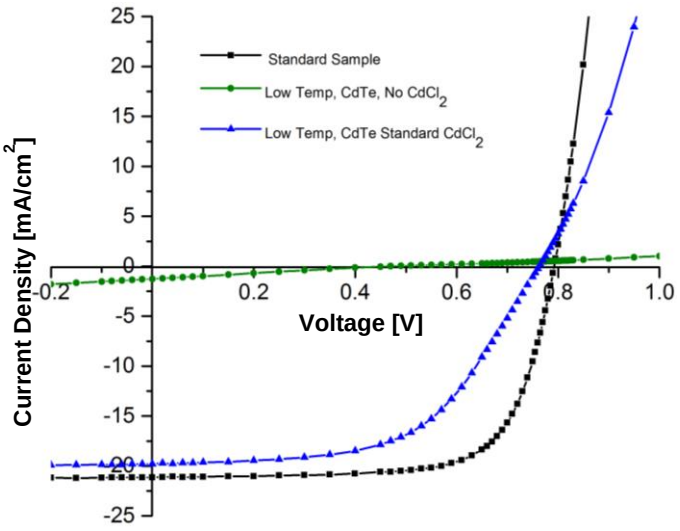

Fig. 4. Current density vs. Voltage for cells with CdTe layer deposited at 100 °C lower substrate temperature.

Cells deposited at lower substrate temperature exhibit poor electrical performance even after standard $CdCl_2$ treatment when compared to a standard CdTe/CdS device. As can be observed in figure 4, such cells have a lower short circuit current as well as lower open circuit voltage. A considerable drop in fill factor is seen and consequences of these in form of poor efficiency are clearly reflected. Electrical performance of these devices which support these observation are summarized in Table II.

TABLE II
ELECTRICAL PERFORMANCE OF LOW TEMPERATURE DEVICES

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	%∩
Standard Sample with Standard Passivation	790	20.6	72.2	11.8
Low Temp CdTe, No Passivation	474	12.7	23.1	1.4
Low Temp CdTe, Standard Passivation	763	19.8	56.2	8.5

V. CELLS WITH HIGHER SUBSTRATE TEMPERATURE AND VARYING PASSIVATION CONDITIONS

Cross section transmission electron micrographs of CdTe grains deposited at 65 °C higher substrate temperature are shown in figure 5. Large density of stacking faults is observed in film that did not undergo $CdCl_2$ passivation treatment. However, standard passivation treatment that causes recrystallization in CdTe absorber layer, eliminated stacking faults and smaller CdTe grains at CdTe/CdS interface are not observed.

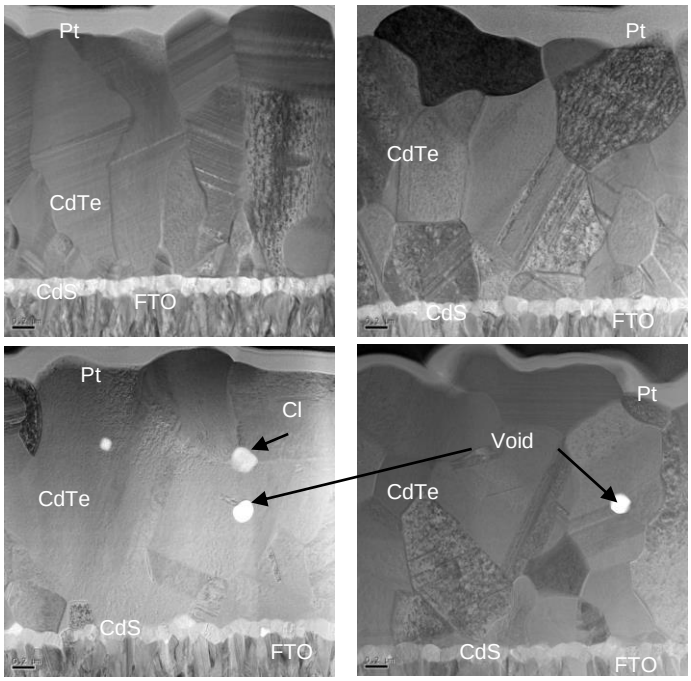

Fig. 5. Cross section BF-STEM micrograph showing effect of $CdCl_2$ passivation on stacking fault and grain structure in CdTe grains in high temperature samples. No passivation (top left), standard passivation (top right), 2 times longer passivation (bottom left) and 10°C higher substrate temperature during passivation (bottom right).

Longer passivation causes further recrystallization where the CdTe grains are larger than in case of standard $CdCl_2$ treatment and reduction of stacking faults is also visible.

However, longer treatment caused chlorine rich regions to form in the CdTe film stack, which had a detrimental effect on device performance.

While the cells that have higher temperature passivation treatment with standard treatment time, have large grains with no stacking faults. No chlorine rich areas are observed in these films. Contradictory to the films with no $CdCl_2$ treatment, these films do not have concentration of smaller CdTe grains at the CdTe/CdS interface.

$CdCl_2$ treatment of the films substantially improved cell performance when compared to films without any $CdCl_2$ treatment. Moreover, considerable variations in device performance are observed with variation in $CdCl_2$ treatment parameters.

Cells prepared from films deposited at higher substrate temperature with 2 times longer standard $CdCl_2$ treatment have comparable short circuit current as compared to cells prepared from films with standard $CdCl_2$ treatment. However, the open circuit voltage and fill factor see a considerable reduction that causes the overall device efficiency to drop. This can be attributed to the higher concentration of chlorine at the grain boundaries as well as chlorine accumulation in voids between grains. Cells prepared using films with 10 ºC higher temperature $CdCl_2$ treatment again have comparable short circuit current and device efficiency. There is an improvement in open circuit voltage and fill factor when compared to standard cell as well as high temperature cells with standard $CdCl_2$ treatment.

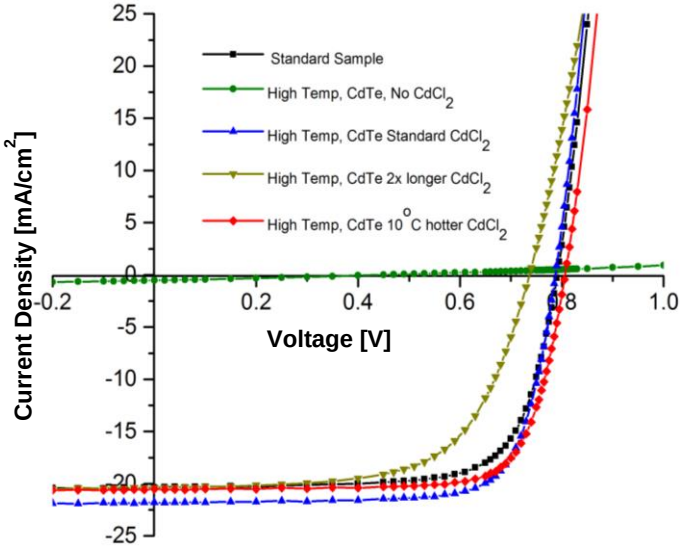

Fig. 6. Current density vs. Voltage for cells with films deposited at 65°C higher substrate temperature with varying $CdCl_2$ passivation treatment.

It is observed that films deposited at higher substrate temperature, with standard as well as higher temperature $CdCl_2$ treatment, exhibit considerable increase in fill factor and device efficiency when compared to standard cell. Table III below summarizes the above mentioned observations that provides a better understanding of the cell performance.

TABLE III
ELECTRICAL PERFORMANCE OF HIGH TEMPERATURE DEVICES

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	%Ƞ
Standard Sample with Standard Passivation	790	20.6	72.2	11.8
High Temp CdTe, No Passivation	440	5.3	28	0.65
High Temp CdTe, Standard Passivation	787	21.8	75.6	13
High Temp CdTe, 2x Longer Passivation	735	20.4	63.6	9.56
High Temp CdTe, 10°C Hotter Passivation	806	20.5	76.2	12.6

Electroluminescence images of these devices give a good understanding of uniformity. Lower efficiency of cells with 2 time longer treatment time is manifested in the form of poor intensity in electroluminescence image. This cell also shows poor uniformity as can be seen in figure 7.

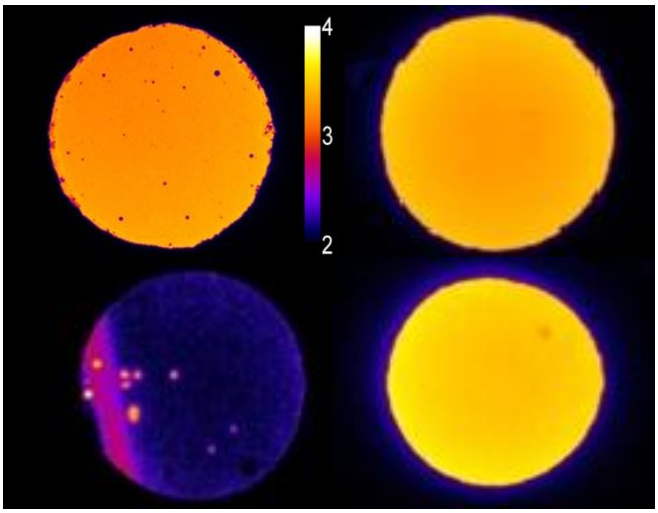

Fig. 7. Electroluminescence image of standard CdS/CdTe cell (top left) as compared to standard passivation with 65 ºC higher substrate temperature (top right), 2 times longer passivation (bottom left) and 10ºC higher substrate temperature during passivation (bottom right).

Higher substrate temperature cells with standard and 10 ºC hotter $CdCl_2$ treatment have very good uniformity with no dead spots. These cells also have better intensity as compared to a standard cell. Cell with 10 ºC hotter $CdCl_2$ treatment temperature with 65 ºC higher substrate temperature give the best intensity as well as uniformity within the scope of this study. This suggests that such process conditions result in better uniformity and intensity of CdTe photovoltaic devices along with improved open circuit voltage.

VI. Understanding the Detrimental Effect of Longer Passivation Treatment

It is observed in the earlier section that a 2 times longer $CdCl_2$ passivation treatment results in poor cell performance. Chlorine is understood to be diffusing through the grain boundary during annealing process. Recrystallization of CdTe grains initiates preferentially at the interface of CdTe and CdS. Figure 5 shows a void between the grains that has very high concentration of chlorine in film that has 2 times longer $CdCl_2$ treatment. Similar voids away from the grain boundary and located inside the CdTe grains do not show any such chlorine rich areas. This supports the observation that chlorine diffuses through the grains to reach the interface of CdTe and CdS. Secondary Ion Mass Spectroscopy depth profile shown in figure 8 shows high concentration of chlorine at the surface and at the interface of CdTe and CdS. No such chlorine rich regions are seen in the CdTe absorber layer. There are no signs within the scope of this study that suggest that chlorine enters the grains to cause recrystallization and change of other material properties that in turn bring about the improvement in device performance. Based on these observation it may be deduced that poor performance of cells with longer $CdCl_2$ treatment is due to chlorine build up at the interface of CdTe and CdS. In addition, possibility of chlorine gathering at CdTe grain boundaries cannot be ruled out that may further cause deterioration in electrical performance of such cells.

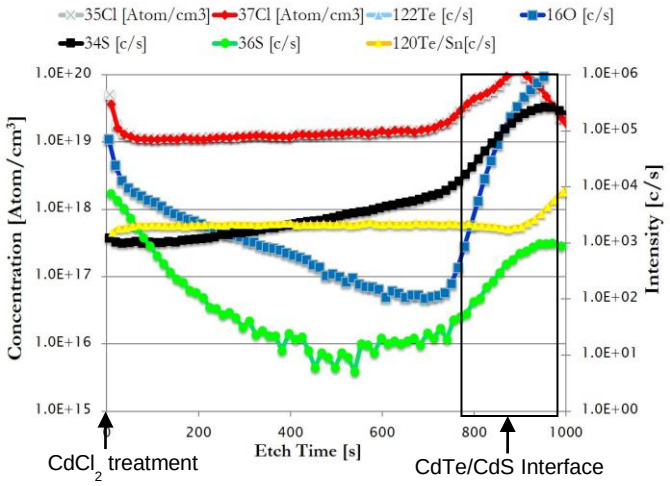

Fig. 8. Secondary Ion Mass Spectroscopy (SIMS) of standard CdTe/CdS film showing higher concentration of chlorine at CdTe/CdS interface.

VII. Conclusions

Lower substrate temperature for CdTe deposition has a detrimental effect on device performance that can be related to film microstructure. Films with higher substrate temperature with hotter passivation treatment gives improved V_{OC} and fill factor with comparable current and efficiency which can also be related to film microstructure. Longer passivation treatment forms chlorine rich regions resulting in lower device performance. Energy Dispersive X-ray Spectroscopy of TEM samples show chlorine build up in the voids between the grains at the grain boundaries. Chlorine diffuses through the grain boundaries to reach the CdTe/CdS interface as can be seen from SIMS depth profile of the films resulting in initiation of treatment at the CdTe and CdS interface.

Lower substrate temperature during CdTe deposition form high concentration of small CdTe grains at the interface of CdTe and CdS that has detrimental effect on cell performance. This also results in high density of longitudinal voids between the CdTe grains in the absorber layer and that extended through the thickness of the CdTe film. Higher substrate temperature during CdTe deposition forms larger grains that can be related to better device performance. Such films in addition to larger grains have grains that are well defined and do not show a lot of voids between CdTe grains. Relationships between these process parameters and uniformity of cells can be established using EL images. High substrate temperature cells with 10 ºC hotter $CdCl_2$ treatment temperature exhibits the best uniformity within the scope of this study.

VIII. Acknowledgements

The research is carried out at Colorado State University is supported by NSF I/UCRC for Next Generation Photovoltaics.

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