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The effect of temperature on resistive ZnO layers and the performance of thin film CdTe solar cells

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ABSTRACT

The use of a highly resistive transparent (HRT) layer has been shown to increase the efficiency of thin film CdTe heterostructure solar cells incorporating a thin CdS layer. In this study ZnO HRT layers were deposited at different substrate temperatures on soda lime glass and on fluorine-doped tin oxide-coated glass to enable structural, optical and electrical characterization. The performance of equivalent films was tested within CdS/CdTe solar cells. The ZnO thickness was limited to 150 nm, whilst the substrate temperature was varied from 20 °C to 400 °C during deposition. X-ray diffraction patterns and transmission electron microscopy of the cross-sectional microstructure of completed devices showed that the growth of the ZnO is improved when the films are deposited at higher temperatures. Film resistivity was lowest at 100 °C and highest at 400 °C, ranging from 10^{-2} Ω·cm to 0.33 Ω·cm. The high temperature deposited ZnO exhibits improved micro-structural growth and an improvement in device efficiency.

1. Introduction

The CdS layer in a CdS/CdTe solar cell absorbs a portion of the solar spectra from 500 nm to lower wavelengths due to its relatively low bandgap (2.45 eV) [1]. It is necessary to use a thin CdS layer to increase the number of photons reaching the CdTe absorber. However, this has the effect of degrading the open circuit voltage (V_{OC}) and fill factor (FF) of the solar cell. V_{OC} and FF degradation is believed to be caused by the creation of weak diodes associated with regions in which the CdS is too thin or with pinholes in the CdS layer [2]. Highly resistive transparent (HRT) layers, also referred to as buffer layers, are deposited between the transparent conducting oxide (TCO) and the CdS layer to limit the effect of these non-uniformities and maintain the diode quality, thereby increasing the efficiency of the solar cell [3–5]. The precise mechanisms by which the HRT layers function is not fully understood and further investigation is required [6]. In this study we explore the effect of temperature on the growth of the ZnO HRT layer and its effect on device performance. ZnO has been shown to be an effective buffer layer in other chalcogenide solar cells and is widely used in copper indium selenide and copper indium gallium selenide devices [7,8].

2. Experimental details

Thin ZnO films were deposited by Radio-Frequency (RF) magnetron sputtering. Soda lime glass (SLG) and NSG TEC™ C10 glass from Pilkington were used as superstrates. The glass superstrates were cleaned using a 10% isopropanol solution in deionized water in an ultrasonic bath at 60 °C for 60 min. Thin films were deposited using an Orion 8 HV magnetron sputtering system (AJA international, USA) equipped with an AJA 600 series RF power supply. The target diameter was 3″, and the ZnO target purity was 99.99%. The glass superstrates were rotated at 10 rpm during deposition to enhance the uniformity of the films. The sputtering process was carried out at a constant power density of 3.5 W·cm^{-2} and at a pressure of 133.3 Pa using pure Ar as the working gas. The temperature of the substrate was varied from 20 °C to 400 °C. The film thickness was fixed at 200 nm on SLG and 150 nm on TCO-coated superstrates. The electrical properties of ZnO films were investigated using Hall Effect measurements by the Van der Pauw method using an Ecopia HMS 3000. The optical properties were investigated by UV-VIS-NIR spectrophotometry with a Cary Varian 5000. The structural properties of films were analysed by X-ray diffraction (XRD) with a Brucker D2 phaser desktop X-ray diffractometer using a Cu-K-alpha X-ray gun. The XRD measurements were obtained using 15 rpm rotation, a 1 mm beam slit and 3 mm anti-scatter plate height. Devices were subsequently fabricated on ZnO-coated superstrates by the PV group of Colorado State University using the Advanced Research Deposition System (ARDS),

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an in-line system which has been described previously [9]. The process included the deposition of CdS and CdTe, a $CdCl_2$ activation treatment and a Cu/Ni based back contact. CdS was sublimated at a substrate temperature of 420 °C whilst CdTe was sublimated at a substrate temperature of 360 °C. The $CdCl_2$ treatment was carried out for 3 min at a substrate temperature of 388 °C. The thicknesses of CdS and CdTe films were maintained at ~120 nm and ~2.3 μm–2.5 μm respectively. Devices were characterized using current density-voltage (J-V) characteristics and cross-section images were obtained using transmission electron microscopy (TEM). Samples for TEM were prepared by focused ion beam milling using a dual beam FEI Nova 600 Nanolab. A standard in situ lift out method was used to prepare cross-sectional samples. An electron beam assisted platinum (e-Pt) over-layer was deposited onto the sample surface above the area to be analysed followed by an ion assisted layer to define the surface and homogenize the final thinning of the samples down to 100 nm. TEM analysis was carried out using a Tecnai F20 operating at 200 kV to investigate the detailed microstructure of the cell cross sections. Normal images were taken using the bright field (BF) detector and for elemental contrast images the high angle annular dark field (HAADF) detector was used.

3. Results

3.1. Tem cross-section images

Fig. 1 shows the cross-section images of devices with a focus at the TCO/ZnO interface. The grain size of the ZnO layer increases at higher temperatures and at 200 °C and 300 °C the grains expand to the full height of the layer, with an average width of between 50 nm and 100 nm. The films deposited at room temperature contain smaller grains. The elemental contrast image (Fig. 2) of the cross section reveals the creation of small voids in the ZnO film deposited at 20 °C. These small voids appear as black spots (highlighted with red circles) and are concentrated at the interface with the TCO. They are possibly caused by stress build-up in the ZnO near-interface region due to the large lattice mismatch with the fluorine-doped tin oxide (ZnO lattice constant c = 0.52066 nm [10], FTO lattice constant c = 0.3198 nm [11]). This phenomenon was not observed at higher ZnO deposition temperatures indicating that partial relaxation of the stress occurs.

3.2. X-ray diffraction (XRD)

XRD analysis of ZnO layers grown on the TCO coated superstrates was performed to evaluate the crystallographic growth at the different deposition temperatures. Fig. 3 shows XRD patterns of the 2Θ range between 30° and 70°. An XRD profile of a bare substrate was added for comparison to identify the peaks associated with ZnO. Four main XRD peaks were identified; (002), (101), (102), and (103), with the (002) and (101) peaks being the most pronounced. The intensity of all the peaks increase when the deposition temperature is raised, suggesting that higher temperatures assist the crystallographic phases to form. The peak position 2Θ and its full width at half maxima (FWHM) were extrapolated by Gaussian fitting (Table 1). The position of all peaks of the various phases is shifted to slightly lower 2Θ angles in comparison with the reference peaks (ICDD 00-003-0752). This can be attributed to the influence of the fluorine doped tin–oxide (FTO) coated

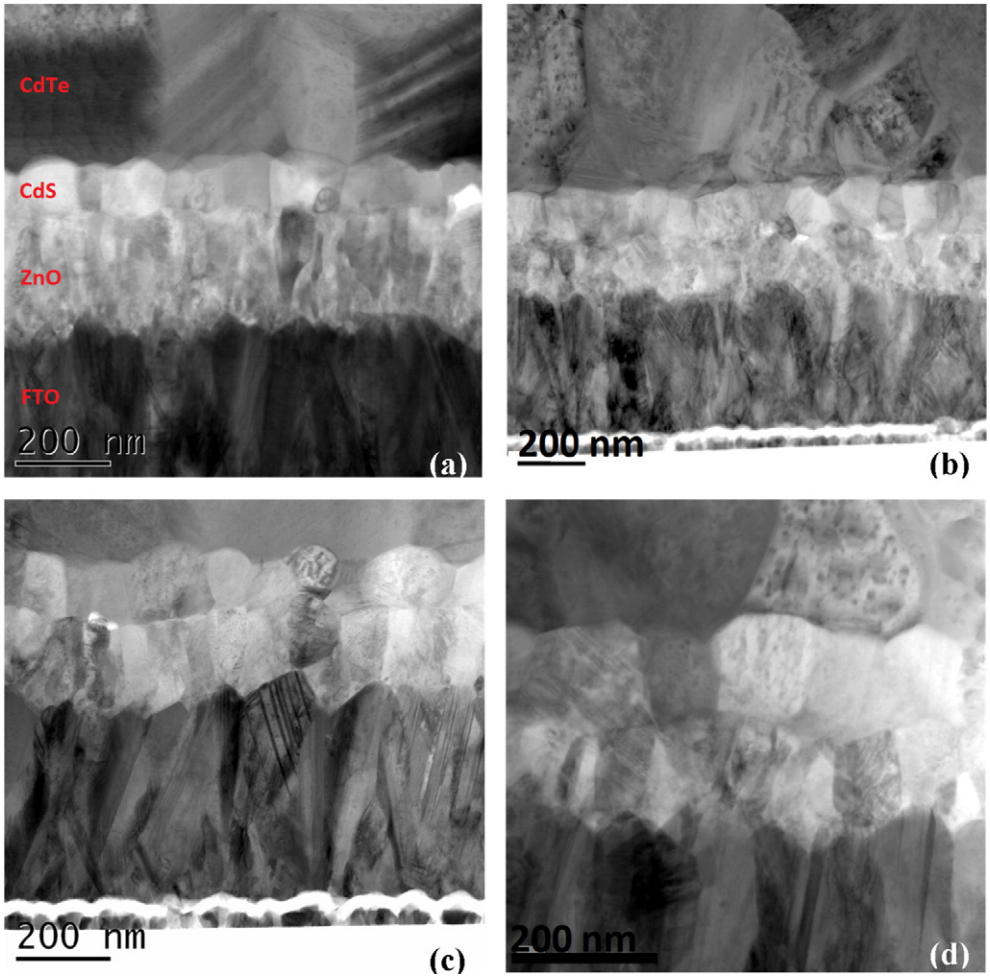

Fig. 1. TEM cross-sections of CdS/CdTe devices including ZnO deposited at 20 °C (1a), 100 °C (1b), 200 °C (1c), 300 °C (1d) using the BF detector.

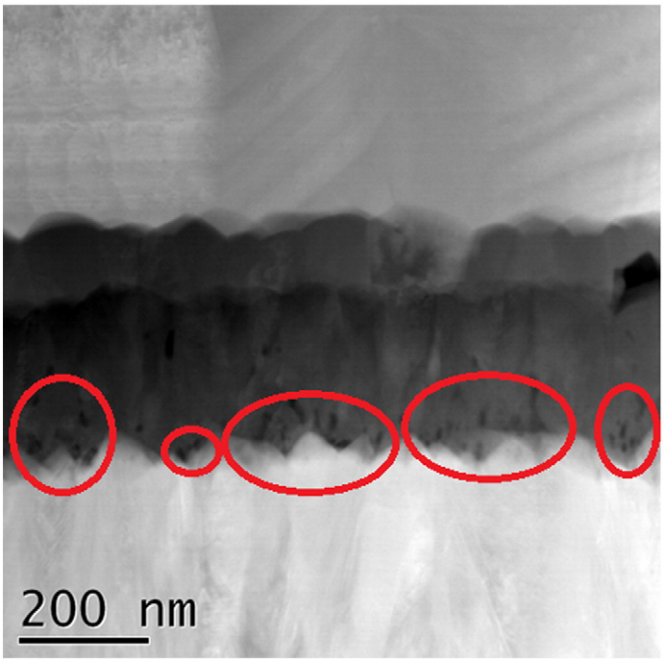

Fig. 2. TEM cross-section of sample containing ZnO deposited at 20 °C taken using the HAADF detector. Close to the TCO/ZnO interface black spots correspond to voids probably caused by interfacial stress due to the lattice mismatch factor between the two semiconductors.

superstrate on the ZnO growth. The FTO crystal structure mismatch with ZnO may force the film to grow in a different way than on bare glass. The peaks associated with the ZnO films deposited at room temperature have the 2Θ peaks close to ICDD whilst their position moves further from the reference peak at higher deposition temperatures. Fig. 2 shows the stress build-up at the TCO/ZnO interface for a ZnO deposited at 20 °C. Use of higher temperature assists the ZnO structure to adjust to the underlying semiconductor, shifting the XRD peaks to lower 2Θ angles. The FWHM of the peaks is reduced for films deposited at higher temperature associated with improved crystal growth.

3.3. Hall effect measurements

The HRT layer is believed to act as a resistive barrier to shunts through the device. As a result, the resistivity is expected to be a key parameter for ZnO used as an HRT layer. Fig. 4 shows that the deposition temperature of 100 °C produced the lowest resistivity of 1.87×10^{-2} Ω·cm, whilst a temperature of 300 °C yielded ZnO films with highest resistivity of 2×10^{-1} Ω·cm, an order of magnitude difference. The resistivity reported here is relatively low compared to those in other studies where the optimal resistivity was found to be from 10^3 Ω·cm and higher [5,7,8]. Oxygen is generally used to increase the resistivity of ZnO films; however, in our study oxygen was not added to the sputtering working gas pressure.

Table 1
Summary of XRD peak position and full width half maxima (FWHM).

Peak	Parameter	Substrate temperature (°C)				
		20	100	200	300	400
(002)	Position 2Θ (°) ICDD: 34.74°	34.44	34.39	34.42	34.40	34.42
	FWHM (°)	0.388	0.422	0.329	0.292	0.235
(101)	Position 2Θ (°) ICDD: 36.80°	36.32	36.28	36.23	36.23	36.22
	FWHM (°)	0.600	0.534	0.468	0.430	0.348
(102)	Position 2Θ (°) ICDD: 48.10°	47.57	47.54	47.48	47.46	47.47
	FWHM (°)	0.731	0.635	0.576	0.552	0.461
(103)	Position 2Θ (°) ICDD: 63.20	62.86	62.82	62.74	62.70	62.74
	FWHM (°)	0.670	0.555	0.564	0.505	0.448

3.4. UV–VIS–NIR spectrophotometry

The transparency of the ZnO films it is very important since it will affect the current output of the device. Fig. 5 shows the transmission curves of the superstrate glass coated with ZnO deposited at the different temperatures. The mean transmittance calculated over the wavelength range from 400 nm and 950 nm was ~80% for all samples with the exception of the room temperature sample which has marginally lower transmission.

3.5. J-V characteristics

A total of 9 devices were fabricated on each superstrate. Current density-voltage (J-V) characteristics of each device were obtained and the mean J-V parameters are summarized in Fig. 6. The mean short circuit current (J_{SC}) ranges from 21.2 mA/cm^2 to 21.8 mA/cm^2. The small difference in current density is expected given the similar transmittance of

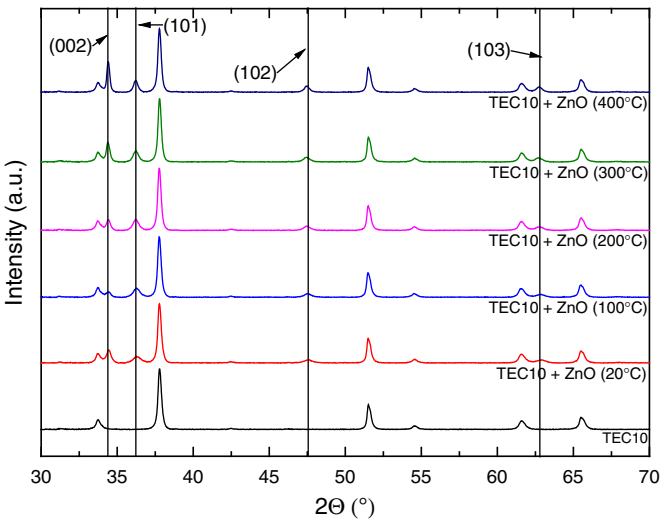

Fig. 3. XRD patterns of ZnO films deposited on soda-lime glass.

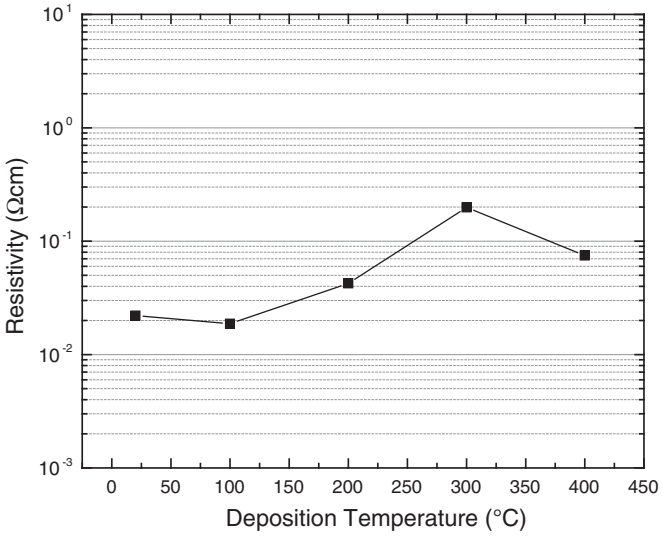

Fig. 4. The resistivity of ZnO films deposited at different substrate temperatures.

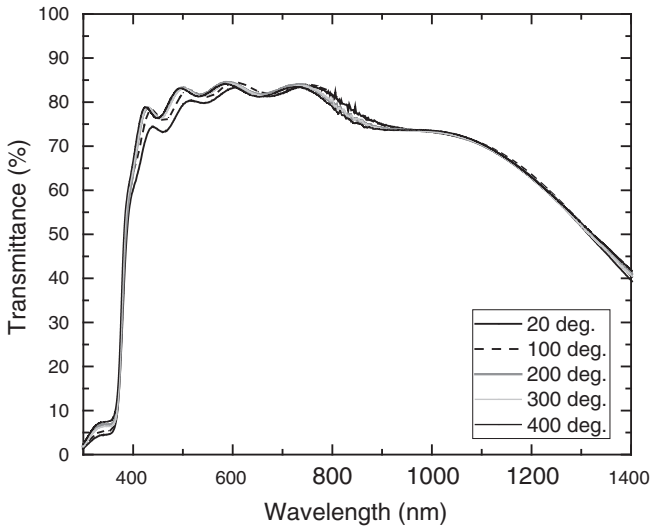

Fig. 5. Transmission spectra of superstrate glass coated with ZnO deposited at different substrate temperatures.

the films. The mean FF increases constantly with increased ZnO deposition temperature from 65% to 69%, with the exception of the 200 °C sample. This increase in FF follows the improvement in crystal structure and the increase in the resistivity. The FF may improve due to a combination of an improved TCO/ZnO interface and improved growth of the ZnO crystal structure and an increasing resistivity of the ZnO buffer layer. However, there is no clear trend between the film resistivity and any other device parameter. The V_{OC} steadily degrades as the ZnO deposition temperature increases, reducing by 23 mV from 798 mV to 775 mV. Overall, the mean device efficiency improves marginally from 11.2% to 11.5%. It is likely that a more pronounced trend on the effects of a ZnO HRT layer on a CdTe device will be observed when the CdS layer thickness is thinned below 100 nm. The relatively thick CdS layer used in this study (120 nm) partially screens the ZnO effect [6].

4. Conclusions

The impact of the deposition temperature on the growth of ZnO HRT layers and the effect on the performance of CdTe thin film solar cells has been investigated. TEM cross-section images and XRD analysis show enhanced grain growth of the ZnO films at deposition temperatures of 100 °C and above. TEM images reveal small voids in the ZnO layer located at the ZnO/FTO interface when the ZnO layer is deposited at temperatures below 200 °C. The XRD peak position shifts towards smaller 2Θ angles when films are deposited at higher temperatures, however there is no correlation between deposition temperature and the degree of peak shift. The occurrence of voids and the shifts in the XRD peaks are linked to the relaxation of the TCO/ZnO interface stress and the stress in the ZnO films. Devices were fabricated with ZnO HRT layers deposited at different deposition temperatures and their performance characterized using J-V measurements. The FF of the devices increases with increased ZnO deposition temperature. This is associated with improvements in the structural quality of the ZnO, the interface quality at the FTO/ZnO junction and the increased resistivity of the ZnO films. The V_{OC} was found to reduce with increasing ZnO deposition temperature. Further work is required to understand this effect. The device efficiency is higher when the ZnO HRT layer is deposited at higher temperatures. A further improvement should occur if the CdS layer thickness is reduced.

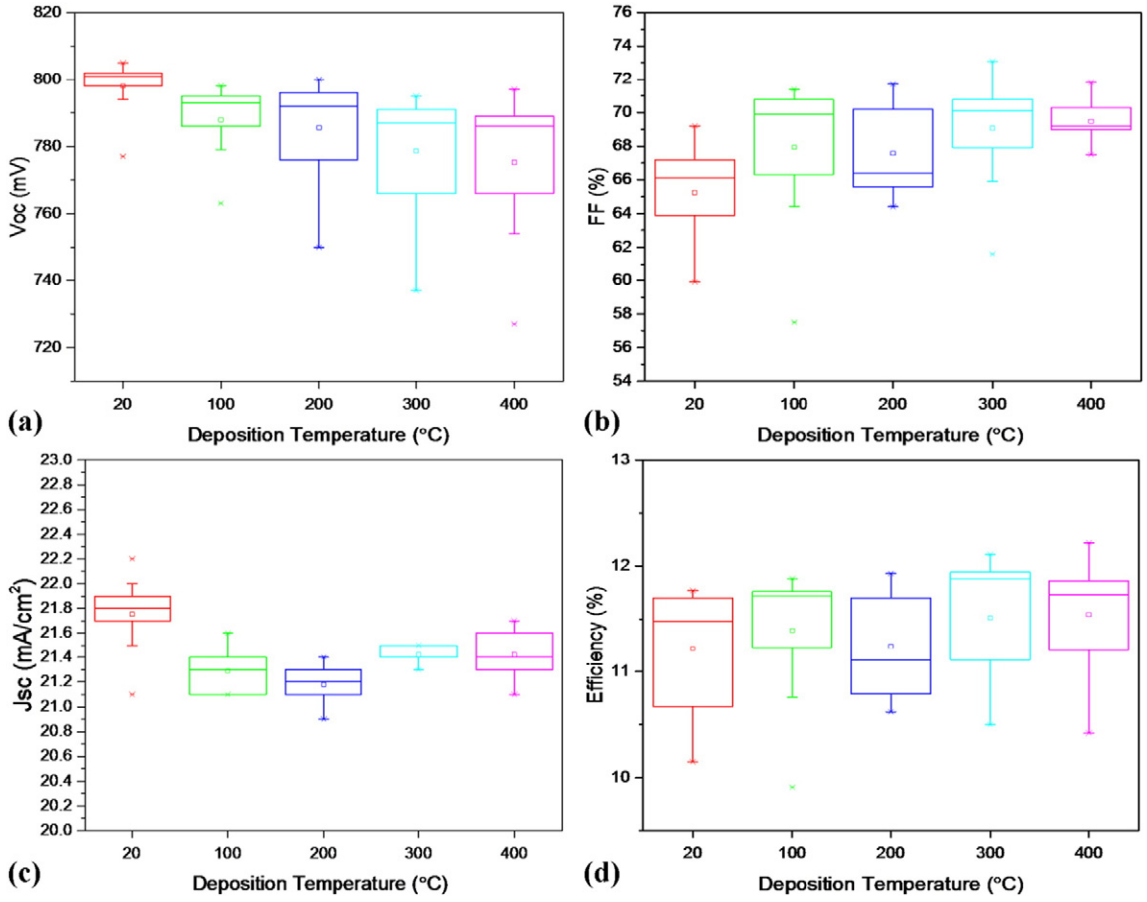

Fig. 6. J-V parameters of CdTe thin film solar cells as a function of ZnO deposition temperature: V_{OC} (6a), FF (6b), J_{SC} (6c), efficiency (6d). The plots show a statistical box chart.

Acknowledgments

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