Performance characterisation of photovoltaic devices:

Managing the effects of high capacitance and metastability

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Abstract

It is essential to make performance measurements of photovoltaics modules in order to quantify the power they will produce under operational conditions. Performance measurements are fundamental throughout the photovoltaic industry, from product development to quality control in manufacturing and installation in the field. Rapid and economic evaluation of photovoltaic performance requires measurements using pulsed illumination solar simulators. However some devices have characteristics which can cause difficulties making these measurements. The aim of this thesis is to overcome these measurement problems focusing particularly on two of the most prevalent and pressing of these problematic characteristics: high capacitance and metastability.

A new method for measuring high capacitance modules in a pulsed simulator, based on tailor made voltage ramps, was developed. The voltage ramp is tailor made such that the measurement time is minimised while maintaining high accuracy (0.5 %), allowing the measurement of high capacitance modules in a single 10ms illumination pulse. The necessary inputs for this method are the capacitance and dark current as a function of voltage for each module. In order to make these measurements, at the high forward bias voltages required, a new system was developed. The tailored voltage ramp can be created individually for each module, since the process is rapid an automatic. This makes the method applicable to a production line or to test house measurements. In addition to their use as inputs for the voltage ramp design, the capacitance and dark current also contain other valuable information, including effective minority carrier lifetime.

In several thin film technologies, such as CIGS, the efficiency is not a fixed value, rather the module is metastable and the efficiency changes depending on the previous exposure /preconditioning of the device. Preconditioning is normally applied to these devices before measurement in order to put them in a specific state that is repeatable and representative of outdoor operation. Improved preconditioning practices are vital for performance measurements in CIGS modules. Therefore the preconditioning behaviour of a variety of CIGS modules from different manufacturers was investigated. The effect of preconditioning varied for different modules, commonly the fill factor improved substantially, but often changes in open circuit voltage were also seen and in some cases also substantial changes in short circuit current. The rates of

preconditioning and relaxation were found to follow stretched exponential behaviour, such that the changes occur linearly on a logarithmic timescale over several orders of magnitude in time. The total time for performance stabilisation was found to vary significantly between different types of module. Because of this stretched exponential behaviour, even though the module took days to fully relax to the dark state, there was significant relaxation within the tens of minutes that it would normally take a module to cool down after light soaking before it could be measured. The major implication of observed kinetics is that in order to achieve repeatable measurement the timing in each element of a preconditioning routine should be controlled such that the fractional error in the duration of each step is small. During the investigation an unexpectedly short timescale preconditioning effect was observed, which occurs on a millisecond timescale and relaxes in seconds. It was shown that the measurement artefacts introduced using this method can be eliminated by using electrical forward bias until immediately before the measurement.

Another measurement system was developed to track the dark current and C-V characteristic of the modules during electrical bias preconditioning and subsequent relaxation. These measurements demonstrate that more than one process involved during preconditioning in CIGS. Changes occur both in the doping in the bulk of the absorber and also in charge accumulation occurring near to the absorber / buffer interface. The theoretical models for preconditioning in CIGS were reviewed and compared to the experimental results. A rate model was developed based on the theory of the metastable V_{Se}-V_{Cu} defect. This model was shown to correspond well to the rates of preconditioning and relaxation in CIGS. The non-exponential behaviour was shown to be compatible with a distribution of activation energies for the transition between different defect states. The difference in the time taken for modules to stabilise is explained by differences in doping density and the density of V_{Se}-V_{Cu} defects.

The work presented facilitates more accurate, economical performance measurements for high capacitance devices and CIGS devices, thereby contributing to the large scale implementation of photovoltaics as power source.

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Many people gave me huge amounts of help during my time completing this thesis and without that help it would not have been possible.

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Without question I would not have made it this far without the support of my parents who taught me to achieve the most that I can.

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Contents

1 Introduction

The need to produce usable energy in an environmentally sustainable manner is one of the biggest challenges of our time. Photovoltaic energy is a beautifully elegant solution to this problem. It has no moving parts, and a panel can simply be left outside and it will directly transform into electricity the solar radiation that falls on it for free every day. The lure of this abundant renewable energy source has fuelled impressive technological improvements and cost reduction over the past decades. PV system price has declined by 75% in less than 10 years [1] and uptake of PV technology has been accelerating rapidly as can be seen from the evolution of installed photovoltaic capacity in Figure 1-1. Currently there is approximately 178GW of installed photovoltaic capacity worldwide which produces roughly 1% of global electricity production. It is predicted that 540GW of installed capacity could be reached by 2019 [1,2]. It is an exciting time for solar photovoltaics as the technology rapidly approaches the inflection point where energy produced in this way becomes cheaper than conventional energy even without subsidies. This point will begin a self-sustaining explosion in the use of photovoltaics and herald a new age of renewable energy where we can finally leave the fossils in the past from which they came.

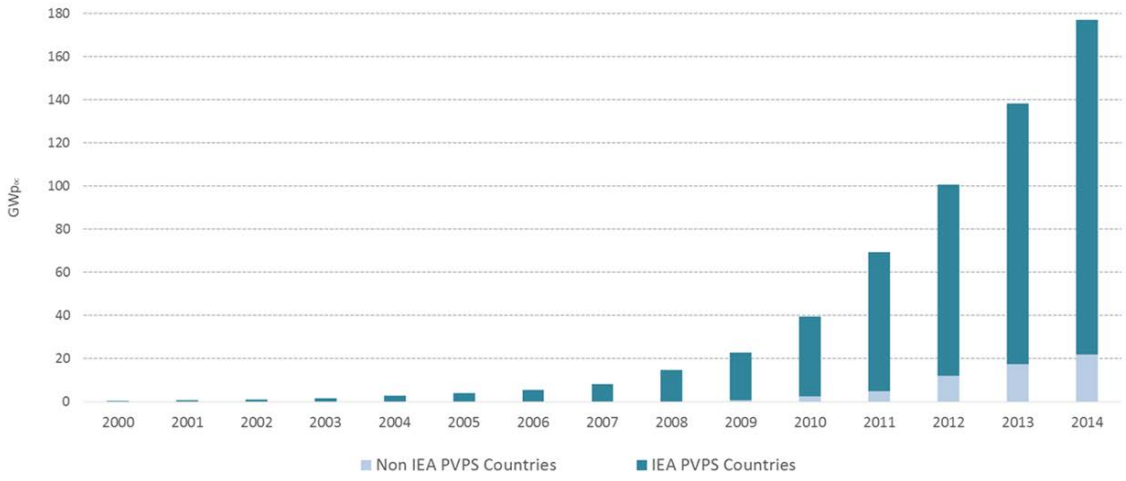


Figure 1-1: The evolution of installed photovoltaic capacity. Source IEA snapshot of global PV markets 2014 [2]**. The strong exponential like growth can be taken as a reason for great optimism.**

New generations of photovoltaic technology continue to provide the improvements necessary for the growth of the industry, however they often also provide fresh challenges. One of the challenges that they present is how to measure their performance under different conditions in order to predict the energy that they will produce when

mounted in any particular location. For a variety of reasons this is often not a trivial task and this challenge is the overarching theme of this thesis.

Performance measurement of PV devices is an essential component of the photovoltaics industry. During manufacturing the performance of each module is measured as a quality control measure. Modules are then often sorted according to their power output with the higher performing modules achieving a higher price. Sorting of the modules also helps to improve the overall efficiency of an installed system, since low power modules in a series string will bring down the output of all the other modules in that string. Installers rely on performance measurements to compare different potential products and to model the energy yield, and therefore financial payback of solar installations. These financial models are extremely important for large installations in order to attract investment and get funding. Overall when there is a problem with performance measurements for a particular photovoltaic technology, it is a big problem.

There are a number of different technology options available for photovoltaic modules, and some of these present unique measurement challenges. Photovoltaic technologies are often categorised into crystalline silicon based vs thin film technologies, but both of these categories have an increasing number of subdivisions. Crystalline silicon is the most established technology and currently represents around 90% of the photovoltaic market [3]. Thin film technologies however are an exciting prospect for the future because they have very strong potential for cost reduction, efficiency improvement and also novel applications such as flexible modules. Within the heading thin film technologies are many different material systems, but only three main options have reached significant commercial production at present. These technologies are in order of current market size: CdTe, Cu(In,Ga)Se_2 (CIGS) and amorphous silicon (a-Si). While a-Si was the first thin film technology to gain a significant market share it has struggled more recently and it appears unlikely that it will be able to achieve the efficiency required to compete with other technologies. CdTe and CIGS however have both demonstrated single cell efficiencies of 22% or over, which demonstrates that modules of these technologies should be able to reach at least similar efficiencies to c-Si based technologies if not eventually surpassing them.

In order to characterise the performance of a photovoltaic device it is necessary to measure its current output as a function of the applied voltage while the cell is under

illumination. This is known as the I-V curve and will also depend on the intensity and spectrum of the light illuminating the device and the temperature of the device. In order to aid comparison of devices the standard IEC 61853-1 [4] was created and is used throughout the PV community. In this standard the device temperature is 25°C and the irradiance on the device is 1000Wm^{-2} with a defined spectrum known as AM1.5G which is based on the spectrum of solar irradiation received at sea-level when the sun is at an angle such that the light travels through 1.5 times more air mass than it would if the sun were directly overhead.

The intensity of 1000Wm^{-2} specified in the standard is close to the maximum intensity ever received from the sun. In general is it difficult and expensive to continuously and uniformly illuminate a large area with such a high intensity, especially with a good spectral match to AM1.5. Additionally, a PV module illuminated at such high intensity will rapidly heat up to well over the 25°C specified in the standard. However, these conditions are relatively easy to achieve using a pulsed solar simulator, where the I-V curve is measured during a short flash often of around 10ms duration. Pulsed simulators are by far the most common method for indoor performance measurements of photovoltaic modules.

One of the problems for performance measurement that is often encountered is that of highly capacitive modules. This problem limits the rate at which the I-V curve can be measured without distortion, and presents a problem for using short pulse simulators to characterise devices. Large capacitance is a problem particularly prevalent in high efficiency modules, for example Panasonic HIT modules, Sunpower back-contact modules and Yingli PANDA bulk n-type modules. It is therefore a problem that is quite likely to persist and become even more troublesome in the future. There are a number of solutions to this problem, including longer pulse simulators, and measuring the I-V curve in sections using several illumination pulses. Other methods try to reduce the measurement time using non-linear voltage ramps. In this thesis the problem of quickly measuring high capacitance modules is addressed and a new method is presented that uses direct measurement of the module capacitance to calculate the fastest rate the voltage can be swept for a given desired accuracy of the measurement.

For many of the thin film PV technologies one of the biggest characterisation problems is that their measured efficiency is not a constant value but varies during the course of

normal operation depending of the exposure history of the modules. In a-Si this problem manifests itself as a seasonal variation in efficiency due to the Staebler-Wronski effect [5]. This type of module gradually reduces in efficiency with light exposure, however the effect is reversed by heating. The Staebler-Wronski effect has been well studied and is now relatively well understood at a material level [6]. A related phenomenon In CIGS, normally called the "light soaking effect" or "preconditioning", has also been extensively studied but is contrastingly less well understood. The effects of light exposure are more favourable in CIGS than in amorphous silicon and it is usually observed that the efficiency improves during light exposure. The performance differences between measurements of CIGS modules made immediately after dark storage and those made after light soaking vary significantly depending on the particular module but can be quite large, improvements in efficiency of over 10% are not uncommon. The preconditioning state of the module therefore has a high impact of the measured efficiency.

A common procedure aiming for consistent measurement is to light soak the modules, wait for them to cool down and then measure them in a standard pulsed simulator. The justification for this procedure is the modules are often seen to increase in efficiency much more quickly than they relax, so that in normal operation the modules will operate for the majority of the time at the increased efficiency observed after light soaking. However the procedure is not well defined, with many manufacturers suggesting different details for the preconditioning routines and measured values often depending strongly on those precise details in a seemingly inexplicable manner. One of the main reasons for the confusion is a basic lack of understanding of the causes of the effect. Despite the fact that metastabilities in CIGS have been extensively studied, there is no universally accepted model for the cause of preconditioning in CIGS. Experimental observations of metastabilities in CIGS produce a variety of different behaviours depending on the fabrication of the device, which is undoubtedly part of the reason for the lack of agreement in the literature. Another reason is because of a lack of measurement possibilities that directly test one theory over another, so that the same experimental results can be interpreted in a variety of different ways. Nevertheless, there are some theories that have gained a significant amount of backing.

Developing a repeatable measurement routine for CIGS modules forms a major theme of this thesis. The effect of preconditioning applied either by light soaking or voltage bias is measured for a variety of CIGS devices and the rates at which the preconditioning occurs and subsequently relaxes are also measured. During the observations an unexpected, additional preconditioning effect was discovered which occurs and relaxes on a much faster timescale than usual. The effect was investigated further and appears be of a different origin from the previously known preconditioning effect, however the effects are not independent.

The theoretical models for the causes of preconditioning in CIGS are numerous and related in a complicated manner to many other controversial aspects of device physics in CIGS. In the final chapter these theories are explored in detail, and discussed in relation to the problem measurement problem. In particular a rate model for the preconditioning is created and observed to represent the observed data. The further implications of this model for device preconditioning and measurement are explored.

2 Principles of Photovoltaics

This chapter introduces the basic principles of photovoltaics. These principles are the fundamental understandings that lay the foundation for the work in this thesis. The operation of photovoltaics will be described followed by details of the specific technologies relevant to this thesis. Finally performance measurements for photovoltaics will be discussed.

2.1 Operation

2.1.1 Basic operation principle

The basic principle of any photovoltaic device is to take energy from incident light falling on the device and turn it directly into electrical energy. Photons of electromagnetic energy are absorbed by electrons in a material increasing the potential energy of those electrons and creating a potential difference / voltage between the excited electron and the empty states they previously occupied. The electrons are then physically separated from the empty states. When an external circuit is provided for the electron to relax back to their initial state, the potential energy of the electrons creates a voltage across the external circuit which causes current to flow. The voltage and current can then be used in the external circuit to do useful work, for example making a cup of tea.

The most successful photovoltaic devices to date are based on PN junctions of inorganic semiconductors. In semiconductors there are two continuous bands of allowable energy levels for electrons separated by a forbidden energy gap known as the band gap. The energy states of the lower energy (valence) band are mostly full of electrons whereas the higher energy (conduction) band is mostly empty. The empty energy states in the valence band take on the properties of new particles, known as holes, which can be considered instead of trying to deal with the enormous number of electrons which nearly fill the valence band. The holes have the opposite charge to electrons. When photons of sufficient energy are incident on the semiconductor they can be absorbed and excite electrons from the valence band to the conduction band, leaving a hole in the valence band. The hole and the electron are both free to move in the semiconductor and are physically separated in space by the effect of the PN junction.

A PN junction is created by connecting an electron rich (n type) semiconductor directly to a hole (rich p) type semiconductor. When this happens the electrons from the n type

region diffuse into the p type region and holes from the p type region diffuse into the n type region. When the electrons and holes diffuse they leave behind a net charge, which creates an electric field opposing further diffusion of holes so that equilibrium is reached between the diffusion of the carriers and the electric field as shown in Figure 2-1. When a photon is absorbed it creates an electron hole pair at the point of absorption, disrupting the equilibrium. The minority carrier from the pair is pushed by the electric field to the other side of the junction separating the electronic charges. When an external circuit is connected to opposite sides of the junction the excess carriers flow around the external circuit.

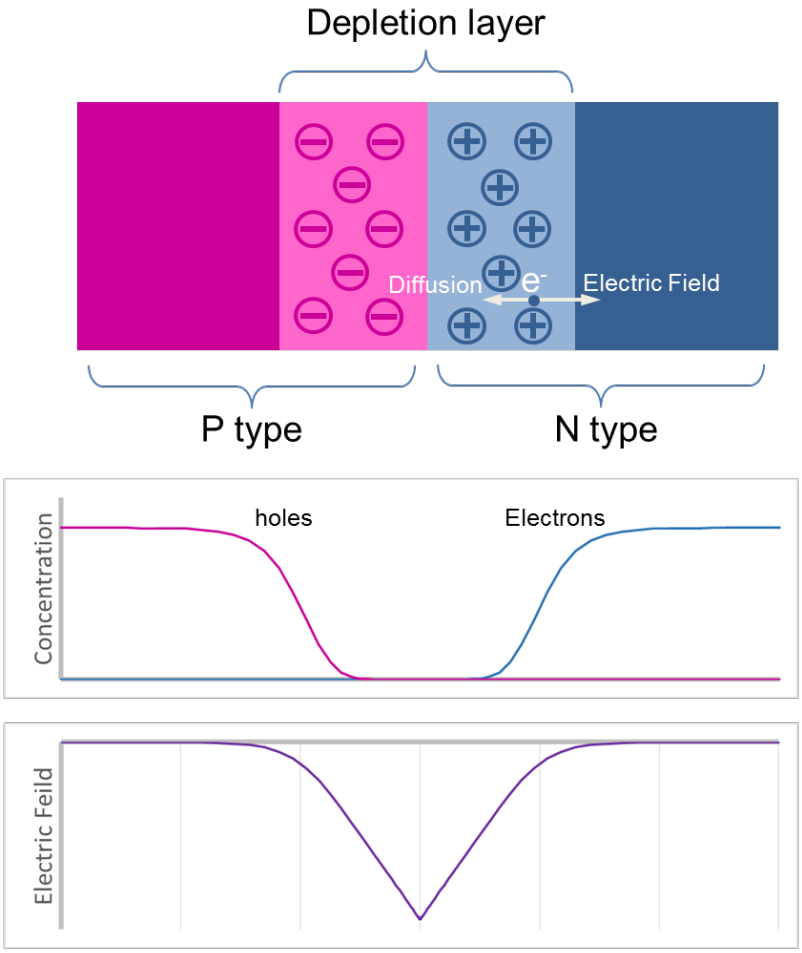


Figure 2-1: Schematic of the PN junction.

Because of the band gap in semiconductors, incoming photons can only excite carriers from one band to another if they have energy greater than the band gap. After a carrier is excited by an incoming photon it rapidly loses energy until it reaches an energy close to the band edge and comes into a quasi-thermal equilibrium with the other excited

carriers. This process is called thermalisation and it occurs very rapidly, on the order of picoseconds [7]. Under these conditions the carriers are not in equilibrium, but there can be considered to be a quasi-equilibrium separately within each band because the processes of generation and recombination between the bands are much slower than the thermalisation within the bands. Any energy of an absorbed photon greater than the bandgap of the semiconductor is lost to thermalisation and the energy of photons with lower energy than the band gap is lost because they never create an electron hole pair. The other unavoidable loss mechanism is radiative recombination which cannot be avoided because it is the reverse of the absorption process. For a continuous spectrum of incident irradiance, increasing the bandgap increases the voltage of the cell but reduce its current because fewer photons have sufficient energy to excite electrons. This trade off means that single bandgap photovoltaic cells operating under the sun have a maximum efficiency which depends on the bandgap of the device. This maximum was first calculated by Shockley and Queisser and is hence known as the Shockley-Queisser limit [8]. Figure 2-2 show the graph of efficiency Vs bandgap for the standard solar spectrum. There are two peaks in efficiency of roughly 33.5% at 1.15eV and 1.4eV. In real devices there are other losses which prevent the Shockley-Queisser limit being reached in practice. These non-ideal losses can be grouped into optical losses which are due to incomplete absorption of the incoming radiation, and electrical losses due to recombination of photo-generated electrons and holes, or voltage drops due to series resistance.

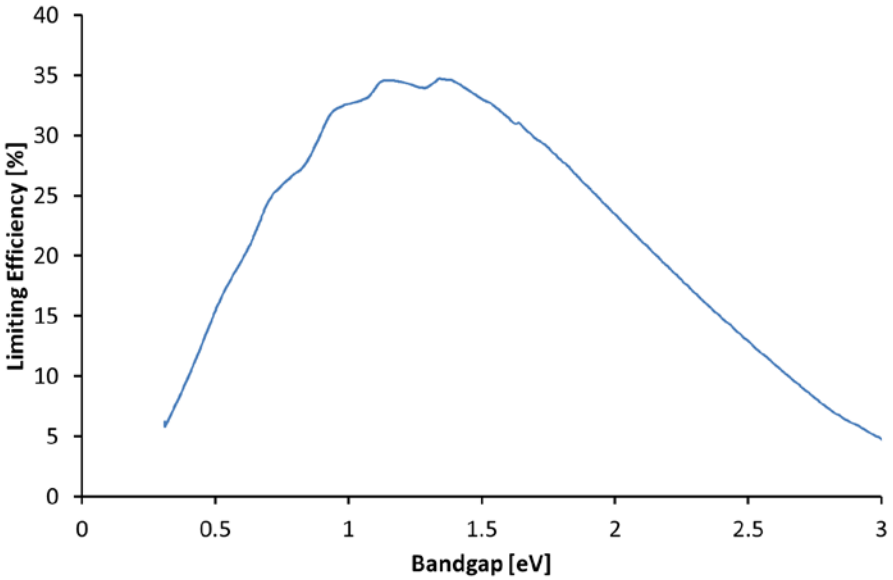


Figure 2-2: Cell efficiency Vs bandgap.

2.1.2 Solar Resource

The sun irradiates the earth with 175,000 TW of light. It drives the weather systems and provides the energy which sustains the bountiful life on our planet. Through photovoltaics it is possible to harness this power to provide for our energy needs as well.

The intensity of the sunlight arriving at the earth is highly variable. There is a highly predictable geometrical component to this variability caused by the orbit and rotation of the earth. These variations cause the cycles of day and night, summer and winter. There is also a much less predictable component to the variation caused by weather. The maximum intensity of sunlight at ground level on a clear sky day is roughly equal to 1000Wm^{-2}. This conveniently round number is referred to as 1 sun illumination and is the intensity used for standard performance test measurements of photovoltaic devices. Statically mounted photovoltaics only receive this intensity of illumination for a very small percentage of the time and are usually operating at lower intensities. Figure 2-3 shows the distribution of annual solar irradiation at different intensities in three different locations. It can be seen that location has a strong impact, which is a combination of the effect of different latitude and different climatic conditions.

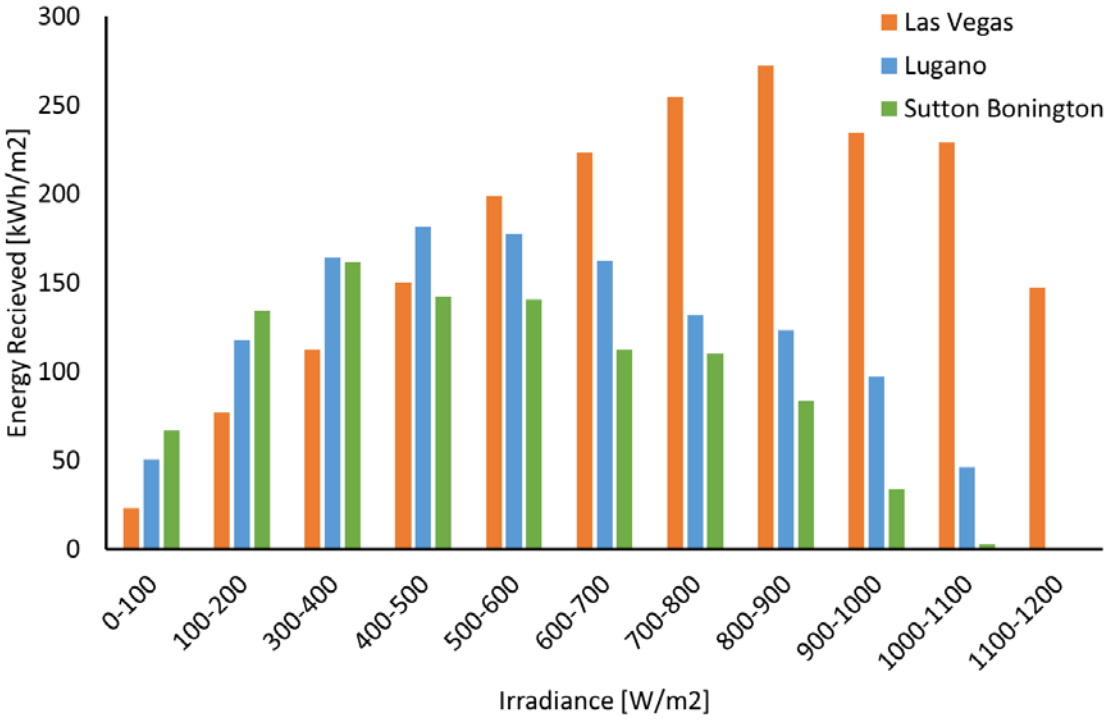


Figure 2-3: The distribution for the fraction of power received on a horizontal plane for different irradiances in: Sutton Bonington, UK; Las Vegas; USA; and Lugano, Switzerland. Data is taken from Meteonorm.

The surface of the sun is a plasma consisting of mainly of hydrogen and helium with a temperature of approximately 6000K. The spectrum of the irradiance emitted by the sun is matched closely to the theoretical black body radiation for 6000K. This is the spectrum of irradiation on satellites, but for terrestrial photovoltaics the spectrum is considerably altered by absorption and scattering in the atmosphere. The inclination of the sun has a large impact on the irradiation arriving at the ground level because it changes the path length of the light through the atmosphere so more light is absorbed. Because of this and other atmospheric factors the spectrum of solar irradiation is not constant and varies throughout the day. The path length of the light through the atmosphere is usually described in terms of the air mass number (AM), which is the mass of air travelled through relative to that when the sun is directly overhead. Examples of typical clear sky spectra at different air mass are shown in Figure 2-4. For performance measurements, an AM1.5 spectrum is used, this corresponds to the spectrum for a panel with a 37° tilt and a sun elevation of 41.8° (IEC 60904-3). It was constructed to be roughly representative of the average spectrum over the whole of the US over the course of a year.

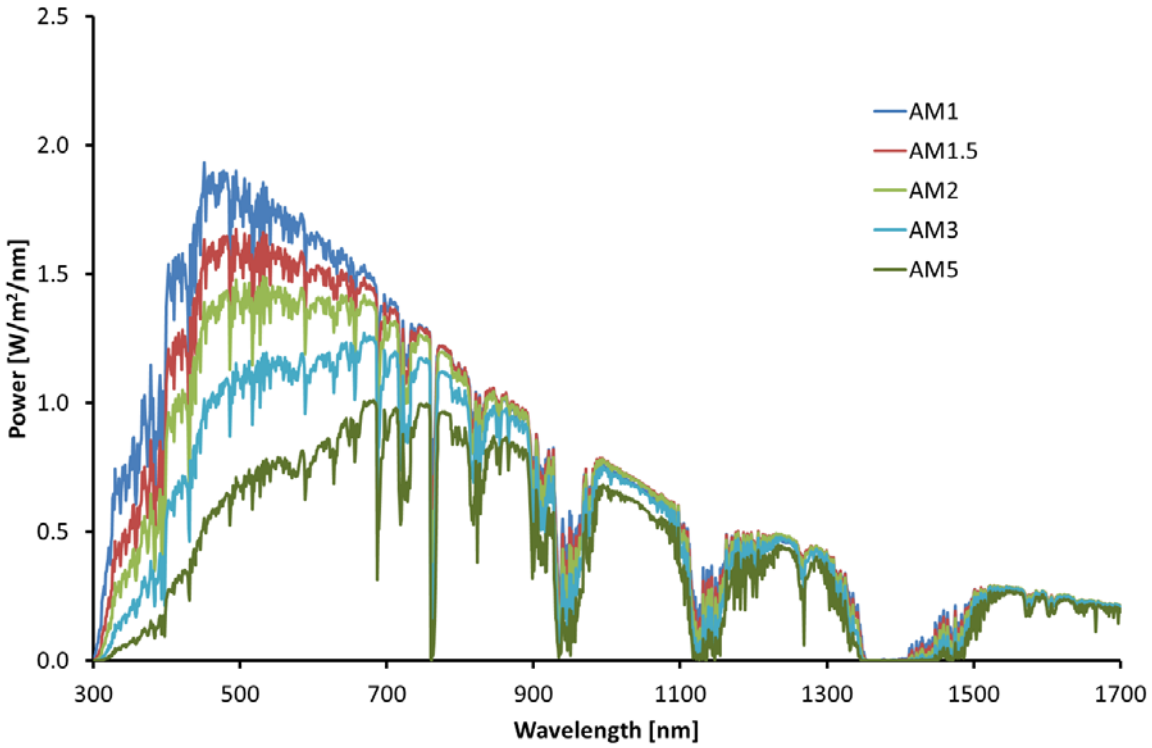


Figure 2-4: The direct incidence solar spectrum at different air mass values, calculated using SMARTS [9]

2.1.3 Band diagrams

Band diagrams are the easiest way to visualise what is happening in solar cells. The band diagram displays the energy level of the conduction and valence band edges and the Fermi levels as a function of the distance through the device. The Fermi level (E_f) represents the average electrochemical potential energy of the charge carriers (electrons and holes). Variation in the Fermi level would represent a driving force for carriers through the device so in equilibrium the Fermi level is flat. As previously discussed, outside of equilibrium the electrons and holes can be considered to form two separate quasi equilibrium populations. There are then separate quasi Fermi levels for the electrons (E_{fn}) and holes (E_{fp}). The closer the Fermi level is to the relevant band the higher the number of carriers is, as described by the Fermi-Dirac distribution. Electrons move in the direction of decreasing E_{fn} whereas holes move in the direction of increasing E_{Fp}. The band diagrams in this section were all created using the photovoltaic device simulation package SCAPS [10].

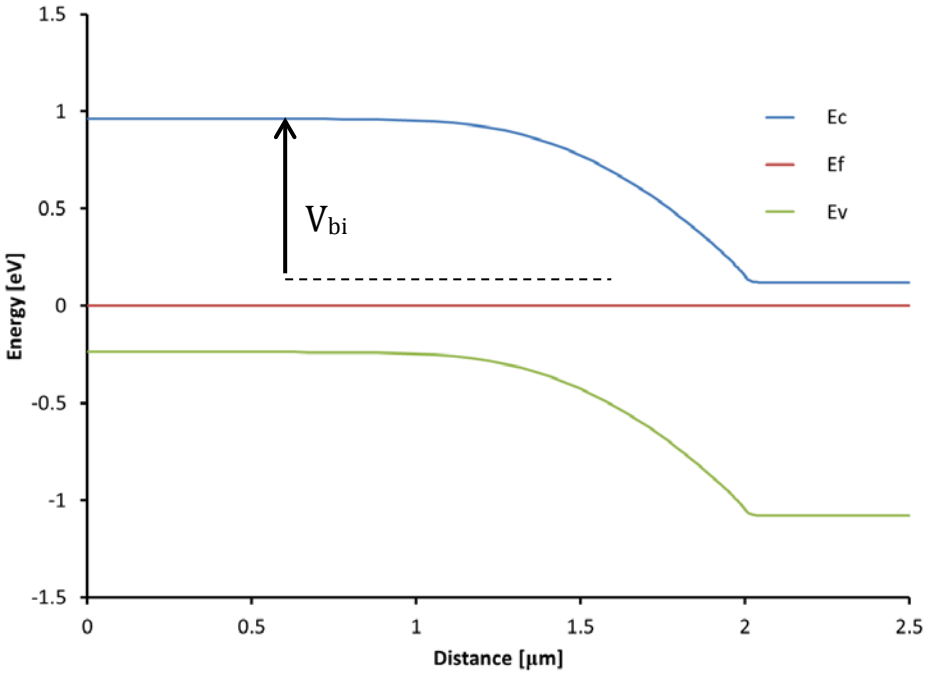


Figure 2-5: Band diagram of a PN junction in equilibrium.

In the dark at zero bias a photovoltaic cell is in equilibrium. Figure 2-5 shows the band diagram of a PN junction in these conditions. The carriers are in equilibrium between the bands as well as within the bands so there is only one Fermi level and it is flat. The device in the diagram is more heavily doped on the n type side. Since the charge on both sides of the junction must balance, the depleted area on the lightly doped side is much

wider and the result is that the majority of the band bending occurs on the p type side of the junction. The built in voltage is an important quantity which is also illustrated.

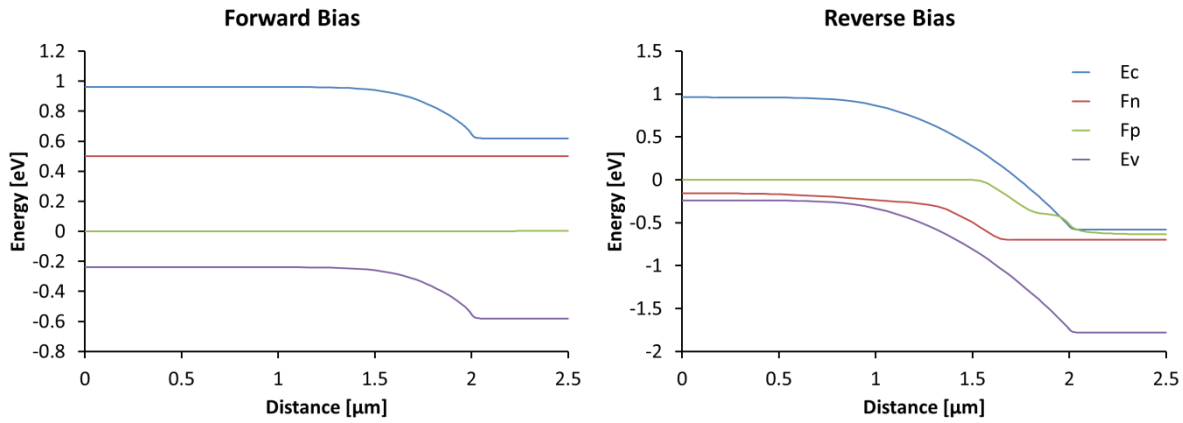


Figure 2-6 band diagram of PN junction in the dark under forward and reverse bias

When an external bias is applied to the cell, charge flows and there is no longer equilibrium in the device, so the Fermi levels split. The bias for a device is dictated by the difference in the majority carrier Fermi level at the two contacts. That is, the difference between the E_{Fn} on the n side contact and E_{Fp} on the p side contact. The Fermi level at the contacts follows the majority carrier Fermi level in the semiconductor at that contact. Forward bias reduces the band bending in the device until the bias is equal to the built in voltage, when there is no band banding as shown in Figure 2-6.

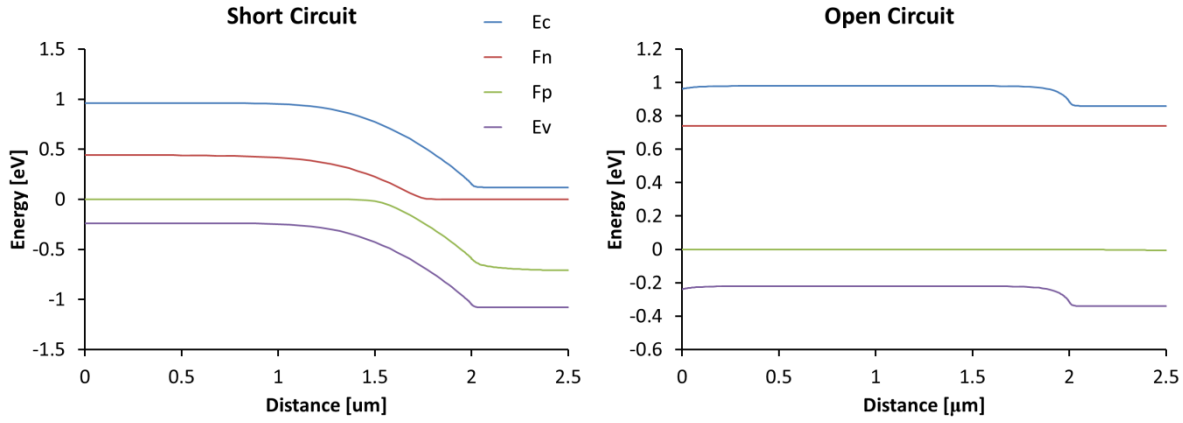


Figure 2-7 band diagram of illuminated PN junction at short circuit and open circuit conditions

Illumination causes generation of carriers and massively increases the concentration of minority carriers. This moves the minority carrier Fermi levels significantly towards the relevant bands. Figure 2-7 shows the illuminated PN junction under different bias conditions. At short circuit the Fermi level of the contacts is the same on both sides of the device. In the junction region there is a significant gradient of the quasi Fermi levels which shows there is a strong force on the carriers which generates the short circuit

current. The increase in minority carriers has reduced the diffusion gradient without reducing the electric field so the carriers now move in the direction dictated by the built in field.

At open circuit there is no current flow. The Fermi level difference between the contacts increases and the band bending flattens out until the quasi Fermi levels are virtually flat. They may in fact slope gradually in opposite directions such that the currents from each carrier type cancel out. This is due to the generation and recombination profiles not matching. For example most of the carriers are generated near the front of the device where the light is incident, but there may be higher recombination at the back contact which causes movement of both carrier types towards the back.

In between the extremes of the open circuit and short circuit conditions there is a voltage difference across and a current flow around the external circuit. The amount of power dissipated by the external circuit depends on the voltage and reaches the maximum power point (P_{mpp}) at the voltage V_{mpp} and current I_{mpp}.

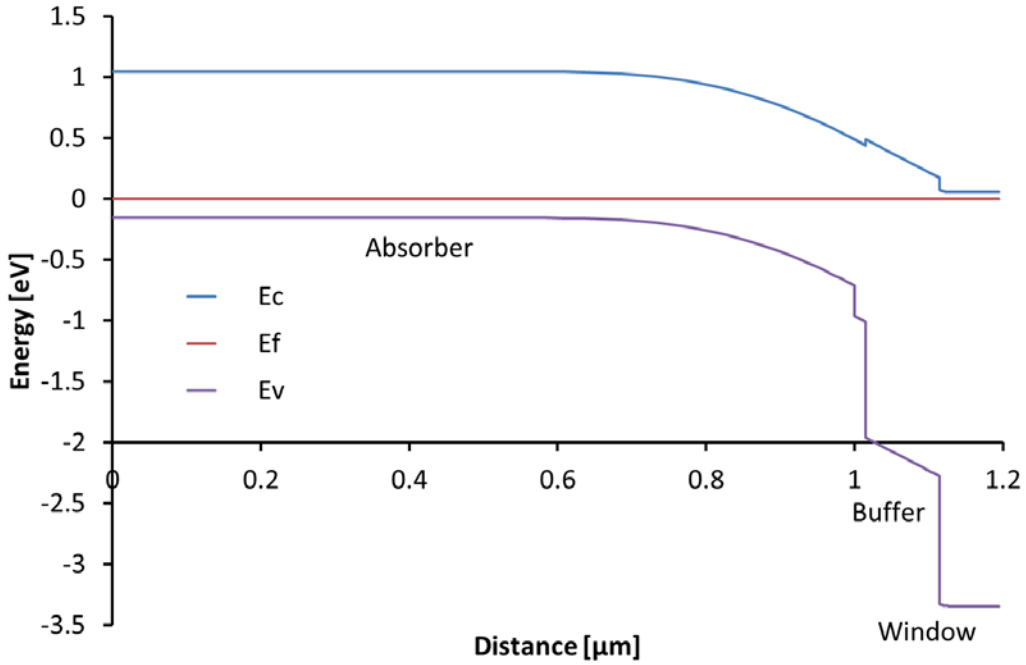


Figure 2-8: Band diagram of an absorber-buffer-window hetero-junction solar cell

Up to now the band diagrams displayed have been homo-junction devices, meaning the semiconductor on both sides of the junction is the same material with different doping. This device structure is typical of Si and GaAs solar cells. Heterojunctions can also be formed between different semiconductors. A common architecture for thin film devices is the absorber-buffer-window structure shown in Figure 2-8. In particular this is the

structure of CIGS devices, which feature prominently in this thesis. In a heterojunction device the band gap of the different semiconductors is not the same so there is a discontinuity known as a band offset at each of the interfaces.

Light enters the cell through the window layer which is a transparent conductor. Light is primarily absorbed in the absorber layer where the majority of the photocurrent generation occurs. The buffer layer improves device efficiency through a number of mechanisms including, improving band alignment, reducing surface recombination and refractive index matching.

2.1.4 Transport equations

In order to quantitatively understand photovoltaic cells we need equations for the movement of charge carriers within the cell, these are called the transport equations.

As was mentioned previously, the carriers within each band can be considered to be in a thermal equilibrium within the band. This means that the probability of carriers occupying an energy level of energy E follows the Fermi-Dirac distribution

$$f(E, E_f, T) = \frac{1}{1 + \exp\big((E - E_f)/kT\big)} \quad \textbf{2.1}$$

Where E_f is the fermi level which represents the average electrochemical energy of the carriers within the band. In general there are two Fermi levels, one for electrons in the conduction band (E_{fn}) and one for holes in the valence band (E_{fp}). In the dark and at zero bias there is equilibrium between the bands as well as within the bands and the Fermi levels are the same. The number of carriers is related to the Fermi level by the equations

$$\begin{aligned} n(E_{Fn}, T) &= \int_{E_C}^{\infty} g(E) f(E, E_{Fn}, T) dE \\ p(E_{Fp}, T) &= \int_{-\infty}^{E_V} g(E) f\big(E, E_{Fp}, T\big) dE \end{aligned} \quad \textbf{2.2}$$

Where g(E) is the density of states, and E_c, E_v are the conduction and valence band edge energies respectively. When the Fermi level is further than kT from the band edge the Fermi Dirac distribution can be approximated very well by the Boltzmann distribution

$$f(E, E_f, T) = \exp\big((E_f - E)/kT\big) \quad \textbf{2.3}$$

And since only the states very close to the band edge are occupied the density of states at the conduction band can usually be approximated by an effective density of states at the band edge energies. This allows the integrals in 2.2 to be easily solved and gives the carrier concentrations as a function of the Fermi levels and the temperature

$$\begin{aligned} n(E_{f_n}, T) &= N_c \exp\big(\big(E_{f_n} - E_c\big)/kT\big) \\ p(E_{f_p}, T) &= N_v \exp\Big(\Big(E_v - E_{f_p}\Big)/kT\Big) \end{aligned} \qquad \textbf{2.4}$$

Where N_c and N_v are the effective conduction band and valence band density of states. A useful relation can be found by taking the product of these two equations at equilibrium

$$np = n_i^2 = N_c N_v \exp\big(-E_g/kT\big) \qquad \textbf{2.5}$$

Where n_i is the intrinsic carrier density. This relation shows that at equilibrium the product of the carrier densities is a constant throughout each semiconductor layer. It is independent of the position relative to the junction and it is even independent of the doping level. Outside of equilibrium the product becomes

$$np = n_i^2 \exp\big(\Delta E_f/kT\big) \qquad \textbf{2.6}$$

Where ΔE_f is the separation between the Fermi levels.

The gradient of the electrochemical potential is the driving force for the movement of the carriers. The currents of the carriers can be expressed as

$$\begin{aligned} j_n &= \mu_n n \nabla E_{f_n} \\ j_p &= \mu_p p \nabla E_{f_p} \end{aligned} \qquad \textbf{2.7}$$

Where μ_n, μ_p are the mobilities of electrons and holes. The gradients of the Fermi levels can be found from taking the gradient of equation 2.4

$$\begin{aligned} j_n &= \mu_n(n\nabla E_c - nkT\nabla \ln(\mathrm{N_c})) + qD_n\nabla n \\ j_p &= \mu_p(p\nabla E_v + pkT\nabla \ln(\mathrm{N_v})) - qD_p\nabla \mathrm{p} \end{aligned} \qquad \textbf{2.8}$$

Where the Einstein relation has been used to replace the mobility with the diffusion constant D. In compositionally invariant materials the band energies depend only on the electric field (F) as $\nabla E_c = \nabla E_v = qF$ and the conduction band density of states is constant. In this case

$$\begin{aligned} j_n &= q\mu_n F n + qD_n\nabla n \\ j_p &= q\mu_p F p - qD_p\nabla \mathrm{p} \end{aligned} \qquad \textbf{2.9}$$

The first term in these equations is known as drift. It comes from the action of the electric field on the carriers. The second term is the diffusion term that comes from the concentration gradient of the carriers. For materials that vary in composition there are additional effective force fields caused by variations in bandgap, electron affinity and band edge density of states. These effective forces can be utilised in devices, for example some devices deliberately widen the bandgap of the absorber layer near the back contact to create an effective field which reduces recombination at the back surface.

In quasi thermal equilibrium the carrier densities are constant which gives the continuity equations

$$\begin{aligned} 1/\mathrm{q}\nabla \cdot j_n + G - R = 0 \\ -1/\mathrm{q}\nabla \cdot j_p + G - R = 0 \end{aligned} \qquad \textbf{2.10}$$

Where G and R are the net generation and recombination rates. These combine with the current equations 2.9 to give

$$\begin{aligned} D_n\nabla^2 n + \mu_n n\nabla \cdot F + \mu_n F\nabla \cdot n + G - R = 0 \\ D_p\nabla^2 p - \mu_p p\nabla \cdot F - \mu_p F\nabla \cdot \mathrm{p} + G - R = 0 \end{aligned} \qquad \textbf{2.11}$$

There are several different mechanisms for recombination that are discussed in the next section. The main generation comes from optical excitation.

2.1.5 Recombination mechanisms

In real solar cells the separation of excited electrons and holes is not perfect and some recombine in the device instead of travelling around the external circuit, reducing the current and voltage that the device can produce. In a perfect device the only recombination mechanism is radiative, which is the reverse process by which the photons were absorbed. In real devices there are other recombination mechanisms that limit the device before the radiative recombination limit.

Recombination mechanisms can be classified according to where the excess energy is transferred. In the case of radiative recombination the energy is transferred to a photon. There are two more cases which are the energy being transferred to another carrier (Auger recombination) or the energy being transferred to a vibration of the crystal lattice (a phonon) through defect recombination. These three recombination mechanisms are illustrated schematically in Figure 2-9. In most devices defect related

recombination is the dominant mechanism, although in some high efficiency devices Auger recombination is dominant.

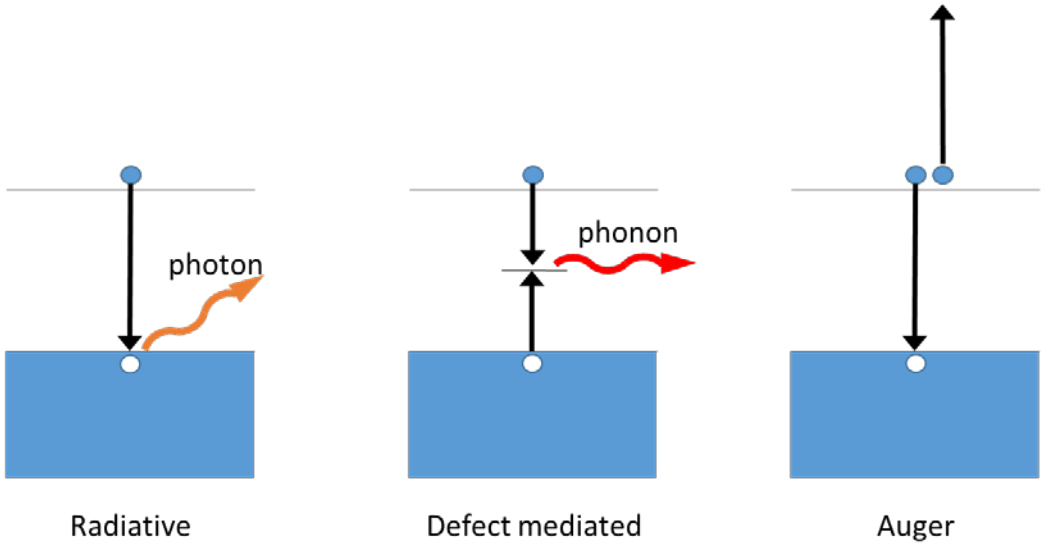


Figure 2-9: Schematic of different recombination mechanisms

If a defect introduces a localised state with an energy level in the band gap then that energy level provides an intermediate step for the relaxation of the electron by absorbing alternately electrons and then holes. After a carrier is captured by the localised state it can either be re emitted, in which case recombination has not occurred, or a carrier of the opposite type can be captured and recombination has occurred. This type of recombination is known as Shockley Read Hall (SRH) recombination. The net rate for SRH recombination is given by the equation [7]

$$R = \frac{np - n_i^2}{\tau_{n,SRH}(p + p^*) + \tau_{p,SRH}(n + n^*)} \qquad 2.12$$

Where $\tau_{n,SRH}$, $\tau_{p,SRH}$ are the SRH lifetimes for electrons and holes. n* and p* are the auxiliary carrier densities, they are the carrier densities that would be realised if the Fermi level were at the trap level. The auxiliary carrier densities are high when the trap level is close the band edge, so from equation 2.12 we can see that in this case the recombination rate are slow. Physically this is because when a defect level has an energy close to the band edge the activation energy for a trapped carrier to be re-emitted from the defect back to the nearby band becomes small and so the probability of that occurring becomes large, much larger than the probability of the carrier being annihilated by a carrier of the opposite type. Thus defects with an energy level close to

the band edges are known as trap states because they continuously trap and re-emit carriers but do not act as efficient recombination centres. Defects with energy levels near the middle of the bandgap on the other hand are efficient at causing recombination and are known as recombination centres [7].

Radiative recombination is the direct recombination of an electron and a hole, with the emission of a photon. This reverse process is always be present and is the limiting process in an optimum device. Its rate is given by

$$R = B(np - n_i^2) \qquad \textbf{2.13}$$

Where B is the radiative recombination constant.

Auger recombination is a three carrier process where the energy from the annihilation of an electron hole pair is transferred to extra kinetic energy for the third carrier. Because it involves the collision of two carriers of the same type the rate depends strongly on the density of the majority carrier, and for very high doping the rate can become high. This eventually counteracts the beneficial increase in built in potential which also comes from increasing the doping. The rate for auger recombination is

$$R = C_n(n^2p - n_0^2p_0) + C_p(p^2n - p_0^2n_0) \qquad \textbf{2.14}$$

Where C_n, C_p are the auger coefficients. The first term is for the case where the excess energy is transferred to an electron (as in Figure 2-9) and the second term is for the case where the energy is transferred to a hole. In p type materials the first term is negligible and for n type materials the second term is negligible.

2.1.6 Depletion approximation

The equations 2.11 and 2.12 can be solved numerically in device simulation packages and this is the most accurate way to proceed. However by making an approximation, known as the depletion approximation, the equations can be solved analytically. In this way a better understanding of the devices can be developed along with some useful equations.

The depletion approximation states that for the purpose of calculating the electric field in a region near the junction the semiconductor is completely depleted of carriers. The net charge in this region is equal to the doping density. This is called the space charge region (SCR). The region outside of this is called the quasi neutral region (QNR), and it is approximated to be completely neutral of charge and have no electric field.

Using this approximation along with Poisson's equation the size of the depletion region on each side of the junction can be found

$$w_n = \sqrt{\frac{2\varepsilon_p \varepsilon_n N_A V_{bi}}{qN_D(\varepsilon_p N_A + \varepsilon_n N_D)}} \quad \textbf{2.15}$$

And

$$w_p = \sqrt{\frac{2\varepsilon_p \varepsilon_n N_D V_{bi}}{qN_A(\varepsilon_p N_A + \varepsilon_n N_D)}} \quad \textbf{2.16}$$

Where w_n, w_p are the depletion widths of the n and p sides of the junction respectively, N_D / N_A are the doping densities of the n / p sides and ε_n, ε_p are the permittivity on the n/p side of the junction. For a one sided junction, where one side of the junction is much more heavily doped than the other, the depletion width on the lightly doped side is much larger and most of the voltage drops on this side. For an n^+-p device the total width of the space charge region (w_{scr}) becomes

$$w_{scr} = w_p = \sqrt{\frac{2\varepsilon_p V_{bi}}{qN_A}} \quad \textbf{2.17}$$

When a bias V is applied to the device the band bending and width of the space charge region changes according to

$$w_{scr} \approx \sqrt{\frac{2\varepsilon_p (V_{bi} - V)}{qN_A}} \quad \textbf{2.18}$$

The change in the depletion width with voltage creates a stored charge and gives rise to a capacitance. This mechanism of charge storage in photovoltaic devices is known as the junction capacitance and it can be a useful way to determine the doping density N_D, N_A as discussed further in section 3.1.

The depletion approximation can be used to solve for the current through the device. It is found that the current is given by

$$j = j_0 \left(\exp\left(\frac{qV_j}{AkT}\right) - 1 \right) - J_{ph} \quad \textbf{2.19}$$

Where J_{ph} is the photocurrent; A is an ideality factor which depends of the dominant recombination mechanism and j_0 is given by

$$j_0 = j_{00} \exp\left(\frac{E_a}{AkT}\right) \quad \textbf{2.20}$$

Where J_{00} is a constant and Ea is the activation energy of the dominant recombination mechanism, which will often be equal to the bandgap energy.

The ideality factors for different recombination mechanisms are shown in Table 2-1.

Table 2-1: Ideality factor for different dominant recombination mechanisms

Dominant recombination mechanism	Ideality factor
SRH recombination in the SCR	2
SRH recombination in the QNR	1
Interface recombination	1
Auger recombination	2/3
Radiative recombination	1

Often the dominant recombination mechanism is different at low and high voltages. For example at low voltages SRH recombination in the space charge region can dominate giving an ideality factor of 2, and then at higher voltages SRH recombination in the quasi neutral region can become dominant since with an ideality factor of 1 it has a stronger voltage dependence.

2.1.7 Defects

Shockley Read Hall recombination via defects was discussed in section 2.1.5. The defects through which this occurs are now discussed in more detail. There are many different types of possible defect and they cover a large range of scales. Point defects are the smallest, they are atomic level defects in the periodicity of the lattice, caused by displaced or missing atoms, or incorporation of impurity atoms. There are also larger defects, which extend over a larger number of dimensions: 1D Line defects and 2D surface or grain boundary defects. Finally there are defects of the device rather than material defects, such as cracks or shunt pathways where a layer is missing in a small region. All of these defects have very important implications for device operation, however the discussion here is restricted to point defects, knowledge of which becomes necessary in chapter 5.

Figure 2-10 is a schematic of some of the different types of point defect, along with the notation used to denote them.

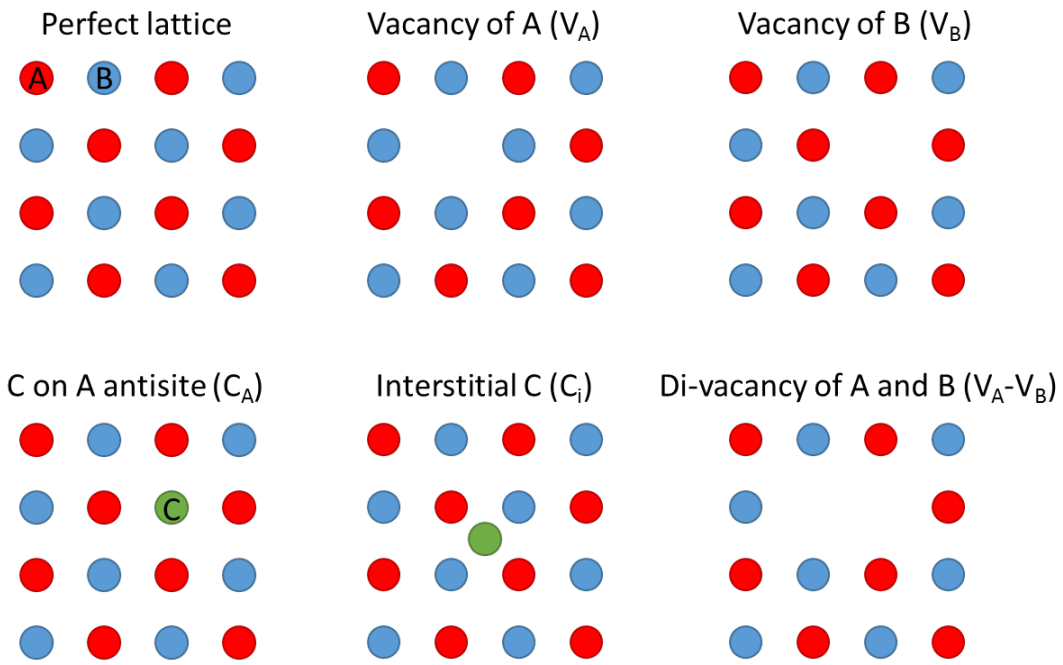


Figure 2-10: Schematic of different types of point defect in the fictional lattice composed of atoms of A and B. The element C is an extrinsic impurity.

The most basic point defects are vacancies, anti-sites and interstitials which are respectively missing atoms, atoms on the wrong site, and atoms inserted between normal lattice points. Complexes can form from combination of the basic defects, the V_A-V_B defect from Figure 2-10 is an example of a defect complex where two vacancies are paired together. Point defects can be intrinsic, meaning that they contain only atoms native to the lattice, as in the case of the examples V_A, V_B, and V_A-V_B in Figure 2-10. Alternatively if a defect contains impurity atoms not normally found in the lattice it is called an extrinsic defect. C_A and C_i are both examples of extrinsic defects. Point defects can introduce localised electronic levels within the bandgap of a semiconductor and depending on where within the bandgap the energy level lies they can act either as dopants, trap states or recombination centres.

The transition energy of a defect is the energy level of the Fermi level when there is equal probability of the defect having either of two charge states. These defect transitions are often depicted as in Figure 2-11 which shows the example defect transition energy levels calculated for CIGS [11].

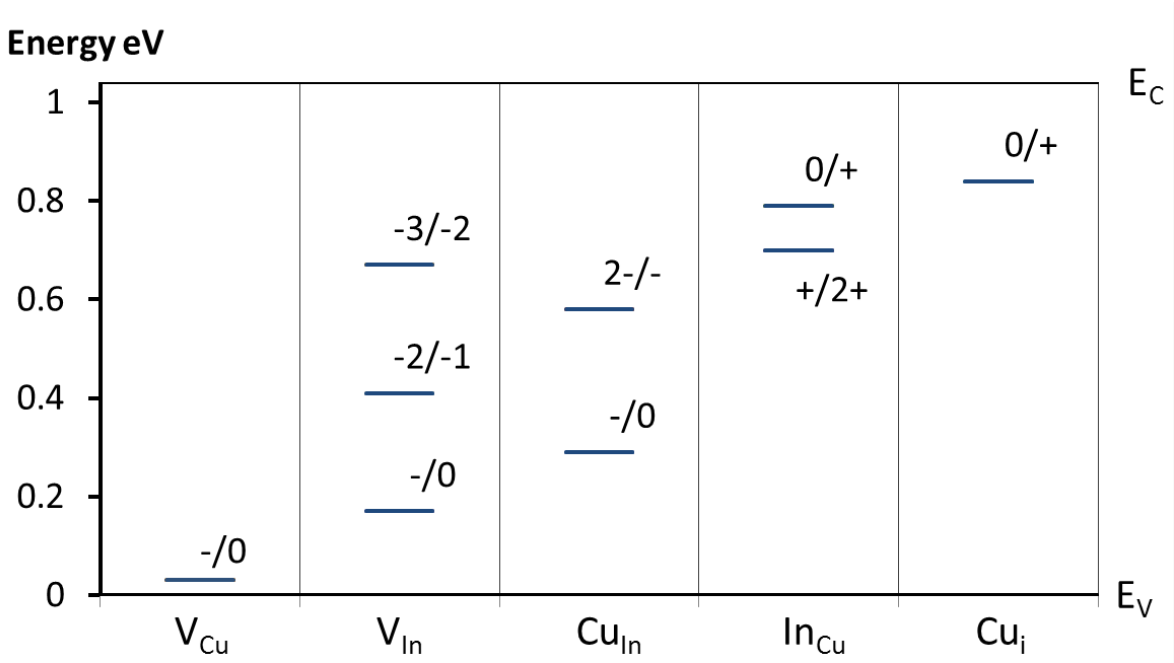


Figure 2-11: Transition energies for defects in $CuInSe_2$ as calculated from Ref [11]

The transition energy is often called the energy level of the defect and considered to be the energy of an electron that occupies the electronic state. However this is not really true since often when the electron occupies the state it then interacts with the lattice causing the atoms to move and relax to a lower energy positions. This in turn changes the energy of the electronic state [12]. This effect is usually known as lattice relaxation. In the common situation where the lattice relaxation is negligible, then the transition energy of the defect can be considered as the energy level for the electron occupying the localised state. Lattice relaxation can be observed for example in the difference between the energy of absorption and luminescence from a defect [12]. When the lattice relaxation is large the character of the defect can completely change, for example changing from a shallow to deep, or donor to acceptor. These types of defect can also exist in a metastable condition where they are thermodynamically less stable than an alternative configuration, due to an activation barrier of transition between the two different states. An example of this kind of metastable defect is the DX centre in AlGaAs, which is one of the best studied cases. Metastable defects have also been observed in several of the materials relevant to CIGS photovoltaic devices: $MoSe_2$ [13], ZnO [14] and also the CIGS absorber itself [15,16]. This type of defect appears to be at least partly responsible for the metastable behaviour of device performance observed in CIGS based photovoltaics.

2.1.8 Equivalent circuits

Equivalent circuits are representations of the electrical properties of a photovoltaic device using standard electrical components. They are a very useful tool for modelling and analysing I-V curves. A typical equivalent circuit is shown in Figure 2-12. In this circuit there is a constant current source which represents the generation of carriers by the incident light. In parallel with this there are two diodes, which represent different types of recombination. One diode has an ideality factor close to 1 and the other has an ideality factor close to 2. The diode with ideality factor 2 represents SCR recombination and also interface recombination. The diode with ideality factor 1 represents QNR recombination. In general these are the largest recombination pathways, but if Auger recombination is significant a diode with ideality factor of 2/3 should be included in the equivalent circuit model. Often, to make the model fit I-V measurement data of real solar cells, ideality factors slightly different from the theoretical values of 1 or 2 are used. Sometimes the same diode dominates over the whole range of interest and then it is possible to successfully model the device using a circuit with only 1 diode. The remaining elements are the series and shunt resistances. The series resistance (R_s) represents ohmic losses, for example at the contacts of the device. The shunt resistance (R_{sh}) represents the effects of ohmic defects, for example a small pinhole in the device allowing contact between the front and rear contacts.

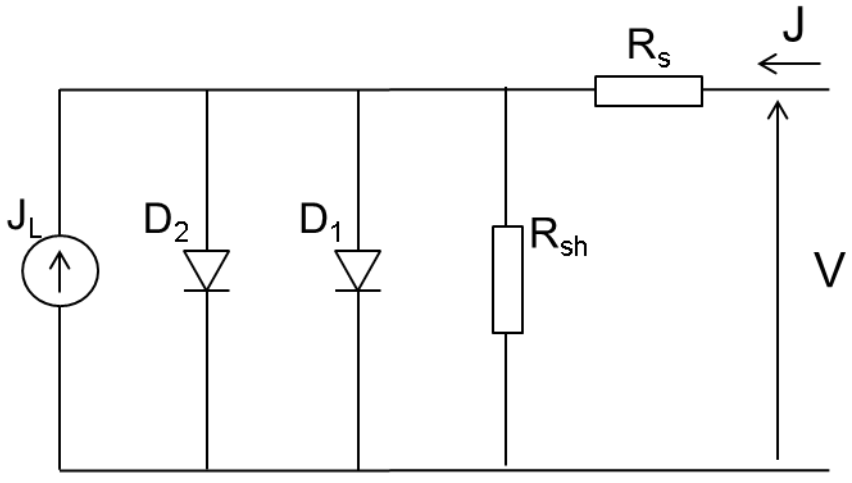


Figure 2-12: Two diode equivalent circuit diagram of a solar cell

From the diode model we get an implicit equation for the solar cell current. In the case that one diode dominates the recombination current we get

$$J(V) = -J_{ph} + J_0\left(\exp\left(-\frac{q(V+JR_s)}{AkT}\right)-1\right)-\frac{V+JR_s}{R_{sh}} \qquad \textbf{2.21}$$

This equation can be solved numerically to show the dependence of a device on irradiance, temperature, series resistance and shunt resistance. In the special case of the open circuit voltage, and when the shunt resistance is high, the equation has a simple explicit solution.

$$V_{oc} = -\frac{AkT}{q} ln\left(\frac{j_{ph}}{j_0}+1\right) \qquad \textbf{2.22}$$

Figure 2-13 shows the I-V curve for different irradiance values, the photocurrent generated in a solar cell is linearly proportional to the incident irradiance, but the open circuit voltage also increases logarithmically with the irradiance. Figure 2-14 shows the variation of the I-V curve with temperature. The main effect is a linear decrease of Voc with temperature. There is in fact a very slight increase in current with temperature which is not evident from equation 2.22 and is caused by a slight narrowing of the bandgap with increasing temperature. For many purposes this change is small enough that Isc can be considered to be constant with temperature. For silicon the bandgap at 0°C is 1.13eV which decreases to 1.10eV at 100°C, corresponding to a 6% increase in short circuit current[17,18].

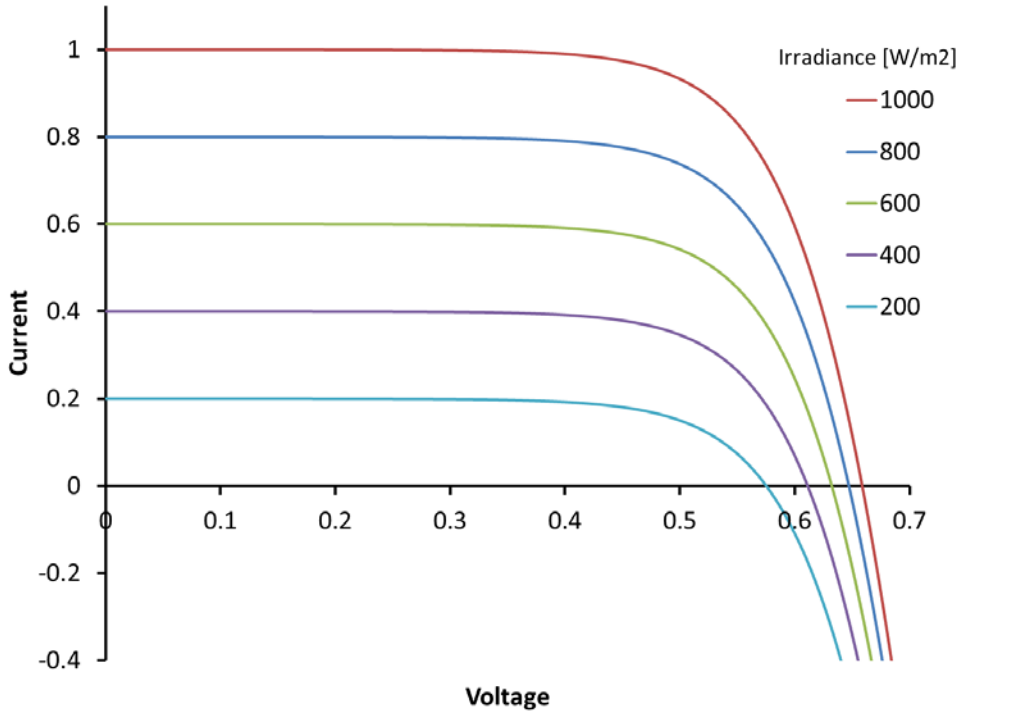


Figure 2-13: I-V curves at different irradiance values.

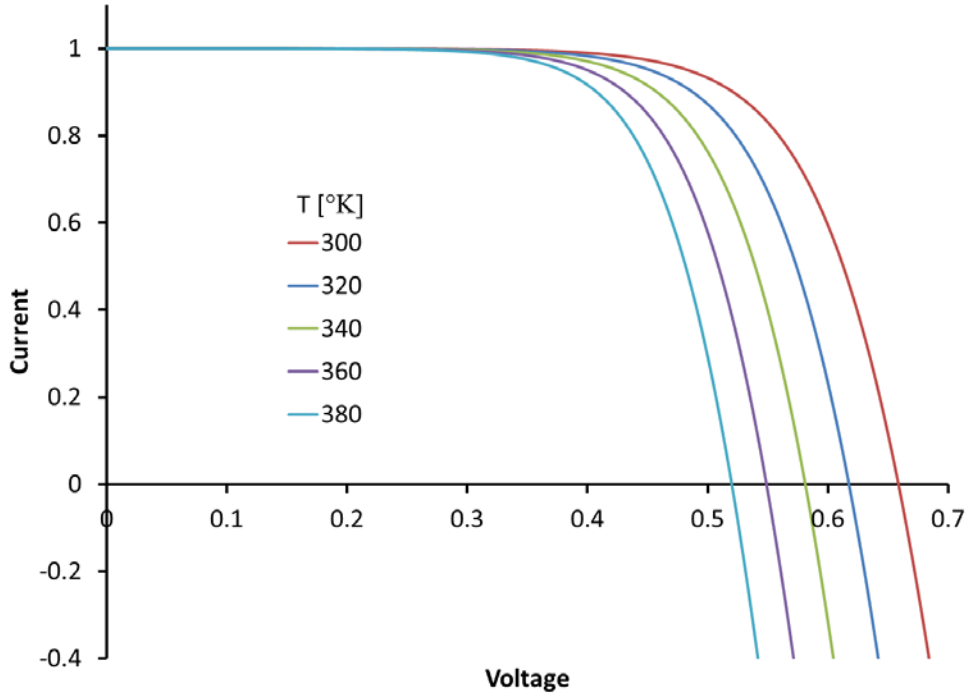


Figure 2-14: I-V curves at different temperatures.

The series and shunt resistances both mainly affect the fill factor of the device but in slightly different ways. The series resistance causes a voltage drop in the device which is larger at higher currents. As the series resistance increases it reduces the slope of the I-V curve at the Voc as seen in Figure 2-15.

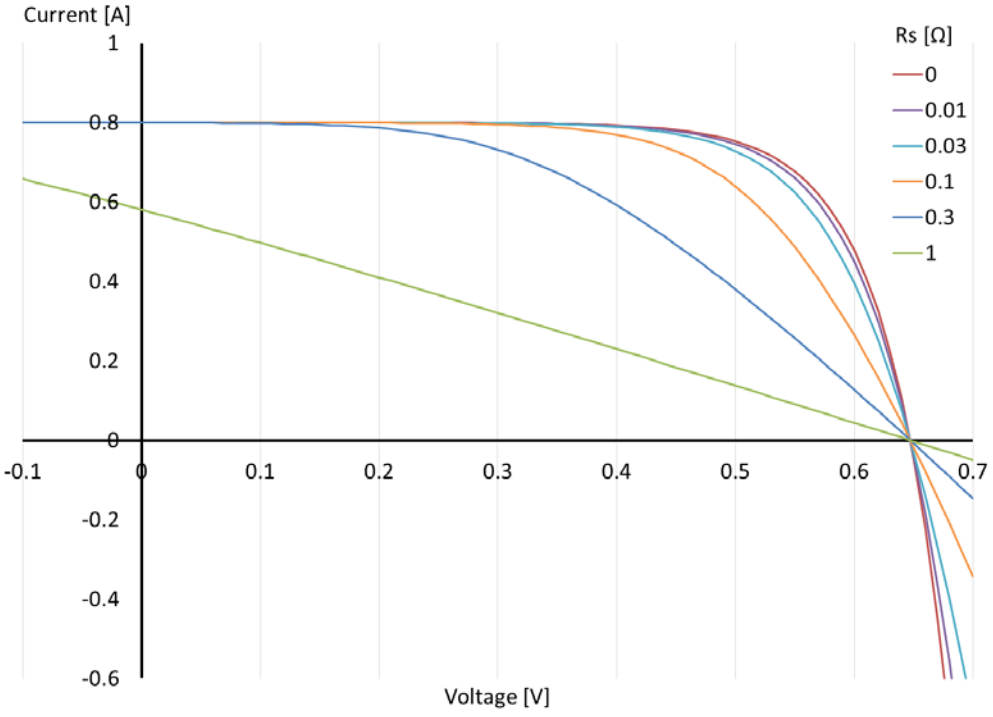


Figure 2-15: Effects of series resistance on I-V curves

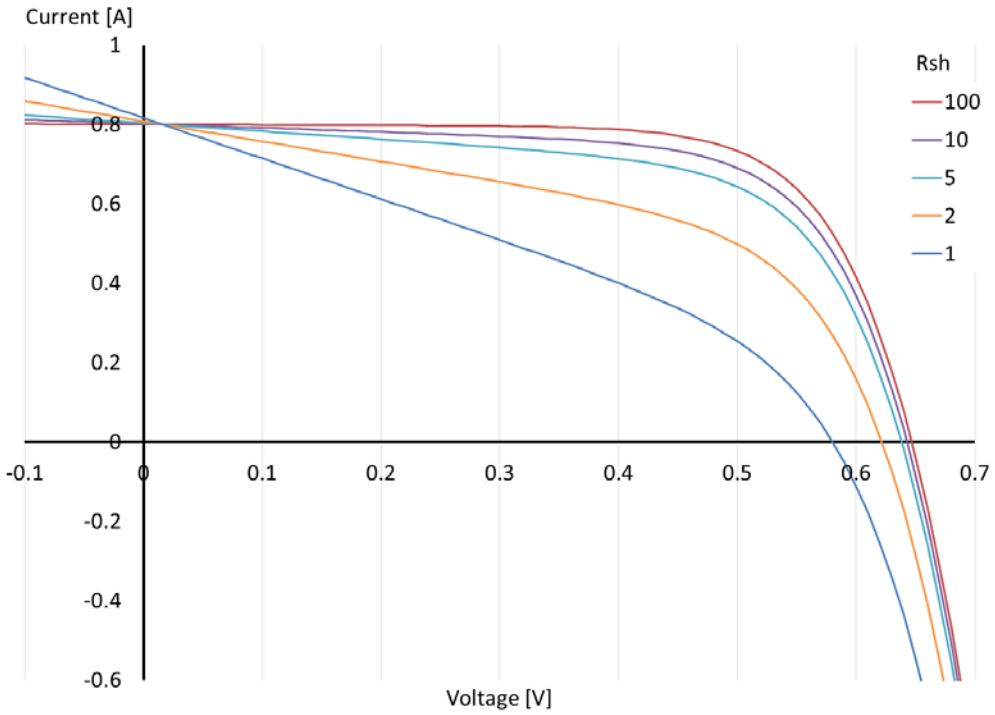


Figure 2-16: Effects of shunt resistance on I-V curves

The shunt resistance works in the opposite way, a more shunted device has a lower shunt resistance, which increases the slope of the I-V curve at the Isc point. Figure 2-16 shows the effect of varying shunt resistance on the I-V curve.

2.2 Different PV technologies

The first photovoltaic cell was created by Becquerel in 1839 more than 175 years ago, so it is unsurprising that since then a whole host of variations on the technology have been explored and developed. Silicon solar cells are by far the market leaders but thin film technologies based on CdTe and Cu(In,Ga)Se_2 absorbers also have a significant market share. Within the umbrella of Si solar cells there are many variations, including whether the cell is mono- or multi- crystalline; whether the base is p type or n type and many more. The device structures which will be relevant in the work of this thesis are the high efficiency silicon technologies, which are relevant because of their high capacitance, and the thin film CIGS technology, which is relevant because of its metastable behaviour. These relevant device structures are presented here.

2.2.1 CIGS

Thin film photovoltaics are a promising technology for several reasons. They have the potential to reduce the production cost and energy payback time of photovoltaics, they can be made flexible which is an advantage for some applications and finally, because of

potentially more optimum bandgap energies, they have higher potential maximum efficiencies than silicon based devices. This is a point which has become more relevant recently as the record efficiency of thin film devices has increased rapidly over that last few years. The record at the time of writing of May 2016 stands at 22.3% for a CIGS device, which is above the record for multi-crystalline silicon at 21.3% and starting to approach the 25.6% efficiency record for a Si heterostructure device[19]. The structure of a typical CIGS solar cell is shown in Figure 2-17.

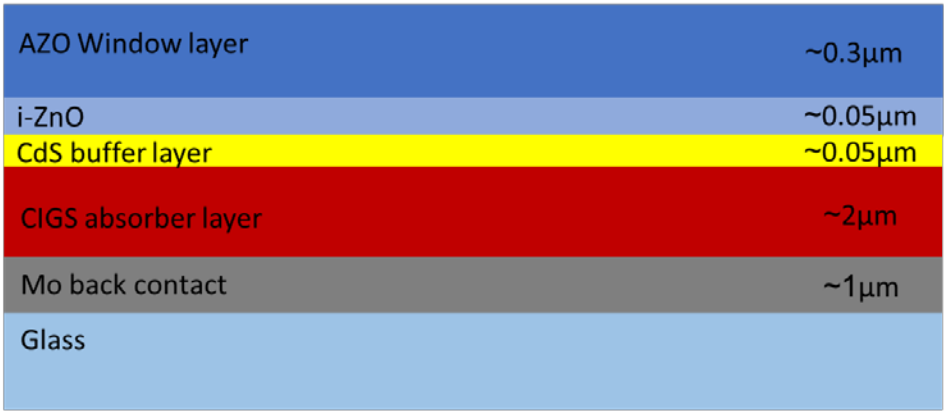


Figure 2-17: CIGS device structure.

In the language of thin film photovoltaics, the CIGS layer is the absorber. It is an intrinsically p type polycrystalline semiconductor $Cu(In_x,Ga_{1-x})(Se_{2y},S_{2-2y})$ with a variable bandgap depending on the relative ratio of In/In+Ga and S/S+Se. The bandgap of the absorber layer can be varied across the range 1.0eV to 1.7eV, although in practice the best devices are made with a bandgap of around 1.15eV. The window layer is a transparent conductor, usually ZnO:Al (AZO). It acts both as the n-type part of the junction and also to conduct current laterally out of the device. The buffer layer is not completely necessary to form a pn junction but it significantly improves the performance of the device. Various different materials can be used for the buffer layer, the most common is CdS but many other options are available [20]. There are a many different variables in CIGS device construction which is reflected in the way that many of the devices have very different characteristics, as will be seen later in the sections on preconditioning in these devices.

2.2.2 High efficiency Si concepts

Heterojunction with Intrinsic Thin layer (HIT) photovoltaics are a high efficiency Si device structure. In this device structure a thin layer of intrinsic a-Si:H is placed

between the n and the p sides of the junction as shown in Figure 2-18. The intrinsic layer provides excellent surface passivation.

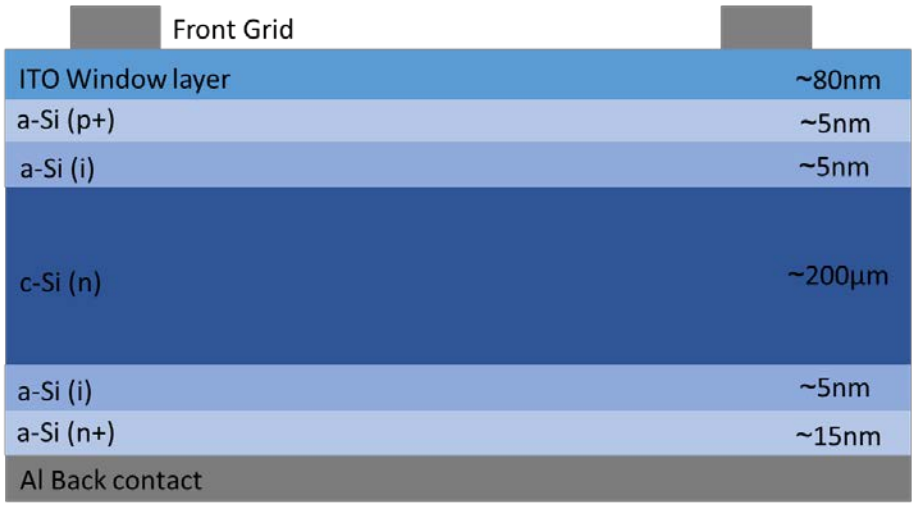


Figure 2-18: HIT device structure.

N type device solar cells are another way to achieve higher efficiencies. The reason is that the Boron used for p type material combines with Oxygen impurities and the resulting Boron-Oxygen defect acts as a recombination centre. Using an n type base material it is possible to get wafers with fewer recombination centres and consequently higher minority carrier lifetimes and higher efficiencies.

Interestingly, the Boron-Oxygen defect is another example of a metastable defect and is responsible for the light induced degradation observed in p type Silicon solar cells [21]. Light induced degradation occurs in the first hours of light exposure and can be reversed by thermal annealing.

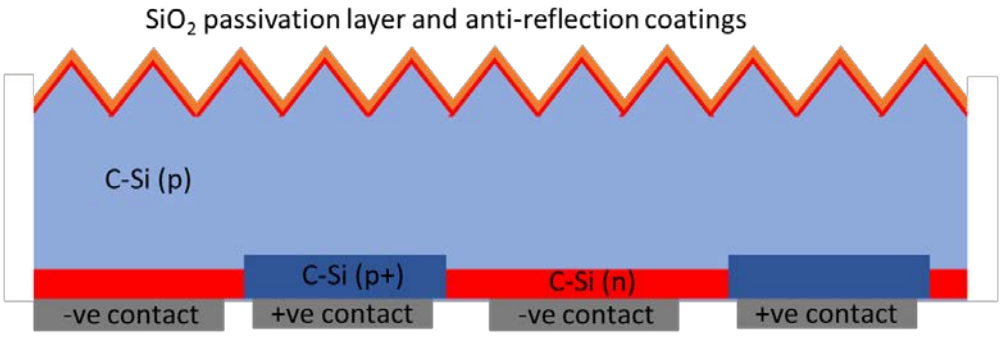


Figure 2-19: Back contact solar cell

Back contact solar cells are another concept to achieve high efficiencies where the contacts are moved to the back of the device, so no shading losses from the metallisation grid occur. In order to achieve a junction on the back of the device high diffusion lengths / minority carrier lifetimes are necessary.

2.3 Performance measurements

2.3.1 Standard Test Conditions

The standard test conditions (STC) for reporting the efficiency of solar cells is defined in IEC 61583 [22] and is by far the most common set of conditions used for reporting photovoltaic device performance. The conditions are a device temperature of 25°C with 1000Wm^{-2} irradiance at normal incidence and a spectrum matching the AM1.5G standard spectrum. Periods of such high irradiance usually heat the module to temperatures significantly above 25°C, however this temperature is convenient for indoor measurements because it is an easily achievable ambient temperature, and therefore device temperature. By only illuminating the module for a short period during the measurement it does not heat up significantly.

In reality, it is often not possible to achieve these conditions sufficiently closely and in particular it can be difficult to match the spectrum. Corrections should be made to account for differences between the actual measurement conditions and the reporting conditions. For small temperature deviations linear interpolation for the values of Isc, Voc, Pmpp and FF can be made. For irradiance deviations a linear correction can be made for Isc but a logarithmic interpolation should be made for Voc and a polynomial interpolation should be used for Pmpp. Another standard IEC 60891 [23] provides correction procedures for the whole I-V curve. For deviations from the standard spectrum there are two possible ways to proceed. If the reference device used to set / measure the intensity of the illumination has the same spectral response as the device under test then the spectral difference has exactly the same effect on the reference device as it has on the device under test and the spectral deviation can be ignored. An alternative option is to use spectral response measurements of the device under test and the monitor device, along with the measurement spectrum to calculate a correction factor, known as the spectral mismatch factor.

$$MMF = \frac{\int d\lambda G_{sim}(\lambda) SR_{DUT}(\lambda) \int d\lambda G_{STC}(\lambda) SR_{ref}(\lambda)}{\int d\lambda G_{STC}(\lambda) SR_{DUT}(\lambda) \int d\lambda G_{sim}(\lambda) SR_{ref}(\lambda)} \quad \textbf{2.23}$$

Where the G is the irradiance of the simulator (sim) or AM1.5 spectrum (STC); SR is the spectral response of the device under test (DUT) or the reference device (ref). It can be difficult to make absolute measurements of spectral response and often an absolute factor multiplies the result. Due to the construction of the MMF these factors in the measured spectral response cancel.

2.3.2 Other performance measurement conditions

Standard test conditions are useful for comparison between devices because the performance of most devices is reported at these conditions. However, for predicting the actual outdoor performance of devices the performance at STC can provide only a basic first order approximation, since the outdoor operating environment spans a wide range of conditions and the temperature and irradiance dependence is not the same in different devices. The solution given within the standard [22] is to measure the device at different conditions. Table 2-2 shows the different conditions defined for reporting, although the measurements are made over a full matrix of irradiance and temperature conditions. The NOCT (Nominal Operating Cell Temperature) condition is an attempt to include information about the amount of heating that occurs in the module when it is operating. It is defined as the temperature that the cells of the module operate at when the module is exposed to 20°C air temperature, 800Wm^{-2} irradiance and 1ms^{-1} wind speed. In practice other aspects such as how the module is mounted and the wind direction can also make a considerable difference to the operating temperature so this condition is not strongly defined [24]. The temperature of the module during operation can be approximated by the equation.

$$T = T_{air} + (NOCT - 20)G/800 \qquad \textbf{2.24}$$

Which is useful for predicting energy yields.

Table 2-2: Set conditions for the reporting of photovoltaic module efficiency, as defined in IEC

Condition	Temperature [°C]	Irradiance [Wm^{-2}]
STC	25	1000
NOCT	20 (ambient)	800
Low Irradiance	25	200
High Temperature	75	1000
Low Temperature	15	500

While it is convenient to measure at a single condition, or a limited number of set conditions it is more representative of outdoor operating conditions to measure the energy generated over a set time period with varying conditions. Standards for this reporting including the creation of standard days are under discussion and will eventually form the standards IEC 61853-3 and 61853-4 [25].

2.3.3 Apparatus

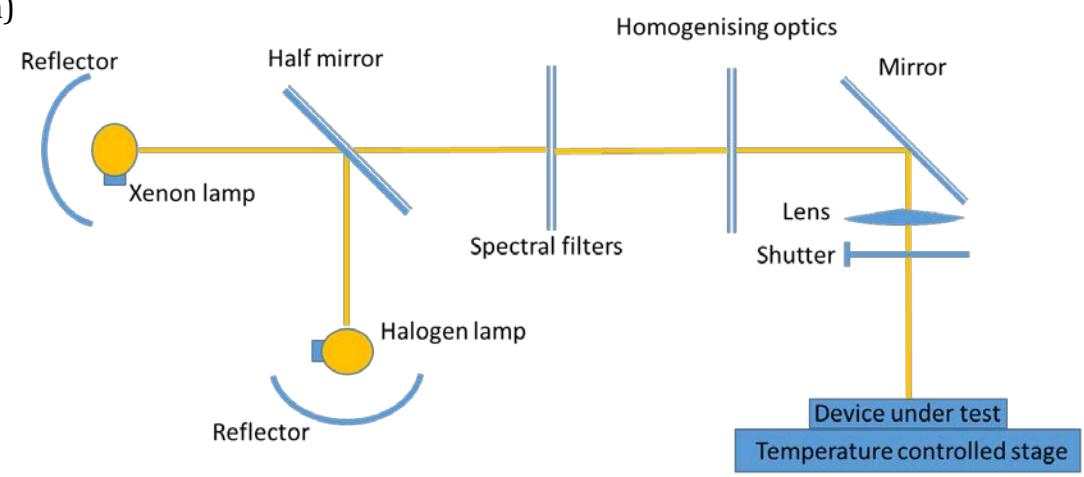
The most obvious way to measure the performance of a photovoltaic device is to leave it outside in the sun and monitor its output. Outdoor performance measurements of this type have many advantages and are indispensable as the only true measurement for the operation of a photovoltaic device in its final environment. However for STC measurements there is a huge drawback to using outdoor measurements in terms of practicality since they rely on waiting for the right time of day, the right time of year and the right weather conditions. For comparison of large numbers of devices this is simply not an option and measurements must be made using a solar simulator. The brief of a solar simulator is to illuminate a photovoltaic device with light which is comparable to that of the sun. Normally the solar simulator is used for STC measurements and therefore the light output is expected to be close to that of STC.

The illumination from the simulator can be pulsed or steady state. For large areas, such as full sized modules, pulsed simulators are normally used due to excessive power requirements and thermal management of steady state simulators. The pulse length in pulsed simulators varies quite widely but is typically in the range 1 to 30ms. It is easier to control the temperature of the device under test using pulsed simulators because the illumination pulse is usually short enough that it does not induce any significant heating in the device. For small area devices it is easier to use a light source that runs continuously in a steady state and this type of simulator is more common for the measurement of individual cells. Steady state simulators reduce the complication of measuring the I-V curve in a short time, which can cause problems for highly capacitive devices and devices with short timescale preconditioning effects.

Figure 2-20 show a schematic of a steady state simulator as well as a photo of one of the best steady state simulators at CREST. The irradiance is set before the measurement using a reference device. The device under test is then placed on top of a temperature

controlled stage. A shutter is used to prevent unnecessarily long light exposure and hence heating of the device.

(a)



(b)

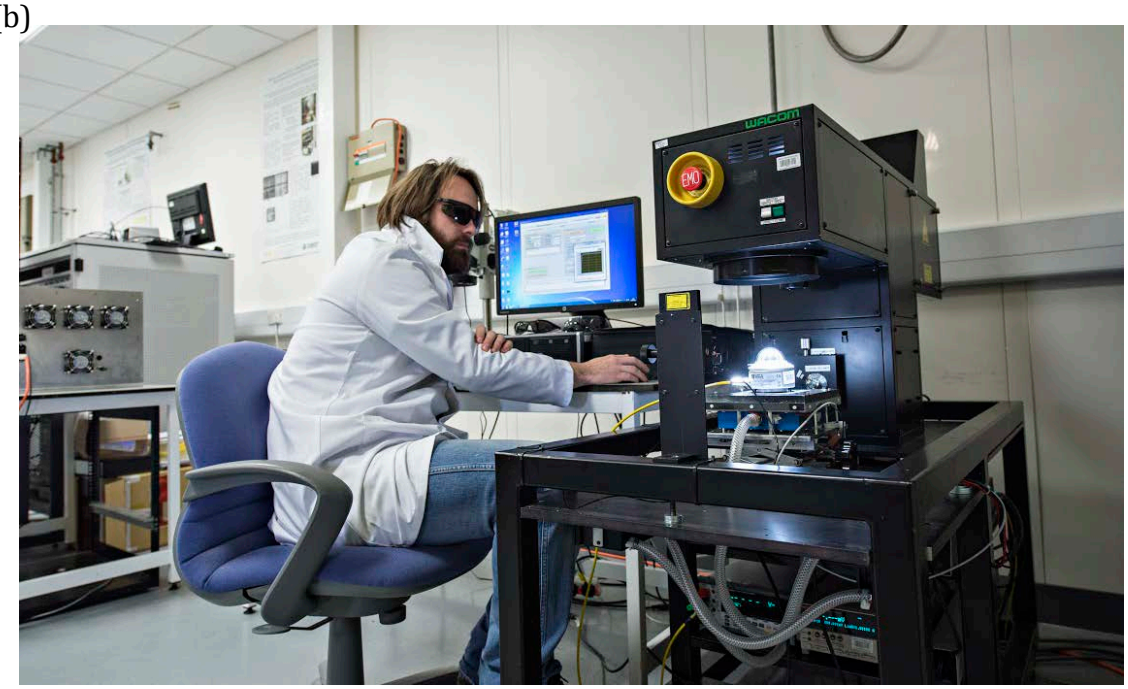
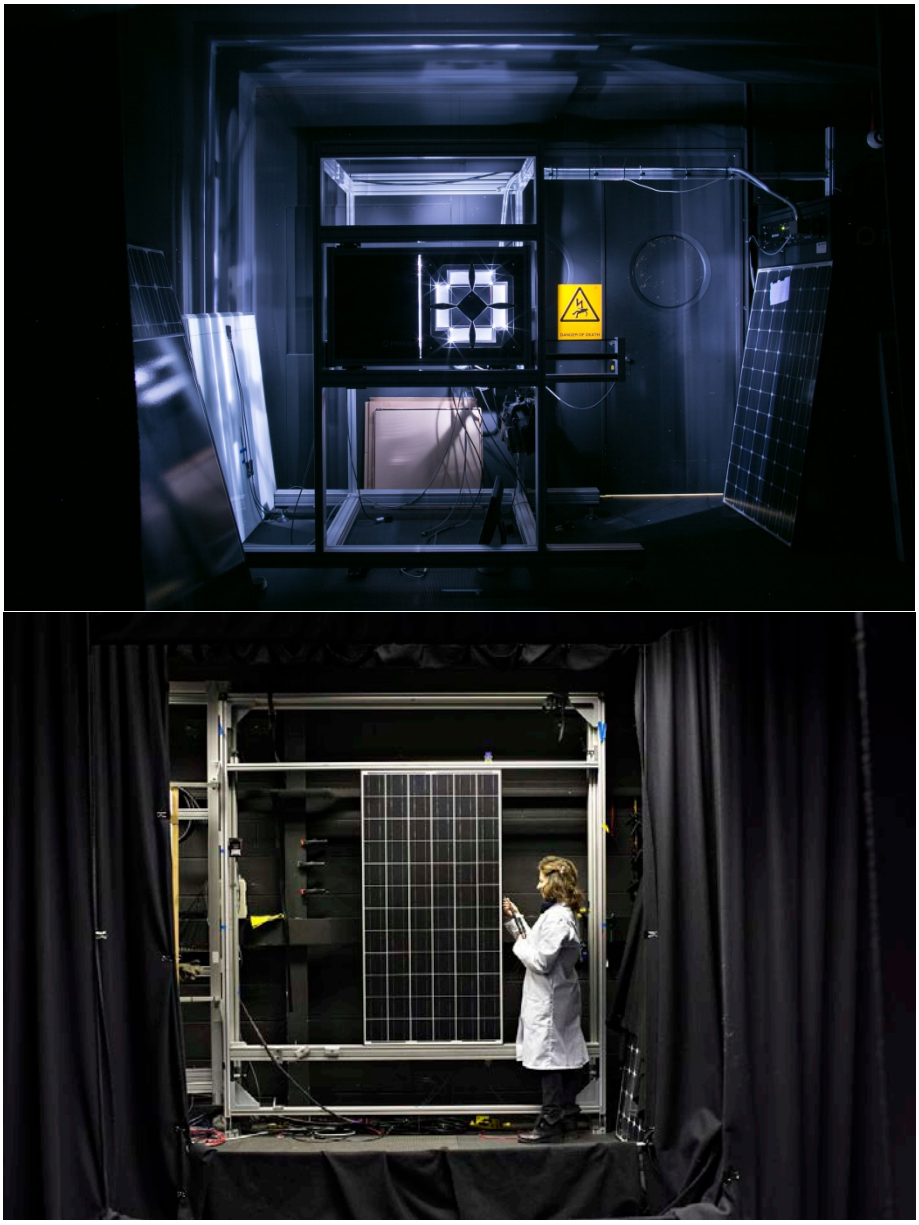


Figure 2-20: a) schematic of steady state solar simulator. b) Photo of the Wacom steady state simulator at CREST

Figure 2-21 shows a schematic of a typical pulsed solar simulator along with a photo of the PASAN IIIb simulator at CREST. The simulator has a 10ms stable (flat-top) illumination pulse. During the pulse the intensity is monitored using a diode on the edge of the illuminated area. The maximum illumination area is over 2x2m which is very difficult to illuminate using a steady state simulator, although a few large area steady state simulators do exist, for example the Apollo simulator at the European Solar Test Institute.



(c)

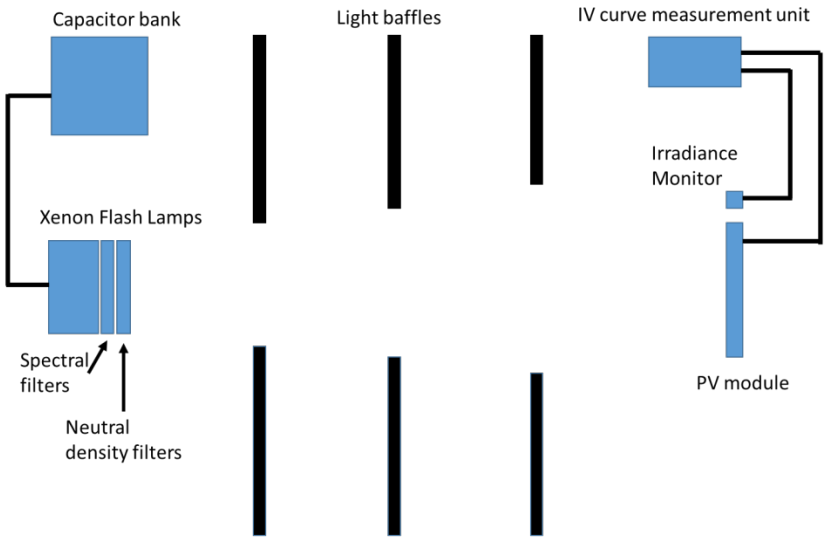


Figure 2-21: Photos and schematic of the PASAN IIIb simulator at CREST. (a) The flash lamps from the module rack. (b) The module rack from the flash lamps. (c) Schematic.

The important parameters for the simulator are the uniformity and stability of the illumination as well as its spectral match to AM1.5. An international standard IEC 60904-9 [26] classifies the quality of simulators according to these parameters, with a grade from A to C for each aspect. High grade simulators are very important for high accuracy measurements, but it can be difficult and expensive to achieve high grade pulsed simulators with long duration pulses for example over 100ms. Sometimes using a pulsed simulator as opposed to continuous light can cause other measurement problems, which will be discussed in the ensuing chapter.

3 Factors affecting Performance measurements of PV devices

3.1 Capacitance

A capacitor is an electrical element that stores charge when a voltage is applied to it. Having capacitors in parallel with other elements does not affect the current or voltage values for a steady applied voltage (DC), but when the applied voltage is changing then the amount of charge that the capacitor can store also changes and a current flows to charge/discharge the capacitor. Solar cells are not intended to be capacitors but they do have an internal capacitance. This capacitance puts a limit to the maximum speed that an I-V curve can be measured because at high voltage ramp rates the charging current is large and the measured current of the device does not represent the steady state operating value. This is a particular problem for measurements of many of the newer, high efficiency technologies since, for reasons that are discussed below, they tend to have higher capacitance than the traditional technologies. In these cases the solar simulator pulse length required to measure the devices using conventional methods becomes longer, typically exceeding 100ms [27], which is more than the pulse length of most commercial solar simulators. Long pulse lengths can be achieved but are technically more challenging and hence more expensive. The other main problem with long pulse lengths is that they can induce heating in the cells, reducing the accuracy of the measurement in a different way. In commercial use, long pulse lengths can become a bottleneck on the production line.

Despite being a potential measurement problem, the capacitance of solar cells can also be a useful feature. This is because it can be easily measured and its dependence on other parameters such as temperature, frequency and voltage gives valuable information about the device. An important example is the extraction of the carrier density and built in voltage from the voltage dependence of the capacitance.

3.1.1 Effects of capacitance on performance measurements

The effect of capacitance on I-V curve measurements depends on the direction of the voltage ramp. If the voltage is ramped from low to high it is referred to as a forward sweep, if the voltage is ramped from high to low it is referred to as a reverse sweep. In a forward sweep the voltage on the device is increasing during the measurement so the capacitance of the device charges up as the voltage increases. The charging of the

capacitance takes some of the photo current that would otherwise have been output by the device, so if the device is measured too quickly the performance is underestimated, this normally manifests itself mainly as a reduction in fill factor with a smaller reduction in Voc as seen in the example in Figure 3-1. Reverse sweep measurements are also shown in the figure. In this case the capacitance of the device is fully charged at the starting voltage and discharges during the measurement, resulting in an overestimation in performance. Again this usually manifests mainly in the fill factor but also a smaller amount in the open circuit voltage. If the reverse sweep measurement is sufficiently fast the rapid discharging can leads to a pronounced hump in the I-V curve as seen in the figure.

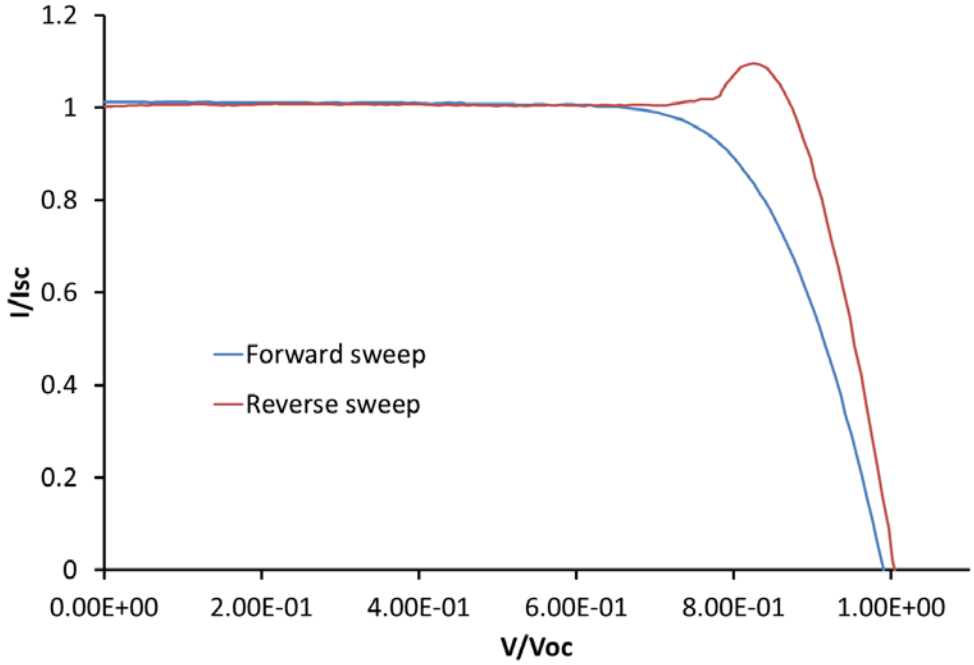


Figure 3-1: The effect of capacitance on I-V curve measurements.

The effects become greater the higher the capacitance of the device and the faster the measurement. It becomes a significant problem for measurements of high efficiency modules using pulsed simulators since the capacitance of these modules is very high and the measurement times are short. However the problem is not restricted purely to high efficiency devices. Dye sensitised solar cells in particular currently have efficiencies significantly below those of the best silicon devices, but they have extremely high internal capacitance, such that measurements of these devices can becomes problematic even on the timescales of around 10s.

3.1.2 Definition of capacitance

For ideal capacitors the capacitance (C) is defined as the charge (Q) stored per unit voltage applied to the terminals (V) giving the equation, $Q = CV$. The capacitance in this idealised case is a constant value independent of voltage or frequency. However many real capacitors, including solar cells, do not have a voltage independent capacitance. In this case there are two possible ways of defining the capacitance. The DC capacitance is defined by

$$C_{dc}(V) = Q(V)/V \tag{3.1}$$

Where $Q(V)$ is the total charge stored on the capacitor. The AC or differential capacitance is defined as the differential change in charge for a small voltage change

$$C_{ac}(V) = \frac{dQ(V)}{dV} \tag{3.2}$$

Any change in the stored charge draws or discharge a current equal to the rate of change of the charge so that

$$I_c = C_{ac}(V)\frac{dV}{dt} \tag{3.3}$$

Where I_c is the current into the capacitor. The differential form is normally easier to work with than the equivalent equation for the DC capacitance.

$$I_c = \left(C_{dc}(V) + V\frac{dC}{dV}\right)\frac{dV}{dt} \tag{3.4}$$

In the case of small oscillating signals complex impedance becomes a very powerful tool for analysing the phase and amplitude of the voltage and current in a circuit [28].

3.1.3 Mechanisms of charge storage in solar cells

There are several different mechanisms of charge storage in solar cells. The junction capacitance is the charge stored as a result of a change in the depletion width of the cell. This is normally the dominant capacitance when the cell is under reverse bias or at small forward bias conditions, typically up to half of the Voc, depending on the specific cell. At higher voltages the diffusion capacitance often dominates. This is the capacitance that results from the increase in minority carrier concentration in the quasi-neutral region of the device. There can also be a capacitance associated with the storage of charge in trap and interface states, which is called the transient carrier

capacitance [29]. This type of charge storage mechanism is the dominant mechanism of charge storage in dye sensitised solar cells, which have a particularly high capacitance due to a high density of electronic trap states in the porous TiO_2 layer.

For an abrupt one sided junction the junction capacitance is given by the equation [18]

$$C^{-2} = \frac{2(V_{bi} - V_{dc})}{q\varepsilon\varepsilon_0 N \quad A^2} \tag{3.5}$$

Where V_{bi} is the built in voltage, V_{dc} is the DC bias voltage, A is the area of the device, q is the charge of an electron, ε_0 is the permittivity of free space, ε is the relative permittivity of the base and N is the doping concentration. By fitting the measured capacitance to this relation it can be used to find the doping level and built in voltage of a device. This equation is valid for reverse bias and low forward bias voltages where this component of the capacitance is the dominant one. In thin film devices there are often a significant number of deep defect levels or interface states that contribute to the capacitance and affect the extracted value of N. For this reason doping densities measured using C-V are often donated N_{cv} to reflect that they may not represent true values. At higher forward bias equation 3.5 is not valid and in particular at $V_{dc} = V_{bi}$ there is a singularity in the equation. At these higher forward bias values the diffusion capacitance normally dominates. It is given by [30].

$$C_{diff} = C_0 \exp\left(b\frac{qV}{kT}\right) \tag{3.6}$$

where b is a fitting parameter and

$$C_0 = \frac{q^2 n_i^2 L_n}{kTN_A} \tag{3.7}$$

Where L_n is the minority carrier diffusion length and n_i is the intrinsic carrier density. This result (not including the fitting parameter) can be derived from considering an abrupt p-n junction in the limit of low injection and no recombination in the space charge region [18]. However, the measured capacitance for some devices only fit equation 3.6 when b is included and is not equal to 1. The origin of the fitting parameter is due to the violation of some of the assumptions of the derivation. The expressions for both the diffusion and junction capacitances are the differential form of the capacitance, this point sometimes causes confusion in the literature.

Using the expressions for the diffusion capacitance the minority carrier lifetime can be found from measurements of the capacitance at forward bias conditions. Alternatively, using the same assumptions of an abrupt p-n junction and low injection, the following expression for the minority carrier lifetime can be derived.

$$\tau = \frac{C_{diff}}{dI/dV_j} \qquad \textbf{3.8}$$

This provides a simple way to measure the minority carrier lifetime. High efficiency photovoltaic technologies are often observed to have higher capacitance; the reason for this is that they tend to have high quality materials with very long minority carrier lifetimes. The high minority carrier lifetimes mean that, for the same voltage, a much higher concentration of minority carriers is accumulated and the diffusion capacitance is much higher, as reflected by the dependence of equation 3.7 on L_n. It is not a coincidence that the higher efficiency technologies tend to have a higher capacitance and it is therefore likely that the associated measurement problems will become more prevalent in the future.

In general, the capacitance could depend on the illumination level as well as the voltage; however, it has been previously shown that the diffusion capacitance in high efficiency silicon cells is not significantly dependent on illumination intensity [28]. This is an important point which means that it should be valid to use directly measured C-V profiles in the dark in order to model the dynamic response of illuminated PV modules, as is done in chapter 4.

3.1.4 Dynamic equivalent circuit models.

In section 2.1.8 an equivalent circuit model of a solar cell was introduced. In that circuit model only the steady state operation is represented, but the model can be extended to include the capacitance of the solar cell as in Figure 3-2. This model now also represents the dynamic behaviour of the cell. The diffusion and junction capacitances are represented as separate elements, but those elements actually represent voltage dependant capacitances, rather than the ideal capacitors usually depicted by the circuit element as drawn. In cases where they were relevant, other contributions to the capacitance could also be added.

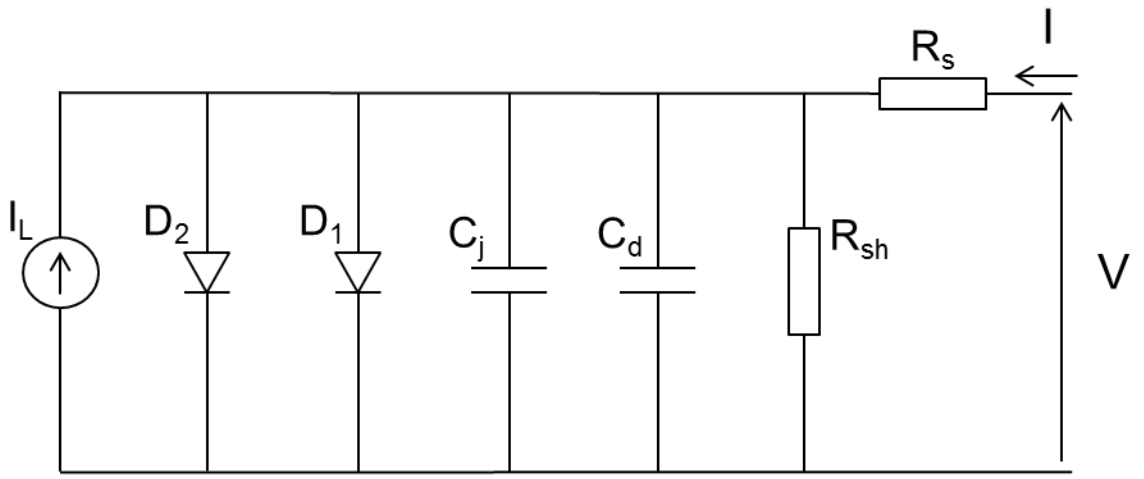


Figure 3-2: Dynamic equivalent circuit diagram for a solar cell. Note that the capacitance elements for the junction capacitance (C_j) and diffusion capacitance (C_d) represent voltage dependent capacitors, rather than ideal capacitance elements.

When analysing small signals only the small voltage and current changes δV, δI need to be considered which leads to the simpler AC equivalent circuit shown in Figure 3-3. The element R_s is equivalent in both models, but the elements R_p and C are related to the elements in Figure 3-2 by the following relations.

$$R_p^{-1} = G_{d1}(V_j) + G_{d2}(V_j) + G_{sh}(V_j) \quad \textbf{3.9}$$

Where G is the differential conductance of the specified circuit element.

$$C = C_j + C_d \quad \textbf{3.10}$$

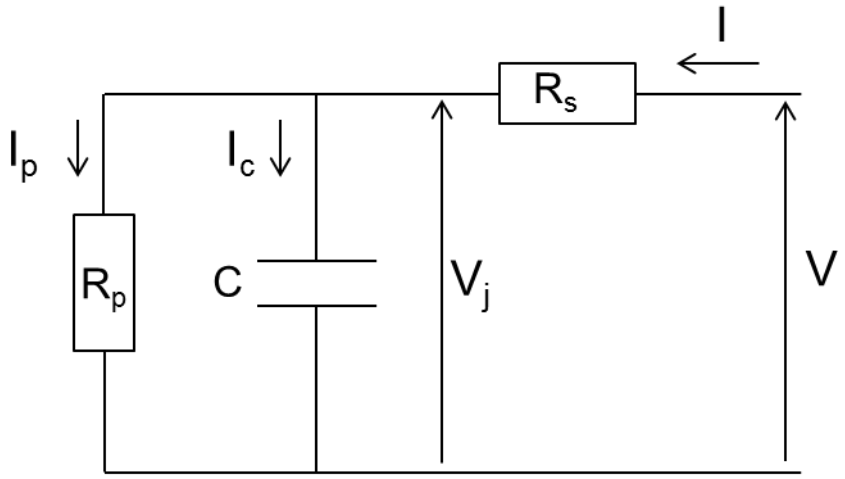


Figure 3-3: simplified equivalent circuit model for small voltage oscillations

Solar modules are made up of series and sometimes parallel connections of individual cells. Assuming identical cells, the capacitance of a series of N connection of cells is reduced by a factor of N whereas the series resistance of the cells is increased by a factor of N, the equivalent circuit of the module takes the same form as the equivalent circuit for a cell but with lumped values for the resistances and capacitances which are adjusted by the appropriate factor of N or 1/N. The trend towards fewer larger cells in modules therefore further contributes towards the increase in module capacitance. However, this increase in capacitance coming from larger cells does not lead to an increase in the error in performance measurements because the current also increases with the cell area, so that the percentage error from capacitive charging remains the same. Equally, the reduction in capacitance from having more cells in series does not affect the error from capacitive charging, because in order to measure the module in the same amount of time the voltage needs to be ramped faster such that the effects again cancel.

The capacitance of photovoltaic devices is regularly measured as the imaginary part of the admittance divided by the frequency. This method is used for example in C-V and admittance measurements. However, this method is only valid in the case where the series resistance of the device can be neglected. At higher bias voltages the value of R_p reduces dramatically and becomes comparable to the series resistance. In this case the impedance of the PV device is then given by

$$Z_{PV} = R_s + \left(i\omega C(V) + G_p\right)^{-1} \quad \textbf{3.11}$$

Now if the series resistance is not known it is necessary to make at least 2 measurements at different frequencies in order to obtain the capacitance.

3.1.5 C-V profiling

Capacitance-voltage profiling is used to find the doping density of the base (or in thin film terminology, the absorber) and the built in voltage of a photovoltaic device. The basic principle is to measure the junction capacitance as a function of voltage and use the expression 3.5 to extract the built in voltage and the doping density. This is often done using a Mott Schottky plot of $1/C^2$ Vs V so that the gradient of the plot yields the doping density and the intercept gives the built in voltage. This approach can be taken a step further. Since the depletion width of the device varies with applied bias, according

to 2.18 and the measured doping density is that at the edge of the depletion region, the technique can be used to measure the doping density as a function of distance from the junction.

In the case of a high concentration of deep defects or surface defects the results of the analysis are affected. In thin film devices in particular this can cause a significant problem as demonstrated in the simulation shown in Figure 3-4. The two CIGS device simulations differ only in that one has a high concentration of deep acceptors. The deep acceptors significantly affect the shape of the measured doping density profile, falsely creating the impression of a doping profile that increases towards the back of the device.

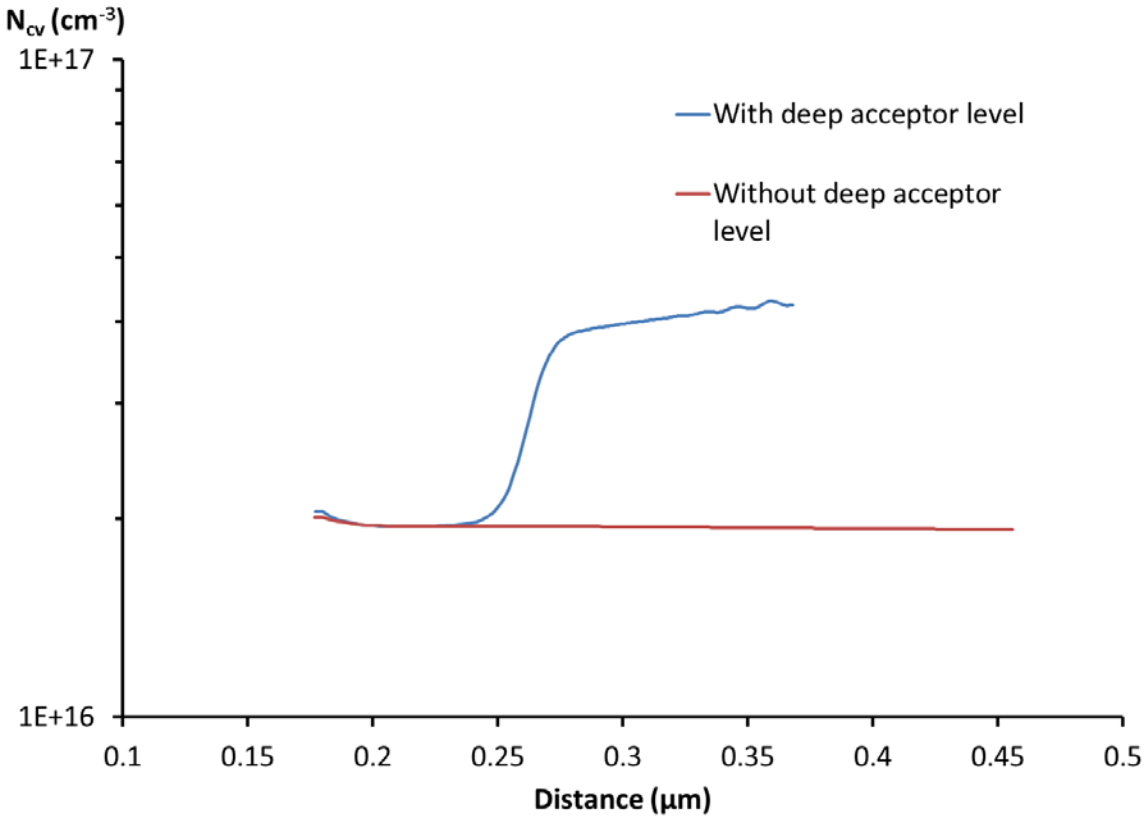


Figure 3-4: Simulated C-V profile for two different CIGS devices. The shallow acceptor doping in both devices is 2e16cm^{-3}, but in one device there is also a high concentration (1e17cm^{-3}) of deep acceptors located at mid gap. In the device with the deep acceptors the measured doping profile is significantly affected.

The discussion of capacitance in this section will be used in chapter 4 where a module C-V measurement system is built for the purpose of optimising I-V measurements of high capacitance modules. The C-V measurements will also be used to extract useful information about the modules. In particular in chapter 5 changes in the net doping density of CIGS modules will be measured during preconditioning.

3.2 Preconditioning in CIGS

3.2.1 Effects on performance measurements

Reversible changes in performance for CIGS devices have been observed since at least 1986 [31]. These changes are generally brought about by exposure to light or electrical bias, and often necessitate preconditioning of devices before performance measurements in order to bring them into a state more representative of stable outdoor operating conditions. Devices which exhibit these reversible changes are often called metastable, referring to the fact that they continue to exist in an unstable state for an extended period of time.

Commonly, devices are found to improve after light soaking or electrical forward bias, but there is a large variation in the changes observed, depending on the device. Sometimes it is predominantly the Voc of the devices that is reported to change [31-33], whereas other times the FF of the devices changes but the Voc remains relatively unchanged [34], or both are seen to contribute equally [35]. The magnitude of the changes varies significantly between devices. They can be very large, with >10% changes not uncommon, at the other extreme some devices display virtually no noticeable preconditioning at all. The important difference between metastable changes and permanent ones are that when the devices are left in the dark their performance gradually returns to its initial state. Elevated temperature is generally seen to increase the rate that the modules return to their initial state and is often used to achieve this in a shorter time [36]. The temperature coefficient for CIGS modules has been shown to depend on preconditioning state [37]. This also means that the difference between performance for preconditioned and unconditioned devices is less at higher temperatures.

For performance measurements it is usually necessary to perform some sort of preconditioning to try bring the device into a specific state. Depending on the purpose of the measurement the requirements of the preconditioning are different. As a minimum it should be possible to repeatably bring the module into the specific state. Normally it is also desirable that the measurement is representative of how the device performs in outdoor operation, this is especially true if the measurement is to be used for energy yield prediction. In the case of degradation studies, the metastability of these devices can swamp the impact of the irreversible degradation if careful attention is not

paid to the preconditioning of the modules before measurement. For example in ref [38] efficiency reduction of up to 20% after damp heat treatment were shown to be largely reversed by light soaking.

IEC 61646 [39] specifies preconditioning standards for thin film modules, but these standards were originally designed for a-Si which displays different characteristics. The standards require the module to be measured after successive light soaking periods of 43kWhm^{-2} integrated irradiance, until the relative changes in consecutive measurements of power are 2% or less. One study on the suitability of the standard for CIGS modules found that several improvements were needed to make the procedure more relevant to CIGS and CdTe modules, in particular minimum illumination intensity and changes to the stabilisation criteria [35]. An underlying assumption of light soaking preconditioning is that relaxation of performance changes takes longer than the time that the modules take to cool down after light soaking. In another study IEC 61646 was found that it was suitable, provided the measurements were made immediately after the preconditioning [40].

The timescale for CIGS preconditioning can vary considerably. Light soaking is generally applied for hours and the relaxation is often seen to take days [41]. However, effects on much shorter timescales have also been observed. For example, it has been shown that the pre-measurement state in the seconds or milliseconds before a measurement is important [42], and that short pulse simulators can underestimate device performance compared to steady state simulators [43,44], although this is not always found to be the case [45,46]. With such a spread in rates for the changes to occur it raises the question whether modules ever reach a stable state during outdoor operation, or whether the performance state of the devices oscillates on a daily basis. Some reports find evidence that the devices reaches a steady operational efficiency [44], another report showed that modules took 100min of light soaking to stabilise, then for different modules they found the relaxation occurred after 2-3 or 9-16 hours in the dark [47]. This indicates that some modules will not be operating at a stable performance state for a considerable proportion of the time.

Several studies have found that the effect of voltage bias is similar to that of light soaking [32,36,48]. This is important because electrical bias can be significantly easier to apply than light soaking for large area modules. However there are also some studies

which report that while electrical bias has an effect on the device performance it is not the same as the effect of light soaking [44,49]. This is an important point and possible reasons for this discrepancy will be discussed again in chapter 6.

CIGS photovoltaics are not alone in displaying metastable performance. a-Si based devices display a strong seasonal variation in efficiency due to the Staebler Wronski effect. This effect is well known and is due to breaking and reforming of dangling bond defects [6,50-52]. As previously mentioned, the initial light induced degradation in p type crystalline silicon devices is actually a metastable performance change which can be reversed by thermal annealing [21].

3.2.2 Other observable device metastabilities

In addition to changes in the I-V curve under operational conditions, there are various other changes that can be observed in CIGS devices. For example the capacitance of the device is often seen to change. Observing these other changes and probing outside the normal operating range of the device has provided considerable insight into the changes occurring during preconditioning and relaxation.

The spectrum of the incident light has an important impact on the changes in the device. Several different metastabilities can be identified / distinguished using different spectral and voltage bias conditionings, although as will be discussed, some may have the same microscopic origin. The main effects that can be seen are:

- Red light effect
- Blue light effect
- Forward bias effect
- Reverse bias effect
- Red on reverse bias

The red and blue light effects refer to specific metastabilities which occur depending on where in the device the light is absorbed. In this context 'red light' refers to light which is absorbed only in the CIGS absorber layer, and 'blue light' refers to light which is absorbed also by the buffer layer. For a typical CdS buffered cell with a CIGS layer bandgap of 1.15 eV the wavelength range for the red light effect is 1050 nm to 500 nm, and the blue light effect occurs for wavelengths below 500 nm. Some other common buffer layers are In_xS_y and Zn(O,S). Both of these buffers have much higher band gap

energies so that the onset of absorption in these layers occurs at shorter wavelengths, which has been shown to reduce the maximum wavelength for the onset of the blue light effect [53].

Under illumination with no blue content, a distortion of the I-V curve can be observed compared to the I-V curve measured under white light [54]. An example of this distortion is shown in Figure 3-5. At lower temperature the distortion can be quite severe and results in the crossover of the white and red light I-V curves [53,55]. Brief exposure to blue light removes the kink in the I-V curve and measurements made again without the blue content only gradually regains the kink in the I-V curve taking several hours to be fully restored [54]. A decrease in the capacitance is observed to occur along with the increase in fill factor after blue illumination. The decrease in capacitance from the blue light effect has been observed to anneal out at 350 K, which shows that the blue light effect is a thermally activated process [56]. The interpretation of this effect is that in the absence of blue light there is a photocurrent barrier and blue light has the effect of somehow reducing or removing that barrier, the different theories of what causes this barrier and it's modulation under blue light will be discussed in the next section on the microscopic origins of preconditioning, and then again in more detail in chapter 6.

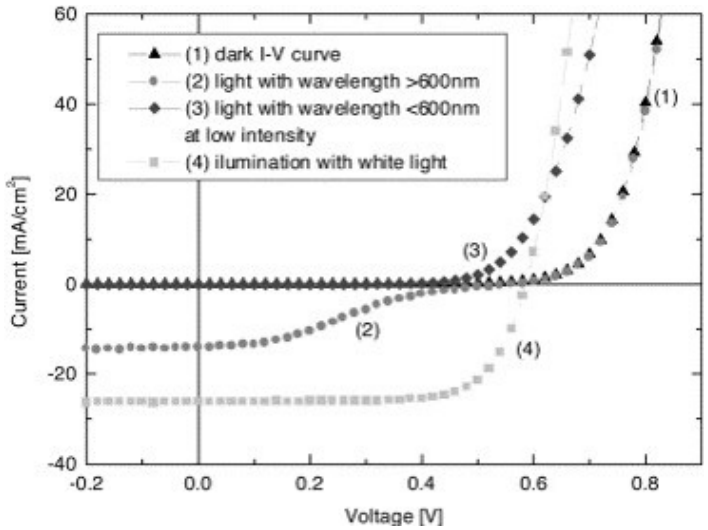


Figure 3-5: IV curves of a CIGS device with and without blue light. Reprinted from ref. [55] **with permission.**

Red light tends to increase the junction capacitance. Sometimes this can improve performance but it can also reduce the performance [56,57]. From studying the CIGS layer without forming a device, it has been shown that the absorption of light in this material causes persistent photoconductivity [58]. This photo induced increase in conductivity persists for extended periods. In ref [59] they used hall mobility

measurements to find that the increased conductivity is due to an increase in carrier concentration rather than an increase in mobility, thus we see that there is a change in the doping. Forward bias of the device is also usually seen to increase the capacitance.

When CIGS devices are reverse biased while illuminated with red light a strong decrease in the depletion width (increase in capacitance) and reduction in FF occurs [49]. Red light soaking and reverse bias separately also induce an increase in capacitance, the defining difference between this red on bias (ROB) state and the previous states is that the ROB metastability can be reversed by very short exposure to blue light, even at low temperatures of 100K. In the absence of blue light it persists at low temperatures and begins to anneal out above 250K. Since the incident light is only absorbed in the absorber layer this effect is clearly related to that layer, and seems to be due to the capture of a large number of electrons by defects in a region close to the interface. The fact that this defect is not occupied by electrons before the ROB treatment indicates that it should be close to the conduction band. In the case of a normal defect energy level this means the electrons are relatively easily thermally emitted which is not the case. The elimination by blue light seems to indicate that recombination with free holes is the dominant relaxation mechanism.

3.2.3 Microscopic origins of preconditioning

It is still under debate exactly what occurs microscopically during the observed metastable effects and how those microscopic changes affect the device performance. Many different hypotheses have been proposed, and there is a large literature on the topic. This section provides a brief overview, but the subject is revisited in more detail in chapter 6. Some of the explanations for the metastabilities in CIGS are

- Cu migration [60,61]
- Photodoping of the buffer layer [54]
- P+ layer [62,63].
- Metastable defects in the CIGS layer
- Metastable defects at the back contact [64]

It has been shown that CIGS thin films display persistent photoconductivity and that it is linked to the admittance and voltage changes in devices [58]. This is good evidence that at least in the case of the red light effect the metastable behaviour in CIGS devices is due to an intrinsic property of the absorber and not the buffer or an interface.

It has been shown from deep level transient spectroscopy (DLTS) measurements that during light soaking, the concentration of deep level defects decreases and the concentration of shallow acceptors increases in a manner indicating that they are in fact different states of the same defect. This finding strongly supports the existence of metastable defects which convert from a deep donor to a shallow acceptor upon minority carrier injection [63]. This mechanism also explains the observed persistent photoconductivity. Further support for this mechanism comes from density functional theory calculation of Lany and Zunger, which predicted that the V_{Se}-V_{Cu} defect is a metastable defect with the expected properties to explain many of the observed metastable effects [65]. The predictions of this defect seem to match very well with the observations of the red light effect and persistent photoconductivity in CIGS, and also explain the effect of the reverse bias metastability.

The blue light effect is caused by absorption of light in the buffer layer, so it was originally proposed that the reason for the metastable behaviour was photodoping of the CdS buffer layer. In this mechanism the compensation of the buffer layer is reduced when photo-generated holes are captured by deep acceptor states. This increase in the effective n-type doping of the buffer reduces the barrier caused by the absorber buffer conduction band offset. Figure 3-6 shows a schematic of the band diagrams and the resulting I-V curve for this mechanism. The blue light effect has also been observed in alternative buffer layers [53], which casts doubt on the buffer photodoping model. It is also possible that photodoping is a general feature of many buffer layers [66]. An alternative explanation is that the changes are occurring in the absorber layer in a region close to the junction with the buffer and that the changes are caused by photo-generated holes from the buffer migrating back into the absorber. Niemegeers et al proposed a model where the surface of the absorber consists of wider bandgap ordered defect complex (ODC) with a high concentration of deep acceptors (p+ layer), a low mobility and donor defects at its interface with the buffer layer [62]. The interface donors pin the Fermi level at the interface, while the combination of the potential drop due to the deep acceptors and the low mobility create a barrier for diode current. The band diagram and I-V curves of this process are also shown in Figure 3-6.

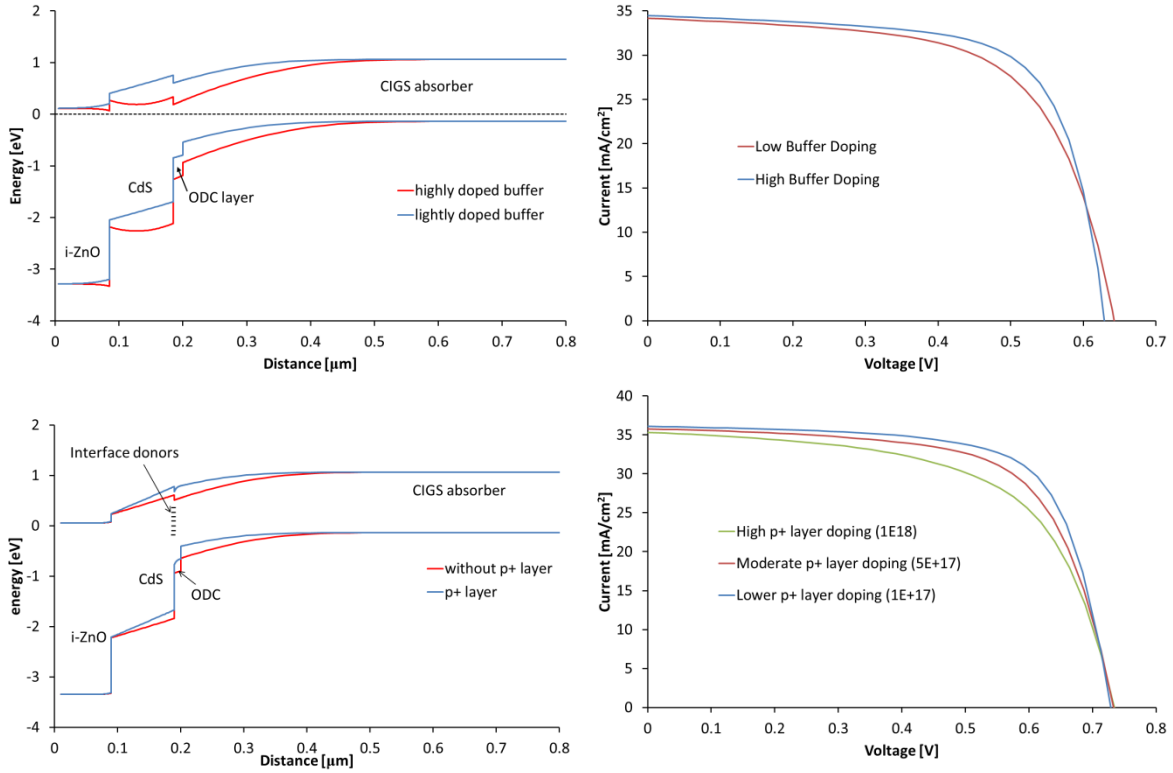


Figure 3-6: Band diagrams of models for the blue light effect. a) photodoping of the buffer layer. b) reduction of a p+ layer in the absorber

Both of the models also explain the crossover of light and dark I-V curves. An alternative p+ layer could be caused by metastable defects, which exist in an acceptor state close to the junction. In particular the In_{Cu}-$2V_{Cu}$ defect is a strong candidate, since from theoretical calculation it is also expected to be metastable and should take an acceptor state when the Fermi level is close to the conduction band but convert to a deep neutral DX state upon capture of holes, with no activation energy for the hole capture process [67].

Copper has been shown to be relatively mobile in CIGS and could be another cause of metastable behaviour since changes of the electric field caused by biasing could cause reversible migration of the copper [60,68].

The previous observations of preconditioning and theories for its origin discussed in this section set the picture for the work which will be presented in chapter 5, where experimental quantification of preconditioning in a variety of CIGS devices is performed. In chapter 6 the possible origins of preconditioning in CIGS will be discussed in more detail and a theoretical rate models for the process will be compared to the experimental results of chapter 5.

4 Capacitance

4.1 Introduction

The internal capacitance of photovoltaic cells can cause significant problems for performance measurement of PV devices, but it also a presents a convenient way to probe several internal device parameters using non-destructive measurements. A variety of capacitance spectroscopy techniques are routinely used for this purpose on PV cells but there are few examples of these methods being used on modules. In this chapter a module scale C-V measurement system is developed and utilised in a novel method to optimise performance measurements of PV modules, conducting them in the fastest possible time without introducing errors from capacitive charging / discharging. This method allows the measurement of high capacitance PV modules within a 10ms illumination pulse and with a simple and automatic sweep optimisation process which can be made individually for each separate module and has strong potential as a production line tool. The measurement system is then also used to probe some of the internal parameters of the device such as doping density and minority carrier lifetime. Again on a production line this extra information could be useful in order to track the origin of unintentional changes in an individual batch or drift over time. A unique aspect of the measurement system is that it is also capable of applying electrical bias preconditioning and measuring light and dark I-V curves, abilities which are exploited further in subsequent chapters to investigate preconditioning in CIGS modules.

4.2 Module impedance and I-V measurement system

4.2.1 Measurement system setup

Figure 4-1 show a schematic diagram of the impedance and IV measurement system. Power is supplied by 2 KEPCO BOP 50V-8A power amplifiers connected in series using a master-slave configuration. The 100V 8A range achieved is sufficient for most photovoltaic modules, if more voltage is required further BOP units can be connected, this was used for example to measure the solar frontier SF150 module which has a STC V_{oc} of 110V. The voltage is measured across a potential divider in parallel with the module consisting of 22kΩ and 1kΩ resistors.

The current through the module is measured using the voltage across a 0.1Ω resistor in series with the module, and making a small correction for the current that travels through the voltage measurement resistors. All the resistors used are thick film, low

inductance type. The voltages are monitored using a national instruments PCI-6120 DAQ card with an 800kHz sample rate, acquired simultaneously over all the channels. This is more than sufficient for the maximum measurement frequency of 24kHz which is set by the bandwidth of the BOP units.

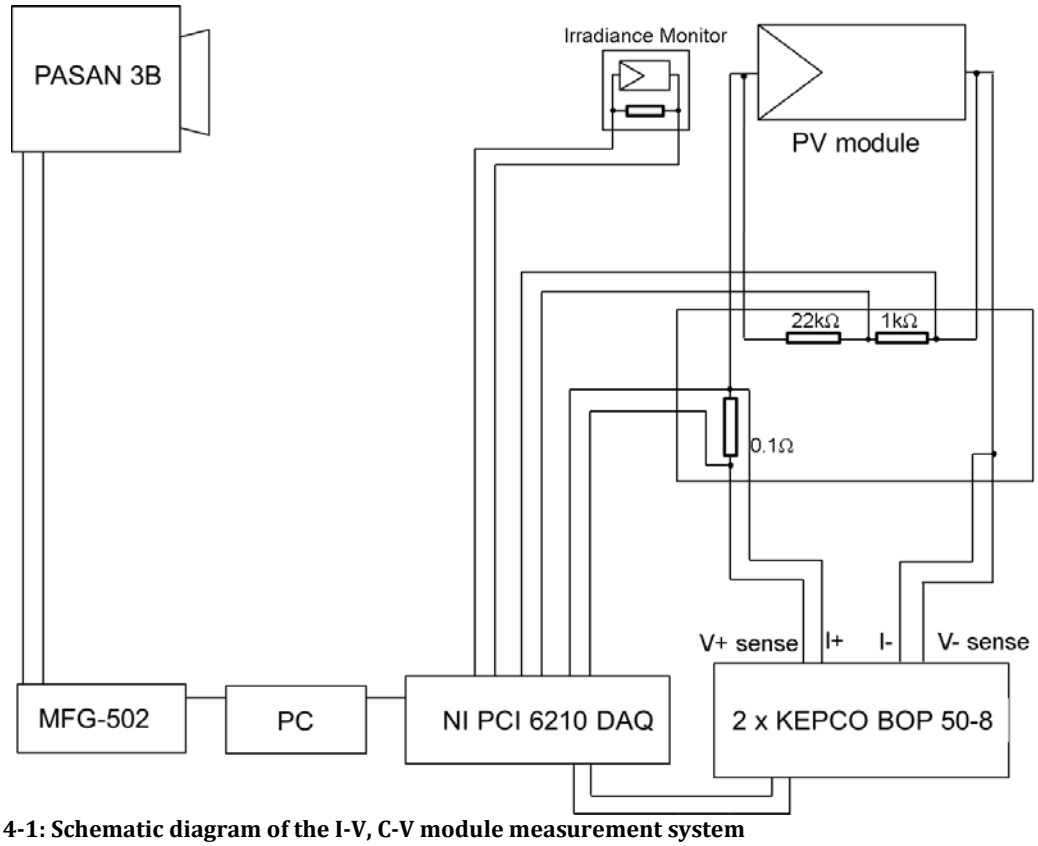


Figure 4-1: Schematic diagram of the I-V, C-V module measurement system

The voltage and current measurements were calibrated using a Fluke 9100 calibrator in the place of the PV module to supply known currents and voltages to the system. In the case of the IV curve measurements, illumination is provided by a PASAN IIIB, AAA rated solar simulator, which provides a pulse of stabilised illumination 10ms in duration. The monitor cell can be used to trigger the KEPCO units to sweep an I-V curve during the illumination pulse. When connected to high capacitance modules it was found that the setup was not able to provide a sharp voltage step, which significantly extends the amount of time required for the current to settle at each measurement point. Instead the I-V measurements of high capacitance modules in this chapter were made using the standard PASAN IIIB load which has a quicker step response for high capacitance modules. However, the capability to use the same power supply/sink for the impedance measurements, I-V measurements and also preconditioning is a powerful tool and in the

later chapters of this thesis it is used for the purpose of preconditioning of CIGS modules.

4.2.2 Correction factors for the impedance measurements

The measurement system finds the impedance of the device under test from the equation Z=V/I, but the measurements of the current and voltage are made assuming that the shunt resistors are perfectly resistive and ignoring any parasitic capacitances or inductances in the system. In reality parasitic elements are present and this leads to phase changes in the voltage at different positions in the system, which can potentially lead to the measured voltage being significantly different to the actual voltage across the PV module. These effects become more important at higher frequencies, so it is important to determine at what frequencies they dominate, in order to understand the limitation of the system.

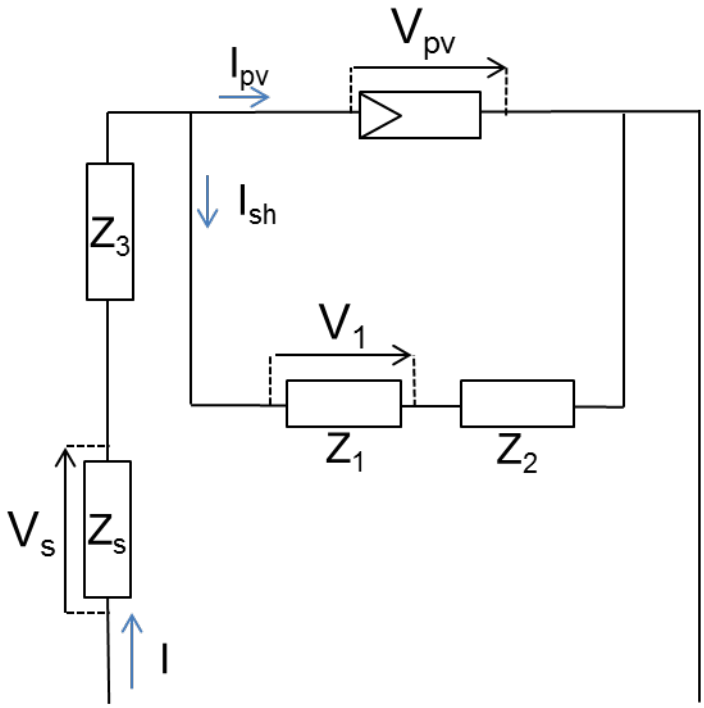


Figure 4-2: Circuit diagram of the measurement system with stray impedances

The circuit in Figure 4-2 accounts for those stray impedances which are expected to be the most important. These are reactive components for the shunt resistors, capacitance in the measurements cables in parallel with the shunt resistors and the impedance of the wiring to the module. The voltages V_1 and V_s are the voltages that are measured and the impedance of the PV module can be written in terms of them as

$$Z_{PV} = \frac{V_1}{Z_1}\frac{Z_1 + Z_2}{V_s/Z_s + V_1/Z_1} \quad \textbf{4.1}$$

Whereas the measured value of Z is given by

$$Z_{meas} = \frac{V_1}{R_1}\frac{R_1 + R_2}{V_s/R_s + V_1/R_1} \quad \textbf{4.2}$$

Dividing the two gives the factor between the measured and the actual impedance

$$\frac{Z_{PV}}{Z_{meas}} = \frac{R_1}{Z_1}\frac{Z_1 + Z_2}{R_1 + R_2}\frac{R_s}{Z_s}\left(1 + \frac{V_1\left(\frac{Z_s}{Z_1} - \frac{R_s}{R_1}\right)}{V_s + V_1 R_s/R_1}\right) \quad \textbf{4.3}$$

In the case where the impedance of the device under test is significantly lower than that of the parallel voltage measurement loop ($\approx 23k\Omega$), then the current through the parallel loop is negligible compared to the current through the device. In that case the term in the brackets of equation 4.3 is equal to 1 and there is a correction factor which is independent of the exact impedance of the device under test

$$Z_{PV} \approx T(f) Z_{meas} \quad \textbf{4.4}$$

Measuring this factor and applying it to the measured results helps to correct for the effect of stray parasitic elements, however for high impedance devices or for very high frequencies further correction terms are needed. At reverse bias (assuming no bypass diode is installed) or low forward bias voltages and low frequencies, PV modules do have high impedances comparable to the 23kΩ impedance of the parallel voltage measurement loop. In this case it is not possible to find a simple correction factor as in the previous case so care should be taken to make measurements in a suitable frequency range, where the error value is not too high for the application. While no longer acting as a good correction factor in the case of high impedance measurements, its magnitude still acts as a guide to the expected scale of the errors.

To find the correction factor T the measurements made on the system developed here were compared to those made using a Keysight E4990A impedance analyser. For this purpose a parallel connection of a 10nF capacitor and a 10Ω resistor was measured at frequencies from 20Hz to 24kHz, the results are shown in Figure 4-3.

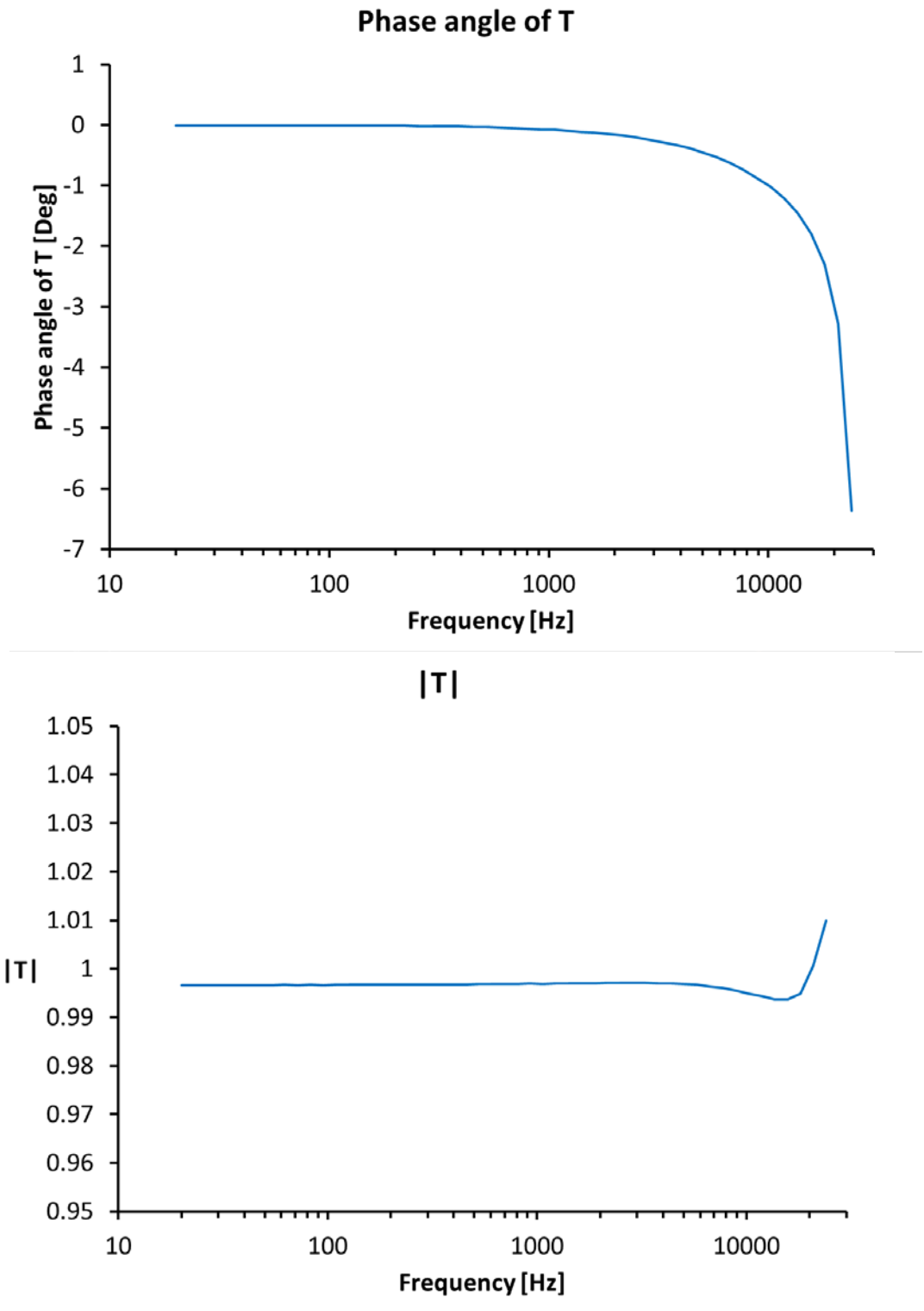


Figure 4-3: Measured value of the factor T which corrects for parasitic reactive elements in the measurement system.

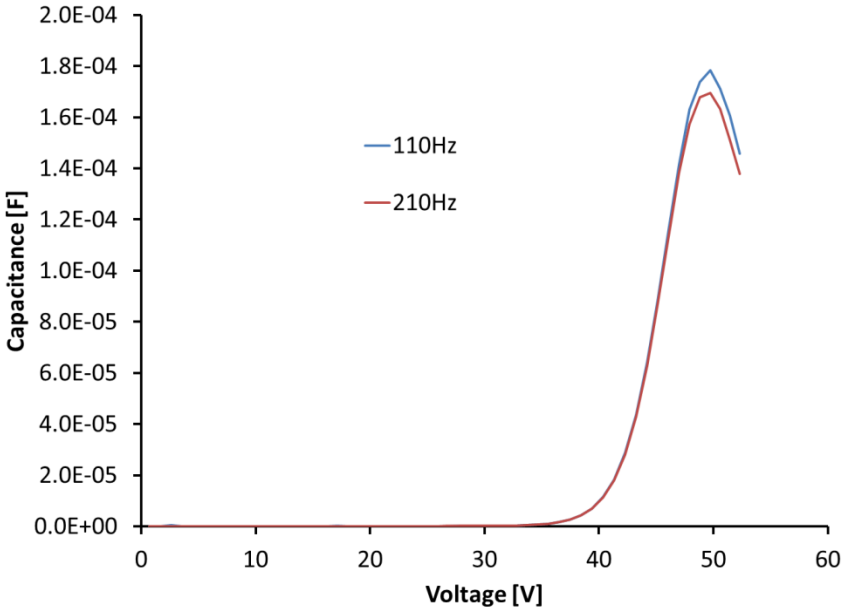
At frequencies below 1kHz there is no significant deviation between the measurements and the correction factor is virtually equal to 1. At higher frequencies the deviation starts to become apparent and increases rapidly to large values for frequencies above 10kHz. As a consequence of this analysis measurements were always performed at

frequencies below 10kHz and the correction factor was applied. This condition assures that the impact of stray impedances is negligible.

4.2.3 Module C-V measurements

In order to measure the capacitance of the module under forward bias it is necessary to measure the impedance at a least two different frequencies as discussed in chapter 2. There are different possible ways to do this. The most accurate is to make many measurements over the whole usable measurement frequency range and find the values of the equivalent circuit model components which best fit the measurement results. This method is known as impedance spectroscopy and is a powerful method which can also be applied to more complicated equivalent circuits, for example those of dye sensitised solar cells [69]. This method is accurate because of the degeneracy of the measurement and also provides confirmation of the validity of the circuit model, or warning of its failure. At the opposite end of the spectrum it is possible to extract the capacitance from just two impedance measurements at different frequencies, which is significantly faster but suffers in terms of accuracy. For C-V measurements, the capacitance is measured at many voltages so advantage can be taken of the fact that the value of R_s can usually be well approximated as independent of the voltage. The Z-V curve can be measured at two different frequencies and the value of R_s calculated as the value which makes the capacitance curves converge for the two different measurement frequencies, which improves the accuracy compared to calculating the capacitance at each voltage point separately, without sacrificing measurement speed. This method is used for the C-V measurements in this chapter: It is suitable for the well behaved Silicon modules measured, in other cases it might be advantageous to make measurements at more frequencies to improve measurement accuracy. Figure 4-4 shows an example for this process. Relatively low frequencies of 110Hz and 210Hz were used for the measurement. Because of the high capacitance of these modules a good signal can still be achieved at low frequencies, however the stray impedance effects are minimised. The series resistance is found as the value which causes the two curves to converge. In this particular case that value of Rs was 0.655Ω, the convergence of the curves is shown if Figure 4-4.

(a)



(b)

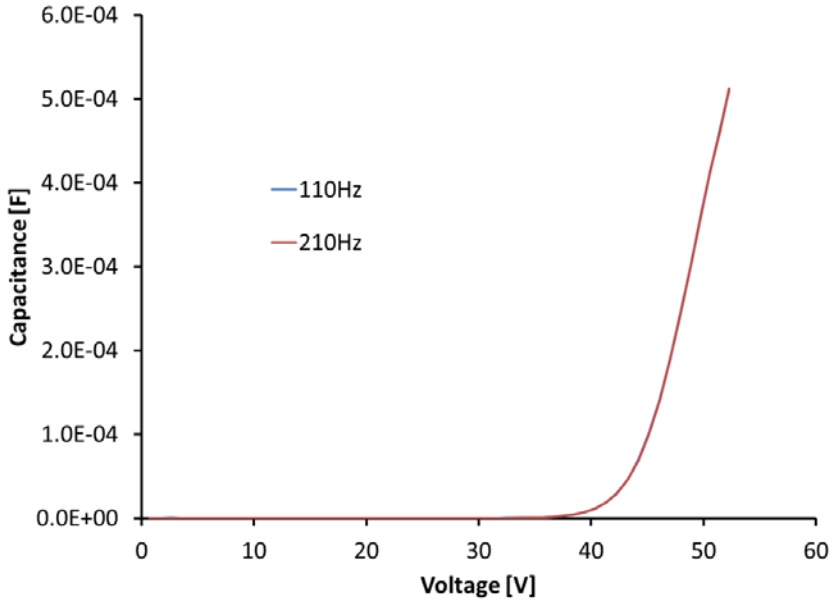


Figure 4-4: a) C-V measurement of an HIT module not accounting for the effects of the series resistance. b) Taking into account a series resistance of 0.655Ω causes the C-V measurements at the different frequencies to converge. The result gives a measurement of the C-V curve and the series resistance simultaneously.

4.2.4 Validation of the impedance measurement system

The impedance measurement system was validated in two ways. For voltages below 40V and currents below 100mA the measurements were compared to those made on the same Keysight E4990A impedance analyser as used in the previous section. For higher voltages or currents validation is more difficult as these exceed the E4990A's maximum ranges. Using a high capacitance module the current transient decay time after a voltage step was measured instead, and compared to the value calculated from the C-V measurements. The calculated value is obtained from the equations presented in subsection 4.3.3. These results can be seen in Figure 4-5. They show that at high

forward bias the calculated value is very sensitive to the measured series resistance. This sensitivity arises from the calculation of the C-V curve from the impedance measurements. The initial measured value of R_s from the C-V measurements was 0.7Ω however subsequent repeat measurements gave a value of 0.72Ω which gives much better agreement with the current transient results as seen in Figure 4-5.

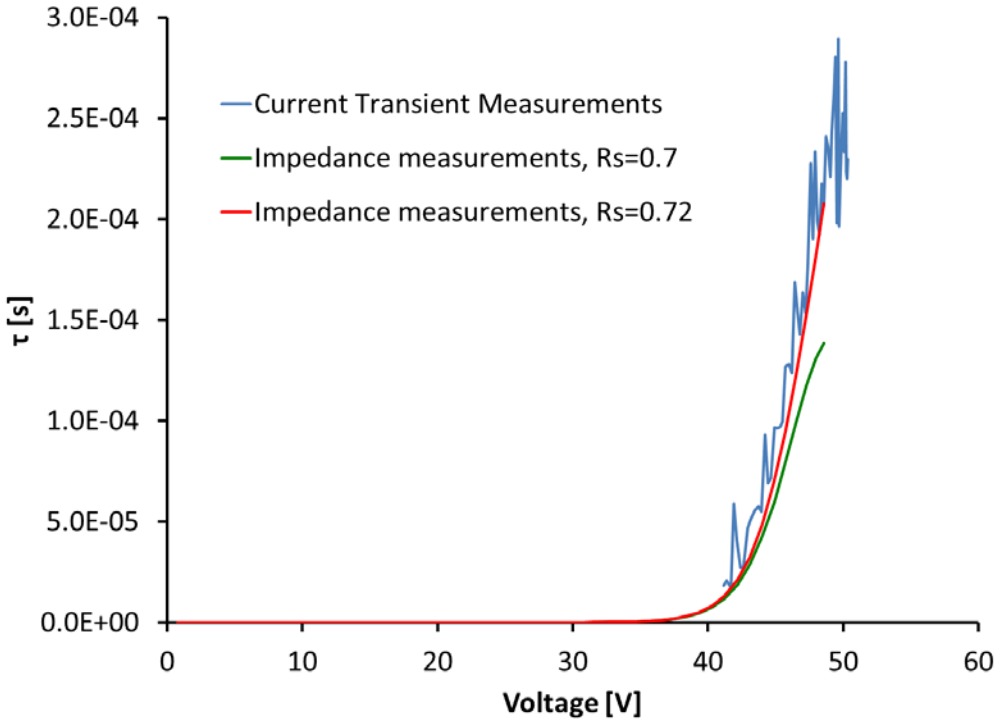


Figure 4-5: Comparison of lifetime curves measured using the current transient method verses impedance measurements. Two different curves are extracted from the same impedance data using different values of the series resistance, showing how the extracted lifetime is very senesitive to this value at high forward bias.

This result shows an important limitation for capacitance measurements of PV devices at high forward bias, that a relatively small error in the measured series resistance has much larger effect on the measured capacitance and the values calculated from it, in this case the current transient time constant. This error increases strongly with forward bias and probably precludes accurate capacitance measurements at and above the open circuit voltage using this technique.

4.2.5 Comparison of different module C-V characteristics

Figure 4-6 shows the measured capacitance for 6 different module types. The p-Si modules could be considered standard crystalline modules. As expected they have a much lower maximum capacitance than the other modules which are different varieties of high efficiency module. The results also show that the capacitance at low voltages is small but at voltages around half of the Voc it starts to increase exponentially. This

exponential increase in capacitance is due to the diffusion capacitance which starts to dominate over the junction capacitance at higher voltages.

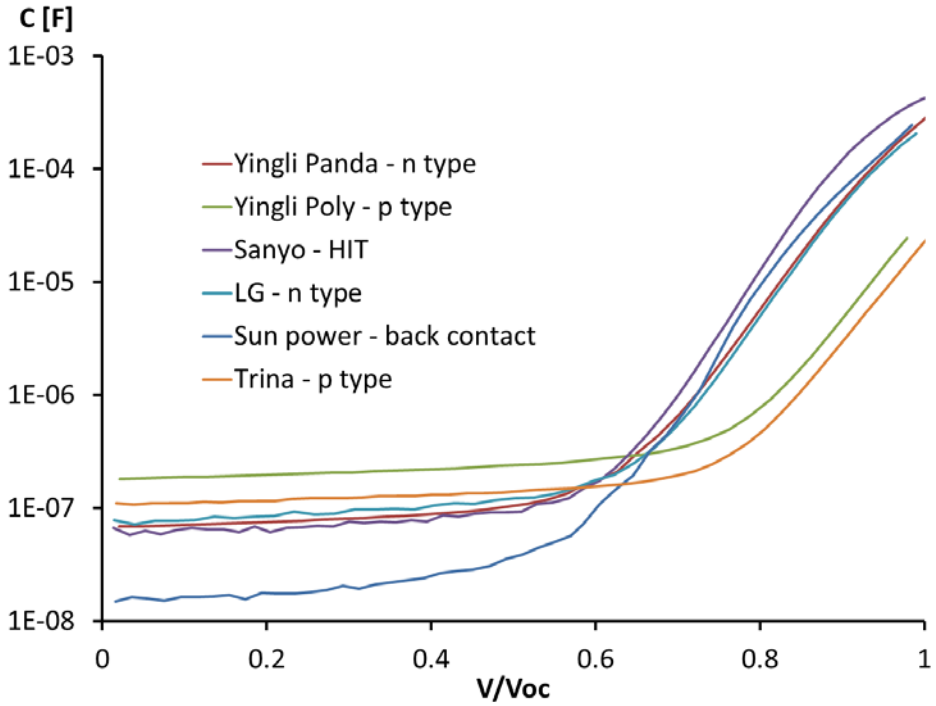


Figure 4-6: Measured C–V curves for a variety of different commercially available module types. The voltages are normalised to the open circuit voltage of the module.

An important factor in the capacitance of a module is the number of series connected cells and the size of those cells. The capacitance of a device scales linearly with the area of the cells and inversely with the number of cells. Modules with a smaller number of larger cells have a higher capacitance than modules with a larger number of smaller cells. Table 4-1 shows the capacitance per unit area per cell and the total capacitance per cell for each of the modules measured, with the capacitance measurements made at the STC Vmpp.

Table 4-1: Comparison of the capacitance at maximum power point for different modules.

module	C [µF]	Cell C [µF/cm^{-2}]	Cell area [cm^{-2}]	Number of cells
HIT (Sanyo)	18.4	8.58	154	72
BC (Sunpower)	20.6	10.1	147	72
n-type (LG)	3.94	0.99	238	60
n-type 2 (Yingli)	4.88	1.20	243	60
p-type 1 (Yingli)	0.82	0.20	243	60
p-type 2 (Trina)	0.59	0.27	156	72

It is interesting to note that the back contact module has a higher capacitance at the Vmpp point than the HIT module, even though from Figure 4-6 the capacitance of the HIT curve is generally higher. The reason for this is that the back contact module has a slightly higher fill factor so the maximum power point is slightly further to the right on the graph.

4.3 Tailored sweep design based on dark I-V and C-V measurements

4.3.1 Concept

C-V and dark I-V curves are measured for the module under test. Using an approximate expected value of the short circuit current, an estimation of the light I-V curve can also be made. From these characteristics the dynamic response after a step change in the voltage can be predicted. The estimated light I-V curves allows the measurement points to be concentrated in the areas of interest, and in addition the knowledge of the dynamic response is used to make sure that the voltage does not dwell unnecessarily at any measurement point. This results in significantly faster measurement times without compromising accuracy. The method predicts the size of the capacitive error and if necessary can split the measurement over multiple illumination pulses.

4.3.2 Review of existing performance measurement protocols

A variety of methods have been developed to deal with the measurement problem presented by high capacitance modules. The simplest methods make use of the fact that the size of the error is related to how quickly the voltage is ramped, so that reducing the voltage ramp rate reduces the error. This can be achieved using speciality long pulse simulators with a stabilised illumination of 100ms or more, or by splitting the measurement up into multiple sections or individual points which can be measured in separate illumination pulses, known as multi flash or multi point measurements [27,70-72].

Another simple solution is to only measure a small voltage range around the expected maximum power point voltage [73]. In this case only the maximum power point is measured and information about the rest of the IV curve is not gathered. In some situations this simple solution may well be the best, however there is useful information contained in the rest of the IV curve, particularly the short circuit current and open circuit voltage, and if the expected range of the maximum power voltage is too large the method could still struggle with capacitance artefacts.

It is possible to reduce the required measurement time by reducing the number of measurement points [29]. This becomes a trade-off with increased errors due to curve interpolation between measured points.

If the C-V characteristic of the module is known it can be used to model the maximum sweep rate, or alternatively the maximum number of measurement points possible for a given pulse duration and allowable measurement error. For individual cells, the capacitance is usually measured using admittance measurements, where an oscillating voltage is applied to the cell and the amplitude and phase of the current response is measured. This is technically possible also for modules and has been used for other purposes [36,74]. However, for the purpose of measuring the C-V curve to predict maximum sweep rates or design faster sweeps other methods are used, often citing the difficulty of direct measurement on modules due to the large currents and powers required [75]. These other methods include open circuit voltage decay [75,76] or extraction from the current decay after a voltage step, which has been referred to as the photocurrent response method [30]. Both of these methods are indirect ways to measure the capacitance. In the case of the photocurrent response method at least one illumination pulse is required to take the measurement, which is a big disadvantage if the method is used to individually measure the C-V characteristic of each module to be measured.

Once the C-V profile is known it can be used to calculate the minimum duration for the voltage ramp [29,30,76]. However in these methods the shape of the voltage ramp was kept constant, whereas in general the quickest measurement uses a non-linear voltage ramp because it is possible to sweep the voltage much faster through certain ranges than others. Two published methods using non-linear voltage ramps for this purpose are the dynamic I-V® [77] and Dragonback® [78].

In the Dragonback method the required measurement voltage can be overshot briefly at each step to increase the capacitive charging / discharging rate then reduced back to the required measurement voltage for the actual measurement. In this way the time taken for the current to stabilise at each set voltage measurement point is reduced. The disadvantage is that voltage profile of this method is relatively time consuming and complicated to set up, and only applicable to modules with very similar characteristics. On a production line it can be very useful if the modules being produced are of adequate

consistency, but could be problematic if the consistency is not high. It is also less useful for test houses where a smaller number of many different module types are measured.

The dynamic I-V method measures the C-V of the module from the time response of the current after a voltage step while under illumination. The necessary settling time for each voltage point is then calculated. To additionally reduce measurement time, the density of voltage measurement points is lowered outside the regions of main interest, namely around the short-circuit, open-circuit and maximum power points. The main disadvantage of the dynamic I-V method is that an additional illumination pulse is required to measure the C-V profile before the optimised I-V measurement can be made.

The error in the measured power of the module is often quoted to assess the effect of capacitance on the measurement, which is an intuitive, obvious choice. However when the whole IV curve is measured then sometimes a way is needed to compare the error at different points along the curve. The error in the current at a specific voltage is not a good measure because at higher voltages where the gradient of the I-V curve is steeper a larger error is less important. In refs [75,76] the error measure used was the distance between points of the same load resistance on the I-V curve normalised to the V_{oc} and I_{sc} values.

4.3.3 Estimating the light I-V

Estimating the light I-V from the dark I-V and the short circuit current is in principle very simple and has even been proposed as an alternative to measuring the I-V curve at all [78]. In order to make this estimation modelling approximations have to be made which reduces the confidence in this method for performance measurements in its own right. However, the method proves sufficiently accurate for the purpose of designing optimised voltage ramps and in the unusual cases where approximation is so poor that the I-V measurement also fails then this will be clear from the measurement result so the problem can be flagged up.

The equation for the current in the light (I_L) from the current in the dark (I_d) is simply

$$I_L = I_d - I_{sc} \tag{4.5}$$

But the voltage must also be transformed according to

4.6

$$V_L = V_d - R_s I_{sc}$$

This transformation can be seen from considering the diagram Figure 4-7. The series resistance and the short circuit current are necessary to perform this transformation.

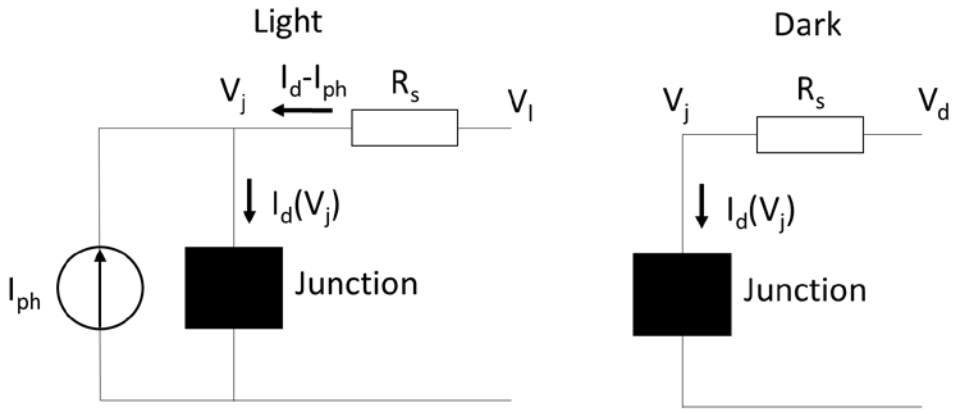


Figure 4-7: Schematic to illustrate how to transform the dark I-V curve to the light I-V curve. At any particular junction voltage the curent in the light case reduces by a contant equal to the photocurrent, and the external voltage also changes due to the change in current across the series resistance. The exact detail of the black box for the junction is not important, it could be a one diode model, two diode model or any other function, the only important point is that it is not illumination dependant.

The series resistance is calculated from the impedance measurements, while the short circuit current is taken as a user input. In the experimental work here the datasheet value for the module was used, on a production line the line average could be used instead. For outlier modules this introduces a large very error into the I-V curve approximation. This large error is usually tolerable however, because the corresponding error in Voc and Vmpp is much smaller than the error in Isc. So for the purpose of setting the region of interest, for increased density of measurement points, it is still possible to successfully put a reasonably tight range around the Vmpp and Voc. An alternative option is to have a separate illumination pulse to measure this value. This method was not chosen in this case because it is a big advantage to be able to make the measurement using only one illumination pulse. However, for some circumstances it might be necessary to implement an initial pulse to obtain a better estimate of the Isc. This might be the case for example if there is a large spread in the Isc values from the production line. In this case the extra pulse does not need to be up to the same high specifications as the pulse used for the actual performance measurement which would save on implementation cost. The pulse could be of much lower intensity than the STC and use the linearity of the short circuit response. It could also be very short compared to the I-V measurement pulse because the voltage does not have to be swept over a

range and the capacitance of the module is orders of magnitude less at the short circuit than maximum power point. Finally, since only a reasonable approximation of the Isc is needed at this stage, the spectrum of the initial pulse does not need to be well matched to the AM1.5 spectrum.

4.3.4 Modelling a small voltage step

The equivalent circuit Figure 4-8 for small oscillations was introduced previously in chapter 3. This equivalent circuit can be used also to model the response of the system to a small voltage step provided the changes in the circuit parameters are small over the voltage range of the step.

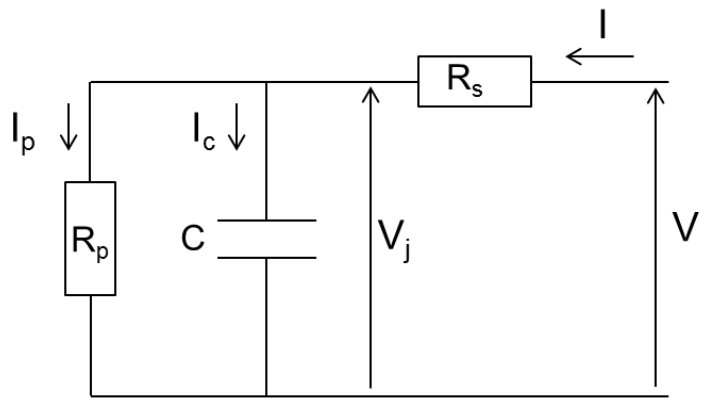


Figure 4-8: equivalent circuit model of a photovoltaic device for small oscillations and small voltage steps

In the following equations all the specified voltages and currents and charges are the differential values from the initial value before the step, however the δ's have been omitted for notational convenience. The junction voltage is given by

$$V_j = V - IR_s \tag{4.7}$$

The total current is the sum of the capacitive charging and the diode current

$$I = I_p + I_c \tag{4.8}$$

The capacitive charging current is given by

$$I_c = C\frac{dV_j}{dt} = C\left(\frac{dV}{dt} - R_s\frac{dI}{dt}\right) \tag{4.9}$$

After the initial voltage step dV/dt=0, using this along with the equations above gives a differential equation for the current in terms of the externally applied voltage.

$$I = -CR_s\frac{dI}{dt} + \frac{V - IR_s}{R_p} \quad \textbf{4.10}$$

Solving this equation using the initial condition that the stored charge is initially 0 and therefore $V_j(t = 0) = 0$ gives

$$I = Aexp\left(-\frac{t}{\tau}\right) + I_{fin} \quad \textbf{4.11}$$

Where the pre-exponential factor is given by

$$A = \frac{VR_p}{R_s(R_s + R_p)} \quad \textbf{4.12}$$

The decay time constant is given by

$$\tau = \frac{CR_s}{1 + R_s/R_p} \quad \textbf{4.13}$$

And finally I_{fin} is the increase in the final settled current.

$$I_{fin} = \frac{V}{R_s + R_p} \quad \textbf{4.14}$$

The values of C, R_s and R_p can be found from the impedance measurements and used to calculate the settling time for each voltage step for a given maximum error in the current. The circuit parameters measured using impedance spectroscopy in the dark are a function of the voltage from that dark measurement. They require converting to a function of the voltage when under illumination. The difference is due to the reversal of the current across R_s in the two instances. In order to make this conversion the estimation of the light I-V curve is used.

In measurements of capacitive modules it is generally observed that the error is high around the maximum power point but lower around the open circuit voltage, even though the capacitance of the module is increasing exponentially with voltage and is much higher at the open circuit than at the maximum power point. Part of the reason for this is explained by the presence of the factor of R_p in equations 4.12 and 4.13. R_p decreases significantly at higher voltages so the initial size of current transient (the factor A from equation 4.12) also decreases significantly.

It should be noted that these equations are not valid in the case of too fast a measurement where one voltage step starts before the current has settled from the previous step. The non-linear terms that enter the equation when this happens can cause a very pronounced hump in the I-V curves made with decreasing voltage.

4.3.5 Error between I-V curves

In the previous section it was discussed how the increased slope of the I-V curve reduces the initial current in the transient after a small voltage step, which contributes towards the lower error in I-V measurements close to Voc compared to Vmpp. The increasing slope also contributes to the lower error at Voc in another way. The error in the current around the open circuit voltage appears instead as much smaller error in the measured voltage because of the steep slope. The error in the current does not reflect this intuitive view, and is not an appropriate error measure for all points on the IV curve. Hence it is argued here that a more appropriate error measure is needed for the purpose of comparing the IV curves.

One method mentioned previously in the review of existing methods is to use the distance between the measured and actual normalised IV curves along lines of equal load resistance [75]. The method used in this work instead finds the distance between the normalised curves along the direction perpendicular to the IV curve. This definition is simple and intuitive, and for the case where the error is small there is a simple relation between the error in the current and the newly defined error ϵ, as depicted in Figure 4-9.

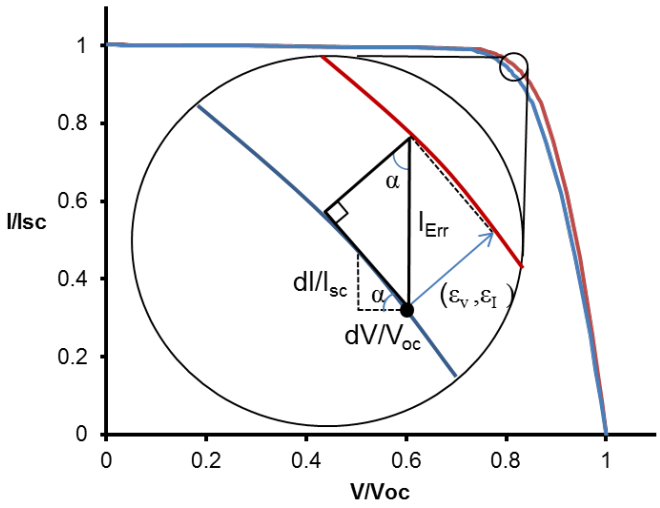


Figure 4-9: Definition of error between two IV curves

An approximation to the error can be made using the values already calculated to give.

$$\epsilon_i = \frac{I_{err,i}}{B_i} \quad \textbf{4.15}$$

where $B_i = \sqrt{\left(\frac{dI}{dV}\right)_i^2 \left(\frac{V_{oc}}{I_{sc}}\right)^2 + 1}$. If a different definition of the error were used then equation 4.15 is still valid but with a different value B_i, for example in the simple case of using purely the current error then $B_i = 1$.

Using this definition the error for each point can be set equal to a constant λ, and using equation 4.11 the settling times are given by

$$t_i = \tau_i \ln(A_i/\lambda B_i) \quad \textbf{4.16}$$

To find how to set λ the sum of all the time steps is set equal to the total available measurement time T, which yields.

$$\lambda = \exp\left(\frac{\sum \tau_i \ln(A_i/B_i) - T}{\sum \tau_i}\right) \quad \textbf{4.17}$$

The settling time for each step is automatically adjusted to make the error the same for each step. The sweep is faster at lower voltages where the capacitance is lower, and slower around the maximum power point where the capacitance is higher.

The sweep can then be optimised even further, since the voltage measurement points can be chosen and since the sweep is faster if the voltage points are more spaced out. So the measurement points are chosen to be closely spaced only in the regions of interest around the short circuit, maximum power point and open circuit, and in other regions a coarser spacing is used. To do this the estimation of the maximum power point voltage and open circuit voltage from the dark I-V measurements are used.

Once the points have been set and λ has been calculated it is possible to calculate an estimate of the capacitive charging error. If this estimated error is larger than a predefined acceptable threshold then either the number of measurement points can be reduced or the measurement can be split into 2 (or more) pulses.

4.3.6 Results of the tailored sweep design

In this subsection a high efficiency back contact type module is used to demonstrate the steps in the tailored sweep design as depicted in Figure 4-10.

The first step is to measure the Z-V of the module at two different frequencies, and use these measurements to extract the C-V profile and series resistance, as described in 4.2.3.

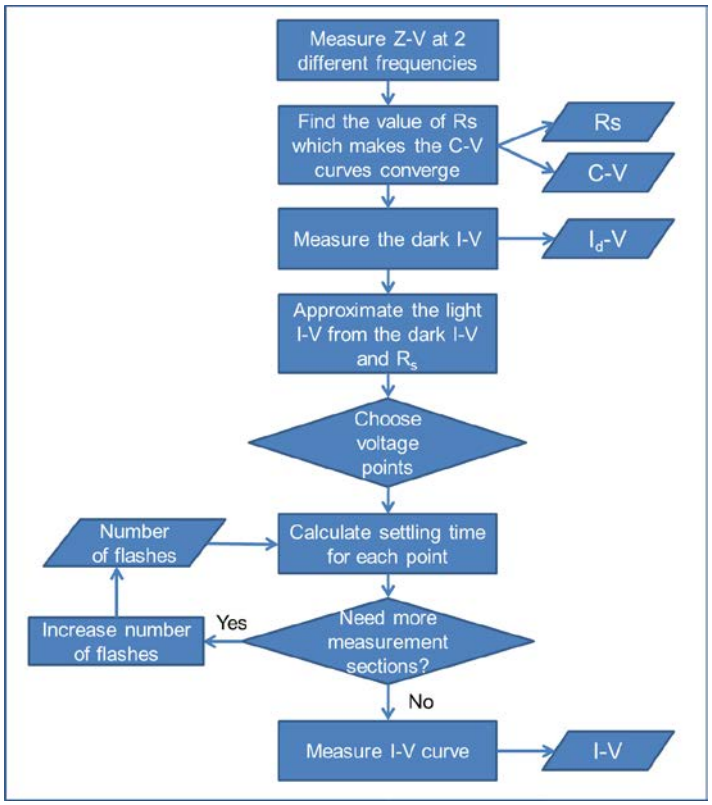


Figure 4-10: Flow diagram for the tailored sweep design process

The dark I-V is now combined with the measured value of Rs and an estimate of the short circuit current to create an estimate of the light I-V curves as show in Figure 4-11. In the figure, two different light I-V curve estimates are shown where the I_{sc} values used are either the datasheet value or the value measured under illumination. The I-V curve as measured in the light is also shown for comparison. In this case there is a 2.8% difference between the datasheet and measured values of $I_{sc,}$ which obviously propagates to the estimated curves. In the case of using the measured I_{sc} value, a much better match to the measured I-V curve overall is achieved. However, a small discrepancy remains due to a slightly higher apparent shunt conductance in the illuminated rather than dark I-V. This example serves as a good demonstration of why it is important to make an actual measurement of the light I-V curve for final performance assessment, rather than trying to reconstruct it from the dark I-V curve and a measured Isc. The remainder of the analysis in this example continues using the curve estimated from the datasheet value to show that the method works even in this case.

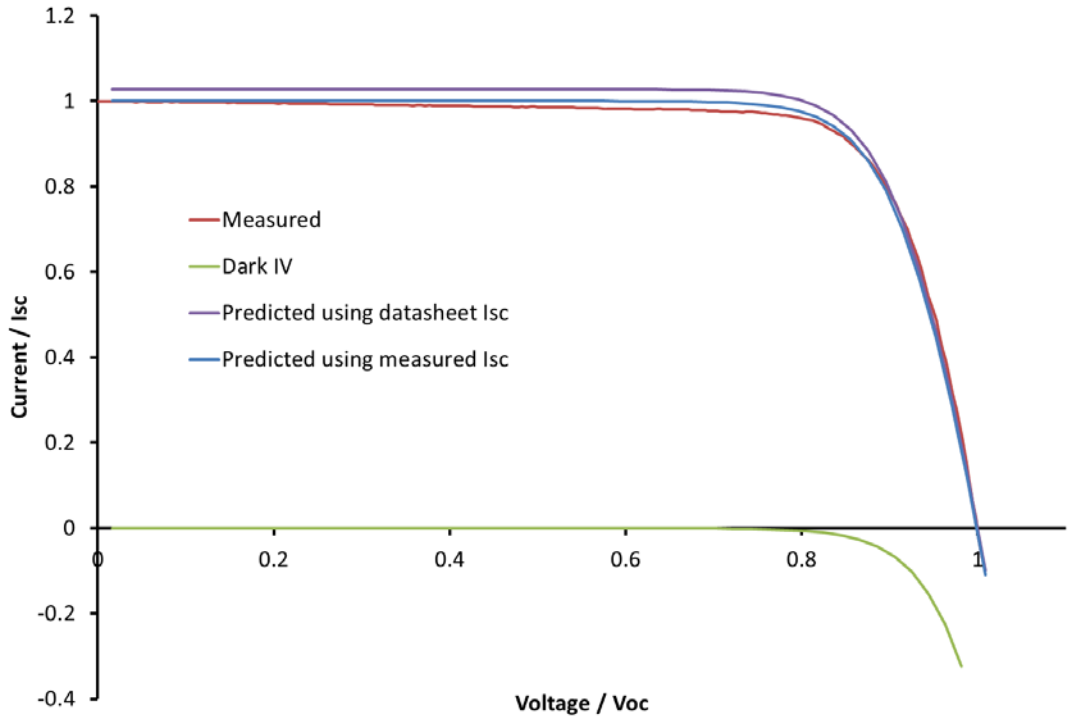


Figure 4-11: Example of light I-V curve estimation from the measured dark I-V curve. Two estimates are shown using different values of the Isc for the estimation. One using the datasheet value of I_{sc}, and the other using the measured value of I_{sc}. The actual measured I-V curve of the device is also shown for comparison and validation of the estimation technique.

The modelled I-V curve is used to extract an estimate for the Vmpp and Voc for the module. These estimates are then used in the next step to decide on the voltage measurement points, as shown in Figure 4-12.

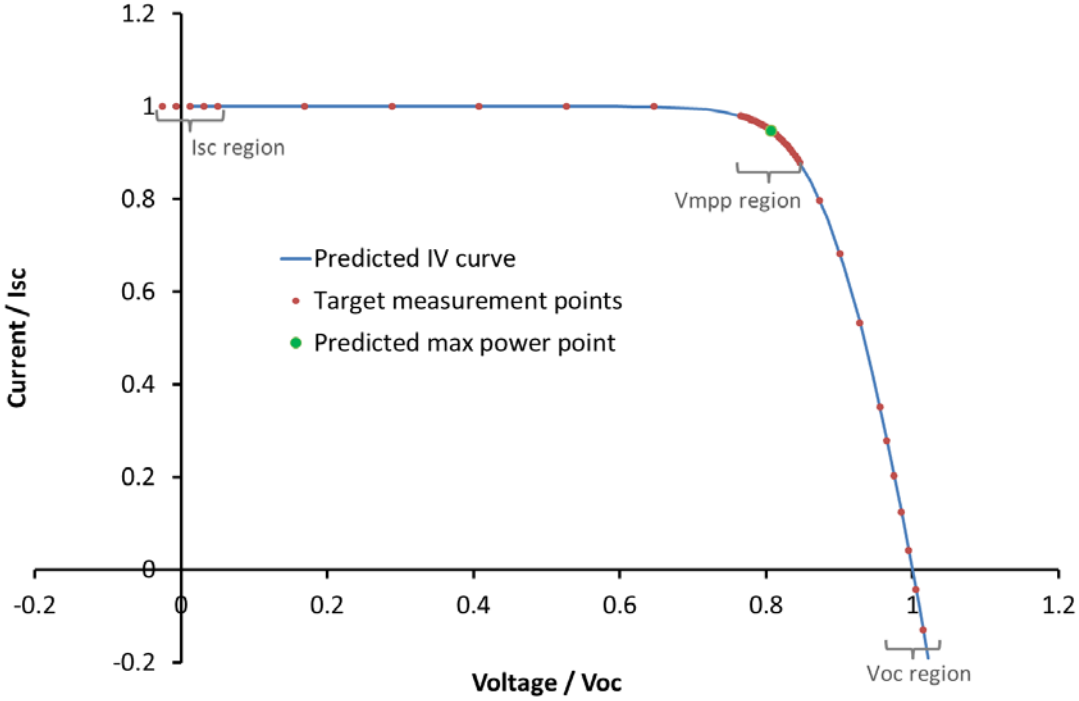


Figure 4-12: Distribution of the I-V curve measurement points

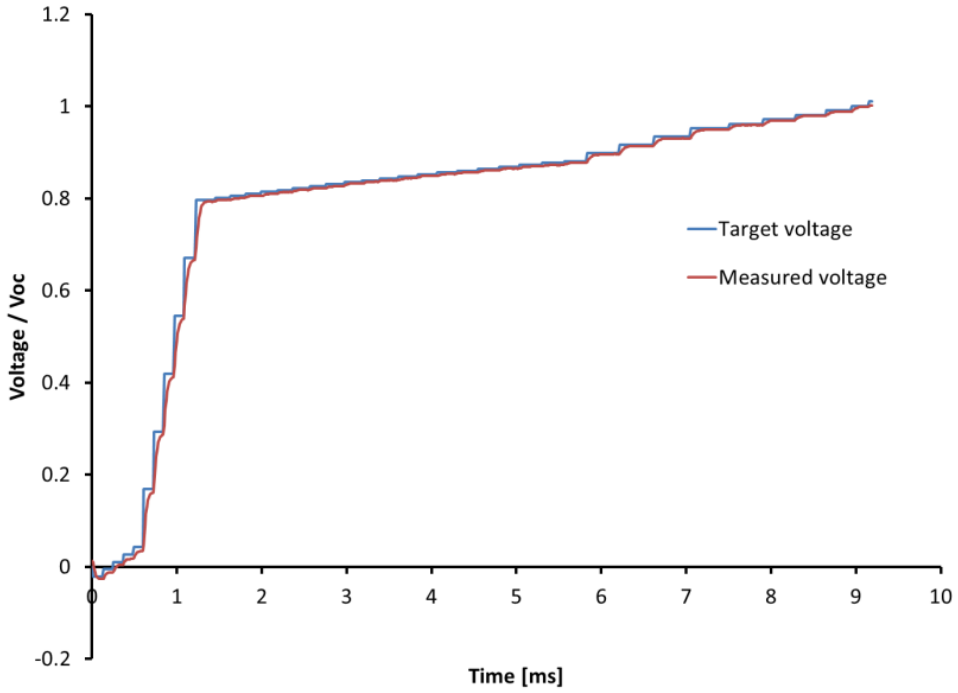
4 measurement points were used around Isc, from -1V to 2V. For the maximum power point section the highest density of points was used, 20 measurement points were spaced in the region within ±5% of the predicted Vmpp, which gives 0.2 V between each measurement point. 8 measurement points were used to connect the Isc and MPP measurement sections. For the Voc section 6 measurement points were spaced in the region within ±3% of the predicted value, and finally 4 points were spaced to connect the MPP and OC measurement sections.

Some of the voltage supplied by the I-V tracer is dropped over series resistances before the module so that the voltage set point of the tracer unit needs to be adjusted in order to achieve the correct voltage at the module. The series resistance in the system up to the module connection was measured as 0.2Ω. The voltage drop over this resistance is estimated using the current from the predicted I-V curve.

Now that the voltage points are set, the settling time for each point is calculated as per equation 4.11-4.13, 4.15-4.17. The total time used for measurement during one pulse of the simulator is 9.2ms, however for each step there needs to be also a constant time which allows the voltage to settle (120μs). The total voltage settling time is subtracted from the total sweep time to find the settling time available to be shared between the points. The calculated voltage sweep profile is shown in Figure 4-13, along with the actual measured voltage sweep. In the measured voltage profile the settling time of the step can be seen as a rounding of the step corners.

In the final step the I-V curve is measured. The current as a function of time during the illumination pulse is shown in Figure 4-13, it can be seen how each time the voltage is changed it causes a large spike in the current which then decays back to the steady state value. Figure 4-14 shows a comparison of the resulting I-V curve with different curves made using linear voltage ramps. For a fair comparison, I-V curves with the same point density around the maximum power point are compared. For the tailored sweep design method there are 5 points per volt in this region, which for a linear voltage ramp translates to 241 points in the full sweep range. When measured using a linear voltage ramp in sections over 10 separate flashes the forward and reverse sweep I-V curves converge, so the capacitance is no longer affecting these measurements and these measurements can be considered as the true IV curve for the purpose of comparison.

(a)



(b)

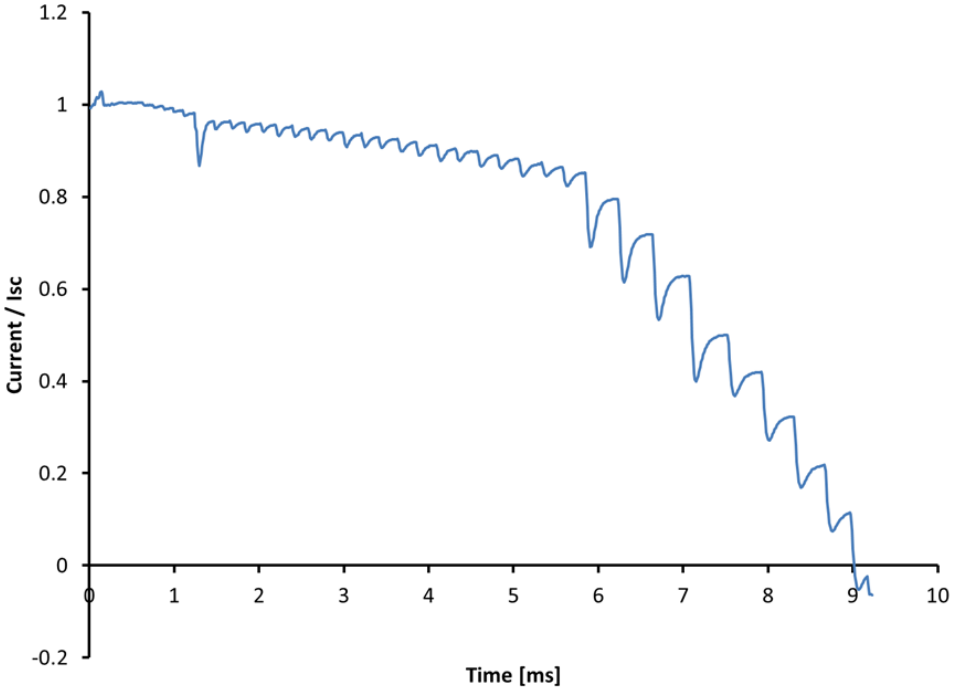


Figure 4-13: (a) Target and actual output voltage profiles. (b) Measured current during the voltage ramp.

The tailored sweep design I-V curve matches closely to the 10 section measurements with measured maximum powers of 206.5W and 206.9W respectively. The difference between these measurements is only 0.2%, which is also in excellent agreement with the predicted error due to capacitive charging. In Figure 4-14 the measurements using a linear voltage ramp over a single pulse are shown for comparison. They give very poor results and show just how much of an improvement the tailored sweep design is.

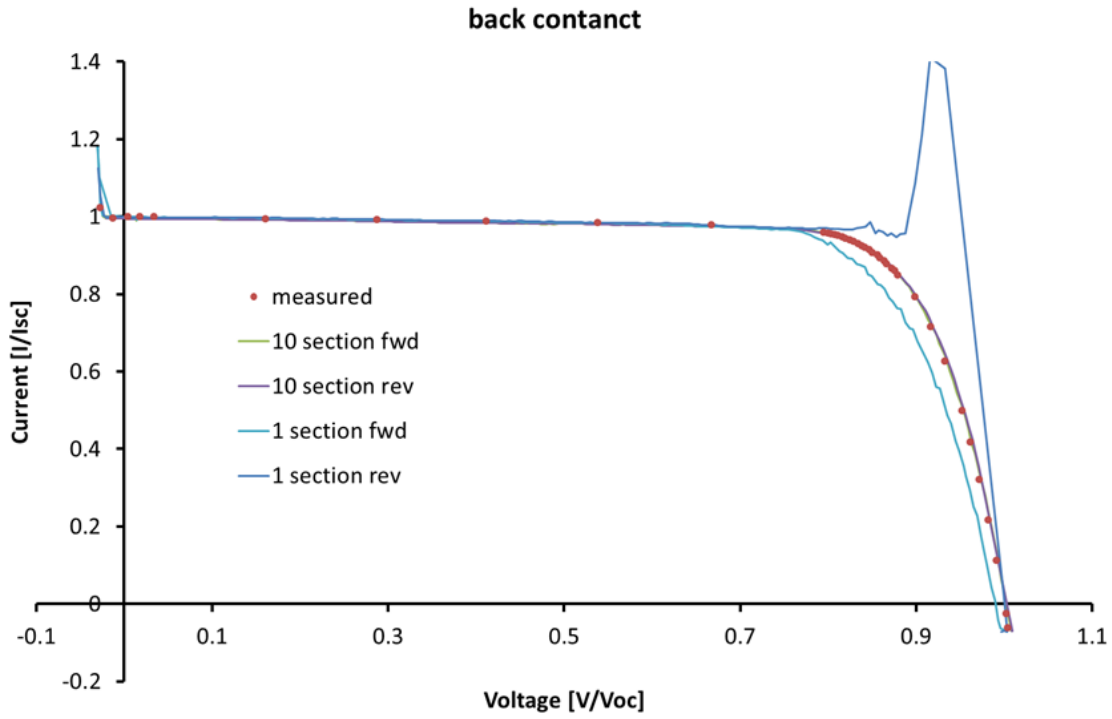


Figure 4-14: Comparison of I-V curves measured using tailored sweep design and linear voltage ramps over single and multiple pulses in different sweep directions

If the estimated error from making the measurement in one sweep is too high then multiple pulses can be used, or the number of measurement points can be reduced. This was the case for a different example of measuring an HIT module, where the estimated capacitance induced error in the maximum power point from using a one pulse was 2.3%, but when increased to 2 sections it became 0.24%. The resultant I-V curves for the HIT module as well as 2 n type modules can be seen in Figure 4-15.

4.3.7 Comparison of measurement protocols

Several high capacitance modules have been measured using the high capacitance sweep design method, and also the traditional split flash linear voltage ramp method. Table 4-2 summarises the results.

Table 4-2: Comparison of IV measurement methods for different modules

	Num sections		Pmax [W]		Voc		Isc	
	linear	tailored	tailored	% diff	tailored	% diff	tailored	% diff
HIT (Sanyo)	12	2	210.7	0.38	50.8	0.03	5.5	0.13
BC (Sun Power)	10	1	206.5	0.25	47.4	0.27	5.62	0.55
N type 1 (LG)	8	1	277.4	0.39	39.2	0.07	9.4	0.16
N type 2 (Yingli)	6	1	253.8	0.02	37.9	0.01	9.07	0.25

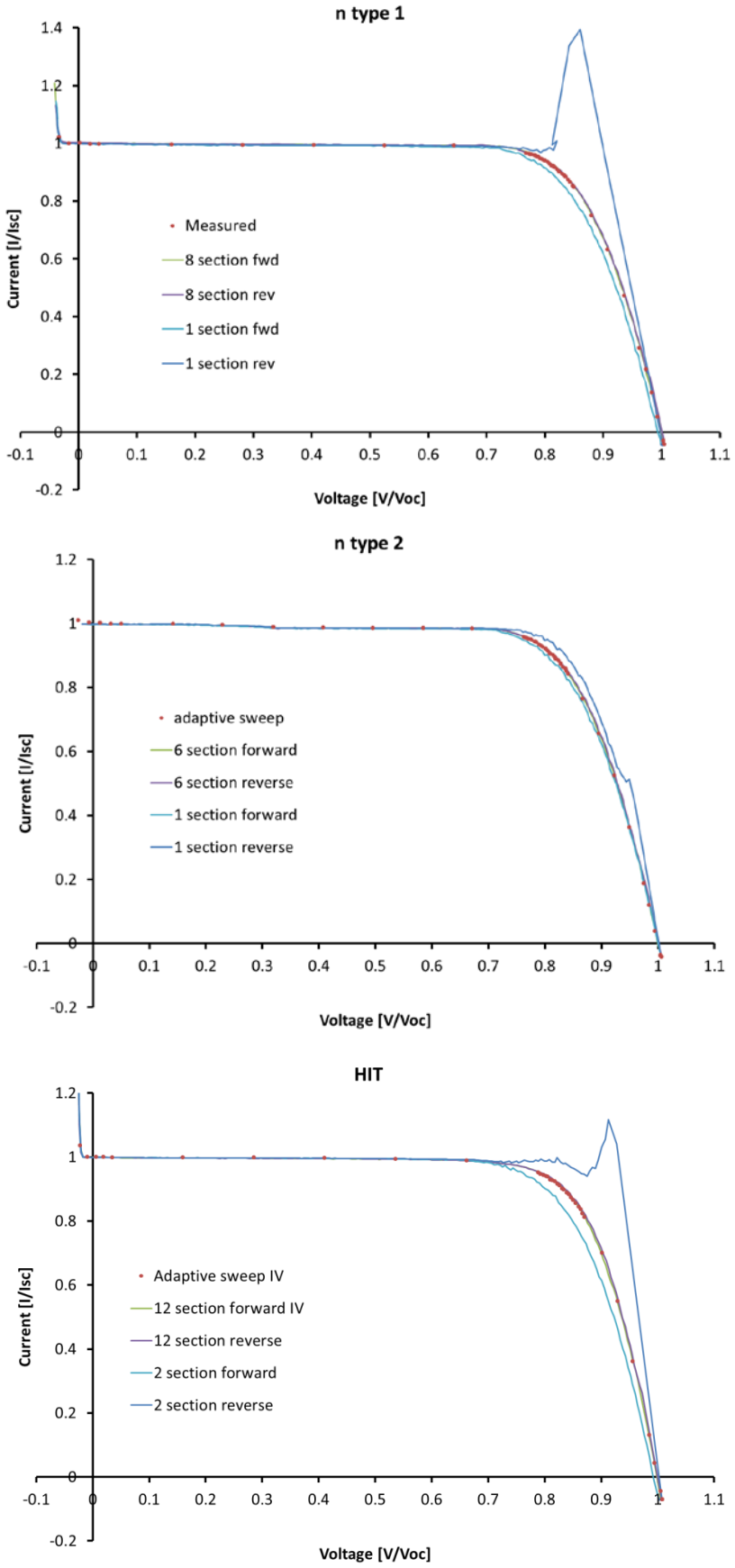


Figure 4-15: Measured I-V curves for different modules using linear voltage ramps Vs tailored voltage ramps.

4.4 Extracting device information

As discussed in section 4.2, a great deal of interesting information can be extracted from capacitance measurements. In particular, the system developed for module measurements is capable of extracting information about carrier density and carrier lifetime.

4.4.1 Carrier density

The carrier concentration can be extracted from the measurements of the C-V profile in the reverse bias and low forward bias regime. From differentiating equation 3.5

$$N_{CV} = \frac{2}{q\varepsilon\varepsilon_0 A^2}\left[\frac{d(C^{-2})}{dV}\right]^{-1} \quad \textbf{4.18}$$

Normally the area and permittivity of the material are known, so that the doping density can be found from the gradient of the plot of C^{-2} Vs V, known as a Mott-Schottky plot. Additionally, the built-in voltage can be obtained from the intercept of the plot. Most modules contain bypass diodes designed to prevent the cells being damaged by reverse bias in operation. The bypass diode prevents the reverse bias regime being used for the measurement, but the parameters can still be extracted from the low forward bias voltage regime.

In the usual case, a module consists of a series connection of multiple cells. In analysing the C-V curve for modules it is assumed that all the cells have equivalent electrical properties, however in reality this will not be the case. This means that each cell has a different operating voltage and the measured capacitance is a rough average of the capacitance of each cell, at the operating voltage that the particular cell is at. If some cells are very badly mismatched then this could have a significant effect on the result.

Additionally, care needs to the taken over which technologies the technique can be applied to. For example in the case of textured solar cells the area of the junction is higher than the projected area of the cell. The area enhancement due to texturing is not necessarily a known quantity and is typically up to 2 times larger than the projected cell area [79]. For back contact solar cells the area of the junction is not equal to the area of the cell either.

Figure 4-16 shows a Mott-Schottky plot for a typical p type crystalline silicon module. The plot is very linear, showing a good fit to 4.18.

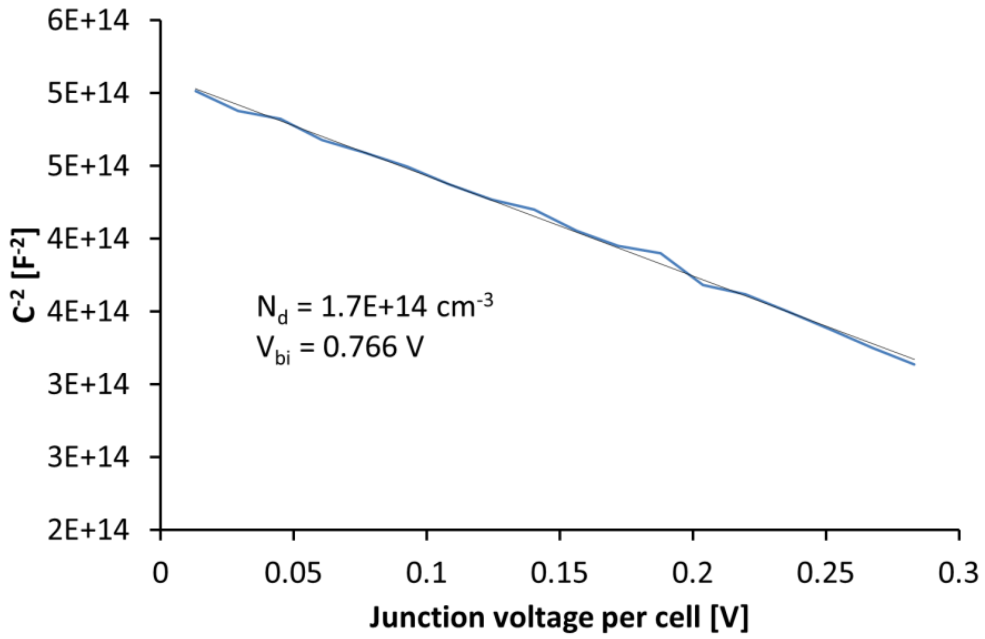


Figure 4-16: Mott – Schottky plot for a c-Si module, showing the linear fit and giving the extracted doping density and built in voltage.

4.4.2 Carrier lifetime measurements

From equations 3.6 and 3.7 the minority carrier lifetime in the device is connected to the diffusion capacitance which dominates the measurement at high forward bias conditions. Taking the logarithm of equation 3.6 gives

$$ln(C_{diff}) = b\frac{qV}{kT} + \ln(C_0) \qquad 4.19$$

Plotting the logarithm of the capacitance against the voltage should give a straight line and from extrapolating the line and finding the intercept C_0 the minority carrier lifetime can be found. Alternative equation 3.8 shows that the minority carrier lifetime is equal to the diffusion capacitance divided by $\frac{dJ}{dV_j}$. It was mentioned earlier that the parameter b is a fitting parameter. In some cases this parameter is unnecessary and the measurements fit well to the line with b=1, as shown in the example of n-type module 1 which is shown in Figure 4-17. However, in some cases this parameter is necessary, as for example for the HIT module shown in Figure 4-184.15, where the measured data fits well if the value of b is 0.95. When the value of b is different from 1 it indicates deviation from the assumptions in the derivation of 4.143.6 / 3.7 which therefore are not necessarily still valid. In the case that the fitting parameter is needed, the resultant minority carrier lifetime should be treated with caution.

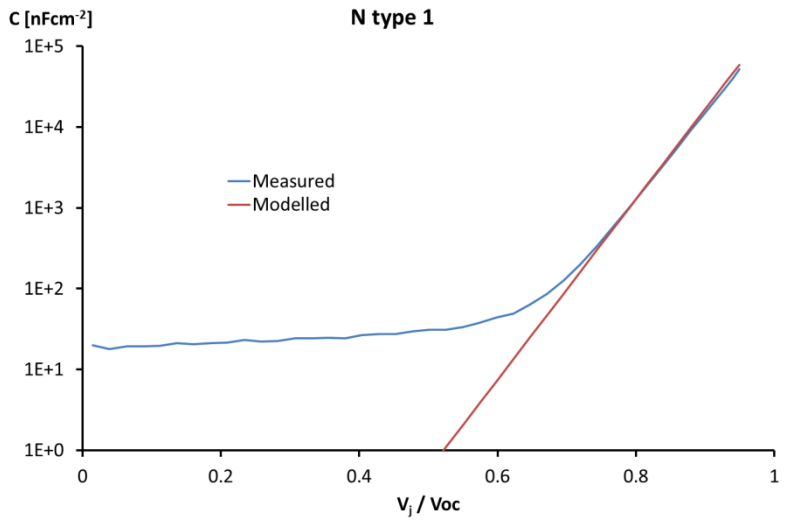


Figure 4-17: The experimental fit of the diffusion capacitance for the n type module 1. In this case the fit is good without the need for the fitting parameter b. The extracted minority carrier lifetime is 125µs.

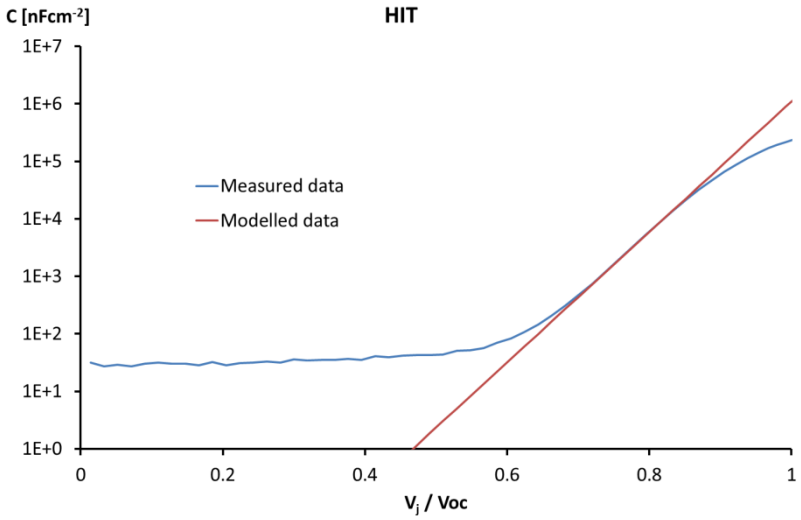


Figure 4-18: The diffusion capacitance of the HIT module. A good fit to the model is obtained with a fitting parameter b=0.95. The extracted minority carrier lifetime is 820µs.

All of the modules measured show a good adherence to the exponential model in some region from roughly 3/4 V_{oc} to a value slightly below Voc. The deviation from the model at lower voltages is expected and is due to the junction capacitance dominating in this range. At voltages near to V_{oc} the measurements tend to increase less strongly than the exponential. The reason for this also is expected because the derivation for equations 4.14, 4.15 assumes low injection, at the voltages near to V_{oc} this is not the case.

Table 4-3: The measured minority carrier lifetimes for each module measured

Module	Minority carrier lifetime [µs]	Voc/cell
HIT	820	0.704
Back contact	560	0.658
N type 1	125	0.658
N type 2	120	0.632

4.5 Conclusions

In this chapter a module scale capacitance measurement system was developed. Two utilities of capacitance measurements were expanded upon in the chapter. Firstly it was used to predict the dynamic response of high capacitance PV modules to step changes in the voltage, which can be used to predict the capacitive charging currents induced by the changing voltage during an I-V measurement. A method was developed to optimise performance measurements using this modelling which allowed fast measurements without sacrificing measurement accuracy. The new method significantly reduces the number of pulses needed to measure a highly capacitive PV module compared to conventional split sweep measurements. Compared to other measurement methods for highly capacitive modules it has the advantage of requiring minimal setup for each module type, reduced possibility for modelling errors, and gives additional useful information in the form of the C-V characteristic, the dark I-V and a precise measurement of the series resistance of the module.

The second application of the system that was discussed in this chapter was to probe internal parameters of the device. The carrier concentration and built in voltage are parameters that are often extracted from C-V measurements in cells and using this system these measurements were also successfully made on modules. This application in particular is utilised further in the next chapter where it is used to measure how the doping density changes as a function of electrical bias preconditioning in CIGS modules. It is also possible to extract the minority carrier lifetime from the C-V measurements at higher forward bias voltages. These measurements were made however as discussed in the chapter they are currently subject to higher uncertainties which originate from the flexibility of fitting different modelling parameters.

Predicting the dynamic response of the module is also useful for the purpose of inverter design, which is another possible application for this measurement system. This application was not explored in this work but is an interesting possible opportunity for further research.

While capacitance measurements of PV cells are a widely used and extremely powerful measurement technique, the same measurements on PV modules are underutilised in the industry. This work shows both how to make capacitance measurements of PV modules and also demonstrates some of the application of these measurements. It is

hoped that this will encourage further adoption of the method. It is predicted that the novel method developed for measuring I-V curves of highly capacitive modules could have a high impact if it is adopted by industry.

Conclusion of the problem of high capacitance and link to metastability in CIGS

There are two major problems for performance measurement of photovoltaics which are addressed in this thesis. Chapter 4 completes the work on the first of these problems, that of high capacitance measurements. These problems generally affect different types of device with high capacitance affecting high efficiency silicon based devices and not causing issues in CIGS devices. These are affected instead by metastable problems, which is the subject of the remaining chapters.

The problem of high capacitance is intrinsically linked with high efficiency, so as the industry continues to push to higher performance modules the measurement issues will become more severe, and solutions to the problem will become even more important than they already are. The tailored voltage ramp method was developed to address this. It successfully provides a solution capable of allowing most high capacitance modules to be measured in a single 10ms illumination pulse, representing up to a tenfold increase in measurement speed. At the same time the error due to capacitive charging is maintained below 0.5%. All the necessary knowledge of the module can be measured prior to the illumination pulse for the I-V measurement, so that the method does not require prior knowledge of the module. The method is applicable to production line measurements since the sweep optimisation can all be performed rapidly and individually for each module.

Many aspects of the work presented in this chapter are also directly relevant to the following chapters on metastability in CIGS. Specifically the measurement system developed is directly useful also for the problem of preconditioning in CIGS. In the previous chapter, C-V measurements of modules were used to model the dynamic response of PV modules upon step changes in voltage, and in turn use that model to optimise the voltage ramp in order to reduce the total measurement time without compromising accuracy. It was already shown that C-V measurements can be used to extract other useful device information including the doping density. This specific use of the system will also be used for monitoring the changes that occur in a PV module during preconditioning.

5 Quantification of Preconditioning in CIGS

5.1 Introduction

The metastable performance changes in CIGS photovoltaics manifest themselves in a variety of different ways depending on the specific device, which makes it extremely difficult to devise a generalised preconditioning routine applicable for all CIGS modules. Much effort has been made to understand these performance changes, and while considerable progress has been made there is still no unanimously accepted theory, equally a comprehensive measurement protocol has not been developed due, at least in part, to a lack of understanding of the causes of these effects.

Preconditioning effects can have a large influence on the measured power output of devices, with differences of over 10% in measured STC power commonly observed. It is very important therefore to have a proper understanding of these effects and how to deal with them for a variety of reasons [80]. Most importantly among these reasons is the fact that STC power measurements are used to set the price for PV modules, so an error in the STC measured power is a very serious problem. If modules cannot be consistently preconditioned to an identical state then degradation studies can be rendered useless because irreversible degradation is masked by reversible metastable changes. These studies are considered critical in order to prove the durability of any new module, so for this purpose it is essential to be able to consistently bring modules to a specific state. For the task of energy yield prediction there is the further requirement that the measurement is not only repeatable but is actually representative of the state of the modules during operation outdoors.

In this chapter a variety of experimental results are presented investigating preconditioning in CIGS devices. The focus is on investigating the rates of preconditioning and relaxation back to an unconditioned state. Since information on these rates was not readily available before this work, this information is one of the most important aspects to come out of this thesis. Sections 5.2-5.4 describe the first investigation that was performed. In these sections light soaking, electrical bias preconditioning and spectral response (SR) measurements were made on a set of CIGS modules from 5 different manufacturers. The SR measurements were performed in order to investigate if there was any link between bandgap and preconditioning. A new measurement system was built to perform the SR measurements, so the system itself is

detailed as well as the results. During this initial investigation of preconditioning, an unexpected short timescale effect was observed. In this effect a performance improvement could be observed after milliseconds of illumination exposure, with relaxation occurring in less than 30 seconds. This effect was investigated in more detail and is presented in section 5.5.

In section 5.6 the electrical bias preconditioning of the modules is investigated again in more detail using the C-V measurement system developed in chapter 4. Using this system it was possible to precondition the modules and make measurements of C-V, dark I-V and light I-V without disconnecting the module. This allowed significant improvement in the accuracy of the timing of the measurement and shorter minimum timescales as well as extraction of extra information from the C-V and dark I-V curves. The C-V measurements give information about changes in the doping density of the CIGS absorber layer during the preconditioning. The set of modules used in this experiment was expanded to include 3 further manufacturers compared to those used in section 4.3.

In the subsequent chapter the experimental results from this chapter are used to support discussion of the theoretical aspects of these preconditioning changes.

Table 5-1 gives a brief description of the modules used for the experimental work in this chapter. Each module unless stated otherwise is from a different manufacturer. Due to availability not all of the modules were used in every experiment.

Table 5-1: list of the modules used for the experimental work

Module	Description	Manufacturer
1	glass substrate	Solar frontier
2	glass substrate	Bosch
3	glass substrate	Q Cells
4	Old module, glass substrate	Siemens
4b	Old module (>2 years outdoor exposure), glass substrate	Siemens
5	Pre-production module, flexible cells on metal foil	TATA
6	Flexible cells on metal foil	Miasole
7	glass substrate	Würth
8	Glass substrate	Avancis

5.2 Light soaking in modules

Relatively little literature was found relating to how long it takes CIGS modules to precondition and how long it takes them to relax back to the dark state. Without this knowledge it is difficult to know how long to precondition a module for and how quickly after the preconditioning the module needs to be measured. The purpose of this experiment was to measure this for a variety of different CIGS modules.

5.2.1 Method

This experiment was carried out on modules 1 to 4 from Table 5-1. Using the pulsed solar simulator, each module was measured at standard test conditions and at 200Wm^{-2} directly after dark storage. The modules were pre warmed on a heating mat to reduce the temperature change of the module during light soaking. Just before measurement the module was covered and moved from the heating mat into position in the light soaker. The cover was then removed at the beginning of the measurements.

Light soaking was applied with metal halide lamps with an intensity equivalent to 200Wm^{-2} for two hours. From discussion in section 3.2 the spectrum of the light is potentially significant so it was measured and is shown in Figure 5-1. During light soaking I-V curves were measured every 4 seconds and between measurements the module was kept at open circuit voltage. The temperature was measured throughout the light soaking. After the light soaking the modules were again measured at STC and 200Wm^{-2}. For modules 1 to 3 periodic measurements were then made at STC to measure the rate at which the modules relaxed to the dark state.

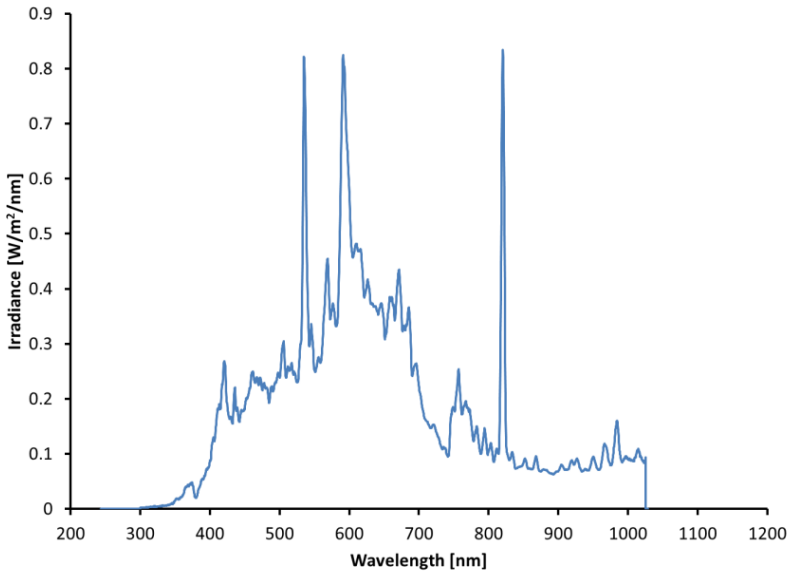


Figure 5-1: Measured spectral output of the light soaker in the wavelength range 300-1025nm.

The STC I-V curves were measured using a AAA rated Pasan IIIB pulsed solar simulator. The I-V curves during the light soaking were measured using single quadrant Egnitec I-V tracers. The module temperature was measured via the Egnitec units using a pt100 sensor at the back of the modules.

5.2.2 Results

After the measurements on the different modules were performed, it was found that all of the modules improved to some extent after the light soaking treatment as can be seen from the measured I-V curves in Figure 5-2. However the extent of the improvement varied. For the STC power measurements the improvement was between from less than 1 % to 5%.

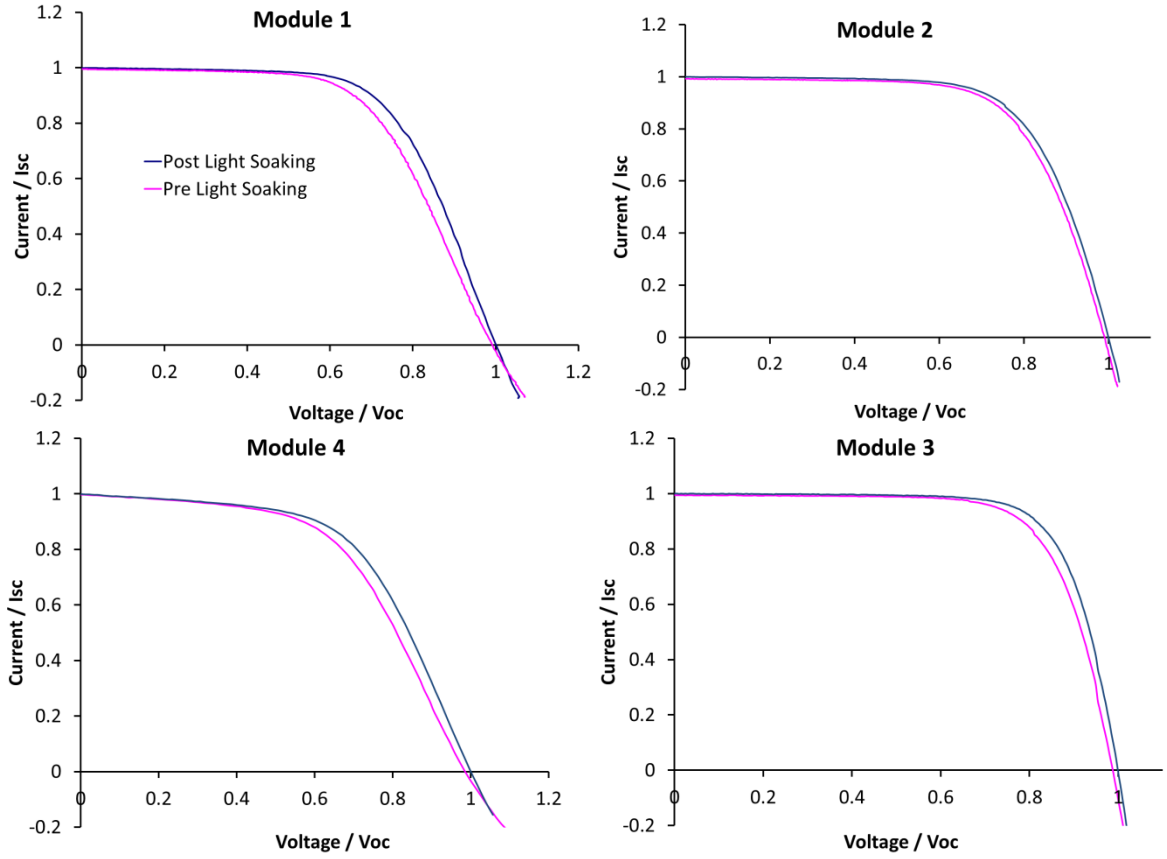


Figure 5-2: IV curves of the modules at STC conditions before and after 2 hours of light soaking at 200Wm^{-2} equivalent

For modules 1 and 4 the improvement was mainly in the form of an improved fill factor, whereas for modules 2 and 3 the V_{oc} also improved significantly. The I_{sc} of all the modules remained the same after preconditioning.

Module 5 was originally intended to be part of the light soaking test, however during the initial measurement it was noticed that there was a very strong hysteresis in the

measurements made with voltage sweeps in opposite directions, which made it impossible to make any sensible measurement. As discussed in the previous chapter hysteresis in the I-V curve is common for high capacitance modules, however this case was different because the problem was not alleviated when the measurement was split between multiple illumination pulses to reduce the voltage ramp. The same effect was also observed in module 4 but to a lesser extent. The measured I-V curves of module 5 are shown in Figure 5-3.

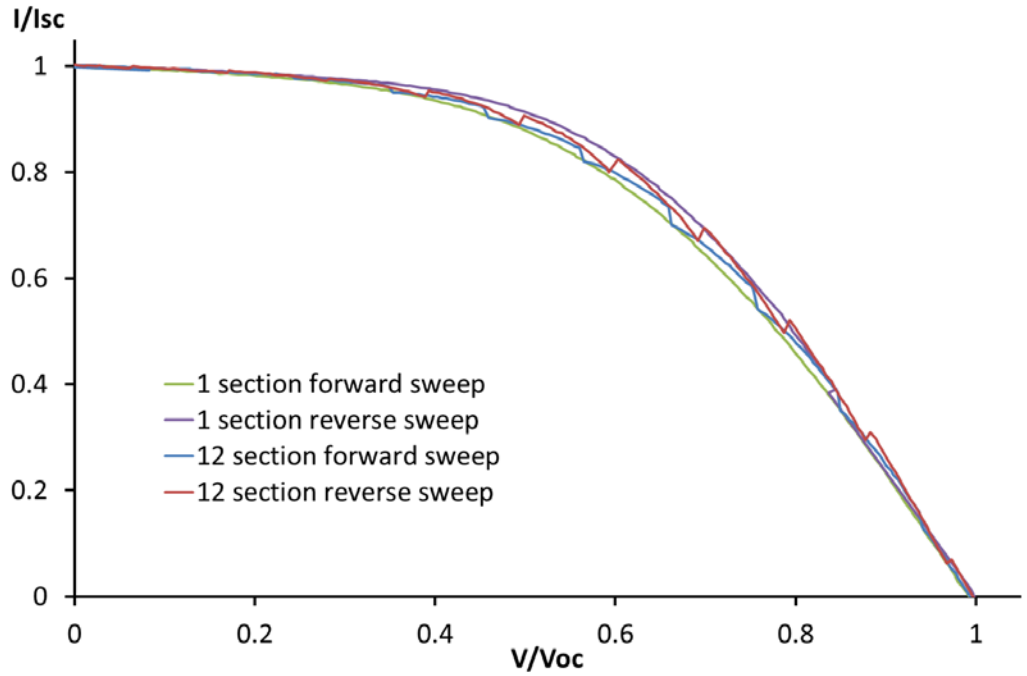


Figure 5-3: I-V curves of Module 5 showing the unusual non-convergence of the forward and reverse I-V curves. From the single section I-V curve measurements the effect appears similar to the effect of high capacitance, however the 12 section measurements appear very different from capacitive effects and instead it appears to be the consequence of ms timescale preconditioning.

If the error were caused by capacitive charging, then during the forward sweep pulse the measured current would reduce relative to the steady state current, instead the opposite is observed. It appears instead as though the module is displaying a metastable performance improvement which occurs on the millisecond timescale and relaxes again within the 30 seconds that the lamp power supply takes to recharge before the next measurement can be made. The further investigation of this unexpected effect is presented in section 5.5.

Pre warming the modules significantly reduced the temperature changes during preconditioning but it was not possible to eliminate entirely. The temperature of the module still changed significantly during the measurements, which obscured the effects of preconditioning in the measured I-V curves. However a performance improvement in

the first minutes can be seen for module 1 which is the module that showed the largest performance change.

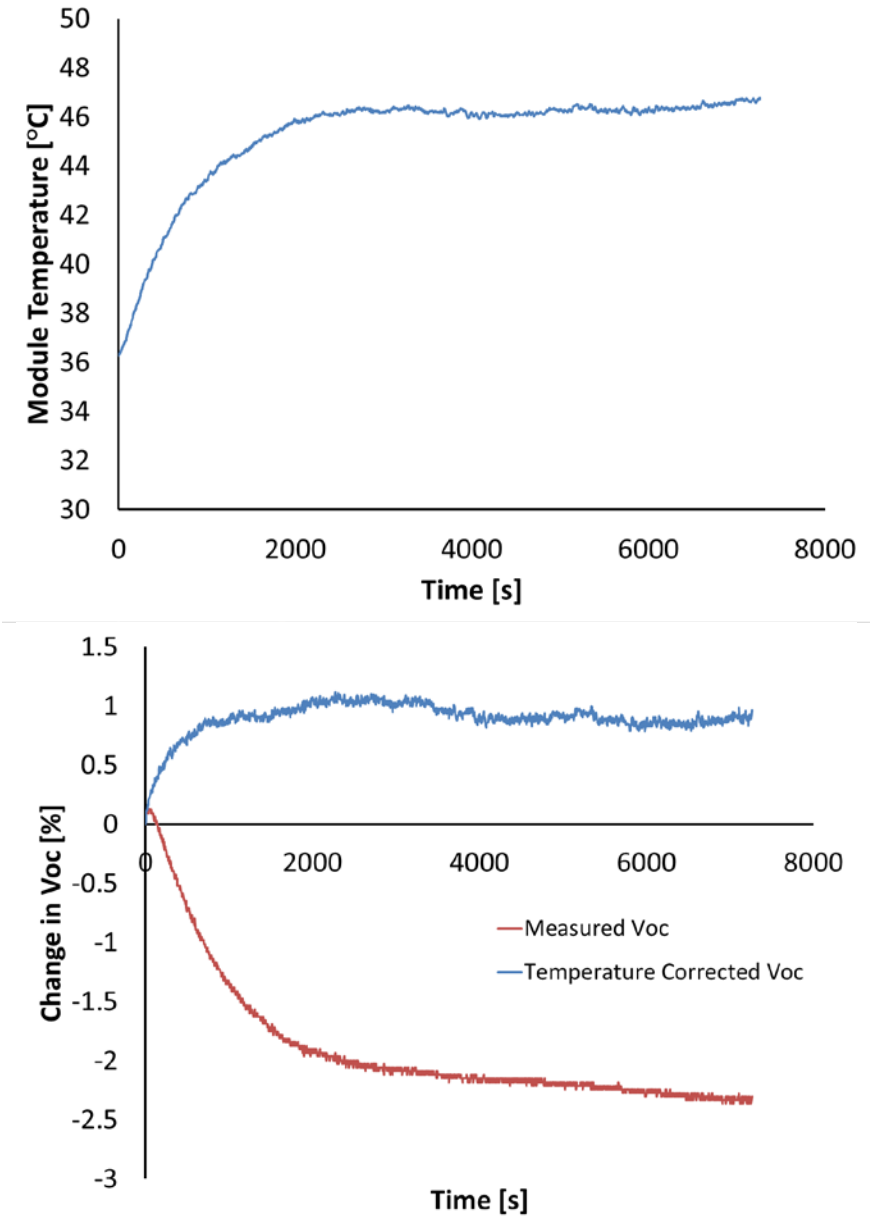


Figure 5-4: Voc and temperature as a function of light soaking time for module 1

Figure 5-4 shows the measured temperature and Voc as a function of light soaking time for module 1. A small increase in the Voc can be seen to increase during the first minute of the measurement despite the fact that the temperature of the module is also increasing which normally causes the V_{oc} to decrease. After the first minute the temperature increase dominates and the measured Voc decreases, so the measured module temperature was used to apply a correction to the measured V_{oc} to try and isolate the changes due to preconditioning from that due to heating of the module. Both the as-measured and temperature-corrected versions are shown in Figure 5-4. The

temperature coefficient used for the correction was 0.3%/K which was taken from the datasheet value for the module. After the correction there is a much more obvious performance improvement, which occurs over a longer period.

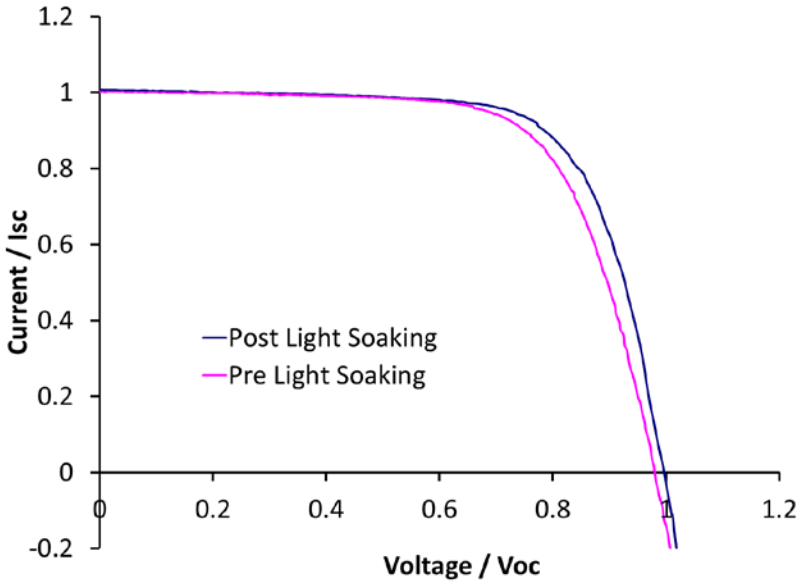


Figure 5-5: I-V Measurements of module 1 from the pulsed simulator at 25°C and 200Wm^{-2}. This measurement was made at reduced irradiance for comparison with the measurements from the light soaker.

The difference in the Voc between the before and after measurements at 200Wm^2 was 2%, the IV curves are shown in Figure 5-5. The size of the improvement seen in the light soaker is slightly less than 1% which seems to agree with other observations that the effect of preconditioning is reduced for higher temperature measurements [37]. It should be noted however that the size of the change measured during the light soaking is relatively small and errors in the temperature correction have a large effect. The total size of the change corresponds to a 3°C temperature difference. Unfortunately due to limitations in the measurement system values of the maximum power point during the preconditioning were too noisy to see the improvement during preconditioning.

For modules 1 to 3 the STC measurements were made periodically for several days after the preconditioning to see how quickly they relaxed to their initial dark state. The results of the relaxation are shown in Figure 5-6. The zero time is taken as the time when the first measurement after the preconditioning was performed, which was around half an hour or longer after the end of light soaking. The relaxation after the light soaking occurs over several days and is much slower than the preconditioning, however the relaxation is occurring much more rapidly at the beginning so it cannot be

clearly shown if significant relaxation occurred during the cooling of the module between light soaking and the first simulator measurement.

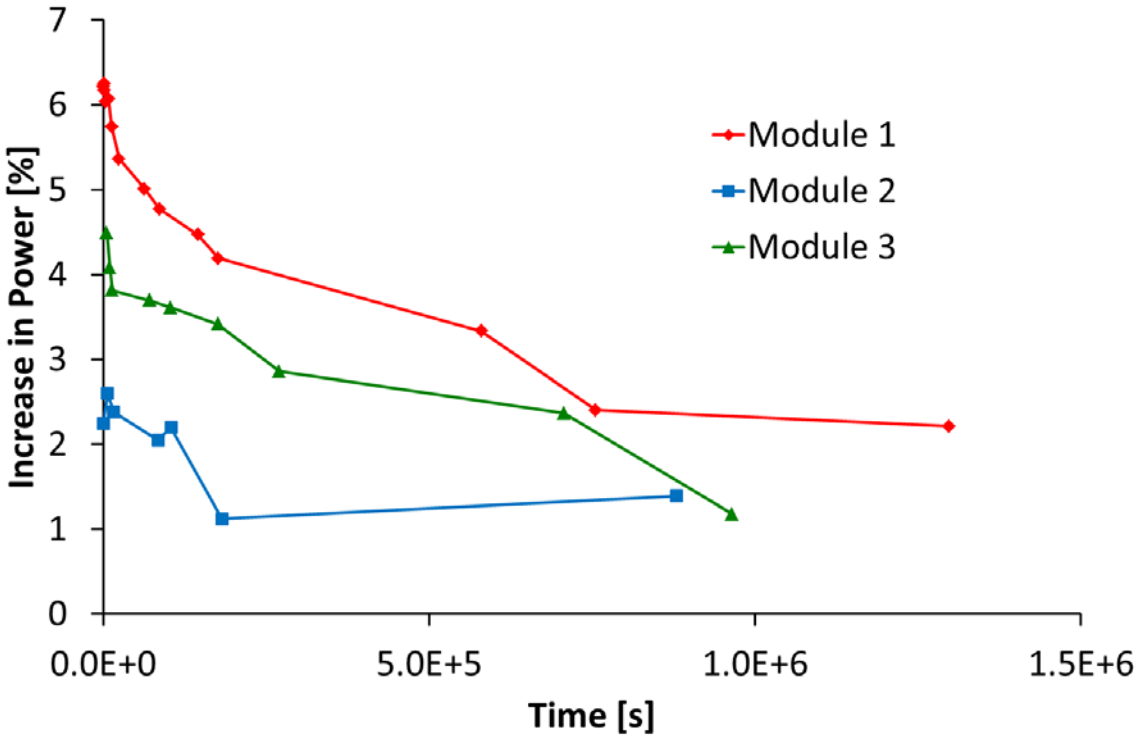


Figure 5-6: Relaxation of the measured power after light soaking. Measured power is displayed as a percentage of the power measured before preconditioning. Time is displayed in seconds for consistency with later plots: 1E6s is 11.5 days.

The light soaking experiments have showed the same increase in efficiency with light soaking usually observed in CIGS modules. It proved very difficult to measure the preconditioning as it was occurring during light soaking because of the heating of the module. The modules took several days to fully return to the relaxed state. An important point to note for subsequent chapters is the relaxation was much faster immediately after the preconditioning. It will be shown that in the time while the module was cooling down there is likely a significant relaxation. During the course of these measurements a new and unexpected preconditioning effect was observed which occurred in the 10ms during the illumination pulse.

5.3 Electrical bias preconditioning in modules

Electrical bias has been seen previously to have a similar preconditioning effect to light soaking and has been suggested as a possible alternative for preconditioning modules for performance measurements [48]. For full sized modules, electrical bias is significantly easier to apply in a controlled way than light soaking. In particular, it induces significantly less heating than light soaking. For this reason the rates of

preconditioning using electrical bias preconditioning on the same CIGS modules as used in the previous section were evaluated.

There is also a strong theoretical case for the equivalence of forward bias and illumination. The persistent photoconductivity effect has been shown to be a property of the bulk CIGS absorber layer caused by an increase in doping density when metastable defects convert from compensating donors to acceptors with the capture of two electrons [63]. This effect must be occurring during the light soaking and seems to be a likely cause of preconditioning in CIGS, although given the many metastable effects observed it may not be the only process occurring. The mechanism for the change is the increase in electron concentration which causes the defect to capture electrons and convert into the acceptor state. Illumination and forward bias both cause an increase in the electron concentration in the absorber layer and so they both equivalently cause this defect conversion.

5.3.1 Experimental setup

In this section, modules 1 to 5 were used. Each module was measured after at least a week in dark storage and then subjected to a forward voltage bias equal to roughly 90% of the open circuit voltage. This voltage was used because it was close to the highest voltage that could be used without causing heating to the module. At intervals during the forward bias treatment the bias was briefly removed and I-V curves were measured. These were measured at standard test conditions using a AAA rated PASAN 3B pulsed solar simulator. The curves were measured using a single pulse with a positive voltage ramp. In the case of module 5 and, to a lesser extent, module 4 there was still a strong hysteresis between the forward and reverse sweep measurement but a single sweep measurement was made for consistency; to reduce the interruption of preconditioning; and since multiple flash measurements did not improve the measurement in any case as demonstrated in Figure 5-3. The module was disconnected from the voltage bias for approximately 10 s during before and 10 s after the I-V measurement, however this was a manual process so the timing varied slightly for each measurement point. Measurements were then taken at intervals after the forward bias treatment to measure the rate at which the modules relaxed to the dark state.

5.3.2 Results

All 5 of the modules exhibited a performance enhancement after forward bias treatment, although the magnitude varied from over 11% (without visible stabilisation) to less than 1%. As with the light soaking the performance improvement was predominantly due to improvement in fill factor, although most modules also showed an improvement in open circuit voltage. Performance improvements occurred very rapidly at first but further improvements continued to occur much more slowly. This can be seen in Figure 5-7, which shows the increase in measured power as a function of time for module 5. On the linear time scale of the plot it seems as though the increase in power has stabilised, however this is deceiving, when the plot is viewed on a logarithmic timescale as in Figure 5-8 the power can be seen to be still increasing, only at a much slower rate.

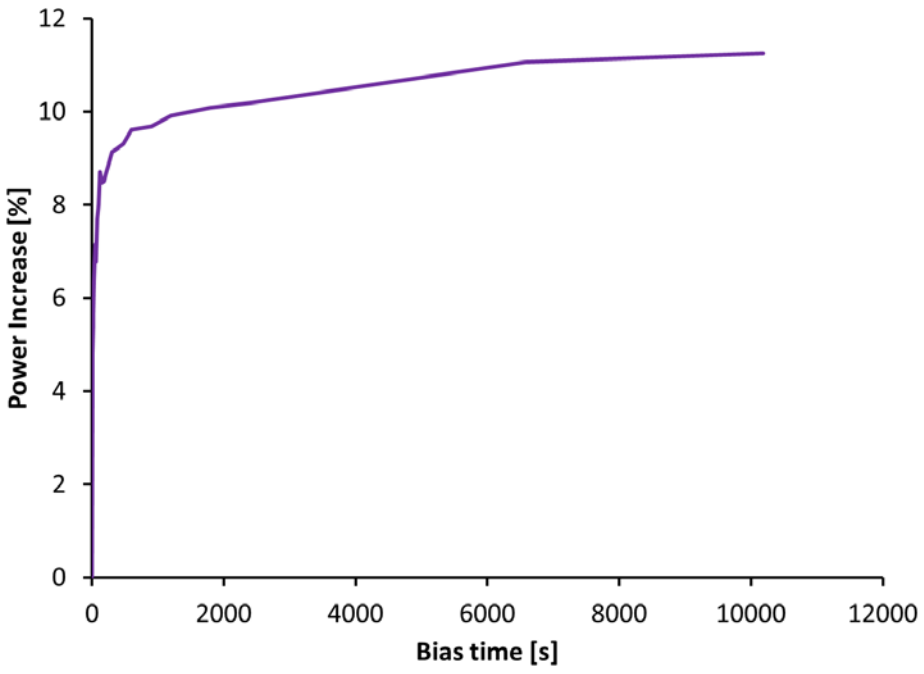


Figure 5-7: Increase in power as a function of forward bias preconditioning time. The increase in power is initially rapid but appears to level out substantially after 2 hours.

On the logarithmic timescale the increase in power is almost linear over several orders of magnitude in time. The modules relaxed to their initial state similarly with an almost linear relaxation on a logarithmic time scale. This is an important observation because it implies that if light soaking is used to precondition CIGS modules, they start to relax back to their dark state during the cooling time even though subsequent measurements show only very small relaxation within further periods equal to the cooling time, which

can give the false impression that the relaxation in the cooling time was negligible. This is a potential problem with the procedure often employed to measure these modules.

The time taken for the modules to stabilise varied quite strongly, taking from less than a minute for module 3 to over 3 hours for module 4, which along with module 5 did not stabilise within the measurement period. In general, the modules that experienced the largest performance change took longer to stabilise.

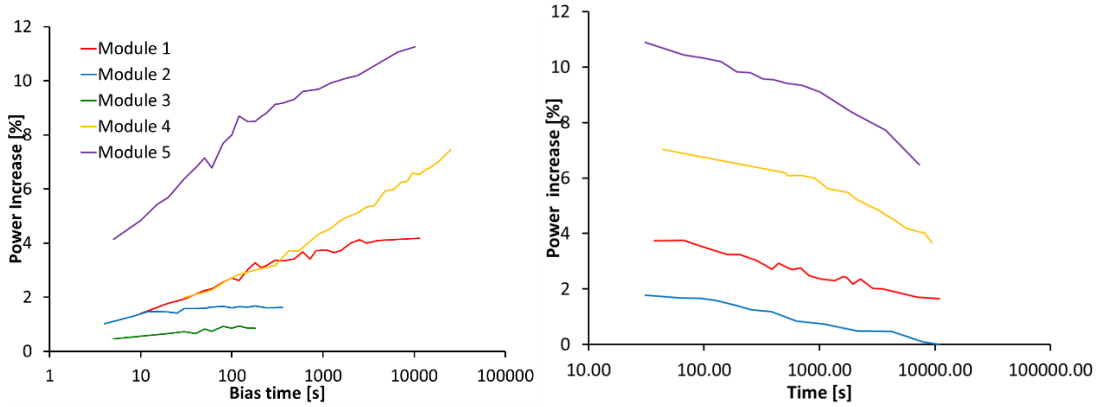


Figure 5-8: The change in the measured power of 5 CIGS photovoltaic modules during electrical bias preconditioning and subsequent relaxation. The relaxation of module 3 is not shown because the noise in the measurement appeared to be bigger than the change in the power which was very small.

5.4 Spectral Response of CIGS modules

One of the potential advantages of CIGS as a photovoltaic absorber material is that its bandgap can be tuned by varying the ratio of $x = \frac{Ga}{In+Ga}$ and also by varying the ratio $y = \frac{Se}{Se+S}$ [81]. In practice, varying the ratios x and y have many additional effects on the device apart from varying the bandgap and different manufacturers use slightly different values for these ratios, which could be one of the factors causing the observed differences in preconditioning. In particular theoretical predictions of the V_{Se}-V_{Cu} defect predict that the activation energy for the defect conversion depends on the ratio x, with no activation energy necessary for small values of x. It is also conceivable that there would be other reasons that the preconditioning would be related to the bandgap. In order to investigate if there is any link, the spectral response of each module was measured and the long wavelength cut off of the spectral response was used to infer the bandgap.

5.4.1 Details of the spectral response measurement system

CREST had no previous spectral response (SR) measurement system suitable for use with modules, so in order to proceed a new SR measurement system was constructed as part of this work. Figure 5-9, shows a photograph of this system. SR measurement on modules has two added complications over those of cells caused by the series connection of cells and simply by the size of the device. There are two types of method for measuring the spectral response, one where the whole device area is illuminated uniformly with the probe light and another where all of the probe light is focused onto a small area within the device. These methods are known as over or under illumination respectively. The probe light can be either light from a grating monochromator, or band pass filtered light from a light source [24,82]. For this system a monochromator was used, which provides the highest wavelength resolution. The high wavelength resolution is desirable for finding the cut off wavelength, however using a monochromator it is more difficult to obtain high illumination. Creating a uniform monochromatic illumination over a module area would waste a considerable fraction of the available light and also be more technically challenging than creating a small spot, so the under illumination method was used.

Figure 5-9: Picture of the measurement system

When there is a series connection of many cells small changes in the current of one cell caused by the perturbing monochromatic light do not necessarily translate to changes in the overall current of the module. This problem is solved using the method of

Hishikawa [83] to force the probed cell to be the current limiting cell as shown in Figure 5-10. In this method the whole module is illuminated with a background light and the measurement cell is partially shaded which causes it to be the current limiting cell. The whole module is also put under forward bias so that the measurement cell does not operate under reverse bias breakdown.

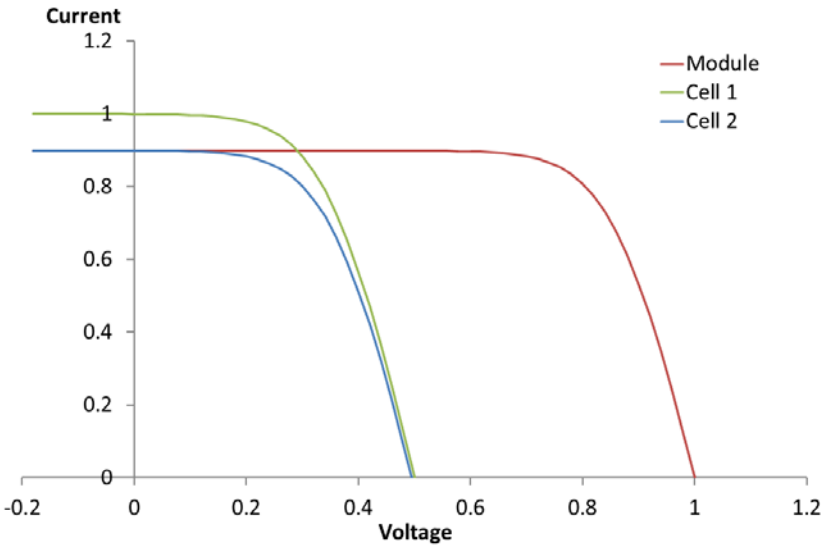


Figure 5-10: Demonstration of a 2 series cell module. Cell 2 is illuminated 10% less than cell 1, which causes cell 2 to be the current limiting cell. A small change to the current of cell 1 is not reflected in the module current whereas a change in the current of cell 2 is. For the spectral response measurements the measured cell is partially shaded to force it to be current limiting so that the module current will respond to the monochromatic perturbation signal.

The monochromatic illumination is chopped at 160Hz and the current output from the module is measured using a lock in amplifier. Figure 5-11 shows a schematic of the system which details the parts used. The wavelength range of the system is 400-1100 nm.

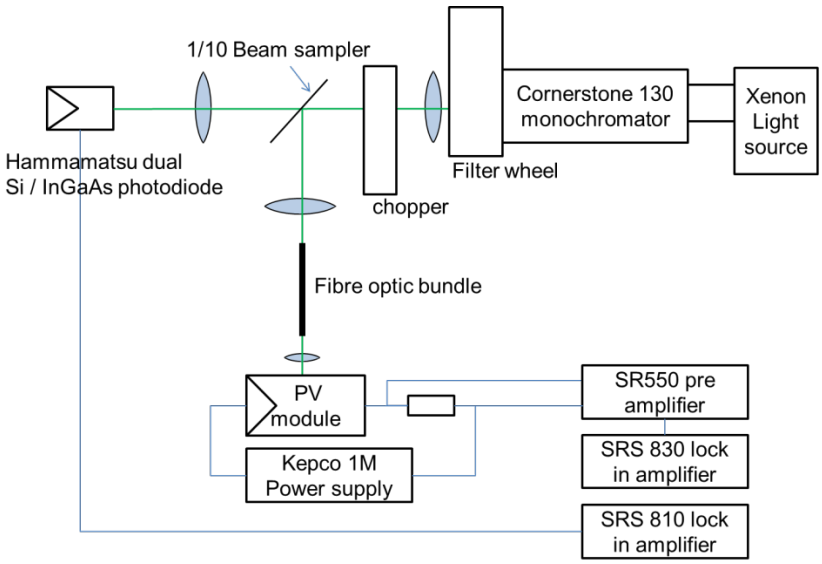


Figure 5-11: Schematic diagram of the SR measurement system built for this work

5.4.2 Results

The measured spectral response of the modules versus photon energy can be seen in Figure 5-12. The results are relatively noisy because of the weak probe signal, however the large difference in signal between the EQE below and above the bandgap means that the noise does not prevent estimation of the bandgap. The results imply the modules have band gaps between 1.06 eV and 1.2 eV. This is in line with expectation since the smallest possible bandgap comes from the pure CIS ternary compound which has a bandgap of roughly 1.0 eV, common absorbers have x=0.3 which gives a bandgap around 1.15 eV but the bandgap of CGS is much higher at 1.7 eV.

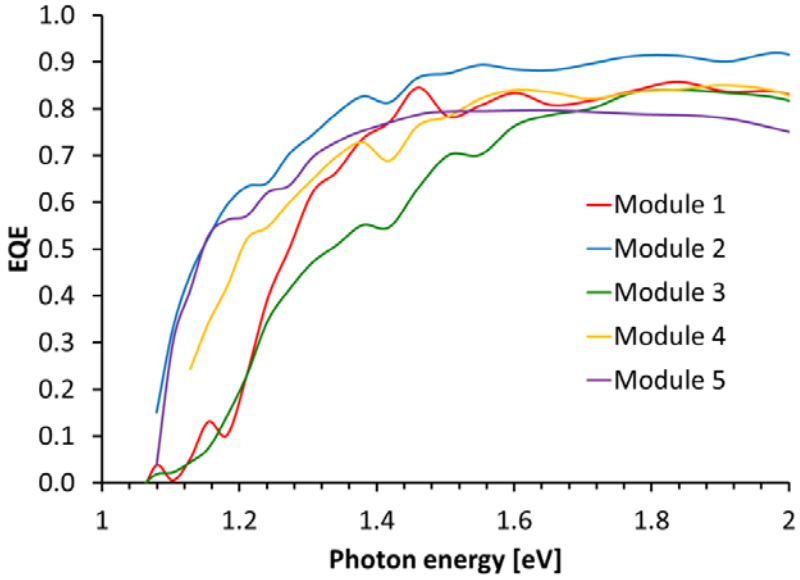


Figure 5-12: External Quantum Efficiency Vs photon energy

Precise estimation of the bandgap and the rates of the preconditioning are difficult with the data available, however this is not necessary as it is readily apparent that the rate of preconditioning does not seem to follow the bandgap. Whereas modules 2 and 3 were the fastest to reach a steady state during the preconditioning they have bandgaps on opposite ends of the measured range. Equally modules 1 and 5 were the slowest to stabilise and were also at opposite ends of the bandgap range. The total size of the efficiency change during preconditioning equally does not show any correlation with the bandgap.

This section was undertaken as a preliminary investigation as to whether the bandgap of the CIGS modules is related to the preconditioning within those devices. The results show clearly that this is not the case, and that another factor or factors must be responsible. One likely candidate is the Fermi level within the devices, which changes

the concentration of free holes and electrons, and therefore changes the rates of metastable defect conversion.

5.5 Millisecond timescale preconditioning

The observation of preconditioning occurring within the 10 ms pulse of the simulator was unexpected and presents a major challenge for performance measurements using pulsed simulators. It was decided to investigate the phenomenon further. The effect was first noticed on module 5, however, closer inspection showed that the effect could be observed in all of the devices. From the initial observation the performance improvement occurred during repeated flashes implying that the effect relaxed within the 30s it takes for the simulator to charge up for the next pulse. The effect was investigated both in modules and for a single cell of the same type as in module 5.

5.5.1 Module measurements

A performance improvement within the milliseconds of the illumination pulse could be observed for all of the devices measured as shown in Figure 5-13.

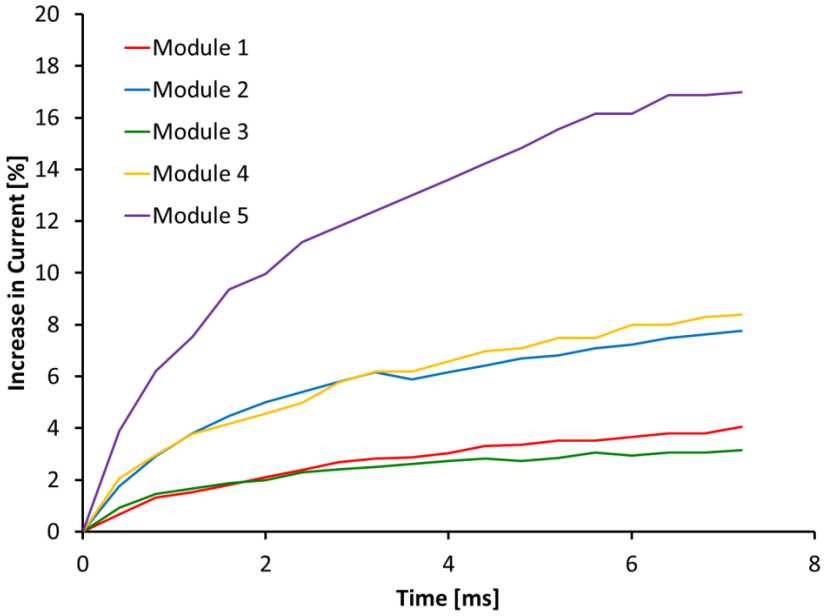


Figure 5-13: Transient preconditioning of different commercial CIGS modules. The current at a constant voltage was measured as a function of time. The voltage of the modules was kept at a constant value roughly equal to 90% Voc.

In this data the voltage was fixed at roughly 90% of the Voc and the current was measured as a function of time. Capacitive charging effects are related to the voltage ramp rate so since the voltage is fixed capacitive charging can again be discounted. The main effect of the ms timescale preconditioning was a fill factor improvement, so the largest percentage improvement in current at a set voltage occurs at a voltage

somewhere between the maximum power point and the Voc. The value of 0.9 Voc was chosen deliberately to be somewhere close to where the maximum percentage current increase was expected. For none of the devices did the current reach a steady state within the period of the illumination pulse.

For all of the modules the magnitude of the millisecond timescale preconditioning was significantly less after 11.5 hours of electrical bias preconditioning was applied as can be seen in Figure 5-14.

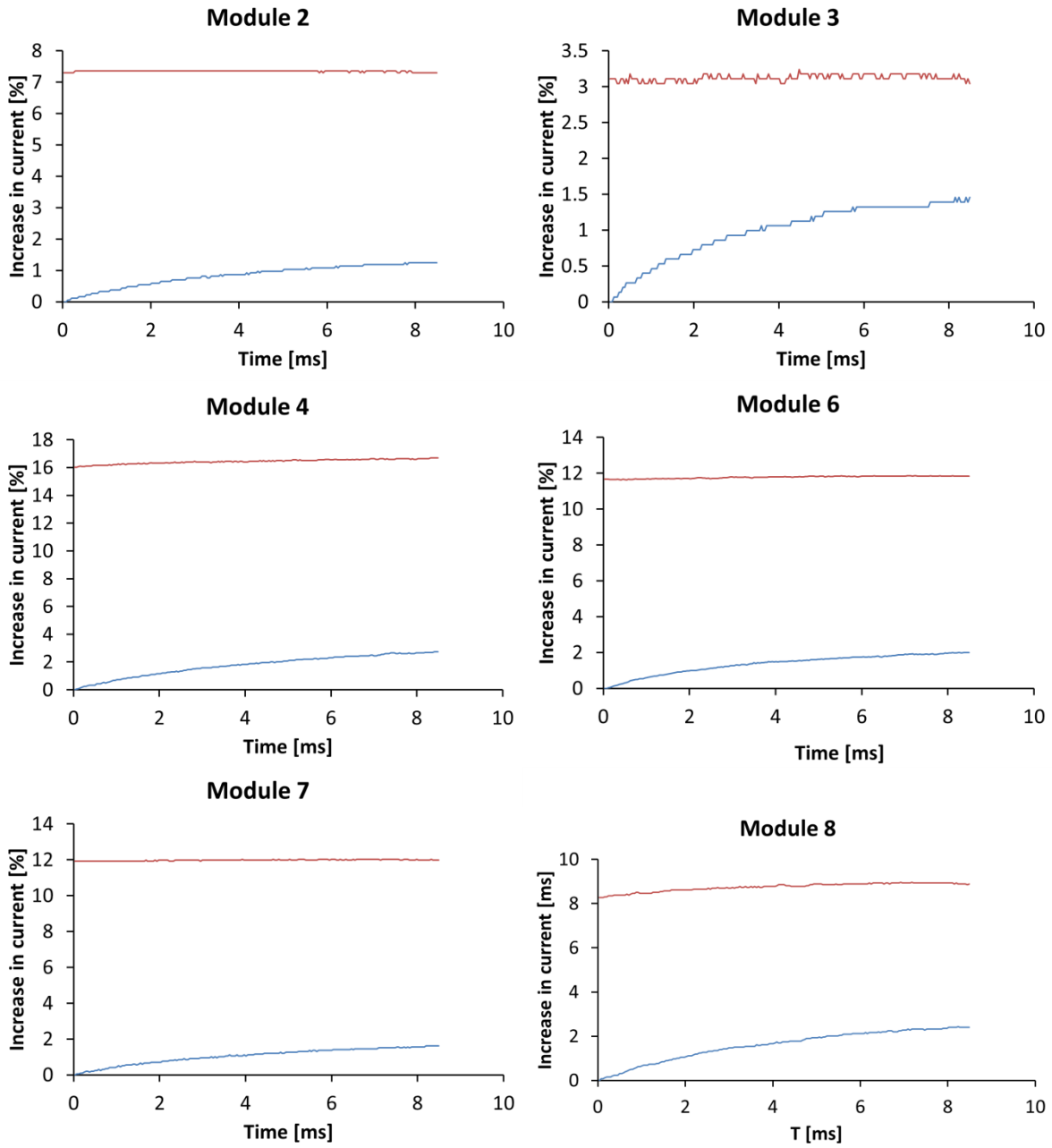


Figure 5-14: Current as a function of time during an illumination pulse. The voltage is held constant at the maximum power point voltage. Measurements were made before (blue) and after (red) voltage bias preconditioning.

This is important because it shows that for most of the modules the preconditioning within the timescale of a simulator pulse is eliminated or reduced to the point of being negligible if preconditioning is previously applied. For the modules where this is the case it significantly simplifies the measurement process. For modules 4b and 8 there was still a noticeable increase in the current during the flash after the preconditioning. The voltage set point for the measurements in Figure 5-14 was chosen to be close to the maximum power point voltage so the effects are not exaggerated as in the results in Figure 5-13. However, since the Vmpp also increases, the effect on the maximum power point is larger than the increase in the current seen in Figure 5-14.

5.5.2 Single Cell Measurements

In order to investigate how long the effect took to stabilise and relax a smaller cell of the same type as the cells in module 5 was used. This allowed measurements that were not possible to investigate from module scale measurements, because of the limitations of the pulse duration and charging time between pulses in the module scale pulsed simulator. For the smaller cell device the CREST prototype LED simulator [84] could be used. The advantages of LEDs as the light source in this case are that they turn on and off very quickly and can easily be programmed to do so for arbitrary pulse durations.

The relaxation rate was measured by measuring the current at a fixed voltage and illumination and then turning the illumination off for different periods of time and measuring the difference in current between just before and just after the dark period. During the dark period the cell is kept at 0 V. During the illuminated periods, the intensity was approximately 350 Wm^{-2}, after correction for spectral mismatch to AM1.5. It should also be noted that the spectral mismatch was quite large due to a lack of power in the infrared range in this simulator. The photocurrent was measured for 10 seconds after the illumination was turned on. As the LEDs heat up after the start of illumination, they gradually reduce in power output, this was compensated by increasing the power input to them in stepwise manner, which kept the power output within an acceptable range that could be corrected using the measured illumination from a monitor diode. Corrections were made for variations in intensity of the light source and the temperature of the cell as it heated up under the light. Corrections were made for irradiance and temperature variation as shown in Figure 5-15.

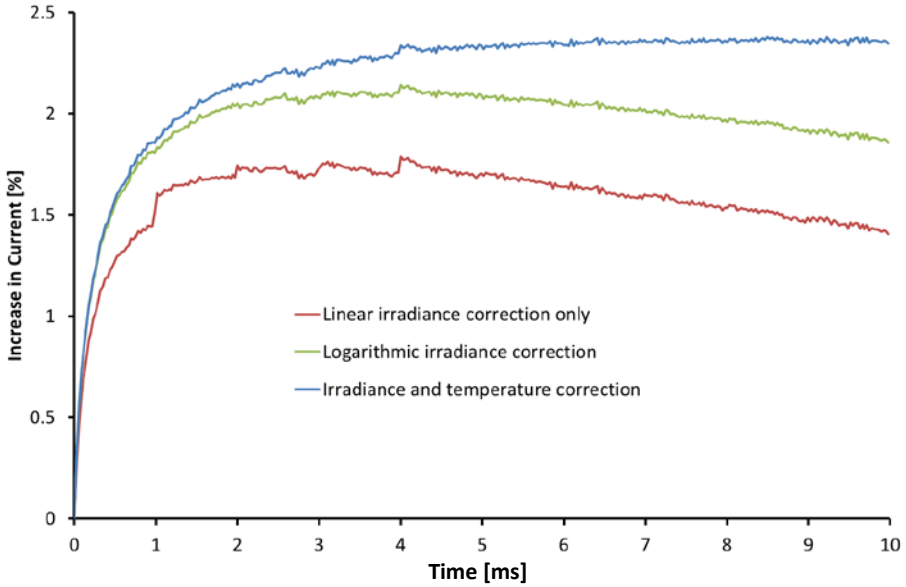


Figure 5-15: Current as a function of time during illumination after different data correction steps.

The temperature correction was approximated as a linear reduction in current with time, the gradient of which was extracted from the final portion of the measurement once the transient had stabilized. This assumes that the linear change in current in this region is primerally due to a change in temperature, and that the rate of change of temperature is the same in this region as in the initial period. The illumination intensity correction consisted of a linear and a logarithmic term. The size of the logarithmic term was determined as the value which eliminated discontinuities in the measured current at the points where the LED power was increased. The final result was a smooth curve showing the increase in current against time since the illumination was applied.

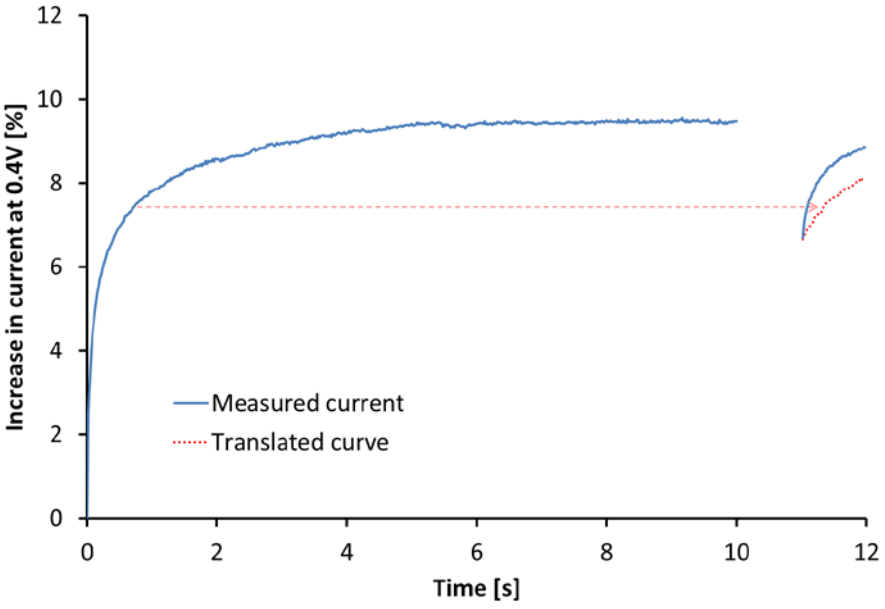


Figure 5-16: Current as a function of time for a single CIGS cell after the light is turned on for 10s, then off for 1s, then on for a further 1s. The blue curve shows the actual output, the red curve is the section of the same curve translated in time for comparison.

Figure 5-16 shows an example of the measured increase in current as a function of time. The increase is again strongly non-exponential, with the current increasing very rapidly in the first 100 ms, with continued, but more gradual, increase until around 6s. After the 1s gap from illumination the current has partially dropped back towards its initial starting point. It quickly begins increasing again with the next period of illumination. The figure also shows a shifted version of the initial current rise for comparison with the rise during the second exposure. The increase during the second exposure is faster than the increase from the same starting point during the first. If the stretching of the exponential were due to an increase in the doping density, which then slowed the rate for further changes, then rate of increase in current should depend on the starting condition of the module and the shifted curve from the first illumination period should match the curve from the second. Since it does not there must be either more than one distinct processes or one process with a distribution of rates.

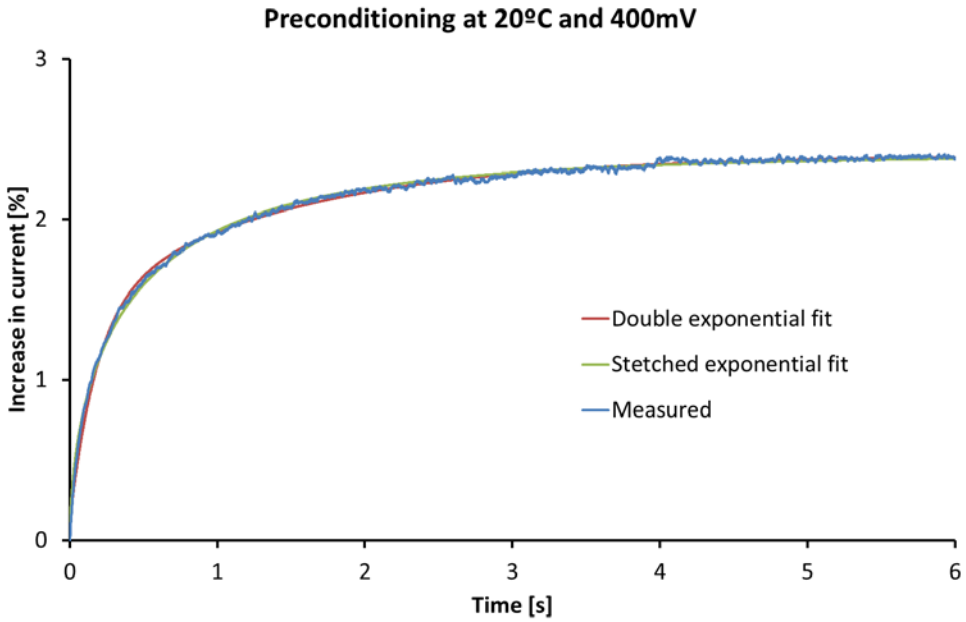


Figure 5-17: Transient rise in photocurrent for a CIGS cell, along with double exponential fit and stretched exponential fit.

Although the measured transients cannot be fitted by a single exponential, they can be successfully fitted by either a sum of two exponentials or stretched exponentials. A sum of exponentials would be the correct model to use if the underlying mechanism has two distinct processes with a different time constant for each. This model provided a good fit to the data, an example of which is shown in Figure 5-17.

The stretched exponential model is

$$\delta = \delta_0 \exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right) \qquad 5.1$$

Where δ represents the change in current. Stretched exponentials are often used to fit changes in various device parameters caused by metastable defects and can appear very similar to the sum of multiple exponentials [85,86]. The stretched exponential model can derive from several different physical origins including a distribution of activation energies. The stretched exponential has one less free parameter than the double exponential fitting, and it is relatively easy to fit to the data. By comparison, fitting the sum of exponentials is harder since very similar curves can be produced with different parameter sets. On comparison of the two methods it was decided to use the stretched exponential model, since on an Arrhenius plot for extracting the activation energies of preconditioning and relaxation this method gives much more linear results. The stretched exponential fit to the preconditioning at 25°C gives a time constant of 0.32 s.

In order to extract the apparent activation energy for the preconditioning the experiment was repeated at a number of temperatures between 15°C and 55°C at the same load voltages. The rate constants of the stretched exponential fits are plotted in an Arrhenius plot in Figure 5-18, which gives an activation energy of 0.27 eV.

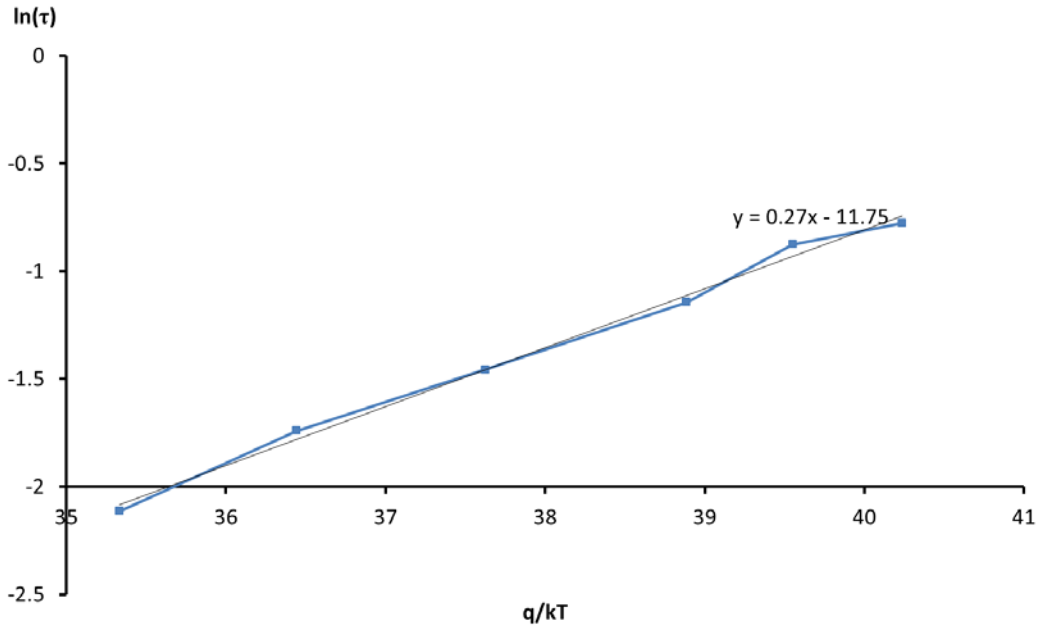


Figure 5-18: Arrhenius plot of the time constant for the stretched exponential increase in the current with preconditioning time. The plot gives an activation energy for the preconditioning of 0.27eV.

The relaxation during the dark period is defined as the percentage drop in current compared to the total increase in current during the initial illumination period. The measured relaxation is shown in Figure 5-19. The stretched exponential fit is also shown. The time constant τ from the stretched exponential fit is 1.66 s and after this time the relaxation is over 60%. Due to the stretching it will take significantly longer to fully relax to the initial state. Extrapolating the fit suggests that after 30 s the relaxation will be over 99%, thus explaining why in the pulse simulator measurements the preconditioning induced during the flash has relaxed before the next measurement.

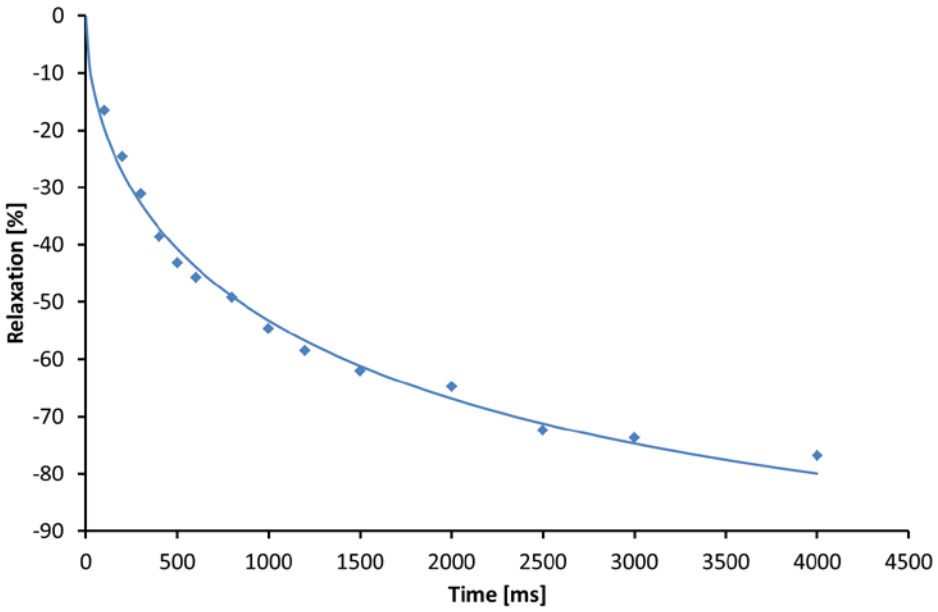


Figure 5-19: Relaxation of the transient preconditioning. The current at a 0.4V was measured for 10s while under illumination then the illumination was stopped and the voltage set to zero for various periods of time before both were re-applied. The current after the gap is plotted as a percentage of the rise in the initial 10s of illumination. The line is the stretched exponential fit to the data.

Both the preconditioning and relaxation rates are much shorter than the rates observed in the previous sections. While the preconditioning rate could be affected by differences in voltage or illumination the relaxation occurs in the dark at 0 V, so it should be unaffected. The difference in relaxation kinetics seems to show that the ms timescale preconditioning is a distinct effect from the longer timescale preconditioning.

In conclusion, for CIGS devices there is a preconditioning effect that occurs on a sufficiently short timescale to cause performance improvements during the illumination flash of pulsed simulators. This effect is common to all modules measured here. In some cases it is large enough to significantly distort I-V measurements, although in many it is not. If electrical bias preconditioning is applied until immediately before the pulse it eliminates or significantly reduces the preconditioning during that pulse, which

provides a solution to the measurement problem. The millisecond timescale preconditioning and associated relaxation follow stretched exponential distributions. In the case of the cell measured and the conditions used here, the time constant for preconditioning was 0.32 s and for relaxation was 1.6 s. In both cases the stretching means that it takes many times longer than the time constant to reach a stabilised state.

5.6 Automated electrical bias preconditioning with I-V, C-V and dark I-V monitoring

The capacitance of CIGS devices is often observed to change during preconditioning. This is likely due to changes in the doping of the device during preconditioning, perhaps through changes in metastable defects, or copper migration. Similarly, the dark current is also linked to preconditioning within the device. There are two reasons to try and observe the C-V characteristic and dark current during preconditioning. Firstly, the changes that occur provide insight into what is occurring and improve understanding. Secondly, it could provide a method to track the preconditioning state of a module without making I-V measurements. This could be used in order to initiate an I-V measurement once a module has reached the desired preconditioning level. In this section electrical bias preconditioning measurements of modules are performed again, but this time making C-V and dark current measurements during the process, using the measurement system developed in chapter 4. The automation of the process also significantly increased the accuracy of the timing during the experiment.

5.6.1 Method

Seven different modules were used for the experiment. Module 4 was not available at the time of these measurements, so module 4b of the same type was used. The modules were biased at the maximum power point voltage, specifically the STC maximum power point voltage measured before preconditioning was applied, since the maximum power point in general varies with preconditioning. After a period of electrical bias preconditioning the I-V curve was measured, and then immediately afterwards the C-V curve was measured. The electrical bias is applied again for double the previous preconditioning period. The dark current is measured continuously while the electrical bias preconditioning is being applied.

For the C-V measurements the amplitude of the oscillating voltage was set to 10mV per cell and a frequency of 5kHz was used. The C-V curve was measured in 8 points from a

low voltage equal to the amplitude of the oscillation up to 1/3rd of the Voc (as measured before preconditioning). The number of points for the CV curve along with the measurement time per point was deliberately kept low in order to reduce the amount of time for the C-V measurement. The preconditioning voltage is applied at all times except during the I-V sweeps which last 10ms each and during the C-V sweeps which last 11s each. After the preconditioning, I-V and C-V measurements of the module were taken at doubling time intervals as the module relaxed.

5.6.2 Results

The percentage changes in the performance parameters Pmpp, FF, Voc and Isc for each of the modules is shown in Figure 5-20. The results are much less noisy than the results of the first preconditioning rate experiment presented in section 5.3 due to the automation of the preconditioning and measurement process, which significantly reduced the timing errors in the experiment. This is an important result in itself as it points towards the fact that many of the errors associated with CIGS measurements are due to insufficient control of timing of the preconditioning. Another advantage of the automation is the considerably shorter minimum preconditioning times that were achieved in this experiment. In the previous experiment a significant amount of preconditioning had occurred for some of the modules within the first preconditioning step, whereas this time the minimum duration before the preconditioning starts to have an effect can clearly be seen for all the devices. The shortest time for the preconditioning to show an effect is for module 4b after only 1 second and in general the modules begin showing signs of change after about 10s. The saturation of the preconditioning changes did not occur for most of the devices in the 11.5 hours of the experiment. For module 4b in particular the performance improvements occur equally over at least 4 orders of magnitude of time, which is a strongly non exponential behaviour. The onset of relaxation in all the samples occurs between 10s and 100s after the application of bias for most of the modules measured. Module 4b again seems to begin slightly earlier and has shown a drop in performance before the first measurement after only 2s. The relaxation also stretches over several orders of magnitude in time.

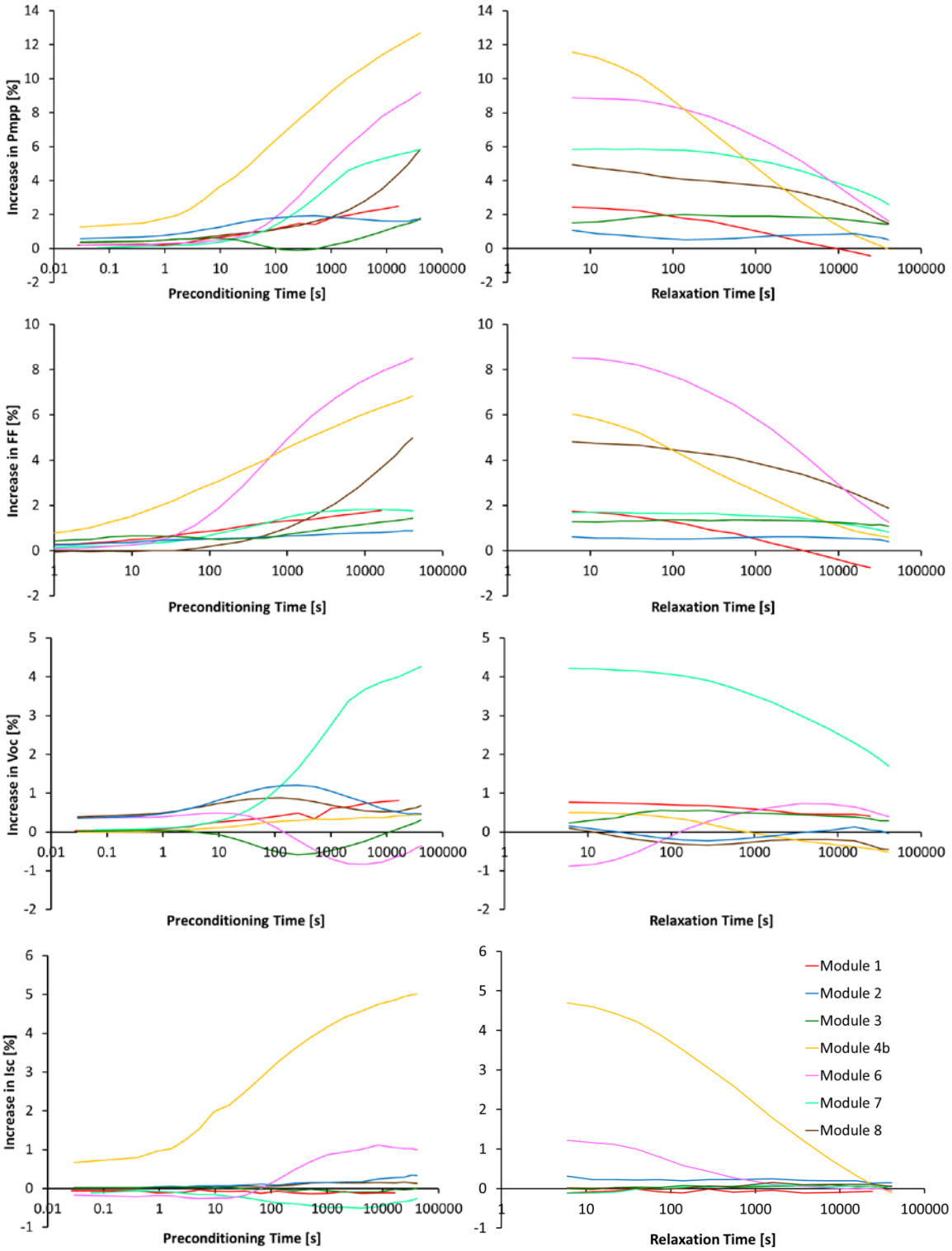


Figure 5-20: Evolution of the performance parameters for each module during preconditioning and relaxation.

In terms of preconditioning the modules the observed kinetics have several important implications. It may be impractical to try and fully stabilise the modules, and to do so may not be truly representative of their outdoor performance, since preconditioning intervals in operation are confined by the length of a day. However, in order to achieve

repeatable results the modules do not necessarily need reach their final stabilised state, the important point is that preconditioning can be applied in a repeatable way. In order to achieve this, the error in the timing of each element of the process should be much less than the length of that process. For example, consider module 4b, after 1000 s of forward bias at Vmpp the module is still changing but in the next 100 s the improvements will be relatively small, even though in the initial 100 s the improvements were very large. Equally, if there is a relaxation period between the preconditioning and the measurement, then the error in the length of this period should be small in comparison to the total length. Considering current procedures used by most laboratories this point is more likely to cause issues with the relaxation period between conditioning a module and measuring it. Given that it takes the module over 10 hours to relax completely it might not be expected that there would be much difference between a measurement made 1 minute after preconditioning was applied and one made 10 after minutes, however for module 4b this results in a 4% difference in the measured power between the two measurements. The alternative is to make sure that the time between preconditioning and the measurement is so short that the module does not have time to begin relaxing at all. For different module types there is a significant variation in the onset time for relaxation, so it should be known for the specific module type before this method can be useful.

Module 4b stands out in several ways, firstly it shows a strong improvement in the short circuit current with preconditioning and secondly for the overall magnitude of the performance increase, which at the end of the preconditioning was more than 12% higher than the initial value and still increasing. This is a significantly older module than the others in the experiment, and has experienced significant degradation from its initial performance. It now has a high shunt conductance as can be seen the IV curves before and after preconditioning in Figure 5-21. The age and degradation of the module are most likely related to the different preconditioning behaviour.

Module 6 also showed a non-negligible change in short circuit current, increasing about 1%. This module also shows a significant increase in performance of about 10% which is mainly from an increase in Fill Factor.

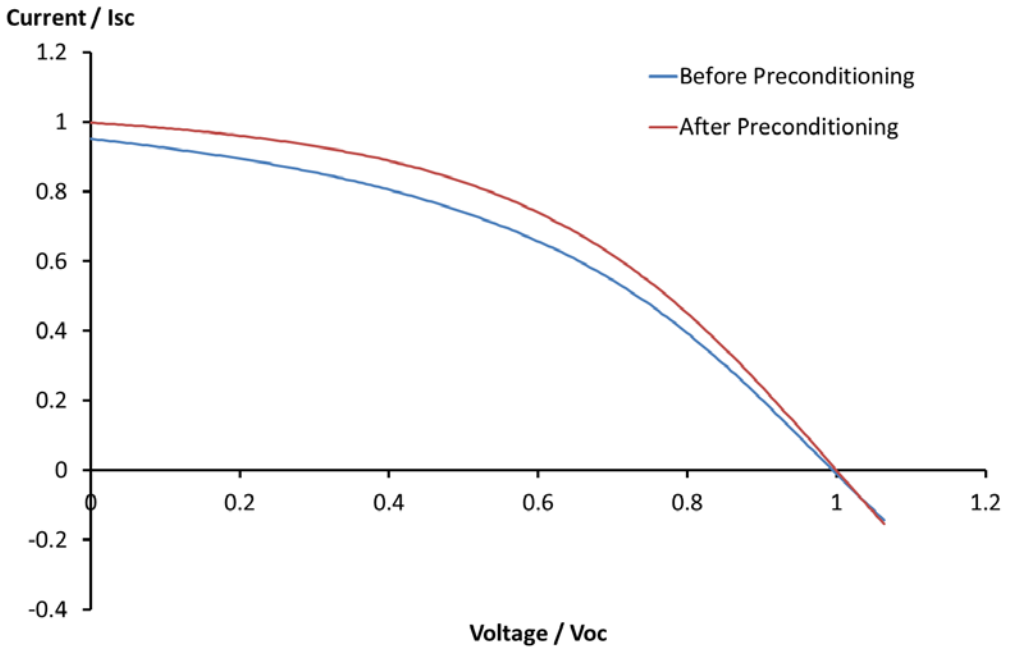


Figure 5-21: I-V curves of module 4b at the beginning and the end of the forward bias preconditioning.

Figure 5-22 shows the C-V curves and Mott Schottky plots for module 2 during the preconditioning. While the Mott Schottky plot is close to linear at the end of the preconditioning, in the earlier stages it deviates substantially from linearity, particularly at the lower voltages. Non linearity in the Mott Schottky plot suggests a spatially varying doping profile through the device, but could instead be due to the effects of deep defects.

The measured C-V curves do not behave as expected if only a change in the doping density were occurring. Figure 5-23 shows these curves for comparison, as calculated from.

$$C^{-2} = \frac{2(V_{bi} - V_{dc})}{q\varepsilon\varepsilon_0 N_A A^2} \qquad 5.2$$

And

$$V_{bi} \approx E_g - \frac{kT}{q} ln\left(\frac{N_A}{N_v}\right) \qquad 5.3$$

The measured results in Figure 5-22 display a near vertical movement of the Mott Schottky plot whereas the model results in Figure 5-23 show that gradient should be changing much more significantly such that the intercept with the x axis is constant.

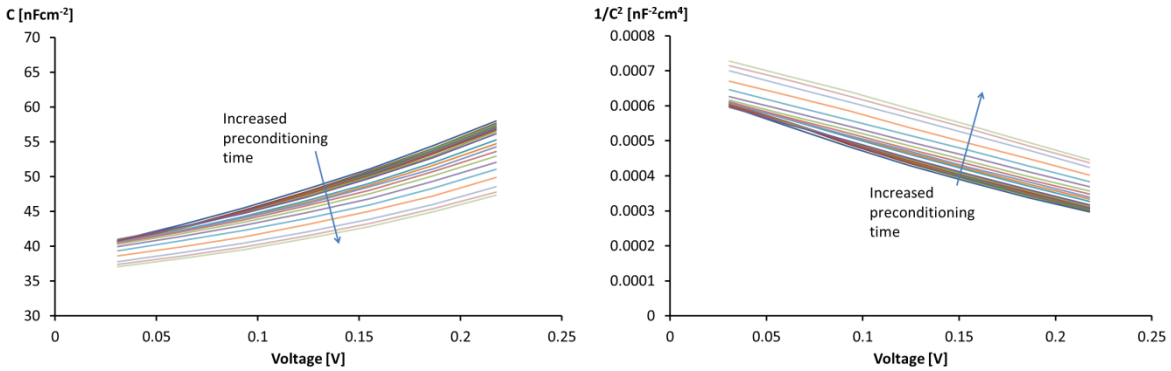


Figure 5-22: C-V and Mott Schottky plots for module 2 during the preconditioning.

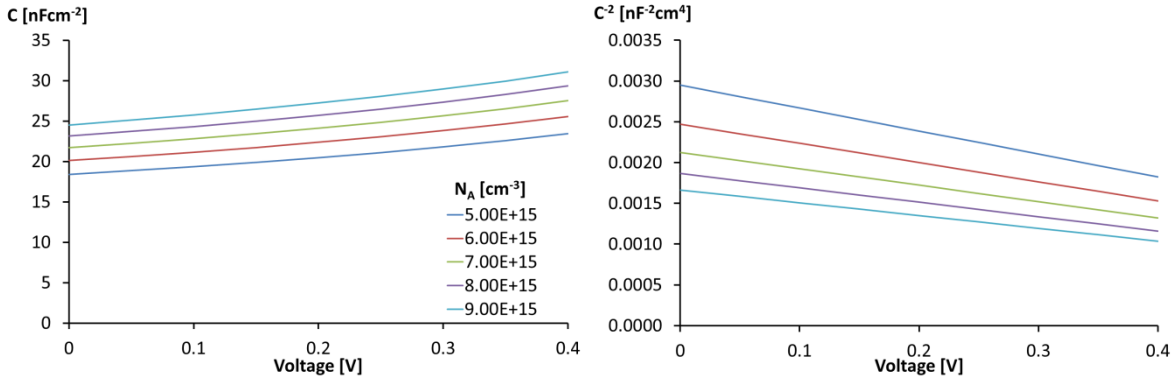


Figure 5-23: C-V and Mott Schottky curves expected if only the doping density was changing

The results correspond with a change of charge deeper inside the space charge region, either at or near the interface. A change in doping of the often hypothesised p+ layer is a very plausible explanation for this effect. To demonstrate this consider the case of an absorber buffer window heterostructure, were the buffer layer is fully depleted and there is an interface charge N_{if} of acceptors, whose charge is independent of voltage. Since the p+ layer is expected to be very thin it can be approximated by this interface charge. The depletion width of the absorber in this case is [81].

$$W_a = \frac{\varepsilon_a d_b}{\varepsilon_b} + \sqrt{\left(\frac{\epsilon_a d_b}{\epsilon_b}\right)^2 + \frac{2\varepsilon_a}{q^2 N_{A,a}}\left[q(V_{bi} - V) + \frac{q^2 N_{d,b} d_b^2}{2\varepsilon_b} - q^2 N_{if} d_b/\varepsilon_b\right]} \qquad \textbf{5.4}$$

Assuming that the interface charge is unable to respond to the AC signal then $C \approx qN_a \frac{dW_a}{dV}$ and therefore

$$C^{-2} = \left(\frac{d_b}{\epsilon_b}\right)^2 + \frac{2}{q^2 \varepsilon_a N_{A,a}}\left[q(V_{bi} - V) + \frac{q^2 N_{d,b} d_b^2}{2\varepsilon_b} - q^2 N_{if} d_b/\varepsilon_b\right] \qquad \textbf{5.5}$$

Changes to N_{if} cause a vertical shift in the Mott–Schottky plot, as demonstrated in Figure 5-24. As the doping in the p+ layer reduces, the capacitance decreases and the Mott–Schottky plot moves vertically upwards. The gradient remains constant and gives

the doping density equivalently to the case equation 5.3 where there is no interface charge. As the doping of the p+ layer reduces, the FF of the device would also be expected to improve. It is not only a change of doping in the p+ layer which could cause the observed change - any change in charge within the space charge region which does not extend to the edge and does not change with voltage could be responsible. Since this charge will affect equation 5.4 in a very similar way by adding different constant term in place of the N_{if} term. Specifically, a photo-doping of the buffer layer or a change in interface charge could both account for the observed C-V profiles.

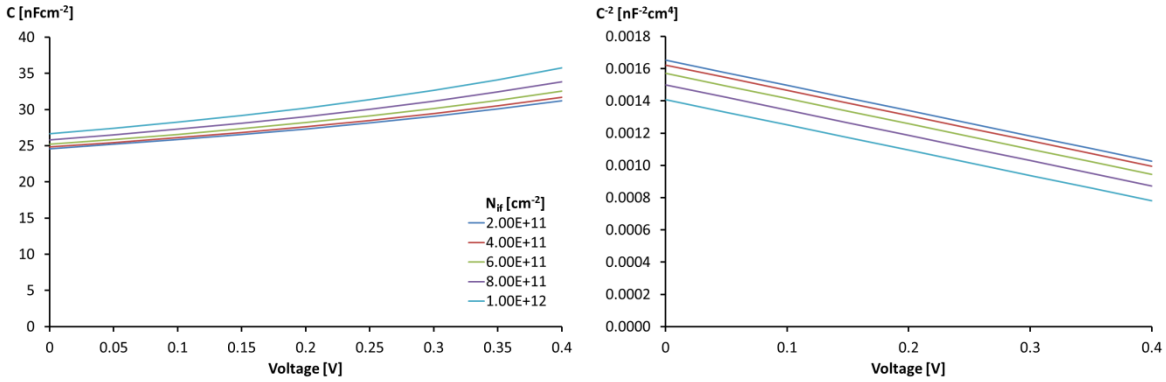


Figure 5-24: Simulated C-V and Mott Schottky curves with the doping of a p+ layer changed

Figure 5-25 shows the evolution of the CIGS absorber doping as extracted from the Mott–Schottky plot of the C-V measurements. Also shown in the figure are the change in the capacitance at 1/3 Voc and the dark current just before the I-V measurement. Large changes in the extracted doping density are observed, the maximum being a 39% increase for the module 4b. Many of the modules display a change in the direction of the doping density variation. For modules 2, 6 and 7 there is a clear increase followed by a decrease whereas for module 3 the opposite occurs.

For four of the modules, N_A relaxed back towards its initial value after preconditioning. However, for modules 3, 6 and 7 before beginning to relax the measured doping density increased rapidly to a value significantly higher than that just before the preconditioning was stopped.

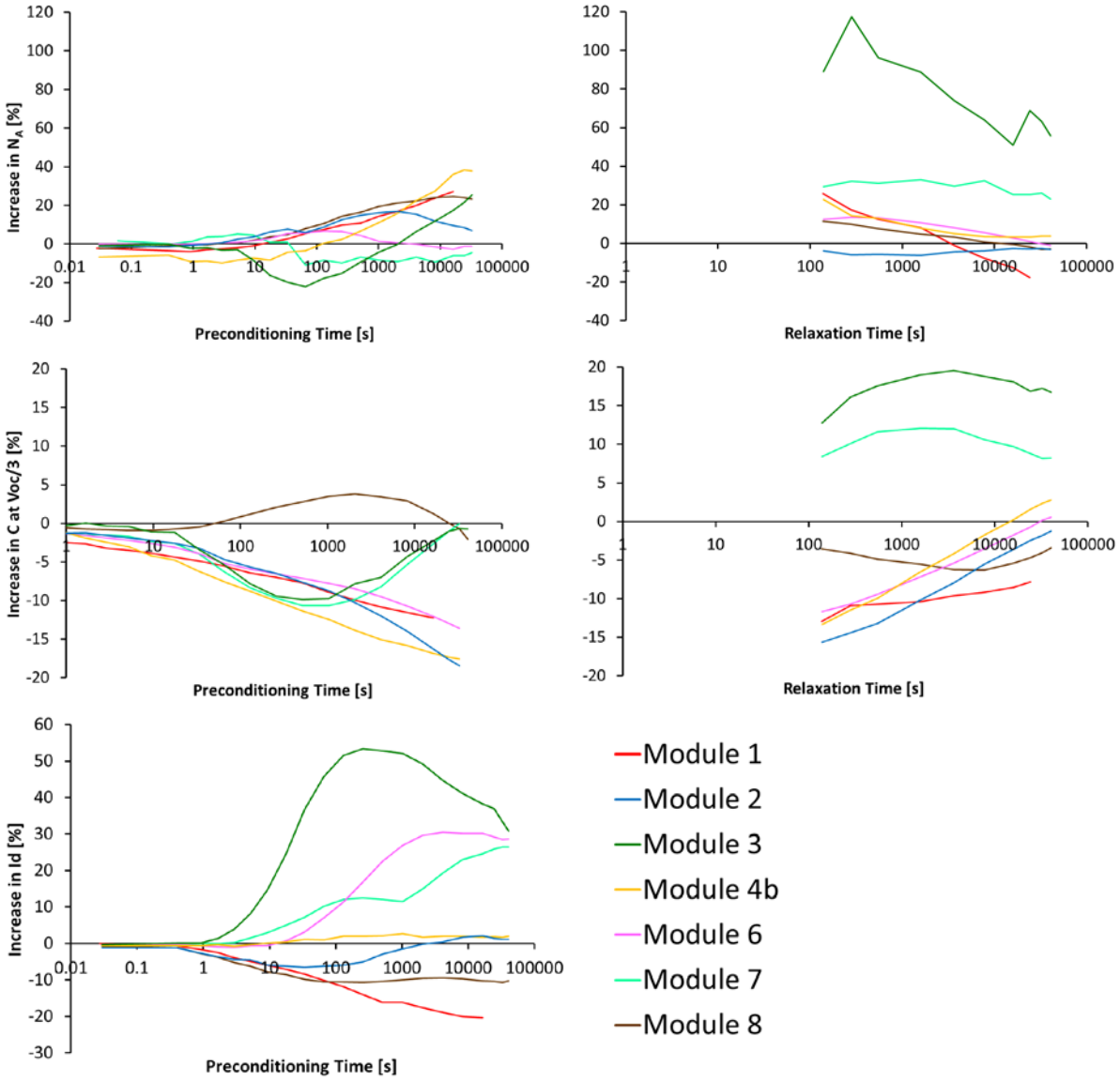


Figure 5-25: Changes in measured doping density and capacitance at 1/3Voc during preconditioning and subsequent relaxation. The change in the dark current during he preconditioning is also shown.

One possible explanation for these effects is that there are two different processes occurring, an increase in doping density in the bulk of the device and a decrease in the density of charge stored in the p+ layer close to the junction. These processes could be related to the red light and blue light effects which have opposite effects on the capacitance and should both be present during light soaking, and may or may not both be present during electrical bias preconditioning. In this explanation, the increases in N_A would come from the increase in bulk doping due to persistent photoconductivity in the bulk, via the same mechanism as the red light effect. The decrease in N_A would come from the same mechanism as the blue light effect, and most likely does not represent a

real decrease in the acceptor doping but some other change at or near the interface which affects the measurement in this way.

As well as the capacitance, the dark current was measured during the preconditioning. Figure 5-26 shows the dark current as a function of the total preconditioning time.

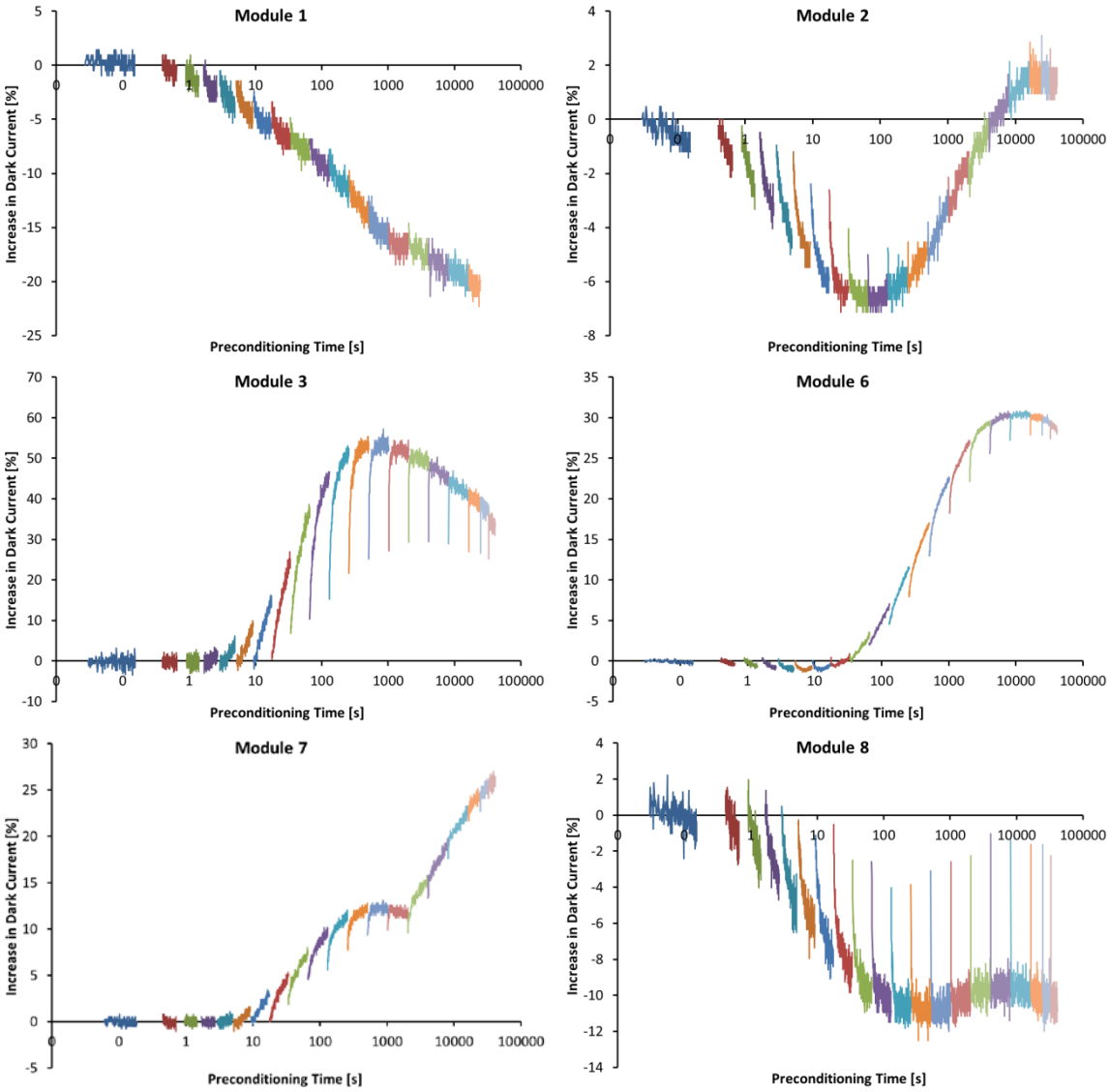


Figure 5-26: Change in the dark current during the preconditioning as a percentage. An increase indicates more current flow.

Each individual preconditioning step is displayed as a separate colour, and it can be seen that during the seconds that the C-V measurement is being performed a large relaxation of the dark current occurs. However, the current re-establishes its previous value relatively quickly and continues on with the slower timescale trend. The results show very clearly that the dark current can change in either direction, even for the same module the current can increase to begin with and then decrease (as in the case of module 3) or the it can do the opposite (as in the case of module 2). The dark current for

module 4b was also measured but is not shown because it remained almost constant. This might be expected since due to the high shunt conductance of this device the relative change in the current is much less, especially since the low Vmpp relative to the Voc means that the device was effectively being measured at a lower voltage, where the diode conductance is much lower.

The mechanisms discussed for the blue light effect both involve the reduction of a photocurrent barrier near to the interface of the absorber and the buffer. When this photocurrent barrier is reduced, either from reduction of the doping in a p+ layer or via photodoping of the buffer, we would expect the dark current to increase, and the crossover between the light and dark curves to be reduced. So, even though the performance is improving the dark current would be increasing which is not what would be expected if the changes in the device were primarily affecting the recombination rate These changes would affect primerally the open circuit voltage, in the light I-V curve and the effect of these changes on the dark current would be expected to be the opposite of the effect on the voltage, so that when Voc is increasing, the dark current would be decreasing. A final mechanism which could affect the dark current strongly is the presence of a back contact barrier.

From examining the curves in Figure 5-26 the variations in the Voc can often be seen as a reflection of the dark current, which would imply that the changes occurring at this point are due to changes in the recombination rate. When the changes in the dark current are not reflected in the Voc, for the most part they are increasing in a similar way to the fill factor, which indicates that at this point there is a reduction in a photocurrent barrier for the device. The correspondence of the dark current and N_A with the Voc and FF provides a potential method to track the preconditioning state of the module.

An interesting point to note is that the magnitude of the changes in the dark current do not seem to correspond to the magnitude of the light I-V performance changes. For example module 3 shows only small variations the light I-V performance even though the change in dark current is very large, at one point reaching over 50% higher than its initial value, indicating that in this case whatever is causing the increase in dark current has only a minor impact on the light I-V curve. The obvious candidate for this would be a non ohmic back contact barrier, since when the device is operating under illumination

a back contact diode would be operating under forward bias and hence have a relatively small impact, compared to when the device was under forward bias in the dark where it would be reversed biased and block the flow of current.

5.7 Conclusions

In this chapter it was shown that there are at least two distinct preconditioning effects that need to be addressed in performance measurements of any CIGS device. One of these effects was unexpected and was found to have received only brief mentions in the literature to date. It occurs on a faster timescale of milliseconds to seconds and relaxes on the timescale of hundreds of milliseconds to tens of seconds. This faster timescale effect was observed on all modules but in most was small enough to have negligible effect on performance measurements. However on some modules the effect was much stronger and does represent a significant measurement problem. It was found that this problem could be eliminated or alleviated by applying a forward voltage bias until immediately before the measurement. The other preconditioning effect seems to correspond to the one usually reported in literature and occurs on a longer timescale. Both effects were seen to occur with a stretched exponential behaviour so that the changes occur equally over several orders of magnitude in time. This has significant implications for preconditioning routines. Often relaxation of preconditioning effects could start to occur within the period between the end of the preconditioning and the measurement, particularly for light soaking where a cooling period is usually required. This relaxation would often be overlooked because subsequent relaxation occurs over a much longer time period. In order to obtain repeatable results the observed kinetics suggest that the timings of both preconditioning and relaxation should be controlled and that the errors in each time should be small compared to the actual time. Measurements of the dark current and C-V during electrical bias preconditioning provide an interesting insight in the processes occurring during the preconditioning, suggesting that more than one effect is responsible for slower timescale preconditioning in CIGS. The capacitance changes indicate that there is a change in the accumulation of charge at or near the interface which occurs as well as the change in doping density.

In the next chapter the theoretical models for preconditioning in CIGS will be discussed and compared to the observations in the chapter including the stretched exponential kinetics and the change in charge near the junction.

6 Causes of preconditioning in CIGS

6.1 Introduction

From the point of view of device measurement it is not possible to have confidence that a particular preconditioning routine gives a good representation of outdoor operation without a proper understanding of what is happening. Currently the only way to achieve this confidence is by comparison with good quality outdoor measurements, but this should be done for each module type separately and if any processing changes are made it may be necessary to repeat the comparison. Preconditioning routines are often developed empirically and separately by different module manufacturers. A much better situation would be a proper understanding of the underlying effects, which could give confidence that the measurement routine is fit for purpose. This would potentially lead to a universally applicable routine for all CIGS photovoltaic devices, and eventual standardisation.

Significant effort has been made by the international research community to elucidate the causes of metastabilities in CIGS. Despite these efforts this topic is still very much debated, although some models have gained significant theoretical and experimental support. Understandably most of the work in this field has been done on small scale lab devices for the purpose of understanding the fundamental device physics. The results are usually framed in the context of improving device performance, with little discussion of the impact on device measurement.

In this chapter the theories regarding preconditioning in CIGS are examined in more detail. Based on some of the most likely theories, models for the rates of preconditioning and relaxation are developed, and compared to the experimental results of the previous chapter. The different origins of metastability are discussed in the context of preconditioning routines to develop an understanding of the applicability of different methods in each case.

6.2 Electronic properties of CIGS devices

As well as the metastabilities, many other aspects of the electronic properties of CIGS devices are controversial. These issues are intimately related to the topic of metastabilities. This section reviews the information of this topic, highlights the areas which are still under debate and makes links between these issues and to the

metastable phenomena. Figure 6-1 shows a schematic representation of those links. The observables are represented in colour, with rings encompassing the different models which can explain them. Each of the links represented by the dashed line will be made clear in the discussion.

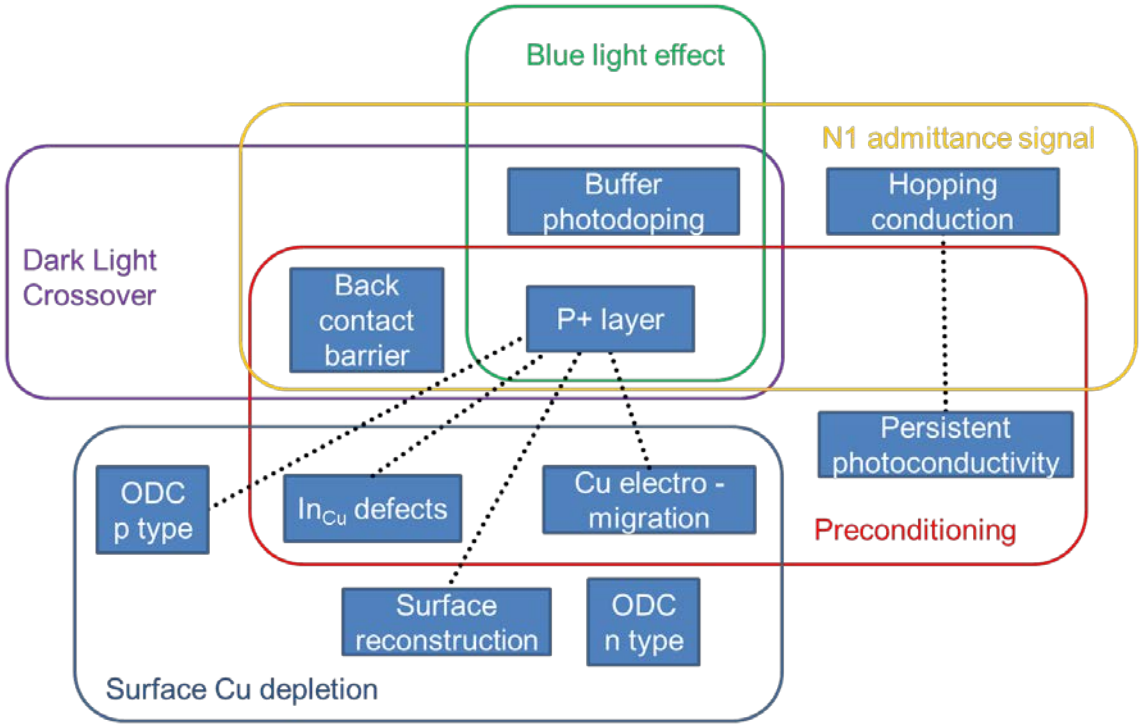


Figure 6-1: Schematic relation of different observables in CIGS and the possible explanations for those observables.

6.2.1 N1 admittance signal

Admittance spectroscopy is a measurement technique often used to measure the energy levels and concentrations of shallow defect states. In this technique, the capacitance of the device is measured as a function of frequency and temperature. Trap states in the device fill up and empty in response to the applied ac voltage, adding to the capacitance of the device. At low temperatures or high frequencies the emission from the traps is too slow and the trap states cease to be able to respond, and hence store charge. As this transition occurs a characteristic step reduction in the capacitance can be observed, the relation between the frequency (ω_i) and temperature (T_i) of the inflection point of this step can be used to calculate the energy level of the trap (E_T) according to

$$\ln\left(\frac{\omega_i}{T_i^2}\right) = \frac{-E_T}{kT_i} + \ln(\sigma\gamma) \qquad 6.1$$

Where σ is the capture cross section for the trap, and γ is a constant related to the effective band edge density of states. Figure 6-2 shows an example of admittance spectroscopy data for a solution processed CIGS device fabricated at CREST [87].

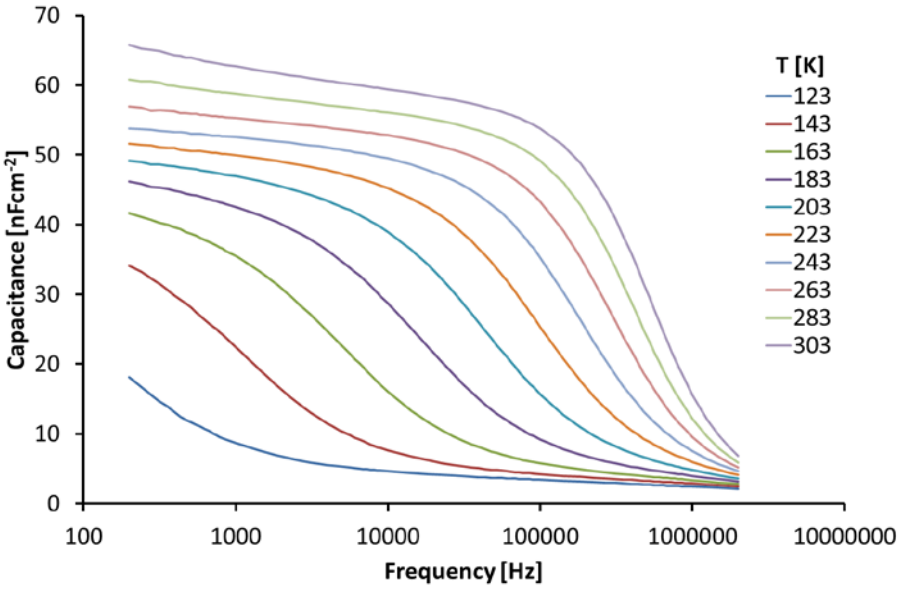


Figure 6-2: Admittance spectroscopy data for a CIGS cell showing the N1 admittance step.

In CIGS devices, the most commonly observed capacitance step has been named the N1 admittance signal. It shows several unusual properties, which are not consistent with the standard interpretation as a shallow trap state.

The N1 admittance signal is a heavily debated subject and an important one because the different interpretations imply different electronic origins and each of those origins has different consequences for the device. The N1 signal itself also displays metastable behaviour, implying a possible relation to the preconditioning effect [88].

The N1 trap state is not always observed at the same energy, rather it is seen to vary between different devices and even in the same device depending on the preconditioning state, or after air annealing. The N1 energy is usually seen between 40 and 200 meV but the activation energy of the signal and the emission pre-factor are experimentally seen to follow the Meyer-Neldel rule [89]

$$\frac{\sigma}{\sigma_0} = \exp\left(\frac{E_T}{E_{char}}\right) \qquad 6.2$$

Where σ_0 and E_{char} are constants that characterise the N1 signal. Figure 6-3 shows the logarithm of the pre-exponential factor against the activation energy for a variety of devices from several papers. All of the data points were considered by the authors to correspond to the N1 signal. The Meyer-Neldel rule is that these should all fit on a straight line, so the data show a reasonable amount of spread from this.

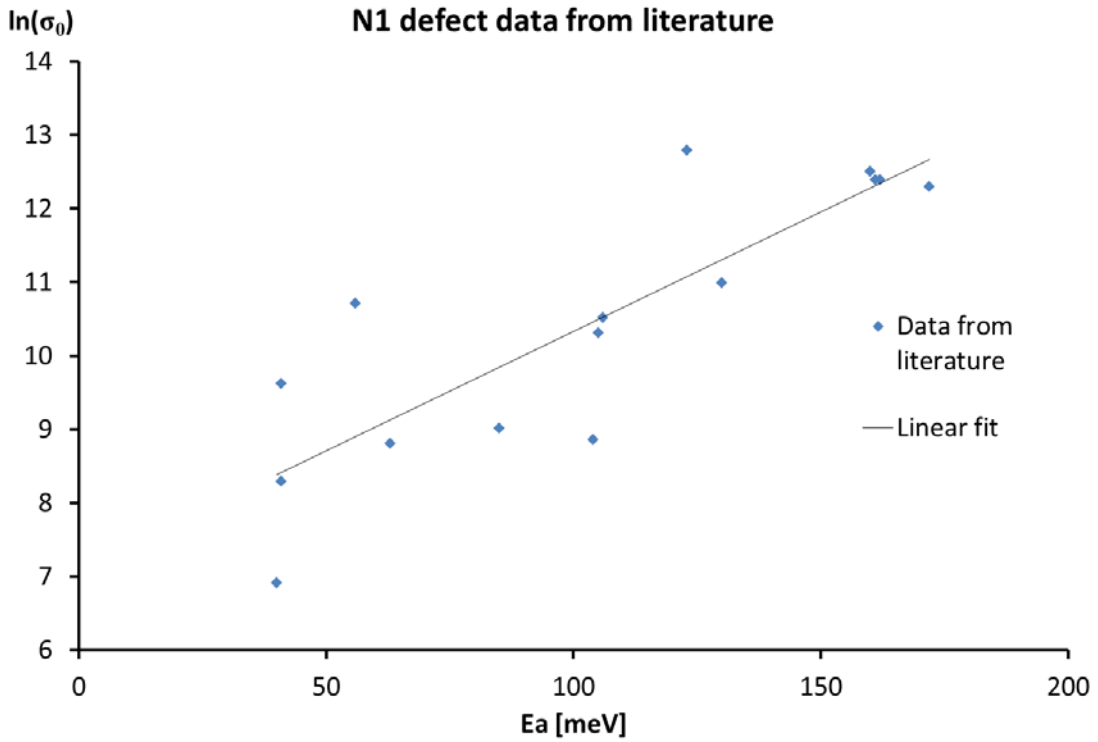


Figure 6-3: Data classified as the N1 defect taken from literature [64,88,90] along with the corresponding linear fit. The linear fit is not that precise, which might be a cause for concern.

The main different theories relating to the origin of the N1 signal are:

i) A bulk trap state as in the classic interpretation.

ii) Minority carrier traps in the inversion region.

iii) Back contact barrier.

iv) Mobility freeze out due to onset of hopping conduction.

The signal was identified as originating from minority carrier traps in the inversion region because it was observed that the N1 admittance signal shifted continuously in energy with air annealing [90]. This immediately implies that the signal is not a bulk signal and is more likely an interface signal. Deep level transient spectroscopy (DLTS) measurements were made to try and observe the corresponding defect using this technique. No majority carrier signal could be observed but a minority carrier signal was seen in DLTS spectra which corresponded to the N1 signal and shifted in the same

manner with annealing. The DLTS spectra were only seen when a small optical filling pulse was used, instead of the more usual larger electrical filling pulse. This is expected from interface states because the emission can be from a broad range of energy levels if a large filling pulse is used. The interpretations of these results lead to the hypothesis that the N1 admittance signal is due to the capacitance signal from minority carrier traps in the inversion region very close to the interface. In this hypothesis the activation energy of the N1 signal corresponds to the distance between the Fermi level and the conduction band at the absorber surface, which provides a very useful method to measure this quantity. This theory supports directly the p+ layer model [62].

Drive level capacitance profiling (DLCP) is another capacitance spectroscopy technique which makes use of varying the size of the oscillating excitation voltage. By changing the size of this voltage and increasing it to voltages above the small excitation range it is possible to obtain the density of states within the bandgap as a function of both energy and spatial position. This technique is relatively insensitive to the presence of interface states, so if the N1 signal is coming from minority carrier traps close to the interface then it should not show up in DLCP measurements. However DLCP investigations did show the presence of the N1 signal, which strongly suggests that the signal is not from interface states after all [91].

Further evidence against the N1 signal as a minority carrier signal in the inversion region comes from the size of the capacitance step compared to buffer layer thickness. If the signal were from a minority carriers at the interface, the size of the capacitance step is expected to relate to the size of the buffer layer - however no correspondence was found [64]. An alternative theory was proposed where the N1 signal originates from a non ohmic back contact. In has also been shown that a back contact barrier can cause a DLTS signal [92].

The final theory for the origin of the N1 is a freeze-out of carrier mobility due to a transition to variable range hopping as the conduction mechanism [93]. Variable range hopping is a conduction mechanism which occurs in disordered semiconductors, whereby charge carriers tunnel between different localised defect states rather than moving freely in the valence and conduction bands. In the limit of very low temperatures, hopping conduction becomes the dominant conduction mechanism for all semiconductors, however it is also observed at higher temperatures for disordered

systems [94]. Hopping conduction has been observed in CIGS in the same temperature range in which admittance spectroscopy measurements are made [95,96]. It has been demonstrated that the freeze out of mobility due to variable range hopping creates an admittance signal that can explain the observed N1 signal and gives an extremely good fit to the data for their measured sample [93]. They also show that conductance vs frequency measurements at temperatures below the step confirm that the sample is in the variable range hopping regime. The activation energy in this case is related to the density of states around the Fermi level [93]. Variation in the doping density due to preconditioning would change the activation energy of this step due to changing Fermi level and therefor the density of states around the Fermi level.

Each of these theories has different implications for the device. A back contact barrier, and a large concentration of traps at the interface could both reduce fill factor of the device and cause the cross-over of dark and light I-Vs. If the N1 signal is due to hopping conduction then the change in activation energy of the signal most likely relates to a change in conductivity of the film, due to a change in the net doping.

6.2.2 Cross over of dark and light I-Vs

CIGS devices usually display a crossover of the dark and light I-V curves, an example of which is shown in Figure 6-4.

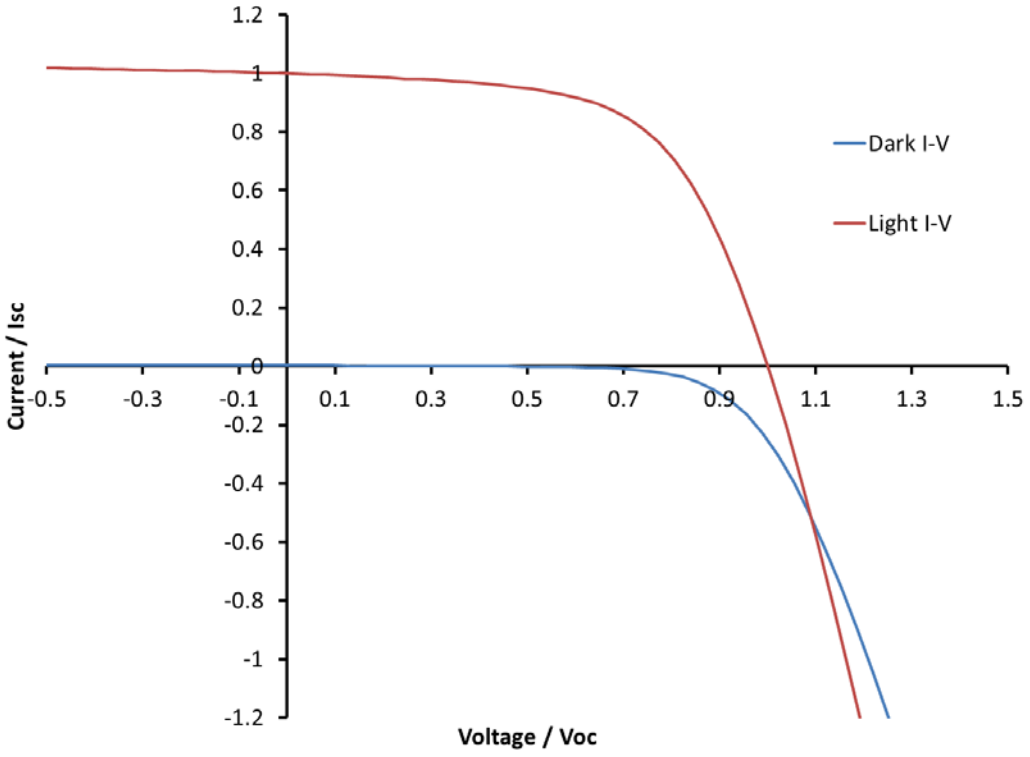


Figure 6-4: Example of the crossover of dark and light I-V curves for a CIGS device. The particular device measured was a solution processed CIGS cell made at CREST [87].

This crossover is a strong violation of the superposition principle. The main theories for the origin of this effect are:

i) Photodoping of the buffer layer and accompanying reduction of the size of the current barrier, caused by a conduction band spike [55].
ii) Reduction of the doping of a p+ layer at the surface of the absorber due to capture of holes photogenerated in the buffer layer [62].
iii) A non ohmic back contact [64].

In both the buffer photodoping model and the p+ layer model, the dark-light crossover is related to the blue light effect, and were previously introduced in this context in section 3.2.3. In both cases it is the blue photons absorbed in the buffer layer that cause the crossover, which was demonstrated experimentally by showing that the crossover is not present if the devices are measured using only red light illumination [55].

A non-ohmic back contact was previously dismissed as the cause of the crossover due to measurements demonstrating its ohmic nature [97]. However this explanation has regained support recently due to its ability to also explain the N1 admittance step. In this model, a second diode at the back of the device blocks the flow of dark current.

The origin of this crossover is particularly relevant for preconditioning. The dark current is seen to change significantly during the preconditioning. All of the theories for the origin of the crossover could also result in a reduction of fill factor, so even without knowing which theory is correct, there is an expectation that there might be a link between the crossover and fill factor changes during preconditioning as was observed in the preconditioning results of the previous chapter.

6.2.3 Origin of the Copper depleted surface region

The surface of the CIGS layer in films and devices is often seen to be copper depleted. The stoichiometry of the surface has been shown to be roughly 1:3:5 [Cu:In+Ga:Se] and n type conductive with a bandgap of about 1.3eV [98]. These results agree well with first principles calculation for the ordering of defect pairs [99]. This leads to the theory that the p-n junction in CIGS devices occurs not between the CdS and the CIGS but rather between the CIGS and an n type defect layer which spontaneously forms on the

surface. This theory is in contrast to the p+ layer model where the defect layer is expected to be strongly p type. Further evidence for an n type defect layer comes from kelvin probe microscopy [100]. Grazing angle X-ray diffraction (XRD) shows a larger ODC with a width of 5 to 60nm depending on the Cu content of the film [101].

An alternative theory is that the copper depletion is actually a surface reconstruction rather than a separate phase forming on the surface. First principles analysis predicts that this happens and leads to spontaneous faceting [102]. Hard X-ray photoelectron spectroscopy (XPS) supports the surface reconstruction model [103], as does angle-dependent soft x-ray emission spectroscopy (AXES) [104], angle-dependant XPS [105], and photoelectron spectroscopy with imaging tunnelling spectroscopy [106]. In this model, the observed n type surface is due to band bending caused by positive surface charge. This observation is particularly relevant in regard to the p+ layer model mentioned previously, since in that model the defected ODC layer takes a central role. An alternative explanation is that the p+ layer which is still compatible with the surface reconstruction model is that is result of relaxing metastable In_{Cu} defects rather than a separate phase [49,107]. If this is the case then the p+ layer would probably not have a reduced valence band maximum compared to the bulk CIGS.

One further option is that the copper depletion could be due to electro-migration of the charged Cu ions under the electric field of the junction. If this is the case, the Cu ions would be expected to flow reversibly upon application and removal of electrical bias, and this has been proposed as an origin of metastabilities [60,108]. This electro-migration of copper is yet another possible explanation for the p+ layer since either the Cu_i^+ ions move away from the surface or V_{Cu}^- move towards it.

The discussion of the controversial electronic properties of CIGS devices shows that there are many links between different aspects and theories, and links to the origin of metastable performance change which will now be discussed.

6.3 Origins of performance change

When considering the cause of the performance changes in CIGS it is constructive to split the origin of the problem into two parts, first of all change in the electronic properties within the device, and secondly the microscopic alteration which drives that change. For example, a change in size of a current barrier at the back contact can be

considered a change in the electronic transport within a device and the microscopic change which causes this could, for example, be a metastable defect changing state from a donor to an acceptor. Given the range of different types of metastable changes that occur in CIGS devices, there may be an interaction of different electronic transport changes and/or different microscopic changes causing them. There are a large number of variables and different processing methods for making CIGS devices, so it should not necessarily be expected that loss mechanisms affecting one device will affect another device in the same way. In this section, the various electronic transport loss mechanisms that have been proposed as potential origins of metastable performance changes are discussed, these changes are then investigated in relation to the various proposed microscopic changes which could be causing them.

6.3.1 Electronic transport mechanisms potentially causing metastabilities

Some of the important aspects of electronic transport within the device that could be related to metastable effects are shown in Table 6-1 along with the performance parameters they would be expected to most affect.

Table 6-1: Aspects of CIGS devices which could cause metastable changes in the device along with the effects they would be expected to cause on the performance of the device.

Device Change	Effects
Recombination rate [7]	Voc, Jsc
Ohmic losses [7]	FF
Shallow doping density / built-in voltage [33,109,110]	Voc
p+ layer doping [49,62,107,111]	FF, Voc, Dark IV
Photodoping of the buffer layer [54,112]	FF
Size of a back contact barrier [88]	Dark IV, FF

The metastable changes related to the red light effect are caused, at least in part, by persistent photoconductivity of the absorber layer, where the increase in conductivity is due to an increase in net doping [33,58,59,113]. Whether an increase in doping causes an increase or a decrease in the voltage of a device depends on the dominant recombination mechanism. If space charge region recombination is dominant, then the voltage will increase as the doping increases, however if the device is interface recombination dominated, then the voltage of the device will decrease [109]. Investigation of SCR recombination dominated devices has shown that changes in

capacitance and voltage correspond, agreeing with the hypothesis that they are both due to changes in the doping [33][110].

The primary effect of changing doping density would be expected to be on the voltage, whereas the most significant change seen in the preconditioning was in the fill factor. For this reason changes in the doping density cannot fully explain the observed preconditioning behaviour without some other linked effect. The changes in fill factor seen in photovoltaic modules could come from either changes in the Ohmic losses or changes in a current barrier. There are several reasons to think there is a current barrier located close to the absorber buffer interface, and that the barrier is modulated by capture of charge. The first reason is that the blue light effect, which increases the fill factor, occurs for light which is absorbed in the buffer layer. As discussed, there are two main theories for this, based on either a p+ layer in the absorber or a conduction band offset. The model of a non ohmic back contact of changing size could also theoretically explain changes in fill factor and dark current, but not the connection with the blue light effect. The support for this model comes mainly from theory that the N1 admittance signal is due to a back contact barrier, however as discussed there are several different interpretations of this barrier.

It is sometimes stated as an argument against the conduction band spike model that the required photodoping of the buffer would lead to an increase in capacitance, whereas observations of the blue light effect cause a decrease in the capacitance [53,114]. This is not necessarily the case: The net doping of the buffer effectively increases from photodoping upon light exposure. Equation 5.5 gave the capacitance for an absorber buffer window heterostructure device under the conditions of a depleted buffer layer. From this equation we can see that if the doping density of the buffer increases then the capacitance should go down. Figure 6-5 shows a SCAPS simulation confirming this, the figure also shows that the fill factor increases with photodoping in the same device model. If the buffer doping is increased still further, then an increase in capacitance can be seen in the SCAPS model, which might be the reason for that it is sometimes stated that this model would always cause the capacitance to go up.

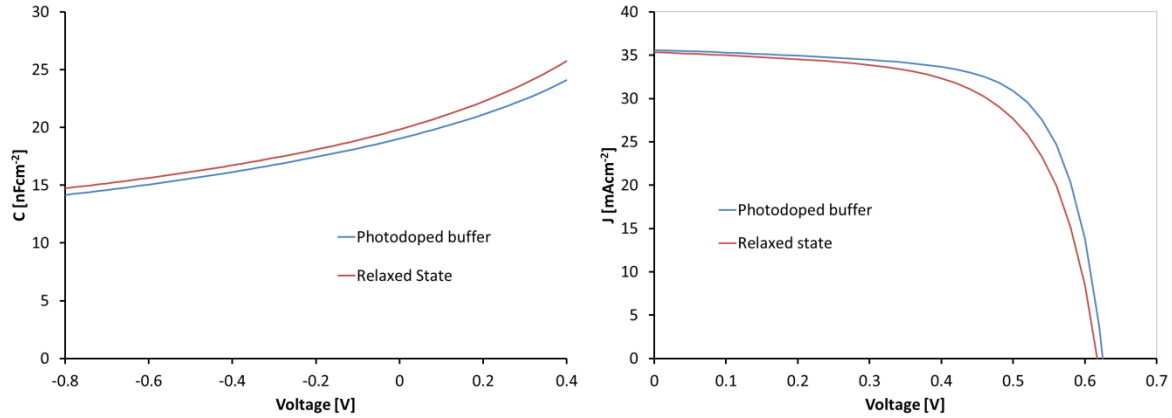


Figure 6-5: SCAPS simulation for a the effect of photodoping in the buffer layer on the C-V and I-V characteristics of a device with a conduction band spike offset at the absorber–buffer interface.

A different argument against the buffer photodoping is that the blue light effect occurs in a variety of different buffer types. It might be possible that strong photodoping is a general feature of all the buffer materials tried but it seems more likely that the change is occurring in the absorber layer. Evidence from electron beam induced current (EBIC) measurements adds support for this theory since the EBIC increases significantly when the region in the absorber close to the junction is bombarded heavily with electrons, indicating that a metastable change occurs due to holes generated in the absorber [111]. The fill factor enhancements seen during the electrical bias preconditioning cannot be explained by photodoping of the buffer, because electrical bias would not cause any significant increase of hole concentration in the buffer, however capture of positive charge in a p+ layer at the surface of the absorber could be active during forward bias and agrees furthermore would cause the decrease in capacitance observed in section 5.6. Changes in the doping in the bulk of the device could cause changes in the band bending, and therefore changes in the charge stored in the p+ layer, providing an explanation how changes in the doping density could affect so strongly the fill factor of the device.

In summary, there appear to be at least two effects occurring: One due to a change in doping in the bulk of the absorber layer, the other is more controversial but the evidence support a capture of positive charge near the absorber–buffer interface either in the absorber itself, or a thin ODC layer. It is also possible that other effects such as changes in a back contact barrier are also occurring.

6.3.2 Microscopic causes of preconditioning

There are several different possible microscopic origins which could be occurring to cause the metastabilities observed in a CIGS device and they could be affecting the device through any of the different electronic changes discussed above.

Metastable point defects seem like the most plausible explanation for some of the observed metastabilities, but several other mechanisms have been proposed including the reversible migration of copper [60,61] or other mobile species [115], continuum of trap states in the absorber junction [32], photodoping of the buffer layer [54].

Experiments have shown that the persistent photoconductivity observed in CIGS is due to conversion of metastable defects. Experimentally it has not been possible to determine the precise nature of that point defect but its properties correspond well with density functional theory calculations of the V_{Cu}-V_{Se} defect [65]. There is experimental support for the presence of this defect in CIGS films from positron annihilation spectroscopy [116,117].

From similar calculations, the In_{Cu} defect and the complexes In_{Cu}-V_{Cu}, In_{Cu}-$2V_{Cu}$ should display metastable behaviour similar to the DX centre in III-V semiconductors [67]. This defect converts between a shallow acceptor and a deep neutral state. This defect is particularly relevant in relation to the p+ layer model since it is predicted to take an acceptor state close to the junction, but convert back to a neutral state without activation energy upon capture of free holes. Thus this defect is a potential mechanism for the change in size of a p+ barrier at the junction. It is able to explain the red on bias metastability, the blue light effect, and the dark-light crossover.

Electron paramagnetic spin resonance studies in $CuGaSe_2$ also indicate that both the V_{Se} and Ga_{Cu}-$2V_{Cu}$ defects are metastable [118]. Photocapacitance measurements also hint that the optical level observed at 0.8eV above the valence band, irrespective of Ga content, belong to a metastable defect [119].

Metastable defects are able to explain the very slow kinetics of preconditioning and the subsequent relaxation. The V_{Se}-V_{Cu} defect in particular is able to explain these timescales as will be shown in section 6.5.2. However, this defect should affect primarily the doping in the bulk of the device rather than at the interface, so initially it would be expected to affect the voltage rather than the fill factor. However, the doping in the base

would affect the band banding and could alter the amount of charge in a p+ layer at the interface.

No specific mechanism has been proposed for metastability of a back contact barrier. However, it should be noted that a layer of $MoSe_2$ usually forms between the CIGS and Mo back contact, and that persistent photoconductivity has been observed in $MoSe_2$ in a different context [13].

The case of the ms timescale preconditioning observed in this thesis could also be due to metastable defects, or to more conventional carrier capture by deep states.

Copper diffusion has also been suggested as a potential cause of metastabilities in CIGS devices [60,61]. Using radio isotope methods it has been shown that copper ions are mobile in the film and that under the influence of an electric field they can electromigrate [61]. The migration under the junction field pushes the copper away from the surface which is why it was also proposed as the reason for the copper depleted surfaces observed in Cu poor films. Since copper vacancies are thought to be shallow acceptors, Cu depletion in the junction region could be responsible for the p+ region. It was also suggested that reversible migration could occur due to the changing field of the junction as bias is applied and removed from the junction. This model is not compatible with the blue light effect since this effect occurs without thermal activation [53]. So if this effect is occurring it would be in addition to the blue light effect.

On analysis of the available body of knowledge, metastable point defects are the most probable cause of the metastabilities in CIGS photovoltaics devices. These defects cause a change in the net doping in the bulk of the device and a change of charge stored in a highly charged p+ layer close to the junction. A combination of the V_{Se}-V_{Cu} defect and variants of the In_{Cu} defect are able to explain the observed phenomenon well, but direct evidence of their implication is missing.

6.4 Metastable defects in CIGS

From first principles calculations two different types of defect have been predicted to display metastable behaviour and have low enough formation energy to occur in significant quantities in CIGS films. The first of these is the V_{Se}-V_{Cu} defect [65] and the second is the In_{Cu}-$2V_{Cu}$ [67]. In both cases the complexing of the defect with the V_{Cu} is predicted to decrease the formation energy, but the other variants of these defects V_{Se},

In_{Cu}-V_{Cu} and In_{Cu} are also predicted to show metastable behaviour and to be present in the device.

6.4.1 Se-Cu di-vacancy (V_{Se}-V_{Cu})

The V_{Se}-V_{Cu} (VV) defect can take two different configurations. These configurations involve a rearrangement of the lattice and hence there is an energy barrier for the transition. The configuration coordinate diagram in Figure 6-6 shows how the energy of the system varies depending on the distance between the two Indium atoms around the defect ($d_{In\text{-}In}$).

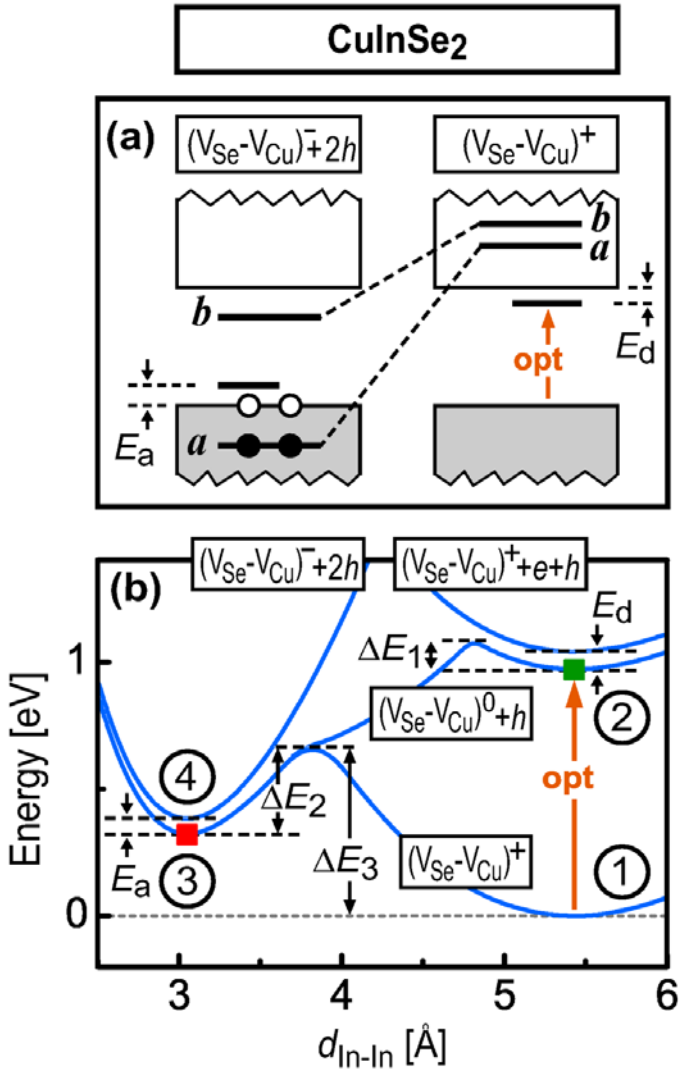


Figure 6-6: Schematic energy level diagram and Configuration coordinate diagram for the V_{Se}-V_{Cu} defect in $CuInSe_2$. Reprinted from [65] with the permission of AIP Publishing. The green and red squares represent the relaxed In-In distances of the donor and acceptor configurations respectively. E_d and E_a are the shallow donor and shallow acceptor energy levels.

In one configuration state, the defect is a shallow acceptor with $d_{In-In} \approx 3$ Å. The points marked 3 and 4 on the diagram represent the neutral and charged state of this configuration. The other configuration state is a compensating donor with $d_{In-In} \approx 5$ Å,

represented by points 1 (charged) and 2 (neutral). The energy levels a and b are the bonding and antibonding levels formed from the two dangling In bonds. Population of the bonding level pulls the In atoms together into the acceptor configuration, whereas depopulation causes the In atoms to move apart into the donor configuration. When the Fermi level is below the transition level ε(+/-) the equilibrium state of the defect is the donor state, and when the Fermi level is above the transition level the acceptor state is the equilibrium state. Because of the activation energy for the conversion, the defect is able to exist metastably in the non-equilibrium state. Under operating conditions, the state of the defect depends on the electron and hole concentrations. If the acceptor and donor states of the defect level are labelled VV^- and VV^+ respectively then the equations for the dominant forward and reverse reactions can be written

$$VV^+ + e^- \rightarrow VV^- + h^+ \qquad 6.3$$

$$VV^- + 2h^+ \rightarrow VV^+ \qquad 6.4$$

The activation energies for each reaction are respectively ΔE_1 and ΔE_2. However the activation energies vary for different compositions. Their calculated values in pure CIS and CGS are shown in Table 6-2 along with the transition energies. Note in particular that the activation energy ΔE_1 vanishes for CGS and high Ga content CIGS.

Table 6-2: Theoretically calculated activation energies and Transition energy for the V_{Se}-V_{Cu} defect.

	CIS	**CGS**
ΔE_1	0.1	0
ΔE_2	0.35	0.28
ε(+/-)	Ev+0.19	Ev+0.32

Experimentally, the activation energies for the increase in photoconductivity in films, and capacitance in devices, has been found as $\Delta E_1 < 0.1$ and $\Delta E_2 = 0.35$ [86]; and $\Delta E_2 = 0.2$ to 0.3 using thermally stimulated capacitance measurements [120].

The equilibrium state in the dark in the bulk p type region is the donor state VV^+, which acts to compensate the acceptor doping in the layer. On illumination the electron concentration increases dramatically and transition 6.3 dominates, causing the shallow acceptor state VV^- to become the stable state. This increases the net doping density in the bulk of the absorber. Nearer to the junction where the electron concentration is higher, the equilibrium state of the defect in the dark is already the acceptor form. The

acceptor form of the defect has an additional VV^{2-} charge state with a transition energy close the conduction band. Near to the junction, the defect could exist in this state and either cause or contribute towards the p+ layer. It was originally proposed [65] that this defect could be responsible for the blue light effect, since blue light is absorbed primarily in the buffer layer and holes created in the buffer layer drift into the CIGS layer, increasing the hole concentration near the junction and decreasing the acceptor concentration there via transition 6.4. However, as will be discussed in the next section, this is unlikely to make any significant change in the distribution of defect configurations and the In_{Cu} / Ga_{Cu} defects seems to be a more likely responsible candidate for the blue light effect.

6.4.2 III_{Cu} defect

The III_{Cu} defects (In_{Cu} or Ga_{Cu}) are metastable defects that have also been theoretically predicted in CIGS. They take either a shallow substitution donor form (III_{Cu}^{2+}) or a deep neutral centre (III_{DX}^{0}), where the DX state is effectively formed as a Frenkel pair of III_i and a copper vacancy. They are also predicted to form defect complexes with V_{Cu} either as (III_{Cu}-V_{Cu}) or (III_{Cu}-$2V_{Cu}$). From thermodynamic calculations it is expected that the last of these is the prevalent form, however the properties of all three defect types are predicted to be similar except for the change in charge state for the addition of V_{Cu}^{-}. These defects are very plausible candidates for the cause of the p+ layer near the junction since they only take the acceptor/neutral (DX) form when the concentration of free electrons is high and the concentration of free holes is low, as is the case near to the junction. These defects have also been proposed as the reason that the efficiency of high gallium content and CGS films is lower than desired since the pinning level of the defect is expected to be closer to the middle of the bandgap in these devices. The configuration coordinate diagram for this defect is shown in Figure 6-7.

Igalson et al [53] have reported capacitance experiments that provide some evidence that this defect is contributing to a p+ layer and is responsible for the blue light effect. Blue light with energy above the bandgap of the buffer is absorbed in the buffer creating free carriers, some of the holes drift across the junction and increase the free hole concentration there. If there are In_{DX} states at the junction, the increase in hole density would cause some of them to convert to the shallow substitutional form, reducing the size of the p+ barrier and explaining why the fill factor is higher when measured with

white rather than red light. The defect is also thought to be responsible for the 'red on bias' metastability which is important because it cannot be explained by the V_{Se}-V_{Cu} defect [114].

The principle reaction for conversion to the DX state is double electron capture:

$$(\mathrm{In_{Cu}} - 2V_{\mathrm{Cu}})^0 + 2e^- \rightarrow (\mathrm{In_{DX}} - 2V_{\mathrm{Cu}})^{2-} \qquad 6.5$$

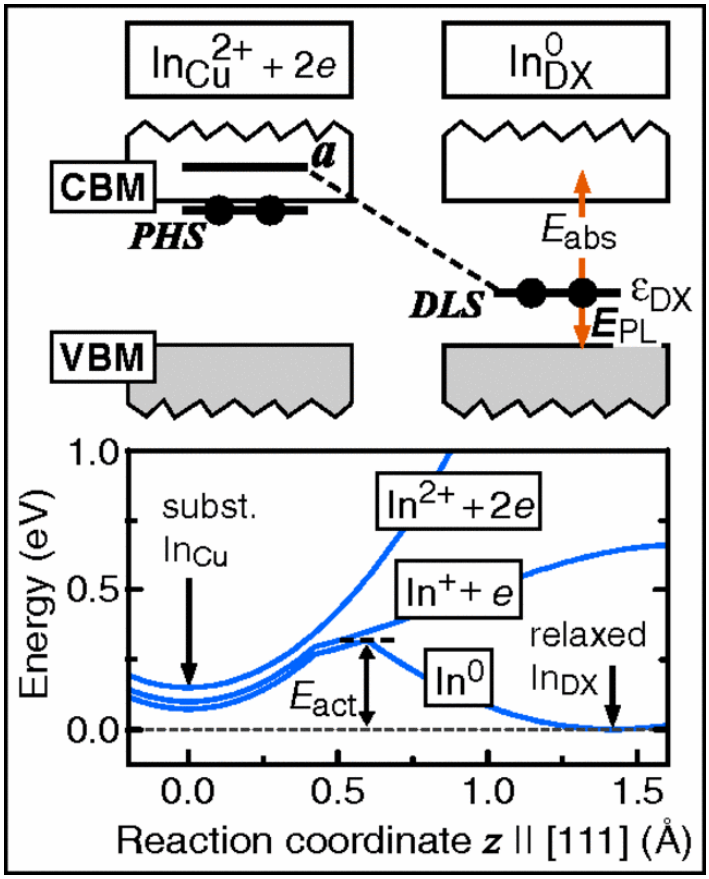


Figure 6-7: configuration coordinate diagram for the In_{Cu} defect, reused with permission from ref. [67]. The left represents the shallow purturbed host state (PHS) of the defect, and the right represents the deep defect localised state (DLS).

There are 3 mechanisms for the conversion of the DX centre to the donor configuration [67]:

1. Optical recombination with free holes $\mathrm{In_{DX}^0} + \mathrm{h^+} \rightarrow \mathrm{In_{DX}^+}$ and subsequent lattice relaxation.
2. Optical absorption of trapped electrons to the conduction band $\mathrm{In_{DX}^0} \rightarrow \mathrm{In_{DX}^+} + e^-$ and subsequent lattice relaxation.
3. Activation of a structural energy barrier and simultaneous electron emission.

The optical recombination with free holes is the reaction that can explain the blue light effect, since via this reaction the acceptor density close to the junction can be reduced when blue light is applied, increasing the number of holes at the junction. The overall equation for this reaction pathway is

$$(\mathrm{In_{Cu}} - 2V_{\mathrm{Cu}})^{2-} + h^{+} \rightarrow (\mathrm{In_{Cu}} - 2V_{\mathrm{Cu}})^{0} + e^{-} \qquad 6.6$$

Whereas for the other two pathways the overall reaction is

$$(\mathrm{In_{Cu}} - 2V_{\mathrm{Cu}})^{2-} \rightarrow (\mathrm{In_{Cu}} - 2V_{\mathrm{Cu}})^{0} + 2e^{-} \qquad 6.7$$

6.5 Kinetics

In this section the observed kinetics of the process are compared to the predictions from the V_{Cu}-V_{Se} and In_{Cu} defects. If the preconditioning is being caused by transitions in defect states then the kinetics of the preconditioning and the defect transitions would be expected to be intimately linked. Transition rate models for both the defect types are created and compared to the preconditioning and relaxation rates observed experimentally for the modules. The default values of various device parameters used to model the rate equations are shown in Table 6-3 along with the reference they were taken from where applicable.

Table 6-3: Parameters used for modelling of the defect transition rates.

Generic		
Parameter	**Value**	**Ref**
Vth	10^7 cm s^{-1}	[65]
ν_{ph}	$5*10^{12}$ s^{-1}	[81]
E_g	1.2 eV	[81]
Nc	$7*10^{17}$ cm^{-2}	[81]
Nv	$1.5*10^{19}$ cm-	[81]
n_i^2	$7*10^{16}$	calculated
ΔE_F	0.55 eV	
N_a	$4*10^{15}$ cm^{-3}	[65]

V_{Cu}-V_{Se} defect parameters		
Parameter	**Value**	**Ref**
σ_n	10^{-16} cm^2	
σ_p	10^{-16} cm^2	
ΔE_1	0.07 eV	[65]
ΔE_2	0.3 eV	[65]
N_{VV}	$0.1*N_a$	

6.5.1 Metastable defects kinetics

The rate equations for the conversion between different defect states need to be known in order to predict the behaviour of metastable defects. In Ref. [65], a model was proposed for the reaction rate which combined the capture/emission rate equations

usually used for trap states (used for example in the analysis of DLTS experiments) with the rate equation for reactions involving transitions over an activation barrier (used for example in modelling defect diffusion).

The reaction rate can then be given as by Decock et al, in a paper relating to the addition of metastability modelling to the simulation package SCAPS [121]

$$\tau^{-1} = \upsilon_{ph} exp\left(-\frac{\Delta E}{kT}\right) \prod_{x=1}^{m} \frac{\tau_{Px}^{-1}}{\upsilon_{ph}} \qquad 6.8$$

Where υ_{ph} is the phonon frequency, ΔE is the activation energy for the transition, the product is over each carrier capture/emission event that is involved in the rate limiting reaction step and τ_{Px}^{-1} is the transition rate associated with each capture emission process given by

$$\begin{aligned} \tau_{ec}^{-1} &= V_{th}\sigma_n n \\ \tau_{ee}^{-1} &= V_{th}\sigma_n N_c \\ \tau_{hc}^{-1} &= V_{th}\sigma_p p \\ \tau_{he}^{-1} &= V_{th}\sigma_p N_v \end{aligned} \qquad 6.9$$

Where n and p are the electron and hole densities, V_{th} is the thermal carrier velocity of the free carriers and σ_n, σ_p are the capture cross section for electrons and holes, respectively. Depending on the assumptions made about the number of carriers involved in the rate limiting reaction step, different equations are obtained.

The kinetics of metastable defects are often seen to be non-exponential, instead following a stretched exponential or sum of exponentials [12,85]. One possible explanation for this is the effect of alloy broadening. This is the case for the DX defect in the InGaAs alloy, where the degree of stretching is found to depend on the alloy composition with simple exponential kinetics for the binary limits GaAs and AlAs and maximum stretching occurring for the equal mix [122]. Careful measurement of that system revealed 4 different time constants that originate from the different number of Al atoms in the neighbourhood of a donor atom [12]. This mechanism would obviously be applicable to the CIGS system which is also an alloy system, so that the presence of Ga or In on different sites adjacent to the defect would be expected to affect the transition kinetics for that defect. Similar effects might be expected from other local

differences in the atomic configuration in the vicinity of the defect. An obvious example that has already been mentioned is the complexing of the defects with copper vacancies, another possibility is the presence of Sodium, which has been shown to strongly affect the metastable defect kinetics [123].

Aside from differences in the local atomic configuration around a defect, longer distance inhomogeneities in the film could contribute also to the non-exponential behaviour. It is known that bandgap and electrostatic fluctuations occur in CIGS devices [124]. These potential fluctuations cause local variations in the carrier concentrations, which would directly affect the rates of metastable defect transitions.

Since it has been shown experimentally that the free carrier density increases with light soaking or electrical bias, this leads to another theory for the non-exponential kinetics. As the defects convert from one state to another it changes the free carrier concentration, which in turn slows down the further progress of the transition [65].

6.5.2 Cu-Se di-vacancy kinetics

The donor to acceptor conversion of the V_{Cu}-V_{Se} defect occurs via electron capture, activation of an energy barrier, and hole emission. As mentioned in the previous section, different rate equations result depending on whether these processes occur simultaneously or step by step. From the calculations of Lany and Zunger [65] the electron capture and activation of the energy barrier should be simultaneous, followed by hole emission as a separate step. The transition rate equations then give.

$$\tau_{VV^{+}\rightarrow VV^{-}}^{-1} = V_{th} n \sigma exp\left(\frac{-\Delta E_1}{kT}\right) \qquad 6.10$$

In the SCAPS model [121] it is assumed that all transitions between metastable states occur via the simultaneous capture or emission of two carriers and activation over a thermal barrier. This assumption gives a different rate equation for transition 6.3

$$\tau_{VV^{+}\rightarrow VV^{-}}^{-1} = \frac{(V_{th}\sigma)^2 n N_v}{\upsilon_{ph}} exp\left(\frac{-\Delta E_1}{kT}\right) \qquad 6.11$$

Both equations have the same linear dependence on the electron concentration and the same activation energy but very different pre exponential factors and therefore rates. Using the device values from Table 6-3, the second case where the capture and emission are simultaneous is approximately 10^4 times slower than the case where the capture

and emission occur as separate steps. This is a significant difference which will have a strong impact on device models. Although either case might be possible in a physical defect, only the first case represents the defect as predicted by Lany and Zunger.

The rate equation for the transition 6.4 is

$$\tau_{VV^- \to VV^+}^{-1} = \frac{\left(V_{th} p \sigma_p\right)^2}{\nu_{ph}} exp\left(\frac{-\Delta E_2}{kT}\right) \quad 6.12$$

In this case the theoretical prediction is that simultaneous capture of two holes is necessary [65], so there is no contradiction with the assumptions made in the SCAPS model [121].

Setting up the rates for the forward and reverse transitions as a differential equation for the concentration of defects in each states gives.

$$\frac{d[VV^-]}{dt} = \tau_1^{-1}[VV^+] - \tau_2^{-1}[VV^-] \quad 6.13$$

In general the transition rates will depend on the concentration of free carriers which also depends on the concentration of acceptors. The concentrations of free carriers approximately obeys the relation

$$np = n_i^2 \exp\left(\frac{E_{Fn} - E_{Fp}}{kT}\right) \quad 6.14$$

Where n_i is the intrinsic carrier density. If it is also assumed that the concentration of holes is approximately equal to the stable shallow acceptor density minus the compensating donor density.

$$p = N_a + [VV^-] - [VV^+] \quad 6.15$$

Equations 6.14 and 6.15 can be substituted into the rate equations and the conversion of VV+ to VV- can be solved numerically. Assuming flat Fermi levels in the absorber layer, then n and p will be constant throughout the quasi neutral region. The value of the cross sections $\sigma_{n,}$ and σ_p used for the simulation was 10^{-16} cm^2. This is smaller than the estimate given by Lany and Zunger (10^{-15}cm^2) but gave a better agreement between the modelled rates and the observed preconditioning rate, whilst still remaining in a realistic range. The value of the activation energies was taken as a linear interpolation between the calculated values assuming Ga/(Ga+In)=0.3. The difference in quasi Fermi

levels used was 0.55V, a value approximately equal to the cell voltages used in the first electrical bias experiment, described in section 5.3. The shallow doping density (N_a) and the total density of the V_{Cu}-V_{Se} defects (N_{VV}) make a significant difference to the results. Figure 6-8 shows the results of the simulation for the conversion of defects to the acceptor state depending on the shallow acceptor density. The deep defect density is set to 10% of the shallow acceptor density in all cases.

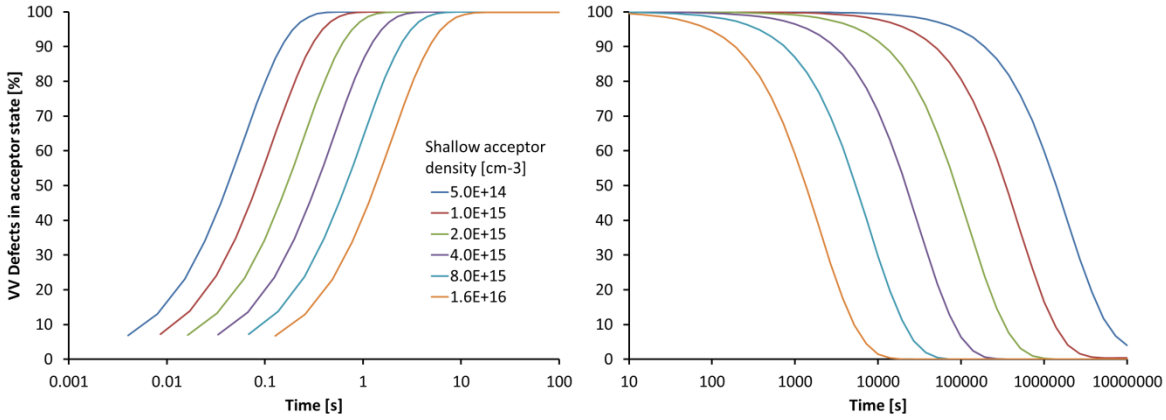


Figure 6-8: Effect of shallow acceptor density on the rate of V_{Cu}-V_{Se} state conversion during electrical bias preconditioning and subsequent relaxation.

The rate of the transition is slower for higher doping densities because there are fewer free electrons. As the total density of V_{Cu}-V_{Se} defects increases to values comparable to the shallow acceptor density, the conversion process starts to become stretched as seen in Figure 6-9.

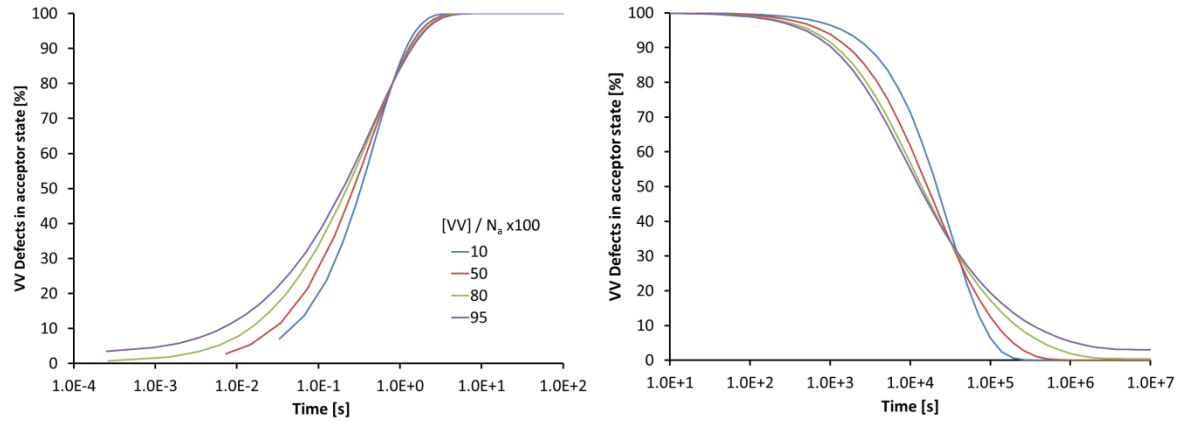


Figure 6-9: Effect of the density of V_{Cu}-V_{Se} defects on the rate of V_{Cu}-V_{Se} state conversion during electrical bias preconditioning and subsequent relaxation.

This is because the number of free electrons/holes starts to become heavily dependent on how many of the defects are in each state. This could be one of the reasons for the observed non-exponential behaviour, however in order to cause the stretching over a sufficient number of orders of magnitude of time the concentration of VV defects needs

to be a significant fraction of the doping density and the free hole concentration should be observed to increase very dramatically by at least an order of magnitude. The maximum increases in net doping seen from the C-V measurements in chapter 5 was 50%, which is lower than the levels expected if the stretching were to be caused by changes of the doping density. It should be noted that the doping density extracted from the C-V curve at room temperature will be heavily affected by the presence of deep defects and will not represent the true value, so it is still possible that the real change in doping density could be much larger than measured in chapter 5. It is possible to significantly improve this measurement in small scale devices by cooling the device down to cryogenic temperatures, so that the capture and emission from deep traps become too slow to respond. It may also be possible to use drive level capacitance profiling in place of C-V measurement. This technique yields a more accurate estimate of the doping density in small scale devices but has not been tried on full sized modules, so would require investigation to understand if there were complications from the module size. Both of these methods are interesting avenues for future research.

An alternative explanation for the stretching is a distribution of rate factors, which could be due to a distribution of activation energies and/or capture cross sections. The $CuInSe_2$ compound is expected to have $\Delta E_1 = 0.1$ and $CuGaSe_2$ to have $\Delta E_1 = 0$. So a distribution of activation energies between these two values in the mixed compound is a likely alternative to a single activation energy for all the defects. Figure 6-10 shows the change in the acceptor state of the VV defect for different values of the activation energy ΔE_1. The graph also shows that fraction of VV defects in the acceptor state if one quarter of the states have activation energies 0, 0.035, 0.07 and 0.1. The result reproduces the stretching behaviour well, and implies that this is the likely cause of the stretching.

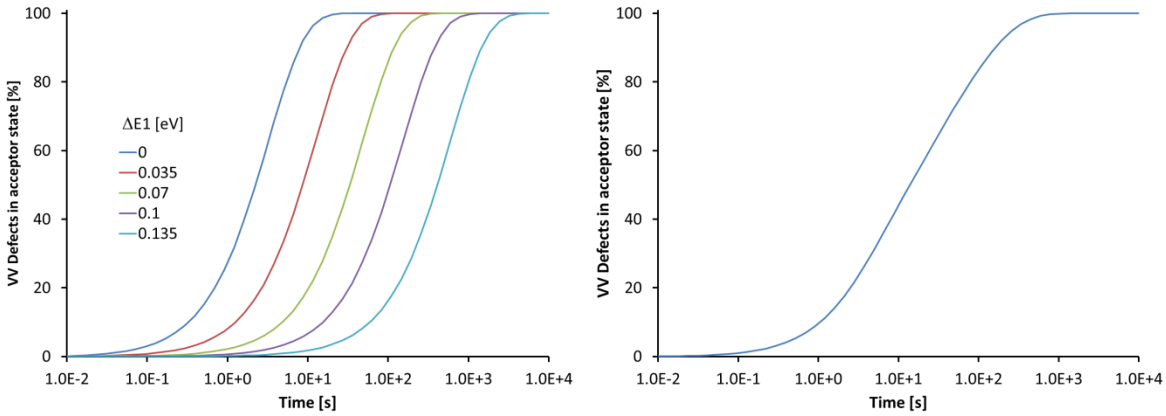


Figure 6-10: Effect of the activation energy for electron capture on the rate of the defect transition during electrial bias preconditioning. The left plot shows different discrete activation energies, the right plot is the average transition rate for a the defect when 1 quarter of the defects have activation energies of 0, 0.035, 0.07, 0.1 eV.

The stretching of the relaxation can be explained similarly by variations in the value of ΔE_2 as shown in Figure 6-11. The distribution of activation energies also offers an explanation for the observation that the relaxation time increases with preconditioning time [86]. This is because the In related defects have a higher activation energy for both the preconditioning and the relaxation. Therefore, compared to defects with Ga in the atomic neighbourhood, defects with In will take longer to convert to the acceptor state during preconditioning, and will also take longer to revert back to the donor state during the relaxation.

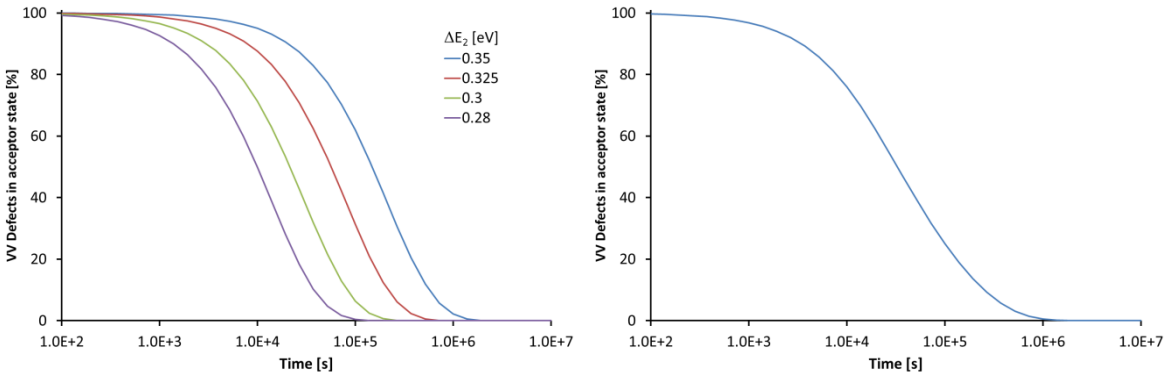


Figure 6-11: Effect of the activation energy for hole capture on the rate of the defect transition during relaxation subsequent to electrial bias. The left plot shows different discrete activation energies, the right plot is the average transition rate for a the defect when 1 quarter of the defects have activation energies of 0.28, 0.3, 0.325, 0.35 eV.

The rate model for transition of defects between the states corresponds reasonable with the experimental rates of preconditioning as shown in Figure 6-12. For the preconditioning the percentage of the defect in the acceptor state roughly follows the observed increase in power for module 1. Whereas for the relaxation the model is

somewhat slower than the observation but similar to module 5 which was the slowest relaxing. An extremely useful suggestion for further work would be a more quantitative model. This would require careful analysis of the doping densities before and after preconditioning which might then allow the extraction of the capture cross sections and the spread of activation energies. These values would be extremely useful for device modelling.

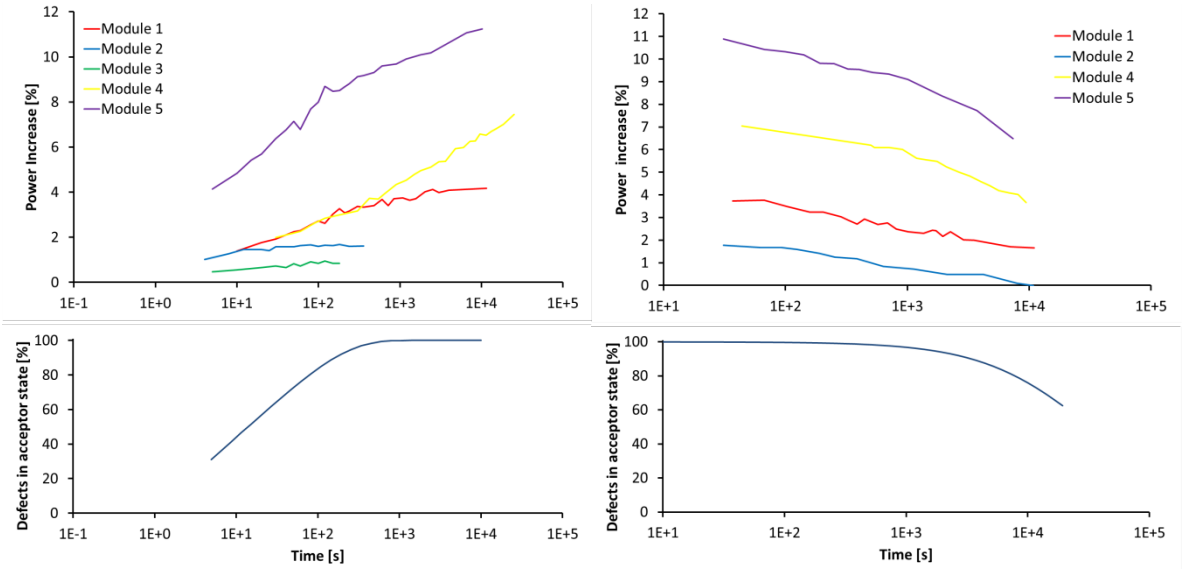


Figure 6-12: Comparison of change in measured power with modelled rate of change of V_{Se}-V_{Cu} between donor and acceptor states.

The carrier concentration depends exponentially on the voltage, so in this model the voltage has a strong effect on the preconditioning rate. This was observed also in the experiments, where the increase in power occurred at a faster rate in the experiments of section 5.3 than those of 5.6, which were preconditioned at a lower voltage. Figure 6-13 shows a model for the effect of varying the voltage on the rate of preconditioning and relaxation.

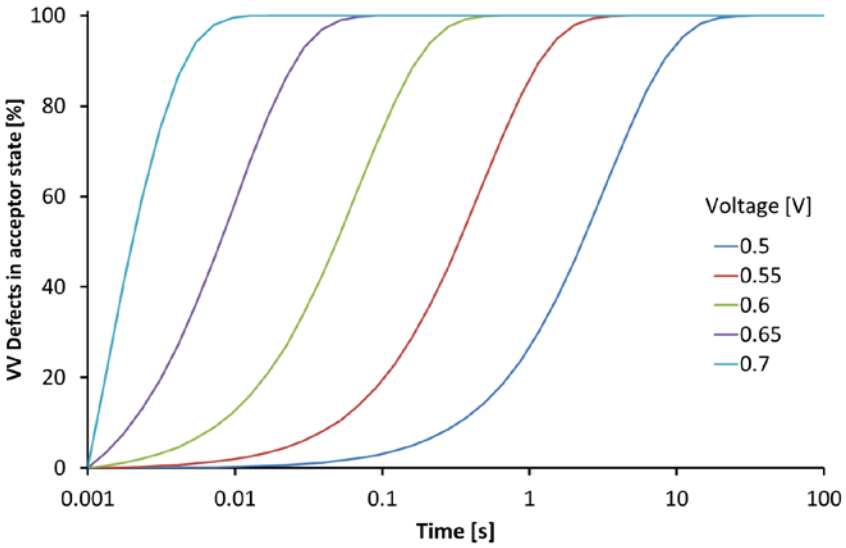


Figure 6-13: Effect of the voltage on the rate of the defect transition during electrial bias preconditioning.

From this we see that for repeatable measurements the voltage used for the preconditioning should be controlled very precisely, and for faster preconditioning a higher voltage should be used.

It has been suggested that the blue light effect could be due to the reverse conversion of the VV defect from the acceptor to the donor state in a region close to the interface, due to the increase in the hole concentration caused by generation in the buffer layer. In steady state the fraction of VV defects in the acceptor configuration will be given by

$$\frac{[VV^-]}{[VV]} = \frac{\tau_2}{\tau_1 + \tau_2} \qquad 6.16$$

At the interface the concentration of electrons will be higher than the concentration in the bulk. Assuming the same default parameters as in the previous section then n in the bulk should be 2.4×10^{10}. Even with this value of n, in order for only 10% of the VV defects to convert into the donor state requires $p=3\times10^{17}$ cm^{-3} which is implausibly high, so it seems unlikely that this defect is the cause of the blue light effect.

For a device in the relaxed state, VV defects just inside the space charge region will initially be in the donor state, as some point closer to the junction the ε(+/-) transition level will cross the Fermi level and the defect will already be in the acceptor state. For the defects in the donor state, when bias is applied the electron concentration will be higher than in the bulk so the defects will convert more quickly. When the bias is removed these states will have a lower hole concentration than the bulk so they will relax back to the donor state more slowly. This adds another component to the kinetics.

The relaxation of the millisecond timescale preconditioning in the previous chapter was seen to occur with a time constant of 1.6s. The predicted relaxation of this VV defect back to the donor state is much slower than this. Unless parameters in the model such as the cross section are considerably erroneous it seems that the millisecond timescale preconditioning must be caused by a different mechanism.

Despite the simplicity of the model used in this section the kinetics of the preconditioning and relaxation are described well by the kinetics of the VV defect transitions. The theory leaves significant scope for the observation that different modules take differing times to stabilise. In particular, differences in N_A and N_{VV} have a dramatic effect and can be expected to vary between differently manufactured modules. The stretched exponential behaviour can be described well by a spread of activation energies for the transition, which has a sound physical basis.

6.5.3 III_{Cu} defect kinetics

Relatively less theoretically calculated information is available about the metastable III_{Cu} defect. In particular, the details for capture cross sections and activation energies for the $CuGaSe_2$ material have not been published. The kinetics of this defect are investigated more here since the VV defect seems unlikely to be the cause of the millisecond timescale preconditioning and also the VV defect seems unable to explain the decrease in capacitance observed during preconditioning. The III_{Cu} defect potentially can explain both of these things.

The deep DX centre captures holes without activation energy and converts to the donor state with subsequent emission of electrons. This will be the dominant process when the device is illuminated with blue light. The rate for this transition is

$$\tau_{DX\rightarrow A,Opt}^{-1} = V_{th}\sigma p \qquad 6.17$$

Due to the absence of an energy barrier for hole capture this process should be quite fast and cannot explain the slower preconditioning normally seen. The conversion back to the DX state requires the capture of two electrons since only then is there a stable state in the DX configuration as seen in the configuration coordinate diagram Figure 6-7. Therefore the electron capture requires simultaneous capture of two electrons and the rate equation will be.

$$\tau_{A\to DX}^{-1} = \frac{(n\sigma V_{th})^2}{\upsilon_{ph}} \exp\left(\frac{-\Delta E_3 - 2E_{pin} + 2E_c}{kT}\right) \quad 6.18$$

Where the activation energy has been related to the activation energy for electron emission from the DX state, and the equilibrium transition level using the principle of detailed balance.

The difficulty with modelling this process compared to the VV transitions is that the carrier concentrations at the interface can vary drastically between different devices and are in general difficult to estimate. Also, the capture cross sections are not known, and could vary within a very wide range depending on whether or not the defect is in a complex with V_{Cu} defects, since this affects the charge state. The question of whether the defects stack to create an ODC, which lowers the valence band minimum, is also relevant because p will be lower if this is the case.

In general, because of these unknown quantities it is currently not possible to create a predictive model for the transition rates for this defect. However, it is possible to demonstrate the feasibility that this defect could be the cause of the millisecond timescale preconditioning. The millisecond timescale preconditioning observed in section 5.5 had a time constant of 320ms. This could correspond to a III_{Cu} defect with $\sigma_p \approx 10^{-17}\ cm^2$ and $p \approx 10^{10}\ cm^{-3}$. Such a relatively small value of the cross section for the DX centre only seems more likely for the neutral centre, i.e. the isolated defect, without complexing to V_{Cu}. The relaxation time constant of 1.6 s implies $\sigma_n \approx 1/n$. Since the substitutional state of the isolated In_{Cu} has charge state of 2+, it should have a large cross section for electron capture, so values of $\sigma_n \approx 10^{-11} cm^2$ and $n \approx 10^{11}\ cm^{-3}$ are a plausible solution.

6.6 Implications for preconditioning

One of the key questions regarding preconditioning is whether there exists a stable end preconditioned state which is independent of the exact illumination and voltage bias conditions or whether the final state reached during preconditioning depends on the preconditioning conditions. A combination of literature and the experimental work from this chapter suggests that the V_{Se}-V_{Cu} defect plays an important role in CIGS device preconditioning. From the properties of this defect, for any realistic operating voltages or illumination levels, the final state should be the same with all of the V_{Se}-V_{Cu} defects eventually taking the shallow acceptor state. Although the time required to reach this

final state may be prohibitively long. There also appear to be other processes occurring during preconditioning, which change the accumulation of charge in the area close to the interface. This process occurs during the electrical bias preconditioning, as evidenced by the decrease in capacitance observed in chapter 5. However, from the literature we know that there is a difference between the application of forward bias and blue light. This suggests that the junction region does not reach a final end point where all the defects are in one state, rather the proportion of defects with different charge states will change depending on the exact preconditioning conditions. This is unfortunate in terms of easily repeatable preconditioning, since it implies that the final stabilised state of the module depends on the preconditioning conditions.

This leads to the question of what the difference will be between electrical bias preconditioning and light soaking. Figure 6-14 shows band diagrams and carrier concentrations for a simulated CIGS device at 0 V in the dark and at $V=V_{oc}$ in the light and in the dark, in this case for a device following the p+ model with a reduced valance band in the ODC layer.

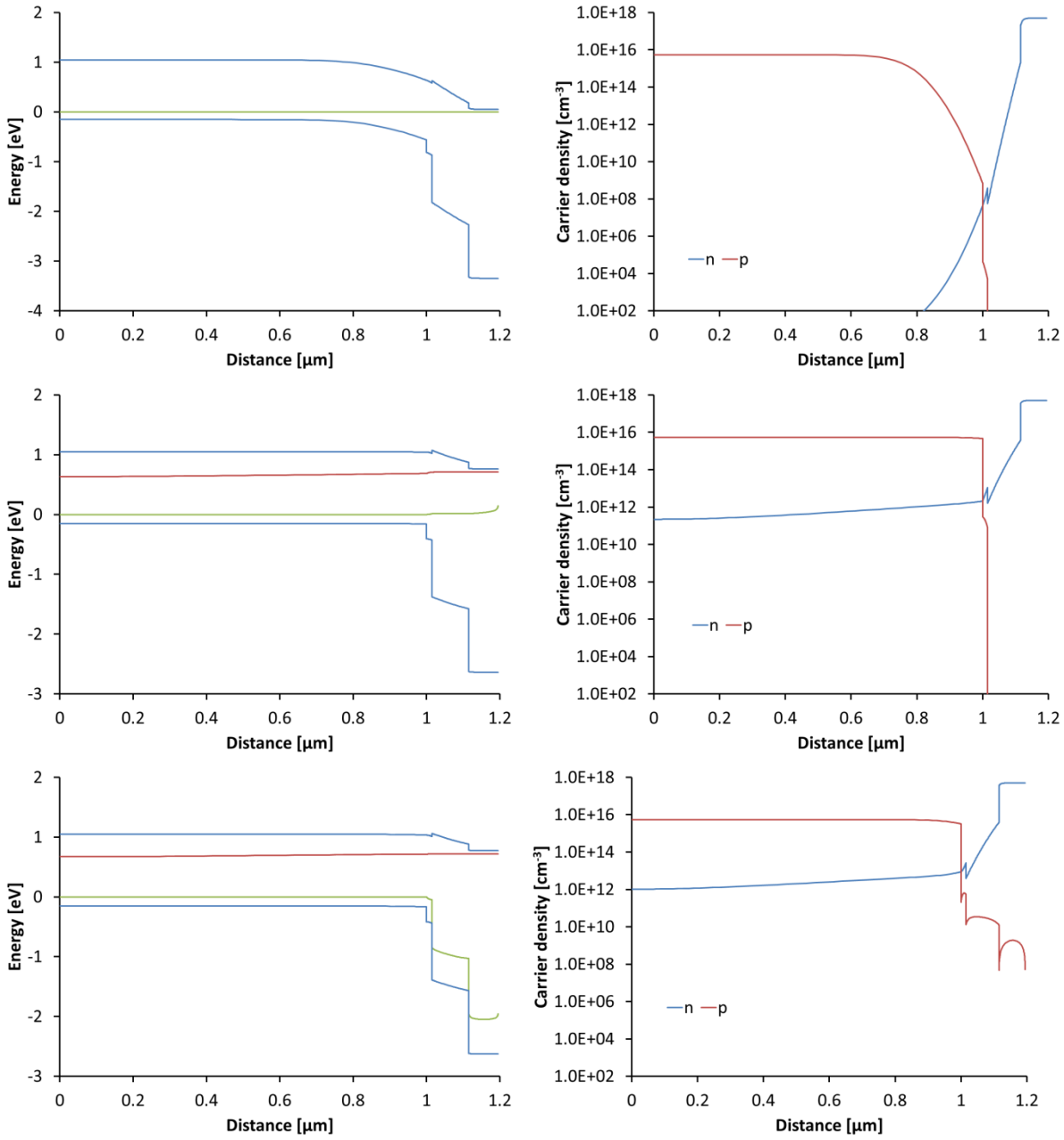


Figure 6-14: Band diagrams and carrier concentrations for CIGS devices in different bias conditions. Top - 0V in the dark. Middle – V_{oc} in the dark. Bottom – V_{oc} under illumination. The device model has a 15nm defect layer with 10^{17} deep acceptor defects.

Both illumination and forward bias drastically increase the electron concentration in the absorber. For the case of the V_{Cu}-V_{Se} defect it should be enough to cause complete conversion of the defects to the acceptor state in either case. However, for the same voltage the electron concentration is slightly higher when illuminated, so the preconditioning would be expected to occur at a faster rate. The strongest difference between the devices under forward bias and illumination is in the hole concentration in the buffer. If a defect layer with a reduced valence band maximum exists, then that band

offset also means that there is an increase in the hole concentration in the ODC layer under illumination compared to only forward bias. However both forward bias and illumination do increase the hole concentration in the ODC layer. So, if parts of the metastability are related to this layer then forward bias would be expected to cause preconditioning but at a different rate and not necessarily reaching the same end steady state distribution of defect charge states. This seems to agree with the experimental evidence that forward bias is changing the charge at the interface, while allowing for the fact that blue light has a larger effect. At voltages below the open circuit voltage the change in hole concentration in the ODC with illumination would be more pronounced.

As discussed in 6.2.3 there are significant reasons to believe that in the interface region there is only a very thin surface reconstruction with reduced valence band, rather than an extended ODC layer. In that case the hole concentration in the absorber should be almost equivalent between forward bias and illumination. The blue light effect might be due to hole capture in the buffer layer or in the thin surface layer. Electrical bias would not be able to cause the same effect as photodoping of the buffer layer. If charge capture occurs in the thin surface region, the implications of this are similar to the case of the extended ODC layer, although there would be a strong contribution from holes tunnelling from the absorber in this case, which would increase the amount of positive charge captured under forward bias.

6.7 Conclusions

The full understanding of preconditioning in CIGS PV devices still requires further research. However, from the literature review and work presented here we can say:

- Literature supports a role for the metastable defect V_{Se}-V_{Cu} and rate modelling the of the transitions of this defect has shown good agreement with the observed preconditioning timescales.
- The non-exponential behaviour of the preconditioning can be explained by a variation in activation energies and capture cross sections for different defect states due to variations in the local atomic configuration.
- The increase in doping density during precondition due to the conversion of V_{Se}-V_{Cu} defect must also change the distribution of charge in the region close to the

junction in order to explain the large change in fill factor observed and the decrease in capacitance.

- The metastable changes caused by this particular mechanism should occur both under forward voltage bias and also under illumination, although the rate of change may be slightly faster under illumination.
- This change in rate can explain the differences observed between preconditioning using light soaking and electrical bias.

From the literature it seems likely that there is an additional effect, related to the blue light effect, for which the action of voltage bias and illumination are not the same. For the changes that relate to the V_{Se}-V_{Cu} defect, the kinetic modelling of this chapter reveal that the net doping density of the absorber is one of the key factors which causes the rate of change to be different for different devices. Hence the preconditioning will occur more quickly for highly doped devices.

7 Conclusions

The overall aim of this thesis was to improve performance measurements of photovoltaic devices. This was achieved for two particular areas where there are significant problems with the existing procedures: the measurement of high capacitance photovoltaic modules and the measurement of metastable CIGS devices.

In the case of high capacitance modules, the aim was to create a method to measure I-V curves of the modules in a pulsed simulator without sacrificing accuracy and in particular to do this in a way that could be automated, and applied individually for each module, so that it is applicable to production line measurements. This aim was successfully achieved by using C-V measurements of the modules to model the dynamic response of the module to changes in the voltage, and subsequently tailoring the voltage profile for the measurement. The reduction in measurement time using the method compared to the multi flash method is up to a factor of 10, and allows most modules to be successfully measured in a single 10 ms illumination pulse. The method was tested using a variety of high capacitance modules and in each case the measured I-V curve parameters agreed with the conventional but much slower multi flash method to within 0.5%. The C-V measurement produced as a by-product of this method is extremely useful in its own right. It can be used to extract minority carrier lifetime and base doping densities. These measurements could be used to help identify the source of unintentional production line changes, and provide an extra quality control check.

The measurement solution created for this problem has important application in industry. High capacitance was demonstrated to be intrinsically linked to high efficiency, so as the PV industry increasingly improves performance, this problem will become increasingly difficult to deal with, however the method presented here should provide an suitable solution for the foreseeable future.

The second performance measurement problem that was identified was the issue of metastability in CIGS devices. The challenge in measuring these devices is that the measured I-V curve depends on the previous exposure of the module. The work presented in this thesis represents significant progress in this field. The preconditioning and subsequent relaxation to the dark storage state were both found to follow strongly non exponential kinetics such that on a logarithmic timescale the changes occur almost linearly over many orders of magnitude in time. The implication of this for

preconditioning procedures is that in order to make repeatable device measurements the timing of each component of a preconditioning routine should be controlled such that the error in the timing is small as a fraction of its overall length. In particular, not only the length of the preconditioning but also the period between preconditioning and measurement should be controlled. This is an important result since this understanding considerably improves the possibilities for repeatable measurement of CIGS devices.

C-V curves and the dark current were measured during electrical bias preconditioning of a variety of CIGS modules. The results agree with theories that during preconditioning there is a reduction in the amount of negative charge in a region near the absorber buffer interface. This model is able to explain well why the parameter which shows the most significant changes during the preconditioning is the fill factor. However the timescale of the preconditioning agrees very well with the expected kinetics of the V_{Se}-V_{Cu} metastable defect. There is significant pre-existing evidence in the literature that this defect is responsible for changes in the bulk doping of the device. This shows that there are two effects occurring, a change in doping of the bulk of the absorber and a change in charge accumulation at the interface. The agreement of the kinetics of the performance improvement and the expected V_{Se}-V_{Cu} defect transition implies that the doping in the bulk directly causes a change in charge accumulation at the interface.

For the case of doping changes in the bulk of the absorber caused by the V_{Se}-V_{Cu} defect, it is possible to use electrical bias preconditioning as an alternative to light soaking for preconditioning of CIGS devices. The exact nature of the changes at the interface remains unclear, but considering the possible options it is likely that there will be some differences in the state reached by electrical bias and light soaking, which explains the differing reports on this subject in the literature.

The kinetic modelling of the V_{Se}-V_{Cu} defect in a device showed that the stretched exponential shape of the preconditioning is explained well by different activation energies and cross sections for carrier capture, due to differences in the local atomic configuration of the device.

During the experimental work an unexpectedly short timescale effect was observed to cause preconditioning during the 10 ms illumination period of a pulsed solar simulator. The effect was particularly strong in the module type for which it was initially noticed

but closer inspection showed that it was also present more generally. Investigation of the timescales of this faster effect again revealed a non-exponential behaviour so that although the preconditioning is strong in the first 10ms the time constant for a stretched exponential fit was 320 ms. The time constant for the relaxation was measured at 1.66 s but it took around 30 s to fully relax. It was found that there was a relatively simple solution to this problem which is to apply electrical bias to the module until immediately before the measurement. For the devices where this effect is a significant problem this is very important result which allows them to be measured in a pulsed simulator.

Now that the photovoltaics industry is entering maturity economic and high accuracy performance measurements of photovoltaic modules are becoming essential. The work presented here represents a step forwards in the ability to achieve these measurement.

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