Numerical Analysis of Lead-free Solder Joints: Effects of Thermal Cycling and Electromigration

By Xu Zha

A Doctoral Thesis SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF DOCTOR OF PHILOSOPHY OF LOUGHBOROUGH UNIVERISITY MARCH 2016

© by Xu Zha, 2016

I

Abstract

To meet the requirements of miniaturization and multifunction in microelectronics, understanding of their reliability and performance has become an important research subject in order to characterise electronics served under various loadings. Along with the demands of the increasing miniaturization of electronic devices, various properties and the relevant thermo-mechanical-electrical response of the lead-free solder joints to thermal cycling and electro-migration become the critical factors, which affect the service life of microelectronics in different applications. However, due to the size and structure of solder interconnects in microelectronics, traditional methods based on experiments are not applicable in the evaluation of their reliability under complex joint loadings. This thesis presents an investigation, which is based on finite-element method, into the performance of lead-free solder interconnects under thermal fatigue and electro-migration, specifically in the areas as follows: (1) the investigation of thermalmechanical performance and fatigue-life prediction of flip-chip package under different sizes to achieve a further understanding of IMC layer and size effects of a flip chip package under thermal cycling; (2) the establishment of a numerical method, simulating void-formation/crack-propagation based on the results of finite-element analysis, to allow the prediction of crack evolution and failure time for electro-migration reliability of solder bumps; (3) the establishment of a flow-based algorithm for combination effects of thermal-mechanical and electro-migration that was subsequent implemented in to an FE model to evaluate the reliability assessment of service lives associated with a flip chip package.

Keywords: lead-free solder joint; micro scale; finite element; thermal fatigue; electromigration; void formation; joint effect.

Acknowledgements

The research was supported by a Marie Curie International Research Staff Exchange Scheme Project within the 7th European Community Framework Programme, No. PIRSES-GA-2010-269113, entitled "Micro-Multi-Material Manufacture to Enable Multifunctional Miniaturised Devices (M6)".

I would like to thank my supervisors Prof. Changqing Liu and Prof. Vadim V. Silberschmidt for their valuable suggestions, guidance and support throughout my PhD study. I appreciate their continuous encouragement and efforts to help me with my research.

I acknowledge the continuous supports that I have received throughout my exchange time from Prof. Fengshun Wu and Dr. Weisheng Xia in Huazhong University of Science and Technology, Wuhan. Their expertise, training and assistance on material characterization and electroplating have guided me in the way of my research.

Thanks are also extended to all my friends and colleagues for their kind helps during my stay at Loughborough and Wuhan. Finally, I would like to thank my parents for their continuous encouragement and support all the time.

Publications

Zha, X., Liu, C., and Silberschmidt, V. V., 2012, "Finite Element Analysis of Thermomechanical Behaviour of Micro-solder Joints", Proc. 13th International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP).

Zha, X., Liu, C., and Silberschmidt, V. V., 2013, "Finite-element Analysis of Anisotropic Behaviour in Electromigration in Micro-solder Joints", Proc. 15th Electronics Packaging Technology Conference (EPTC).

Table of Contents

Abstract	I
Acknowledgements	II
Publications	III
Table of Contents	IV
List of Abbreviations	VII
List of Figures	VIII
List of Tables	XIV
Chapter 1. Introduction	1
1.1 Background	1
1.2 Motivation and objectives	2
1.3 Thesis structure	5
Reference	7
Chapter 2 Reliability issues in flip-chip packages	
2.1 Introduction	
2.2 Thermal cycling	8
2.2.1 Microstructure of solder bumps	9
2.2.2 Mechanical properties of materials in a solder bump	17
2.2.3 Fatigue prediction model	
2.3 Electro-migration	27
2.3.1 Driving forces of atomic transport in EM	
2.3.2 Failures resulted by Electro-migration	30
2.4 Summary	
Reference	
Chapter 3 Modelling on reliability issues of flip-chip packages	42
3.1 Introduction	42
3.2 Two/three-dimensional models	42
3.3 FEA of solder bumps under thermal cycling	44
3.4 FEA of solder bumps under electro-migration	
3.5 Summary	52
Reference	54
Chapter 4. Microstructure geometry and shape prediction of solder bump	s in flip-
chip packages	58
4.1 Introduction	58
4.2 Microstructure geometry of solder bumps	59
4.2.1 Experimental procedure	60
4.2.2 Results and discussion	
4.3 Shape prediction of solder bumps	
4.4 Summary and conclusions	
Reference	
Chapter 5. Mechanical behaviours of package and single solder bump	
under thermal cycling	
5.1 Introduction	
5.2 Analysis procedure	
5.2.1 Model description and loading conditions	75

5.2.2 Material properties	
5.2.3 Justification of 2-D/3-	D FE models
5.2.4 Mesh convergence and	llysis of 2-D model91
5.3.1 Package warpage: effe	cts of creep behaviour94
0 10	on mechanical behaviours
	evolution of solder bumps: effect of IMC layers
	98
5.3.4 Stress state of solder b	umps: effect of miniaturization
	der bumps under thermal cycling loads 105
	method
	106
	gle solder bump of BGA115
	115 115
6.2 Distributions of Current dens	ity and temperature in single solder bump116
	loading conditions117
	121
	the model
	122
	oid/crack under electro-migration
	and failure criteria of electro-migration in solder
1	
	rack expansion caused by electro-migration. 142
6.4 Summary and conclusions	
6.4 Summary and conclusions Reference	
6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f	147 149 atigue and electro-migration on solder bumps
6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f	147 149 atigue and electro-migration on solder bumps 151
6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f	147 149 atigue and electro-migration on solder bumps 151 151
6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure	147 149 atigue and electro-migration on solder bumps 151 151
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the 	147 149 atigue and electro-migration on solder bumps 151 151 152 ermal-fatigue life of solder bump under electro-
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate th migration 	147 149 atigue and electro-migration on solder bumps 151 151 152 ermal-fatigue life of solder bump under electro- 152
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 	147 149 atigue and electro-migration on solder bumps 151 151 152 153 154 152 153 154 155 152 153 154
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 	147 149 atigue and electro-migration on solder bumps 151 151 152 152 152 152 152 152
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 	147 149 atigue and electro-migration on solder bumps 151 151 152 152 152 152 154 158 158 159
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolution and evolution and evolution and evolution	147 149 atigue and electro-migration on solder bumps 151 151 152 153 154 155 10ading conditions 158 159 ution of stress in global model under effects of
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolution void formation and crack press 	147 149 atigue and electro-migration on solder bumps 151 151 152 152 152 153 154 155 154 158 159 151 152 153 154 155 155 155 156 157 158 159 159 159 159 159 159 151 152 <t< td=""></t<>
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolution void formation and crack pression of the second s	147 149 atigue and electro-migration on solder bumps 151 151 152 152 16 152 16 152 10 152 10 152 10 152 10 153 154 159 ution of stress in global model under effects of 0 0 159 strains and prediction of thermal fatigue life with
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolution void formation and crack print 7.3.2 Accumulated inelastic global model 	147 149 atigue and electro-migration on solder bumps 151 151 151 152 bermal-fatigue life of solder bump under electro- 152 loading conditions 158 159 ution of stress in global model under effects of opagation 159 strains and prediction of thermal fatigue life with 162
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolve void formation and crack pression of the series of	147 149 atigue and electro-migration on solder bumps 151 151 151 152 10ading conditions 154 159 159 159 159 159 159 159 159 162 under joint effects of thermal fatigue and electro-
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolution void formation and crack pr 7.3.2 Accumulated inelastic global model	147 149 atigue and electro-migration on solder bumps 151 151 152 153 154 155 10ading conditions 158 159 159 159 159 159 159 159 159 159 150 151 152 153 154 155 156 157 158 159 151 152 153 154 155 155 156 157 158 159 151 152 153 154 155 156 161 162 164
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolution void formation and crack pression of the service of	147 149 atigue and electro-migration on solder bumps 151 151 151 152 bermal-fatigue life of solder bump under electro- 152 loading conditions 159 ution of stress in global model under effects of opagation 159 strains and prediction of thermal fatigue life with 162 under joint effects of thermal fatigue and electro- 164 164
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolve void formation and crack pression 7.3.2 Accumulated inelastic global model 7.4 Summary and conclusions	147 149 atigue and electro-migration on solder bumps 151 151 151 152 10ading conditions 153 154 155 10ading conditions 159 159 159 159 159 159 159 159 162 162 164 166 168
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolution void formation and crack pr 7.3.2 Accumulated inelastic global model 7.3.3 Service life of package migration 7.4 Summary and conclusions Chapter 8. Conclusions and future volution and service service	147 149 atigue and electro-migration on solder bumps 151 151 152 10ading conditions 152 loading conditions 158 159 ution of stress in global model under effects of opagation 159 strains and prediction of thermal fatigue life with 162 under joint effects of thermal fatigue and electro- 164 168 work
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3 Results and discussions 7.3 Results and discussions	147 149 atigue and electro-migration on solder bumps 151 151 152 152 153 154 155 10ading conditions 159 159 159 159 159 159 159 159 159 161 162 164 164 164 168 work 169 169
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolve void formation and crack pr 7.3.2 Accumulated inelastic global model 7.3.3 Service life of package migration 7.4 Summary and conclusions	147 149 atigue and electro-migration on solder bumps 151 151 152 10ading conditions 152 10ading conditions 153 154 155 10ading conditions 158 159 ution of stress in global model under effects of opagation 159 strains and prediction of thermal fatigue life with 162 under joint effects of thermal fatigue and electro- 164 165 work 169 try and shape prediction of a solder bump 169
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3.1 Distribution and evolution void formation and crack pr 7.3.2 Accumulated inelastic global model 7.3.3 Service life of package migration 7.4 Summary and conclusions 8.1 Main conclusions and future volutions	147 149 atigue and electro-migration on solder bumps 151 151 152 153 154 155 10ading conditions 156 157 10ading conditions 158 159 159 159 159 159 159 159 159 159 159 161 162 under joint effects of thermal fatigue and electro- 164 165 vork 169 try and shape prediction of a solder bump 169 rs of package and single solder bump of BGA
 6.4 Summary and conclusions Reference Chapter 7. Joint effects of thermal f 7.1 Introduction 7.2 Analysis procedure 7.2 Analysis procedure 7.2.1 Method to calculate the migration 7.2.2 Model description and 7.2.3 Material properties 7.3 Results and discussions 7.3 Results and discussions	147 149 atigue and electro-migration on solder bumps 151 151 152 10ading conditions 152 10ading conditions 153 154 155 10ading conditions 158 159 ution of stress in global model under effects of opagation 159 strains and prediction of thermal fatigue life with 162 under joint effects of thermal fatigue and electro- 164 165 work 169 try and shape prediction of a solder bump 169

8.1.4	Joint effects of thermal fatigue and electro-n	nigration on solder bumps
8.2 Majo	r contributions	
	work	
Appendix		
11		

List of Abbreviations

ACA	Anisotropic Conductive Adhesive
ACTC	accelerated thermal-cycling test
BGA	ball grid array
BSE	Back Scattered Electron
CTE	Coefficient of Thermal Expansion
EDS	Energy Dispersive Spectrometer
FC-PBGA	flip-chip plastic ball grid array
FE	Finite Element
FEA	Finite Element Analysis
FEM	Finite Element Method
GB	giga byte
GB IC	giga byte Integrated Circuit
IC	Integrated Circuit
IC IMC	Integrated Circuit intermetallic compounds
IC IMC I/Os	Integrated Circuit intermetallic compounds inputs/outputs
IC IMC I/Os MB	Integrated Circuit intermetallic compounds inputs/outputs mega byte
IC IMC I/Os MB SEM	Integrated Circuit intermetallic compounds inputs/outputs mega byte Scanning Electron Microscopy
IC IMC I/Os MB SEM SOH	Integrated Circuit intermetallic compounds inputs/outputs mega byte Scanning Electron Microscopy stand-off height

List of Figures

Fig. 1. 1. Geometrical road map of interconnects [6]
Fig. 1. 2. Schematic of the thesis structure
Fig. 2. 1. Thermal fatigue cracks in (a) Sn3.5Ag solder joint and (b) Sn3.8Ag0.7Cu solder joint [7]
Fig. 2. 2. Electrolytic Cu/SnAgCu diffusion couple annealed at 125 °C for 1000 h [8]
Fig. 2. 3 . BSE image of the structure of the IMC layer at Ni side in the Cu/Sn/Ni solder joint with 100 μm-height [9]
Fig. 2. 4. Micrographs of cross-sectional views of IMCs during isothermal aging [17]
Fig. 2. 5 . Microstructure of Sn-3.5Ag solder upon different cooling rates: (a) 24K/s-water quenching, (b) 0.5K/s-air cooling, (c) 0.08K/s-furnace cooling [20]13
Fig. 2. 6 . Cross-sectional BSE mode SEM images of the Cu/Sn/Cu solder joint with (a) 100 μ m SOH; (b) 50 μ m SOH; (c) 20 μ m SOH; (d) 10 μ m SOH [23] 15
Fig. 2. 7. The mean Cu concentration changes in the solder bulk with the reducing SOH [23]
Fig. 2. 8 . Crystal structure of β -Sn. (a) Body-centred tetragonal unit cell; (b) contracted diamond structure. The dimension of unit cell (along a and b in (a)) are 0.58318 and 0.31819 nm (along c) [26]16
Fig. 2. 9 . Typical creep curve showing the three steps of creep. Curve A, constant-load test; Curve B, constant-stress test [36]
Fig. 2. 10 . (a) Comparison of creep data from bulk Sn59Pb40Ag1 solder and flip chip Sn63Pb37 solder for a temperature of T=20 °C; (b) Comparison of creep data from bulk SnAg3.8Cu0.7 solder and flip chip SnAg4Cu0.5 for a temperature of T=20 °C; The flip chip creep data form T=5 °C, 50 °C was corrected for this temperature [43]
Fig. 2. 11. Low-cycle fatigue curve ($\Delta \epsilon p$ vs. N) for Type 347 stainless steel. [47] 25
Fig. 2. 12 . A schematic diagram of a flip chip interconnects including Al traces, solder joints and Cu conductors [53]
Fig. 2. 13 . (a) & (b) Sn-Pb bumps under 0.6 A/135 °C at 306 h; (c) Sn-Pb under 0.6 A/125 °C at 616 h; the red arrows indicate the direction of electron current [65] 31

Fig. 2. 15. (a) Typical microstructure of a Sn37Pb solder joint as-reflowed, (b) a Sn3.5Ag0.5Cu solder joint as-reflowed, (c) Pb-rich phase coarsening in a Sn37Pb solder joint, and (d) Ag-rich IMC coarsening in a Sn3.5Ag0.5Cu solder joint [**70**]... 32

Fig. 2. 17. SEM images of the morphological evolution in Sn3.5Ag1.0Cu solder joints under a current density of 1.5×10^4 A/cm² at 125 °C (a) before the experiment, the time point A, (b) after 75 h, 14% of the failure time, the time point B, (c) after 280 h, 53% of the failure time, the time point C, (d) after 425 h, 81% of the failure time, the time point D, and (e) after 515 h, 98% of the failure time, the time point E [72]...... 34

Fig. 3. 6. Schematic of TSV in Si interposer from IME [29]...... 50

Fig. 4. 1. Schematic view of micro-structure and design parameters for a solder	1
Fig. 4. 2. Schematic diagram of the electroplating system	
Fig. 4. 3. (a) The Power source of electroplating system; (b) The fixture clampin copper substrates	0

Fig. 4. 4. The electroplating system used in the experiment
Fig. 4. 5 . Cross sections of the samples after: (a) 5 min, (b) 10 min, (c) 15 min and (d) 20 min electroplating durations
Fig. 4. 6. Relationship of the Sn layer thickness and the electroplating durations 64
Fig. 4. 7 . The reflow oven
Fig. 4. 8. Actual temperature sensed by thermo-couple in reflow
Fig. 4. 9. Cross section of as-reflowed specimen by FEM
Fig. 4. 10. EDS results of Line P at: (a) Point A, (b) Point B, (c) Point C and (d) Point D
Fig. 4. 11. Two-dimensional FE-model of a micro solder bump in ABAQUS 6.14 69
Fig. 4. 12 . The evolution of a BGA solder ball using energy-based method by Surface Evolver: (a) initial state; (b) refine the element first time; (c) minimize the potential energy first time; (d) refine the element second time; (e) minimize the potential energy second time; (f) refine the element third time; (g) minimize the potential energy third time
Fig. 4. 13. Geometry of joints with different standoff height predicted by Surface Evolver
Fig. 5. 1. A schematic top-view of the BGA and the positions of FE-models
Fig. 5. 2 . Geometry and boundary conditions of the package for FE analysis: (a) quarter of the structure; (b) reading chip is removed from (a) (Unit: mm)
Fig. 5. 3 . Location, geometry and boundary conditions of the package for FE analysis: (a) location of 2-D model in the package; (b) 2-D model with mesh; (c) enlarged view of a single solder bump (Unit: mm)
Fig. 5. 4. Underfill with mesh in the package for FE analysis
Fig. 5. 5. Thermal cyclic load in simulations: 3600 s corresponding to 3 cycles 80
Fig. 5. 6 . Geometry of solder bump in 200 μm standoff height with IMC layer: (a) the position of IMC layer in a meshed solder bump; (b) different thickness of IMC layer
Fig. 5. 7 . Geometry of solder bumps with 20 μm SOH with: (a) flatten IMC layer; (b) scallop-shaped IMC layer
Fig. 5. 8 . Crystal structure of Sn grain [11]

Fig. 5. 10. Mises stress distribution at the end of thermal cycling in: (a) cross section of 3-D quarter model; (b) chip array with chip removal and (c) 2-D plain strain model 90

Fig. 5. 21. Distributions of accumulative inelastic strains in the outmost bump with 200µm-SOH with no IMC layer after the third cycle (t=3600 s): (a) creep strain; (b) plastic strain. 107 Fig. 5. 22. Evolution of accumulated equivalent inelastic strains at A and B in the solder Fig. 5. 23. Distribution of equivalent inelastic components in outmost solder bump with 20-µm-SOH: (a) the equivalent creep strain; (b) the equivalent plastic strain...... 109 Fig. 5. 24. Evolution of accumulated equivalent inelastic strains at A and B in the solder Fig. 6.1. Three typical current-flow paths in solder bump (red arrows represent possible paths of electrons): (a) from one corner to opposite corner; (b) from one corner to other corner located on same side; (c) from one sides centre to other117 Fig. 6. 2. Geometry and current flow path in a meshed solder bump of BGA118 Fig. 6. 3. Geometry and current flow path in a meshed solder bump of TSV119 Fig. 6. 4. Heat boundary conditions of FE models: (a) surfaces in contact with air; (b) Fig. 6. 5. Meshed solder bump with different numbers of elements: (a) 753 elements, **Fig. 6. 6.** FE-simulated distribution of the *ECD* vector in Model I (unit: A/mm^2): (a) vector magnitude; (b) vector component along X-axis; (c) vector component along Y-Fig. 6. 7. FE-simulated distribution of the HFL vector magnitude in Model I (unit: Fig. 6.8. FE-simulated distribution of the EPOT in Model I (unit: V) 129

Fig. 6. 12. FE-simulated distribution of the EPOT in Model II (unit: V)...... 133

Fig. 6. 14. FE-simulated distribution of the HFL vector magnitude in Model III (unit	
N/mm ²)	5

Fig. 6. 15. FE-simulated distribution of the <i>EPOT</i> magnitude in Model III (unit: V)
Fig. 6. 16. Flow chart of void formation and crack expansion simulation 141
Fig. 6. 17 . Enlarged view of elements located at the right upper area of Model I and their numbers generated by ABAQUS 6.14
Fig. 6. 18 . Distribution of thermal-electrical results in Model I after the removal of Element 2180: (a) <i>ECD</i> vector magnitude; (b) <i>HFL</i> vector magnitude
Fig. 6. 19 . Crack expansion in solder bump and the distribution of electrical potential at failure time
Fig. 6. 20 . Cross-sections of SnAgCu solder bumps under electro-migration based on experiments: (a) Morphological evolution in Sn3.5Ag1.0Cu solder joints under a current density of 1.5×10^4 A/cm ² at 125 °C [12]; (b) Cross-section of the 0.3 mm diameter solder ball at 1500 h [13]
Fig. 6. 21. Relationship of electrical potential and crank length in the model 145
Fig. 6. 22. Relationship between electrical potential and migration time in the model
Fig. 7. 1 . Flow chart of assessment of thermal-fatigue life for solder bumps in BGA void formation and crack expansion
8 8 1
void formation and crack expansion
void formation and crack expansion
 void formation and crack expansion
 void formation and crack expansion
 void formation and crack expansion

List of Tables

Table 2. 1. Summary of the elastic properties of Ag ₃ Sn, Cu ₆ Sn ₅ and Cu ₃ Sn based on calculation [28-30]. 18
Table 2. 2. Young's modulus and hardness of various IMCs
Table 3. 1. Displacement, Equivalent Strain Ranges and Strain Energy Density [38]44
Table 4.1 . The ingredients of electrolyte solution of electroplating
Table 4. 2 . Temperatures and durations set by the reflow oven
Table 4. 3 . Element components in IMC 68
Table 5. 1. Material properties of silicon [6] 83
Table 5. 2. Material properties of BT [6]
Table 5. 3. Material properties of tin alloy (Sn-3.5Ag) [5]
Table 5. 4. Material properties of IMC [6] 85
Table 5. 5 The elastic stiffness constants for tin as a function of temperature
Table 5. 6 Parameters of the viscoelastic underfill models [14]
Table 5. 7. Computing time and memory size of 2-D and 3-D FE models 88
Table 5. 8. The inelastic strain of 2-D and 3-D model in each cycle
Table 5. 9. The calculation cost and evaluating indicators for different element numbers
Table 5. 10 . Comparison between the predicted fatigue cycles for the solder bump with different IMC thickness and bump size
Table 6. 1. Material properties used in FE models for coupled thermal-electrical analysis [3, 5] 122
Table 6. 2. The calculation cost and evaluating indicators for different element numbers
Table 6. 3. Constants used in the numerical model [8]
Table 7. 1. Thermal-electrical properties of copper and SAC305 in sub-model [6, 7] 158

Table 7. 2. Mechanical properties of silicon, BT, SAC305 and underfill 11[4, 5]	U
model [4, 5]	
Table 7. 3. Transformed atoms due to electro-migration, thermo-migration	
migration in critical location with $N0 = 1$ in one thermal cycle	

Table 7. 4. Calculated life in service of solder bump under the joint effects of thermal fatigue and electro-migration

 166

Chapter 1. Introduction

1.1 Background

In electronics manufacturing industry, solder joint plays an important role of interconnection of integrated circuit (IC) packaging. It serves two key purposes: (1) to enable the electrical connection between a chip and a substrate; (2) to provide mechanical bonding which supports a chip to a substrate. There are many types of interconnections such as anisotropic conductive adhesive (ACA), wire bonding, flip-chip technology and so on. Different types of interconnections are applied in various packaging industries. Due to its high inputs/outputs (I/Os) density and compacted structure, flip chip technology is regarded as a promising next generation packaging method. In response to environmental protection and multi-function device, two major developing trends, lead-free soldering and miniaturization, are proposed by modern electrical industry.

In electronics packages, the tin-lead (SnPb) alloys are commercially used as a promising interconnection material for a long time. The reasons for their popularity are their good solderability, adequate melting-temperature point, suitable electrical and mechanical property and relatively low expense. However, lead is considered as a type of toxic chemicals to both human health and environment [1]. According to the waste electrical and electronic equipment (WEEE) legislation [2], the use of lead in consumer electronic devices was forbidden from 1st July, 2006 for any the consumer electronics products in EU. As a consequence, lead-free devices have received increasing attention around the electronic industry. Hence, those potential lead-free soldering materials have to be investigated before application.

On the other hand, due to the miniaturisation, solder joints in flip chip technology, also known as solder bumps, are experiencing decreases in their height and pitch sizes (**Fig. 1.1**). When the size of a bump shrinks to less than 15 μ m/pitch 30 μ m, their microstructure and mechanism differs very much from large ones [**3**]. At micro scale, a solder

1

joint contains only one or a few grains, and hence its mechanical behaviours shift from polycrystalline to single crystal-based [4, 5]. The results derived from large solder bumps may not be applicable to micro ones. Therefore, their microstructural features and mechanical properties are of importance in device miniaturization.

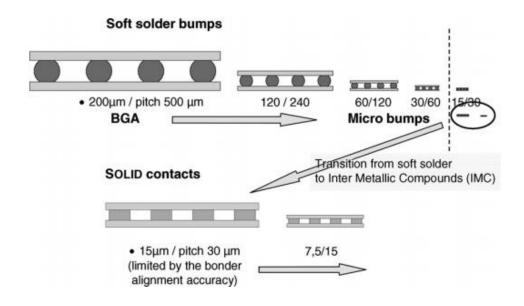


Fig. 1. 1. Geometrical road map of interconnects [6]

To electronic assembly, solder joint has to meet both mechanical and electrical requirements. Therefore, its reliability is a key factor considering the service lifespan of electronic devices. The two trends mentioned above are arising some new problems in electronic products lifespan prediction. The reasons resulting in failures of solder joint varies. There are two main types of failure modes: thermo-mechanical stress (thermal fatigue) and electro-migration [7].

1.2 Motivation and objectives

In flip-chip packaging, chips and substrates are usually made of different materials; which means they have different coefficients of thermal expansion (CTE). Generally, the difference of CTE between a chip and a substrate is large (10 times), resulting in alternating thermal stress and fatigue. Studies have shown that the interfaces between solder material and chip/substrate pad were stress concentration part in the whole

package. At this area, tin alloys react with pad materials, forming intermetallic compounds (IMC). Mechanical properties and microstructures of IMC vary from solder part. Therefore, IMC is the key of solder joint reliability under thermal cycling. In addition, the components replacing lead in lead-free alloys tend to react with tin, forming some other IMC particles with different properties. These IMC particles are distributed in the solder alloy and impact influences on mechanical properties of solder joint. With the shrinkage of solder dimensions, the volume proportion of IMC increases rapidly. When the height decreases to around tens microns, the intermetallic compound even takes most volume proportion in solder ball. The layer of IMC becomes a potential area of fracture, which results in the failure of solder bump. Therefore, it is important to investigate the mechanical behaviours of solder bumps under the effects of thermal loadings.

Another important reliability issue is electro-migration. Electro-migration is defined as a transport of materials in a conductor, leading to gradual movement of microstructures. Electro-migration is caused by the exchange of momentum between conducting electrons and diffusing metal atoms, and usually occurs under high direct current densities. With the trend of solder bump size decrease, electro-migration becomes a more challenging problem. After a long-time scale of atom movement, voids and cracks are formed in solder bumps. The formed voids and cracks accelerate the effects of current crowding, which results in expansions of voids and cracks. Therefore, the service life of a solder bump under electro-migration must be estimated to figure out its electrical reliability. Furthermore, voids and cracks in a solder bump are potential area of stress concentration. The joint effect of thermal fatigue and electro-migration should be investigated.

The primary aim of this thesis is to investigate the influence of thermal fatigue and electro-migration on service life together with their interactions. To achieve these aims, numerical methods were adopted to investigate problems effectively and precisely. Following objectives and tasks of the research were therefore identified and implemented in the thesis work:

1. Characterization of the microstructure and shape of solder bumps by observation and programming: The microstructure of IMC including its thickness

and morphology in a prepared specimen was revealed by SEM observation. The shapes of IMC in a solder bump under both micro and macro scale were predicted by an energy-based programming to indicate the effects of design parameters. Based on these two results, a geometry of BGA package structure was determined for the following simulation.

- 2. Investigation of mechanical behaviours of packages and fatigue life of single solder bump under thermal cycling loads by FEA: Based on the geometry data of different solder bump sizes, several FE models of flip-chip-on-board (FCOB) package under thermal cycling loading were built and analysed. The effects of standoff height and the IMC layer of solder bump on mechanical behaviours under thermal loads were investigated. Also, package-level warpage and stress status in single bump were revealed by numerical results. Furthermore, the service lives of solder bumps were estimated based on accumulative inelastic strain of thermal fatigue.
- 3. Investigation of thermal-electrical distribution and electro-migration effects in single solder bump by FEA: A thermal-electrical coupled FE model based on single solder bump was used to estimate electro-migration. Current and temperature distributions in the solder bump under different current loadings were analysed and discussed. An algorithm of voids formation based on simulation results was proposed and realized by numerical methods. The process of void propagation was revealed and the service life due to electro-migration was estimated by the algorithm.
- 4. Estimation of the joint effects of mechanical stress and electro-migration using numerical methods: The effects of voids formed in electro-migration on mechanical behaviours of FCOB package were studied by simulation. An algorithm of joint effects of mechanical loads and electro-migration was proposed to estimate solder bump service life.

So far, many researches focused on single reliability issue in a solder bump of BGA package, including its mechanism and effect. However, in real application, several issues usually occur at the same time and their interactions cannot be neglected. This research made an attempt to assess joint effects of two common reliability issues by

numerical methods. An algorithm based on FE elements removal was proposed to investigate a BGA package with changing microstructures. According to the research, thermal fatigue life combined with electro-migration was further understood. It proved that the joint effects of reliability issues need to be considered for further electronic packages reliability assessment.

1.3 Thesis structure

The thesis consists of eight chapters, as illustrated in Fig. 1. 2.

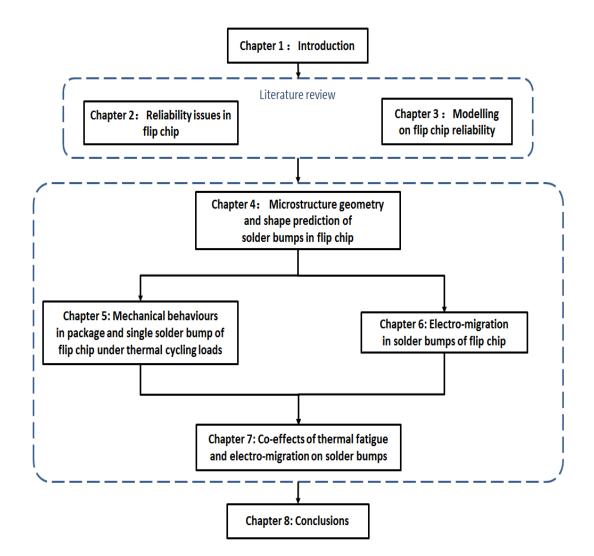


Fig. 1. 2. Schematic of the thesis structure

Chapter 1 gives a background as an introduction of the work in this thesis. The problems and challenges based on the findings of literatures are identified. This chapter also provides the motivations and objectives of this thesis.

Chapter 2 and 3 reviews the relevant literatures about the investigations on mechanical behaviours and electro-migration of solder joints/bumps in flip chip interconnects. The effects of these two main reliability issues on service life of solder bumps are also revealed. Chapter 2 mainly provides previous studies about material properties studies of creep and electro-migration. Some experimental works about different reliability issues are also illustrated in this chapter. Chapter 3 presents some previous work about modelling of solder interconnects in flip-chip assembly. Numerical studies about mechanical and electrical reliabilities are also included by this chapter.

Chapter 4 presents the microstructure geometries and the shapes of solder bumps. The microstructure and geometry studied in this chapter mainly refer to the morphology of IMC existing in the solder joints. Some samples of Sn/Cu structure are prepared and observed to reveal the real morphology of IMCs to feed the FE numerical analysis. An energy-based program is also used to predict some important shape parameters of solder bumps. The geometry of a solder bump used in FEA is determined in this chapter.

Chapter 5 adopts FE-methods to investigate the mechanical behaviours on package level and solder bump level under thermal cycling loads. The warpages of flip chip packages under the effects of creep and IMC are presented. The stress status in solder bumps under thermal cycling loads is illustrated and the most critical bump is identified in this chapter. A prediction method based on accumulative inelastic strain is also used to predict the fatigue life of solder bump under thermal cycling loads.

In Chapter 6, the distribution of current density and temperature determined by FEA is presented. These results are used to calculate the atom flux due to electro-migration. An algorithm based on atoms concentration to simulate voids formation and propagation is proposed in this chapter. Based on the results of this algorithm, the service life due to electro-migration can be estimated.

The joint effects of thermal fatigue and electro-migration based on the results and discussions in previous chapters are investigated in Chapter 7. An atom flux resulted by hydrostatic stress is introduced to calculate full atom flux under electro-migration. This

chapter proposes an algorithm to evaluate the reliability under the joint effects.

Based on the works and discussions in previous chapters, Chapter 8 summarizes the major findings and conclusions in each previous chapter. A number of suggestions based on the main results and discussions in this thesis are provided for future work in this chapter.

Reference

- Abtew M., Selvaduray G., "Lead-free Solders in Microelectronics", *Material Science Engineering*, R 27 (2000), pp. 95-141.
- [2] Pang John. H. L., Low T. H., Xiong B. S., Xu L., Neo C. C., "Thermal cycling aging effects on Sn-Ag-Cu solder joint microstructure, IMC and strength", *Thin solid films*, vol. 462-463 (2004), pp. 370-375.
- [3] LaLonde A., Emelander D., et al., "Quantitative metallography of β-Sn dendrites in Sn-3.8Ag-0.7Cu ball grid array solder balls via electron backscatter diffraction and polarized light microscopy", *Journal of Electronic Materials*, 33, 12 (2004), pp. 1545-1549.
- [4] Gong J., Liu C., et al., "Modelling of Ag₃Sn coarsening and its effect on creep of Sn–Ag eutectics", *Electronics Components and Technology Conference*, 2007, pp. 677-693.
- [5] Matin M. A., Coenen E. W. C., et al., "Correlation between thermal fatigue and thermal anisotropy in a Pb-free solder alloy", *Scripta Materialia*, 53, 8 (2005), pp. 927–932.
- [6] Huebner H., S.P., Barchmann B., Eigner M., et al., "Micro contacts with sub-30μm pitch for 3D chip-on-chip integration", *Microelectronic Engineering*, 83, 11-12 (2006), pp. 2155-2162.
- [7] Frear D. R., Ramanathan L. N., J.-W. Jang and N. L. Owens, "Emerging Reliability Challenges in Electronic Packaging", *IEEE 48th Annual International Reliability*, 2008.

Chapter 2 Reliability issues in flip-chip packages

2.1 Introduction

Flip-chip assembly of chips on substrates has been in existence for decades since the first developed in the 1960's [1] by IBM [2]. With the industrial trend of electronic products and systems moving towards lead-free, miniaturization, lightweight and high reliability, flip-chip packages are widely used in many electronic applications for high I/O density, small profile, high performance and low cost [3]. Lead-free solder ball grid array (BGA) plays a very important role in flip-chip technology as it provides both mechanical supports and electronic connections between a chip and a substrate. Accordingly, many efforts have been made to improve the reliability of solder joints in flip-chip plastic ball grid array (FC-PBGA).

In this chapter, some literatures regarding reliability issues in flip-chip packages were reviewed and summarized to serve as foundations of the researches in the following chapters. Reliability of flip-chip packages is affected by many issues, e.g., thermal cycling, electro-migration, high-temperature excursion, size effect. Specifically, literatures about thermal cycling, electro-migration and size effect were mainly concerned in this chapter as they are the most common reliability issues in solder bumps

2.2 Thermal cycling

In a working process, electronic components in packages generates a lot of heat. Also, electrical currents in traces or resistances induce Joule heating within packages. With increasing integrated scale and working power of circuit, electronic packages generate more heat and experience higher temperature. Generally, components in flip-chip assembly are made by some materials with different coefficients of thermal expansion (CTE). For example, CTE of Model RR4 PCB is 18 ppm/K [4], Cu is 17 ppm/K [5], Si is 2.6 ppm/K [6] and SiO₂ is 0.4 ppm/K [5]. Due to a cyclic working-on and off status

of packages and various ambient temperatures, mounted components with different materials expand or shrink to different level. The constraint between them results in thermal stress among electronic packages. For a typical structure of a FC-PBGA, thermal stress is caused by CTE mismatch of chip, solder balls and substrate. With damage accumulated in thermal cycling, fatigue void expands to final failure of the package, as presented in **Fig. 2. 1**.

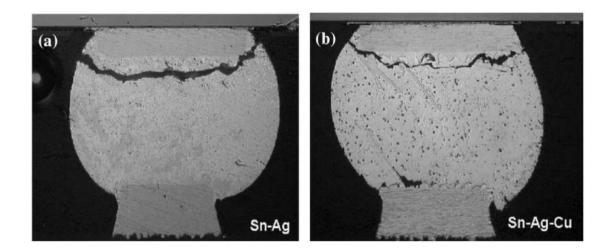


Fig. 2. 1. Thermal fatigue cracks in (a) Sn3.5Ag solder joint and (b) Sn3.8Ag0.7Cu solder joint [7]

Mechanical behaviours of electronic components under thermal cycling are usually determined by their material thermal-mechanical properties and microstructures. For microstructure of a solder bump, effects of miniaturization and IMC layer evolution under aging are specifically reviewed. For thermal-mechanical properties, elasticity, plasticity and creep behaviours are mainly concerned in this section

2.2.1 Microstructure of solder bumps

Intermetallic compounds (IMC)

During reflow assembly process, metallurgical reactions between liquid solder alloy and metallized copper bond pad produce intermetallic compounds (IMC) interfaces of bonded materials. Also, thickness of the produced IMC layer increases under aging conditions when electronic components experience thermal loadings.

Interfacial reaction between Cu and Sn results in a formation of Cu_3Sn and Cu_6Sn_5 IMC layers, as presented in **Fig. 2. 2**. Some electronic packages employ a thin Ni layer between solder and copper pad to prevent an over-consumption of copper pad. The IMC layers formed between Ni and Sn are more complex than that between Cu and Sn, as illustrated in **Fig. 2. 3**. Two layers are detected within this IMC structure: a very thin Ni-Cu-Sn IMC layer and a (Cu, Ni)₆Sn₅ intermetallic [**8**, **9**].

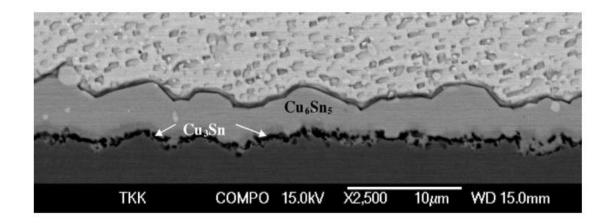


Fig. 2. 2. Electrolytic Cu/SnAgCu diffusion couple annealed at 125 °C for 1000 h [8]

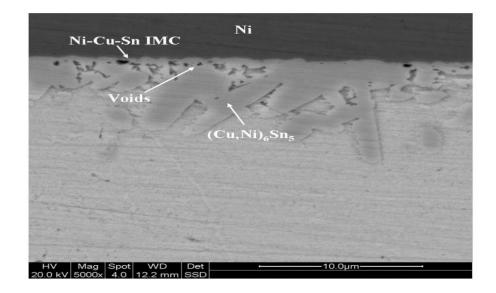


Fig. 2. 3. BSE image of the structure of the IMC layer at Ni side in the Cu/Sn/Ni solder joint with 100 μm-height [9]

After its formation in reflow, a growth of interfacial IMC layer can be observed during service of electronic devices, as the solder bump is usually exposed to high temperature [10]. In order to investigate the growth of IMC layers by experiments, solder bumps were stored in a high temperature environment, i.e., over 100 °C, to accelerate the growth process of interfacial IMC layers. According to some previous studies, relationship between thickness of an interfacial IMC layer and aging time is usually reported to follow parabolic law [11, 12]:

$$H = h_0 + K \times \sqrt{t} , \qquad (2-1)$$

where *H* is the thickness of the interfacial IMC layers after aging; h_0 is the initial thickness of the interfacial IMC layers; *K* is diffusion coefficient; *t* is aging time. The diffusion coefficient *K* is the slope of the $H-\sqrt{t}$ curve, which can be obtained by curve fitting. The diffusion coefficient *K* is involved in the Arrhenius equation as growth on IMC layer is a temperature-controlled process. The Arrhenius equation is correlated with the activation energy of the growth of interfacial IMC layers [13]

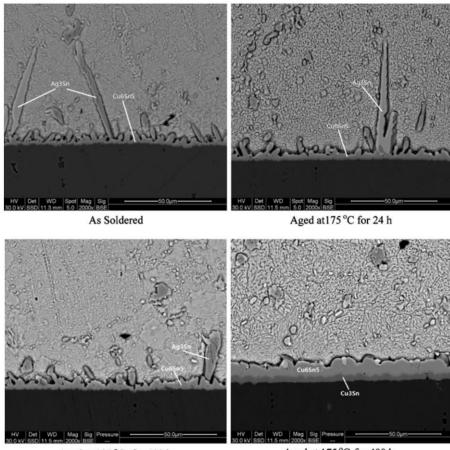
$$K = A \exp \left(-\frac{E}{RT}\right) , \qquad (2-2)$$

where A is a temperature-independent pre-exponential factor; E is the activation energy of growth of interfacial IMC layers; R is the ideal gas constant; T represents the absolute temperature. This equation can be utilised to derive the activation energy of a growth of IMC layers in aging.

In the growing process of Cu_6Sn_5 and Cu_3Sn IMC layers, morphology of Cu_6Sn_5 layer transfers gradually from dendritic to scalloped-shape after prolonged aging; while Cu_3Sn IMC layers remains layer-shape throughout aging process (**Fig. 2. 4**). Generally, two types of mechanisms are considered as possible contributes to morphology evolution of Cu_6Sn_5 IMC layer: variation of diffusion distance [**14**] and curvature effect [**15**].

As an evolution of interfacial Cu₆Sn₅ layer morphology is resulted by growth of interfacial Cu₆Sn₅ layer, the evolution is determined by inter-diffusion and reactions

between Sn and Cu atoms during aging. It has been proved that Cu atoms diffuse through thin Cu₃Sn layer quickly, but take a longer time through the interfacial Cu₆Sn₅ layer [**16**]. This fact is due to a longer diffusion distance in Cu₆Sn₅ IMC layer. Furthermore, diffusion distance in Cu₆Sn₅ layer varies with locations at a peak or a valley of scallops. It is longer at a peak and shorter at a valley. Consequently, it can be expected that Cu atoms from UBM pass through faster at a valley and react with solder, forming extra Cu₆Sn₅ IMC in the valley. Therefore, the morphology of the Cu₆Sn₅ layer is gradually flattened during aging [**14**].



Aged at 125 °C- for 400 h

Aged at 175 °C-for 400 h

Fig. 2. 4. Micrographs of cross-sectional views of IMCs during isothermal aging [17]

Curvature is considered as another factor affecting morphology evolution of interfacial Cu₆Sn₅ layer in aging. Difference of curvature rates at peaks and valleys can lead to Cu atom concentration gradient. Therefore, Cu atoms move from peaks to valleys as the atom concentration of peaks is higher than valleys. As a consequence, growth of Cu₆Sn₅ IMC at peaks is hindered and growth at valleys is motivated [**15**]. After a morphology

transition in interfacial Cu₆Sn₅ IMC layer, it keeps gradual growing as a layer-shape with relatively more even thickness.

Apart from morphology changes, materials of a typical IMC layer, Cu₃Sn and Cu₆Sn₅, have stiffer mechanical properties than solder and higher melting temperature. A brittle nature of IMC materials has been reported by [**8**, **18**] to impact reliability of solder bumps in chip-level devices. In their investigation, Laurila et al. [**8**], pointed out that due to IMCs' inherent brittle mechanical behaviours and tendency to generate voids and defects, thick IMC layer at the solder/pad metal interface may degrade the reliability of the solder bump. Due to their relative high melting temperature, Cu₃Sn and Cu₆Sn₅ IMCs present almost no creep behaviour under working temperature of electronic packages. The mismatch of mechanical properties between solder and IMC layer results in stress concentration at interface of solder and pad. Therefore, these locations become the most critical area in electronic packages under thermal stress. Details of mechanical properties of IMC materials are reviewed in Section 2.2.2.

Besides, in Sn-Ag and Sn-Ag-Cu alloys, reaction of Sn and Ag atoms generates Sn-Ag intermetallic compounds. For eutectic Sn-Ag3.5 alloy, its microstructure is composed of Ag₃Sn and β -Sn matrix. Due to its low content in the alloy, Ag₃Sn forms some particles dispersed in alloys. However, its size, shape and distribution are not uniform under different conditions. A main influencing factor of Ag₃Sn is supposed to be cooling rate during solidification of liquid alloy (**Fig. 2. 5**).

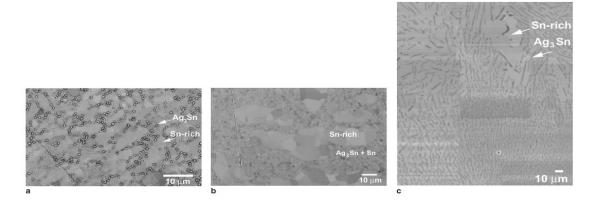


Fig. 2. 5. Microstructure of Sn-3.5Ag solder upon different cooling rates: (a) 24K/swater quenching, (b) 0.5K/s-air cooling, (c) 0.08K/s-furnace cooling [20]

Temperature cooling rate in (c) of **Fig. 2. 5** is close to the equilibrium condition in Sn-Ag alloy solidification. Large rod-like Ag_3Sn IMCs are randomly distributed in a Sn-rich matrix. Real cooling rate in solder joints is much higher than equilibrium condition. Under this condition, the alloy phase is composed by larger Sn-dendrites and some dispersed spherical Ag_3Sn IMCs. For the higher cooling speed, a refined microstructure of a dense eutectic mixture of Sn and Ag_3Sn dispersed in a Sn-rich matrix can be observed.

Effects of miniaturization of packages

In responding to higher electrical performance and miniaturization in electronic products [20], BGA density of interconnections increases very fast, resulting in a significant decrease in pitch/size of solder bumps. As a result, the size of solder bumps is becoming smaller in electronic packages, which leads to a reduction of stand-off height (SOH) of solder bump. SOH is defined as a total height of IMC layers and solder bulk. According to [21, 22], SOH decreases from 80-100 μ m to 20 μ m when bump pitch reduces from 200 μ m to 50 μ m in packages.

According to the research of [23], SOH had a significant effect on Cu₆Sn₅ IMC thickness and proportion in a Cu/Sn/Cu sandwich structure. The cross-sectional back-scattered electron (BSE) mode SEM images of the sandwich structure with 100, 50, 20 and 10 μ m SOH are presented in Fig. 2. 6. The formed IMC layer was identified as Cu₆Sn₅ by EDS analysis. Generally, IMC layer thickness refers to a total thickness of IMC at both chip side and substrate side of a solder joint. Defining a mean value of IMC thickness by dividing the measuring area of IMC by the length of interfacial IMC in the solder joint, changes of IMC thickness and proportion in the solder joints with the reducing SOH are presented in Fig. 2. 7.

In some past researches about mechanical behaviours in large size solder bumps, morphology of IMC layers was usually neglected or treated as a flatten surface [24, 25]. Under macro size scale, this assumption brings minor error as IMC layer takes a very low proportion in a solder bump. Under an effect of aging, only average thickness of

IMC layer need to be considered in the researches of mechanical behaviours in a solder bump. However, the morphology of IMC layer cannot be neglected in those researches of solder bumps under micro scale.

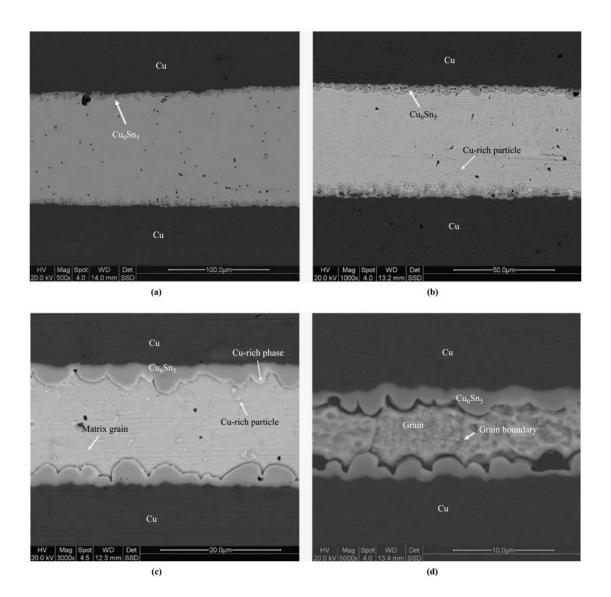


Fig. 2. 6. Cross-sectional BSE mode SEM images of the Cu/Sn/Cu solder joint with(a) 100 μm SOH; (b) 50 μm SOH; (c) 20 μm SOH; (d) 10 μm SOH [23]

Another important effect on solder bump behaviours induced by miniaturization is anisotropy of Sn matrix. For most lead-free material, e.g., Sn-Ag-Cu, Sn-Ag, the main constituent is solder, which is usually over 95%. The morphology of a Sn-Ag-Cu solder microstructure is mainly influenced by solidification conditions. Ag₃Sn and Cu₆Sn₅ IMCs are formed in Sn matrix under a slow cooling rate, resulting in Sn-Ag-Cu eutectics. If the cooling rate increases, large amounts of Sn dendrites are formed as the alloy system deviates from an equilibrium state. Both Sn matrix and Sn dendrites, the main components of a Sn-Ag-Cu solder bump, have a same crystal lattice structure as β -Sn. The unit cell structure of β -Sn is body-centred tetragonal, which is composed of contracted diamond cubic as shown in **Fig. 2. 8** [26].

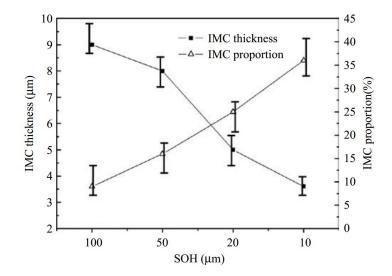


Fig. 2. 7. The mean Cu concentration changes in the solder bulk with the reducing SOH [23]

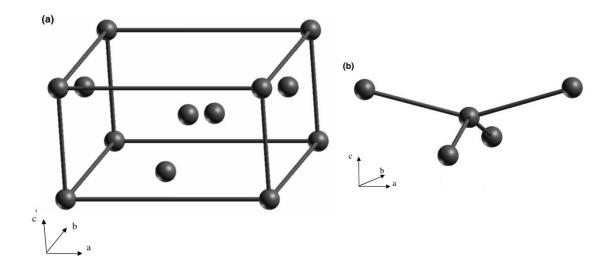


Fig. 2. 8. Crystal structure of β -Sn. (a) Body-centred tetragonal unit cell; (b) contracted diamond structure. The dimension of unit cell (along a and b in (a)) are 0.58318 and 0.31819 nm (along c) [26].

The crystal structure of β -Sn determines that some properties along c direction are different from a and b direction, which leads to anisotropy of β -Sn properties. In their study [27], Bieler *et al.* have investigated the eutectic structure and orientation of β -Sn crystal of Sn-Ag-Cu/Cu solder bump with 420 µm diameter under thermal cycling fatigue. According to their study, number of β -Sn crystal lattices in the solder bump is limiting and their orientations are distributed randomly. Besides, the orientation of β -Sn has effects on CTE and elastic modulus of the solder bump. Accumulative damage resulted by thermal fatigue also present a relationship with β -Sn orientation. Arfaei *et al.* have researched fatigue life of Sn-Ag-Cu/Cu solder bump with 500 µm diameter under shear test. They also found that there were few β -Sn crystal lattices in the solder bump and their numbers and orientations influenced shear fatigue life.

To summary, mechanical behaviours of solder bumps under micro scale are highly dependent on the orientations of β -Sn crystal lattice. Therefore, experimental tests about solder bumps under micro scale should adopt statistical method to investigate the effect of crystal structure orientation on their mechanical behaviours. Similar effects on electrical properties, e.g., electrical resistivity, can be also found in researches about electro-migration. It is discussed in details in Sections 2.3.

2.2.2 Mechanical properties of materials in a solder bump

A typical solder bump structure in BGA is usually formed by two copper pads and solder alloy. Due to the metallurgical reactions between liquid solder alloy and metallized copper pad mentioned in Section 2.2.1, IMC layer of Cu₃Sn and Cu₆Sn₅ can also be found in a solder bump after manufacturing process. Also, traces of Ag in Sn-Ag-Cu solder alloy are reacted with Sn, generating Ag₃Sn. Due to their high melting temperature, the IMC material Cu₃Sn, Cu₆Sn₅ and Ag₃Sn presents only elastic behaviours under thermal cycling, while Sn presents obvious visco-plastic behaviours. Therefore, elasticity of IMCs and visco-plasticity of solder are focused in this section.

Elasticity

Due to the micro size of IMC layer thickness and IMC particle, it is difficult to carry

out experimental studies on the interfacial IMCs in solder joints. Therefore, some previous studies adopted numerical calculation to evaluate the elastic moduli of IMCs in solder bumps [**28-30**]. The ideal elastic properties of Ag₃Sn, Cu₆Sn₅ and Cu₃Sn investigated by calculation are listed in **Table 2. 1**. As discussed in Section 2.2.1, some materials in micro solder bumps contain limiting number of crystal grains, which may present different properties as bulk specimen. Hence, their grain anisotropy under micro scale was also calculated. Among the materials, both Ag₃Sn and Cu₃Sn were reported with notable anisotropy under micro scale based on the calculation [**28, 30**].

Table 2. 1. Summary of the elastic properties of Ag₃Sn, Cu₆Sn₅ and Cu₃Sn based oncalculation [28-30].

	Shear modulus (GPa)	Young's modulus (GPa)	Poisson's ratio	Anisotropy
Ag ₃ Sn	28.6	77	0.347	Yes
Cu ₆ Sn ₅	46	119	0.29	
Cu ₃ Sn	56	147	0.315	Yes

However, the mechanical properties presented in **Table 2. 2** are based on ideal crystal structures of IMC materials. These are probably different from the properties of IMCs in solder bump as they usually contain some crystal defects. Some researches based on experimental methods were also carried out to investigate mechanical properties of IMCs.

Due to the micro size of interfacial IMC layers, positioning accuracy involved in mechanical tests of a micro scale solder bump is highly required, which is beyond capability of traditional tensile or shear test rigs. Therefore, in order to conduct tests on the IMCs, nano-indentation platform, which is usually equipped with nano-scale indenters and accurate positioning system, are widely used in evaluating the Young's modulus and hardness of interfacial IMC layers in solder joints, e.g., interfacial Cu₆Sn₅, Cu₃Sn and Ni3Sn4 [**31**, **34**]. The mechanical properties of IMCs in a solder joints obtained by nano-indentation tests is presented in **Table 2. 2** [**31- 33**].

Materials	Specimens	Hardness (GPa)	Reduced Modulus, E _r (GPa)	E (GPa)	References	
Cu ₆ Sn ₅	Sn-3.5Ag/Cu	6.1±0.5	123±6	125±7	[31]	
	Sn-37Pb/Cu	5.6±0.4	116±4	116±4	[31]	
	Bulk	6.3±0.3	114±1	115±2	[31]	
	Sn-3.8Ag- 0.7Cu/Cu	5.7±0.5		97±3	[32]	
Cu ₃ Sn	Sn-3.5Ag/Cu	5.7±0.6	132±5	136±6	[31]	
	Bulk	5.7±0.3	120±6	122±6	[31]	
Ni ₃ Sn ₄	Sn-3.5Ag/Ni	8.1±0.6	140±8	143±9	[31]	
	Sn-37Pb/Ni	8.9±0.6	136±6	138±7	[31]	
Cu-Ni- Sn IMC	Sn–3.8Ag– 0.7Cu/Ni-Au	7±1		160±5	[32]	
	95.5Sn- 3.8Ag- 0.7Cu/ENIG			207±6 (0 h); 165±3(260h); 146±3(500h)	[33]	

Table 2. 2 . `	Young's	modulus a	and hardness	of	various	IMCs
-----------------------	---------	-----------	--------------	----	---------	------

Visco-plasticity/Creep

In general, inelastic deformation in crystalline solids is a rate-dependent behaviour. Visco-plasticity usually describes rate-dependent plasticity in solid metals, in which crystallographic slip is the dominant process. Some researchers have carried out experimental methods to investigate the rate-/temperature-dependent stress-strain response of lead-free solders in bulk as well as in solder bump [23, 35]. They employed various strain rates and temperatures to evaluate their effect on the mechanical properties of solder bump, such as the Young's modulus, yield stress and ultimate strength. All of the experimental results presented that the Young's modulus, yield stress and ultimate strength increase with the strain rate, while an increase in temperature showed opposite effects.

Creep behaviour is generally defined as a progressive deformation of a material at a constant stress [36]. It usually occurs at high homologous temperature (current temperature/melting temperature) and stress. For most metals and alloys, creep behaviour is significant when material temperatures is over 30% of its melting point [37]. Generally, a whole process of creep can be divided into three stages, as presented in Fig. 2. 9: the primary creep, the secondary or constant rate creep and the tertiary creep. Creep behaviour is usually featured in the slope of curve, i.e., $d\epsilon/dt$ or $\dot{\epsilon}$. Following a sudden strain in specimen, ε_0 , creep rate decreases with time in the primary stage. Then it keeps steady as a constant value in the secondary stage. Finally, the cross section of specimen shrinks rapidly and creep rate increases until final fracture in the tertiary stage.

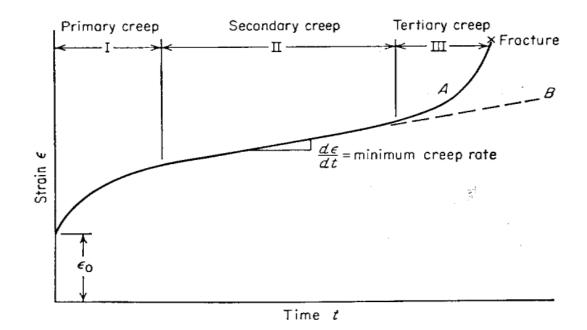


Fig. 2. 9. Typical creep curve showing the three steps of creep. Curve A, constant-load test; Curve B, constant-stress test [36]

The secondary stage of creep process is regarded as the most important feature to assess the material creep resistance. In actual situation, creep is hard to describe as it depends on many factors, e.g., loading rate, temperature, residual stress. However, the secondary stage creep (steady rate creep) is sufficient to be defined as material creep behaviour (Curve B in **Fig. 2. 9**). The formula describing steady rate creep is a relationship between creep strain rate and function of temperature and stress,

$$\dot{\varepsilon} = f(T,\tau) \quad . \tag{2-3}$$

If a low or medium stress is applied to specimen, this relationship can be described by power law, also known as Dorn equation [**38**],

$$\dot{\varepsilon} = A \; \frac{Gb}{RT} \; D \; \left(\; \frac{b}{d} \; \right)^p \left(\; \frac{\tau}{G} \; \right)^n \; , \qquad (2-4)$$

where A and p are constants related to microstructure and grain size, E is the Young's modulus, n is stress exponent, G is shear modulus, b is Burgers vector, D is diffusion coefficient, d is grain size, τ is shear stress, R is the Boltzmann constant, T is absolute temperature. This equation can precisely describe the steady rate creep and rupture in the third stage of SnPb solder. In Equation 2-4, the diffusion coefficient D is considered as a time-function rather than a constant in creep behaviour. Thus, if think of introducing time-influences, replace D with $D = D_0 \exp(-\frac{Q}{RT})$, Equation 2-4 can be modified as,

$$\dot{\varepsilon} = A \ \frac{Gb}{RT} \ D_0 \ \left(\frac{b}{d}\right)^p \left(\frac{\tau}{G}\right)^n \exp\left(-\frac{Q}{RT}\right). \tag{2-5}$$

In most of real applications, temperature (T) is relatively high when material presents creep behaviour. Therefore, the effects of $\frac{1}{T}$ is much smaller compared with $\exp(-\frac{Q}{RT})$. Here Q is activation energy. Besides, shear modulus (G) of metal fluctuates slightly with temperature changes. For further simplification of Equation 2 - 5, neglecting $\frac{1}{T}$, and treat G as a constant and replace all the constants as a single one, A₁, Equation 2 - 5 can be written as,

$$\dot{\varepsilon} = A_1 \left(\frac{\tau}{G}\right)^n \exp\left(-\frac{Q}{RT}\right) \ . \tag{2-6}$$

Neglecting the fluctuation affluences of shear modulus (G), the Dorn equation can be finally described as,

$$\dot{\varepsilon} = A_1'(\tau)^n \exp\left(-\frac{Q}{RT}\right) , \qquad (2-7)$$

which is also known as Norton power law and usually applied at low or medium stress [39].

Solder alloy has different magnitudes of stress exponents at different stress regions [40]. At high tress, however, this power law equation is not suitable anymore. In other word, the former power law breaks down under this condition. According to experiment data, strain increases more rapidly compare to the low or medium stress, which means creep rate is higher under this condition. The relationship now can be described as,

$$\dot{\varepsilon} = A_2 \exp(B_2 \tau). \tag{2-8}$$

The inconsistency of constitutive equations at low/high stress brings inconvenience in research application, especially in computer simulation. It is hard to define a certain transformation point of stress when carrying out finite element analysis. Therefore, Frost and Ashby proposed a hyperbolic sine model to analysis creep at both high and low stress load, which combines Equation 2 - 7 and Equation 2 - 8,

$$\dot{\varepsilon} = A_3 \frac{G}{T} [\sinh\left(\alpha \frac{\tau}{G}\right)]^n \exp\left(-\frac{Q}{RT}\right), \qquad (2-9)$$

where A_3 is a constant, α is stress level constant, n is stress exponent.

In some previous papers, both the power law model and the hyperbolic sine model were successfully applied in creep analysis. However, it may result in some problems when these models are applied in the creep behaviour of eutectic Sn-Ag or Sn-Ag-Cu alloys. Properties of microstructure in Sn-Ag or Sn-Ag-Cu alloys differ very much from Sn-Pb solders. "The biomaterial system Sn and Pb solidifies in a simple eutectic system with limited miscibility. The SnPb eutectic consists on solid solution strengthened Sn and Pn mixed crystals, which have a very similar deformation resistance. In contrast, the biomaterial system Sn and Ag or Sn and Cu solidifies in a complex system forming various intermediate phase" [41]. The two significant phases, Ag₃Sn and Cu₆Sn₅,

present much higher deformation resistance than Sn matrix. The mechanism of these two reinforced phases will be discussed in details in later section in this report. Due to this reason, Wises and Wolter proposed a model based on power law model [41, 42],

$$\dot{\varepsilon} = A_1 \left(\frac{\sigma}{\sigma_N}\right)^{n_1} \exp\left(-\frac{Q_1}{RT}\right) + A_2 \left(\frac{\sigma}{\sigma_N}\right)^{n_1} \exp\left(-\frac{Q_2}{RT}\right) , \qquad (2-10)$$

where A_1 and A_2 are constants, Q_1 and Q_2 are activation energy, σ_N is the deformation resistance relative parameter. The steady creep rate is expressed into two power law terms. The first term refers to the creep behaviour under low stress load when the climb creeps dominate and the second term corresponds to creep behaviour at high stress where glide/clime creep affect together. The data in the eutectic SnAgCu bulk specimens have validated the assumed two-term power law model.

These constitutive equations are the results of fitting curve process based on the data in bulk specimen. However, they need to be validated when applied to flip chip reliability assessment. Bulk specimen usually contains many grains and presents isotropic mechanical properties. In flip chip solder bumps, a number of grains decreases rapidly and may show some directional effects of mechanical properties, as introduced in Section 2.2.1. To investigate whether these creep constitutive equations can be applied to micro-size, some researches has compared the bulk specimens and solder joints [43, 44].

The results in **Fig. 2. 10** show that the equations mentioned above can still be applied in flip chip specimen. However, different constitutive relations are applicable for different conditions. The hyperbolic sine model can be used to describe the steady state creep rate of flip chip joints made by tin-lead alloys and bulk specimens made by Sn-Ag-Cu alloys. The single-term power law model can describe the steady state creep rate of flip chip joints made by Sn-Ag-Cu alloys. The figures illustrate that the creep behaviour of Sn-Ag-Cu solder in a flip chip bump is very different to that of bulk specimens. Meanwhile, the creep behaviour of Sn-Pb flip chip solder joints is very similar to bulk specimens. Based on these data comparisons, a conclusion can be made that the effects of size on creep behaviour in Sn-Ag-Cu alloys is more significant than that in Sn-Pb alloys.

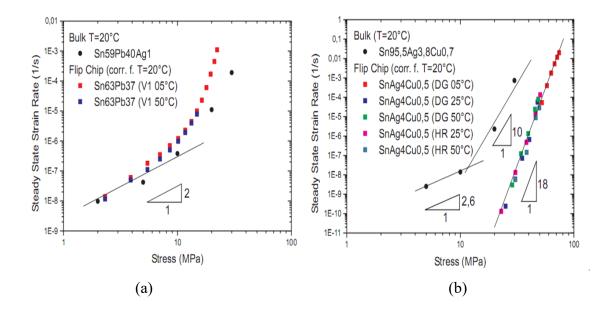


Fig. 2. 10. (a) Comparison of creep data from bulk Sn59Pb40Ag1 solder and flip chip Sn63Pb37 solder for a temperature of T=20 °C; (b) Comparison of creep data from bulk SnAg3.8Cu0.7 solder and flip chip SnAg4Cu0.5 for a temperature of T=20 °C; The flip chip creep data form T=5 °C, 50 °C was corrected for this temperature [43].

2.2.3 Fatigue prediction model

Focusing on mechanical wear-out mechanism, most fatigue failures are usually introduced by thermo-mechanical stress cause by mismatch of Coefficient of Thermal Expansion (CTE). In classical metallurgy, fatigue failure is defined as the permanent damage produced by cyclic stress and strain [45]. The generation of fatigue failure can be divided into two stages: (1) the initiation of micro-cracks; (2) the propagation of micro-cracks to macro-cracks. Generally, the direction of crack propagation is perpendicular to the direction of principal stress. However, in real application, it is difficult to monitor and track the initiation and propagation in components. Hence, researchers proposed some expedient failure indicators based on finite element analysis.

So far, W. W. Lee, *et al.*, has systematically reviewed fourteen solder joint fatigue models with an emphasis on summarizing the features and application of each fatigue model [46]. In that paper, the fatigue models were classified into five categories: stress-based, plastic strain-based, creep strain-based, energy-based and damage-based. For the

thermal fatigue-induced fracture form CTE mismatch, stain-based fatigue model is widely used in prediction of thermal cycle numbers. Hence, the models in this category are introduced in details in following parts.

Now there is a growing recognition of engineering fatigues that most fatigues happen under high stress and low numbers of cycles condition. **Fig. 2. 11** shows the test results under low numbers of cycles represented by the relationship between plastic stain $\Delta \varepsilon_p$ against cycles number *N*. From the figure results, a linear curved is obtained when they are both plotted in log coordinates. This relationship is best known and widely used as Coffin-Manson fatigue model [47, 48],

$$\frac{\Delta \varepsilon_p}{2} = \varepsilon'_f \ (2N)^c \ , \qquad (2-11)$$

where $\Delta \varepsilon_p/2$ is the plastic strain amplitude, ε'_f is the fatigue ductility coefficient defined by the stain intercept at 2N = 1 and approximately equal to the true fracture ductility ε_f for many metals, 2N is the number of stain reversals to failure (one cycle counts two reversals), c is the fatigue ductility exponent which varies between -0.5 to -0.7 for many metals.

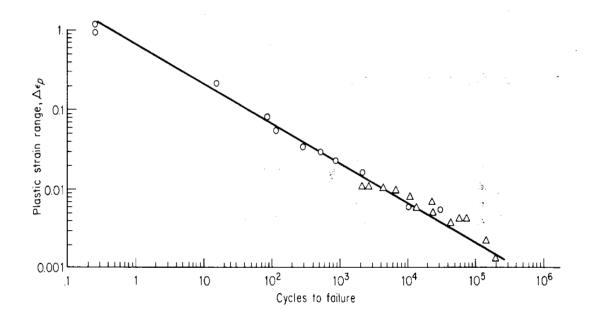


Fig. 2. 11. Low-cycle fatigue curve ($\Delta \epsilon_p$ vs. N) for Type 347 stainless steel. [47]

When considering the elastic strain which happens under low stress and high numbers of cycle, Basquin equation is adequate to describe the relationship [49],

$$N\sigma_a^p = C \quad , \tag{2-12}$$

where σ_a is the stress amplitude and *p*, *C* are empirical constants. Equation (2 – 12) can also be written as the form of Equation 2 – 13,

$$\sigma_a = \frac{\Delta \varepsilon_e}{2} E = \sigma'_f \ (2N)^b \quad , \qquad (2-13)$$

where $\Delta \varepsilon_e/2$ is the elastic strain amplitude, *E* is elastic modulus, σ'_f is the fatigue strength coefficient defined by the stress intercept at 2N = 1 and approximately equals to the true fracture stress σ_f , 2N is the number of stain reversals to failure (one cycle counts two reversals), b is the fatigue strength exponent which varies from -0.05 to -0.12 for most metals. For the entire strain regime, the combination of elastic and plastic strain is

$$\Delta \varepsilon = \Delta \varepsilon_e + \varepsilon_p \quad , \tag{2-14}$$

and the final model is described as [48]

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma_f'}{E} \ (2N)^b + \varepsilon_f' \ (2N)^c \ . \tag{2-15}$$

In finite element analysis, the equation will be simplified and written as [50, 51],

$$N = B_1 (\Delta \varepsilon_{acc,eqv}^{in})^{B_2} , \qquad (2-16)$$

where B_1 and B_2 are material constants, $\Delta \varepsilon_{acc,eqv}^{in}$ is the accumulated inelastic strain in the stable cycle which can be achieved after the third cycle in thermal cycling test. The term $\Delta \varepsilon_{acc,eqv}^{in}$ can be obtained by summing the plastic strain $\Delta \varepsilon_p$ and creep strain $\Delta \varepsilon_c$ which are derived from finite element analysis.

2.3 Electro-migration

In modern microelectronic industry, solder joints are designed to carry 0.2 A of electrical current, and this will be doubled in the near future according to [52]. This results that an average current density through a 50 μ m-diameter solder bump may approach 10⁴ A/cm². With the need of miniaturization of electronic packages, diameter and pitch of BGA may further decrease. This demands a reducing cross-section of conductive lines and solder interconnects, while on the other hand, they are expected to conduct a higher current density. At the same time, as Joule heating generated by electrical current is proportional to square of the current density, the local temperature of conductive lines and solder bumps will increase substantially. During service, the solder joints experience a temperature increase of more than 100 °C, to approximately 82% and 76% of the melting temperatures of eutectic Sn-Pb and Sn-Ag-Cu, respectively [53]. As a consequence, under the joint effect of a high current density and a high homologous temperature, diffusion of atoms in crystal lattice is anticipated [54]. This proves that electro-migration (EM) is an important reliability issue in the application of high current density packages.

2.3.1 Driving forces of atomic transport in EM

Electro-migration (EM) is usually defined as a diffusion controlled mass transport phenomenon due to the application of electrical current. In a previous study by Huntington and Grone, they proposed that thermal-activated metal ion becomes free in the crystal lattice and is influenced by two opposing forces, i.e., a direct force and an electron wind force in a metal [55]. The direct force refers to the force applied by electrical field due to the applied electrical current. The electron wind force is described as a force experienced by a metal ion in the direction of the electron flow due to the momentum exchange between the moving electrons and the ion. In their study, the electron wind force was identified as the primary driving force responsible for an electro-migration failure in electronic interconnections. Therefore, the equation for the atomic flux due to EM (\vec{J}_{EM}) is described as:

$$\vec{J}_{EM} = \frac{N}{kT} e Z^* \vec{J} \rho D = \frac{N}{kT} e Z^* E D , \qquad (2-16)$$

where Z^* is a dimensionless quantity known as the effective charge or valence, which reflects the direction and the magnitude of the momentum exchange; e is the electron charge; N is the concentration of local atoms; \vec{j} is the current density; ρ is the electrical resistivity; E is the electric field strength; kT is the average thermal energy and D is the thermally-activated diffusivity, which could be further expressed as:

$$D = D_0 \exp\left(-\frac{E_A}{kT}\right) \quad , \tag{2-17}$$

where D_0 is the materials self-diffusion coefficient and E_A is the activation energy.

Moreover, due to a significant accumulated heat caused by electrical current, another atomic migration process, thermo-migration (TM), are triggered and influence the reliability of packages. Due to the differences in electrical resistance and thermal dissipation of components in the flip-chip interconnect structure (see Fig. 2. 12), it can be predicted that the heat accumulated at the chip side is larger than that at the substrate, which lead to an evident temperature gradient across solder joints. When this gradient increase highly enough, it can provide a considerable driving force for the diffusion of atoms.

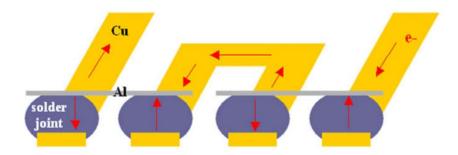


Fig. 2. 12. A schematic diagram of a flip chip interconnects including Al traces, solder joints and Cu conductors [53]

The driving force of TM comes from the energy transported by the moving atoms and

the interactions with heat carriers in the lattice [56]. The governing equation to describe the atomic flux caused by TM (\vec{J}_{TH}) is [57]:

$$\vec{J}_{TH} = -\frac{NQ^*D_0}{kT^2} \exp\left(-\frac{E_A}{kT}\right) \nabla T \quad , \qquad (2-18)$$

where Q^* is the heat of transport and ∇T is the thermal gradient. The other terms in this equation have been defined below Equation 2 – 17. As a potential reliability issue for flip-chip solder interconnects, TM induced-void or crack formation has been introduced in the 2007 ITRS [58].

Moreover, based on the Nabarro-Herring model describing the equilibrium vacancy concentration, some vacancies are formed in the tensile stress region, while less vacancies are generated in the compressive stress area. So, there is a vacancy concentration gradient decreasing from the cathode to the anode [59]. Hence, the atom flux caused by hydrostatic stress gradient is a retardation to that caused by EM. The atomic flux under a mechanical force can be expressed as:

$$\vec{J}_s = -\frac{N\Omega D_0}{kT} \exp\left(-\frac{E_A}{kT}\right) \operatorname{grad}\sigma_M$$
, (2-19)

where $\sigma_M = \frac{\sigma_{xx} + \sigma_{yy} + \sigma_{zz}}{3}$ is hydrostatic stress, σ_{xx} , σ_{yy} and σ_{zz} are the stress values for three principle directions and $\operatorname{grad}\sigma_M$ is the field gradient of σ_M .

Some previous studies have proved that SnAgCu – the lead free solder alloy – shows more resistivity to electro-migration than SnPb. A possible explanation for this difference is given in terms of the back stress [60]. As the elastic modulus or stiffness of the SnAgCu solder is larger than that of SnPb, the back stress gradient in SnAgCu is predicted to be higher. Therefore, the effect of back stress is relatively larger for the SnAgCu solder than SnPb alloy, which means it presents more resistivity to EM. Moreover, if the stress balances with the wind force at a critical length, there is no net atomic flux, which has been known as the Blech condition [61]. Let $\vec{J}_{EM} + \vec{J}_s = 0$, the critical length can be obtained, as:

$$X_c = \frac{\Omega \sigma_c}{eZ^* \vec{j}\rho} \quad , \tag{2-20}$$

where X_c is the critical length and σ_c is the critical compressive yield stress. The effect of the critical length and the back stress in a solder were studied by Wei and Chen [62]. Their experimental study proved that the critical length in eutectic Sn-Pb solder could be calculated by Equation 2 - 20.

Based on the descriptions above, the total atom flux caused by electrical current can be expressed as the sum of the three components:

$$\vec{J}_{Total} = \vec{J}_{EM} + \vec{J}_{TH} + \vec{J}_s$$
 (2 - 21)

$$=\frac{N}{kT}eZ^{*}\vec{j}\rho D_{0}\exp\left(-\frac{E_{A}}{kT}\right)-\frac{NQ^{*}D_{0}}{kT^{2}}\exp\left(-\frac{E_{A}}{kT}\right)\nabla T-\frac{N\Omega D_{0}}{kT}\exp\left(-\frac{E_{A}}{kT}\right)\operatorname{grad}\sigma_{M}$$

Under a thermal cycling caused by electrical current, these driving forces of atomic transport can be found in a solder bump. Therefore, these atom fluxes resulted by different reasons should be quantified in order to investigate the importance of the driving forces.

2.3.2 Failures resulted by Electro-migration

So far, many studies focused on Pb-rich and Pb-free solder alloys to investigate electromigration [63-67]. In a Sn-Pb solder joint, the Sn and the Pb phase are distributed uniformly before electro-migration. According to [63], after 20-hour electronic current stressing, missing of intermetallic compounds and voids formation can be observed at the cathode. According to [65], during electronic current stressing, the Sn and the Pb phase segregate from each other as illustrated Fig. 2. 13, and then distribute again as shown in the figure. During distribution process, the solder diffuses into pad part and force the materials to move towards solder part, which may result in failures along the interface.

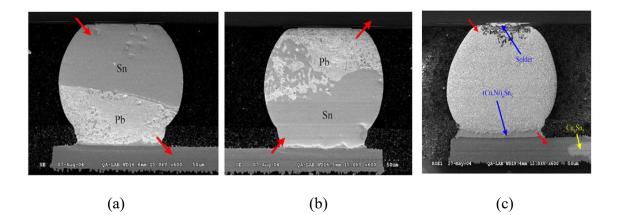


Fig. 2. 13. (a) & (b) Sn-Pb bumps under 0.6 A/135 °C at 306 h; (c) Sn-Pb under 0.6 A/125 °C at 616 h; the red arrows indicate the direction of electron current [**65**]

Similar separations can also be found in eutectic Sn-Bi solder bump since its microstructure and constitution are very close to eutectic Sn-Pb [68, 69]. The mass accumulation of Bi in a Sn58Bi solder bump solder joint under a current density of 5 $\times 10^3$ A/cm² at 75 °C is shown in Fig. 2. 14. As a dominant effective charge carrier, atoms of Bi moved along the direction of electron flow and accumulated at the anode side. Also, as a result of high level concentration of Bi atoms, a phase segregation is evident through the figure, which is like the Pb segregation with Sn in Sn-Pb alloy.

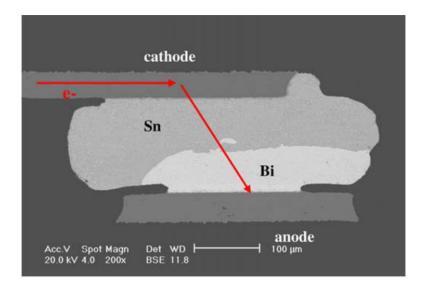


Fig. 2. 14. SEM image of mass accumulation of Bi in a Sn58Bi solder joint under a current density of 5 × 10³ A/cm² at 75 °C [16]

For most lead-free solder alloys, e.g., Sn3.5Ag, Sn4Ag0.5Cu, and Sn0.7Cu, the migration of the substitutional elements (Ag, Cu) is not significant compared with the self-diffusion speed of Sn. Therefore, the phase separation in lead-free alloys is hard to be observed. Instead, a fast interstitial diffusion of Cu, Ni and Ag, which caused dissolution of UBM and IMC, plays a dominant role in the failure of electro-migration in the lead-free solder systems.

Under the effect of electro-migration, another evident phenomenon of the microstructural evolution in solder bumps is phase coarsening. **Fig. 2. 15** illustrates this effect in Sn37Pb and Sn3.5Ag0.5Cu solder joints under a moderate current density of 6×10^2 A/cm2 at 125 °C [**70**]. The microstructures of Sn37Pb and Sn3.5Ag0.5Cu solder joints as-reflowed are illustrated in **Fig. 2. 15** (a) and (b), respectively. In these two figures, a fine sized Pb-rich phase or some particles of Ag₃Sn is dispersed in a Sn-rich matrix, respectively. After being stressed under electrical current for 600 h, the coarsening of the Pb phase and Ag-rich phase was evident, as shown in **Fig. 2. 15** (c) and (d).

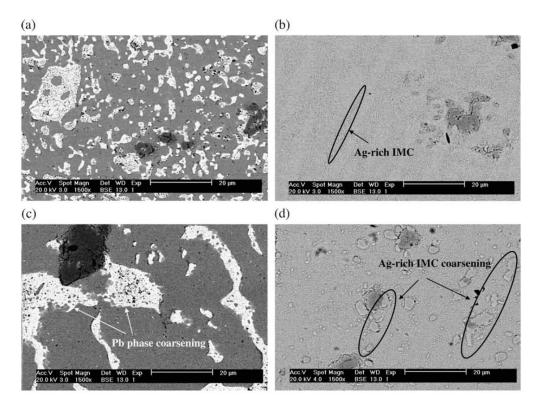
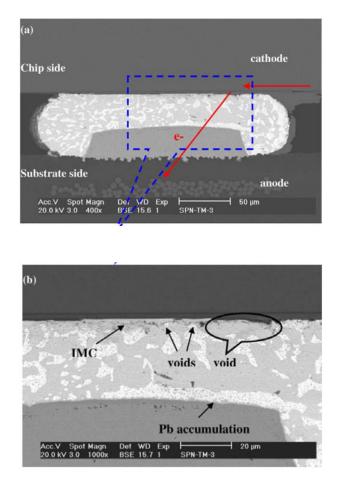
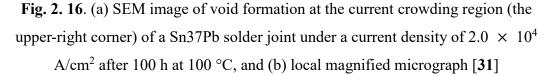


Fig. 2. 15. (a) Typical microstructure of a Sn37Pb solder joint as-reflowed, (b) a Sn3.5Ag0.5Cu solder joint as-reflowed, (c) Pb-rich phase coarsening in a Sn37Pb solder joint, and (d) Ag-rich IMC coarsening in a Sn3.5Ag0.5Cu solder joint [**70**]





The microstructural evolution caused by atoms transportation under electro-migration includes not only phase separation and coarsening, but also void formation at interfaces. This change affects the stress distribution under thermal fatigue evidently. Fig. 2. 17 displays the progress of void formation and expansion in Sn3.5Ag1.0Cu solder joints under a current density of 1.5×10^4 A/cm² at 125 °C [72]. The typical morphology of the interface between the trace and the solder before the experiment is presented in Fig. 2. 17 (a). After an electro-migration time of 75 h, as shown in Fig. 2. 17 (b), some voids were formed at the right upper corner of the interface. The formation of the voids gradually displaced the current to the surrounding areas which caused a lateral growth. Since the expansions of voids resulting in the redistribution of the UBM opening, where the current density is low at the beginning stage of electro-migration.

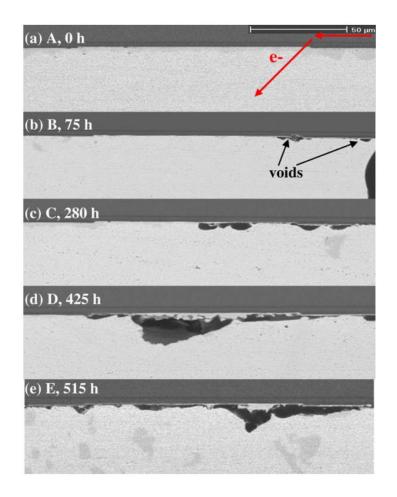


Fig. 2. 17. SEM images of the morphological evolution in Sn3.5Ag1.0Cu solder joints under a current density of 1.5 × 10⁴ A/cm² at 125 °C (a) before the experiment, the time point A, (b) after 75 h, 14% of the failure time, the time point B, (c) after 280 h, 53% of the failure time, the time point C, (d) after 425 h, 81% of the failure time, the time point D, and (e) after 515 h, 98% of the failure time, the time point E [72]

2.4 Summary

Some literatures about the reliability of solder joints under thermal cycling and electromigration were reviewed in this chapter. The effect of thermal cycling of packages on microstructure evolution in a solder interconnection was briefly presented. Also, the effects of miniaturization on the microstructures change were reviewed. A Large proportion of IMC layers and a transformation from multi-crystal to single-crystal behaviours were introduced in the solder bumps under micro-scale. A series mechanical properties of solder alloys, including elasticity and creep, were reviewed in this chapter. Moreover, a widely used fatigue model was discussed and transferred it into a form in FEM. Besides, the driving force of electro-migration, including three components, was discussed in this chapter. The effects of electro-migration on the microstructure degradation in solder interconnections from some previous work were also introduced.

Reference

- Bailey C. and Stoyanov S., "Reliability of flip-chip interconnect for fine pitch applications", *International Conference on the Business of Electronic Product Reliability and Liability*, 27-30 April 2004. Bangkok, Thailand. pp. 187-191.
- [2] Zhang Z., Park, S., Darbha K. and Master R. N., "Impact of usage conditions on solder joint fatigue life", *Electronic Components and Technology Conference*. 1 -4 June, 2010. Las Vegas, Nevada. pp. 14-19.
- [3] Chen F. X., Pang JHL. "Fatigue reliability analysis of Sn-Ag-Cu solder joints subject to thermal cycling", *IEEE Transition Device Material Reliability*, Vol 13 (2013), pp. 36–49.
- [4] Vandevelde B., Degryse D., Beyne E., et al. "Modified micro-macro thermosmechanical modelling of ceramic ball grid array packages", *Microelectronics Reliability*, 2003, 43 (2), pp. 307-318.
- [5] Sunohara M., Tolunaga T., Kurihara T., et al. "Silicon interposer with TSVs (through silicon vias) and fine multilayer wiring", *the 58th Electronic Components and Technology Conference*, Lake Buena Vista, FL, United States, IEEE, 2008, pp. 847-852
- [6] The W., Lihui G., Kumar R., et al. "200-mm wafer-scale transfer of 0.18-um dualdamascene Cu/SiO₂ interconnection system to plastic substrates", *IEEE Electron Devices Letters*, 2005, 26 (11), pp.802-804.
- [7] Frear D. R., Jang J. W., Lin J. K., et al. "Pb-free solders for flip-chip interconnects", *JOM*, 2001, 53(6), pp.28-33.
- [8] Laurila T., Vuorinen V., Kivilahti J. K., "Interfacial reactions between lead-free solders and common base materials", *Material Science Engineer*. R. Vol. 49 (2005), pp. 1-60
- [9] Wang, B., Wu F. S., et al., "Effect of Miniaturization on the Microstructure and Mechanical Property of Solder joints", 2009 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP).
- [10] Tan F. L. and Tso, C. P., "Cooling of mobile electronic devices using phase change materials", *Applied Thermal Engineering*, vol. 24 (2004), pp. 159-169.
- [11]Chan Y. C., So A. C. K., and Lai J. K. L., "Growth kinetic studies of Cu–Sn intermetallic compound and its effect on shear strength of LCCC SMT solder joints", *Materials Science and Engineering: B*, vol. 55 (1998), pp. 5-13.

- [12]Peng W., Monlevade E., and Marques M. E., "Effect of thermal aging on the interfacial structure of SnAgCu solder joints on Cu," *Microelectronics Reliability*, vol. 47(2007), pp. 2161-2168.
- [13]Choi S., Lucas J. P., Subramanian K. N., and Bieler T. R., "Formation and growth of interfacial intermetallic layers in eutectic Sn-Ag solder and its composite solder joints" *Journal of Materials Science: Materials in Electronics*, vol. 11 (2000), pp. 497-502.
- [14]Kim D., Chang J.-h., and Park J., "Formation and behaviour of Kirkendall voids within intermetallic layers of solder joints", *Journal of Materials Science: Materials in Electronics*, vol. 22 (2011), pp. 703-716.
- [15]Choi W. and Lee H., "Effect of soldering and aging time on interfacial microstructure and growth of intermetallic compounds between Sn-3.5Ag solder alloy and Cu substrate", *Journal of Electronic Materials*, vol. 29 (2000), pp. 1207-1213.
- [16]Kejun Z., Stierman R., Cheng C. T., Edwards D., Ano K., and Tu K. N., "Kirkendall void formation in eutectic SnPb solder joints on bare Cu and its effect on joint reliability," *Journal of Applied Physics*, vol. 97 (2005), pp. 024508-024508-8.
- [17] Li X. Y., Li F. H., Guo F., and Shi Y. W., "Effect of Isothermal Aging and Thermal Cycling on Interfacial IMC Growth and Fracture Behaviour of SnAgCu/Cu Joints", *Journal of Electronic Materials*, Vol. 40 (2011), No. 1, pp.51-61
- [18] Alam M.O., Chan, Y. C. and Tu K. N., "Elimination of Au-embrittlement in solder joints on Au/Ni metallization", *Journal of Materials Research*, 2004. 19(5), pp. 1303-1306.
- [19]Ochoa F., Deng X., Chawla N., "Effects of Cooling Rate on Creep Behaviour of a Sn-3.5Ag Alloy", *Electronic Materials*, Vol. 33 (2004), No. 12, pp.1596-1607
- [20] Wolf, M.J., Engelmann, G., Engelmann, G., Dietrich, L. and Reichl, H., "Flip chip bumping technology – status and update", *Nuclear Instruments and Methods in Physics Research A*, Vol. 565 (2006), No. 1, pp. 290-5.
- [21]Knickerbocker J.U., Andry P.S., et al., "Development of next-generation systemon-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection", *IBM Journal of Research and Development*, Vol. 49 Nos 4/5, pp. 725-53.
- [22]Plieninger R., Dittes M. and Pressel K., "Modern IC packaging trends and their reliability implications", *Microelectronics and Reliability*, Vol. 46 (2006), Nos 9/11,

pp. 1868-73.

- [23] Wang, B., Wu F. S., et al., "Effect of stand-off height on the microstructure and mechanical behaviour of solder joints", *Soldering & Surface Mount Technology*, Vol. 22 (2010), Iss 1, pp. 11 – 18.
- [24] Chiou Y. Ch., Jen Y. M., Huang Sh. H., "Finite element based fatigue life estimation of the solder joints with effect of intermetallic compound growth", *Microelectronics Reliability*, Vol 51 (2011), pp. 2319-2329.
- [25]Che F.X., Pang John H.L., "Characterization of IMC layer and its effect on thermomechanical fatigue life of Sn-3.8Ag-0.7Cu solder joints", *Journal of Alloys* and Compounds, 541 (2012), pp. 6–13.
- [26]Gong J. C., Liu C., et al., "Micromechanical modelling of SnAgCu solder joint under cyclic loading: Effect of grain orientation", *Computational Materials Science 39 (2007)*, pp. 187–197
- [27]Bieler T. R., Hairong J., Lehman L.P., et al., "Influence of Sn grain size and orientation on the thermomechanical response and reliability of Pb-free solder joints", *IEEE Transactions on Components and Packaging Technologies*, 32 (2008), pp.370-381.
- [28]Kumar S. and Jung J., "Mechanical and electronic properties of Ag3Sn intermetallic compound in lead free solders using ab initio atomistic calculation", *Materials Science and Engineering: B*, vol. 178 (2013), pp. 10-21.
- [29]Lee N. T. S., Tan V. B. C. and Lim K. M., "First-principles calculations of structural and mechanical properties of Cu₆Sn₅", *Applied Physics Letters*, vol. 88 (2006), pp. 031913-031913-3.
- [30] Jiunn C., Yi-Shao L., Ren C. Y., and Huang D. J., "First-principles calculations of elastic properties of Cu₃Sn superstructure," *Applied Physics Letters*, vol. 92 (2008), pp. 081901-081901-3.
- [31] Jang G. Y., Lee J. W., and Duh J. G., "The nanoindentation characteristics of Cu₆Sn₅, Cu₃Sn, and Ni₃Sn₄ intermetallic compounds in the solder bump", *Journal of Electronic Materials*, vol. 33 (2004), pp. 1103-1110.
- [32]Che F. X. and Pang J. H. L., "Characterization of IMC layer and its effect on thermos-mechanical fatigue life of Sn-3.8Ag-0.7Cu solder joints," *Journal of Alloys and Compounds*, vol. 541 (2012), pp. 6-13.
- [33] Xu L. and Pang J. H. L., "Nano-indentation characterization of Ni-Cu-Sn IMC

layer subject to isothermal aging," Thin Solid Films, vol. 504 (2006), pp. 362-366.

- [34] Yang P. F., Lai Y. S., Jian S. R., Chen J., and Chen R. S., "Nanoindentation identifications of mechanical properties of Cu₆Sn₅, Cu₃Sn, and Ni₃Sn₄ intermetallic compounds derived by diffusion couples," *Materials Science and Engineering: A*, vol. 485 (2008), pp. 305-310.
- [35] Amagai M., Watanabe M., Omiya M., Kishimoto K. & Shibuya T., "Mechanical characterization of Sn–Ag-based lead-free solders", *Microelectronics Reliability*, vol. 42 (2002), no. 6, pp. 951-966.
- [36] George. E. Dieter, "Mechanical Metallurgy" (1988). Singapore: McGraw-Hill
- [37]Kassner M. E., "Introduction" in Fundamentals of creep in metals and alloys, Second edition, Elsevier, Amsterdam, London, pp. 1-8, 2009.
- [38]Bird J. E., A. J.M., Dorn J.E., "Quantitative Relation between Properties and Microstructure", Israel University Press, 255, 1969
- [39]Lau J. H., "Thermal Stress and Strain in Microelectronics Packaging", Van Nostrand Reinhold, New York, 67, 1993.
- [40]Clech J. P., Review and analysis of lead-free solder material properties. Website: http://www.metallurgy.nist.gov /solder/, December 14, 2015.
- [41] Wiese S., Wolter K. J., "Microstructure and creep behaviour of eutectic SnAg and SnAgCu solders", *Microelectronics Reliability*, 44 (2004), pp. 1923-1931
- [42]Wiese S., Feustel F., Meusel E., "Characterisation of constitutive behaviour of SnAg, SnAgCu and SnPb solder in flip chip joints", Sensors and Actuators, 99 (2002), pp. 188-193
- [43] Wiese S., Schubert A., et al., "Constitutive Behaviour of Lead-free Solders vs. Lead-containing Solders-Experiments on Bulk Specimens and Flip-Chip Joints", *Electronic Components and Technology Conference*, 2001.
- [44] Wiese S., Wolter K. J., "Creep of thermally aged SnAgCu-solder joints", *Microelectronics Reliability*, 47 (2007) pp. 223-232.
- [45]Bannantine J. A., Comer J. J., Handrock J. L., "Fundamentals of metal fatigue analysis", Englewood Cliffs, NJ: Prentice-Hall, 1990, pp. 59
- [46]Lee W. W., Nguyen L. T., Selvaduray G. S., "Solder joint fatigue models: review and applicability to chip scale pacakges", *Mricoelectronics Reliability*, 40 (2000), pp. 231-244
- [47]Coffin L. F., Hitchcock J. O., "Low-cycle Fatigue", Met Engineering Q, 3, 4 (1963), pp. 15-24

- [48]Kilinski T. J., Lesniak J. R., Sandor B. I., "Modern approaches to fatigue life prediction of SMT solder joints", In: J. H. Lau, editor. Solder joint reliability theory and applications. *New York: Van Nostrand Reinhold*, 1991 (Chapter 13).
- [49] Lau J., Pao Y. H., "Solder Joint Reliability of BGA, CSP, Flip-Chip and Fine Pitch SMT Assemblies", New York: McGraw-Hill, 1997.
- [50] Mukai M., Kawakami T., et al., "Thermal fatigue life prediction of solder joints using stress analysis", Proc IEEE IEMT/IMC 1997, 1, pp. 204-208
- [51]Pang H. L., Low T. H., et al., "Lead-free 96.5Sn-3.5Ag flip chip solder joint reliability analysis", 9th international conference thermal and thermomechanical phenomena in electronic systems, 2 (2004), pp. 160-184.
- [52] Tu K. N., "Solder joint technology: materials, properties, and reliability", 1st ed, New York: Springer Science + Business Media LLC, 2007.
- [53]Chan Y.C., Yang D., "Failure mechanisms of solder interconnects under current stressing in advanced electronic packages", *EPA Progress in Materials Science*, 55 (2010), pp. 428-475.
- [54]Chen C, Liang S.W., "Electromigration issues in lead-free solder joints", *Journal of Material Science: Material of Electronics*, 18 (2007), pp. 259-268.
- [55]Huntington H. B, Grone A.R., "Current-induced marker motion in gold wires", Journal of Physics and Chemistry of Solids, 20 (1961), pp. 76-87.
- [56]Ye H., Basaran C., Hopkins D.C., "Mechanical degradation of microelectronics solder joints under current stressing", *The International Journal of Solids and Structures*, 40 (2003), pp. 7269-84.
- [57]Campbell D. R., Huntington H. B., "Thermomigration and electromigration in zirconium", *Physics Reviews*, 179 (1969), pp. 601-12.
- [58] Assembly and packaging section. In: *International technology roadmap for semiconductors*. San Jose: Semiconductor Industry Association; 2007.
- [59]Herring C., "Diffusional viscosity of a polycrystalline solid", Journal of Applied Physics, 21 (1950), pp. 437-45.
- [60] Ouyang F. Y., Chen K., Tu K. N., Lai Y. S., "Effect of current crowding on whisker growth at the anode in flip chip solder joints", *Applied Physics Letters*, 91 (2007), 231919.
- [61]Blech I. A. "Electromigration in thin aluminum films on titanium nitride", *Journal of Applied Physics*, 47(1976), pp. 1203-8.
- [62] Wei C.C., Chen C., "Critical length of electromigration for eutectic SnPb solder

stripe", Applied Physics Letters, 88 (2006), 182105.

- [63]Lee T. Y., Tu K. N., "Electromigration of eutectic SnPb and SnAg_{3.8}Cu_{0.7} flip chip solder bumps and under-bump metallization", *Journal of Applied Physics*, vol. 90 (2001) No.9, pp. 4052-4058.
- [64] Lai Y. S., Cheng K. M., et al., "Electromigration of Sn-37Pb and Sn-3Ag-1.5Cu/Sn-3Ag-0.5Cu composite flip-chip solder bumps with Ti/Ni(V)/Cu under metallurgy", *Microelectronics Reliability*, vol. 47 (2007), pp. 1273-1279.
- [65]Liu Y. H., Lin K. L., "Damages and microstructural variation of high-lead and eutectic SnPb composite flip-chip solder bumps induced by electromigration", *Journal of Materials Res*, vol. 20 (2005), pp. 2184-2193.
- [66] Huang Annie T., Gusak A. M., Tu K. N., "Thermomigration in SnPb composite flip chip solder joints", *Applied Physics Letters*, 88 (2006), 121911.
- [67] Meinshausen L., Weide-Zaage K., Fremont H., "Migration induced material transport in Cu-Sn IMC and SnAgCu microbumps", *Microelectronics Reliability*, 51 (2911), pp.1860-1864
- [68] Yang Q. L, Shang J. K., "Interfacial segregation of Bi during current stressing of Sn-Bi/Cu solder interconnect", *Journal of Electronic Materials*, 34 (2005), pp.1363-7.
- [69] Chen L. T., Chen C. M., "Electromigration study in the eutectic SnBi solder joint on the Ni/Au metallization", *Journal of Materials Research*, 21(2006), pp. 962–9.
- [70] Wu B. Y., Alam M. O., Chan Y. C., Zhong H. W., "Joule heating enhanced phase coarsening in the Sn37Pb and Sn3.5Ag0.5Cu solder joints during current stressing", *Journal of Electronic Materials*, 37(2008), pp. 469–76.
- [71] Yang D., Chan Y. C., Wu. B. Y., Pecht M., "Electromigration and thermomigration behaviour of flip chip solder joints in high current density packages", *Journal of Materials Research*, 23 (2008), pp. 2333–9.
- [72] Yang D., "Study on reliability of flip chip solder interconnects for high current density packaging", Doctor of philosophy thesis. Hong Kong: City University of Hong Kong; 2008.

Chapter 3 Modelling on reliability issues of flip-chip packages

3.1 Introduction

Due to their small size and complex structure, electronic packages are difficult to carry out experiments to validate their reliability. Moreover, normal test methods are not easy to find reasons of failures in time. Some reliability issues concerning time scale, e.g. electro-migration and thermo-migration, takes a very long time before failure occurrence. To solve the problems above, finite element method (FEM) was employed in electronics industry as a key assistant of design and test. Finite element analysis (FEA) has been widely used in electronic industry to assess reliability issues for decades.

Generally, FEM is defined as a numerical mthode for finding approximate solutions to boundary value problems based on partial differential equations. It can be used to simulate various reliability problems in electronics reliability. Numbers of papers adopted FEA to analyse the solder bumps subjected to thermal cycling test condition by using some commercial software, i.e. ABAQUS, ANSYS, MARC. Many issues about mechanical reliability, including IMC growth [1], voids in a single bump [2], effects of parameters in constitutive equation [3], have been discussed in previous studies. Some others employed FEA to research the migration in micro-bumps [4]. This chapter mainly concerned FE-models together with the methodology employed in some previous studies.

3.2 Two/three-dimensional models

Studies adopted different FEA geometric models including both two-dimensional and three-dimensional (2-D & 3-D) for different reasons. Here, some simulations about creep behaviour are reviewed and compared. Creep behaviour analysis in FEA is

different from elastic analysis. Unlike elastic deformation, it belongs to time dependent behaviour and program must calculate out all the data in each time increment. Therefore 2-D model with less elements and less equations number is a better choice to reduce calculation time. However, the validation of results from 2-D model must be strictly assessed compared with 3-D model. Generally, finite element models of solder bump reliability often adopt 2-D-plane strain models [**33**, **34**]. Meanwhile, some others use 3-D-1/8th symmetric model [**35-37**], 3-D-strip models [**38**] and 3-D-1/4 symmetric model [**39**].

Based on mechanic theory, there are 6 components to describe stress and strain of one point in three dimensional spaces respectively: σ_x , σ_y , σ_z , τ_{xy} , τ_{xz} , τ_{yz} for stress and ε_x , ε_y , ε_z , γ_{xy} , γ_{xz} , γ_{yz} for strain. In 2-D problems, the geometry of model lies in a plane and all loads are applied in the same plane. Two-dimensional problems can be divided into two categories: plane stress and plane strain. In plane stress condition, all the stress components related with the out-of-plane coordinate (*Z*) are zero, i.e., σ_z , τ_{xz} , $\tau_{yz} =$ 0. Plane strain considers a very large thickness compared with its in-plane dimensions, which means al the strain components associated with the out-of-plane coordinate (*Z*) are zero, i.e., ε_z , γ_{xz} , γ_{yz} . Theoretically, the thickness of model is zero in plane stress condition while it is infinite in plane strain condition. Therefore, results of the 2-Dplane stress and 2-D-plane strain are the two limits of 3-D problems. The whole 3-D are experiencing thermal-expansion introduced deformation thus 3-D geometry will generate more accurate results than 2-D models. Considering the complexity and calculating expense of 3-D models, a 3-D-strip model of the package was used sometimes.

Table 3. 1 shows analysis results of different models derived form a same solder joint package. All the data represent the status of the most dangerous bump in the model. Results have shown that the 2-D-plane strain and 2-D-plave stress indeed bound the 3-D models. Displacements (Δx and Δy) decrease from 2-D-plane strain model to 2-D-plane stress model. As a consequence, the total equivalent strain of 2-D-plane strain model and 3-D-1/8th model are higher than the rest two models. According to the von Mises yield criteria, the material will yield when the von Mises equivalent stress reaches the yield point. Plastic strain will follow the yield status of material. Therefore, 2-D-

plane strain model will yield first among all the models and develop higher equivalent plastic and creep strain. As a result, 2-D-plane strain model will obtain the lowest number of fatigue cycles based on fatigue model and 2-D-plane stress model tends to get the highest. Based on these conclusions, 3-D-1/8th model should be the first choice when using finite element analysis to assess the reliability owing to its adequate results. In application engineering, there is a widely accepted recognition that reliability assessment must be stricter than analysis results in order to secure safety issues. Therefore, if a 2-D model must be adopted to reduce the complexity and computing cost, 2-D-plane strain is highly recommended which generates more severe reliability prediction.

	Plane strain	3D 1/8 model	Strip model	Plane stress
Δx. horizontal (mm)	0.00534	0.004371	0.004189	0.004198
Δy. vertical (mm)	0.01897	0.01749	0.0148	0.01478
Eq total strain (%)	0.8064	0.7479	0.7138	0.7194
Eq plastic strain (%)	0.3233	0.2705	0.2494	0.1331
Eq creep strain (%)	0.3188	0.2831	0.2586	0.151
Strain energy density (MJ/m ³)	0.2562	0.2253	0.2208	0.2226

Table 3. 1. Displacement, Equivalent Strain Ranges and Strain Energy Density [38]

3.3 FEA of solder bumps under thermal cycling

Due to the structure of thermal circulation box, the equipment of mechanical test cannot set and sense the behaviours of sample simultaneously. Traditional test methods to assess the reliability of electronic packages under thermal cycles is using mechanical shear or tensile test to evaluate the strength of samples after thermal cycling aging [5]. The schematic drawing of shear testing on a solder joint is presented in **Fig. 3. 1**.

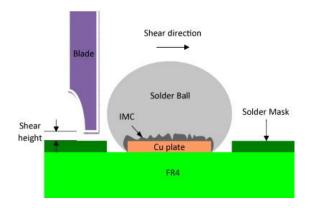


Fig. 3. 1. Schematic drawing of shear testing on solder joint [5].

Drawbacks of this experimental method are that the mechanical failure caused by the blade does not represent the failure of fatigue resulted by thermal cycling; moreover, stress state in the solder bump is hard to measure and investigate during thermal cycling. To overcome the drawbacks above, some researcher adopted FE-model to simulate the packages [6, 7]. Also, FEM was used to assess the effects of design factors on flip-chip packages under thermal fatigue [8]. Generally, FEA process involves generating a geometric model of a flip chip package and undergoing a temperature-cycling condition. Some constitutive equations describing mechanical behaviours of materials are applied. Structures of the packages and materials of the structure are the two key factors in the simulations of mechanical behaviours of flip-chip packages.

For the factor of structures in a solder bump, the voids resulted by defects or other failures have received some attentions. In [10] [11] and [12], Effects of voids with different sizes and locations in a solder bump were evaluated.

The FE-model of voids used in these studies are presented in **Fig. 3. 2** and **Fig. 3**. **3**. Moreover, some researchers adopted FEA in crack propagation analysis [20, 21]. According to [12], voids are not the place of crack initiation and propagation. The cracks usually start outside of the solder joint and grow toward inside of the solder bump. It also found that the creep strain is not always large with the existence of a void but is depending on the combination of the voids' position and size.

Generally, the analysis of thermal fatigue life consists of crack initiation and crack

propagation. With the help of FEA, the inelastic strains due to thermal fatigue can be identified. Hence, the Coffin-Manson law, which is a widely accepted fatigue life prediction model based on inelastic strains, was employed in simulation [13-19]. This equation has been discussed in details in Section 2.2.3.

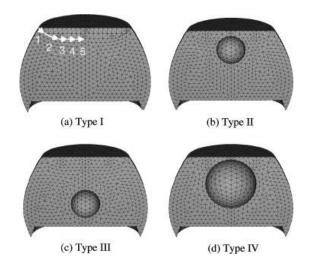


Fig. 3. 2. Void location and size in solder for FEA [11]

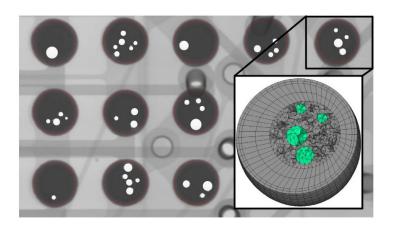


Fig. 3. 3. X-ray image of a BGA component section showing solder balls with multiple voids and exemplary mesh [10]

Normally, all the micro-structural changes of a solder bump results in a redistribution of the largest inelastic strains. The inelastic strains in thermal fatigue process also fluctuate with the temperature of the packages. According to [1], the inelastic strain accumulated in each cycle tends to be steady after the third cycle of thermal fatigue. Therefore, most papers adopt the accumulated inelastic strain of the model in third cycle

of thermal fatigue to estimate its fatigue life, as presented in **Fig. 3. 4**. With the combination of FEA and the Coffin-Manson law, effects of many structural changes on thermal fatigue life can be evaluated.

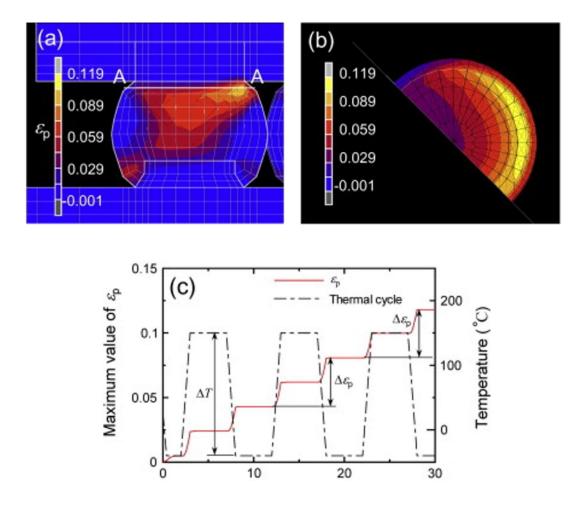


Fig. 3. 4. Example of FEA. (a) Distribution of ε_p in the solder bump after three thermal cycles. (b) Distribution of ε_p at the A–A plane in (a). (c) The history of the maximum value of ε_p together with the temperature profile [22]

For the materials used in FEA, electronic components, except for solder alloy, presents elastic properties under thermal cycle. These components usually include chips, substrates, copper traces, IMCs and underfills. The Hook's law was used to describe elastic property, which is relatively simple. However, due to its low melting temperate and soften stiffness, solder alloy presents inelastic behaviours during thermal loading. The studies mentioned above usually adopted the hyperbolic sine model, which has been introduced in Section 2.2.2, or the Anand constitutive equation, as below.

$$\dot{\varepsilon_p} = A \exp(-\frac{Q}{RT}) \left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}},$$
 (3-1)

where $\dot{\varepsilon_p}$ is the inelastic strain rate, A is the pre-exponential factor, Q is the activation energy, R is gas constant, T is absolute temperature, ξ is the multiplier of stress, σ is the equivalent stress, m is strain rate sensitivity. The evolution equation is as:

$$\dot{s} = \left\{ h_0(|B|)^a \frac{B}{|B|} \right\} \dot{\varepsilon}_p \quad ,$$
 (3-2)

Where $B = 1 - s/s^*$ and $s^* = \hat{s} \left[\frac{\varepsilon_p}{A} \exp(\frac{Q}{RT})\right]^n$, h_0 is the hardening/softening constant, a is the strain rate sensitivity of hardening/softening. The quantity s^* represents a saturation value of deformation resistances. \hat{s} is a coefficient, and n is the strain rate sensitivity for the saturation value of deformation resistance, respectively.

However, these models are not applicable to those solder bumps under micro-scale. At micro scale, a lead-free SnAgCu solder joint contains only one or a few crystal grains, and therefore, its mechanical behaviour transfers from polycrystalline to single crystal based one [23,24]. Therefore, a crystal visco-plasticity model is proposed by [25] for a micro-solder bump. In the study, it has been proved that the gradient of the equivalent stress in a crystal visco-model w larger than that from the traditional isotropic model.

3.4 FEA of solder bumps under electro-migration

Generally, experimental methods for testing the reliability of electronic packages under electro-migration apply current stress on samples to carry out an accelerating test. A drawback of for this method is that it takes a long time before failure of samples. As introduced in Section 2.3.2, the failure time of electro-migration is usually from 200 h to 500 h. Moreover, in order to ensure a relative shorter testing time, electrical currents, which are much larger than that in normal use of electronic packages, are applied to the samples. Some sensors for electrical resistivity testing are also used to measures the sample during experimental time.

To overcome the drawback and inconvenience of experimental method, FEA was adopted widely in estimation of reliability of solder bumps under electro-migration. Generally, FEA process involves generating a geometric model of a single bump and experiencing an electrical current load. According to the reviews in Section 2.3.1, electro-migration accompanies with thermo-migration, as the Joule heating effect induced by current is inevitable. Therefore, a coupled thermal-electrical analysis based FE should be employed before next step.

According to a coupled thermal-electrical analysis, distributions of current and temperature in the solder bump can be obtained. Moreover, distributions of the current density and the temperature gradient can be calculated from former results. Based on Equation 2 - 21, the atom flux caused by electro-migration is determined by the current density, the temperature gradient and the gradient of hydrostatic stress. If an estimation of stress factor is needed, a mechanical load can be applied to the model. A corresponding distribution of hydrostatic stress can be also obtained by FEA.

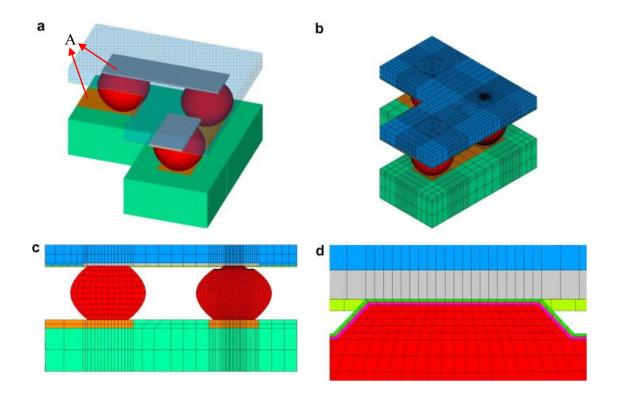
So far, many studies concerning electro-migration in a solder bump have adopt FEA to analysis distributions of current and temperatures [26-28]. A typical model of BGA involving the coupled analysis shows some similarities to the one of thermal-mechanical modelling, as presented in Fig. 3. 5.

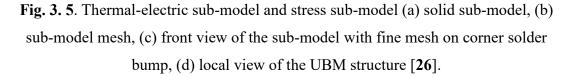
The difference between the two models is that the model for electro-migration includes metal traces to provide current flow path and voltage loading port. Component A in **Fig. 3. 5** is the copper traces in the model. The loading current provide the definition of current density at some boundaries. According to the Ohm's Law, the distribution of current density in other places can be calculated. Therefore, a material properties of electrical conductivity should be clearly defended. Moreover, some thermal boundary conditions on the external surfaces should be included in the model. Based on the heat transfer law, a definition of material properties of thermal conductivity is needed in the simulation.

Also, FE-models are used to analyse the reliability of joints under electro-migration in TSV package [29-31]. A typical structure of a TSV interconnection is illustrated in

Fig. 3. 6. Effects of different diameter of TSV interconnections and various current

loading types on the model are simulated in [31]. It also provided some design suggestions based on the simulated results at the end of [31].





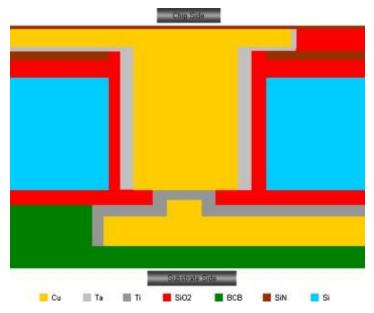


Fig. 3. 6. Schematic of TSV in Si interposer from IME [29].

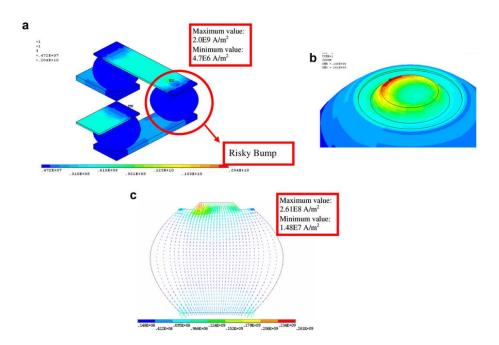


Fig. 3. 7. Current density distribution with current load 1.7 A (a) current density distribution for trace-and-bump, (b) local current density in corner risky bump, (c) current density vector contour for risky bump [**26**].

Many results for the previous studies have indicated that a current crowding effect was found at the interface of traces and interconnections. **Fig. 3. 7** gives an example of simulated results. Generally, some parts of electrical current changes their directions when the current enters solder joint from copper traces. According to FE results, current density at the area of current entrance is usually the highest value in the model, which indicates that the area is a potential failure place of electromigration.

The temperature and its gradient distribution in [26] are illustrated in Fig. 3. 8. It represents a typical distribution of temperature in coupled thermal-electrical. The difference of temperature distribution is very small while the temperature gradient is very large due to the size of the solder bump. Based on this fact, the temperature in a electrical package is usually treated as a uniform value. However, the factors induced by temperature gradient are of great importance, such as thermo-migration.

In FEA of electromigration reliability, the coupled thermal-electrical simulation is followed by an algorithm of void formation. The duration time dependent evolution equation of the local atomic concentration caused by an applied current is the traditional mass balance continuity equation [26, 32]:

$$\operatorname{div}(\vec{J}) + \frac{\partial N}{\partial t} = 0 \quad , \qquad \qquad 3-3)$$

where N is the normalized atomic concentration and \vec{J} is the total normalized atomic flux. The calculation of \vec{J} is based on the results of the coupled thermal-electrical stimulation. When the value of N reduced to a certain low value (below 20%), voids are formed at the corresponding area.

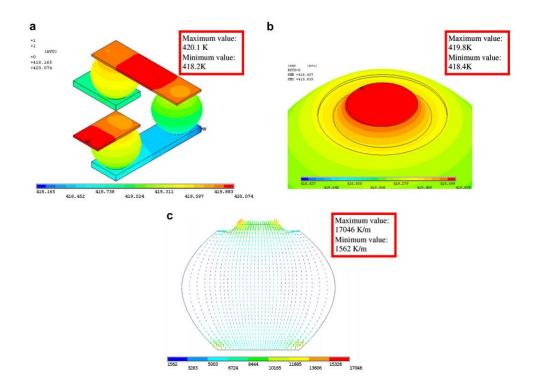


Fig. 3. 8. Temperature and its gradient distribution in sub-mode and solder bump (a) temperature distribution for trace-and-bump, (b) temperature distribution for corner bump, (c) temperature gradient vector contour for risky bump [26].

3.5 Summary

The chapter reviewed some literatures about the selection of 2-D/3-D FE-models and

the simulations about thermal cycling and electromigration. The advantages and disadvantages of 2-D and 3-D FE-models were compared and discussed. Some suggestions were proposed for the selection of the models in FEA. The method and process of simulation of an electronic package under thermal cycling were presented. Results of a typical modelling for evaluation of fatigue life were illustrated in this chapter. The thermal-mechanical properties used in FEA were also listed. Meanwhile, the model and the method employed in simulations of electromigration were displayed and discussed. Results of coupled thermal-electrical simulation proved that the critical failure area in a solder bump was usually located at the interface of solder bump and traces. Moreover, the governing equation used for voids formation simulation was mentioned at the end of this chapter.

Reference

- Chiou Y. C., Jen Y. M., Huang S. H., "Finite element based fatigue life estimation of the solder joints with effect of intermetallic compound growth", *Microelectronics Reliability*, 2011.
- [2] Huang Annie T., Gusak A. M., Tu K. N., "Thermomigration in SnPb composite flip chip solder joints", *Applied Physics Letters*, 88 (2006), 121911.
- [3] Schwerz R., Meyer S., et al., "Finite Element Modelling on Thermal Fatigue of BGA Solder Joints with Multiple Voids", 34th International Spring Seminar on Electronics Technogly 2011, pp. 380-385.
- [4] Liu Y. H., Lin K. L., "Damages and microstructural variation of high-lead and eutectic SnPb composite flip-chip solder bumps induced by electromigration", *Journal of Materials Res*, 20 (2005), pp. 2184-2193.
- [5] Tian Y., Hang C., et al., "Effects of bump size on deformation and fracture behaviour of Sn3.0Ag0.5Cu/Cu solder joints during shear testing", *Materials Science and Engineering A*, 529 (2011), pp. 468-478.
- [6] Lau J. H., Alto Palo, "Solder joint reliability of flip chip and plastic ball grid array assemblies under thermal, mechanical, and vibrational conditions", *Components, Packaging, and Manufacturing Technology: Part B*, vol.12 (1996), pp. 728-735.
- [7] Hong B. Z. "Thermal fatigue analysis of a CBGA package with lead-free solder fillets", Thermal and Thermomechanical Phenomena in Electronic Systems, 1998, pp. 205-211.
- [8] Yu Q., Jin J.C., Abe H., Shiratori M., "Study on influence of the design factors on the reliability of BGA solder joints", *Conference on Thermal & Thermomechanical Phenomena in Electronic Systems (2004)*, pp. 343-349.
- [9] Gong J., Liu C., et al., "Modelling of Ag₃Sn coarsening and its effect on creep of Sn–Ag eutectics", *Electronics Components and Technology Conference*, 2007, pp. 677-693.
- [10]Schwerz R., Meyer S., et al., "Finite Element Modelling on Thermal Fatigue of BGA Solder Joints with Multiple Voids", 34th International Spring Seminar on Electronics Technogly, 2011, pp. 380-385.

- [11]Yu Q., Shibutani T., et al., "Effect of process-induced voids on isothermal fatigue resistance of CSP lead-free solder joints", *Microelectronics Reliability*, 2008, vol. 48, Issue 3, pp. 431–437.
- [12]Bin Z. and Baojun Q., "Effect of voids on the thermal fatigue reliability of PBGA solder joints through submodel technology", *Packaging Technology*, 2008, pp. 6-10.
- [13] Ladani L. J., Dasgupta A. "Effect of voids on thermo-mechanical durability of Pbfree BGA solder joints: modelling and simulation", *International mechanical engineering congress and exposition (2005)*, pp. 1–6.
- [14]Kim D. S., Yu Q., Shibutani T., Sadakata N., Inoue T., "Effect of void formation on thermal fatigue reliability of lead-free solder joints", *the intersociety conference on thermal and thermomechanical phenomena in electronic systems (2004)*, pp. 325– 329.
- [15]Kariya Y., Niimi T., Suga T., Otsuka M., "Low cycle fatigue properties of solder alloys evaluated by micro bulk specimen", ASME InterPACK, 2005, pp. 1–6.
- [16]Kitano M., Kumazawa T., Kawai S., "A new evaluation method for thermal fatigue of solder joint", *the 1992 joint ASME/JSME conference on electronic packaging*, pp. 301–8.
- [17] Lau J. H., "Solder joint reliability of flip chip and plastic ball grid array assemblies under thermal, mechanical, and vibrational conditions", *IEEE Transaction Components Package Manufacturing Technology B*, 19 (1996), pp. 728–735
- [18] Mukai M., Takahashi H., et al., "Mechanical fatigue tests of solder bumps", Adv Electron Pack, EEP-26-1 (1999), pp. 449–455.
- [19]Q. Yu, ShiratoriM. "Fatigue-strength prediction of microelectronics solder joints under thermal cyclic loading", *IEEE Transact Compon Pack Manufact Technol*, 20 (1997), pp. 266–273.
- [20]B. Li, L. Yin, Y. Yang, X. Zhang, "FE Simulation of Size Effects on Interface Fracture Characteristics of Microscale Lead-Free Solder Interconnects", 2009 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP).
- [21] Alam M. O., Lu H., Bailey C.s, Chan Y. C., "Finite-Element Simulation of Stress Intensity Factors in Solder Joint Intermetallic Compounds", *IEEE Transactions on Devices and Materials Reliability*, vol. 9 (2009), No. 1, pp. 40-48.

- [22] Tohmyoha H., Ishikawaa S., et al., "Estimation and visualization of the fatigue life of Pb-free SAC solder bump joints under thermal cycling", *Microelectronics Reliability*, vol. 53 (2013), Issue 2, pp. 314-320.
- [23]Gong J., Liu C., Conway P. P., Silberschmidt V. V., *Electronics Components and Technology Conference (ECTC'56)*, San Diego, 2006, pp. 250–257
- [24] Matin M.A., Coenen E.W.C., Vellinga W.P., Geers M.G.D., Scripta Mater, 53 (2005), pp. 927–932.
- [25]Gong J., Liu C., et al., "Micromechanical modelling of SnAgCu solder joint under cyclic loading: Effect of grain orientation", *Computational Materials Science*, 39 (2007), pp. 187–197.
- [26]Liu Y., Liang L., Irving S., Luk T., "3D Modeling of electromigration combined with thermal–mechanical effect for IC device and package", *Microelectronics Reliability*, 48 (2008), pp. 811–824
- [27]Choi W. J., Yeh E. C. C., "Electromigration of flip chip solder bump on Cu/Ni(V)/Al thin film under bump metallization", *Electronic Components and Technology Conference*, 2002, pp. 1201-05.
- [28]Hsu Y. C., Shao T. L., Chen Chih, "Electromigration induced failure in SnAg3.8Cu0.7 solder joints for flip chip technology", *Electronic Materials and Packaging*, 2002.
- [29] Tan Y. C., Tan C. M., Zhang X. W., Chai T.C., Yu D. Q., "Electromigration performance of Through Silicon Via (TSV) – A modelling approach", *Microelectronics Reliability*, vol. 50 (2010), pp. 1336–1340.
- [30]Frank T., Moreau S., Chappaz C., et al., "Reliability of TSV interconnects: Electromigration, thermal cycling, and impact on above metal level dielectric", *Microelectronics Reliability*, vol. 53, Issue 1, pp. 17-29.
- [31] Jiwoo Pak, Mohit Pathak, Sung Kyu Lim and David Z. "Modeling of electromigration in Through-Silicon-Via based 3D IC" 2011 Electronic Components and Technology Conference.
- [32]Jing J. P., Liang L., Meng G., "Electromigration Simulation for Metal Lines", *Journal of Electronic Packaging*, vol. 132 (2010), 011002.

- [33] Pang H. L. J., Tan T. I., Lim G. Y., Wong C. L., "Thermal stress analysis of direct chip attach electronic packaging assembly", *IEEE 1997 Electronic Packaging Technology Conference*, pp. 170-176.
- [34] Michealides S. and Sitaraman S. K., "Effect of material and geometry parameter on the thermo-mechanical reliability of flip-chip assemblies", *IEEE Intersoc. Conference Thermal Phenomena*, 1998, pp. 193-200
- [35]Pang John H. L., Chong D. Y. R., Low T. H., "Thermal Cycling Analysis of Flip-Chip Solder Joint Reliability", *IEEE Transactions on Components and Packaging Technologies*, 2001, Vol. 24, No. 4.
- [36] Schubert A., Dudek R., et al., "Thermo-mechanical reliability analysis of flip chip assemblies by combined microdac and the finite element method", Advances in Electronic Packaging, *New York: ASME*, 1997, Vol. 2, pp. 1647-1654.
- [37] Schubert A., Dudek R., Michel B., "Material mechanics and thermo-mechanical reliability of flip chip area array packages", Advances in Electronic Packaging, *New York: ASME*, 1999, Vol. 1, pp. 181-188.
- [38]Pang John H. L., Chong D. Y. R., "Flip Chip on Board Solder Joint Reliability Analysis Using 2-D and 3-D FEA Models", *IEEE Transactions on Advanced Packaging*, Vol. 24 (2001), No. 4, pp. 499-506.
- [39]Cheng X., Liu C., Silberschmidt V.V., "Numerical analysis of thermo-mechanical behaviour of indium micro-joint at cryogenic temperatures", *Computer Material Science*, 2011, pp. 274-281.

Chapter 4. Microstructure geometry and shape

prediction of solder bumps in flip-chip packages

4.1 Introduction

This research aims to investigate thermal fatigue and electro-migration reliability of solder bumps in flip-chip package. Since the joint effects of these two issues of reliabilities are hard to evaluate precisely and effectively, finite-element analysis (FEA) is employed as a main method of the analysis. Evaluation of reliability in flip-chip packages can be simplified and accelerated by FEA; moreover, complex joint effects under the two reliability issues can be analysed.

Previous studies proved that the microstructure of solder bumps and geometry of design parameters showed great effects on their reliabilities [1] [2]. The microstructure of a solder bump in this research mainly refers to thickness and morphology of IMC layer, as presented in **Fig. 4. 1**. Some other additions in lead-free tin alloy, i.e. Ag, also react with Sn, resulting in the formation of Ag₃Sn IMC. The Ag₃Sn IMCs are usually dispersed articles distributed in Sn matrix. However, as the percentage of Ag in widely used solder alloy is very low and most part of solder bump is formed by Sn matrix [**3**], the IMCs formed by traced additions are neglected in this research. To ensure a reliable evaluation for reliability issues, this chapter presents thickness and morphology of IMC layers in solder bumps under micro-scale. The graph of thickness and morphology of the IMC layer, which are based on experimental observation, were dealt with statistically to gain its main features. The features are employed in FE-models as the shape of their IMC layers in following chapters.

Besides, an external shape of a solder bump is determined by geometries of some design parameters, including pad diameter (d), standoff height (h) and lower/upper contact

angle (θ), as presented in **Fig. 4. 1**. The pad diameter and standoff height (SOH) determine the size of solder bump and the array's pitch. The lower/upper contact angles are determined by volume of the solder.

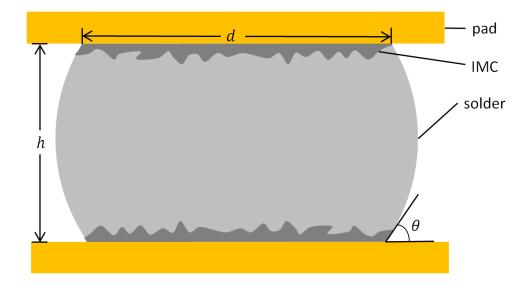


Fig. 4. 1. Schematic view of micro-structure and design parameters for a solder bump

According to [1], a distribution of stress in mechanical behaviours of electronic packages highly depends on these design parameters. The relationship of the diameter of solder balls, pad diameter, contact angle and standoff height of the bumps, and the influence of gravity on their geometry were investigated by an energy-based approach in this chapter. The profiles of solder bumps generated by the programming are used in the following chapters.

4.2 Microstructure geometry of solder bumps

Microstructures of solder bumps under macro scale (over 100 μ m SOH) were observed and reported in many previous works [4-6]. However, the morphologies in micro solder bumps reported by papers were different. The influences of the IMC morphology in large solder bumps were usually neglected, since the morphology of IMC in micro solder bumps affected their reliability much more than the solder bump under macro scale. This experiment aims to valid the IMC morphology in micro scale

and some samples of Sn/Cu structure were prepared and observed. Conventional fabricating methods in flip-chip packaging technology were not applicable in this experiment, since the samples were supposed to be micro scale. The height of solder layer in samples should be controlled precisely. Generally, traditional method to control the length of intervals is to use some gauges as a distance configuration, like micrometre and venire calliper. Resolution of venire calliper is much larger than 10 microns, while micrometre could reach minimum resolution of 10 microns and theoretically it is suitable for distance controlling here. However, considering the backward tolerance of screw thread, micrometre is not reliable to set a 10-micron interval, and physical gauges could not achieve the aim of controlling micro distance in this experiment. Therefore, electroplating was employed in this experiment. The rate of metal coating increase in electroplating is determined by electrical current and it can be very slow (1 μ m/1 min). By employing this method, the thickness of metal layer can be controlled by strength of applied electrical current and time and kept in a range of certain value for a long time. Another advantage of electroplating is that the thickness of metal coating layer is consistent on the whole surface of cathode, which is a necessary condition for requirements of this experiment.

4.2.1 Experimental procedure

Electroplating process

Electroplating is a process that uses electrical current to dissolve metal cations and form a coherent metal coating on an electrode. Under applied electrical current, mental atoms of anode dissolve into solution and move towards cathode. Electroplating system is usually formed by four parts: anode, cathode, electrolyte solution and electrical power source.

Under the effect of electrical current, anode material dissolves into electrolyte solution, becoming cations and move towards cathode. Hence, anode is supposed to be pure mental tin (over 99.9%) and cathode should be copper substrate. One surface of copper substrate must be smooth enough for deposition of dissolved tin atoms. The unwanted

surfaces are covered by block layer to prevent them from electroplating. Electrolyte solution used for electroplating in this experiment was made of dilute sulphuric acid and stannous sulphate (H₂SO₄/ SnSO₄). The schematic diagram of this electroplating system is shown in **Fig. 4. 2**.

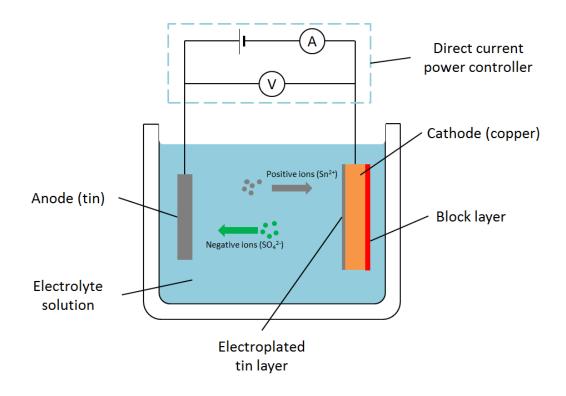


Fig. 4. 2. Schematic diagram of the electroplating system

Since the structure of electroplated metals usually contains some small voids and grooves, some additional ingredients called "*brightener*" in electrolyte were required to obtain a bright electroplating surface. Here, a product of additive RX-770/RX-780 from Zhejiang Haining Rongxin Electronics Co., Ltd was employed. RX-770/RX-780 was a newly environmental friendly acid based tin plating brightener additive full bright acid tin additives. RX-770 played a role of opener while RX-780 was supposed to be a brightener. These two additives were used together with different doses in electrolyte solution. The final ingredients of electrolyte solution are listed in **Table 4. 1**. In this experiment, 500 mL of electrolyte solution was enough for the specimens and the fixture clamping.

Chemical compositions	Unite	Range	Optimal
SnSO ₄	g/L	20-40	25
H ₂ SO ₄	g/L	130-200	170
RX-770	mL/L	4-8	6
RX-780	mL/L	0.5-2	1

Table 4.1. The ingredients of electrolyte solution of electroplating

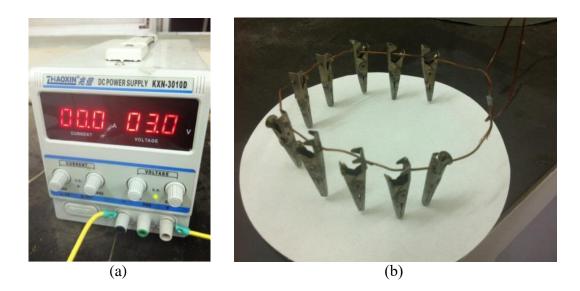


Fig. 4. 3. (a) The Power source of electroplating system; (b) The fixture clamping for copper substrates

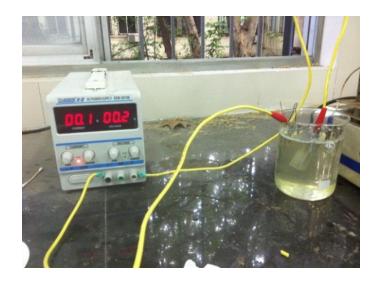
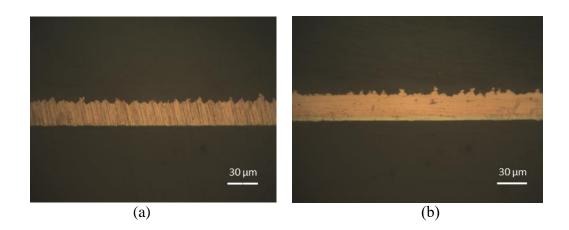


Fig. 4. 4. The electroplating system used in the experiment

The power source of electroplating system adopted a DC (direct current) power supply KXN-3010D from Zhaoxin Co., Ltd, as in **Fig. 4. 3** (a). The power supply is supposed to provide steady value of electrical current. Hence, it was supposed to be working under constant current condition. Copper substrates were used as cathode in single electroplating process. In order to fix all the substrates, a fixture clamping made by a copper wire and alligator clips was prepared to hold the copper substrates in electrolyte solution, as in **Fig. 4. 3** (b). The whole electroplating system is presented in **Fig. 4. 4**.

To obtain the relationship of Sn layer thickness and electroplating time, the cross sections of the samples with different durations were observed by optical microscope, as in **Fig. 4. 5**. The relationship of the layer thickness and electroplating durations are presented in **Fig. 4. 6**.



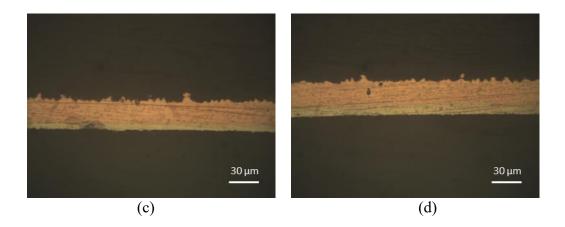


Fig. 4. 5. Cross sections of the samples after: (a) 5 min, (b) 10 min, (c) 15 min and (d) 20 min electroplating durations

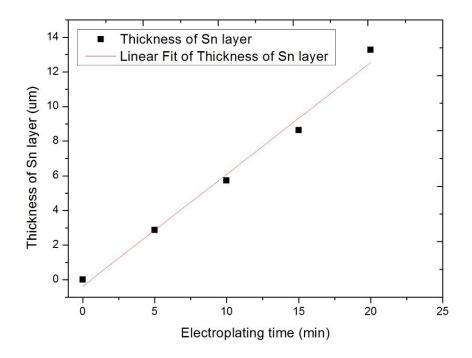


Fig. 4. 6. Relationship of the Sn layer thickness and the electroplating durations

During electroplating, if the area of anode and cathode vary in process, the electroplating rate changes and this relationship is not applicable. Hence, the cathode including both specimens and fixture clamping was submerged into electrolyte solution. According to **Fig. 4. 6**, thickness of the Sn layer was proportional to its duration of electroplating. And the electroplating time of a thickness with 20 μ m of Sn layer was 29.8 min, based on the results of liner fit of the data. The method mentioned above was used only to estimate and determine time intervals when thickness of Sn layer reaches 10 μ m. As the increase rate was very low, this method was proved to be acceptable.

Reflow process

Reflow process in this section actually refers to two processes: metallurgy welding and time aging. To weld a Sn layer to a copper substrate, the specimens underwent an increase of temperature to over 270 °C, as the melting temperature of Sn is 232 °C. Then the temperature was kept at 270 °C for a while to allow Sn and Cu reacted with each other, forming intermetallic compound layer (IMC). After that, the temperature dropped to 60 °C gradually and was kept at this level for 250 s. During this period, Cu

atoms from copper substrates diffused to the interface between IMC and Sn layer. Then these Cu atoms reacted with Sn atoms, causing an increase of the IMC layer.



Fig. 4. 7. The reflow oven

Table 4. 2. Temperatures and durations set by the reflow oven

No.	Temp/°C	time/s	No.	Temp/°C	time/s
1	80	20	15	195	24
2	100	20	16	200	20
3	120	24	17	210	20
4	130	20	18	215	24
5	140	20	19	225	20
6	150	20	20	240	20
7	155	20	21	245	24
8	158	150	22	250	20
9	163	24	23	260	20
10	170	20	24	265	24
11	175	20	25	270	15
12	180	24	26	265	24
13	185	20	27	160	40
14	190	20	28	60	250

A reflow oven providing heating source and temperature controlling in this process is presented in **Fig. 4. 7.** The controlling temperature rose to 270 °C from room temperature and then decreased to 60 °C. It has been reported that cooling rate in Sn

solidification mainly influenced morphology of micro-structure [7]. Therefore, decreasing rates of temperature in the oven should be controlled precisely. Temperature change could be programmed by the reflow oven. The reflow temperature curve data set by oven are listed in **Table 4. 2**.

However, the real temperature in the reflow oven cannot follow as the program settings strictly. Furthermore, the reflow oven employed in this experiment could not control the cooling process as there were only heaters inside. Therefore, in order to sense the actual temperature, a thermo-couple was used to test the internal temperature of the reflow oven. The sensed temperature with time is presented in **Fig. 4. 8**.

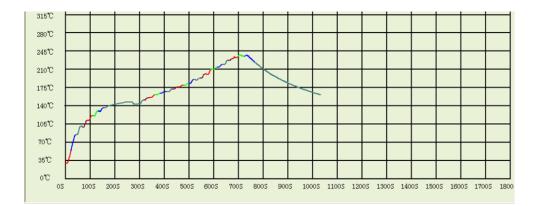


Fig. 4. 8. Actual temperature sensed by thermo-couple in reflow

After reflow process, the sample was grinded and polished to expose its cross-section. Then it was corroded slightly by 96% $C_2H_5OH + 4\%$ HCl (volume) solutions for the convenience of observation.

4.2.2 Results and discussion

In micro solder bumps, both of dimensions in height and diameter directions are supposed to be around $20\mu m$. However, as the morphology of IMC layer presents characteristics of high randomness, microstructure in one single micro-solder bump hardly represents characteristics of IMC layer in 20 μm thickness of solder joint. Hence, a type of sample with larger dimensions in diameter direction was adopted in this chapter to investigate morphology in micro-solder joints. Fig. 4. 9 presents the

observation of cross section in after-reflow specimen by SEM.

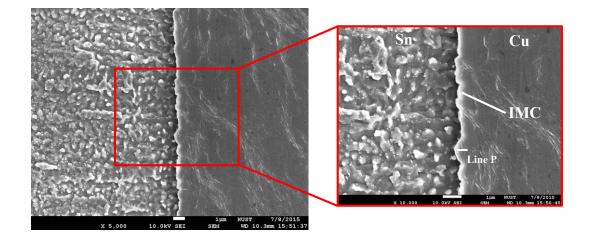


Fig. 4. 9. Cross section of as-reflowed specimen by FEM

In **Fig. 4.9**, the solder part in Sn/Cu structure shows the uneven morphology as it has been corroded by solution while the Cu part presents a relatively flat surface. Sn dendrites caused by gradually cooling process could be observed in solder part of the specimen. A scalloped IMC layer with around $2-\mu m$ thickness was found on the interface of Sn and Cu. In order to figure out the composition of the IMC layers, Energy Dispersive Spectrometer (EDS) was used to detect the materials located in four points on Line P, as presented in **Fig. 4.9**. The four points were named as Point A to D from the right end of Line P to the left. The results of EDS at these four points are presented in **Fig. 4.10**.

Table 4. 3. lists the percentage in atom numbers of elements at Point A, B, C and D. Due to the inter-diffusion of Cu and Sn atoms during reflow-process, the concentration of Cu decreased from Point A to D, while the concentration of Sn atoms increased from A to D. The ratio of percentage in atom numbers at these four points varied from 1.02 to 1.34. These values indicated that the main component of formed IMC layer was Cu₆Sn₅. Some papers have reported that two types of intermetallic compound, Cu₆Sn₅ and Cu₃Sn, were found in the IMC layers of Sn-Cu structure and the IMC layer of Cu₃Sn was found at the interface of Cu₆Sn₅ IMC layer and Sn [**9**]. However, this type of IMC layer was usually formed after long-time aging and it was not found in this experiment. Therefore, the layer formed by Cu₃Sn IMC was neglected.

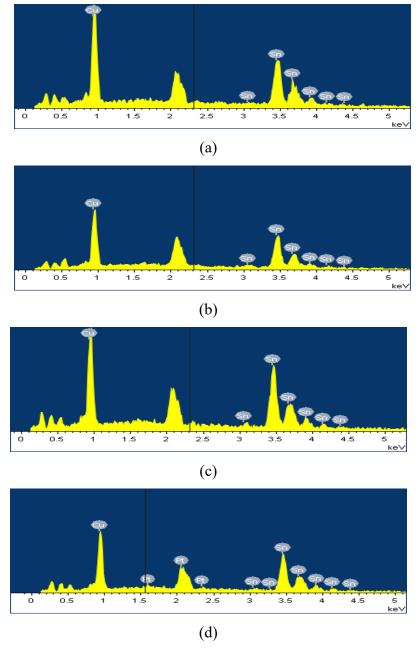


Fig. 4. 10. EDS results of Line P at: (a) Point A, (b) Point B, (c) Point C and (d) Point D

Table 4. 3. Element components in IMC

	Point A	Point B	Point C	Point D		
Element		% in mass				
Cu	57.36	55.08	51.92	45.89		
Sn	42.64	44.92	48.08	44.66		
Ratio	1.34	1.23	1.08	1.02		

To investigate the characteristics of the IMC layer, "UTHSCSA Image Tool" software was used for image processing. According to calculation, the average value of thickness of the IMC layer is around 2.0 µm. Moreover, to get statistical data of IMC layer roughness and build the geometrical structure in FE software, 70 pairs of coordinates of points on the outline of the IMC layer surface were obtained by using UTHSCSA Image Tool. These data were transferred into ABAQUS 6.14 software to generate a two-dimensional model of micro-solder joint (as illustrated in **Fig. 4. 11**). This model could be used in following simulations of stress.



Fig. 4. 11. Two-dimensional FE-model of a micro solder bump in ABAQUS 6.14

4.3 Shape prediction of solder bumps

Some previous studies have proved that some design parameters of solder joints in BGA, i.e., pad diameter (*d*), standoff height (*h*), diameter of solder balls (ϕ) and contact angle (θ), have significant effects of mechanical behaviour of solder joints. The geometry of solder joints can be determined easily by a geometry-based truncated sphere method, which assumes that the solder ball after reflow is a part of sphere without considering the effect of gravity and surface energy. However, the geometry of solder joints determined by this method shows some difference especially for contact angle from real situation. Therefore, a method based on energy minimization was adopted to determine the geometry of solder balls. During reflow process, total potential energy in a liquid solder ball could be pressed as sum of surface potential energy and gravity potential energy,

$$E_{totall} = E_s + E_g = \iiint_V \rho g z dV + \iint_S \sigma dA \qquad (4-1)$$

where ρ is the density of liquid solder, which is 7.04 g/cm³; g is the gravitational acceleration constant (i.e., $g = 9.80 \text{ m/s}^2$); z is the displacement of the potential energy in the z axis direction, i.e., the standoff height direction in solder; V is the integration volume of the solder joint; σ is the surface tension, which is supposed to be 500.0 mN/m by the pendant drop method using a surface tension measurement system (OCA20, Dataphysics, Germany) at 260°C in a nitrogen ambient [8]; A is the surface area of the liquid solder.

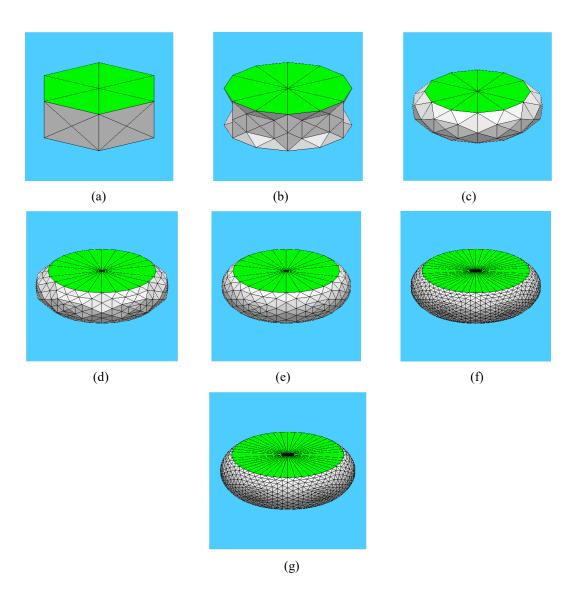


Fig. 4. 12. The evolution of a BGA solder ball using energy-based method by Surface Evolver: (a) initial state; (b) refine the element first time; (c) minimize the potential energy first time; (d) refine the element second time; (e) minimize the potential energy second time; (f) refine the element third time; (g) minimize the potential energy third time.

Based on this equation, shape of liquid solder ball during reflow process could be determined. Therefore, an energy-based program, Surface Evolver, were used to determine the geometry of liquid solder balls. **Fig. 4. 12** shows the evolve procedure of solder geometry. Firstly, the volume of liquid solder ball was input into program as a constant. Then the program generated a simple polyhedron with limited number of joints and faces. After that all elements located on the surface of solder ball were refined; every edge of each element were divided into two parts with the same length. Then the energy of this refined polyhedron was minimized to achieve a stable status. After several times of refinement and energy minimization, geometry of solder ball tends to be a minimum value of energy, which was the stable status of it.

An assumption was made that the solid solder ball kept the same geometry as its liquid status. Here, three standoff heights (20um, 100um and 200um) were adopted in this simulation to compare the shrink size effect of solder balls. **Fig. 4. 13** shows the geometry of joints with different standoff height predicted by Surface Evolver.

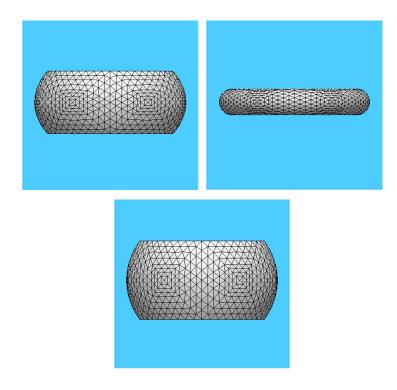


Fig. 4. 13. Geometry of joints with different standoff height predicted by Surface Evolver

According to the results by Surface Evolver, the potential energy of gravity took 0.045%, 0.125% and 0.254% of the total value for the bumps with 20um, 100um and 200um, respectively. Therefore, the effect of gravity on the shape of solder bump could be neglected and its external surface could be treated as a part of sphere. The profiles of solder balls generated by Surface Evolver will be used in FE-models for the following simulation. The program in Surface Evolver for the prediction of the shape of a solder bump can be found in Appendix.

4.4 Summary and conclusions

This chapter introduced the preparation of Sn/Cu structure with thickness of Sn layer of 10 μ m. Electroplating was employed to control the thickness of Sn layer precisely. Micro-structures of Sn/Cu sample were observed and the formed IMC layer between Sn and Cu is validated to be IMC-Cu₆Sn₅. A 2-D model of IMC layer based on observed results was developed for the simulation in later chapters. An energy-based method was used to determine the shape of solder bumps in BGA.A program software Surface Evolver was employed to predict different combination of copper pad diameter and standoff height. The IMC morphology and the shape of solder bump developed by experimental and numerical methods could be used as simulation geometry in followed chapters.

An as-reflowed Sn/Cu structure with the 10- μ m-thickness of Sn electroplating layer was prepared and observed. Based on the observation, the component of IMC in the sample is Cu₆Sn₅ and its average thickness is around 2 μ m. The main feature of the morphology of IMC layer was dealt with statistically and transferred into FE-model. Moreover, the external shape of a solder bump with certain combination of paddiameter and stand-off-height was predicted by an energy-based programming method. The results proved that the effect of gravity on the external shape could be neglected. The surface of a solder bump is part of a sphere.

Reference

- [1] Liu X. S., Lu G. Q., "Effects of solder joint shape and height on thermal fatigue lifetime", *IEEE Transactions on Advanced Packaging*, 2003, 26 (2), pp. 455-465.
- [2] Khor C. Y., Abdullah M. A., Leong W. C. "Fluid/ structure interaction anlysis of the effects of solder bump shapes and input/output counts on moulded packaging" *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2012, 2 (4), pp. 604-616.
- [3] J. Gong, C. Liu, et al., "Modelling of Ag₃Sn coarsening and its effect on creep of Sn–Ag eutectics", *Electronics Components and Technology Conference*, 2007, pp. 677-693.
- [4] Chen W. M., McCloskey P., O'Mathuna S. C. "Isothermal aging effects on the microstructure and solder bump shear strength of eutectic Sn37Pb and Sn3.5Ag solders", *Microelectronics Reliability*, vol. 46 (2006), pp. 896–904.
- [5] Frear D.R., Jang J.W., Lin J.K. and Zhang C. "Pb-Free Solders for Flip-Chip Interconnects", *JOM*, vol. 53 (2001), Issue 6, pp 28-33.
- [6] Nah J. W., Kim J. H., et al., "Electromigration in flip chip solder bump of 97Pb-3Sn/37Pb–63Sn combination structure", *Acta Materialia*, vol. 52 (2004), pp. 129-136
- [7] Gong J., Liu C., Conway P. P., Silberschmidt V. V., "Formation of Sn dendrites and SnAg eutectics in a SnAgCu solder" Scripta Materialia, vol. (2009), pp. 682-685.
- [8] Qin H.B., Li W.Y., Zhou M.B., Zhang X.P. "Low cycle fatigue performance of ball grid array structure Cu/Sn-3.0Ag-0.5Cu/Cu solder joints", *Microelectronics Reliability*, vol. 54 (2014), pp. 2911-2921
- [9] Laurila T., Vuorinen V., Kivilahti J. K., "Interfacial reactions between lead-free solders and common base materials", *Material Science Engineer*. R. Vol. 49 (2005), pp. 1-60

Chapter 5. Mechanical behaviours of package and single solder bump of BGA under thermal cycling

5.1 Introduction

Solder joints serve as electrical connections and mechanical supports in electronic packages. So, failure of solder joints could cause electronic devices to malfunction. Hence, reliability of solder bumps of micro-scale considering effects of their micro-structure is the main concern in this research.

In flip-chip packaging, chips and substrates are usually made of different materials, which means they have different coefficients of thermal expansion (CTE). Generally, the difference of CTE between chips and substrates are large, resulting in their different expansions even under uniform thermal loading conditions. Since the solder bumps constrain expansion of a chip and a substrate, warpage at a package level and shear deformation at a bump level occur. As thermal loadings in electronic package are usually cyclic, deformations caused by these loadings can lead to inversed stress state in the package. Hence, fatigue analysis becomes an important issue in assessment of package reliability.

For components under thermal fatigue, voids and cracks in structure decrease their durability significantly. Many aspects in manufacturing and service processes of solder joints lead to microstructural changes in therm. In manufacturing, solder-joint design parameters, i.e., a stand-off height (SOH), a pad diameter and a surface shape, affect their mechanical reliability [1, 2]. Moreover, IMC formation caused by interactions between Sn and Cu atoms during a reflow process changes stress distributions significantly. Mechanical properties and microstructure of IMC varies in solder parts. Hence, IMC is the key to solder-joint reliability under thermal cycling. In service, an increase in thickness and shape changes of IMC caused by aging can affect mechanical

reliability of solder joints. With decreasing dimensions of solders, a volume fraction of IMC in joints increases rapidly. When a joint height decreases to around tens microns, intermetallic compounds even take most volume proportion in solder balls.

In this chapter, package warpage and stress distributions under the effect of IMCs and their growth with FEA were estimated and investigated. Two-D and three-D FE models built by ABAQUS 6.14 were compared and discussed to choose a suitable FE model for the simulation of this research. Different SOHs of solder bumps were investigated for the whole package undergoing an external thermal cycling. Surface shapes of solder bumps and IMCs in the models were based on calculation and microstructure of real solder joints (Chapter 4) respectively. A stress state of the solder ball under the most dangerous conditions was also analysed. A life in service of the package under thermal loading based was estimated based on the level of accumulated equivalent inelastic strains at the end of chapter.

5.2 Analysis procedure

5.2.1 Model description and loading conditions

As discussed in Chapter 3, a 3-D model of a 1/8th of the package is adequate for finite element analysis (FEA) to assess its mechanical reliability. However, in the simulations of this research, high non-linear mechanical behaviour should be taken into consideration due to its increasing computation costs. In the following chapters, a thermal-mechanical analysis needs to be repeated after each removal of elements in the FE model based on the algorithm. Therefore, a 2-D plane-strain model is a better choice for its simplicity and relatively reliable prediction of the results. Considering the boundary condition limits in ABAQUS, a 3-D model of a quarter of the package was adopted in simulation. Its results are discussed and compared with a 2-D plane-strain model in the following section of this chapter.

The whole package-model to be analysed was a typical BGA structure including three

components: a reading chip, a substrate and a 10×10 solder bump array. A schematic top-view of the BGA structure are presented in **Fig. 5. 1**.

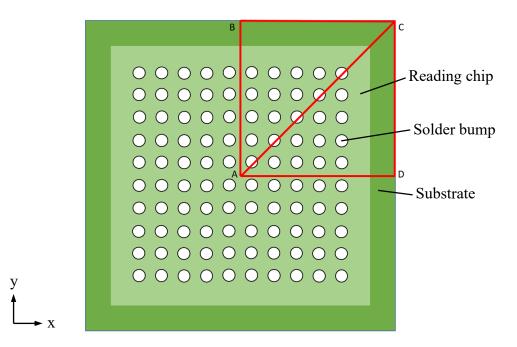
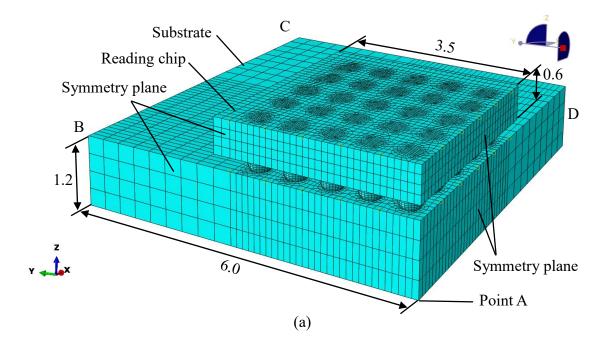


Fig. 5. 1. A schematic top-view of the BGA and the positions of FE-models

Fig. 5. 1 also illustrates the positions of the 3-D and 2-D models. The part of the model in the red coloured rectangle A-B-C-D is the 3-D model of a quarter. Point A is the centre point of the model. The 2-D plane-strain model is the plane in A-C.



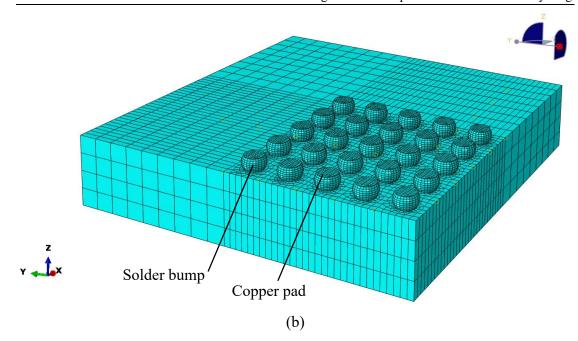
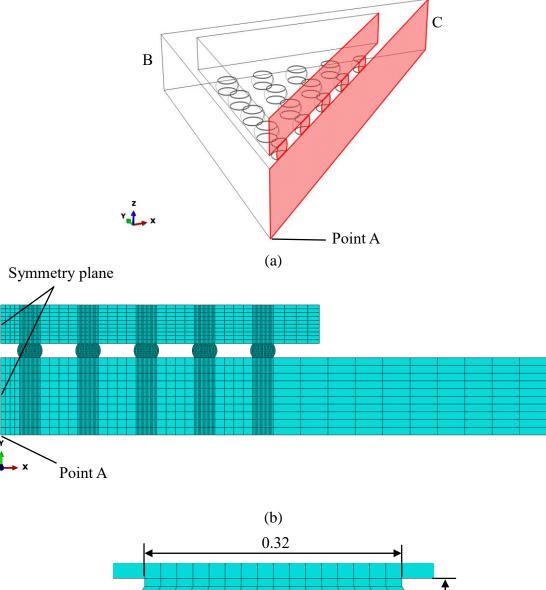


Fig. 5. 2. Geometry and boundary conditions of the package for FE analysis: (a) quarter of the structure; (b) reading chip is removed from (a) (Unit: mm)

The geometry and boundary conditions of the 3-D models with meshing are presented in **Fig. 5. 2**. The FE mesh given in **Fig. 5. 2** was generated in ABAQUS using the hexahedron element type (C3D8R, an 8-node linear brick, reduced integration, hourglass control) and it contained 43816 elements in total. Considering the package's symmetry, boundary conditions of all the cross section planes located in A-B and A-D were set as symmetric planes. The Point A (marked in **Fig. 5. 2**) located in bottom centre of the substrate was set as a fixed point. The bonding types of bump/chip and bump/substrate were set as ideal bonding, which means there was no relative horizontal or vertical displacement between contacting faces.

For the size of the model, the chip was $7 \times 7 \times 0.6$ mm and the substrate was $12 \times 12 \times 1.2$ mm. The SOH of solder bump array was 200 μ m and the pitch was 640 μ m. The copper pad diameter was 320 μ m. The shape of single solder bump was defined by the calculation results of Chapter 4.

For the 2-D model, its location in package is presented in The geometry and boundary conditions of the 2-D models with meshing are presented in **Fig. 5. 3**. The FE mesh given in **Fig. 5. 3** was generated in ABAQUS using the plain-strain element type (CPE4R, a 4-node bilinear plane strain quadrilateral, reduced integration, hourglass



control) and it contained 3500 elements in total.

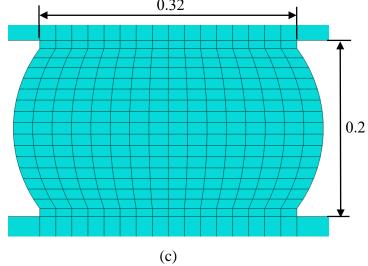


Fig. 5. 3. Location, geometry and boundary conditions of the package for FE analysis:(a) location of 2-D model in the package; (b) 2-D model with mesh; (c) enlarged view of a single solder bump (Unit: mm)

The Point A (marked in **Fig. 5. 3**) was also set as a fixed point. The central axis crossing Point A of the package was set as symmetric plane in 2-D model. The bonding types of bump/chip and bump/substrate were also the same as 3-D model.

Generally, as mentioned in introduction, a IMC layer was formed between solder bump and copper pad. However, the IMC layer usually presents elastic behaviour during thermal cycling and this simulation mainly focus the inelastic deformation of solder. Therefore, for the convenience of model building and discussion, the IMC layer was neglected in the comparison of 2-D and 3-D model. In following detailed discussion, the effect of different thicknesses of IMC layer is estimated by simulation in details.

In real application, an electrically-insulating adhesive (as presented in **Fig. 5. 4**) is underfilled between chip and substrate to provide a stronger mechanical connection, a heat bridge, and to ensure the solder joints are not stressed due to differential CTEs.

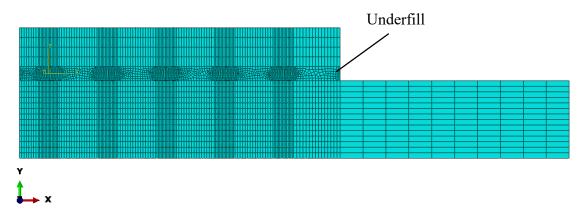
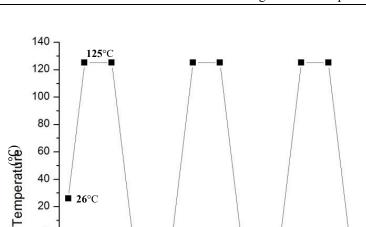


Fig. 5. 4. Underfill with mesh in the package for FE analysis

The whole model was exposed to a thermal-cycling heating condition. Some previous studies reported that the temperature gradient in the flip chip packages was so small that could be neglected [**3**]. Hence, the temperature of all parts in models was set to be uniform when temperature fluctuates. Thermal load started from room temperature $(26 \text{ }^{\circ}\text{C})$, reached to the highest point of $125 \text{ }^{\circ}\text{C}$ in 180 s. Then it was kept at this level for 300 s and then decreased to the lowest of -40 $^{\circ}\text{C}$. At the lowest temperature, the hold time was also 300 s and then temperature went back to room temperature. One single cycle lasted for 1200 s. The whole modelled process lasted 3600 s and covered 3 cycles (**Fig. 5. 5**. Thermal cyclic load in simulations: 3600 s corresponding to 3 cycles).



■ 26°C

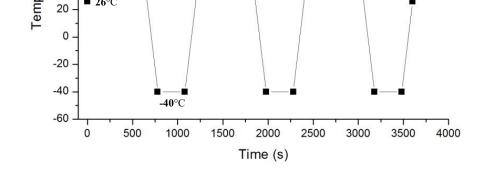


Fig. 5. 5. Thermal cyclic load in simulations: 3600 s corresponding to 3 cycles

To investigate a size effect on mechanical behaviour of the package, two sizes of solder bumps with a SOH of 200 µm and 20 µm were analysed. As discussed in Chapter 4, certain combinations of pad diameters and SOHs were chosen to avoid the effects of contact angle.

The size effect researched in this chapter included two factors. The first one is a morphology transition of the IMC layer. For the model with a 200 µm SOH of solder bumps, morphology of the IMC layer surface was neglected and treated as a flat, since its thickness was small compared with a bump size. However, the effect of an IMC thickness increase on mechanical reliability of a package have been reported in some previous works [4]. Therefore, the IMC growth effect on mechanical behaviour was evaluated in this chapter. Geometry of a solder bump geometry with 200-µm-SOH with different IMC thickness is presented in Fig. 5. 6.

Coloured areas in Fig. 5. 6 represent the IMC layers formed by Cu₆Sn₅; the thickness of these IMC layers was 3 μ m. In simulations, two level of thickness of IMC – 1.5 μ m and 3 µm were analysed as listed in [5]. For the model with 1.5 µm of IMC, the material of the red-coloured areas was set as Cu₆Sn₅ while the rest of bump was solder.

In the model with 3 μ m of IMC, the material of both red and orange coloured areas was set as Cu₆Sn₅.

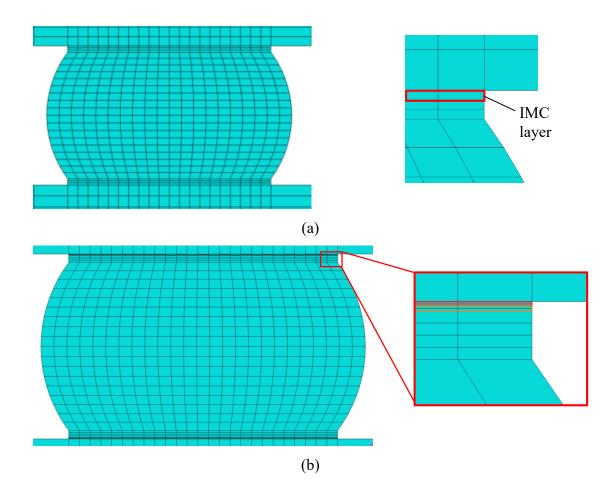


Fig. 5. 6. Geometry of solder bump in 200 μm standoff height with IMC layer: (a) the position of IMC layer in a meshed solder bump; (b) different thickness of IMC layer

For a solder bump with the 20 μ m SOH, a IMC layer takes a large part of the volume in a bump, which means that neither its thickness nor morphology can be neglected. The effects of both thickness and morphology should be evaluated in simulations. According to Chapter 4, the initial average IMC thickness of after-reflow solder bumps was 2 μ m. In this part of simulations, a model with the similar structure shown in **Fig. 5.** 2 (a) was built and analysed. The size of the model with 20 μ m SOH solder bump was 1/10th of the model in **Fig. 5.** 2. Geometric features of a single bump with different thicknesses and morphologies of IMC layers are displayed in **Fig. 5.** 7.

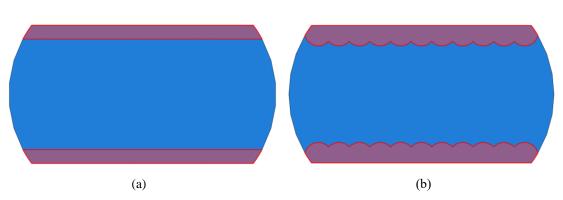


Fig. 5. 7. Geometry of solder bumps with 20 μm SOH with: (a) flatten IMC layer;(b) scallop-shaped IMC layer.

To figure out the effects of morphology, the scallop shape of IMCs was introduced into the model as shown in **Fig. 5. 7**. However, the uneven structure resulted in complexity of the mesh, increasing the calculation time and cost. Hence, only the solder bump located on the edge of package had the scallop-shaped IMC layer; the rest four bumps were supposed to have simpler morphology of IMCs. This simplicity could reduce the cost of calculations without significant changes to a stress distribution in package.

The second factor of size effect is anisotropy of single grain crystal of materials. As its size is close to a single Sn grain, a micro solder bump is usually formed by one or a few tin grains. For IMC layer, as Cu_6Sn_5 is the main part, its material behaviour is still regarded as isotropic elastic based on **Table 2. 1**. Considering the Sn grain is body-centred tetragonal and its properties along c-axis are different from the other two directions (**Fig. 5. 8**), two typical directions of single Sn grain were simulated and compared in this section.

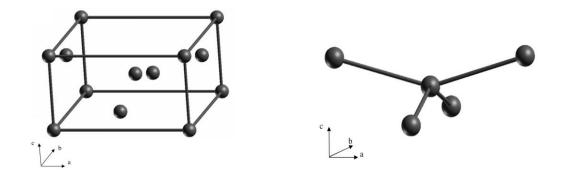


Fig. 5. 8. Crystal structure of Sn grain [11]

For the two typical Sn grain directions, the c-axis was set along X, Y-coordinate respectively. The two situations were estimated and compared based on FE analysis results. Considering the random directions of Sn grain in physical situation, the direction of the Sn grain in each solder bump were different in a package. Therefore, the two typical grain directions were only applied on the outmost solder bump while the rest bumps were still set as isotropic materials.

5.2.2 Material properties

The simulated model underwent a fully coupled thermal-displacement process. Basic material properties of the modelled materials including an elastic modulus, the Poisson's ratio and CTE should be taken into consideration. The simulated model contained 5 materials: silicon (chip), Cu₆Sn₅ (IMC), BT (substrate), SAC305 (solder) and compound polymer (underfill).

The chip and substrate were supposed as a uniform material made by silicon and BT respectively. Melting point of silicon and BT are relative high compared with service temperature. Therefore, their properties included only elastic behaviour and thermal expansion. These two properties of silicon vary with temperature. Hence, temperature-dependent data were used to define silicon's material properties, as shown in **Table 5**. 1 and 5. 2 [6].

	Elastic	2	Thermal Expansion
Temperature/°C	Elastic Poisson's Modulus/MPa Ratio		CTE
-40	192100		1.5e-6
25	191000	0 279	2.6e-6
50	190600	0.278	2.8e-6
125	190000		3.1e-6

Table 5. 1. Material properties of silicon [6]

Elasti	c	Thermal Expansion
Elastic Modulus/MPa	Poisson's Ratio	CTE
26000	0.39	1.5e-5

 Table 5. 2. Material properties of BT [6]

The solder bump was formed by two constituents: a tin alloy (SAC305) and IMCs. The melting temperature of the tin alloy is relatively low compared to the service temperature according to Chapter 3. Hence, it demonstrates creep behaviour during thermal cycling loadings. This simulation adopted hyperbolic-sine model to describe creep behaviour [7],

$$\dot{\epsilon} = A \left[\sinh \left(\alpha \frac{\tau}{G} \right) \right]^n \exp \left(- \frac{Q}{RT} \right) , \qquad (5-1)$$

where A is a constant, α is the stress level constant, n is stress exponent. Besides, its elastic and thermal expansion data are needed for elastic deformation, as shown in **Table 5.3**.

Table 5. 3. Material properties of tin alloy (Sn-3.5Ag) [5]

Creep (hyperbolic-sine)							
Power Law Multiplier (A)	Hyperb Law Multiplier (α)	Eq Stress Order (n)	Activation Energy (Q)	Universal Gas Constant (R)			
7.01	0.081	5.5	48364.2	8.31			
Elastic			Thermal Expansion				
Temperature /°C	Elastic Modulus/MP a	Poisson's Ratio	CTE				
-40	57392						
25	47662	0.4	2.25e-5				
50	43919	0.4					
125	32692						

Another key property of solder is its plastic properties. The plastic behaviour data for SAC305 adopted in this simulation were taken from [5], as in Fig. 5.9

For intermetallic compounds, their properties are simpler owing to their high melting temperature. Material properties of IMCs were just set as elastic and thermal expansion. Thinking of IMC's steady properties in creep process, its elastic data were set as temperature-independent, as listed in **Table 5. 4**.

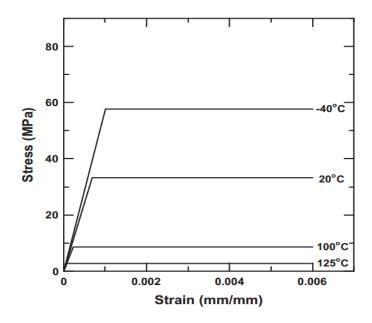


Fig. 5. 9. Temperature-dependent stress–strain curves of elastic-plastic properties for 96.5Sn–3.5Ag solder materials [5].

Elastic			Thermal Expansion
Elastic Modulus/MPa	Poisson's Ratio	Temperature/°C	CTE
		-40	1.63e-5
85600	0.31	25	1.76e-5
	0.31	50	1.81e-5
		125	1.93e-5

For the Sn single grain, its crystal structure can be represented as having tetragonal symmetry. These spatial constraints require a matrix of six independent constants to describe the elastic properties, as presented in Equation 5-2. The stress-strain coordinate system X, Y and Z was chosen here to be coincident with the crystallographic unit cell axis a, b and c (see Fig. 5. 8), respectively. A local datum coordinate was used to assign grain directions. The constants in Equation 5-2 as a function of temperature from [12] are listed in Table 5. 5.

$$C_{ij} = \begin{pmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0\\ C_{12} & C_{11} & C_{13} & 0 & 0 & 0\\ C_{13} & C_{13} & C_{33} & 0 & 0 & 0\\ 0 & 0 & 0 & C_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & C_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & C_{66} \end{pmatrix}$$
(5 - 2)

 Table 5. 5 The elastic stiffness constants for tin as a function of temperature

 (Units: 10³ MPa) [12]

Temp (K)	C ₁₁	<i>C</i> ₁₂	C ₁₃	C ₃₃	C ₄₄	C ₆₆
77	81.52	57.90	36.42	100.40	26.20	27.81
300	72.30	59.40	35.78	88.40	22.03	24.00
301	72.0	58.5	37.4	88.0	21.9	24.0
418	65.8	58.6	37.7	80.8	19.1	21.4

The plastic and creep deformation of Sn crystal grain are highly dependent on the temperature and stress. Their mechanism resulted by different slip system are complex, therefore, experimental data from some previous study varied. In [13], Yomogita carried out stress relaxation test of Sn single grain in $(1 \ \overline{1} \ 0)$. The results are close to bulk specimens. In 1979, S. N. G. Chu and J. C. M. Li researched the compression creep deformation of Sn crystal structure in $[0 \ 0 \ 1]$, $[1 \ 0 \ 0]$ and $[1 \ 1 \ 0]$. In high temperature, creep behaviours in these three directions were closed and their activation energy are the same. Based on these facts, although some other studies proved that Sn single grain and bulks presented differences in inelastic deformation, the plastic and creep behaviours of Sn grain were set the same as the large solder bump in order to

reduce the complexity of simulation.

Another component in the package is underfill. It is a polymer based compound material, and is supposed to have a deformation behaviour which is dependent on temperature and time. In this chapter, a linear-viscoelastic model was used to describe mechanical behaviours of underfill by consideration of time dependent deformation. It is expressed by a series of generalized Maxwell models, as Equation 5 - 3:

$$E(t) = \sum_{i=1}^{3} E_i e^{-t/\tau_i} + E_{\infty} , \qquad (5-3)$$

where E_{∞} is the tensile modulus when the time approaches infinite. The parameters E_i and τ_i are the tensile modulus and the retardation time of the Maxwell model, which can be expressed as

$$E_i = K_i (E_0 - E_\infty)$$
 . (5-4)

The parameters in Equation 5-3 and 5-4 are listed in Table 5. 6[14].

 Table 5. 6 Parameters of the viscoelastic underfill models [14]

E_0 (MPa)	E_{∞} (MPa)	<i>K</i> ₁	$ au_1$ (s)	<i>K</i> ₂	$ au_2$ (s)	<i>K</i> ₃	$ au_3$ (s)
5630	1300	0.264	0.198	0.2	451	0.536	30435

In ABAQUS 6.14, elastic modulus, Poisson's ratio and CTE are also need to be defined. According to [5], these parameters are set as 5630 MPa, 0.3 and 20 ppm/K, respectively.

5.2.3 Justification of 2-D/3-D FE models

Table 5. 7 summarizes the comparison of model information for 2-D plain strain and3-D quarter FE models. A underfill was not included in the 2-D and 3-D model here.All the data in this table are from analysis recordings of ABAQUS 6.14.

Comparing with the 2-D model, the 3-D quarter model showed an increase of 30 times in computing time and 18 times in space requirement, which means 3-D quarter model has much worse computing efficiency. In a previous study [8], a comparison of 2-D and 3-D model also showed significant increase times of 3-D model. Based on the analysis methods in following chapters, this thermal-mechanical analysis need to be repeated. The repeat times were related to the numbers of failure elements during service, which are depended on mesh density. Therefore, the adoption of 3-D model increases calculation cost dramatically and makes the following simulations unrealistic. If the calculating accuracy of 2-D plain strain model produces a reasonable agreement with 3-D quarter model, it is a better choice for simulation.

	2-D plain strain	3-D quarter			
Computing time	15 min	7 hrs 11 min			
Memory size	610 MB	10.8 GB			
Element number	3500	43816			
Running hardware	Intel Core i7 2.20G Hz, 8GB RAM				
Solution scheme	ABAQUS Standard/Visco step				
(c)					

Table 5. 7. Computing time and memory size of 2-D and 3-D FE models

Fig. 5. 10 presents stress distributions in 3-D quarter model and 2-D plain strain model at the end of thermal cycling (t=3600 s). The cross section in A-C section of 3-D quarter model is illustrated in (a) of **Fig. 5. 10**. Mises stress distribution at the end of thermal cycling in: (a) cross section of 3-D quarter model; (b) chip array with chip removal and (c) 2-D plain strain model. The stress distribution of solder bumps in (a) and (c) shows some similarities according to **Fig. 5. 10**. Mises stress distribution at the end of thermal cycling in: (a) cross section of 3-D quarter model; (b) chip array with chip removal and (c) 2-D plain strain model, especially in solder bumps. Their highest residual stresses are both located at the peripheral of the outmost solder bump (illustrated by yellow arrows). In addition, the values of highest stress are close to each other. For a further estimation of stress in 2-D and 3-D model, the stress histories of the peripheral part in the outmost solder bump during thermal cycling are plotted in **Fig. 5. 11**. Mises stress history of the peripheral of the outmost solder bump during thermal cycling. During low-dwell-temperature periods, the stress experiences a relaxation process, in which the

2-D and 3-D present some differences. Unlike 2-D plain stress model, thickness of the solder bump in 3-D model is finite and its structure restrict deformation of the solder bump. Therefore, the 3-D model presents more resistance to high-temperature deformation. However, during the high-temperature-dwell, temperature increase and decrease periods, insignificant differences in stress were observed between 2-D plain strain model and 3-D quarter model.

In [8], a 2-D plain strain model, a 2-D plain stress model, a 3-D slice model and a 3-D 1/8th model were built and compared. The results also showed that the 3-D slice model and 2-D plain strain model had adequate consistency in analysis results of 3-D 1/8th model. The compared simulation results in [8] mainly focused on the inelastic strains, including both creep strains and plastic strains. Inelastic strain is commonly used to estimated fatigue life in many researches. Therefore, the inelastic strain of 2-D and 3-D model in each cycle were recorded and listed in Table 5.8.

Table 5. 6. The metastic strain of 2-D and 5-D model in each cycle						
Inelastic strain	1st cycle	2nd cycle	3rd cycle			
2-D plain strain	0.14193	0.13936	0.13983			
3-D quarter	0.15011	0.14110	0.13904			

Table 5. 8. The inelastic strain of 2-D and 3-D model in each cycle

According to the inelastic strains in **Table 5. 8**, the 2-D plain strain presents 5.1% less, 1.2% less and 0.6% more than 3-D quarter model in three cycles respectively. Based on the conclusions in [**5**], the accumulated inelastic strain in BGA after 3rd cycle tends to be a stable state. Hence, the difference of inelastic strain after 3rd cycle between 2-D and 3-D model keeps steady. The 2-D plain strain model shows good agreement in inelastic strain with 3-D quarter model.

In some studies of BGA simulation [8-10], a 3-D slice model was proved that it had both good efficiency and agreement with 3-D quarter/octant model. However, these 3-D slice models were taken from a strip part of the package, which did not contain the outmost solder bump. The simulation results in **Fig. 5. 10** prove that the outmost bump is the most critical part in the package. Besides, a 3-D slice model including the outmost solder bump cannot be realized due to boundary conditions. Hence, 3-D slice model is not applicable for this research.

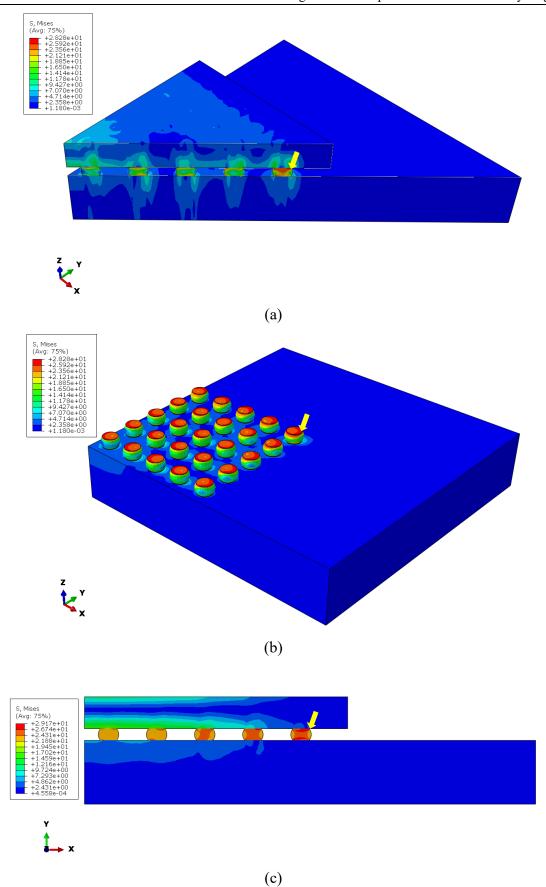


Fig. 5. 10. Mises stress distribution at the end of thermal cycling in: (a) cross section of 3-D quarter model; (b) chip array with chip removal and (c) 2-D plain strain model

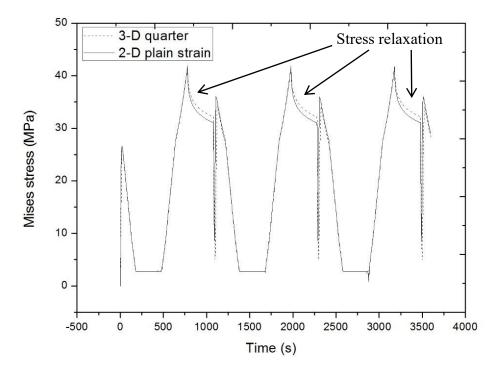


Fig. 5. 11. Mises stress history of the peripheral of the outmost solder bump during thermal cycling

In summary, comparing with a 3-D quarter model, a 2-D plain strain model of the BGA package underestimates stress during stress relaxation in solder bump resulted by its creep behaviours under high temperature. As for accumulated inelastic strains, the 2-D model presents good agreements with 3-D model, especially in steady stage period. Meanwhile, the calculation cost of the 2-D plain strain model is much less the 3-D quarter model. Considering the simulation accuracy and the computing cost of the two FE models, a 2-D plain strain model is used for the rest mechanical simulations in this research.

5.2.4 Mesh convergence analysis of 2-D model

In FE analysis, mesh quality of model is a key factor for calculation accuracy and efficiency. Theoretically, a finer mesh leads to better accuracy of analysis results. However, an increasing number of elements results in higher calculation cost. Hence, choosing an adequate mesh density for FE model is important for the research.

According to the discussion in last section, 2-D plain strain model is used. So, mesh convergence analysis is carried out on 2-D model. The solder bumps in the model experience inelastic deformation during thermal cycling and they are the key part of failure. Meanwhile, the chip and the substrate present only elastic behaviour which shows less dependence on mesh density. Based on these facts, four element densities in the solder bumps were meshed and mesh density in the chip and the substrate keep the same. The underfill was not included in this analysis.

According to **Fig. 5. 11**, the stress and inelastic deformation reaches the highest during low-temperature-dwell period. Besides, stress relaxation was also found in this time which is resulted by inelastic behaviours of Sn. Therefore, the maximum and the minimum stress of the critical location in the first thermal cycle are adopted as the evaluating indicator of mesh convergence. The accumulated inelastic strain at the end of thermal cycling is also used to analyse mesh convergence in this section.

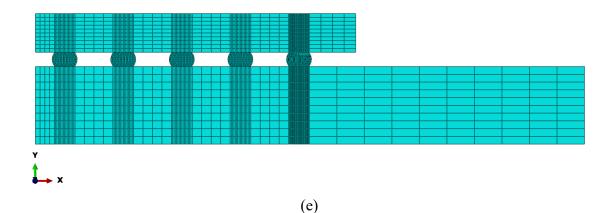


Fig. 5. 12 presents the elements in the solder bump under five different mesh densities. The chip and the substrate is not illustrated in this figure. The number of elements in each solder bump is 72, 272, 1020, 2295 in (a), (b), (c) and (d) respectively. For the situation of (e), two different mesh density was used in one FE model. The outmost solder bump was meshed as (c) while the rest four bumps were meshed as (b).

The calculation cost and evaluating indicators for different element numbers are listed in **Table 5. 9**. When the element number increases from 72 to 1020, both the maximum

stress and inelastic strain increases while the minimum stress keeps the same. This indicates that the analysis accuracy rises with the growing number of elements. However, the computing time and memory size increases significantly while the increase of accuracy is limiting. Besides, the mesh type in (e) presents a relative high analysis accuracy and adequate calculation cost. In fact, it could be regarded as a sub-model of the outmost solder bump which is the critical analysis object in the package. Accordingly, the following mechanical FE analysis use the mesh type in (e) as the element control method.

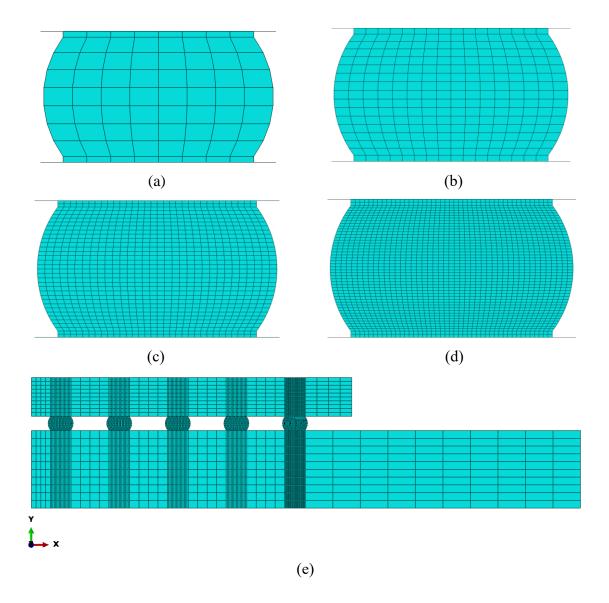


Fig. 5. 12. Meshed solder bump with different numbers of elements: (a) 72 elements, (b) 272 elements, (c) 1020 elements, (d) 2295 elements and (e) the finely meshed outmost bump

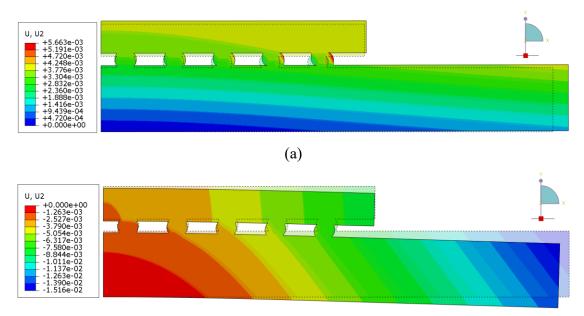
Element case	Computing time	Memory size	Max stress	Min stress	Inelastic strain
(a)	13 min	278 MB	41.03 MPa	2.644 MPa	0.3242
(b)	20 min	610 MB	42.30 MPa	2.644 MPa	0.5330
(c)	1 hr	2.5 GB	43.12 MPa	2.644 MPa	0.6026
(d)	2 hr 30 min	6.3 GB	43.34 MPa	2.644 MPa	0.6140
(e)	29 min	1.2 GB	43.02 MPa	2.644 MPa	0.5980

 Table 5. 9. The calculation cost and evaluating indicators for different element numbers

5.3 Results and discussion

5.3.1 Package warpage: effects of creep behaviour

Since the CTE of substrate is about one order larger than the chip, its expansion or shrinkage during thermal cycling is larger than the chip. Hence, a package-level warpage is expected. The FE-simulated warpage behaviour of the studied BGA package with solder bumps with 200 μ m SOH is presented in **Fig. 5. 13** and **5. 14** (no IMC layer). The model shape depicted by dash line present undeformed shapes before thermal cycling loads and the coloured contours show out-of plane deformations (displacements in Y-axis).



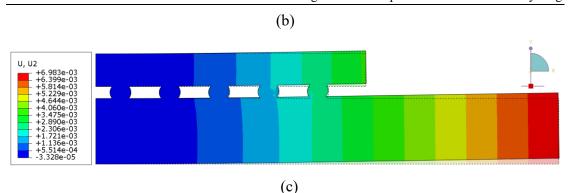
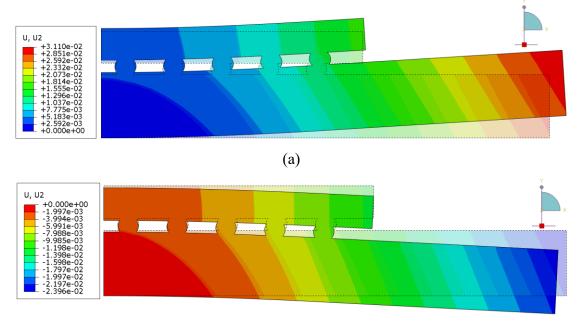


Fig. 5. 13. FE-simulated warpage deformations of studied package with solder bumps with 200 μ m standoff height (inelastic behaviour included): (a) start of high-dwell-temperature period in first cycle (t = 180 s); (b) start of low-dwell-temperature period in first cycle (t = 780 s) and (c) end of third cycle (t = 3600 s). (Deformation scale factor = 15)



(b)

Fig. 5. 14. FE-simulated warpage deformations of studied package with solder bumps with 200 μm SOH solder bumps (inelastic behaviour excluded): (a) start of highdwell-temperature period in first cycle (t = 180s); (b) start of low-dwell-temperature period in first cycle (t = 780s) (Deformation scale factor = 15)

As **Fig. 5. 13** (a) and (b), concave-up and concave-down shape of the package appeared when temperature increased and decreased, respectively. When the package reaches the highest temperature, it displacement in Y-axis is much smaller than lower temperature. Besides, the deformation of solder bump under high temperature is larger than low

temperature according to its deformed shape in **Fig. 5. 13** (b). It indicates that the leadfree solder material integrates the package better under low temperature, therefore a larger bending is expected. This phenomenon is caused by creep and plastic behaviours of solder material in high temperature. As these two inelastic behaviours are obvious due to a high activation energy, the bumps present some "flow" properties under high temperature. Under a low temperature loading, elastic behaviours are the mainly mechanical properties of lead-free solder (**Fig. 5. 13** c). As a comparison, the levels of warpage in the models show not much differences of low temperature when inelastic behaviours are not included in the model (**Fig. 5. 14** b).

Moreover, residual deformations of the studied package were found at the end of the third cycle. It proves that inelastic strains of solder accumulate in each thermal cycle. The accumulated inelastic strains are the potential reason for fatigue failures in solder bumps, which will be discussed in details below. Based on these results, creep is an important issue to predict adequately stress distributions and their evolution in simulations of mechanical deformation of the BGA package, especially at high temperature. Creep properties of solder should be included in all the simulations about mechanical behaviours of solder bumps below.

It is worthy noticing that the deformation of the outmost solder bump is larger than other bumps when package temperature changes. This indicates that it experienced greater stress and strain status. Hence, a local fine-mesh FE model is considered for the outmost solder bump as it will be the critical location for thermal fatigue.

5.3.2 Influence of underfill on mechanical behaviours

In most cases an electrically-insulating adhesive is underfilled between chip and substrate to provide a stronger mechanical connection and heat bridge. In this section, the effects of the underfill on solder bumps were estimated.

To investigate the effects of underfill, the maximum stress in the outmost solder bump are depicted in **Fig. 5. 15**. The highest stress of the bump occurred at the start of low-dwell-temperature (t = 780s) according to time history outputs of ABAQUS 6.14. For

the convenience of discussion, the model without underfill is regarded as Case A and the model considering effects of underfill is call Case B. From this picture, the lower stress value of Case B is close to Case A, while the its maximum stress is approximately 11.5% less than Case A. Furthermore, the distribution of the stress in Case A presents symmetry to the centre line while Case B is symmetric to the centre point. It indicates that the underfill tends to integrate the deformation of solder bump with it. Moreover, as presented in **Fig. 5. 15**, the high and low stress area in Case A are close to each other while they are relatively far away in Case B. Given the stress range in the two pictures, it can be regarded that the stress gradient of Case A is larger than Case B.

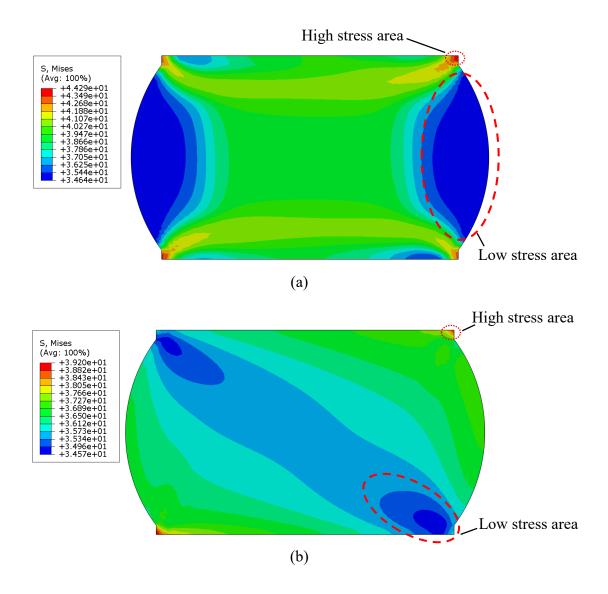


Fig. 5. 15. FE-simulated stress distribution of the outmost solder bump at start of lowdwell-temperature period in first cycle (t = 780s): (a) Case A (underfill excluded); (b) Case B (underfill included)

Therefore, the underfill distributes the thermal expansion mismatch between the chip and the substrate, preventing stress concentration in the solder bumps. Due to its obvious effects on stress distribution of the solder bumps, the underfill is taken into consideration in the following simulations. However, as its stress state is not related to the final failure of the solder bump, the underfill is usually hided in following figures.

5.3.3 Stress distribution and evolution of solder bumps: effect of IMC layers

A distribution of von-Mises stress in the solder bump array of the FE-model after three thermal cycling loads is presented in **Fig. 5. 16**, which also clearly shows the stress status of the outmost bump. IMC layer was not included in this model. For the convenience of observation, the rest materials were hidden from the figure.

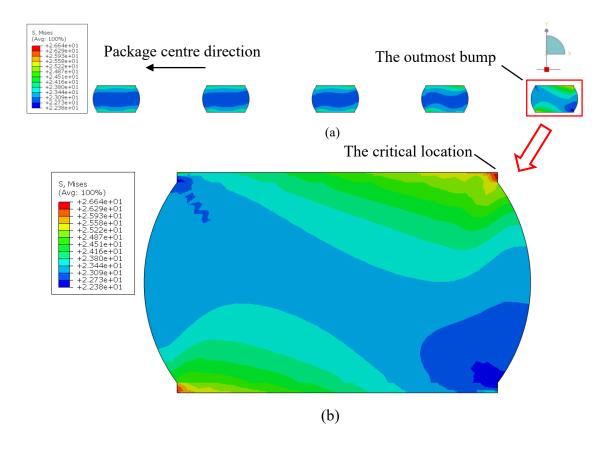


Fig. 5. 16. Distribution of Mises stress at the end of thermal cycling (t=3600s): (a) in the bump arrays; (b) in the outmost solder bump

As the coefficient of thermal expansion of BT-substrate is much higher than that of silicon, expansion or shrinkage of the substrate is larger than that of the chip under temperature changes. However, solder bumps also act as a connection of the chip and the substrate, constraining their relative displacements; the solder bumps, therefore, undergo an alternating shear deformation along the interface between the chip and the substrate. Moreover, as the elastic modulus of chip is much higher than that of the substrate, the changes in distance between the chip and the substrate were not the same when the package tends to deform together. Therefore, the bumps also underwent tensile and compression deformation. According to Fig. 5. 16 (a), the solder bumps present a trend that the stress distribution presents higher centre-symmetry when the its distance to package centre increases. Since displacements of the chip and the substrate at their edges are larger than that at the centre, the peripheral joints are subjected to higher deformations, resulting in larger residual stresses. In Fig. 5. 16, the largest residual stress is distributed in the outmost solder bump. Therefore, it will be investigated as a critical part of the package.

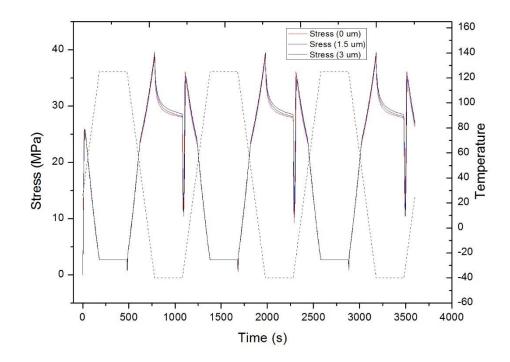


Fig. 5. 17. Stress history of the critical location in the outmost solder bump

To figure out effects of the IMC layer, it was introduced to the model for comparison. As presented in Section 5.2.1, two different thicknesses of IMC layer were employed in simulations for a comparative study. Hence, three FE models with the IMC layer of 0 μ m (no IMC layer), 1.5 μ m and 3 μ m were simulated. The stress history of the critical location in the outmost solder bump are plotted in **Fig. 5. 17**.

In this figure, stress histories of the three models are plotted by solid lines; the red, blue and black solid line represents the bump with IMC thickness of 0 μ m, 1.5 μ m and 3 μ m, respectively. The temperature of thermal loading is also depicted by dash line in this figure for discussion.

As presented in Fig. 5. 17, the stress history of the critical location present cyclic fluctuation with temperature change. The curves with different thicknesses of IMC overlap with each other in most time, which means that the increase of the IMC layers thickness have very little effects on the stress status in a solder bump. However, some differences can be observed at low-dwell-temperature periods while there is no significant variance at high temperatures. Due to their elastic properties, the chip and the substrate tends to deform more when temperature increases. However, the solder material presents inelastic under high temperature. Its plastic and creep properties release the stress in the bump continuously, and finally enters into plastic flow at highdwell-temperature period. In fact, there are two factors affecting the stress in the solder bump. The first one is inelastic properties of solder alloy; the second is the larger relative displacement of chip and substrate in higher or lower temperature. When the package temperature increase from room level, these two factors have contrary effects. The second factor are decreased by the first factor. Meanwhile, during low temperature period, the two factors have the same effects on stress in bump, which make it larger than other period of thermal cycling. Some literatures based on simulation about stress evolution in lead free solders also presented some similar curves [4][9]. In [4], the stress history of a package chip on board was studied and presented. The diameter and the SOH of the solder bumps in [4] are close to the model in this research. However, the bumps connect a BT-substrate together with a FR-4 PCB, which have similar elastic properties. Therefore, the maximum stress calculated by [4] is smaller, meanwhile, its evolution trend showed similarities to this simulation.

For a further investigation on stress situation in the outmost solder bump, its stress

components at -40 °C in first cycle (t = 780 s) are presented in **Fig. 5. 18**. It was found that the largest stress components are the normal stresses σ_{11} , σ_{22} , the levels of which are of the same order of magnitude as the von-Mises stress. Normal stress σ_{11} represents the tensile or compression along X-axis. According to **Fig. 5. 18**, all the σ_{11} are positive, indicating a tensile condition in along X-axis in the bump. In fact, since the CTE of the tin alloy is larger than substrate and the chip, its shrinkage under low temperature is higher than the other two components. Furthermore, as the CTE of chip is much smaller than tin, then tensile stress on the top interface of the bump is larger than bottom. To conclude, the stress component along X-axis is mainly caused by self-expansion/shrinkage of the solder bump.

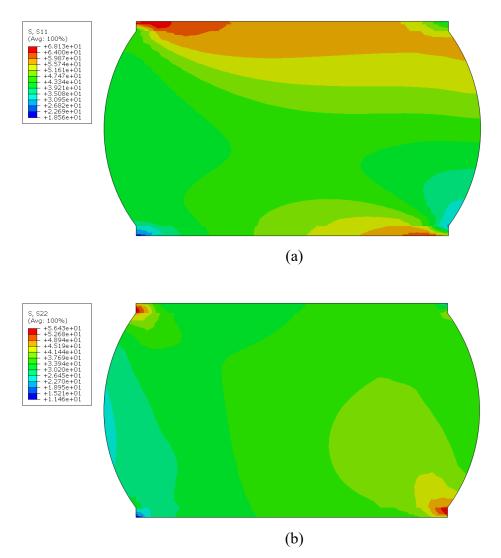


Fig. 5. 18. Stress distributions in outmost joint without IMC layer at -40 °C in first cycle (t=780s): (a) stress component σ_{11} ; (b) stress component σ_{22}

Another stress component, σ_{22} , is also positive in the solder bump, indicating that underwent a tension between top and bottom surface. This character of stress is resulted by the different extents of warpage of the chip and the substrate due to their different elastic moduli. Under low temperature, the substrate tends to shrink more than chip, resulting a separation trend between these two components. Obviously, the outmost solder bump experienced the largest separation, which results in the largest tension in the package.

5.3.4 Stress state of solder bumps: effect of miniaturization

Distributions of von-Mises stress in solder bumps of 20-µm-SOH after three thermal cycles are presented in **Fig. 5. 19**. To investigate the direction effect of c-axis in Sn lattice structure, two cases of the outmost solder bump, c-axis along X-coordinate and Y-coordinate, are also illustrated in **Fig. 5. 19**. For the convenience of description and discussion, the former is called Case A and the latter is called Case B. The IMC layer was removed from this figure for the observation of stress state in the solder part.

Unlike the solder bumps in macro size, the high stress area is no longer distributed at the righter upper corner of the solder part, according to **Fig. 5. 19**. Instead, the highest stress is located at the adjacent area of the peak of scalloped IMC layer, as circled in **Fig. 5. 19** (b). Based on these results, a concept of effective IMC layer can be proposed for the bumps with scalloped IMC layer. Due to the stiffness property of IMC, the deformation of the solder material located in valley area is constraint by the two adjacent peaks of IMC layer. This part solder experienced less deformation in thermal cycling. Therefore, the effective IMC thickness. The distance from the scalloped top to the valley of the IMC layer can be treated as an effective IMC thickness. This brings the locations of the largest stress near the IMC scalloped tops.

For the effect of anisotropy in elastic properties of Sn grain, the simulation results of Case A are very close to Case B. Considering the simulation error of FEA, it can be concluded that the anisotropy of elastic properties have almost no effects of distribution of the stress in a micro-size bump. However, the anisotropy of inelastic properties of

Sn grain was not taken consideration into this simulation due to lack of experimental data and consistent results. Hence, it cannot be concluded that the anisotropy of Sn grain has no effects on mechanical behaviours of the solder bump. Some further investigations are needed to obtain the description of inelastic behaviours of single Sn grain.

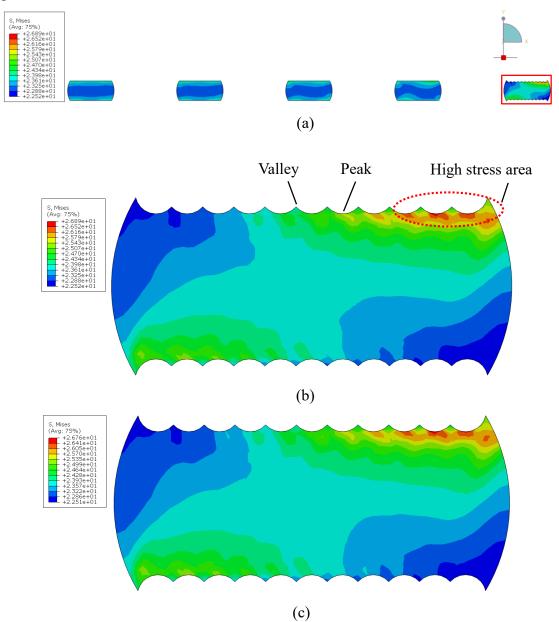


Fig. 5. 19. Distribution of von Mises stress in package with solder bumps of 20-μm-SOH after third cycle (t=3600 s) in: (a) the bump arrays; (b) the outmost solder bump with c-axis along X-coordinate; (c) (b) the outmost solder bump with c-axis along Ycoordinate (IMC layer was removed)

In order to further investigate on stress situation in the outmost solder bump under micro

size, its stress components at -40 °C in first cycle (t = 780 s) are presented in **Fig. 5. 20**. Considering the minor effects of Sn grains on mechanical behaviours of the solder bump, only the stress state in Case A is illustrated in this figure. It was found that the largest stress components are the normal stresses σ_{11} , σ_{22} , the levels of which are of the same order of magnitude as the von-Mises stress. Here, σ_{11} represents tensile or compress conditions of materials along X-coordinate. Notice that σ_{11} in valley area is relatively low compared to the highest value in **Fig. 5. 20** (a), indicating the mechanical constrain effects of IMC scalloped shape along X-coordinate. On contrary, high values of σ_{22} tend to distribute in the valley area, which proves that these locations underwent tension during thermal cycling. From these results, deformations of the solder along its diameter direction are limited by the scallop-shaped IMC layers, resulting a reduction in effective height of solder; while deformations along the bump's height direction are affected less by IMC layers.

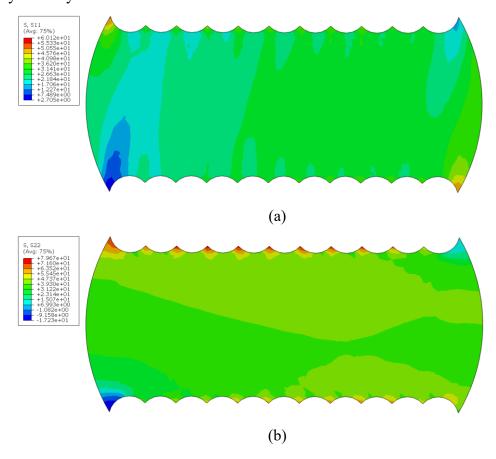


Fig. 5. 20. Stress distributions in outmost solder bump of 20- μ m-SOH with c-axis of Sn grain along X-coordinate at -40 °C in first cycle (t=780s): (a) stress component σ_{11} ; (b) stress component σ_{22}

5.4 Fatigue-life prediction for solder bumps under thermal cycling loads

5.4.1 Fatigue-life prediction method

Some models were proposed to evaluate the fatigue life of solder joints; they were discussed in Section 2.2.3 The most widely accepted and commonly used models are based on a single parameter - inelastic accumulated strain - as the damage indicator. The model based on the Coffin-Manson equation for the life prediction for the Sn-Ag-Cu solder bump was adopted for this study:

$$N = C_1 (\Delta \varepsilon_{in}^{acc})^{C_2}, \qquad (5-2)$$

where N is the number of cycles; C_1 and C_2 are the material constants mentioned in section 2.2.3, with values 27.63 and -1.08 for SAC305, respectively; $\Delta \varepsilon_{in}^{acc}$ is the accumulated inelastic strain in a stable cycle, which could be obtained by summing the equivalent inelastic strain increments of all load steps in the stable cycle:

$$\Delta \varepsilon_{in}^{acc} = \sum_{i=1}^{n} \Delta \varepsilon_{in,i}^{eqv} . \qquad (5-3)$$

According to [5], the accumulative equivalent inelastic tends to be steady after three cycles of thermal loadings. Furthermore, the inelastic strains accumulated in the third cycle are commonly used to evaluate the fatigue cycles of solder bumps. Hence, $\Delta \varepsilon_{in,i}^{eqv}$ is represented by the strains accumulated in the third cycle. The equivalent inelastic strain increments of the *i*th load step, $\Delta \varepsilon_{in,i}^{eqv}$, can be expressed as a function of inelastic strain component increments of the *i*th load step based on simulation results:

$$\Delta \varepsilon_{in,i}^{eqv} = \frac{\sqrt{2}}{3} \left\{ \left(\Delta \varepsilon_{11,i}^{in} - \Delta \varepsilon_{22,i}^{in} \right)^2 + \left(\Delta \varepsilon_{22,i}^{in} - \Delta \varepsilon_{33,i}^{in} \right)^2 + \left(\Delta \varepsilon_{33,i}^{in} - \Delta \varepsilon_{11,i}^{in} \right)^2 + \frac{3}{2} \left[\left(\Delta \varepsilon_{12,i}^{in} \right)^2 + \left(\Delta \varepsilon_{23,i}^{in} \right)^2 + \left(\Delta \varepsilon_{13,i}^{in} \right)^2 \right] \right\}^{1/2} .$$
(5 - 4)

In this simulation, inelastic strain of component increments includes only creep and plastic strains. Therefore, $\Delta \varepsilon_{in,i}^{eqv}$ is obtained by summing the plastic and creep parts:

$$\Delta \varepsilon_{in,i}^{eqv} = \Delta \varepsilon_{pl,i}^{eqv} + \Delta \varepsilon_{cr,i}^{eqv}$$
(5-5)

In FE software ABAQUS 6.14, $\Delta \varepsilon_{pl,i}^{eqv}$ represents the equivalent plastic strain PEEQ and $\Delta \varepsilon_{cr,i}^{eqv}$ is the equivalent creep strain CEEQ. All the data for PEEQ and CEEQ come from the results of simulations.

5.4.2 Results and discussion

Accumulated inelastic strains in solder bumps

According to Equation 5 - 2, larger inelastic strains result in a shorter fatigue life of a solder bump. To evaluate the service life under thermal cycling, distributions of CEEQ and PEEQ in solder bumps should be figured out. As the outmost solder bump underwent the largest deformation during thermal cycling, its CEEQ and PEEQ distribution is supposed to be the estimation indicator of fatigue life. Here, the distribution of CEEQ and PEEQ in the outmost solder bump with 200 μ m stand-off height at the end of simulated thermal cycling are displayed in Fig. 5. 21. There is no IMC layer in this model.

In this figure, the distribution of CEEQ in macro size bump presents similarities to its stress distribution. For an inelastic material, a larger inelastic strain causes larger residual stress in the structure. Therefore, the highest values are located at the right upper and left lower interfaces, where the largest residual stress is located. However, the distribution of PEEQ showed some differences to the CEEQ. The largest value of PEEQ was found only at the left lower corner of the bump. Considering the magnitude of PEEQ is close to CEEQ, the inelastic strains of both A and B in **Fig. 5. 21** need to be investigated to determine the largest strain in the solder bump. Therefore, the accumulative inelastic strain during thermal cycling of location A and B are plotted in **Fig. 5. 22**.

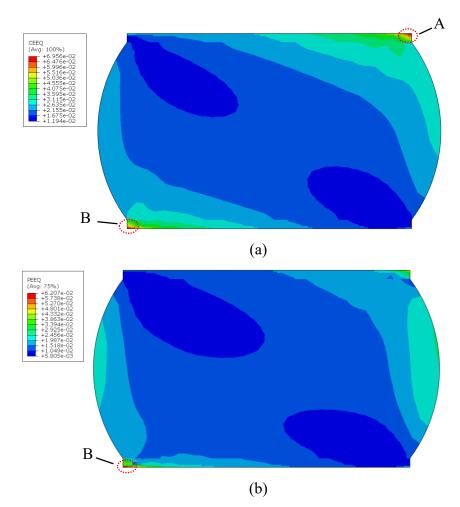


Fig. 5. 21. Distributions of accumulative inelastic strains in the outmost bump with 200-µm-SOH with no IMC layer after the third cycle (t=3600 s): (a) creep strain; (b) plastic strain.

From this figure, the inelastic strain of the location B was higher than location A. Therefore, its inelastic strain history was used to estimate the fatigue life of the solder bump without IMC layer. Some further investigations on the models with IMC layer also indicated that the largest inelastic strain was distributed at the lower left corner of the solder, corresponding to the B in the bumps without IMC. The results of inelastic strains at these locations are also plotted in **Fig. 5. 22**. From the curves, the formation of IMC layer in the solder bump increased its inelastic strains. Furthermore, with the increasing thickness of IMC layer, the largest inelastic strains grew fast. In fact, the existence of the IMC layer reduced the thickness of solder alloy, which underwent inelastic strains during thermal cycling. Consequently, the strains became larger due to its reduction in SOH directions as the deformations of the chip and the substrate did not

change. Hence, the formation of IMC layer tends to reduce the thermal-fatigue reliability of flip-chip package.

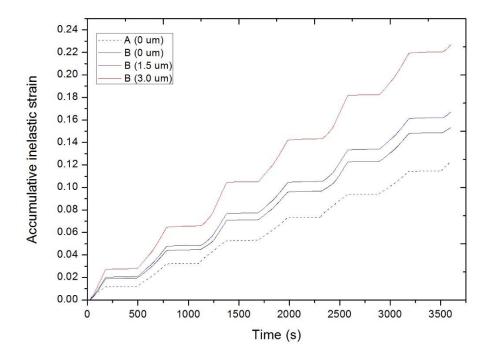
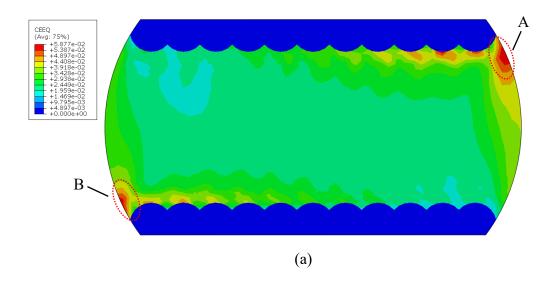


Fig. 5. 22. Evolution of accumulated equivalent inelastic strains at A and B in the solder bump of 200-µm-SOH with different thickness of IMC layer.

For the package with solder bumps of the 20um stand-off height, the distributions of CEEQ and PEEQ in the outmost solder bump in Case A at the end of thermal loadings are presented in **Fig. 5. 23**.



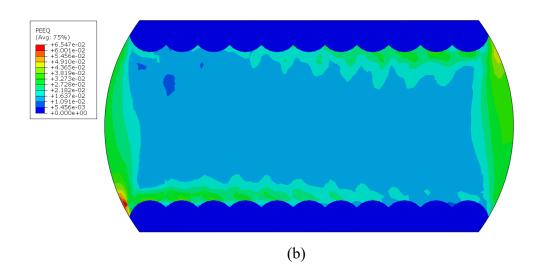


Fig. 5. 23. Distribution of equivalent inelastic components in outmost solder bump with 20-µm-SOH: (a) the equivalent creep strain; (b) the equivalent plastic strain

According to **Fig. 5. 23**, distributions of CEEQ and PEEQ in the solder bump with 20- μ m-SOH presented some differences. Some large values of inelastic strains were still distributed at the right upper and left lower area of solder alloy. However, the largest inelastic strains were found at the contacting area between the solder and the underfill, as circled in **Fig. 5. 23** (a). Correspondingly, like the distribution of PEEQ in macrosize solder bump, the largest PEEQ of the solder bump with 20- μ m-SOH was located at location B, as presented in **Fig. 5. 23** (b). Therefore, the inelastic strains of these two locations need some further investigations to decide the fatigue-life calculation indicator.

It can be observed from that the inelastic strains of location B is larger than A, which shows similarity to the macro-size bump. Therefore, the evolution history of the inelastic strains at location B was used in the calculation of thermal fatigue life of micro-size bump. As a comparison, the curves indicating the history of inelastic strains in the bumps of 200-µm-SOH without IMC were also plotted in **Fig. 5. 24**. Based on the curves, the micro-size bump experienced smaller inelastic strains during thermal cycling. Since the elastic properties of IMC layer is closer to chip and substrate than solder alloy, it integrates the whole package under the warpage deformation. Therefore, the micro-size bumps undergo smaller deformation during thermal cycling due to the increase of package strength.

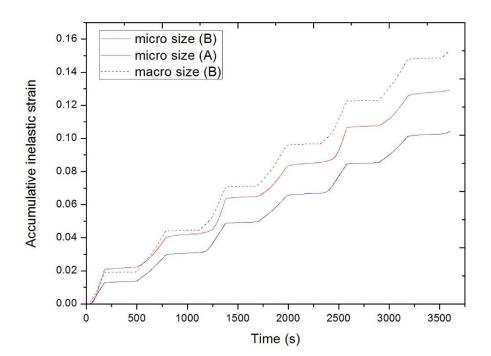


Fig. 5. 24. Evolution of accumulated equivalent inelastic strains at A and B in the solder bump of 20-μm-SOH

Calculated fatigue life

Based on the Equation 5 - 2, **Table 5. 10** gives the results of reasonable fatigue life prediction under the consideration of IMC thickness and bump size. The simulated thermal-fatigue life of the solder bump of 200-µm-SOH is 675 cycles without considering the effects of IMC layer. In most literatures, a chip-scale package (CSP) was usually simulated and studied. In this structure, a BT-based chip was mounted on a PCB, forming a similar structure in this chapter. However, as the CTE of BT-substrate and PCB are very close, thermal fatigue life of this structure tended to be long. In [5], the predicated thermal-fatigue life reached around 2500 cycles. However, the structure simulated in this study focused on the BT-based chip only. Under this condition, the difference of CTE of chip and BT-substrate is very large, resulting a much shorter thermal-fatigue life. Based on a previous simulation in [10], the thermal fatigue life of this structure in around 1200. However, the properties of underfill in [10] were set as elastic, which has been proved by [14] that it overestimated the thermal-fatigue lives of the package. Here, to validate the simulation in this chapter, if the underfill in this simulation was set the same as [10], the updated fatigue cycles were 1056, which was close to the results of [10].

Bump	$\Delta arepsilon_{in}^{acc}$	Predicted thermal-fatigue cycles	Percentage compared to (A)
Macro size with no IMC	0.05191	675 (A)	0%
Macro size with 1.5-µm IMC	0.05668	614	9%
Macro size with 3.0-µm IMC	0.07728	441	34.6%
Micro size	0.04278	831	123.1%

Table 5. 10. Comparison between the predicted fatigue cycles for the solder bump with different IMC thickness and bump size

From the results in **Table 5. 1**, the IMC layer decreased thermal-fatigue cycles of the package. With the increase of IMC layer thickness, this reduction was more obvious. In contrast, the solder bump of 20-µm-SOH showed better reliability under thermal-cycling loads, even its IMC proportion was much larger than the bump in macro-size bump. In fact, the less mechanical property difference between IMCs and other components (chip and BT-substrate) integrates the whole package. A large proportion IMCs in micro-size bump tends to enforce the strength of the package, leading to a smaller concave-up and concave-down warpage. Under this condition, the solder part in the bump experiences smaller cycling deformations. Based on these discussions, a large proportion of IMC layers in a solder bump improves the thermal-fatigue reliability of a package.

5.5 Summary and conclusions

In this chapter, FEA models of flip-chip solder bumps with micro structures were developed. Their performances under thermal cycling loads were presented and discussed. The service -life spans of solder bumps based on accumulative inelastic strain were estimated. From the presented results and discussions, it could be concluded that:

- Creep properties of the solder affected its mechanical behaviour under high temperature significantly. Its high-temperature behaviour was influenced by creep properties insignificantly. To estimate the mechanical behaviour of solder bumps properly, creep properties must be included into simulations.
- The joint located on the edge of the BGA underwent the largest deformation in the package. The highest stresses and strains were located at the upper right corners of the outmost solder joints, which indicated that this place is the most critical area in the whole package.
- 3. The IMC layers affected the stress distribution in the solder bumps. Formation and increased thickness of the IMC layer resulted in heavier stress concentrations at the critical area in the bumps, reducing thermal-fatigue reliability of the package.
- 4. The solder bumps with the tens of microns stand-off height presented higher stiffness under thermal cycling loads. A large proportion of IMC layers in a solder bump improved the thermal-fatigue reliability of a package
- 5. The scalloped shape of the IMC layer formed in the solder bumps with the tens of - microns stand-off height changed the distribution of stresses and strains. The stress and strain concentrations could be found at the area of the solder adjacent to the tops of scalloped IMCs on the right upper side and the contacting area of underfill, which showed significant differences with the large solder bumps.
- 6. Formation of the IMC layer decreased the fatigue life cycles of solder bumps under cycling thermal loading, as the existence of the IMC layer reduced the effective stand-off height of the solder bumps. The predicted life of solder bumps with the small stand-off height was much longer than that of the large ones.

Reference

- [1] Liu X. S., Lu G. Q., "Effects of solder joint shape and height on thermal fatigue lifetime", *IEEE Transactions on Advanced Packaging*, 2003, 26 (2), pp. 455-465.
- [2] Khor C. Y., Abdullah M. A., Leong W. C. "Fluid/ structure interaction anlysis of the effects of solder bump shapes and input/output counts on moulded packaging" *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2012, 2 (4), pp. 604-616.
- [3] Liu Y., Liang L., "3D Modeling of electromigration combined with thermalmechanical effect for IC device and package", *Microelectronics Reliability*, 48 (2008), pp.811–824.
- [4] Che F.X., Pang John H. L., "Characterization of IMC layer and its effect on thermomechanical fatigue life of Sn-3.8Ag-0.7Cu solder joints", *Journal of Alloys* and Compounds, vol. 541 (2012), pp. 6–13.
- [5] Chiou Y. Ch., Jen Y. M., Huang Sh. H., "Finite element based fatigue life estimation of the solder joints with effect of intermetallic compound growth", *Microelectronics Reliability*, Vol 51 (2011), pp. 2319-2329.Material properties 1/N
- [6] Frost, H. J. and Ashby, M. F. "Deformation mechanism maps: the plasticity and creep of metals and ceramics", *Pergamon Press*, 1982, Oxford, UK.
- [7] Lau J. H., Lee S.WR., "Modeling and analysis of 96.5Sn–3.5Ag lead-free solder joints of wafer level chip scale package on build up micro via printed circuit board", *IEEE Transactions on Electronics Packaging Manufacturing*, 25 (2002), pp. 51-58.
- [8] Alfred Y., Charles L. and John H.L., "Flip chip solder joint fatigue analysis using 2D and 3D FE models", Proceedings of the 5th International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, 2004.
- [9] Robert S., Sebastian M., "Finite element modelling on thermal fatigue of BGA solder joints with multiple voids", 34th International Spring Seminar on Electronics Technology, 2011, pp. 380-385.
- [10]Pang John H. L., Chong D. Y. R., "Flip Chip on Board Solder Joint Reliability Analysis Using 2-D and 3-D FEA Models", *IEEE Transactions on Advanced Packaging*, Vol. 24 (2001), No. 4, pp. 499-506.
- [11]Gong J. C., Liu C., et al., "Micromechanical modelling of SnAgCu solder joint

under cyclic loading: Effect of grain orientation", *Computational Materials Science 39 (2007)*, pp. 187–197.

- [12] Vold C. L., Glicksman M. E., et al., "The elastic constants for single-crystal lead and indium from room temperature to the melting point", *Journal of Physics & Chemistry of Solids*, 1977, 38(2):157-160.
- [13]Yomogita K., "Effect of Recovery on the Plastic Deformation of β-Tin Single Crystals", Japanese Journal of Applied Physics, 1970, 9(12):1437-1444.
- [14] Feustel F., Wiese S., Meusel E., "Time-dependent material modeling for finite element analyses of flip chips", *Electronic Components & Technology Conference*, 2000:1548-1553.

Chapter 6. Electro-migration in single solder bump of BGA

6.1 Introduction

In service of electronic components, electrical currents go through solder bumps, which arouses some reliability issues. As introduced in Chapter 1, currents induce two results in bumps: Joule heating and electro-migration.

Joule heating causes an increase in temperature together with thermal stresses in microsolder bumps. Therefore, Joule heating process is regarded as a multi-physics process as fields of electrical current, temperature and stress under this condition. Electromigration is usually defined as a transport of materials in conductor, leading to gradual changes of microstructure. Generally, electro-migration is caused by an exchange of momentum between conducting electrons and diffusing metal atoms and usually happens under high densities of direct current. As a consequence of their small sizes, magnitudes of current density in solder bumps can exceed 1×10^4 A/cm². The crowded current density transports atoms along the direction of electron flows, i.e., from a cathode to an anode. Hence, atoms piles up at the anode side and voids will appear at the cathode side, changing the microstructure of solder joints and initiating crack propagation. Besides, the movement and coarsen of intermetallic compounds (IMCs) was also observed in experiments [1, 2]. Due to their stiffer mechanical behaviour, the movement of IMCs changes the distribution of stress. Based on the above, electromigration is an important source of micro-structured transformations; the electromigration effect changes the microstructure in solder bumps significantly and forms some voids at the cathode side. When analysing reliability of solder joints, these phenomena caused by electro-migration must be taken into consideration.

As electro-migration is a current-driven process, the distribution of current density in solder bumps determines the effects of electro-migration. However, it is hard to measure

current-density distribution information, with experimental methods in solder bump with its limited size. Therefore, this chapter adopts FEA to investigate distributions of current and temperature in solder bumps under current stressing. Different current flow paths in solder are compared in analysis together with the effect of decreasing bump sizes.

Moreover, movement of metal atoms in solder bumps causes voids formation at the cathode side, which is a critical area for both mechanical and electronic loadings. Therefore, investigation of formation and expansion of void/crack located at the cathode side plays a key role in evaluation of electro-migration. This chapter develops an algorithm based on FEA results of current density distribution to simulate formation and evaluation of void/crack in solder bumps.

6.2 Distributions of Current density and temperature in single solder bump

Electro-migration in solder bumps is affected by two factors, caused by electrical current: current density and temperature distributions. To figure out these factors in a solder bumps, a coupled thermal-electrical analysis based on the finite-element method is used in this chapter. In a coupled FE thermal-electrical analysis, the Joule heat caused by current is a heat source in the model. When current flows across a solder bump, a part of its energy converts into Joule heat:

$$Q = \vec{j}^2 \rho t \quad , \tag{6-1}$$

where Q is the Joule heat density, \vec{j} is the current density vector, ρ is the localized electrical resistivity, t is the current loading time. According to this equation, the current load is supposed to be the loading condition in the FE model.

The Joule heat is transferred to other parts in the model following heat-transfer law after its generation. In this simulation, there is no other heat source except the Joule heat. Therefore, only heat boundary conditions including heat sink and film heat exchange are included in this model. Details of the FE model including boundary conditions and material properties are introduced in this section. The results for a coupled thermalelectrical problem are also presented.

6.2.1 Model description and loading conditions

As the simulation in this chapter focuses on distributions of current and temperature in solder bumps, models based on a single solder bump from the BGA are built here. External mechanical loadings, which result in stress distribution in the solder bump, are neglected, and electrical current is the only loading factor in this simulation. Also, some heat boundary conditions are applied to the FE model.

For the current loading conditions, three typical current-flow paths across a single solder bump as presented in **Fig. 6.1** are commonly used in electronic packages

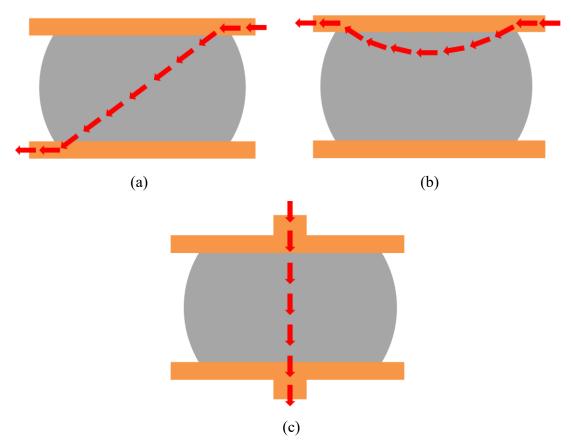


Fig. 6. 1. Three typical current-flow paths in solder bump (red arrows represent possible paths of electrons): (a) from one corner to opposite corner; (b) from one corner to other corner located on same side; (c) from one sides centre to other

The types illustrated as (a) and (b) in **Fig. 6.1** are usually observed in a BGA package where traces of Al or Cu are located in chips and substrate. The main current-flow directions along traces are usually perpendicular to the height direction of solder bumps; it crosses solder bumps in the package from one side to another. The direction of current flow changes when it enters the solder bump. A meshed solder bump with dimensions in **Fig. 6.2** presents current flow paths regarding (a) and (b) in **Fig. 6.1**. To provide current entrance and exit port, copper traces were added on the top and bottom of the solder bump. The size of the solder bump is the same as the large one in Chapter 5.

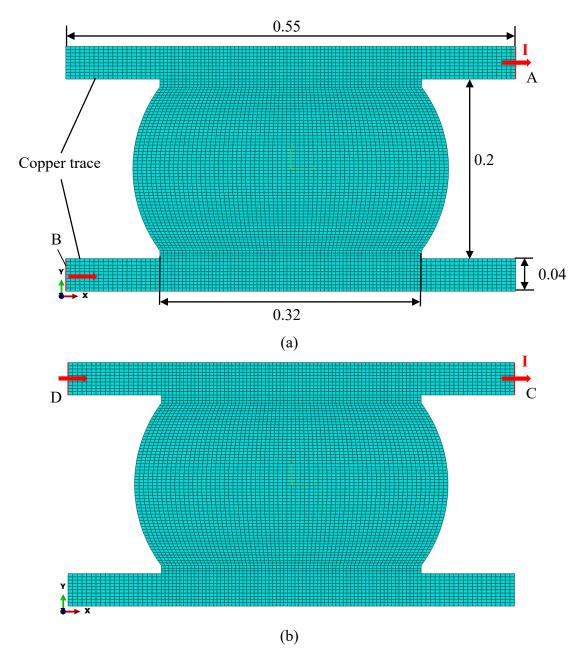


Fig. 6. 2. Geometry and current flow path in a meshed solder bump of BGA

(Unit: mm)

The voids are supposed to be formed at the right upper corner of the solder bump, which was proved the critical place in Chapter 5. Regarding a current flow direction is opposite to a flow direction of electrons, the electrical potential of Port A and C is set as zero while a surface current load is applied on another port. The (a) and (b) in **Fig. 6. 2** are the corresponding situations of (a) and (b) in **Fig. 6. 1**, respectively. A surface current density of 100 A/mm² is applied on Port B and D.

The type illustrated as (c) in **Fig. 6. 1** are commonly found in a typical TSV package. The main current-flow directions along traces are usually the same as the height direction of solder bumps. The direction of current flow does not change when it enters the solder bump. A meshed solder bump with dimensions in **Fig. 6. 3** presents current flow paths regarding (c) in **Fig. 6. 1**. The size of the solder bump is the same as the large one in Chapter 5. For the electrical boundary conditions in **Fig. 6. 3**, the electrical potential of Port E is set as zero while a surface current load 100 A/mm² is applied on Port F.

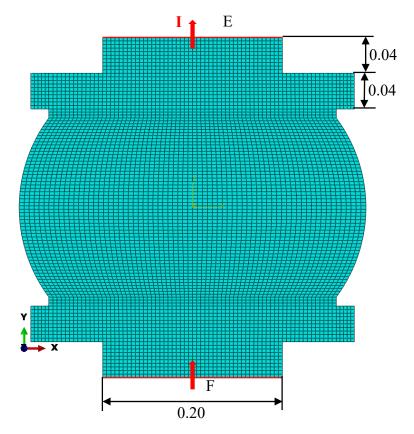


Fig. 6. 3. Geometry and current flow path in a meshed solder bump of TSV (Unit: mm)

Different current-flow paths results in different current crowding effects in the solder bumps. So, the distributions under the effects of these three typical current loadings should be analysed. The models (a) & (b) in **Fig. 6. 2** and (c) in **Fig. 6. 3** are characterized as Model I, II and III in the following discussion of this chapter. All the models were analysed in ABAQUS 6.14 by using coupled thermal-electric steady state step. The element type in these model is set as DC2D4E: a 4-node linear coupled thermal-electrical quadrilateral. Model I and II contains 6470 elements while Model III contains 6750 elements.

Decreasing the size of a solder bump and its geometry leads to current crowding. This results in an increasing value of current density, generating a large amount of Joule heat. The Joule heat concentrates in some certain places in the solder bump, causing high temperature gradients.

The current load defined the electrical boundary condition in this model. The currentdensity distribution could be calculated based on the descriptions above. To obtain the temperature distribution, heat boundary conditions on all external edges should also be defined, with the Joule heat supposed to be the heat source in this model.

The exposed external edges in this model could be classified into two types. All the solder bumps surfaces and a part of copper traces were exposed to ambient environment, as highlighted in **Fig. 6. 4** (a). These surfaces were supposed to be contacted with air. The air is treated as a heat sink as its temperature was mainly influenced by heat generated by other components in the electronic packages. In this simulation, the temperature of air kept at 115 °C. The surface film coefficient between these surfaces and air was set as 20 W/(m²•K) [**3**].

Other external surfaces of the FE model are faces of the copper traces embedded in the chip and substrate, as highlighted in **Fig. 6. 4** (b). These surfaces are contacted with other materials in the package. To simplify the calculation and analysis, temperatures of the chip and substrate are also set as a constant value, 120 °C [8]. Considering heat conductivity of that chip and the substrate are relatively larger than that of air, the surface film coefficients between these faces and other materials were set as one value,

50 W/($m^2 \cdot K$) [3].

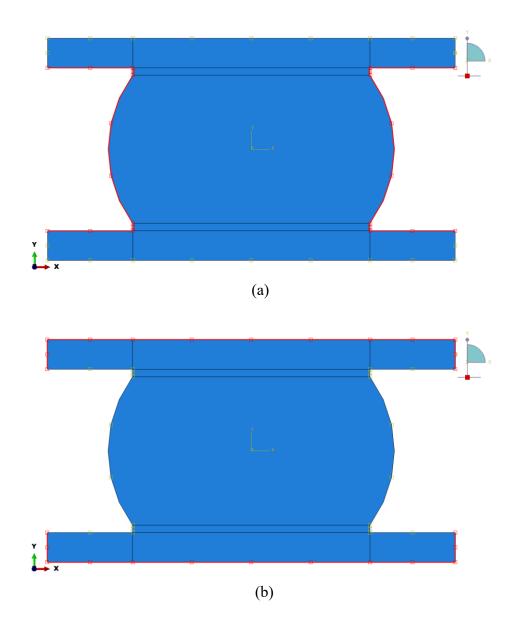


Fig. 6. 4. Heat boundary conditions of FE models: (a) surfaces in contact with air; (b) surfaces embedded in chip and substrate.

6.2.2 Material properties

The simulated model underwent a fully coupled thermal-electrical process. Only metal parts in the package were included in simulations. Basic material properties including density, specific heat, thermal conductivity and electrical conductivity should be taken into consideration. The simulated model contains two materials: copper (trace) and SAC305 (solder). The relevant properties of these materials are listed in **Table 6.1**. As dimensions of the FE model is based on *mm*, the properties in **Table 6.1** are expressed base on *mm* unit

 Table 6. 1. Material properties used in FE models for coupled thermal-electrical

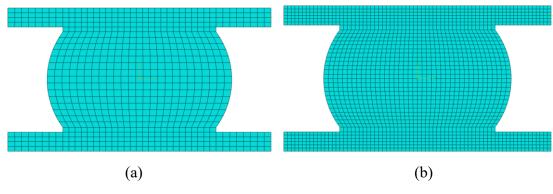
Propertires	Density (tone/mm ³)	Thermal Conductivity (W/mm-K)	Electrical Conductivity (/Ω-mm)
Copper	8.94e-9	0.3862	58800
Solder	7.4e-9	0.078	8120
IMC	8.28e-9	0.0341	5700

analysis [3, 5]

6.2.3 Mesh convergence of the model

In FE analysis, mesh quality of model is important for calculation accuracy and efficiency. Theoretically, a finer mesh leads to better accuracy of analysis results. However, an increasing number of elements results in higher calculation cost. Hence, choosing an adequate mesh density for FE model is important. Here, Model I is used for the mesh convergence analysis.

Fig. 6. 5 presents the elements in the solder bump under four mesh densities. The number of elements in each solder bump is 753, 1880, 4865, 11500 in (a), (b), (c) and (d) respectively.



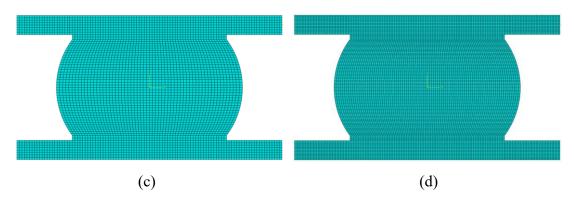


Fig. 6. 5. Meshed solder bump with different numbers of elements: (a) 753 elements,(b) 1880 elements, (c) 4865 elements and (d) 11500 elements

This convergence analysis adopts some maximum values of the outcomes from ABAQUS 6.14 coupled thermal-electric (Max *EPG*, Max *EPOT* and Max *HFL*) as evaluating indicators. These outcomes will be discussed and explained in next section. The calculation cost and evaluating indicators for different element numbers are listed in **Table 6.2**.

 Table 6. 2. The calculation cost and evaluating indicators for different element numbers

Element	Computing	Memory	Max EPG	Max EPOT	Max HFL
case	time	size	V/mm	mV	W/mm ²
(a)	30 s	372 KB	4.435e-2	7.960	0.8802
(b)	45 s	613 KB	4.577e-2	7.964	0.9639
(c)	1 min 30 s	1123 KB	5.009e-2	7.967	1.0220
(d)	2 min 23 s	2629 KB	5.045e-2	7.968	1.0645

When the element number increases from 753 to 11500, all the thermal-electrical outcomes increases. This indicates that the analysis accuracy rises with the growing number of elements. When the number of element rises over 4304, the computing time and memory size increases significantly while the increase of accuracy is limiting. Considering the combination of accuracy and efficiency, the mesh density closing to (c) is a relatively suitable choice for the FE coupled thermal-electrical analysis in this chapter.

6.2.4 Results and discussion

• Output of thermal-electrical analysis in ABAQUS

The simulation in this section deals with a steady state process. Once the loading and boundary conditions in the FE model were defined, the simulation results presented certain values if the structure of the model did not change. Therefore, the results in this section are supposed to be for steady-state conditions.

In ABAQUS, the output variables of thermal-electrical analysis include four values: the current magnitude and components of the electrical potential gradient vector (*EPG*), current magnitude and components of the heat flux per unit area vector (*HFL*), electrical potential degrees of freedom at a node (*EPOT*) and temperature values at a node (*NT*). The variable *EPOT* is the electrical potential, φ , at a node in the model. The variable *EPG* in two-dimensional coordinate system is defined as:

$$EPG = \left(-\frac{\partial\varphi}{\partial x}, -\frac{\partial\varphi}{\partial y}\right) . \tag{6-2}$$

According to the relationship between electrical potential, φ , and electrical field strength, \vec{E} , the variable EPG represents the distribution of \vec{E} in the model. Based on the Ohm's law, the relationship between the current density, \vec{j} , and \vec{E} is presented as:

where σ is localized electrical conductivity, ρ is localized electrical resistivity. According to Equations 6-2 and 6-3, the electrical-current density could be expressed with *EPG*, as:

$$\vec{j} = \frac{1}{\rho} EPG \quad . \tag{6-4}$$

Also, the electrical-current density could be calculated and expressed as *ECD* in ABAQUS 6.14.

Another important variable in this simulation is the heat flux per unit area vector, *HFL*. Its relationship with temperature gradient is as:

$$HFL = \left(-k\frac{\partial T}{\partial x}, -k\frac{\partial T}{\partial y}\right) = k \left(-\frac{\partial T}{\partial x}, -\frac{\partial T}{\partial y}\right) = -k\nabla T \quad , \qquad (6-5)$$

where k is localized thermal conductivity. In this section, the distributions of *ECD*, *HFL* and *EPOT* from ABAQUS 6.14 output results are presented. Among them, *ECD* and *HFL* are the two key variables for the electro-migration process. Therefore, these two outputs should be presented and analysed in details.

The current density and temperature distribution in Model I

The distributions of *ECD* in Model I are presented in **Fig. 6. 6**. In this model, the electrical current enters from the left lower side to the right upper side, as presented in **Fig. 6. 2** (a). The copper traces are hided from this figure. Here, the effects of intermetallic compound (IMC) were not included in this model. This type of current-flow path was commonly used in some previous simulation studies [**8**, **9**], and it was called a daisy-chain structure when bumps in array were connected with others.

According to **Fig. 6. 6**, the distribution of the *ECD* vector is symmetric regarding to the centre point of the solder bump, as the electrical current loading was symmetric with regard to the point. From the distribution of the *ECD* vector magnitude, the largest values of this vector are located at the lower left and upper right area of the solder ball, as red circled in **Fig. 6. 6** (a). At these locations, according to **Fig. 6. 6** (b) and (c), the current density component along X-axis is 106.1 A/mm² while its component along Y-axis is 393.3 A/mm². This indicates that a large part of current changes direction from X-axis to Y-axis as its direction is all along X-axis in copper traces. The direction change at these locations resulted in a current crowding effect. The current density at the current entrance and exit of the solder bump is 430.0 A/mm² while

the average current density is 65.19 A/mm^2 . It can be seen that the current density at the corner is approximately one order of magnitude higher than the average value due to the electrical current crowding effect. It agrees the conclusion of reference [10].

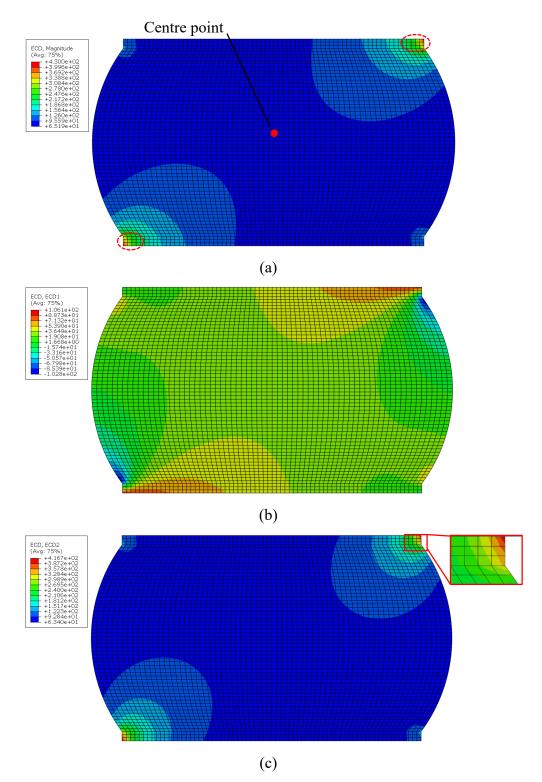


Fig. 6. 6. FE-simulated distribution of the *ECD* vector in Model I (unit: A/mm²): (a) vector magnitude; (b) vector component along X-axis; (c) vector component along Y-

axis 126 As electro-migration is usually caused by high-density electron wind, voids or cracks resulted by electro-migration may occur at the current exit place firstly. Even the average current density is a solder bump is under the threshold value of triggering electro-migration, its value at the contact surface of the bump may exceed the threshold. Furthermore, current crowding leads to an increase in Joule heating, and the resulting hot spots are surrounded by temperature gradients. **Fig. 6. 7** presents the distribution of the *HFL* vector in the bump, which is proportional to temperature gradient according to the Equation 6 - 5.

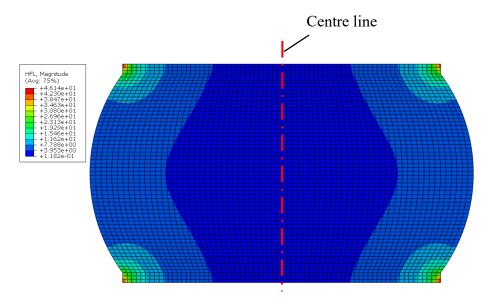


Fig. 6. 7. FE-simulated distribution of the HFL vector magnitude in Model I (unit: W/mm^2)

In Fig. 6. 7, the distribution of the *HFL* vector is symmetric with regard to the centre line of the solder ball, although the heat resource induced by the electrical current-flow was symmetric with regard to the centre of the solder bump. As the solder bump is formed by metal components and their thermal conductivity is relatively high, the generated Joule heat transferred to other parts of the solder bump soon. The distribution of transferred heat was affected by other heat boundary conditions, including the account for sink temperature and the film heat-exchange coefficient. As the heat boundary conditions were symmetric with regard to the centre line of the solder bump, the distributed heat presents the similar situation. In a previous simulation study [8], a distribution of temperature gradient also presented symmetrical characteristic to the centre line of the bump, while its current loading type is the same as Model I. From the

distribution of the *HFL* vector magnitude, the largest values of vector were located at the four corners of the solder ball. The highest value of temperature gradient could be calculated from Equation 6 - 5: $\nabla T_{\text{max}} = 591.5$ K/mm.

From **Fig. 6. 6** and **Fig. 6. 7**, it can be seen that both the maximum value of current density and temperature gradient are located at the corner, which makes these places the critical area in electro-migration. For the exit corner of the current, the directions of electron-flow and temperature gradient are opposite, which means the atom flux caused by these two factors are the same. Therefore, the current-flow exit place becomes the most critical area in the solder bump.

Since current density and temperature gradient are hard to measure by experimental methods due to a compact structure of BGA, most previous studies used FE analysis to estimate these two important factors in electro-migration. Results of simulations in [8] and [9] presented similar current density distributions as this section and their maximum density values are around 200 A/mm². Considering the SOHs of solder bumps in [8] and [9] are both 500 μ m while the SOH in this simulation is 200 μ m, the current density value of 430 A/mm² is reasonable. For the temperature gradient, it is highly dependent on the settings of environment. In this chapter, the coupled thermal-electrical process is supposed to be a steady state, which means temperatures of all the component and environment keeps steady during this period. Some experiment tests [11] and simulations [8] under steady state proved that the temperature gradient in a solder bump was over 200K/mm. Regarding the difference of environmental settings, the outcomes of this simulation are acceptable.

When a void due to electro-migration are formed at the interface of solder and copper trace, it expands to inside of the bump along the interface, which leads to a reduction of the contact area and electrical resistance. Therefore, in real application, resistance measurement is usually used to detect failure status of a solder bump. When electrical current applied on a solder bump keeps the same, the electrical potential difference between the two ports of the solder bump increases with its resistance. Hence, a distribution of *EPOT* in ABAQUS 6.14 is used to measure the potential difference of the model, as presented in **Fig. 6. 8**.

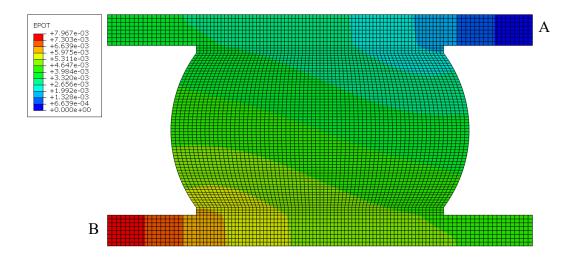


Fig. 6.8. FE-simulated distribution of the *EPOT* in Model I (unit: V)

In Model I, Port B was the electrical current entrance of the model and Port A was its exit. Therefore, Port A was the electrical ground connection and Port B was the high electrical-potential position. The potential difference between Ports A and C is 7.967 mV, according to **Fig. 6. 8**. This value is used to assess the increase of the electrical resistance of the solder bump in following simulations.

The current density and temperature distribution in Model II

In the Model II, the electrical current enters into the model from the left upper side to the right upper side. Since the electrical conductivity of copper is much higher than tin (see **Table 6.1**), the resistance of traces is much lower than solder bump. Consequently, a large part of the current-flow from entrance cross the copper pad while the current crossing the solder bump takes only a small proportion in total value. The current-flow path in Model I has been studied in many researches about electro-migration in solder bump as the current crossing solder bump arouses mass transportation directly. In this section, a coupled thermal-electrical process about Model II is analysed by FEA as a comparison to Model I.

A distribution of *ECD* vector in Model II is presented in **Fig. 6. 9**. Also, the copper traces are hided from this figure and effects of intermetallic compound (IMC) were not included in this model.

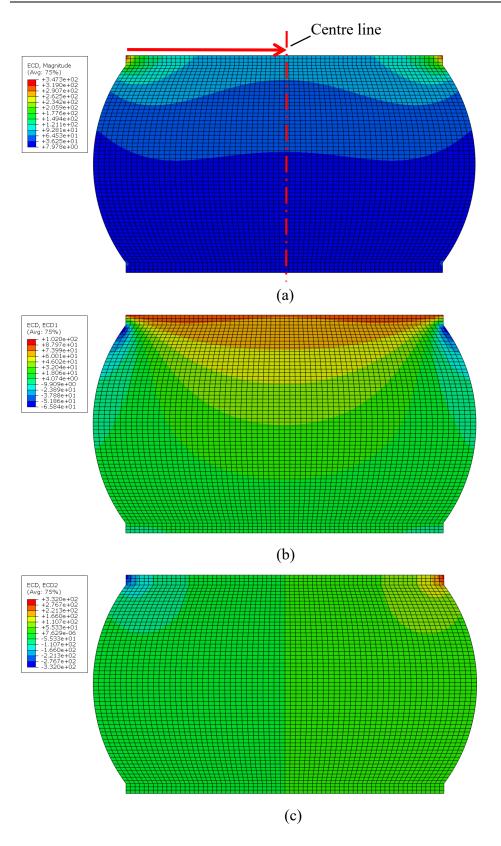


Fig. 6. 9. FE-simulated distribution of the *ECD* vector in Model II (unit: A/mm²): (a) vector magnitude; (b) vector component along X-axis; (c) vector component along Y-

axis

According to **Fig. 6. 9**, the distribution of the *ECD* vector is symmetric regarding to the centre line of the solder bump, as the electrical current loading was symmetric with regard to the line. It is worthy noticing that electrical current crowding is also found at the corners of the solder bump. The maximum magnitude of current density is 347.3 A/mm², which is only 20% less than the stressing current in Model I. This value of current density is stressing enough to arouse the electro-migration in this location. Furthermore, the maximum value of current density along Y-axis is three larger than the value along X-axis according to (b) and (c) in **Fig. 6. 9**. It indicates a direction change of current-flow at the corner of the bump. For a further investigation of current density distribution, components of the *ECD* vector along X-axis and Y-axis on the interface of the copper trace and the solder bump are plotted in **Fig. 6. 10**. Considering the symmetry of current density distribution, only a half of interface from the current entrance to the centre line was investigated here. The red line-arrow in **Fig. 6. 9** (a) illustrates the direction and position of the interface.

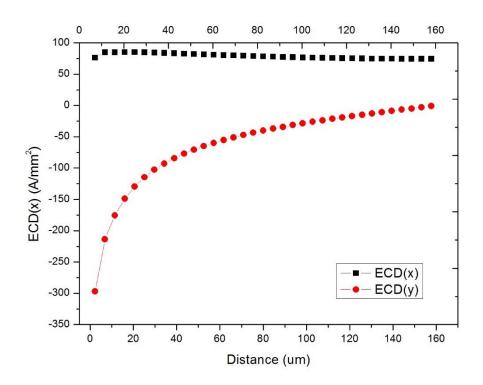


Fig. 6. 10. Components of the *ECD* vector along X-axis and Y-axis on the interface of the copper trace and the solder bump

In Fig. 6. 10, the minus sigh of ECD(y) represents the direction of Y-components of current density. From this figure, ECD(y) decreases rapidly from the location of the

current entrance. Meanwhile, ECD(x) keeps relatively steady along the interface. It indicates that some part of the current enters into the solder bump. The area between ECD(y) curves and x-axis in **Fig. 6. 10** represents the value of the current part that goes into the solder bump. It could be calculated that this part of electrical current takes 28.87 % of the total value based on this figure. Although this proportion is not large, current crowding was still found at the corners of the bump due to flow direction change. Therefore, attentions should be aroused for the electrical current-flow path as in Model II. Some further researches are required to understand the evolution progress of electromigration failure under this type of current loading.

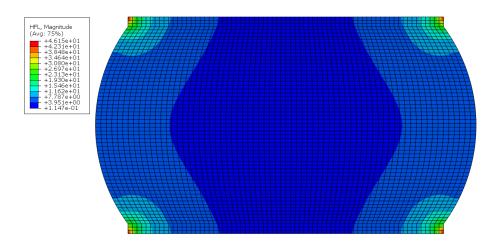


Fig. 6. 11. FE-simulated distribution of the *HFL* vector magnitude in Model II (unit: W/mm²)

For the temperature gradient of Model II, a distribution of the *HFL* is presented in **Fig. 6. 11**. According to this figure, the distribution is similar to the Model I; the maximum temperature gradient ∇T_{max} = 591.5 K/mm is very close to the value 591.4 K/mm in Model I. This results reveals that the temperature distribution in a solder bump is mainly affected by package structure and environment rather than current distribution in the solder bump. When the package temperature rises due to Joule heating of electrical current, structures and materials in the package determines the temperature distribution. As the solder bumps and traces are made of metals, their heat conducting abilities are much better than other parts of package. Hence, the temperature distribution in a solder bump shows a low sensitivity to electrical current loading types For a comparison of equivalent resistance in Model I, electrical potential between current entrance and exit are also illustrated, as **Fig. 6. 12**.

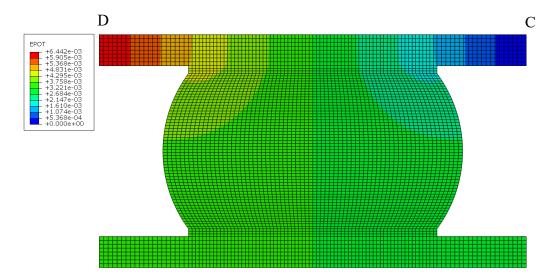


Fig. 6. 12. FE-simulated distribution of the *EPOT* in Model II (unit: V)

In Model II, Port D was the electrical current entrance of the model and Port C was its exit. Therefore, Port C was the electrical ground connection and Port D was the high electrical-potential position. According to the figure, the largest magnitude value of *EPOT* in Model II is 6.442 mV, which is 19.1% less than the highest value in Model I. It means that the equivalent electrical resistance of Model II is 19.1% less than Model I. This resistance difference resulted by current loading type should be paid enough attentions in package reliability assessment. A common criteria used in electrical industry for bump failure detection is that the increased electrical resistance of a bump reaches 15-20 % of its original value. Hence, the resistance difference due to current loading type may result in misunderstanding in failure assessment of a solder bump.

Distributions of current density and temperature in Model III

The models discussed in former two sections simulated the solder bumps in the BGA. In this section, the simulation results of a solder bump in TSV are discussed. In a typical TSV package, the direction of electrical current in copper traces was the same as solder bumps, which means the direction of electrical-current flow remained the same when it entered the solder bump from the copper trace.

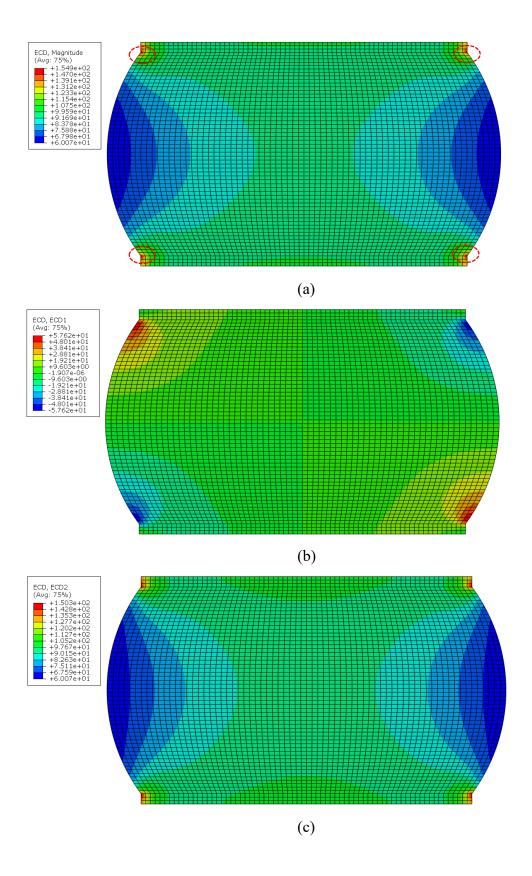


Fig. 6. 13. FE-simulated distribution of the *ECD* vector in Model III (unit: A/mm2): (a) vector magnitude; (b) vector component along X-axis; (c) vector component along

Y-axis 134 The distribution of *ECD* in Model III is presented in **Fig. 6. 13**. The electrical-current crowding is no longer located at the four corners. The maximum current density is distributed at the four structure corner of solder bump, as red circled in **Fig. 6. 13** (a). At these locations, the cross-section of current-flow appears a sudden change. Consequently, it leads to a change of flow direction. It could be seen from **Fig. 6. 13** (b) that the X-axis component of current density increases about 6 times to its average value at entrance. However, according to this figure, the maximum magnitude value of *ECD* in Model III is 154.9 A/mm², which is 64% less than that in Model I and 55.4% than in Model II. It indicates that the lever of current crowding in Model III is much less than Model I and II, which means The solder bumps in TSV show more resistivity of electromigration than in BGA. Besides, since the current crowding in TSV is mainly affected by cross-section change of the bump, some controlling method of bump shape could be used in package design to reduce the electro-migration effect.

For temperature gradient in Model III, its distribution of the *HFL* vector magnitude is presented in **Fig. 6. 14**. The larger values of the vector were located at the four corners of the solder ball. The highest value of temperature gradient could be calculated from Equation 6-5: $\nabla T_{max} = 742.6$ K/mm. This value is 25.5% larger than the maximum value of temperature gradient in Model I.

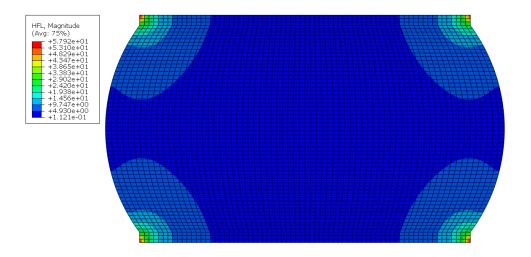


Fig. 6. 14. FE-simulated distribution of the *HFL* vector magnitude in Model III (unit: W/mm²)

It is worthy noticing that the maximum temperature gradient in Model III is larger than Model I while its maximum current density is lower than Model I. A similar phenomenon was also found in Model II: the distribution of its temperature gradient is nearly the same as Model I while its current density is different from Model I. Therefore, it is further confirmed that the distribution of temperature is affected by structure and environment rather than current density. Although the heat boundary conditions in Model III were set the same as Model I, its model structure is different from Model I. Accordingly, the distribution of temperature gradient in Model III shows inconsistency to Model I and II. On the other hand, larger applied current on solder bumps, which usually causes larger current density, results in more Joule heating in the package. It may cause a different temperature gradient distribution in a bump. However, this difference is triggered by environmental temperature change rather than current density directly. Based on these discussions, heat dissipation of an electronic package is a key method to control the thermo-migration in solder bumps.

The electrical potential distribution in Model III is presented in **Fig. 6. 15**. Port F is the electrical current entrance of the model and Port E is the exit. The potential difference between Ports E and F is 2.941 mV. The equivalent resistance of the Model III was 54% less than that of Model II and 63.2% less than in Model I. It indicates that the current of solder bumps in TSV will be larger than those in BGA when the applied electrical potentials are the same, which may arouse some reliability issues.

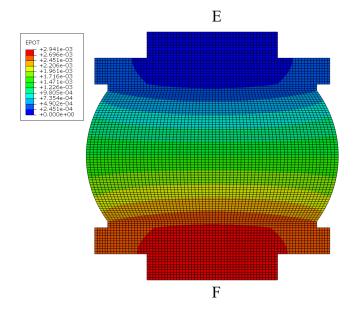


Fig. 6. 15. FE-simulated distribution of the *EPOT* magnitude in Model III (unit: V)

6.3 Formation and evolution of void/crack under electro-migration

It is widely known that electro-migration is a current-controlled mass-diffusion process. The rate of electro-migration is highly dependent on values of electrical current density. Besides, electro-migration also results in thermos-migration and stress-migration in a solder bump. Atom flux caused by these migration processes in solder bump leads to transportation of atoms and void formation. In this section, governing equations of the atom flux are used to calculate its values in a solder bump based on the results of Section 6.2. Then, a calculation algorithm is developed to simulate formation and evolution of voids or cracks during the electro-migration process. The obtained results could be used to estimate a service life of solder bumps under electro-migration.

6.3.1 Numerical description and failure criteria of electro-migration in solder bump

Generally, a mathematical model describing electro-migration process includes three subparts: electro-migration, thermo-migration and stress-migration. In this model, metal atoms diffuse from one void in a crystal lattice to another. Therefore, flux density of voids is used to describe the diffusion here.

For electro-migration, metal atoms experience two types of forces under the effect of current. One is caused by electric field, which is also the propelling force of current carriers. This force is called *electric field force*. Another is resulted by a momentum exchange between carriers and mental atoms since charged carriers move to form electrical current. This force is called *electron wind force*. Directions of these two forces are opposite. However, both of them could be expressed as a function of electron charge, e. Hence, the migration flux density of electro-migration is expressed as:

$$\vec{J}_{EM} = \frac{N}{kT} e Z^* \vec{j} \rho D_0 \exp\left(-\frac{E_A}{kT}\right) , \qquad (6-6)$$

where N is the atomic density, Z^* is the effective charge number, \vec{j} is the vector of 137

electrical density, ρ is temperature-depended resistivity, D_0 is the materials selfdiffusion coefficient, k is the Boltzmann constant, T is the absolute temperature, E_A is the activation energy.

For thermo-migration, a temperature distribution is not uniform under a high value of electrical-current density, resulting a temperature gradient. The temperature gradient is regarded as a propelling force of atom movement. The migration flux density of thermos-migration is as:

$$\vec{J}_{TH} = -\frac{NQ^*D_0}{kT^2} \exp\left(-\frac{E_A}{kT}\right) \nabla T \quad , \tag{6-7}$$

where Q^* is the molar heat flux, $Q^* = \beta H_m - H_f$, H_m and H_f represents molar enthalpy of voids migration of forming.

For stress-migration, parts of material expand or shrink under high temperature and high temperature density. However, an extent of expansion or shrinkage is not the same due to different coefficients of thermal expansion and uneven temperature gradients. This results in thermal stress gradients in a material. Thermal stress gradient propels the formation and propagation of micro voids, when it reaches a threshold value. Massdiffusion triggered by thermal stress gradient is described as follows:

$$\vec{J}_s = \frac{N\Omega D_0}{kT} \exp\left(-\frac{E_A}{kT}\right) \text{grad } \sigma_M$$
, (6-8)

where σ_M is the hydrostatic stress, $\sigma_M = \frac{\sigma_{xx} + \sigma_{yy} + \sigma_{zz}}{3}$, σ_{xx} , σ_{yy} and σ_{zz} represent stress values of three principle directions. In the simulations of this stage, mechanical loads and respective material behaviours are not included. Therefore, there is no stress distribution in the model and stress-migration is not taken into consideration.

Considering all mentioned above, the total flux density of electro-migration could be expressed as:

$$\vec{J}_{Total} = \vec{J}_{EM} + \vec{J}_{TH} = \frac{N}{kT} eZ^* \vec{j} \rho D_0 \exp\left(-\frac{E_A}{kT}\right) - \frac{NQ^* D_0}{kT^2} \exp\left(-\frac{E_A}{kT}\right) \nabla T$$
$$= \frac{ND}{kT} \left[eZ^* \rho \vec{j} - Q^* \frac{\nabla T}{T} \right] , \qquad (6-9)$$

where D is expressed as,

$$D = D_0 \exp\left(-\frac{E_A}{kT}\right) \ . \tag{6-10}$$

This is the constitutive equation describing electro-migration process, which is used in simulations. Notice D_0 is a constant coefficient and D is a temperature-dependent parameter. According to Equation 6-9, the total migration flux density could be further expressed as

$$\vec{J}_{Total} = Nf(T, \vec{j}, \nabla T) \quad , \tag{6-11}$$

Where $f(T, \vec{j}, \nabla T) = D(kT)^{-1}eZ^*\rho \vec{j} - D(kT^2)^{-1}Q^*\nabla T$. The time dependent evolution of the local atomic concentration is given based on the mass diffusion equation, as:

$$\operatorname{div}(\vec{J}_{Total}) + \frac{\partial N}{\partial t} = 0 \quad . \tag{6-12}$$

From Equation 6 - 11, the flux density value is proportional to the atomic concentration N and to the function f in which different physical parameters are included. So Equation 6 - 12 is equivalent to the following equation:

$$NF + \frac{\partial N}{\partial t} = 0$$
 , (6-13)

where $F = \operatorname{div}(f)$. Integrating Equation 6 - 13 in a time increment, it can be obtained that

$$\int_{N_{i}}^{N_{i+1}} \frac{dN}{N} = -\int_{t_{i}}^{t_{i+1}} F dt \quad , \qquad (6-14)$$

where N_i and t_i are the atom concentration and time at the beginning of the time increment; N_{i+1} and t_{i+1} are the respective parameters at the end of the time increment. With the explicit Euler algorithm, Equation 6 - 14 could be simplified as

$$\frac{N_{i+1}}{N_i} = e^{-F_i \Delta t_i} \quad , \tag{6-15}$$

where F_i is the value of function F during the time increment and Δt_i is the length of the time increment. Assuming the failure in one element resulted by migration process at the end of the *m*th time increment, multiplying all the equations of each time increment, it could be obtained that

$$\frac{N_m}{N_{m-1}} \times \frac{N_{m-1}}{N_{m-2}} \cdots \times \frac{N_{i+1}}{N_i} \cdots \times \frac{N_2}{N_1} \times \frac{N_1}{N_0} = e^{-(F_m \Delta t_m + F_{m-1} \Delta t_{m-1} \cdots + F_i \Delta t_i \cdots + F_1 \Delta t_1 + F_0 \Delta t_0)} \quad (6-16)$$

If the model structure and boundary conditions do not change, the distribution of electrical-thermal results remains the same. This means that the function F is the same before failure occurs in one element. Therefore, equation 6 - 16 could be simplified as

$$\frac{N_m}{N_0} = e^{-F_j t}$$
 , (6-17)

where N_m is the atom concentration of the element at the failure due to migration; N_0 is the initial atom concentration; F_j is the value of the function F before the failure and t is the time from the beginning of the migration process to the failure occurrence.

When the ratio of atom concentration in an element to its initial value reaches a certain number, the failure is considered to occur and the element is removed from the model. Hence, a void is formed at the location of this element. This value of atom concentration is called *failure criterion*. A widely accepted failure criterion of atom concentration is between 10 % and 20 % [7]. In this simulation, it was set at 10%. Based on this criteria, when $F_i t$ was equal to 2.3, a void was formed at the corresponding element.

The simulation of crack formation and expansion are based on element removal and thermal-electrical field reconstruction. Before the removal of elements, the distribution of current density (\vec{j}) and temperature gradient (∇T) can be obtained by the analysis in Section 6.2. After a period of time, atom concentration in some elements decreases to 10 % of its original value, and these elements are removed from the model. Due to the removal of these elements, the structure of the model changes and the distribution of thermal-electrical field also changes. Therefore, the model with new structure should be analysed again to determine the new distribution of \vec{j} and ∇T . The whole process is repeated till the electrical resistance of solder bumps reaches 115 % of its original value. The flow chart of void formation and crack expansion is presented in **Fig. 6. 16**. All the constants used in the numerical model form [8] are listed in **Table 6. 3**.

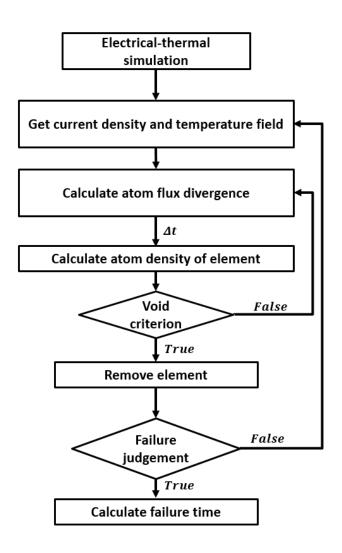


Fig. 6. 16. Flow chart of void formation and crack expansion simulation

Constant	Z^*	Q^*	D_0	E_A
Value	-23	0.0094 eV	0.027 m/s ²	1.0 eV

 Table 6. 3. Constants used in the numerical model [8]

6.3.2 Voids formation and crack expansion caused by electro-migration

In this section, Model I was used to simulate the voids formation and crack expansion as its current loading type is a common one. According to the results of Section 6.2, the largest values of *ECD* and *HFL* were both located at the right upper corner of the solder bump. Therefore, the largest atom flux could be found at the element located in the right upper corner. Once a void is formed at this element, the element adjacent to the first element become the potential voids. Therefore, the elements located at the right upper area the solder bump should be investigated in details. The enlarged view of the elements and their numbers generated by ABAQUS 6.14 are presented in **Fig. 6. 17**.

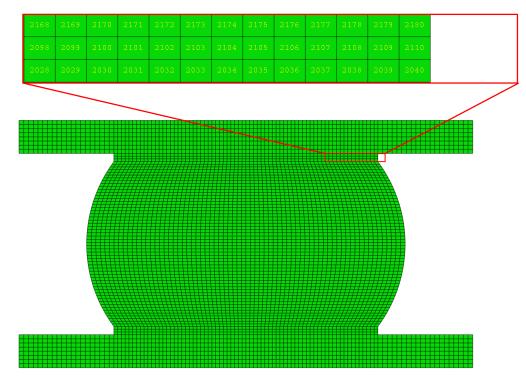


Fig. 6. 17. Enlarged view of elements located at the right upper area of Model I and their numbers generated by ABAQUS 6.14

Accordingly, Element 2180 is the first failure element due to the largest atom flux in it.

After its removal, the new distribution of *ECD* and *HFL* in the solder bump are showed in **Fig. 6. 18**. It could be seen from **Fig. 6. 18** that the current density increases significantly when Element 2180 is removed from the model. The maximum value in this figure is 575.6 A/mm² and is located in Element 2179 which is next to Element 2180. According these results, once a void is formed at the upper corner of the bump, the current crowding increases significantly and the area adjacent to the formed void becomes a critical location.

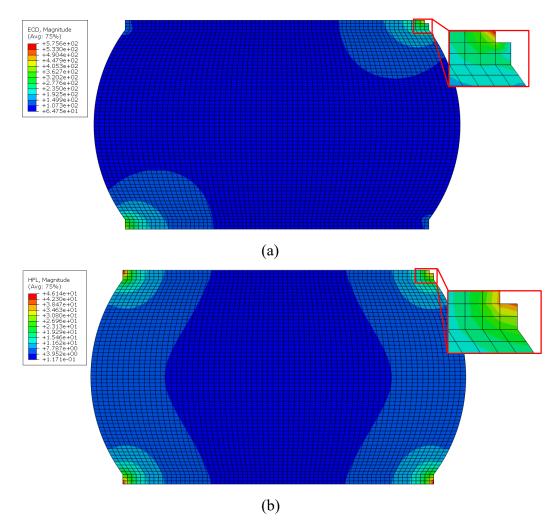


Fig. 6. 18. Distribution of thermal-electrical results in Model I after the removal of Element 2180: (a) *ECD* vector magnitude; (b) *HFL* vector magnitude

According to the distribution of *HFL*, large temperature gradient is located in both Element 2179 and 2110. However, based on the calculation of div \vec{J}_{TH} and div \vec{J}_{EM} , the atom flux caused electro-migration is about three orders higher than the one caused by thermos-migration. Some simulation results in [8] and [9] also support this

conclusion. Therefore, a new void is formed at Element 2179 rather than Element 2110. Following this evolution trend, a crack will expand along the interface of the solder bump and the copper pad, as illustrated in **Fig. 6. 19**.

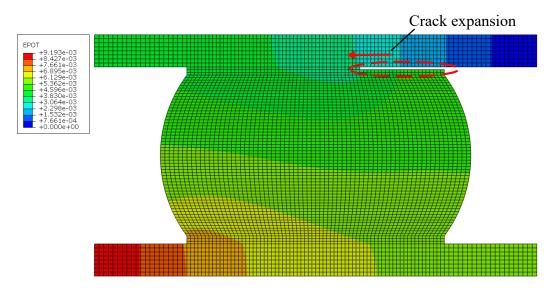


Fig. 6. 19. Crack expansion in solder bump and the distribution of electrical potential at failure time

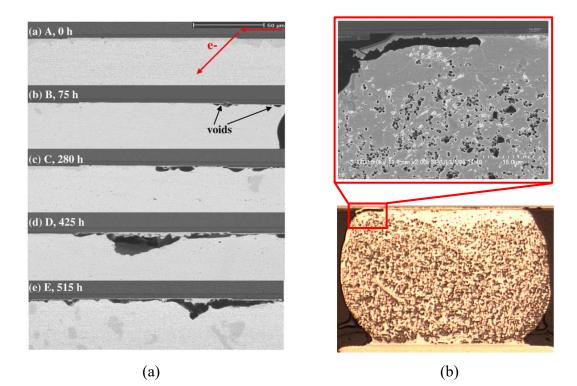


Fig. 6. 20. Cross-sections of SnAgCu solder bumps under electro-migration based on experiments: (a) Morphological evolution in Sn3.5Ag1.0Cu solder joints under a current density of 1.5 × 10⁴ A/cm² at 125 °C [12]; (b) Cross-section of the 0.3 mm diameter solder ball at 1500 h [13]

To validate the simulation results of crack propagation under electro-migration, some experimental pictures based on previous researches are presented in **Fig. 6. 20**. Both of the solder bumps in **Fig. 6. 20** are made of SnAgCu solder material. The contact area of solder bump and copper pad is a flat surface, which is the same as the condition of this simulation. Both of the experimental results in these literatures shows similar voids shape to simulation results. **Fig. 6. 20** (a) also illustrates the crack propagation process. The initial voids occurred at the entrance of electrical current, where is the current crowding location according to the simulation. Then the voids expanded along the interface of trace and solder bump gradually, resulting in a separation of pad and solder. Compared with experimental pictures, the prediction of void expansion shape in this simulation is reasonable. The expansion times from simulation and some experiment-based literature will be discussed in following discussions

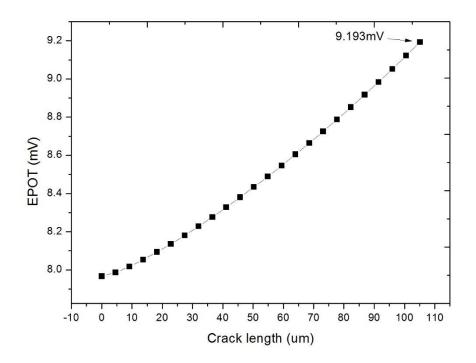


Fig. 6. 21. Relationship of electrical potential and crank length in the model

For failure assessment of solder bumps, a widely accepted industrial standard about electronic-package service lifespan is that the increasing electrical resistivity reaches 15% of the original value. In this simulation, as the electrical current loading on the model is a constant value, the failure was considered to occur when the value of *EPOT* reached over 115% of its initial value according to the standard. The distribution of the

electrical potential in the model when the failure occurred are presented in **Fig. 6. 19**. When failure occurred in the solder bump, its electrical potential increased from 7.967 mV to 9.193 mV while 23 elements (Element 2158-2180) were removed. A relationship between electrical potential and crack length is illustrated in **Fig. 6. 21**. From this figure, during the propagation of crack, the electrical resistance increases with the crack length. Also, the increasing speed of the resistance grows when the crank propagates. The changing trend indicates that the crack propagation due to electro-migration is a continuous propelling process. Once a void is formed in the solder bump, its transformation into a crack and propagation is fast increasingly. When the *EPOT* of the solder bump reaches the 9.193 mV, which is 115.4% of its initial value, the crank length reaches around 105 μ m. This is the failure state of the solder bump under electro-migration in this simulation.

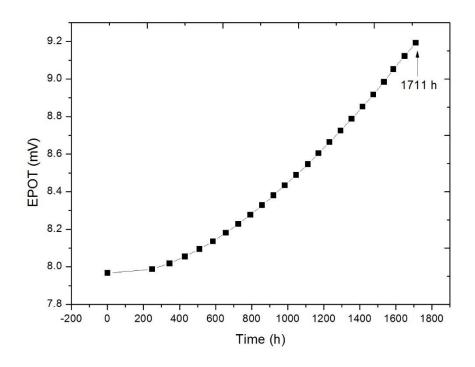


Fig. 6. 22. Relationship between electrical potential and migration time in the model

To estimated failure time of the model, following steps were adopted. Calculate the failure time of 1st element (Element 2180) as Δt_1 and record the atom concentrations in the rest 22 elements; Remove the failure element and re-analyse thermal-electrical distribution of the new structure; Calculate the failure time of 2nd element (Element 2179) from the atom concentration in 1st step to failure as Δt_2 , meanwhile, record the

atom concentration in the rest 21 elements. Repeat these steps for all elements and add the failure times of each element (Δt_1 to Δt_{23}) to obtain the total failure time.

The relationship between the electrical resistivity and the migration time is presented in Fig. 6. 22. The total time from the beginning of void formation to the failure of the model bump is 1711 h. The starting time of void formation is 248.4 h s of electromigration process. According to the figure, once the void was formed in the solder bump, its expansion speed increases with the crack evolution. So far, there was rare experiment-based report of the failure time of electro-migration under a normal-use condition, as the SnAgCu solder material presents a relative high resistance to electromigration and its failure time is quite long. Based on results from a previous simulation [8], the failure time of a SnAgCu solder bump is 1475 h. The current density applied on the solder bump in [8] was close to the simulation in this chapter, however, its environmental temperature was around 140 °C, which is 20 K higher than settings in this simulation. Although it was proved that the atom flux resulted by thermo-migration can be neglected compared with electro-migration, a higher temperature causes a higher diffusion coefficient in Equation 6-6, which results in higher atom flux. Therefore, a shorter service life is expected under higher temperature and the life prediction of solder bumps under electro-migration generating by this chapter is reasonable.

6.4 Summary and conclusions

In this chapter, FE models of single solder bumps with different current loading types were built. Their thermal and electrical performances under electrical current loading were presented and discussed. An algorithm to simulate formation and evolution of voids based on the FE results was developed. From the presented results and discussions, it could be concluded that:

 In solder bumps of the BGA package, some electrical currents change their directions when they enter bumps from copper traces. This results in severe electrical current crowding at the corners connecting the copper trace and the solder bump.

- 2. Electrical-current crowding can be found at the changing cross-section in a solder bump of TSV package. However, the level of current crowding is much lower than that in the bumps in BGA. The solder bumps in TSV shows a higher service lifespan than the bumps in BGA under electro-migration.
- 3. The distribution of temperature in a solder bump is affected more by environmental temperature rather than by the electrical current. The difference of temperature in the solder bump could be neglected while its gradient is relatively high due to the size of solder bumps.
- 4. The atom flux caused by thermo-gradient migration is much lower than that caused by current-migration, which means it could be neglected during the migration process.
- 5. Electrical current crowding became more severe with the process. Once the void was formed in the solder bump, its expansion speed increases with its evolution.

Reference

- Yang D., "Study on reliability of flip chip solder interconnects for high current density packaging", Doctor of philosophy thesis. Hong Kong: City University of Hong Kong; 2008
- [2] Wu B. Y., Alam M. O., Chan Y. C., Zhong H. W., "Joule heating enhanced phase coarsening in the Sn37Pb and Sn3.5Ag0.5Cu solder joints during current stressing", Journal of Electronic Materials, 37(2008), pp. 469–76.
- [3] Liu Y., Liang L., "3D Modeling of electromigration combined with thermalmechanical effect for IC device and package", *Microelectronics Reliability*, 48 (2008), pp.811–824.
- [4] Wang T., Lai Y., Wu J., "Effect of underfill thermomechanical properties on thermal cycling fatigue reliability of flip-chip ball grid array", ASME Journal of Electronic Packaging, vol. 126(2005), pp. 560-564.
- [5] Pak J., Pathak M., Lim S. K. and Pan D. Z. "Modeling of Electromigration in Through-Silicon-Via Based 3D IC", *Electronic Components and Technology Conference (2011)*.
- [6] Gong J. C., Liu C., et al., "Micromechanical modelling of SnAgCu solder joint under cyclic loading: Effect of grain orientation", *Computational Materials Science 39 (2007)*, pp. 187–197.
- [7] Jing J. P., Liang L., Meng G., "Electromigration Simulation for Metal Lines", *Journal of Electronic Packaging*, vol. 132 (2010), 011002.
- [8] Liu Y., Liang L., Irving S., Luk T., "3D Modelling of electromigration combined with thermal–mechanical effect for IC device and package", *Microelectronics Reliability*, 2008, 48(6), pp. 811-824.
- [9] Liang S. W., Chang Y. W., Shao T. L., "Effect of three-dimensional current and temperature distributions on void formation and propagation in flip-chip solder joints", *Applied Physics Letter 2006*;89(2):021117
- [10]Black J.R., "Mass Transport of Aluminum by Momentum Exchange with Conduction Electrons", Proc. Int. Reliability Physics Symposium, 1967, pp. 148-159.
- [11]Hsiao HY, Chen C. Thermomigration in flip-chip SnPb solder joints under alternating current stressing. Appl Phys Lett 2007;90:152105.
- [12] Yang D., "Study on reliability of flip chip solder interconnects for high current

density packaging", Doctor of philosophy thesis. Hong Kong: City University of Hong Kong; 2008.

[13]Gee S, Kelkar N, Huang J, Tu KN. "Lead-free and PbSn bump electromigration testing", I Proc. Int. PACK 2005, IPACK2005-73417, July 17–22

Chapter 7. Joint effects of thermal fatigue and electromigration on solder bumps

7.1 Introduction

In service of electronic packages, electrical currents go through solder bumps with alternating power-on and off state, resulting in warming up and cooling down of packages. This reliability issue was discussed in Chapter 5. Also, electrical-currents result in atom migration in solder bumps, inducing voids formation, as analysed in Chapter 6. However, these two reliability issues are not two isolated processes. They are both caused by electrical current and occur at the same time; therefore, their effects on service life of packaging are influenced by each other.

In Chapter 5, it was proved that the fatigue life of solder bumps was determined by the largest accumulated equivalent creep strain (CEEQ) and plastic strain (PEEQ). According to the conclusions in Chapter 5, large values of CEEQ and PEEQ are normally located at the area of stress concentration. Stress concentration in a solder bump is usually determined by its microstructure and external conditions. If microstructure of a solder bump changes, its internal stress is redistributed and stress concentrator will relocate. Under effect of electro-migration, transformation of metal atoms in solder bumps causes formation of voids and crack expansion at cathode side, which is a critical area for both mechanical and electronic loadings. Hence, microstructure of solder bumps is changed due to electro-migration. Therefore, distributions of CEEQ and PEEQ are also changed during progress of electro-migration and thermal fatigue, affecting predictions of thermal-fatigue cycles for the packaging. Previous research studies on thermal fatigue life prediction usually focused on solder bumps with fixed microstructures [1] [2]. This method tended to overestimate thermal-fatigue life, caused by alternating electrical current in solder bumps. Hence, thermal-fatigue life, caused by alternating electrical current in solder bumps.

fatigue estimation for solder bumps should take changing micro structures into consideration. In this chapter, changes in micro-structures particularly refer to void formation and crack expansion caused by electro-migration.

This chapter proposes a FE-based scheme to predict the fatigue life of 96.5Sn–3.5Ag (lead-free SAC305) solder bumps for FC-PBGA packages under effects of electromigration. The proposed analysis procedure incorporates the concepts of voids formation and continuous damage accumulation. The void is assumed to form as a result of electro-migration and expand progressively together with thermal cycles, and with the shape predicted by the algorithm proposed in Chapter 6. The thermal fatigue-life for voids of certain shape is predicted with the method discussed in Chapter 5. Considering that the void expands with electro-migration and thermal cycles, the fatigue damage at each thermal cycle caused by electro-migration could be evaluated using a linear damage rule. The final fatigue life of the solder ball can be obtained when the accumulated damage reaches unity.

7.2 Analysis procedure

7.2.1 Method to calculate thermal-fatigue life of solder bump under electromigration

To incorporate the concepts of void formation and crack expansion with electromigration and continuous damage accumulation at the critical solder bump in the reliability analysis, this study proposes a scheme (see it in **Fig. 7. 1**) to determine the thermal-fatigue life of solder bumps in BGA with the void-expansion effects.

The texts listed in the left-hand column of **Fig. 7. 1** are related to mechanical simulations presented in Chapter 5. However, in Chapter 5, thermal cycling loads of the package were caused by external environment. Since it was necessary to estimate the thermal fatigue life of electronic packages under harsh conditions, the range of

environmental temperature was much larger than that of the normal use of electronics. In this chapter, the external temperature is set as in the normal environment. Therefore, a thermal-mechanical and a thermal-electrical coupling model were used for this part of simulation. The right-hand column in **Fig. 7.1** is also different from the discussion in Chapter 6 as thermal stress was induced in this chapter. Hence, the stress-migration component mentioned in Equations 6-8 and 6-9 should be included in the simulation of this chapter.

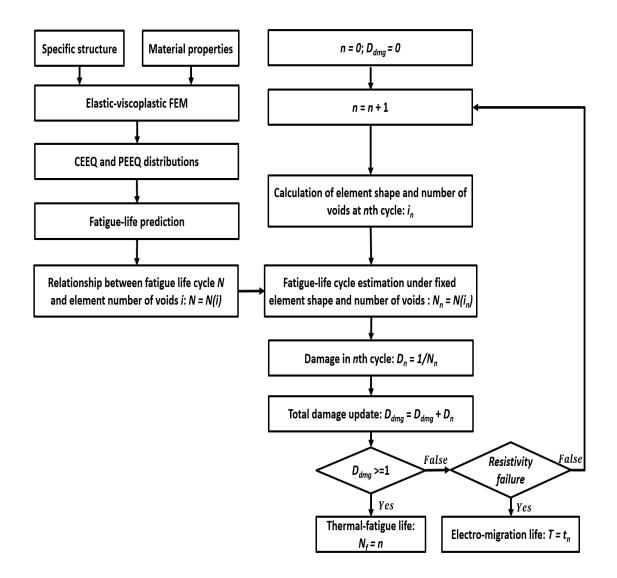


Fig. 7. 1. Flow chart of assessment of thermal-fatigue life for solder bumps in BGA void formation and crack expansion

In thermal-mechanical FE analysis of ABAQUS, only a model with a certain structure

can be built and calculated. It is hard to simulate a transient process while a model structure is also changing. Therefore, in order to estimate the fatigue time with crack expansion, a damage indicator D_{dmg} , as illustrated in **Fig. 7. 1**, was used to record accumulated damage of the critical bump in each damage. According to previous studies and the simulation in Chapter 5, inelastic strain accumulated in each cycle kept steady after the 3rd thermal cycle. It can be assumed that the fatigue damage accumulated in each cycle are same. For a certain structure, each cycle contributes $1/N_n$ of the total fatigue damage in thermal cycling. When the model undergoes m cycles before it changes to a new structure, fatigue damage accumulated in the former structure is recorded as m/N_n . This step can be repeated in the new structure of the model until its next one. Then add all the fatigue damage for each structure of the model; if the sum of the damages reaches unit I, final thermal fatigue occurs.

In simulations of this chapter, structure changes were induced by crack propagation which was caused by electro-migration. Effects of cracks on thermal fatigue is presented and discussed in this chapter. Also, fatigue life will be compared with electromigration life to determine which failure mechanism occurs first.

7.2.2 Model description and loading conditions

According to the method presented in **Fig. 7. 1**, simulations of joint effects could be achieved employing a global model and a sub-model. The global FE model simulates the thermal-mechanical behaviour of the BGA package. A 2-D plain strain model of a typical BGA structure as in Chapter 5 was employed, including four components: a reading chip, a substrate, a solder bump and a underfill. Considering the model symmetry, only half of the model was built and analysed to reduce the calculation cost. **Fig. 7. 2** presents the model of package and some solder bumps with their FE mesh. To simplify the model, effects of intermetallic compounds were not considered in this simulation.

The results of Chapter 5 proved that the solder bump located at the outmost of packaging experienced the largest strain and stress under thermal cycling. Furthermore, the highest values of CEEQ and PEEQ were located at the right upper corner in the

solder bump, making this area the most critical part in the package. Based on these results, the solder bump located at the edge of BGA is assumed to be the most important object for the analysis. Hence, the outmost solder bump was finely meshed, as in **Fig. 7. 2**. To cooperate with thermal-electrical modelling in following steps, the mesh density in the outmost solder bum were the same as the Model I in Chapter 6, which contains 4270 elements in total.

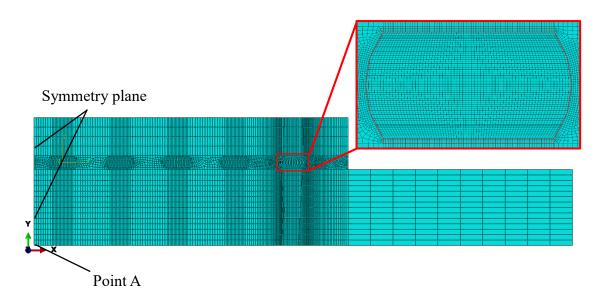


Fig. 7. 2. Global FE model of the package and local solder bumps with mesh

The outmost solder bump was supposed to be a sub-model of the global model. Thermal-electrical analysis together with simulation of voids formation and crack expansion was applied to the sub-model in the subsequent simulation process.

For boundary conditions, plane YOZ was assumed to be a symmetric plane. The global package is supposed to be fixed on a printed circuit board (PCB). Therefore, a centre of the global model, i.e. point A in **Fig. 7. 2**, is a neutral point which was set as a fixed point in the finite-element model. To simplify the model, connections of substrate/array and array/reading chip were set as ideal bonding, which means there was no horizontal or vertical relative movement between their contacting surfaces.

The global model was supposed to experience a thermal-cycling heating condition. Some previous research studies reported that the temperature gradient in the flip-chip packages was so small that can be neglected [3]. Hence, temperature of all the parts in this model was set to be uniform when temperature fluctuated. In Chapter 5, thermal cycling range was from the lowest -40 °C to the highest 125 °C. This temperature range is usually employed for an accelerated thermal-cycling test (ACTC), and is much larger than that for the normal use of electronic devices. In this chapter, another thermal cycling load simulating a daily use of electronic packages was adopted. The temperature applied on the FE model rose from room temperature (25 °C) to the highest level (120 °C). This region represents the process of switching-on of an electronic packaging and takes around 180 s. Then the temperature at the highest level lasts for 300 s and decreases gradually to room temperature in 600 s. After that, it is kept at room level for 120 s and then enters into next cycle. One single cycle lasts for 1200 s. The whole process modelled with FEM lasted 3600 seconds and covered 3 cycles, as presented in **Fig. 7. 3**.

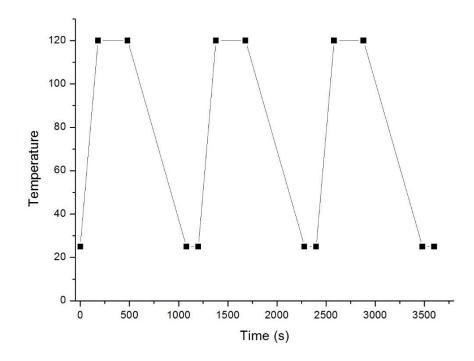


Fig. 7. 3. Thermal cyclic load in the FE model (Temperature in °C)

According to the simulations presented in Chapter 5, the existence of IMCs at the interface of the solder bump and chip/substrate increased the calculation cost significantly. Since the simulation in this chapter focused on the joint effects of electromigration and thermal fatigue on solder, an IMC layer was not included in the model of this chapter.

In working state, all the bumps in the package may experience electrical current loading. Since the outmost bump is the most critical one in thermal-cycling, its reliability under current loading should be analysed. Hence, a sub-model of the outmost solder bump is used to analyse thermal-electrical distribution. Based on the algorithm proposed in Chapter 6, results of thermal-electrical analysis can be used to calculate the service life of electronic packages under effects of electro-migration. The geometry and loading condition of sub-model is the same as Model I in Chapter 6, as presented in **Fig. 7. 4**. Since the mesh of the outmost bump in global model adopts the density used in Chapter 6, a consistency of mesh in global model and sub-model shows convenience in data exchange.

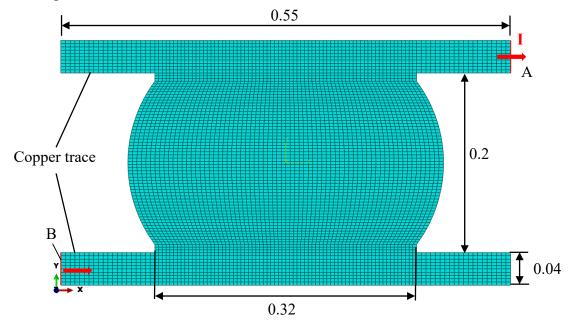


Fig. 7. 4. The geometry and loading condition of the sub-model

Thermal-electrical simulation in Chapter 6 described a steady state. Meanwhile, thermal-mechanical simulation in Chapter 5 were a time-transient process. In order to combine these two simulations, some assumptions need to be proposed to define the thermal boundary conditions of the sub-model. The first one is that the electro-migration mainly occurs in high-temperature-dwell of thermal cycling. When electrical current is applied on components, the package is heated up by Joule heating. Compared to the final steady working state, the time of heating is short and electro-migration in this period can be neglected. When the electrical current is cut off, the temperature decreases and electro-migration stops. Hence, the electro-migration is assumed to be a steady process in high-temperature-dwell of thermal cycling. The second assumption is

that the temperature gradient cannot be neglected in the sub-model while the temperature was set as a constant value in global model. Based on simulations in [8], the temperature range in a BGA package is 1.4 K. The mechanical properties of materials used in electronic package changes very little under such a small temperature range. However, the temperature gradient in a solder bump is very large due the microstructure of package, especially to electro-migration. Hence, in thermal-electrical simulation, temperature gradient need to be considered. Based on these assumptions, the boundary conditions of this model were set the same as Chapter 6.

7.2.3 Material properties

The global model underwent a fully coupled thermal-displacement process. Basic material properties including the elastic modulus, the Poisson's ratio and CTE should be taken into consideration. Some inelastic mechanical properties such as creep and plastic parameters were also needed. As IMC layer was not included in this model, there are three materials: silicon (chip), BT (substrate) and SAC305 (solder). All the related material properties were discussed in Section 5.2.2 of Chapter 5, and presented in Tables 5. 1, 5. 2, 5. 3 and Fig. 5. 5. All the mechanical properties adopted are listed in Table 7.1.

The sub-model experiences a fully coupled thermal-electrical process. Only metal parts in the package were included into this simulation. Thermal and electrical material properties, including thermal and electrical conductivity, should be taken into consideration. The simulated model contains 2 materials: copper (trace) and SAC305 (solder). The relevant properties of these materials are listed in **Table 7. 2**.

Propertires	Density (tone/mm³)	Thermal Conductivity (mW/mm-K)	Electrical Conductivity (/mΩ-mm)		
Copper	8.94e-9	386.2	58.8		
SAC305	7.4e-9	78	8.12		

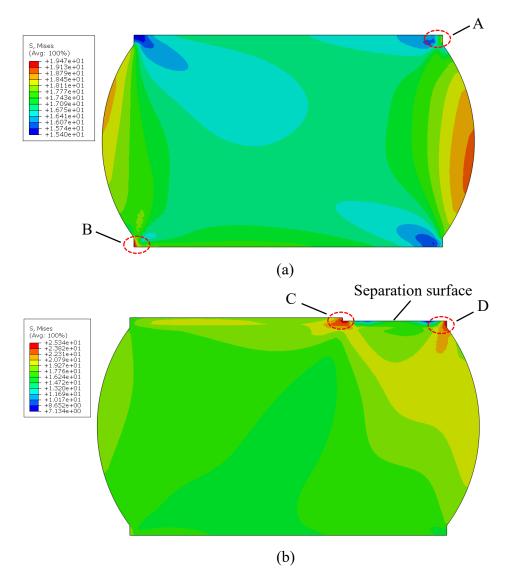
Table 7. 2. Mechanical properties of silicon, BT, SAC305 and underfill in the global
model [4 , 5]

Silicon (chip)												
Tomporatur	o/°C	Elastic				hermal E						
Temperatur	e/ L	Pois	son's Ratic	Elastic I		stic M	odulus/MPa		Coe	efficient of Expansion		
-40			0.278		192100				1.5e	-6		
25					191000				2.6e	-6		
50					190600				2.8e	-6		
125					190000			3.1e-6				
BT (substrate)												
					lastic				Thermal Expansion			
		Pois	son's Ratic)	Ela	stic M	[odulus	/MPa	Coe	Coefficient of Expansion		
			0.39		26000		1.5e-5					
SAC305 (solder)												
Temperature/°C		Elastic					Thermal Expansion					
Temperatur	e/ L	Pois	son's Ratic)	Ela	stic M	[odulus	/MPa	Coefficient of Expansion			
-40		57			7392							
25	25		0.4		47662			2.25e-5				
50	50				43919							
125						-	2692					
	Creep (hyperbolic-sine)											
Power L	aw		erbolic		Equivalent		Activation		Universal			
Multipli	ier		Aultiplier	Stress Order		Energy			Gas Constant			
7.01		0	.081		5.5 48364.2		8.31					
Compound polymer (underfill)												
	Visco-elastic											
E_0 (MPa)	a) E_{∞} (MPa) K_1 τ_1 (s) K_2 τ_2 (s)		$ au_2$ (s)		K_3	$ au_3$ (s)						
5630	13	300	0.264	0.	0.2 451		451		0.536	30435		

7.3 Results and discussions

7.3.1 Distribution of stress/strain in global model under effects of void formation and crack propagation

According to the results in Chapter 6, some elements are removed to simulate voids formation and crack propagation due to electro-migration. Hence, the model with and without the crack in the outmost solder bump were presented and compared in this section. The residual stress distribution in the outmost bump with/without crack are presented in **Fig. 7. 5**. Here, the length of crack was the same as the one at the failure



time of electro-migration, which was around 105 µm in total.

Fig. 7. 5. Distribution of residual stresses in outmost joint after thermal cycling (t = 3600 s): (a) bump without void; (b) bump with failure occurrence due to electromigration

Thermal cycling loading in this simulation was set closing to normal use of electronic packages. Therefore, the fluctuation range of temperature was much smaller than Chapter 5, and it did not include low-temperature period. Hence, the package only experienced only concave-up deformation. Moreover, due to the creep and plastic properties of Sn under high temperature, the stress concentration in solder bump was relaxed. Notice that the stress range in **Fig. 7. 5** (a) is 4 MPa while it is around 18 MPa in (b), indicating the stress concentration in latter was much larger than the former. In the solder bump with crack, two high-stress locations are found according to **Fig. 7. 5**

(b). The area C is the tip of the crack, undergoing a large deformation in thermal cycling due to the mismatch in the CTE of BT-substrate and the chip. It is the outmost location of the contacting interface with the copper pad, corresponding to area A in **Fig. 7.5** (a). Another location is area D, where is the corner of contacting surface with the underfill. Due to the crack resulted by electro-migration, the surface of the solder bump beneath the crack was separated with the copper pad, which makes it a free surface without mechanical constraints. Therefore, the lowest stress in the solder bump were distributed in this surface, as presented in **Fig. 7.5** (b). Meanwhile, the material located in area D tended to deform together with the underfill, resulting in a stress concentration location. For a further understanding of the area with large deformations, the distribution of CEEQ and PEEQ of the two models are presented in **Fig. 7.6**.

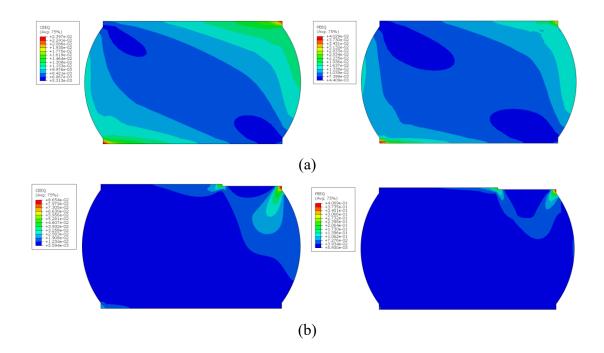


Fig. 7. 6. Distribution of CEEQ and PEEQ in the outmost solder bump after thermal cycling (t = 3600 s): (a) bump without void; (b) bump with failure occurrence due to electro-migration

According to **Fig. 7. 6** (a), the highest CEEQ and PEEQ were still located at the right upper and the lower corner of the solder bump without voids, although its residual stress distribution presented a different condition. For the solder bump with a crack, the large values of CEEQ and PEEQ were located at D area, which is similar to its stress distribution. Therefore, these areas were considered as the potential locations for fatigue

failure initiation, and their strain histories will be further investigated in next section associating with fatigue-life prediction.

7.3.2 Accumulated inelastic strains and prediction of thermal fatigue life with global model

According to the discussions in Chapter 5, the model based on the Coffin-Manson equation for the life prediction of Sn-Ag-Cu solder bump joint was adopted:

$$N = C_1 (\Delta \varepsilon_{in}^{acc})^{C_2} \tag{7-1}$$

where *N* is the number of cycles to failure in fatigue; C_1 and C_2 are the material constants mentioned in Section 2.4.2, with values of 27.63 and -1.08 for SAC305 respectively; $\Delta \varepsilon_{in}^{acc}$ is the accumulated inelastic strain in a stable thermal cycle, which can be obtained by summing the equivalent inelastic strain increments of all load steps in the cycle:

$$\Delta \varepsilon_{in}^{acc} = \sum_{i=1}^{n} \Delta \varepsilon_{in,i}^{eqv} . \qquad (7-2)$$

To evaluate the fatigue life, the history of the largest accumulated inelastic strain in the solder bump should be figured out. The accumulated inelastic strain is formed by its creep part (CEEQ) and plastic part (PEEQ) here. Based on the discussion in former section and chapter, area A, B and D are the three potential locations with large values of inelastic strain. Hence, their strain evolution histories during thermal cycling are plotted in **Fig. 7.7** for comparison. The solid and dashed curves in this figure represent the simulated strain results for cases with and without the void effect, respectively.

According the evolution histories in **Fig. 7. 7**, the inelastic strains in the solder bump with crack are much larger than the bump without crack. This result is reasonable as a void or a crack in a structure leads to stress concentration, and some inelastic strains if the structure is under cycling mechanical loads. For the locations in the bump without crack, area B presents higher accumulative strains compared with area A. This result is

the same as the conditions in Chapter 5. Hence, the inelastic strains of location B will be used to calculate the thermal-fatigue life.

Based on the discussion above, the accumulated inelastic strains in area B are used as the $\Delta \varepsilon_{in}^{acc}$ in Equation 7 – 1 for the bump with crack. Some further observation of FE results found that the largest inelastic strains always distribution at area B when the crack propagates. Hence, the fatigue life can be predicted under the assumption that the crack length was constant during the thermal cycling. **Fig. 7. 8** shows the relationship between the predicted fatigue life of the solder bump and the crack length.

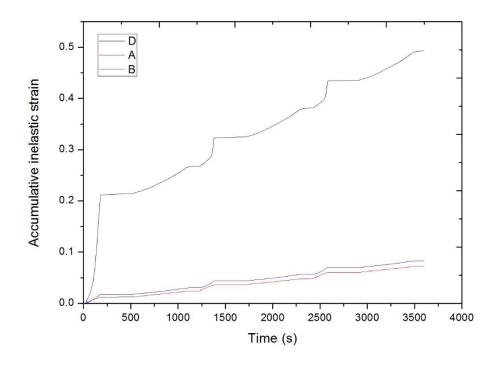


Fig. 7. 7. History of accumulated equivalent inelastic strain at the area A, B and D for global model

Notice that the thermal fatigue cycles of the solder bump without crack in this chapter was 1847, which was approximately 174% larger than the bump's life in Chapter 5. The thermal cycling loading in Chapter 5 was an accelerated thermal-cycling test (ACTC). The temperature range in that test condition was much higher than daily application, as set in this chapter. Therefore, the package showed a better reliability under a normal thermal cycling loading in this chapter.

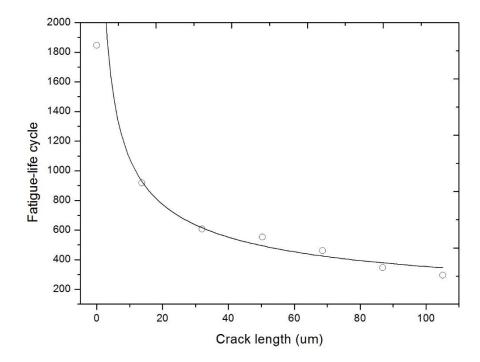


Fig. 7. 8. Relationship between the predicted fatigue life and the crack length

7.3.3 Service life of package under joint effects of thermal fatigue and electromigration

The calculation of the life in service of the sub-model under effects of electro-migration adopted the method proposed in Chapter 6. However, unlike the conditions employed in Chapter 6, thermal stress was also induced in this simulation. Hence, the effects of stress-migration need to be evaluated. Mass diffusion triggered by the thermal stress gradient is described as [6]:

$$\vec{J}_s = -\frac{N\Omega D_0}{kT} \exp\left(-\frac{E_A}{kT}\right) \operatorname{grad}\sigma_M$$
, (7-3)

where $\sigma_M = \frac{\sigma_{xx} + \sigma_{yy} + \sigma_{zz}}{3}$ is hydrostatic stress, σ_{xx} , σ_{yy} and σ_{zz} are the stress values for three principle directions. In ABAQUS 6.14, a mechanical output variable, *PRESS*, is defined as the equivalent pressure stress as:

$$PRESS = -\frac{1}{3} (\sigma_{xx} + \sigma_{yy} + \sigma_{zz}) = -\sigma_M . \qquad (7-4)$$

Under the effect of thermal cycling, hydrostatic stress σ_M varies with time, which means the stress component \vec{J}_s varies during a thermal cycle. Also, the thermalmigration component \vec{J}_{TH} and electro-migration component \vec{J}_{EM} changes with time during the cycle. Since electro-migration occurs under the effects of electrical current, it was supposed there was no migration process in room temperature. The value of thermal-migration \vec{J}_{TH} is highly determined by the temperature gradient and is relatively low at room temperature. Therefore, \vec{J}_{TH} is assumed to be constant in the periods of the heating and high-temperature-dwell for convenience of calculations. The stress-migration component \vec{J}_s was calculated with Equation 7 - 4 by integrating σ_M with time. **Table 7. 3** presents the data on migration of atoms caused by three migration components in the critical location of the solder bump without the void during the thermal cycle.

Table 7.3. Transformed atoms due to electro-migration, thermo-migration and stressmigration in critical location with $N_0 = 1$ in one thermal cycle

Migration component	div \vec{J}_{EM}	div \vec{J}_{TH}	div \vec{J}_s	\vec{J}_{total}
/m ³	2.572e-06	1.585e-10	7.56e-08	3.022e-03

According to **Table 7. 6**, the value of atom flux caused by electro-migration is much higher than that for the rest migration components. Therefore, electro-migration caused by flow of electrons was the dominant process in electro-migration. In calculation of service life, the atom flux due to stress-migration and thermos-migration in thermal cycling of this chapter could be neglected. The total migration time in one thermal cycle is 480s

The calculation process for life in service of solder bump under the joint effects of thermal fatigue and electro-migration is presented in **Table 7. 4**. In this table, the migration time is calculated based on the data from the results of thermal-electrical analysis with the sub-model. Column "Cycles" presents the corresponding number of

thermal cycles during the migration time. The damage is computed as a ratio of number of cycles to the corresponding fatigue life from. It indicates the damage contributing to the final thermal fatigue failure during the migration time. From the results in **Table 7**. **4**, failure caused by thermal fatigue occurs prior to the one due to electro-migration in the solder bump as the accumulated damage reached unit before the formation of the first void. It indicates that the thermal-fatigue failures in the electronic packages are the main failure mode under a daily-used condition. The SnAgCu solder material presents a relative better performance in electro-migration than in thermal-fatigue failure. As the algorithm proposed by this chapter is an element-based method, it is not suitable to the condition before the removal of element. However, notice that the time before the first void formation was very close to the thermal-fatigue limits of the solder bump under the condition in this simulation, some micro voids formed before the first removal of the element may initiate the reduction of the thermal-fatigue.

 Table 7. 4. Calculated life in service of solder bump under the joint effects of thermal fatigue and electro-migration

Void-forming element	Migration time	Cycles	Damage	Accumulated damage
1st	248.4 h	1863	1.01	1.01

7.4 Summary and conclusions

In this chapter, a FE model comprising a global model and a sub-model was built to assess the service life of a typical BGA package under joint effects of thermal fatigue and electro-migration. The global model and the sub-model were used for thermalmechanical and thermal-electrical analyses respectively. From the presented results and discussions, it could be concluded that:

 Voids formed by electro-migration change the location of stress concentration in solder bumps of the BGA package. The stress concentration could be found at the tip of the void and the contacting area with underfill. These locations tend to become the most critical area in the solder bump.

- 2. Void formation and crack propagation in the solder bump increases highest values of stress significantly. The differences in stresses for packages with and without the void are affected by creep behaviours of solder.
- 3. In the process of void growth, inelastic strains in solder bumps increased significantly at the early time of void expansion. However, strain increments tended to decrease with the void evolution. In the late stage before electro-migration failure a decreasing trend of inelastic strains was found. The thermal-fatigue life under the effect of voids evaluation presents similar trends as it is determined by inelastic strains in solder bumps.
- 4. Failures caused by electro-migration occur prior to those due to thermal fatigue in solder bumps. The electrical current crowding becomes more severe with this process. The service life of solder bumps is determined by the failures caused by electro-migration. For solder bumps exposed to the effect of electrical current, thermal cycling exerts a limited effect on their life in service.

Reference

- Li X., Wang Z., "Thermo-fatigue life evaluation of SnAgCu solder joints in flip chip assemblies", *Journal of Materials Processing Technology*, vol 183 (2007), pp 6–12.
- [2] Wang T., Lai Y., Wu J., "Effect of underfill thermomechanical properties on thermal cycling fatigue reliability of flip-chip ball grid array", ASME Journal of Electronic Packaging, vol. 126(2005), pp. 560-564
- [3] Liang S. W., Chang Y. W. and Chen C., "Effect of Al-trace dimension on Joule heating and current crowding in flip-chip solder joints under accelerated electromigration", *Applied Physics Letters*, vol. 88 (2006), 172108.
- [4] Chiou Y. Ch., Jen Y. M., Huang Sh. H., "Finite element based fatigue life estimation of the solder joints with effect of intermetallic compound growth", *Microelectronics Reliability*, Vol 51 (2011), pp. 2319-2329.Material properties 1/N
- [5] Lau J. H., Lee S.WR., "Modeling and analysis of 96.5Sn–3.5Ag lead-free solder joints of wafer level chip scale package on buildup microvia printed circuit board",
- [6] IEEE Transactions on Electronics Packaging Manufacturing, 25 (2002), pp. 51-58.Pak J., Pathak M., Lim S. K. and Pan D. Z. "Modeling of Electromigration in Through-Silicon-Via Based 3D IC", Electronic Components and Technology Conference (2011).
- [7] Liu Y., Liang L., Irving S., "3D Modelling of electromigration combined with thermal-mechanical effect for IC device and package", *Microelectronics Reliability*, 48 (2008), pp. 811-824.

Chapter 8. Conclusions and future work

8.1 Main conclusions

Based on the presented modelling results in the previous chapters, main conclusions of this thesis are summarized in this chapter. As each chapter is focused on individual research topics and they are all correlated with others, the summaries and the main conclusions for the findings of entire thesis can be drawn in the following sections.

8.1.1 Microstructure geometry and shape prediction of a solder bump

An as-reflowed Sn/Cu structure with the 20- μ m-thickness of Sn electroplating layer was prepared and observed. Based on the observation, the component of IMC in the sample is Cu₆Sn₅ and its average thickness is approximately 2 μ m. The main features of the morphology of IMC layer was dealt with statistically and transferred into FEmodel. Moreover, the external shape of a solder bump with certain combination of paddiameter and stand-off-height was predicted by an energy-based programming method. The results proved that the effect of gravity on the external shape could be neglected. The surface of a solder bump could be achieved by revolution of a part sphere while the sphere centre was not on the revolution axis.

8.1.2 Mechanical behaviours of package and single solder bump of BGA under thermal cycling

Two-dimensional FE-models of flip-chip packages with solder bumps with pre-defined microstructures were developed. Their performances under thermal cycling loads were investigated and discussed. From the simulated results, creep properties of the solder affected the mechanical behaviour of solder bump under high temperature significantly. To evaluate the mechanical behaviour of solder bumps properly, creep properties must be included in the simulations.

According to the distribution of thermal stress, the joint located on the edge of the BGA underwent the largest deformation in the package. The highest stresses and strains were located at the upper right corners of the outmost solder bumps, which indicates that these places are the most critical area in the whole package. Besides, formation and increased thickness of the IMC layer resulted in heavier stress concentrations at the critical area in the bumps.

The solder bumps with the tens-of-microns stand-off height presented higher stiffness under thermal cycling loads. Their scalloped shape of the IMC layer changed the distribution of stresses and strains. The stress and strain concentrations could be found at the area of the solder adjacent to the tops of scalloped IMCs on the right upper side.

Based on the results of prediction of thermal fatigue, formation of the IMC layer reduced the fatigue life of solder bumps, as the existence of the IMC layer reduced the effective stand-off height of the solder bumps. The predicted life of solder bumps with the small stand-off height was much longer than that of the large ones.

8.1.3 Electro-migration in single solder bump of BGA

Two-dimensional FE-models of single solder bump with different current-loading types were developed. Their thermal and electrical performances under electrical-current loading were simulated and discussed. From the results, electrical currents change their directions when they enter bumps from copper traces in solder bumps of the BGA package. This results in severe electrical current crowding at the corners connecting the copper trace and the solder bump. Also, electrical-current crowding could also be found at the connecting corners of the copper trace and the solder bump in the TSV package. However, its level was much lower than that in the bumps in BGA. On the other hand, the distribution of temperature in a solder bump was affected more by environmental temperature than by the electrical current. The difference of temperature in the solder bump could be neglected while its gradient is relatively high due to the size of solder bumps.

An algorithm to simulate formation and evolution of voids has based on the FE results

was developed. From the presented results and discussions, the atom flux caused by thermo-gradient migration was much lower than that caused by current-migration, which means it could be neglected during the migration process. And electrical current crowding became more severe with the process. Once the void was formed in the solder bump, its expansion speed increased with its evolution.

8.1.4 Joint effects of thermal fatigue and electro-migration on solder bumps

A FE-model comprising a global model and a sub-model was built to assess the service life of a typical BGA package under joint effects of thermal fatigue and electromigration. Based on the results, voids formed by electro-migration change the location of stress concentration in solder bumps of the BGA package. The stress concentration could be found at the tip of the void and this location tends to become the most critical area in the solder bump. Besides, the voids in the solder bump increases high values of stress in the model significantly. In the process of void growth, inelastic strains in solder bumps increased significantly at the early time of void expansion. However, strain increments tended to decrease with the void evolution in the late stage. The thermalfatigue life under the effect of voids evaluation presents similar trends as it is determined by inelastic strains in solder bumps.

Failures caused by electro-migration occur prior to those due to thermal fatigue in solder bumps. The electrical current crowding becomes more severe with this process. The service life of solder bumps is therefore determined by the failures caused by electro-migration. For solder bumps exposed to the effect of electrical current, thermal cycling exerts a limited effect on their life in service.

8.2 Major contributions

This systematic simulation has elaborated a modelling process to evaluate service life based on real micro-structures in a solder bump. A FE-model including some solder bumps based on the main features of real ones was built and evaluated under the condition of thermal fatigue. Furthermore, an FE-based estimation method of the changing structure in the solder bump was proposed to evaluate thermal-fatigue reliability. The concept, accumulative damage, can be applied to other conditions of gradual structure changes in the solder bump.

For electro-migration, a numerical description, based on the governing equations, was proposed to simulate voids formation and crack propagation in a solder bump. However, as this method was based on element removal from FEA, it showed a high dependency on the mesh quality of the FE model. This method provided a method to simulate void formation during FE analysis, which could be referred for the following simulation related to structure changes. For the precise prediction of void/crack shape, this method is not applicable.

In addition, based on the former two parts, a FE-based flowchart to evaluate the joint effect of thermal fatigue and electro-migration was proposed in this work. As the joint effect of these two reliability issues was rarely researched so far, the flowchart proposed a process to evaluate the combination of these two failure reasons. It is helpful understand their priority of occurrence and interaction of failure mechanism when the electronic packages are facing a complex using condition.

8.3 Future work

The work in this thesis can be further enhanced and extended by further investigations recommended as follows:

1. The method of the prediction of external shape of the solder bump is an energybased programming process. Some other methods, e.g. a geometry-based truncated sphere method and force-balance analytical solution, can also be applied to the prediction of external shapes. By comparing the results of these methods, a more precise external shape of solder bump can be achieved.

2. The evolution of the morphology of IMC layers in a micro-scale solder bump under aging can be further investigated. Since the morphology of IMC layers in a solder bump under micro-scale has great effects on its mechanical behaviours, it should be analysed under different conditions. Main morphology features of IMC layers after various durations of aging should be studied statistically.

3. This thesis adopted the accumulated inelastic strains in a solder bumps as an indicator to estimate its fatigue life. However, this method is generally based on some bulk specimens. Therefore, for those solder bumps under micro-scale, effect of crystal lattice, e.g. anisotropy and grain boundary, should be considered for precise evaluation of fatigue life.

4. Two-dimensional FE-models was used to simulate the voids formation and crack propagation under electro-migration. However, as the method to simulate void is based on removal of elements, three-dimensional FE-models should be a better approach to calculate the total service life under electro-migration as a potential future work.

Appendix

Surface Evolver programs

```
// mircron ball grid array joint.
// tension and gravity
evolver_version "2.11c" // needed for zforce.cdm
// physical constants
parameter S TENSION = 500
                                   // liquid solder surface tension, mN/m
parameter SOLDER DENSITY = 7.04 // grams/cm<sup>3</sup>
                           // \text{ cm/sec}^2
gravity constant 980
// configuration parameters
parameter height = 0.02
                             // height of upper pad, cm
parameter radius = 0.016
                              // radius of pads, cm
// lower pad
constraint 1
formula: z = 0
// upper pad
constraint 2
formula: z = height
// rim of pads
constraint 3
formula: x^2 + y^2 = radius^2
vertices
// lower pad
   radius*cos(0*pi/3) radius*sin(0*pi/3) 0
                                               constraints 1,3 fixed
1
2
   radius*cos(1*pi/3) radius*sin(1*pi/3) 0
                                               constraints 1,3 fixed
3
   radius*cos(2*pi/3) radius*sin(2*pi/3) 0
                                               constraints 1,3 fixed
4
   radius*cos(3*pi/3) radius*sin(3*pi/3) 0
                                               constraints 1,3 fixed
5
                                               constraints 1,3 fixed
   radius*cos(4*pi/3) radius*sin(4*pi/3) 0
6
   radius*cos(5*pi/3) radius*sin(5*pi/3) 0
                                               constraints 1,3 fixed
// upper pad
7
   radius*cos(0*pi/3) radius*sin(0*pi/3) height
                                                    constraints 2,3 fixed
                                                    constraints 2,3 fixed
8
   radius*cos(1*pi/3) radius*sin(1*pi/3) height
9
   radius*cos(2*pi/3) radius*sin(2*pi/3) height
                                                    constraints 2,3 fixed
10 radius*cos(3*pi/3) radius*sin(3*pi/3) height
                                                    constraints 2,3 fixed
11 radius*cos(4*pi/3) radius*sin(4*pi/3) height
                                                    constraints 2,3 fixed
                                                    constraints 2,3 fixed
12 radius*cos(5*pi/3) radius*sin(5*pi/3) height
```

edges // lower pad edges 1 constraints 1,3 fixed 1 2 2 2 3 constraints 1,3 fixed 3 3 4 fixed constraints 1,3 4 4 5 fixed constraints 1,3 5 5 6 constraints 1,3 fixed 6 6 1 fixed constraints 1,3 // upper pad edges fixed 7 7 8 constraints 2,3 8 8 9 constraints 2,3 fixed 9 9 10 constraints 2,3fixed 10 10 11 constraints 2,3 fixed 11 fixed 11 12 constraints 2,3 12 127 constraints 2,3 fixed // vertical edges 13 1 7 14 2 8 15 3 9 16 4 10 17 5 11 18 6 12 faces // lateral faces 1 14 -7 -13 tension S_TENSION 1 2 2 1 5 -8 -14 tension S TENSION 3 3 16 -9 -15 tension S_TENSION 4 4 17 -10 -16 tension S TENSION 5 5 18 -11 -17 tension S_TENSION 6 6 13 -12 -18 tension S_TENSION // lower pad -6-5-4-3-2-1 fixed no refine color red tension 0 7 // upper pad 8 7 8 9 10 11 12 fixed no_refine color green tension 0 constraint 2 bodies // defined by oriented face list 1 12345678 volume 1.3*pi*radius^2*height density SOLDER_DENSITY read hessian_normal // Typical evolution gogo := { u; g 5; r; g 5; r; g 5; hessian; hessian }