THIN FILM CDTE SOLAR CELLS DEPOSITED BY PULSED DC MAGNETRON SPUTTERING

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A Doctoral Thesis

Submitted in partial fulfilment of the requirements for the award of

Doctor of Philosophy of Loughborough University

CERTIFICATE OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this thesis, that the original work is my own except as specified in acknowledgments or in footnotes, and that neither the thesis nor the original work contained therein has been submitted to this or any other institution for a degree.

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Abstract

Thin film cadmium telluride (CdTe) technology is the most important competitor for silicon (Si) based solar cells. Pulsed direct current (DC) magnetron sputtering is a new technique has been developed for thin film CdTe deposition. This technique is industrially scalable and provides uniform coating. It is also possible to deposit thin films at low substrate temperatures. A series of experiments are presented for the optimisation of the cadmium chloride ($CdCl_2$) activation process. Thin film CdTe solar cells require $CdCl_2$ activation process to improve conversion efficiencies. The role of this activation process is to increase the grain size by recrystallisation and to remove stacking faults. Compaan and Bohn [1] used the radio-frequency (RF) sputtering technique for CdTe solar cell deposition and they observed small blisters on CdTe layer surface. They reported that blistering occurred after the $CdCl_2$ treatment during the annealing process. Moreover, void formation was observed in the CdTe layer after the $CdCl_2$ activation process. Voids at the cadmium sulphide (CdS)/CdTe junction caused delamination hence quality of the junction is poor. This issue has been known for more than two decades but the mechanisms of the blister formation have not been understood. One reason may be the stress formation during CdTe solar cells deposition or during the $CdCl_2$ treatment. Therefore, the stress analysis was performed to remove the defects observed after the $CdCl_2$ treatment. This was followed by the rapid thermal annealing to isolate the $CdCl_2$ effect by

simply annealing. Small bubbles observed in the CdTe layer which is the first step of the blister formation.

Using high resolution transmission electron microscopy (HR-TEM), it has been discovered that argon (Ar) working gas trapped during the deposition process diffuses in the lattice which merge and form the bubbles during the annealing process and grow agglomeration mainly at interfaces and grain boundaries (GBs).

Blister and void formation were observed in the CdTe devices after the $CdCl_2$ treatment. Therefore, krypton (Kr), neon (Ne) gases were used as the magnetron working gas during the deposition of CdTe layer. The results presented in this thesis indicated that blister and void formation were still existing with the use of Kr an Ne. Xe, which has a higher atomic mass than Kr, Ne, Ar, Cd and Te, was used as the magnetron working gas and it resulted in surface blister and void free devices.

Keywords: CdTe; thin film; solar cells; pulsed DC magnetron sputtering; $CdCl_2$ activation process; bubble formation, blistering, working gas.

To the memory of my grandfather Baki Çalışkan

Acknowledgement

I would like to express my sincere gratitude to my supervisors Prof Michael Walls, Dr Gianfranco Claudio and Dr Jake Bowers. I would especially like to express my gratitude and thanks to Prof Walls for his guidance, motivation and patience throughout my PhD research. I would like to thank Dr Claudio for his help especially in the early stages of my PhD. I also thank Dr Bowers for his supervision. I would like to express my deep gratitude to Ministry of National Education, Republic of Turkey for funding my studies. I would like to acknowledge Colorado State University for providing samples.

I am grateful to Dr Piotr Kaminski for his invaluable assistance during my PhD. I wish to thank Dr Ali Abbas for his support in material characterisation. Bianca and Fabiana thanks for your support during the experiments. Gerald I would like to thank for proof reading this thesis. I would like to thank everyone at CREST. I am thankful to all my friends for their present and support.

I would like to thank Prof Davide Mariotti and Prof Roger Smith for accepting being my examiners.

To my Mom and Dad, my Brother, there are not enough words I can say to describe how grateful I am for your constant love and support.

Publications

PATENT APPLICATION

Loughborough University, British Patent Application No. 1618474.9 – Improvements to the deposition and formation of coatings for photovoltaic cells for use in the generation of solar power, 2 November 2016.

CONFERENCE PAPERS

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Contents

ABBREVIATIONS

A: absorption

A: constant

Å: angstrom

AC: alternating current

Al: aluminium

Al_2O_3: alumina

Ar: argon

As: arsenic

a-Si: amorphous silicon

at%: atomic percent

B: boron

C: carbon

C_B: conduction band

CCI: coherence correlation interferometry

Cd: cadmium

CDA: compressed dry air

$CdCl_2$: cadmium chloride

CdS: cadmium sulphide

CdTe: cadmium telluride

CIGS: copper indium gallium di-selenide

CIS: copper indium selenium

Cl: chlorine

c-Si: crystalline silicon

CSS: close space sublimation

CSU: Colorado State University

CSVT: close space vapour transport

CTO: cadmium stannate (Cd_2SnO_4)

Cu: copper

CZTS: copper zinc tin sulphide

d: lattice constant

d_0: baseline d-spacing (stress relief)

2θ: diffraction angle

DC: direct current

DI: de-ionised

EDX: energy dispersive x-ray

η: efficiency

E_F: Fermi level

Eg: band gap energy

e. m. f.: electro-motion-force

f: the fraction of working gas trapped in the material

Fe: iron

FEG-SEM: field emission gun scanning electron microscope

FF: fill factor

FIB: focused ion beam

FTO: fluorine doped tin oxide

GaAs: gallium arsenide

GB: grain boundary

Ge: germanium

GW: gigawatt

h: Plank’s constant

H: hydrogen

HAADF: high angle annular dark field

HCF: helical complex field

He: helium

HR-TEM: high resolution transmission electron microscopy

IPA: isopropanol

IR: infra-red

Jsc: current density

Kr: krypton

LACBED: large-angle convergent-beam electron diffraction

LCOE: levelized cost of energy

LU: Loughborough University

MFC: mass flow controller

min: minutes

Mo: molybdenum

MOFSET: metal-oxide-semiconductor field effect transistor

n: integer

N: the number of Ar atoms bombarding a unit area per unit of time

N_2: nitrogen

N_A: acceptor atom density

N_D: donor atom density

N_V: holes density

Nb_3Ge: niobium-germanium

Ne: neon

Ni: nickel

NREL: National Renewable Energy Laboratory

OECD: Organisation for Economic Co-operation and Development

p: numerical coefficient

P: phosphorus

poly-Si: polycrystalline silicon or polysilicon

Pt: platinum

PV: photovoltaic

PVD: physical vapour deposition

R: deposition rate

R: reflectance

RF: radio-frequency

Rn: radon

ROHS: restriction of the use of certain hazardous substances

rpm: revolutions per minute

RT: room temperature

RTP: rapid thermal processor

sccm: standard cubic centimetres per minute

SDD: silicon drift detector

SEM: scanning electron microscopy

Si: silicon

SiO_2: silicon dioxide

STEM: scanning transmission electron microscopy

SWLI: scanning white light interferometry

α: sticking coefficient

ε: strain

TCO: transparent conducting oxide

Te: tellurium

TEM: transmission electron microscopy

$TiSi_2$: titanium silicide

T: transmittance

v: frequency

V_B: valence band

Voc: open circuit voltage

VTD: vapour transport deposition

wt.: weight

Xe: xenon

XRD: x-ray diffraction

λ: x-ray wavelength

ZnTe: zinc telluride

ZTO: zinc stannate (Zn_2SnO_4)

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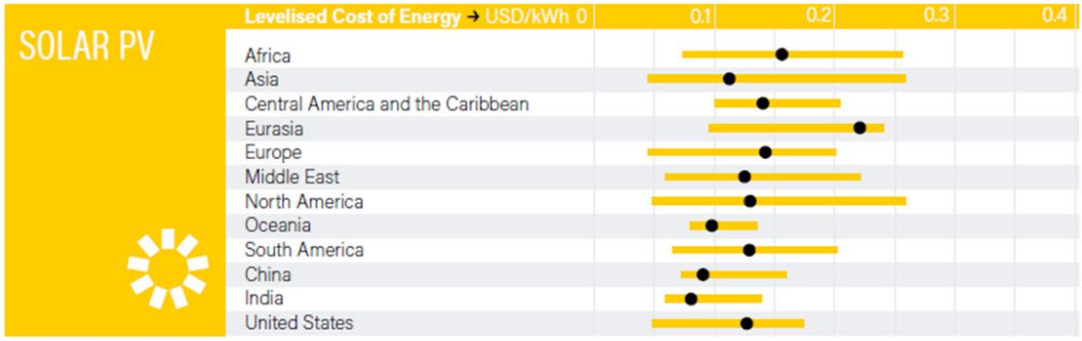
CHAPTER I

1. Introduction

Since 1990, renewable energy technologies have become an important field of research due to the insecurity of supply of fossil fuels. These technologies became more important in the 21st century due to concerns over climate change since they offer energy that is clean and sustainable. [2], [3] The capacity of renewable power has increased by ~9% between 2015 and 2016 with total global capacity reaching a total ~2,017 gigawatt (GW). In this period, renewable energies accounted for about 62% of new additions to power generating capacity worldwide. The share of renewable sources was as follows: Solar photovoltaic (PV) ~47%, wind with 34%, 15.5% from hydropower, and ~3.5% bio-power sources. [4]

The levelized cost of energy (LCOE) of solar PV has decreased by 58% between 2010 and 2015 [5]. Figure 1-1 shows recent energy and investment costs of PV technology and its capacity factors by region. The capacity factor is the ratio of the

energy output to the theoretical output during the same amount of time. It is estimated that the installation costs of utility-scale PV systems will fall by a further 57% between 2015 and 2025 [5].



= LCOE range ● = LCOE weighted average wa = weighted average

Investment Cost → USD	min	max	wa	Capacity Factor →	min	max	wa
Africa	818	6848	● 2344		0.14	0.28	● 0.2
Asia	832	6124	● 1414		0.1	0.25	● 0.16
Central America and the Caribbean	1337	4000	● 2001		0.16	0.23	● 0.19
Eurasia	1484	3697	● 2537		0.1	0.18	● 0.14
Europe	944	2827	● 1370		0.1	0.3	● 0.12
Middle East	1311	4000	● 2554		0.17	0.35	● 0.26
North America	965	5900	● 2203		0.12	0.34	● 0.2
Oceania	1600	2785	● 2477		0.2	0.25	● 0.23
South America	1407	4951	● 2477		0.12	0.34	● 0.24
China	1022	1953	● 1083		0.17	0.19	● 0.17
India	916	1832	● 1064		0.16	0.22	● 0.19
United States	1241	2971	● 1998		0.16	0.32	● 0.19

Figure 1-1 Status of Solar PV Technology: Costs and Capacity Factors (IRENA) [4]

1.1. Photovoltaic devices

PV devices are made of semiconductor materials and convert light into electrical power [6], [7]. The high energy photons with low wavelengths and high frequencies are suitable for PV conversion (Figure 1-2).

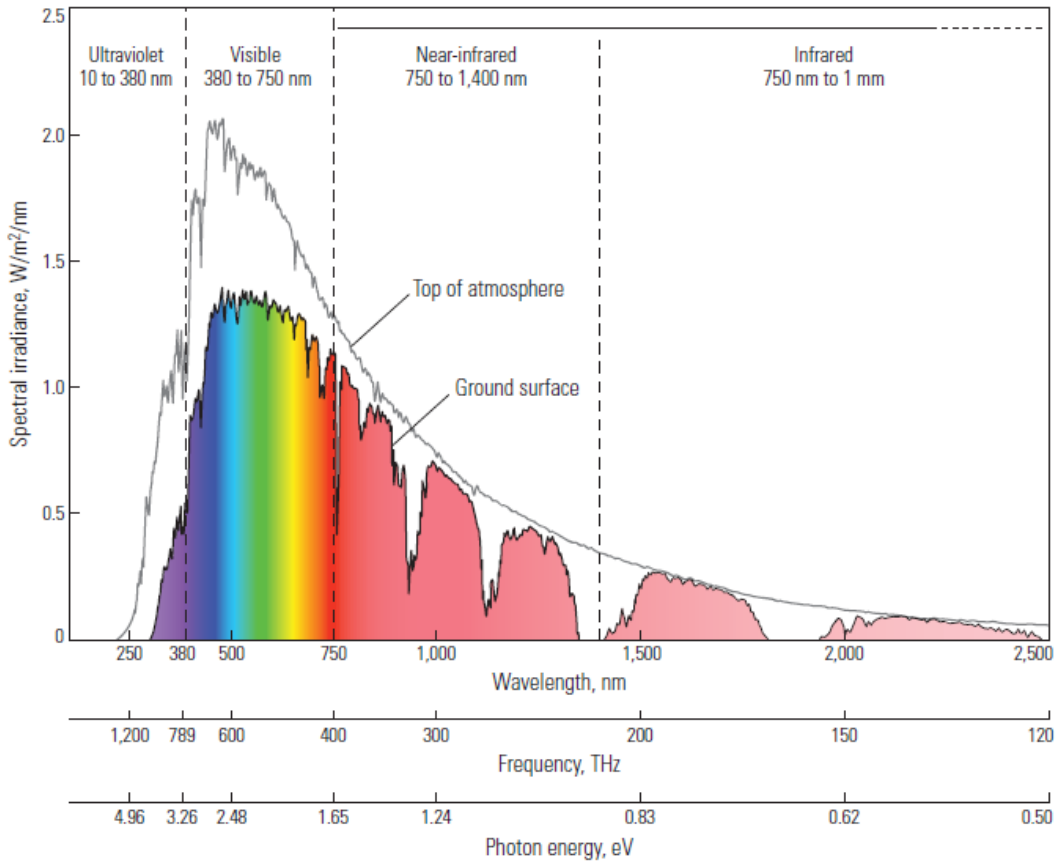


Figure 1-2 Solar radiation spectrum [8]

1.1.1. Semiconductors

A semiconductor has an empty conduction band and a filled valence band at zero temperature. The electron voids in the valence band are called holes. Donors are the

impurities that emit electrons into the conduction band. Band gap energy (*Eg*) is the energy difference between the valence and the conduction band edges. An intrinsic semiconductor contains no impurity carriers. In n-type materials, ionized donors provide free electrons and the Fermi level (E_F) the highest energy level that electrons occupy at absolute zero, is close to the conduction band (C_B). In p-type materials, it is the opposite, where E_F is closer to the valence band (V_B). [9], [10] Figure 1-3 shows a type I band alignment of (0001) CdS/CdTe heterojunction.

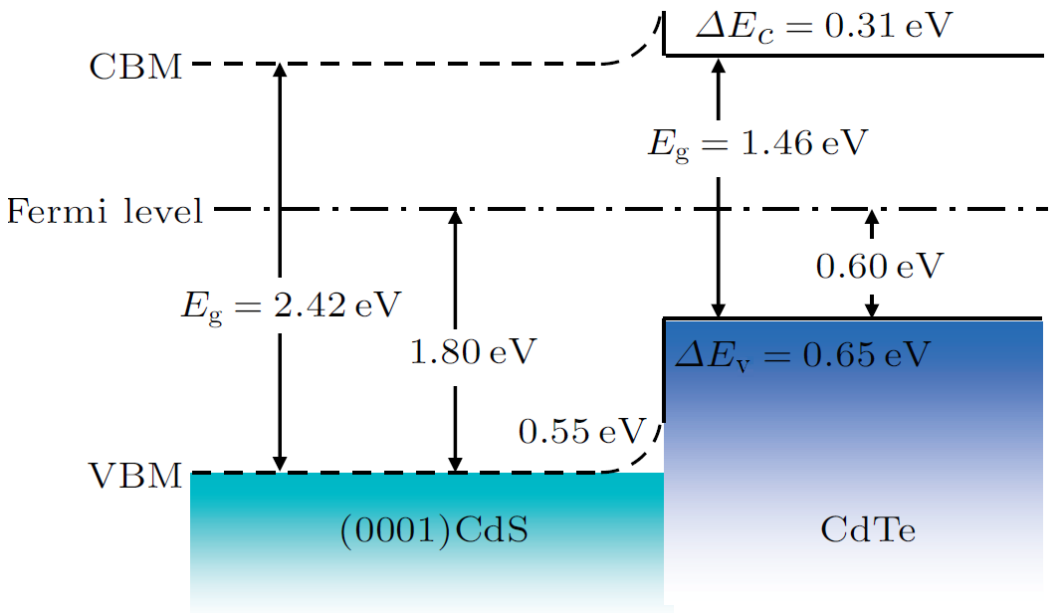


Figure 1-3 Band alignment of (0001)CdS/CdTe heterojunction showing the Fermi level, valence band offset and the conduction band offset [11]

1.1.2. P-n junction

A p-type material is a semiconductor which has been doped by a three valent atom (such as Si doped with boron (B)) and which will have an excess of acceptor atom density (N_A) compared to the donor atom density (N_D) resulting in $N_A >> N_D$. An n-

type material is a semiconductor which has been doped by a pentavalent atom (such as Si doped with phosphorous (P)) and has an excess of electron density compared to the hole density ($N_D >> N_V$). When a p and n type material join, the electrons and holes near to the junction neutralise each other with the formation of a region called "the depletion region", shown in Figure 1-4. The majority carriers in both regions will pass through the junction and this exchange creates an electric field which will balance the total charge [6].

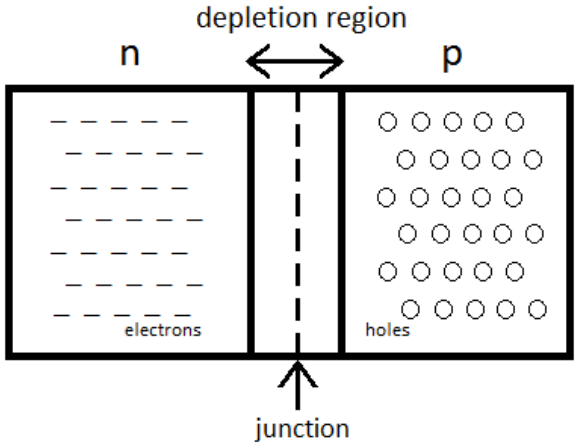


Figure 1-4 A schematic model of a p-n junction

1.2. Solar Cells

The two technologies dominating the PV market are crystalline silicon (c-Si) and thin film devices with market shares of 93% and 6%, respectively [12]. The first study on c-Si was performed by Ohl [13]. He invented an improved method for light-sensitive electric devices by cutting a Si ingot, includes a natural barrier, which is a suitable material for photo electro-motion-force (e. m. f.) solar cell production. This was followed by Chapin et al. [14] who worked on a new Si p-n junction photocell

in 1954. A thin layer of Si was deposited on top of an n type material and they achieved a cell efficiency of 6%. Fraas [15] reported that Hoffman Electronics improved the efficiency from 8% to 14% between 1957 and 1960. They also presented how to use a grid contact which reduced the resistance of the solar cell [15]. Lindmayer and Allison [16] from Comsat Laboratories developed the violet cell which extended the response to wavelengths below 0.5 μm. This device increased the fill factor (*FF*) and improved the short circuit current density (*Jsc*). Zhao et al. [17] achieved an efficiency of 24% in 1995 by reducing the resistance loss and using double layer antireflection coatings for Si devices. Battaglia et al. [18] reported that Panasonic, Japan achieved 25.6% power conversion efficiency which is the current world record for a c-Si solar cell.

Thin film PV technology has advantages over c-Si films such as reduced material usage due to direct bandgap materials, lower cost and the higher absorption coefficient [19]–[21]. Moreover, the conversion efficiencies of thin film devices are currently comparable with polysilicon (poly-Si) based PVs [22]. Thin film solar cells can be divided into three categories each of which has been commercialised. These are amorphous Si (a-Si), copper indium gallium di-selenide (CIGS) and CdTe thin film devices. a-Si devices are not as promising as CIGS or CdTe due to the Staebler-Wronski effect which affects the stability under light exposure [23], [24]. CIGS thin film technology is limited by its high production costs due mainly to the co-evaporating process which requires several material sources and an additional selenisation process which uses a highly toxic gas [25], [26]. CdTe solar cells is an

attractive technology for PV applications with low production costs reported recently at $0.45/Wp [27]. However, there is evidence that CdTe modules may be purchased for < $0.35/Wp indicating a further recent decrease in cost [28], [29].

A drawback of thin film CdTe technology is the mild toxicity of the CdTe. Fthenakis [30] reported that CdTe, shown in Figure 1-5, is less toxic and less soluble than cadmium (Cd) and tellurium (Te) [31]. CdS is also less toxic than Cd and Te compounds [30]. $CdCl_2$ used during the activation process is highly toxic however rinsing the film with DI after the treatment remove the $CdCl_2$ residue on the surface of the CdTe device. There is no health or environmental risks found during the use of CdTe PV technology. Test results showed that encapsulation in glass substrate avoids escape of CdTe to the environment [32]. Moreover, PV companies are working on re-cycling CdTe solar panels to protect the environment [31]. Cd use on PV modules is not prohibited by EU's Cd directive 91/338/EEC because the Cd is non-metallic in CdS and CdTe. However according to restriction of the use of certain hazardous substances (ROHS) regulations, CdTe will require an exception if there is any environmental, safety or health issues. [33]

Figure 1-5 Image of CdTe components [34]

CdTe is an ideal p-type semiconductor with a 1.45 eV direct bandgap which is close to the optimum for a solar cell and corresponds to a efficiency limit of ~30% [35]. The highest recorded efficiency for thin film CdTe technology is currently 22.1% reported by First Solar [22] as reported in the National Renewable Energy Laboratory (NREL) efficiency table in Figure 1-6.

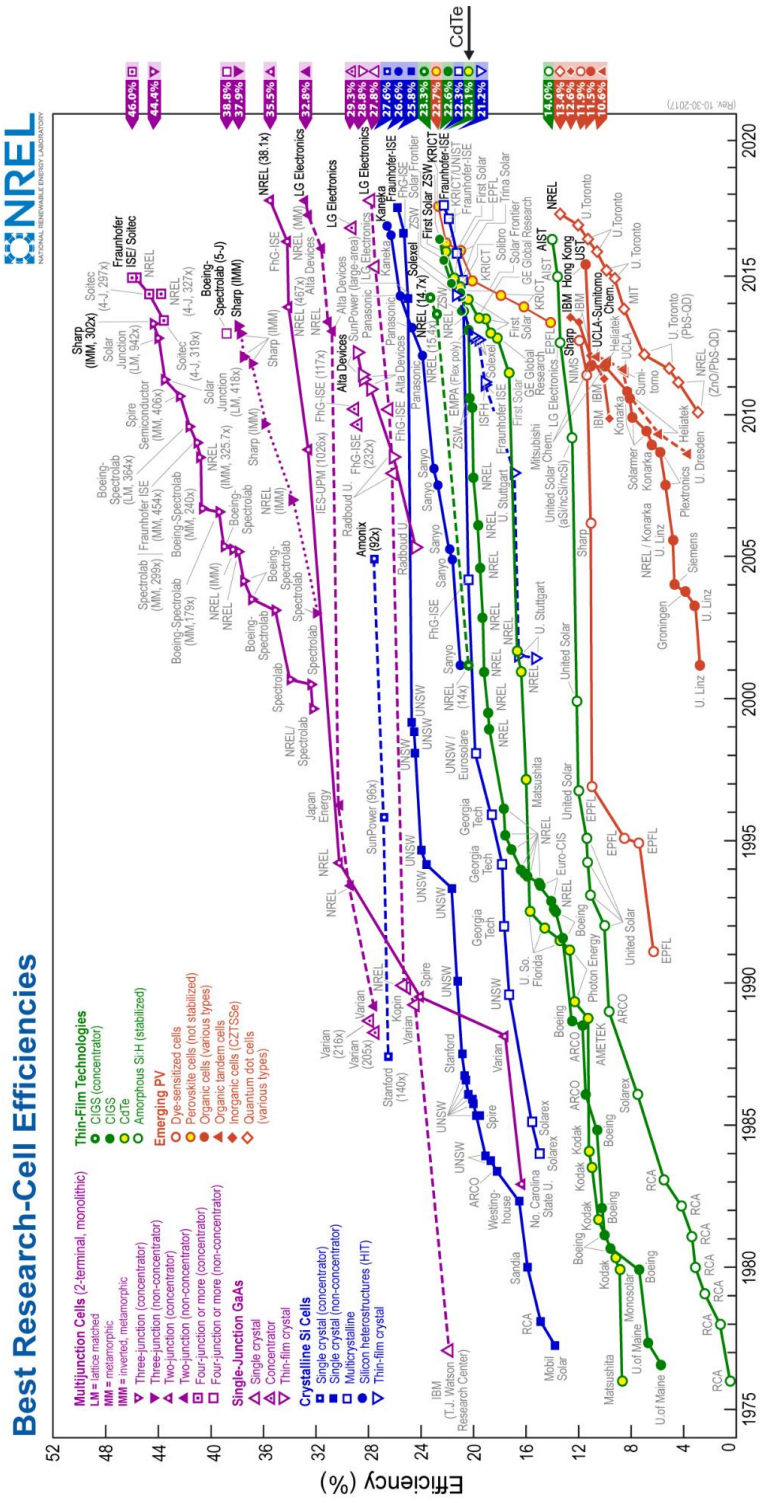


Figure 1-6 Cell Efficiencies by 2016 NREL [22]

1.2.1. Thin film CdS/CdTe solar cells: state-of-the-art

Figure 1-7 shows the timing of efficiency improvements and other notable developments in CdS/CdTe. The first CdTe device, CdTe-CdS p-n heterojunction solar cell, was reported in 1972 with an efficiency of 6%. The solar cells were prepared with high vacuum evaporation of CdS and vapour deposition of CdTe. [36] Nakayama et al. [37] from Matsushita Electric Industrial Co. Ltd. fabricated ceramic CdTe solar cells by screen printing and obtained 8.1% efficiency in 1976. In 1977, Mitchell et al. [38] achieved 8.4% efficiency for vacuum evaporated CdS/CdTe solar cells. Tyan and Webster [39], [40] from Eastman Kodak Company improved the conversion efficiency to 8.9% in 1980. They reported that an increase in substrate temperature during CdTe sublimation improved the efficiency [34]. In 1983, the reported highest efficiencies for close space sublimated (CSS) and close space vapour transport (CSVT) grown CdTe solar cells were 10.5% [41].

Kuribayashi et al. [42], [43] from Matsushita Electric Industrial Co. Ltd. reported a 12.8% efficient screen printed CdTe solar cells. The efficiency was improved by optimising the copper (Cu) added carbon (C) paste back contact [43]. Meyers [44] from Ametek Applied Materials Laboratory obtained 10.4% efficient cell with a novel design “CdS/CdTe/zinc telluride (ZnTe) n-i-p solar cell” in 1987. Mitchell et al. [45] from ARCO Solar achieved 10.5% efficiency by CSVT. Albright et al. [46] from Photon Energy reported 12.3% efficiency due to having developed a more transparent window layer in 1989. Morris et al. [47] improved the CdTe device efficiency to 13.1%. They used an electrodeposition process for deposition of the

CdS and CdTe layers. The University of South Florida [48]–[52] reported 13.4%, 14.6%, and 15.8% efficiencies of CSS grown thin film CdTe in the early 1990s. It has been reported that an efficiency of 14% was achieved for CdTe solar cells using electrodeposition in 1995 [32]. In 1997, Aramoto et al. [53], [54] from Matsushita Battery Industrial Co. Ltd. reported 16% efficiency of a thin film CdTe device deposited by CSS. Wu et al. [55] from NREL developed a new device structure "cadmium stannate (CTO)/zinc stannate (ZTO)/CdS/CdTe) which increased the efficiency to 16.5% in 2001. Acevedo [56] also achieved 16.5% efficiency for a Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe solar cell device. In 2009, Plotnikov et al. [57] from the University of Toledo fabricated a variety of thin CdTe devices and they achieved a maximum efficiency of 13.7%. Their 0.5 µm thick CdTe device resulted in 9.7% efficiency. Achievements on such thin devices can reduce the manufacturing cost more. Efficiencies of 17.3% by First Solar, 18.3% by GE Global, 18.7%, 20.4%, 21.5%, and 22.1% were achieved by First Solar between 2011 and 2016 [58]–[63].

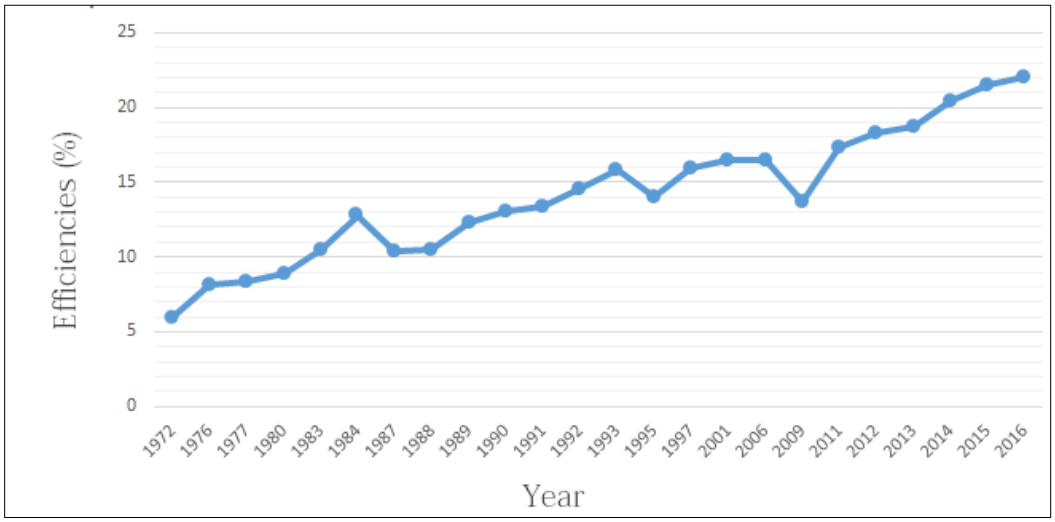


Figure 1-7 The change on the CdTe solar cell efficiencies and other notable development [32], [36]–[63]

1.2.2. Deposition Methods

Thin films of CdTe can be deposited using a number of techniques including vapour transport deposition (VTD), CSS and magnetron sputtering [64]–[66]. A VTD system, shown in Figure 1-8, delivers a vapour stream to the substrate and then the vapour desaturation results in the film formation [67], [68]. Substrate temperatures of around 250 ºC are high enough to deposit an efficient cell by sputtering [69]–[72], compared to 400 ºC to 500 ºC stated for VTD [73], [74].

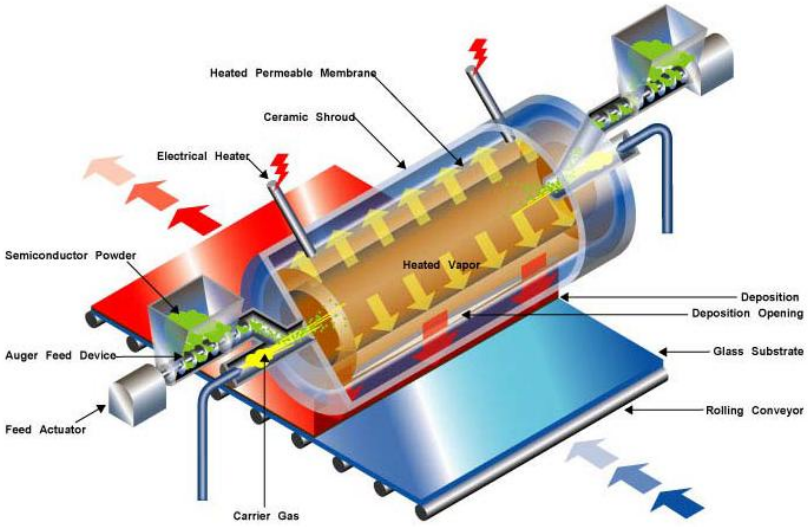


Figure 1-8 A schematic of the VTD [75]

CSS is also a physical vapour deposition (PVD) process at high substrate temperature allowing fast growth of the film. Highly efficient CdTe devices have been deposited with CSS, using a configuration shown schematically in Figure 1-9. Thin film CdTe devices are deposited at substrate temperatures of over 400 ºC under vacuum with CSS [68], [76]–[78].

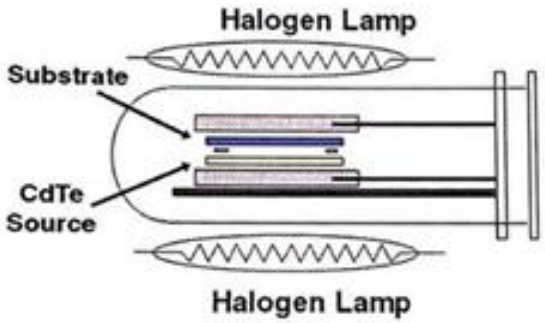


Figure 1-9 A schematic of the CSS [32]

DC magnetron sputtering is not suitable for dielectric targets, however RF magnetron sputtering has been widely used for thin film CdTe deposition [79]–[81]. The main advantages of the RF magnetron sputtering are the exceptional uniformity of the deposited layer, high thin film density and relatively low substrate temperatures during the device growth [82], [83]. A schematic diagram of the RF sputtering system used is shown in Figure 1-10.

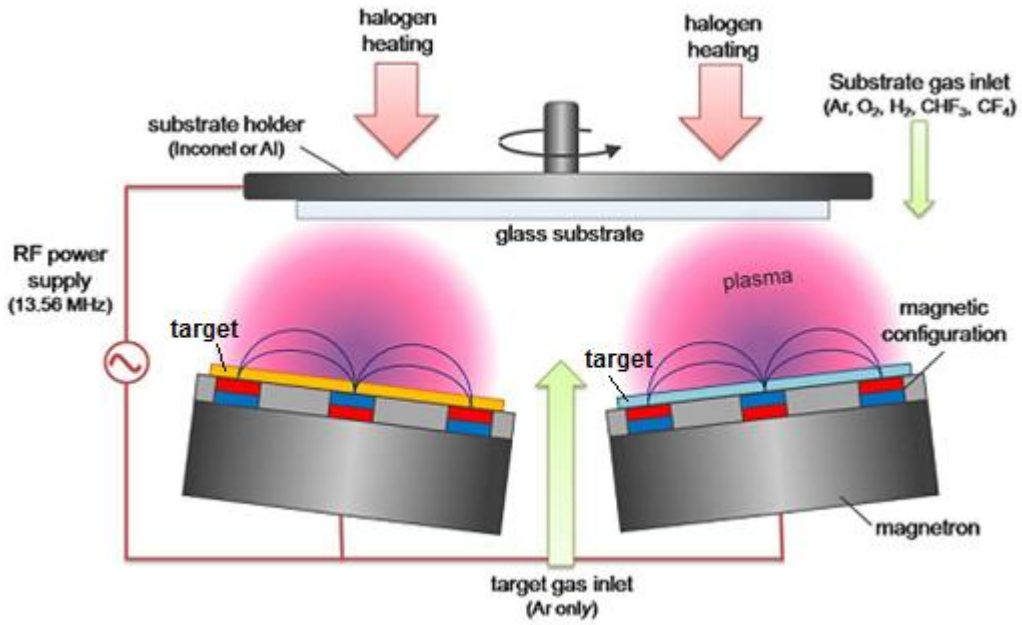


Figure 1-10 A schematic of the RF sputtering system [80]

1.2.3. Post annealing and the Cadmium Chloride ($CdCl_2$) Activation Process

For high conversion efficiency, CdTe solar cells require a $CdCl_2$ annealing process to remove defects. The $CdCl_2$ annealing activation process increases the grain size, causes recrystallization, removes stacking faults and passivates GBs. [81], [84]–[87] The $CdCl_2$ treatment also improves the *FF* and *Jsc* even though some defects remain.

There are two methods for the $CdCl_2$ activation process; wet treatment and evaporation. For the wet treatment, $CdCl_2$ solutions are prepared and either dropped onto the film surface or the film is dipped in the solution and then annealed [88]–[90]. For the evaporation process, $CdCl_2$ is deposited on thin film under vacuum and then annealed [91]–[93].

1.3. Scope of the Thesis

The novelty of this thesis lies in the deposition of thin film CdTe devices by pulsed DC magnetron sputtering. This deposition technique has not been used for thin film CdTe previously. In this thesis, it has also been discovered that Ar used as the working gas is trapped in the CdTe layer during the deposition process and this is responsible for dramatic surface blistering observed after the $CdCl_2$ activation process. For avoiding this acute problem, Xe replaced Ar as the working gas during the deposition of CdTe with pulsed DC magnetron sputtering.

The main objective of this study is to establish a high rate pulsed DC sputtering process conditions that lead to blister free devices and also minimises the density of defects in the absorber material (CdTe).

In order to achieve this objective, the following procedures were adopted:

- Deposition of thin film CdTe by pulsed DC magnetron sputtering and optimisation of the deposition conditions to maximise deposition rate and minimise stress.
- Optimisation of the $CdCl_2$ treatment process for sputtered CdTe devices.
- Structural analysis of CdTe films by pulsed DC sputtering.
- Rapid thermal annealing.
- Utilisation of Xe as a novel working gas for sputtering process.

1.3.1. The structure of the thesis

This chapter gives a short historical overview of the PV market, solar cells, deposition methods, annealing and the $CdCl_2$ activation process to improve the cell performance.

Chapter 2 introduces the methods used for thin film CdS/CdTe deposition, pulsed DC magnetron sputtering and a comparison with RF sputtering and CSS. The annealing processes of CdS/CdTe solar cells with rapid thermal processor (RTP) are described. The $CdCl_2$ treatment which is an essential process for CdTe devices, is identified. Furthermore, the effects of $CdCl_2$ treatment methods are compared. The characterisation methods used for sputtered CdS/CdTe solar cells are explained, including voltage measurements for electrical performance, and scanning electron microscopy (SEM) and transmission electron microscopy (TEM), which were used for microstructural analyses.

Chapter 3 introduces the strain analysis of CdS/CdTe devices deposited by pulsed DC magnetron sputtering using x-ray diffraction (XRD). Deposition conditions are optimised to eliminate the strain in the cell during deposition.

Chapter 4 provides a review on gas bubble formation in thin film materials. This chapter describes the thin film CdS/CdTe deposition with pulsed DC magnetron using Ar as the working gas. TEM, HR-TEM and energy dispersive x-ray (EDX) measurements are used for further analysis.

Chapter 5 focuses on annealing the as-deposited devices with a RTP at different conditions. Voltage, TEM, HR-TEM and EDX measurements are performed to examine the effect of the annealing process on the CdTe layer.

In Chapter 6, to eliminate the bubble, blister or void formation in the CdTe layer, Kr and Ne gases are explored as the working gas during the deposition of the CdTe layer. In order to examine the $CdCl_2$ treated films after depositing with different gases, HR-TEM and other characterization methods are used.

In Chapter 7, a thin film CdS/CdTe solar cell deposited by pulsed DC magnetron sputtering with Xe as the working gas is examined demonstrating that it results in surface blister and void free films.

Chapter 8 summarises the thesis and provides suggestions for future work.

CHAPTER II

2. Magnetron Sputtering for PV

Pulsed DC power is widely used for sputter deposition of metal and dielectric thin films. Dielectric thin films such as metal-oxides are usually deposited by reactive sputtering. However, pulsed DC magnetron sputtering has not been previously used for thin film CdTe solar cell deposition. This chapter explains the advantages of using this power source over RF sputtering. Then, the methodology of the deposition process and annealing and $CdCl_2$ treatment processes are introduced. The characterisation methods are explained for the electrical and microstructural analysis.

2.1. Introducing Pulsed DC

Pulsed DC enables sputtering of dielectric and insulating compounds, which is impossible with DC power. The main advantage of this system is that it prevents arcs with voltage reversal. A patent on the voltage reversal concept to prevent arcing was

registered by Cormia et al. [94]. Drummond [95] improved the concept to enable its industrial use. It is known that pulsed DC magnetron sputtering improves the microstructure of the deposited films [96]. This deposition technique improves the optical coatings due to increased deposition energy and the incorporation of surface diffusion during the 'off' part of the cycle [97]. Pulsed DC magnetron sputtering technology has simplified the deposition of semi-insulating materials. This technology offers commercially attractive deposition rates and system design issues are also simplified [98] .

2.1.1. Advantages over Radio-Frequency sputtering

Until recently magnetron sputtering was exclusively carried out using DC and RF power sources. RF sputtering is used since it is suitable for the deposition of dielectric thin films. The drawback of the method is its limited deposition rate due to its low duty cycle and high deposition pressure. [96], [99], [100] In pulsed DC, deposition rate depends on the power delivered to the plasma during the on-time. In pulsed DC excitation, higher ion energies also reduce the strain in the film and improve the structural quality.

In pulsed DC, positive charges on the surface of a dielectric layer on the target surface are the main reason of arcing. These positive charges accumulate during every on-time pulse while ions bombard the surface of the target [98]. These positive charges are neutralized in the off phase of the pulse.

Pulsed DC provides high deposition rates, which are comparable with evaporation techniques. Pulsed DC has an advanced arcing suppression technology which improves the film quality. It is also compatible with some resistive, dielectric targets and reactive sputtering. [100]–[102]

2.2. Deposition of CdTe with Pulsed DC Magnetron Sputtering

This section describes the development of pulsed DC magnetron sputtering, a high rate deposition method, to deposit thin film CdS/CdTe solar cells. Thin film CdS/CdTe solar cells are deposited in a superstrate configuration as shown in Figure 2-1. The NSG TEC10 fluorine doped tin oxide (FTO) coated glass substrates were obtained from Pilkington NSG Group. FTO is a transparent conducting oxide (TCO) which is used as a front side electrode. The thickness of the substrates is 3.2 mm and the sheet resistance is 10 ohm/square. [103]

Lisco [104] studied the deposition of a CdS layer with pulsed DC magnetron sputtering. Lisco optimised the deposition conditions for CdS layer deposition. This thesis will present the way to optimise the process conditions for the deposition of CdTe absorber layer using pulsed DC magnetron sputtering. A stable back contact is required to obtain an efficient device.

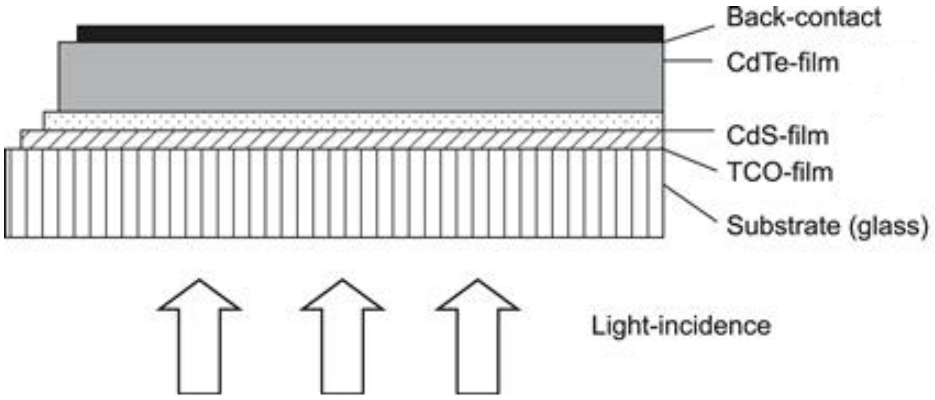


Figure 2-1 Thin film CdS/CdTe solar cell in superstrate configuration [105]

The PV Solar sputtering system is shown in Figure 2-2a. It has four circular magnetrons with 150 mm diameter mounted vertically around a chamber and there is a load lock to allow loading of the substrates. Figure 2-2b indicates the CdTe target (99.99% pure, Testbourne) used for the sputtering process. In Figure 2-2c, a schematic of the substrate holder is shown. The substrates are mounted vertically on a rotating carrier for uniform coating in the horizontal direction. Six substrates can be placed on the rotating carrier and the substrate size used is typically 5 x 5 cm. The distance between the target and the substrate is ~10 cm. The pulsed DC magnetron sputtering (PV Solar) system has been used to deposit CdS and CdTe layers on Pilkington TEC10 glass substrates.

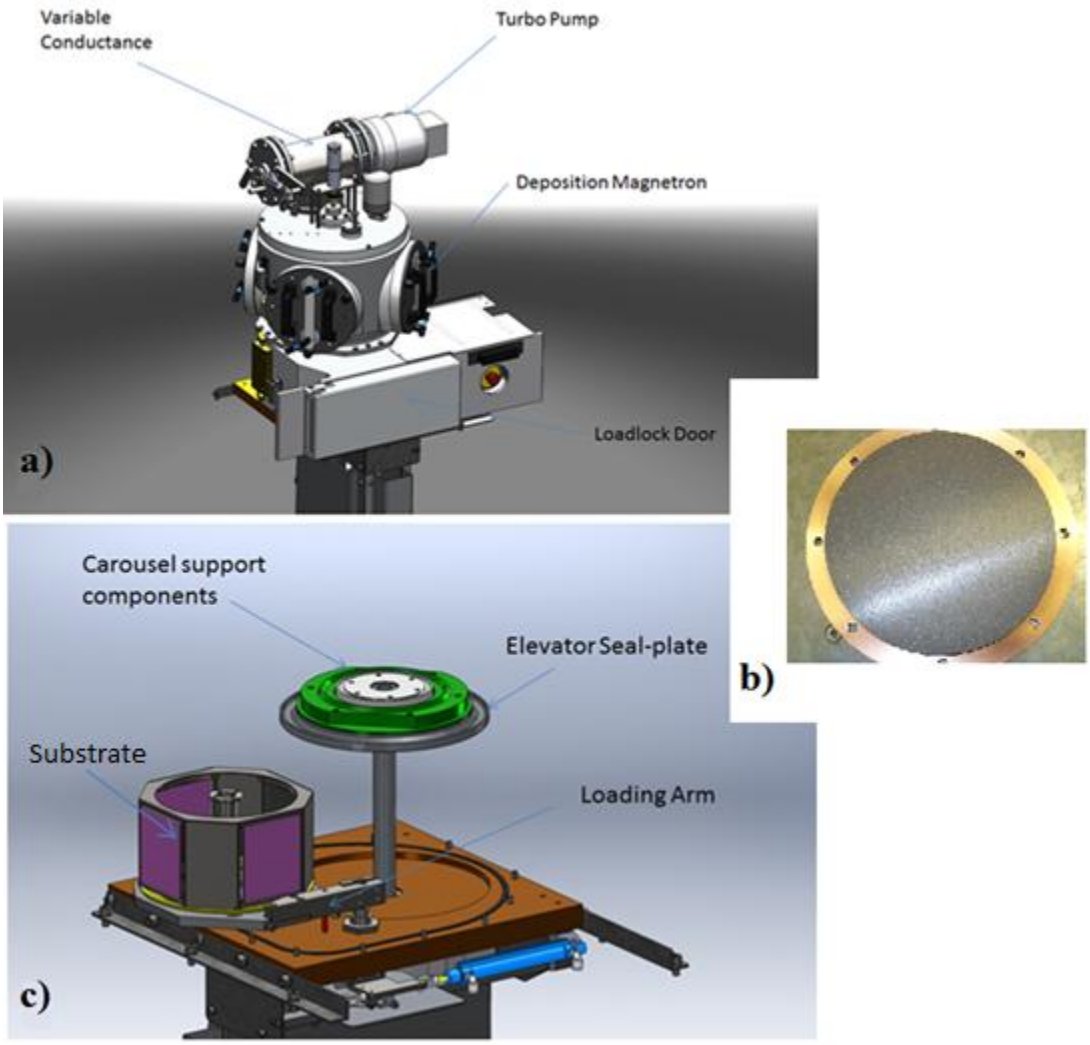


Figure 2-2 a) A schematic diagram of the 'PV Solar' sputtering system (Power Vision Ltd., Crewe UK) used for thin film CdS/CdTe solar cell deposition, b) CdTe target and c) loading the substrate carrier

The pumping system contains a turbomolecular pump (Edwards nEXT300S) backed by a rotary pump to evacuate the main chamber to a lower pressure level. There are two vacuum chambers; a main chamber and a smaller load lock chamber in the PV Solar. The load lock enables unloading the samples into the deposition chamber and it enables faster loading. It is possible to deposit thin films with rotation at ~120 rpm

in the horizontal direction which provides excellent uniformity. To achieve uniformity in the vertical direction, disposable masks are mounted in front of the magnetron target. It is also possible to deposit films without rotation. A 5 kW pulsed DC power supply (Advanced Energy, Inc., Pinnacle Plus 5 kW) was used to form the magnetron plasma required for the sputtering. Water cooling of the magnetron target is required to prevent overheating.

Figure 2-3 shows the basic magnetic design using magnets and soft iron, and the balanced and unbalanced magnetic field patterns. In balanced magnetrons, the central and outer magnets have equal strength. In unbalanced magnetrons, either some of the field lines from the central pole does not pass into outer ring (type I) or some do not pass into the central magnet from the outer magnet (type II). [106] When using unbalanced magnetrons more electrons are lost to the plasma. This increases the plasma length which also provides high substrate current. Moreover, unbalanced magnetrons can assist the production of dense and high quality coatings. [107]–[110]

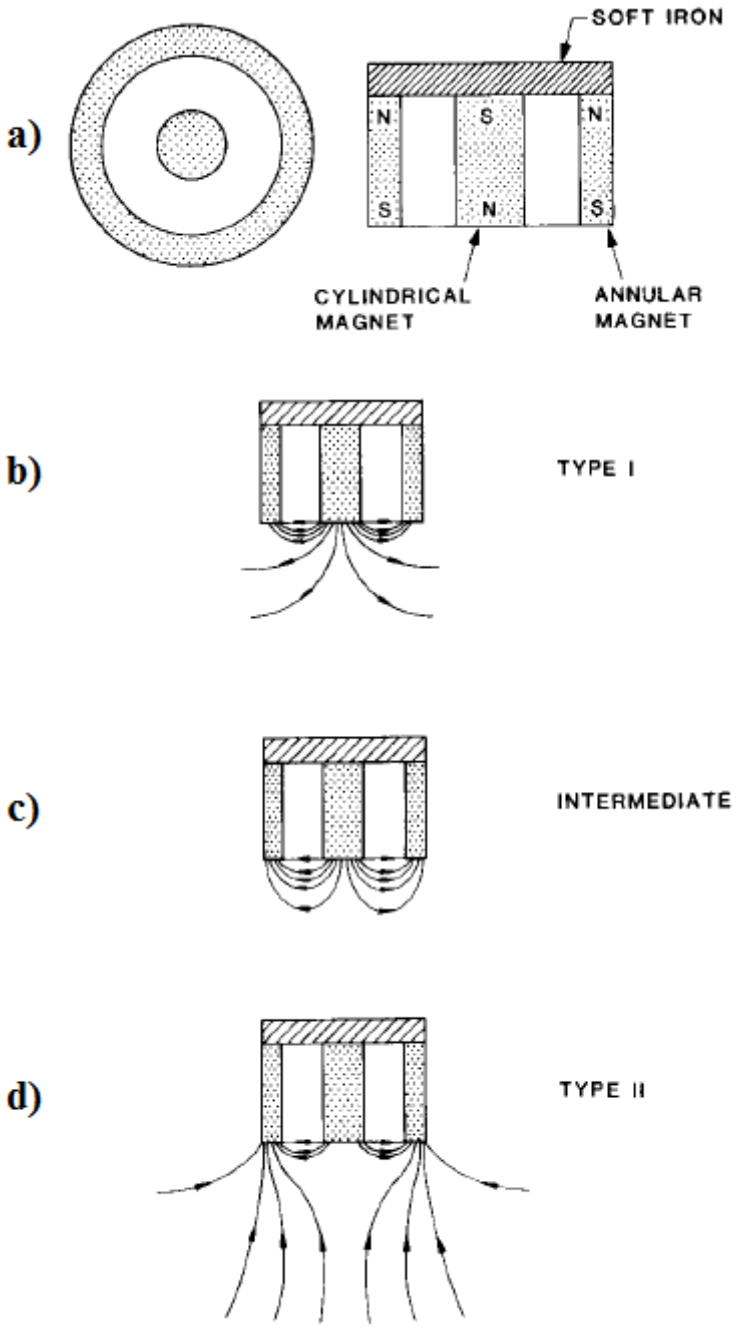


Figure 2-3 a) Basic magnetic design, b) type I unbalanced, c) balanced, d) type II unbalanced magnetic field patterns [106]

High deposition rates are achievable with this sputtering strategy. The pulsing frequency is in the range from 150 up to 350 kHz. The initial pressure is around 1 x

10^{-5} mbar. The deposition of CdS and CdTe layers was carried out using Ar as the working gas through a mass flow controller (MFC-MKS 1179A) rated at 100 sccm and the pressure was fixed to ~3.3 µbar. The voltage on the target is ~800 V during the sputtering process. The substrate temperature can be increased up to 450 °C if the substrate is stationary and 250 °C if the substrate is rotating. The thickness of the layer is controlled by deposition time. [111]

A solution of isopropanol (IPA) and de-ionised (DI) water (1:10) was prepared and the substrates were cleaned for 60 minutes (min) at 60 °C using an ultrasonic bath. This was followed by an ultrasonic bath in DI water for 5 min at 60 °C. Then, a Glen100-P AE Advanced Energy plasma treatment reactor was used for the plasma cleaning process (with Ar/nitrogen (N_2) for 5 min). The deposition of CdS and CdTe layers was performed in an Ar environment, at 250 °C with rotation or at 450 °C without rotation. A 150 nm thick layer of CdS and a 1-2 µm layer of CdTe were deposited sequentially without breaking the vacuum. DC sputtering causes arcing mainly on the surface of the target. To prevent this issue, the pulsed DC magnetron sputtering system is designed to deposit dielectric films [98]. A magnetron is driven by a pulsed DC voltage; biased at 300-800 V. Switching the voltage prevents arcing [112]. Moreover, the films deposited by pulsed DC magnetron sputtering have improved microstructure and it is possible to deposit optical quality coatings due to increased deposition energy. The deposition energy is determined by the induced voltage on the substrate holder. A high flux of relatively low energy (<100 eV) ions is ideal to deposit dense films [96], [97].

2.3. $CdCl_2$ Activation Process and Pre-annealing

2.3.1. $CdCl_2$ Activation Process

The $CdCl_2$ activation treatment is a key process to improve the electrical and structural characteristics of thin film CdTe solar cells. This activation process has been used for thin film CdTe devices since 1985 [113]. Wet treatment with solutions and vapour process are the main methods for this activation process [32]. The $CdCl_2$ treatment also removes defects (such as stacking faults), passivates GBs, and causes grain growth by recrystallisation [68], [84]–[87].

In this study, the $CdCl_2$ treatment has been performed with thermal evaporation, wet chemical treatment, and vapour deposition in a tube furnace. Each process was separately optimised, and the results are compared.

2.3.1.1. Thermal Evaporator

An Edwards E306 thermal evaporator (shown in Figure 2-4) has been used for the $CdCl_2$ activation process. The $CdCl_2$ beads (anhydrous, −10 mesh, 99.999%, Sigma-Aldrich) were placed in a crucible and loaded into the chamber. The substrate was loaded onto the target plate. A shutter was used to control the thickness of the $CdCl_2$ deposited on the substrate. The system has a rotary backing pump and an oil diffusion high vacuum pump. The chamber pressure pumped down to $7x10^{-3}$ mbar with the mechanical pump and then the high vacuum pump pumped down to 10^{-5} mbar. A quartz crystal microbalance detector was used to monitor the thickness of the $CdCl_2$ layer. Water cooling is required to prevent overheating.

A range of thicknesses from 50 nm to 400 nm of $CdCl_2$ layer was deposited on thin film CdTe devices. The deposition time was between 5 min to 10 min. The as-deposited thin film CdTe solar cells were then placed on a hot plate. The devices were annealed for 1 min to 20 min between 370 °C and 400 °C. After the annealing process, the substrates were cleaned with DI water and IPA.

Figure 2-4 Edwards E306 thermal evaporator

2.3.1.2. Wet Chemical Treatment

Another method for the $CdCl_2$ treatment involved the preparation of solutions with $CdCl_2$ and methanol. Different concentrations in the range of 0.1% weight (wt.) to

0.5% wt. of $CdCl_2$ in methanol were prepared. The solutions were dropped onto the film surface of the substrates and then they were placed on a hot plate. Thin film CdTe solar cells were annealed for 1 min to 20 min. The annealing temperature was between 370 °C and 400 °C. After the annealing process, the substrates were cleaned with DI water and IPA.

2.3.1.3. Vapour deposition in a tube furnace

The tube furnace system used for the $CdCl_2$ activation process is shown schematically in Figure 2-5. Thin film CdTe solar cells were loaded into a tube furnace which was vacuum evacuated. Pre-sputtered CdTe solar cells were placed above ~0.5 g – 1 g $CdCl_2$ powder (99.99% trace metal basis, Sigma-Aldrich) loaded in a graphite box and introduced into the tube reactor. The sample holder consists of a bottom box and a top plate. The box was filled with $CdCl_2$ powder. The top plate on the box is used for uniform substrate heating. The system was sealed and the process was placed under vacuum at 50-100 mbar. The device and the $CdCl_2$ were heated using infra-red (IR) lamps and kept at constant temperature. During the activation process, the substrate holder was heated uniformly and $CdCl_2$ vapour was formed. The vapour diffuses into the substrate and activates it. The CdTe devices were treated between 370 °C and 408 °C for 6 min to 30 min to optimize the process. Following the $CdCl_2$ treatment, the CdTe solar cells were rinsed into a dedicated beaker using DI water and dried using compressed dry air (CDA).

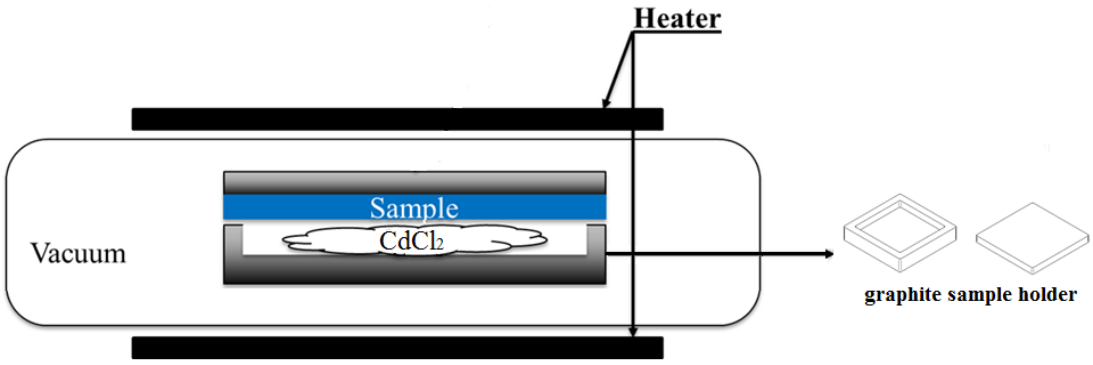


Figure 2-5 A schematic of the tube furnace system used for $CdCl_2$ treatment

2.3.2. Annealing with Rapid Thermal Processing

The $CdCl_2$ activation process is an essential step to improve the performance of the magnetron sputtered CdTe solar cells however this process also causes catastrophic damage to the CdTe devices. It is not clear if the blister formation or delamination issues in the CdTe device are a result of the annealing process or the chemical effect of using $CdCl_2$. To address this issue, RTP annealing was performed without the presence of chlorine (Cl) on as-deposited CdTe solar cells. IR lamps were used to anneal the samples in a tube furnace, whereas RTP system contains a halogen lamp for the annealing process. RTP system has a better temperature controller with +/-1 ˚C accuracy. This system also provides higher heating/cooling rates. The pressure during the annealing process with the tube furnace is ~50 mbar, whereas it can be reduced down to ~10 mbar for the RTP annealing.

Figure 2-6 shows the RTP-1000D4 system which has been used for annealing thin film CdTe solar cells. The system is fitted with a 10 kW halogen lamp to heat the system. The heating/cooling rate and temperature during the annealing process are

controlled by a temperature controller. CdTe devices were placed on the sample holder and both ends of the tube were sealed with flanges. The temperature and heating/cooling rates were pre-set through the temperature controller for the annealing process. [114] RTP provides a fast annealing process. The system enables annealing at high temperatures in short times. It is also quite simple to use the system once the process parameters are set.

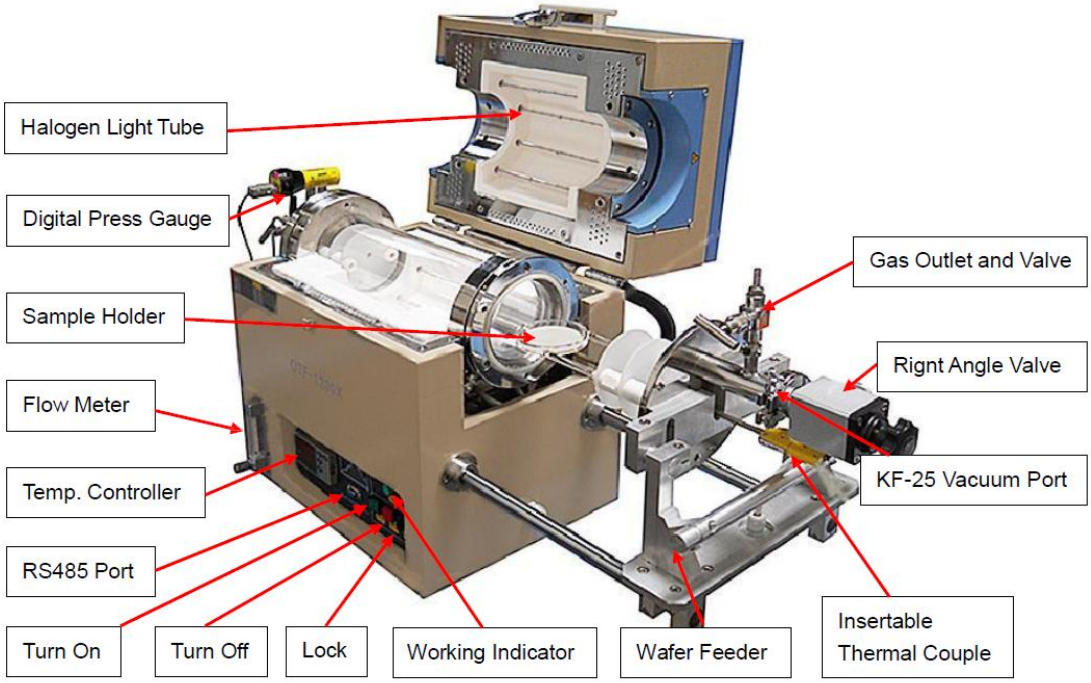


Figure 2-6 A schematic diagram of the rapid thermal processor [114]

2.4. Solar Cell Characterisation

CdS layer deposition with pulsed DC magnetron sputtering was optimised by Lisco [104] at Loughborough University (LU). Therefore, this work is focused on thin film CdTe deposition using pulsed DC magnetron sputtering.

Material, electrical, and microstructural analyses are required to investigate the surface morphology, grain size, and defects within the grains or at the CdS/CdTe interface of CdS/CdTe devices, before and after the $CdCl_2$ activation process. All device thickness and roughness were measured by a profilometer to calculate the deposition rates of the CdTe devices [115]. The devices were placed on an X-Y stage which was moved during the scan. The software "Ambios Technology XP2 Stylus Profiler" was used to scan and obtain the data.

2.4.1. Electrical Characterisation

The primary figure of merit was to measure the V_{OC} of the cells which was performed using a digital multimeter and a light source, after the deposition and annealing process. This method was used as a performance indicator to monitor the increase in the V_{OC}.

Then a Quorum Q150T ES sputter coater was used to deposit ~50 nm thick gold back contact on thin film CdS/CdTe devices. A Newport solar simulator, with a 1000 W Xe lamp and an AM1.5g filter, was used to measure the *Jsc*, open circuit voltage (*Voc*), *FF*, and cell efficiency (η). An electrometer (Keithley 4-point probe) was used for the J-V measurements. A Sciencetech Simulator software recorded the J-V curve measurements.

2.4.2. Optical Characterisation

Coherence correlation interferometry (CCI) is a scanning white light interferometry (SWLI) technique used for thin film thickness measurements using the helical

complex field (HCF) function [116]–[118]. A SWLI system is shown in Figure 2-7. The CCI (Taylor Hobson) is a non-contacting measurement method. Film uniformity and void detection can also be performed using the CCI technique [119]. Taylsurf CCI software was used to acquire the data.

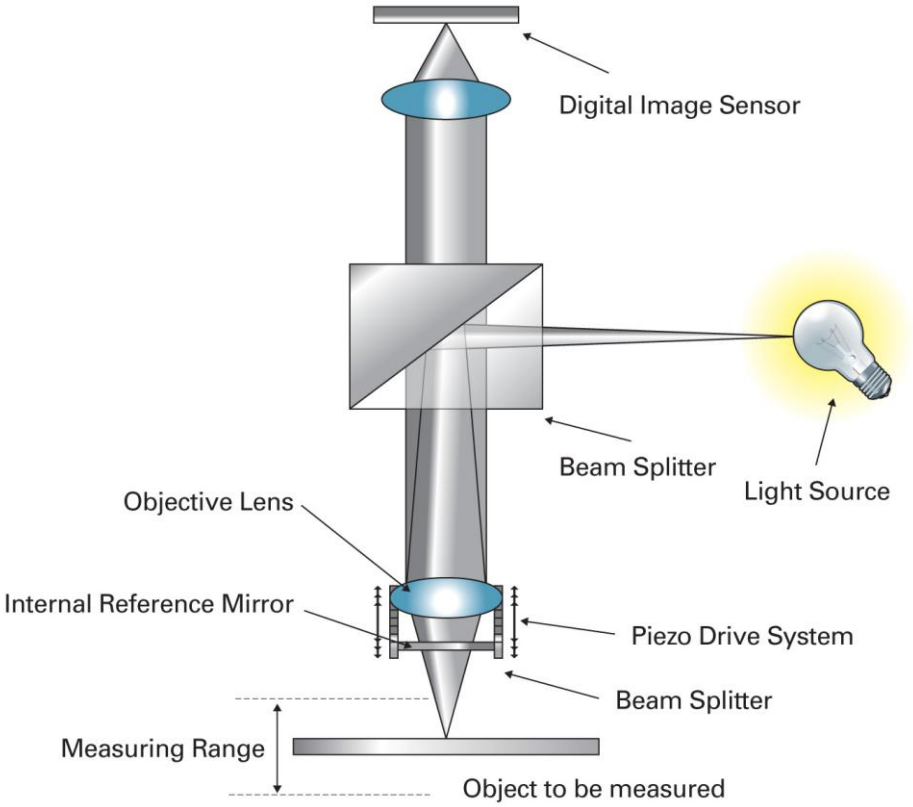


Figure 2-7 A schematic of a scanning white light interferometry [120]

2.4.3. Structural Characterisation

2.4.3.1. X-Ray Diffraction (XRD) Measurements

In this study, XRD measurements were performed by Chen and the data used to determine the strain of the thin film CdS/CdTe solar cells. Film strain can affect the

band gap and the transmission edge, so the transmission edge was measured with the spectrophotometer.

A Varian Cary 5000 UV-Vis-NIR spectrophotometer was used for this purpose, shown in Figure 2-8. XRD data was collected with a Bruker D2 Phaser benchtop. SCAN software was used to obtain the data. The band gap was calculated using the transmission data.

There is an integrating sphere and set of gratings to perform the transmission and reflection measurements in the range from 200 nm to 1400 nm. Absorption of CdTe solar cells was estimated by using the formula:

$$1=R+T+A \qquad (2.1)$$

where R is the reflectance, T is the transmittance and A is the absorption.

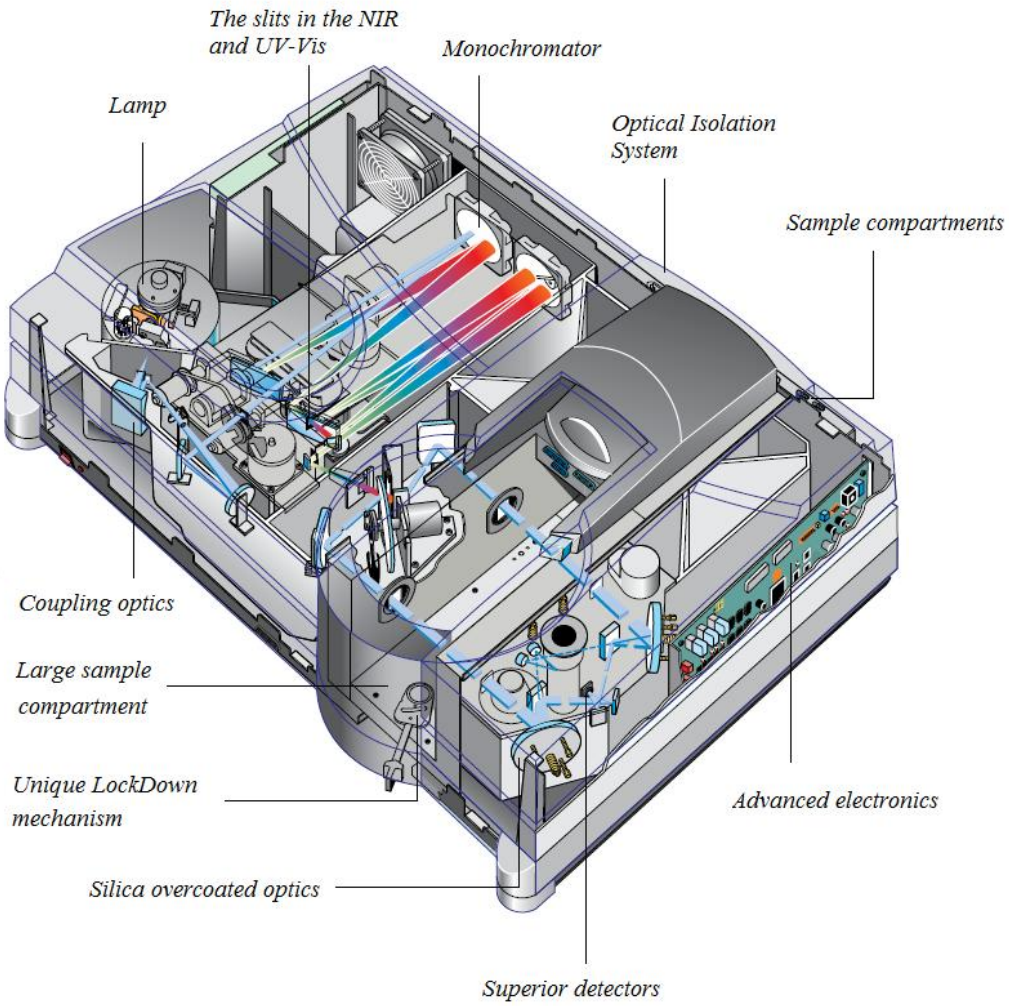


Figure 2-8 A schematic diagram of the spectrophotometer [113]

2.4.3.2. Scanning Electron Microscopy (SEM)

A Leo 1530VP field emission gun scanning electron microscope (FEG-SEM) was used to analyse the surface of the thin film. EDX analysis was carried out in the FEG-SEM to obtain chemical analysis. The acceleration voltage was 20 kV and the aperture size was 60 μm. It is an easy and fast method for grain size measurements however it is also hard to quantify the size of the grains due to the topography of the

CdTe layer in the fracture section. An SEM image of a sputtered CdTe solar cell is shown in Figure 2-9. The grain sizes were between 200 nm and 300 nm.

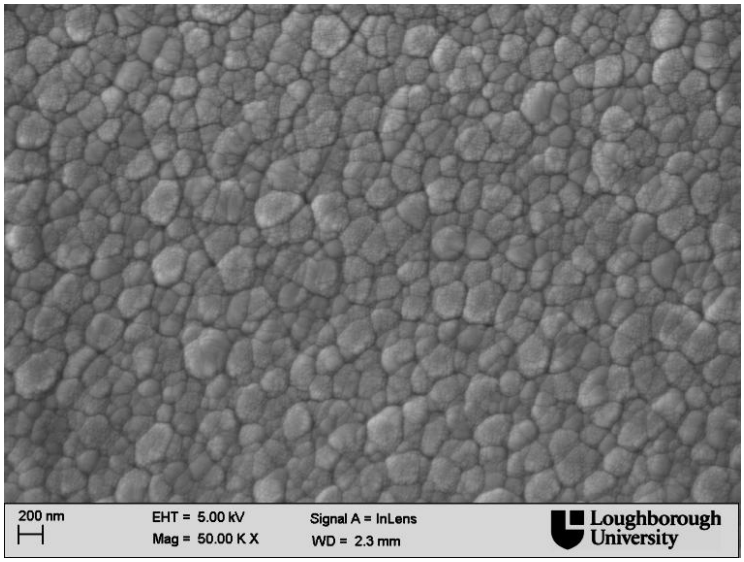


Figure 2-9 SEM image of the surface of a sputtered CdTe solar cell. Typical grain sizes of the sputtered film is 200 nm to 300nm.

2.4.3.3. Transmission Electron Microscopy (TEM)

TEM has been used to determine the composition (with EDX) and nanoscale structure of thin film CdTe devices deposited by pulsed DC magnetron sputtering. These measurements were performed by Abbas. In order to understand the properties of the sputtered materials, it is important to investigate the surface morphology and defects in the films and grain sizes. TEM provides a much clearer view of the grains in the film compared to SEM.

TEM samples were prepared by focused ion beam (FIB) milling using a dual beam FEI Nova 600 Nanolab. For preparing cross-sectional samples through the coating

into the glass superstrate, a standard in situ lift out method has been used. A layer of platinum (Pt) was deposited to determine the surface and homogenize the thinning of the films. TEM was performed using a Jeol JEM 2000FX, with an Oxford Instruments 30 mm^2 EDX detector and a Gatan Erlangshen ES500W digital camera. HR-TEM images were carried out using a FEI Tecnai F20 scanning transmission electron microscopy (STEM) for further investigation of the cell cross-sections. This is a useful technique to analyse the defects within the lattice in the grains. STEM was also carried out in a FEI Tecnai F20 STEM, with Gatan bright and dark field STEM detectors, high angle annular dark field (HAADF) STEM detector, Gatan Enfina electron energy loss spectrometer, and an Oxford Instruments X-max N80 TLE silicon drift detector (SDD) EDX detector. The detector was used to collect elemental distribution maps. These maps were collected into a single frame using long dwelling times and a small condenser aperture, to minimize drift and beam spread during collection.

CHAPTER III

3. Strain Analysis of thin film CdTe solar cells deposited by pulsed DC magnetron sputtering

3.1. Introduction

Due to the high energy of bombarding ions during deposition, sputtered films are susceptible to strain and stress. The substrate temperature and the Ar working gas deposition pressure are important parameters to control the film strain. Higher gas pressures will reduce the energy of deposition due to collisions with gas atoms between the target and substrate. This will reduce the strain in the film.

Grain size has also an impact on the film strain. Smaller grains in CdTe layer will result in more grains and more GBs which will cause more defects or stacking faults

on thin films. The film strain can also be responsible for the blistering, void formation and delamination of the films after the $CdCl_2$ activation process [121]. This can also lead to catastrophic damage at the CdS/CdTe interface during the $CdCl_2$ activation process.

Thin film CdTe solar cells were deposited using pulsed DC magnetron sputtering, this was followed by the $CdCl_2$ activation process to improve the cell performance and structure. However, delamination of the solar cells occurred after the treatment. In Figure 3-1, SEM images of a CdS/CdTe solar cell after the $CdCl_2$ treatment shows the delamination occurred at the CdS/CdTe junction. Moreover, exfoliation occurred at some of the surface blisters. Delamination could be caused by compressive stress in the sputter-deposited thin films. Therefore, a series of experiments were conducted to minimise stress and eliminate this as a possible cause of delamination.

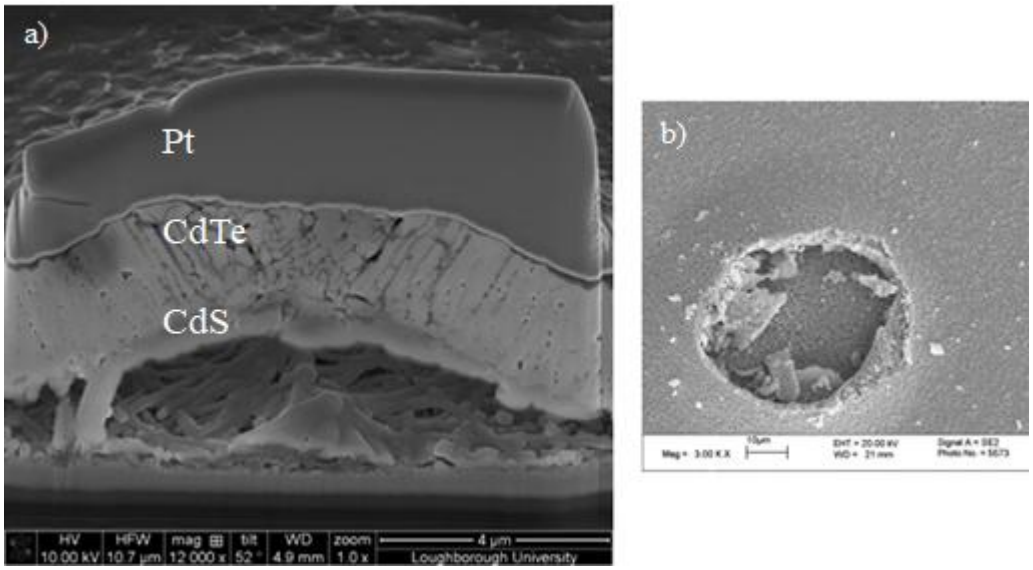


Figure 3-1 SEM cross-sections of a sputtered device following activation with $CdCl_2$ a) delamination occurrs at the CdS/CdTe junction, b) exfoliation occurs at the surface blister

One of the first works on thin film stress was done by Stoney [122]. The Stoney equation is still used to determine the stress in thin films from the film and substrate thickness and the elastic properties of the substrate [123], [124]. Finegan and Hoffman [125] did research on evaporated iron (Fe) films on microscope cover glasses in 1959. In 1972, Doljack and Hoffman [126], [127] published their research on intrinsic stress in vapour-deposited nickel (Ni) films on a Si substrate, where Hoffman found that the stress could be generated at the GBs in the film. Abermann et al. [128] have proposed an alternative method on stress measurement. In the following years, several studies and reviews have been conducted on the stress analysis of mainly sputtered thin films [129]–[134]. Seel et al. [135] presented a model to predict the kinetics of stress during the deposition of thin films. Doerner and Nix [136] have calculated the Young's modulus and worked on the plastic and elastic properties of thin films. They showed that hardness obtained from the loading

curve depends on strain rate [136]. In 2001, Freund and Chason [137] have proposed a model for the process on the elastic solids (with cohesion) contact theory to estimate the stress.

In this chapter, all process parameters including deposition temperature and Ar gas flows are analysed and optimised to minimize the strain in the deposited films. Furthermore, post annealing was investigated as a way to reduce the strain.

3.2. Experimental

3.2.1. Pulsed DC Magnetron Sputtering

Table 3-1 Synthesis conditions for CdTe deposition using pulsed DC magnetron sputtering and post-deposition annealing parameters

CdTe deposition conditions	
Deposition rate (nm/s)	1.6-2.8
CdTe thickness (µm)	1-2
Substrate temperature (°C)	RT-400
Magnetron working gas	Ar
Flow rate (sccm)	20-100
Pressure (µbar)	1.9- 8.1
Post-deposition annealing on a hot plate	
Annealing time (min)	0-30
Annealing temperature (°C)	300-400

3.2.2. Characterisation

TEM was used to investigate the microstructure of thin film CdTe solar cells deposited using pulsed DC magnetron sputtering. The grain size and crystalline

structure of the CdTe solar cells were obtained from the TEM images. XRD was used to determine the strain and stress of the CdS/CdTe devices and verify the crystal structure. A Bruker D2 PHASER was used to collect the XRD data of the CdTe solar cells. The X-ray source was set at 30 kV and 10 mA. The scanning range was 20° ~ 90° (*2θ*). The step size was 0.02° and the speed was 0.1 s/step. To collect detailed data for the (111) peak analysis during the XRD experiment, the 23.2° ~ 24.2° (*2θ*) range was scanned with a smaller step size of 0.01° and a slower speed of 1 s/step.

To assess the stress within the film, the location of the (111) peak in the XRD spectra was monitored over time. The strain leads to a change in the inter-planar spacing of the lattice planes, and this change causes a shift in the diffraction pattern. The strain and stress in the CdTe device can be calculated by monitoring this shift of the peak in the XRD spectra [138]. The lattice constant d was calculated using:

$$n\lambda = 2d \sin\theta \qquad (3.1)$$

where n is an integer, λ is the wavelength of the X-rays, and 2θ is the diffraction angle.

Strain was calculated by comparing the bulk d_0 spacing with measured d:

$$\varepsilon = \frac{d-d_0}{d_0} \qquad (3.2)$$

CdTe devices for the TEM analysis were prepared by FIB milling using a dual beam FEI Nova 600 Nanolab. HR-TEM images were obtained using a FEI Tecnai F20 for further analysis of the cell cross-sections. A Varian 5000 UV-Vis spectrophotometer

was used to determine the transmission edge and band gap of the deposited CdTe devices. The data was collected for wavelengths in the range between 200 nm and 1400 nm. The band gap was calculated using the transmission data.

3.3. Results

Two sets of experiments have been performed to investigate the effect of different substrate temperatures and to investigate the influence of different Ar gas flow rates on the stress formation in the as-deposited thin film CdTe devices. The Ar gas flow was set between 20 sccm and 100 sccm and the temperature kept constant. The substrate carrier was rotated during the depositions. The Ar gas flow was set to 50 sccm and the substrate temperature was varied from RT up to 400 °C. Figure 3-2 shows an XRD spectrum of an as-deposited sputtered thin film CdTe device. The CdTe devices showed the cubic phase with a (111) orientation.

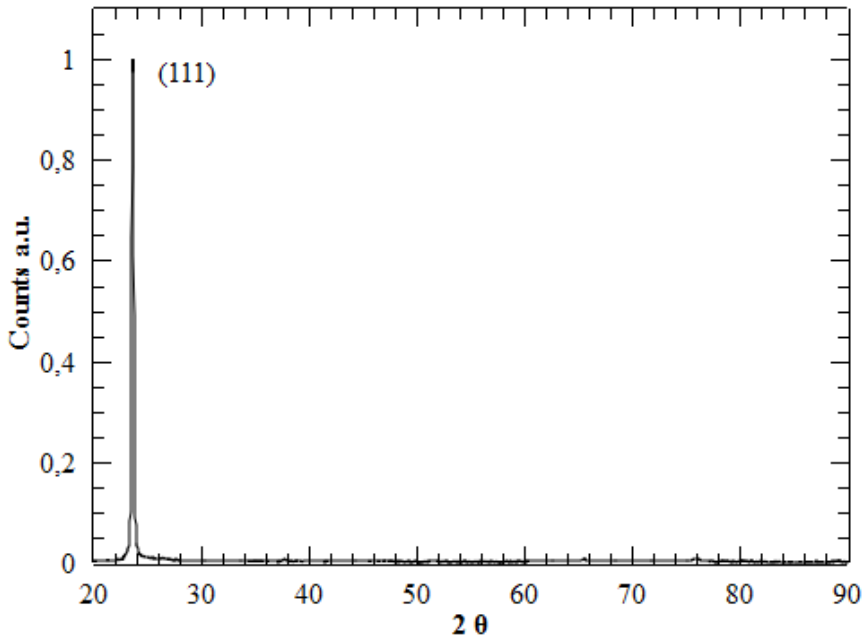


Figure 3-2 XRD spectrum of a thin film CdTe solar cell deposited at RT using 50 sccm Ar magnetron working gas

3.3.1. Argon gas flow

The deposition rate of the CdTe solar cells was calculated by measuring thin film thickness using a stylus profilometer. CdTe film depositions were performed using different gas flows to investigate the effect of the process pressure on the deposited CdTe devices. Figure 3-3 shows measured static deposition rates. It was observed that increasing the gas flow resulted in a decreased deposition rate. For the CdTe solar cell deposited at 20 sccm of Ar, the deposition rate was measured as 2.4 nm/s, which decreased to 1.7 nm/s at 100 sccm of Ar. Based on this figure, the best deposition rates were produced at lower substrate temperature.

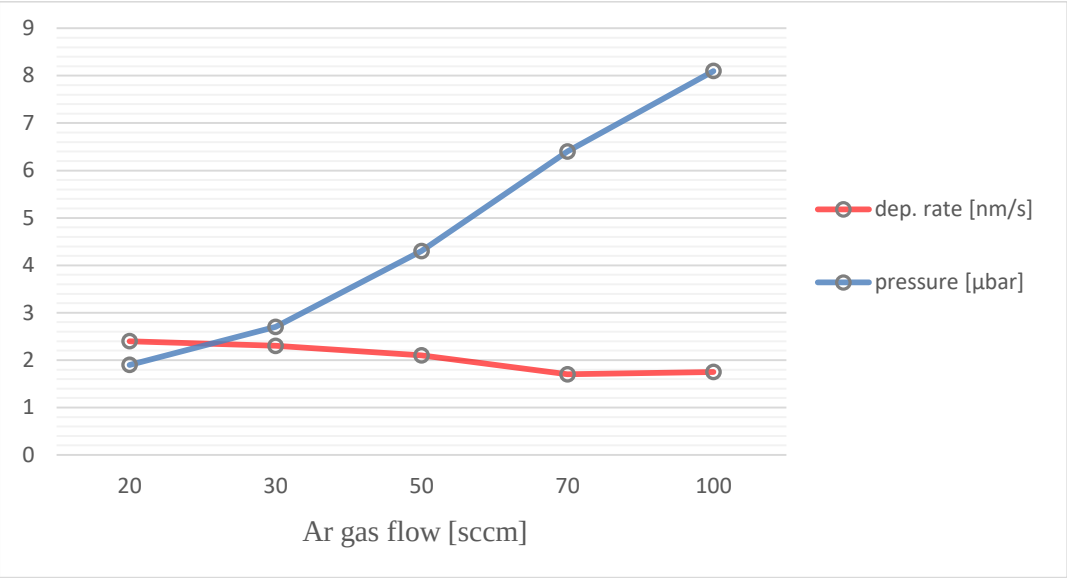


Figure 3-3 Static deposition rates measured for as-deposited thin film CdS/CdTe solar cells sputtered at different Ar flow rates. Substrate temperature was constant during the CdTe deposition.

In the as-deposited material, the parallel line defect structures correspond to high densities of stacking faults. Some types of stacking fault defects (polytype) introduce holes traps into the material which limits photo-generated carrier collection and the cell performance. [139] However, these tetrahedral stacking faults have low energy which causes negligible offset in the valence band and minor disruption in the lattice and band gap potential. Therefore, these defects should be electrically benign.

Figure 3-4 shows the TEM images of device cross sections for 20, 50, 70, and 100 sccm Ar gas flows without substrate heating. The TEM images of cross sections showed a change in the crystalline structure for thin film CdS/CdTe devices deposited with different Ar gas flows. Thin film CdTe solar cell deposited at 20 sccm Ar gas flow rate show a crystalline structure consisting of small crystallites.

The thin film CdTe solar cells deposited at 50 sccm, 70 sccm and 100 sccm Ar gas flow rates show a more distinct columnar grain structure, with a grain diameter of ~100 nm or more, and extend through the entire thickness of the CdTe device. The larger grain size and columnar structure cause lower GB volume and reduce transverse GBs. [140]

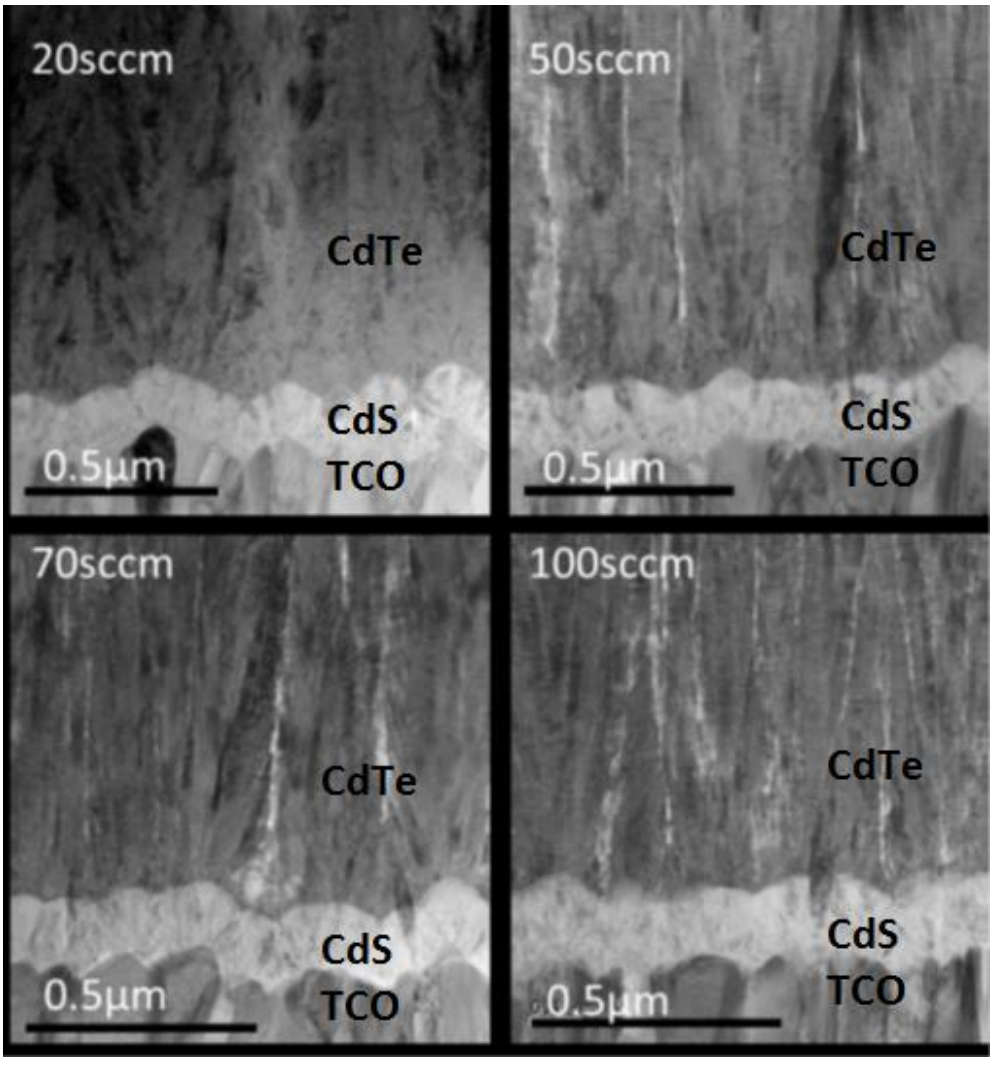


Figure 3-4 TEM cross-section of thin film CdS/CdTe solar cells deposited using different Ar flow rates (20-100 sccm) without substrate heating

XRD measurements were utilised to observe the shift in the Bragg peak with lateral position in the substrate. Depending on the changes in d-spacing, the (111) peak in the X-ray pattern is subject to a shift because of the changes in the internal stress in the substrate. A solar cell deposited by CSS and treated by $CdCl_2$ annealing was used as a baseline. The peak position for this stress free bulk material is indicated for reference as a black dashed line on Figure 3-5. This XRD shows the measurements for thin film CdTe solar cells deposited at different Ar flow rates. The data was used to calculate strain in the film. Compressive stress formation was observed when the peak shift towards lower diffraction angles.

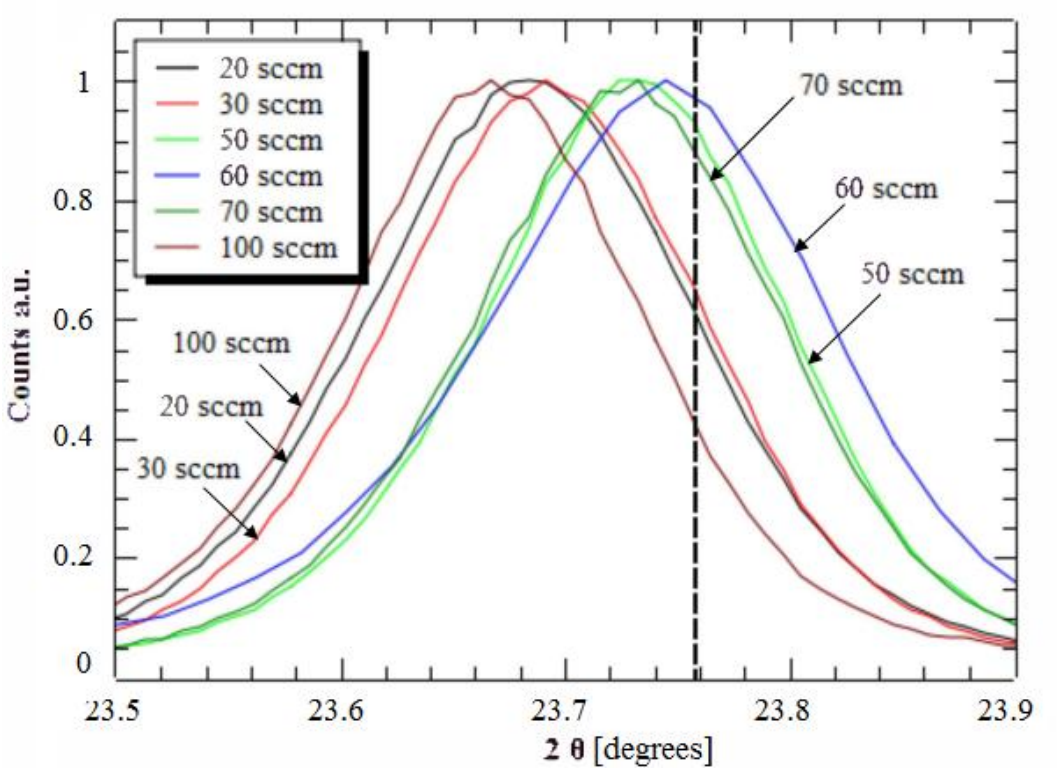


Figure 3-5 XRD spectra showing (111) peak location measured for CdTe films deposited at various Ar gas flow rates. Temperature was kept constant at RT. The black dashed line shows the 2θ value of the stress free bulk CdTe .

The XRD data was collected to calculate the *d* spacing and strain. The results are shown below in Table 3-2.

Table 3-2 Strain of the thin film CdS/CdTe solar cells deposited at RT using different Ar flow rates

Argon (sccm)	20	30	50	60	70	100
Pos. (º2Th.)	23.684	23.692	23.732	23.745	23.732	23.667
Strain	3.09e-3	1.06e-3	1.06e-3	5.45e-4	1.06e-3	3.77e-3

Figure 3-6 shows the strain and pressure measured for CdTe devices at different Ar flow rates. It was observed that at lower and higher gas flow rates, the strain was higher. The reason of higher strain at lower or higher gas flows is the change in the gas pressure which then causes defects in the films. The lowest strain was at 60 sccm Ar.

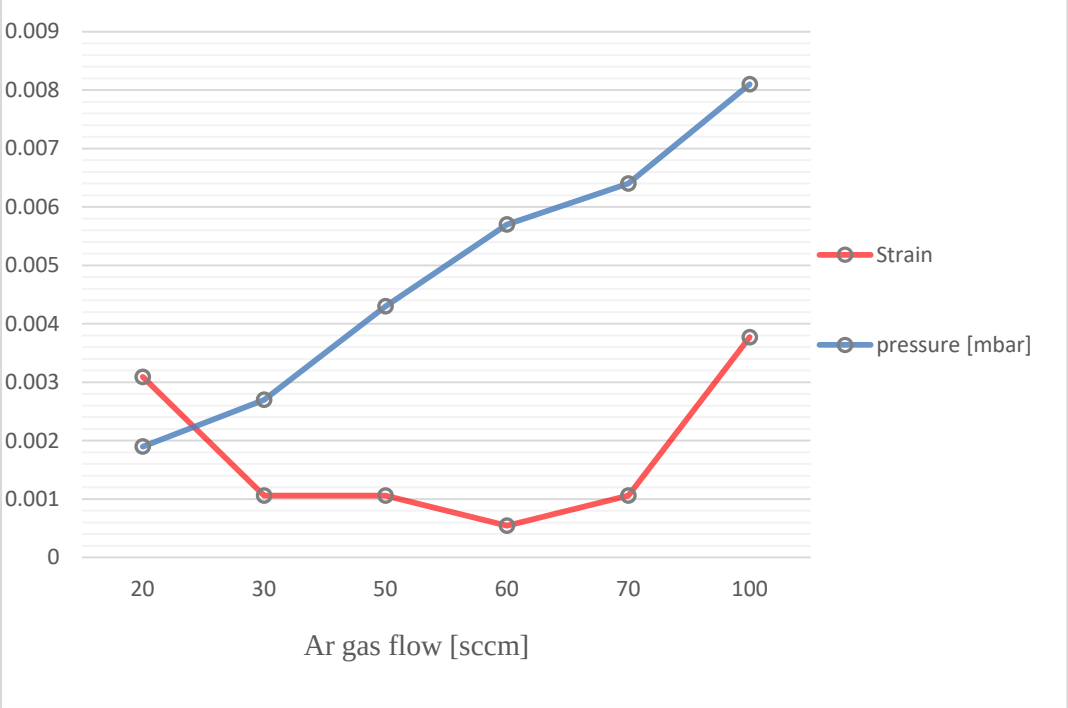


Figure 3-6 Strain and pressure measured for thin film CdS/CdTe solar cells deposited at RT using different Ar flow rates. A minimum occurs at 60 sccm.

The Urbach Equation can be used to determine the band gap energy (*Eg*):

$$\propto = \frac{A(hv-Eg)^p}{hv} \qquad (3.3)$$

where A is a constant, h is the Plank's constant, p is the numerical coefficient and v the frequency [141]. In this case p was 0.5. For the value α=0, the Eg was

determined. In Figure 3-7, $(\alpha hv)^2$ is shown as a function of the band gap at different Ar gas flow rates in the range from 20 to 100 sccm.

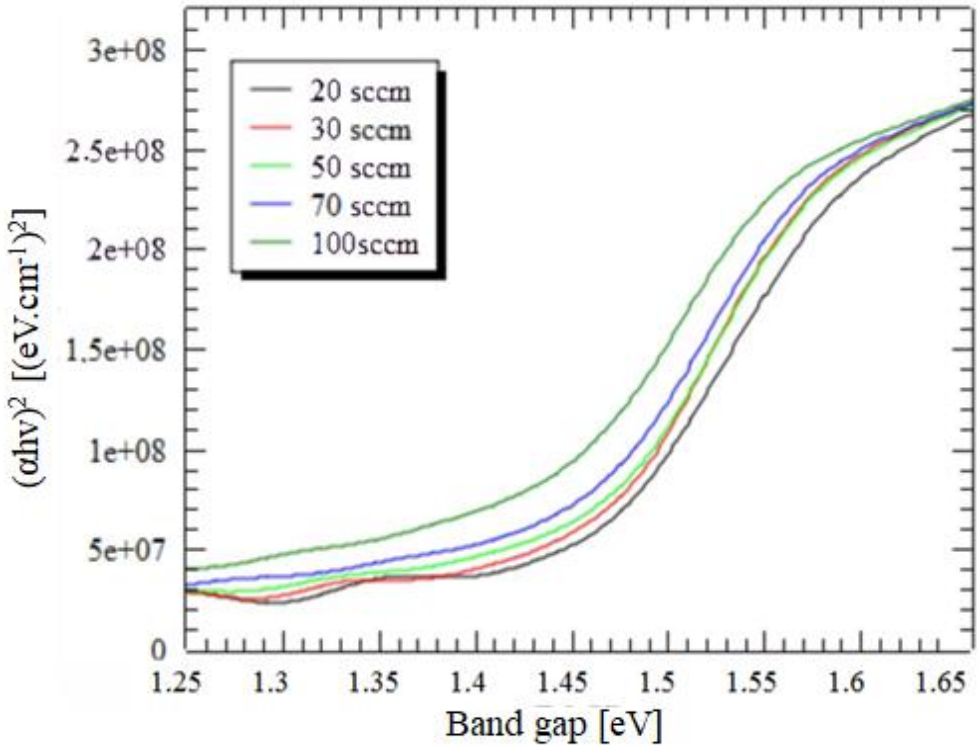


Figure 3-7 Tauc plot, estimated from the $(\alpha hv)^2 = f(hv)$ for thin film CdTe solar cells deposited at RT using various gas flows.

In Figure 3-8, the calculated band gaps for thin films deposited at different Ar gas flow rates are shown. The analysis indicates that with the increase of the Ar gas pressure, the band gap of the deposited CdTe devices decreased. The films deposited at 20 sccm have the highest band gap of 1.425 eV which is close to direct band gap of CdTe (1.5 eV).

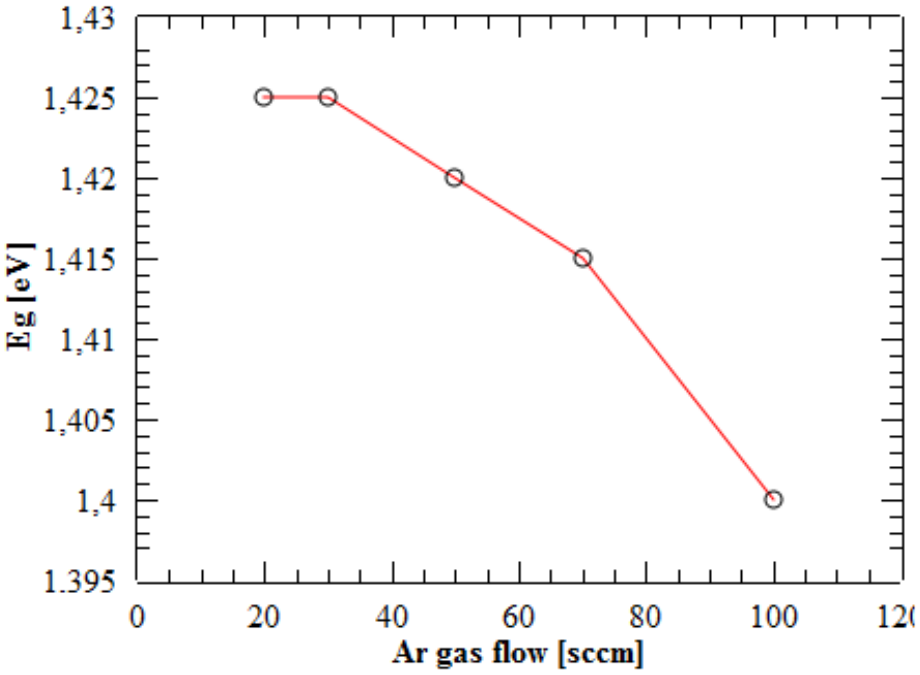


Figure 3-8 The band gap of thin film CdS/CdTe solar cells as a function of the Ar gas flow used during deposition at RT.

3.3.2. Deposition temperature

The effect of the substrate temperature on thin film CdTe solar cells was studied. Samples were deposited between RT of ~30 ºC and 400 ºC. The Ar gas flow was set to 50 sccm during the film deposition. The deposition rates of thin film CdTe solar cells, prepared at various temperatures were calculated from the step height measurements obtained using a stylus profilometer. Figure 3-9 shows the deposition rates measured for films deposited at different substrate temperatures. The deposition rates of CdTe layers at RT, 200 °C, and 400 °C were measured to be 2.8 nm/s, 2 nm/s, and 1.6 nm/s, respectively.

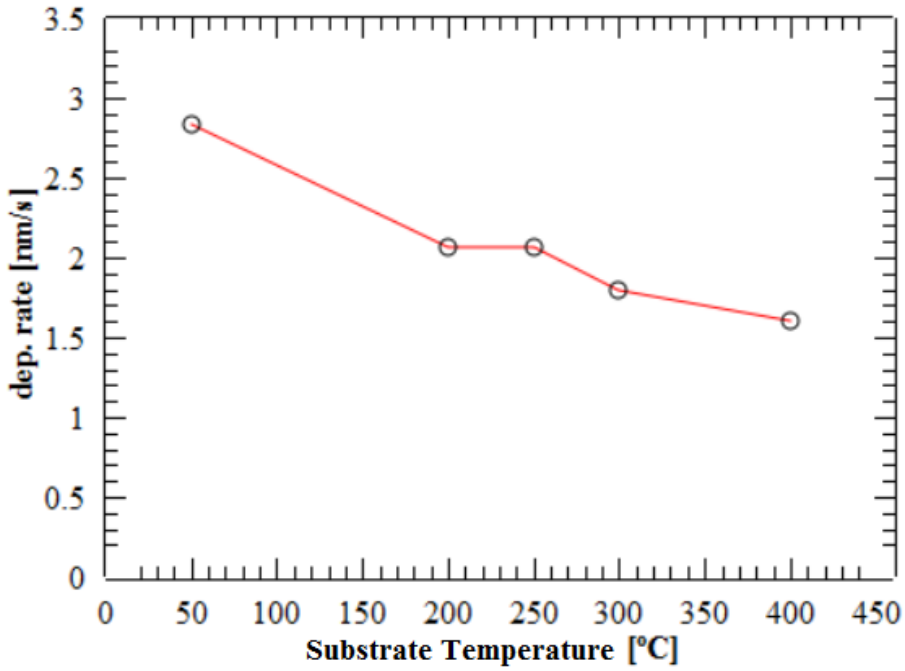


Figure 3-9 Static deposition rates measured for thin film CdTe solar cells deposited at different substrate temperatures using 50 sccm Ar flow rate. The data at 50°C was deposited without substrate heating.

The deposition rate reduced as the substrate temperature increased. Increase in pressure at higher deposition temperatures may be the reason of lower deposition energy and lower deposition rates. Increase in pressure will reduce the mobility of the adatoms with the reduced ion bombardment. The adatom density is affected by desorption and diffusion. A growth model for CdTe is shown in Figure 3-10. Desorption of a Te adatom, diffusion of a Cd-Te pair and two pairs of Cd-Te are shown. It is assumed that growth is limited by desorption of Te. Highest deposition rate was found to be at RT however there were also other parameters considered such as compactness or porosity of the sputtered film.

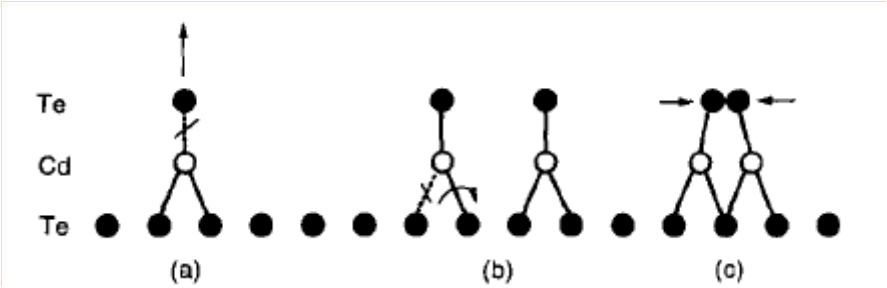


Figure 3-10 CdTe growth model a) desorption of a Te adatom, b) diffusion of a Cd-Te pair, c) Cd-Te pairs meet [142]

TEM images of the material cross-section of thin film CdS/CdTe devices deposited without substrate heating and at 200 °C are presented in Figure 3-11. Both CdTe devices had a columnar grain structure and the grains extend through the sample thickness. The CdTe solar cell deposited without substrate heating showed smaller grains in the range 50 nm to 70 nm diameter. The CdTe device deposited at 200 °C showed a similar grain structure to the device deposited without substrate heating. However, the grain diameters were larger up to 250 nm due to higher substrate temperature during the deposition of CdTe layer. The reason can be explained with the thin film growth theory; nucleation, grain growth, coalescence and formation of the film. [143], [144] At high temperatures, critical radius will increase to form stable nuclei. Grains will have low probability to be nucleated and this will reduce the population density and increase the grain size.

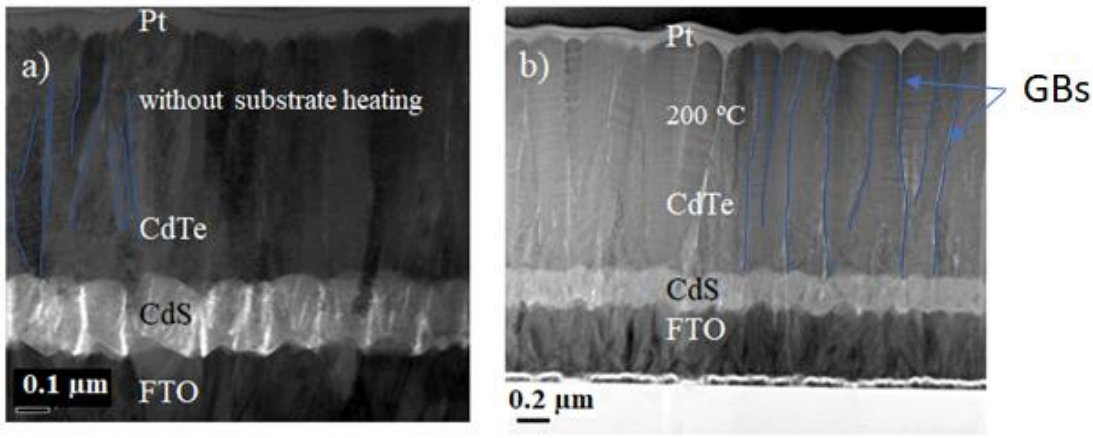


Figure 3-11 TEM images of cross-section of thin film CdS/CdTe solar cells deposited using 50 sccm Ar on to FTO coated glass a) without substrate heating, and b) at 200°C. The films show a structure with columnar grains.

The TEM images of cross sections of thin film CdTe solar cells deposited at 300 ºC and 400 ºC are shown in Figure 3-12. The films show a structure with columnar grains. Increasing the temperature of film deposition has increased the grain size. In the TEM cross-sections of CdTe devices deposited at 300 ºC, the grain size was measured up to ~300 nm, and when deposited at 400 ºC the grain size was measured to be up to ~500 nm.

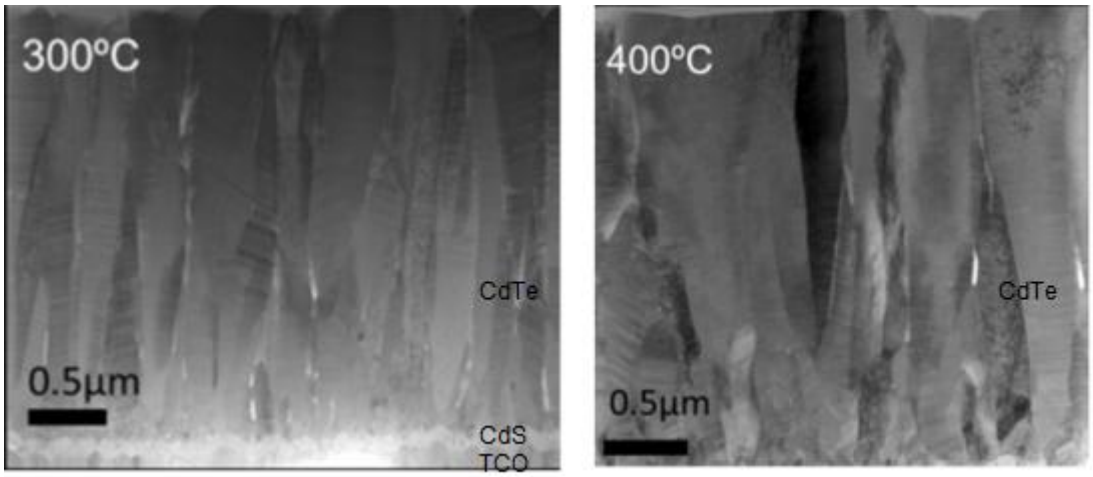


Figure 3-12 TEM images of cross-section of CdS/CdTe solar cells deposited at 300 ºC and 400 ºC using 50 sccm Ar gas flow.

EDX analysis of the as-deposited CdTe device is shown in Figure 3-13. 47.9 atomic (at)% Cd and 48.1 at% of Te were observed in the CdTe layer. The EDX measurement shows the presence of 1.9 at% to 4 at% of Ar in the as-deposited film. There is higher concentration of Ar observed close to the surface. This may be due to deposition of the CdTe layer at a temperature of 200℃ that Ar ions won't be trapped. There was only about 0.1 at% Ar in the CdS layer.

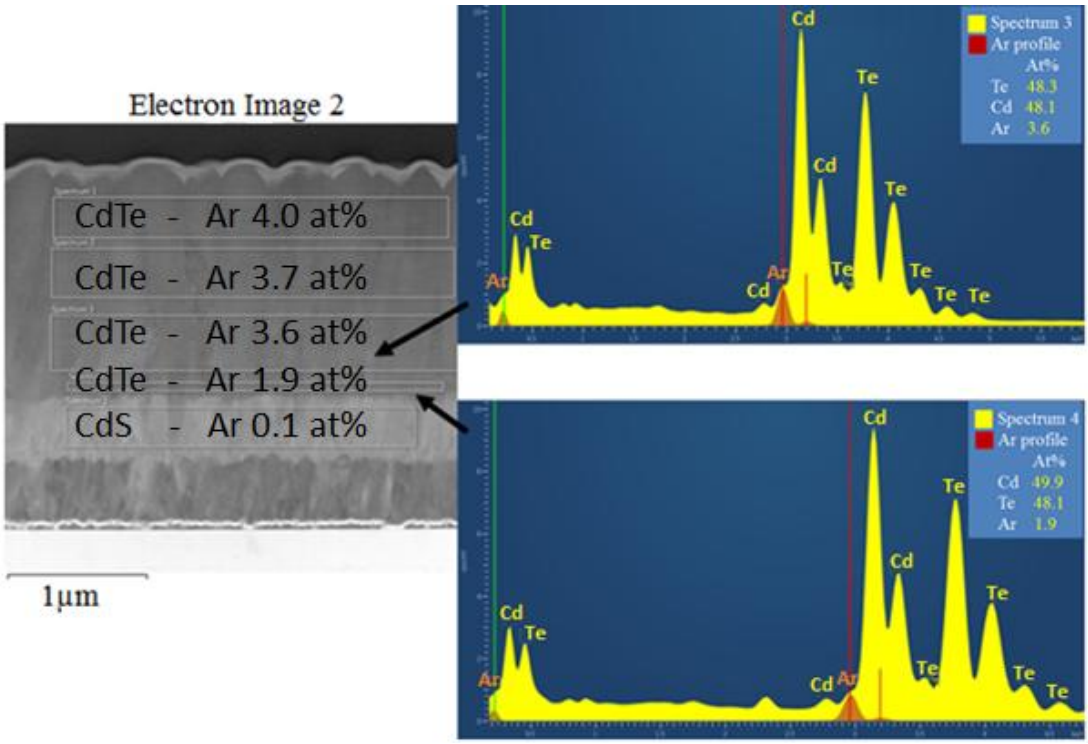


Figure 3-13 EDX spectra of as-deposited thin film CdS/CdTe solar cell using 50 sccm Ar working gas at 200 ºC.

Figure 3-14 shows atomic scale resolution HR-TEM images of thin film CdS/CdTe solar cells deposited by pulsed DC magnetron sputtering. The images show the defects in the as-deposited CdTe solar cells. These images show there is high density of stacking faults in thin film CdTe solar cell deposited without substrate heating. There is less defect density observed in the solar cell deposited at 200 ºC.

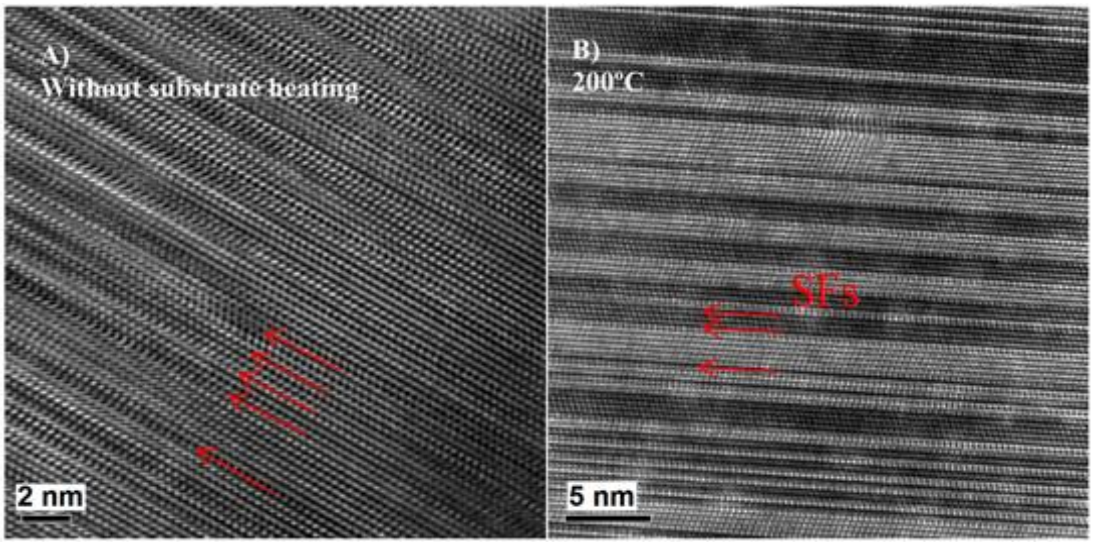


Figure 3-14 HR-TEM images of cross-section of thin film CdS/CdTe solar cells deposited using 50 sccm Ar a) without substrate heating, b) at 200°C. High density of stacking faults were observed on the sample deposited at RT.

XRD measurements were used to calculate the strain in the thin film.

Figure 3-15 shows the XRD data measured for thin film CdTe solar cells deposited at different substrate temperatures. The peak (111) position for stress-free bulk material is marked as a dashed line for reference. For thin film CdTe solar cells deposited without substrate heating, the peak shifted towards lower angles, showing compressive stress in CdTe devices. The (111) peak shifted towards the lower angles for the CdTe film deposited at 400 ºC. For CdTe films deposited between 200 ºC and 300 ºC, the peak shifted closer to the stress-free bulk material value. The d spacing values and strain in CdTe solar cells were calculated from the XRD data. The results of these calculations are given below in Table 3-3.

Table 3-3 Strain and d-spacing of the thin film CdTe solar cells deposited at various substrate temperatures using 50 sccm Ar

Temperature	Ambient	100 ºC	200 ºC	250 ºC	300 ºC	400 ºC
Pos. (º2Th.)	23.704	23.708	23.7652	23.732	23.732	23.716
Strain	2.24e-3	2.08e-3	2.99e-4	1.06e-3	1.06e-3	1.74e-3
d spacing value (Å)	3.7503	3.7497	3.7431	3.7459	3.7459	3.7485

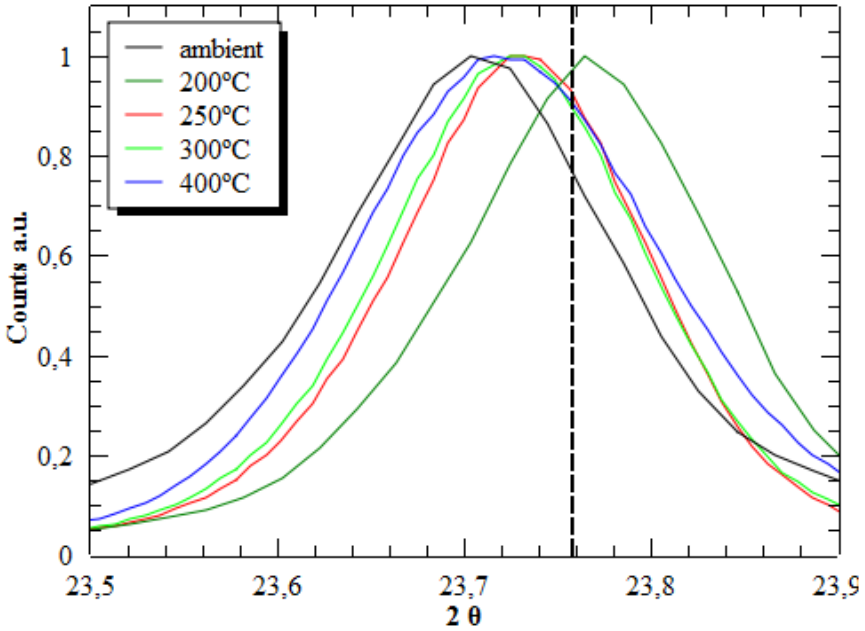


Figure 3-15 XRD spectra showing the (111) peak location measured for thin film CdTe solar cells deposited at different temperatures using 50 sccm Ar

Figure 3-16 shows the strain measured for the films deposited at different substrate temperatures and are based on the shift of the peak. The strain was highest for thin film CdTe solar cell deposited without substrate heating. The strain decreased as the substrate temperature was increased. The minimum strain was at 200 ºC. For the

temperatures above 200 ºC, increasing the substrate temperature results in an increase in the strain. The reason of the strain formation during the deposition process may be the presence of Ar in the CdTe layer.

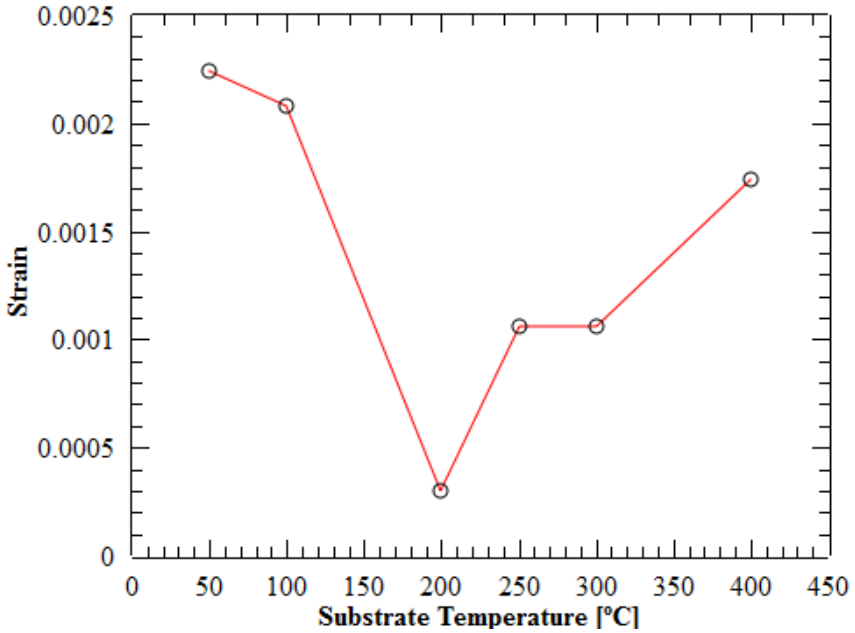


Figure 3-16 The strain measured for thin film CdTe solar cells deposited at different substrate temperatures using 50 sccm Ar

Figure 3-17 shows Tauc plot analysis of thin film CdTe solar cells deposited at various substrate temperatures. $(\alpha h\nu)^2$ is shown as a function of the band gap energy. The slope shows the direct transition of electrons between the valence and the conduction band. The band gap energy is determined to be 1.45 eV.

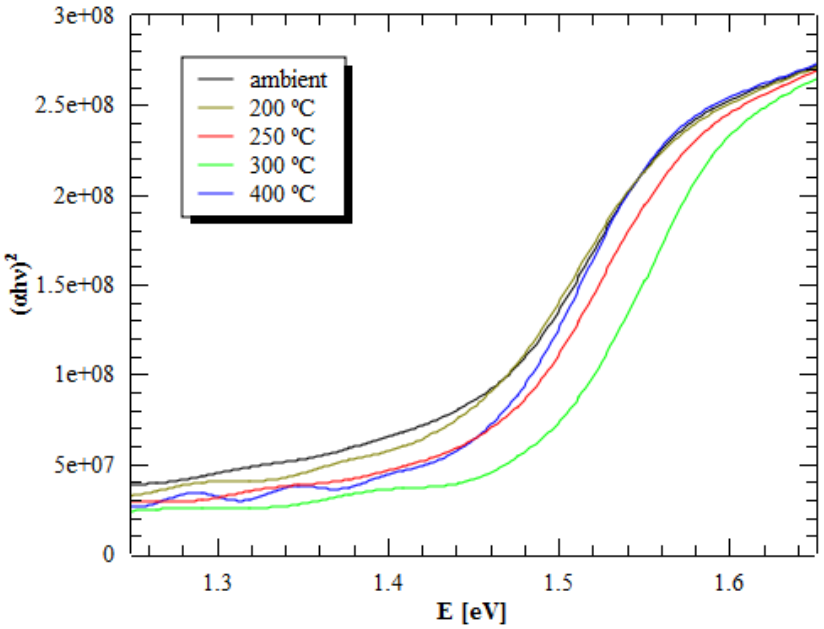


Figure 3-17 A Tauc plot analysis of thin film CdS/CdTe solar cells deposited at different substrate temperatures using 50 sccm Ar

Figure 3-18 shows the band gaps for CdTe devices deposited at various substrate temperatures using 50 sccm Ar. The bandgap was 1.415 eV at lower substrate temperatures. The band gap close to the bulk value of CdTe, 1.45 eV, was obtained at a substrate temperature of 300 ºC.

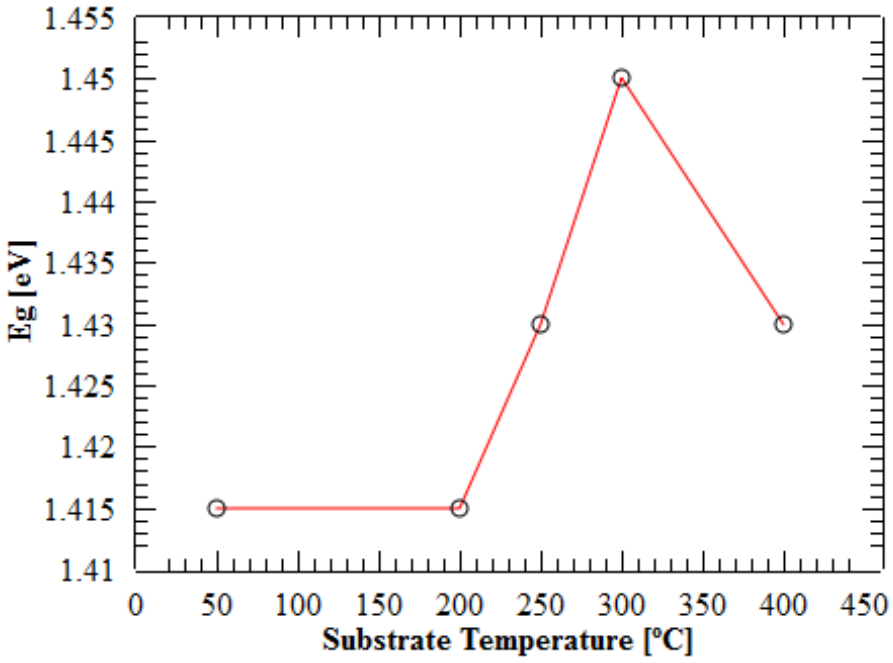


Figure 3-18 The band gap of thin film CdS/CdTe solar cells, deposited using 50 sccm Ar, as a function of substrate temperature. The band gaps were calculated from the Tauc plot.

3.3.3. Device Annealing

The deposited thin film CdTe solar cells were post annealed at different temperatures to remove the stress developed during the sputtering process. The devices were placed on a hot plate and annealed in ambient air for 10 min. Table 3-4 shows the *d* spacing values at different annealing temperatures. The thin film CdTe devices were deposited at 100 ºC, at an Ar gas flow rate of 50 sccm. The devices were annealed at 300 ºC, 350 ºC, and 400 ºC.

Table 3-4 d spacing values for the CdS/CdTe solar cells treated at different annealing temperatures for 10 min. CdTe was deposited at 100 ºC using 50 sccm Ar. Baseline (111): d spacing value for the state-free state is 3.742.

Substrate Temperature	*d* spacing value (Å)
300 ºC	3.7625
350 ºC	3.7435
400 ºC	3.7403

Figure 3-19 shows the effect of post annealing on the thin film properties. The experiment indicated that the stress in the film can be reduced by post annealing.

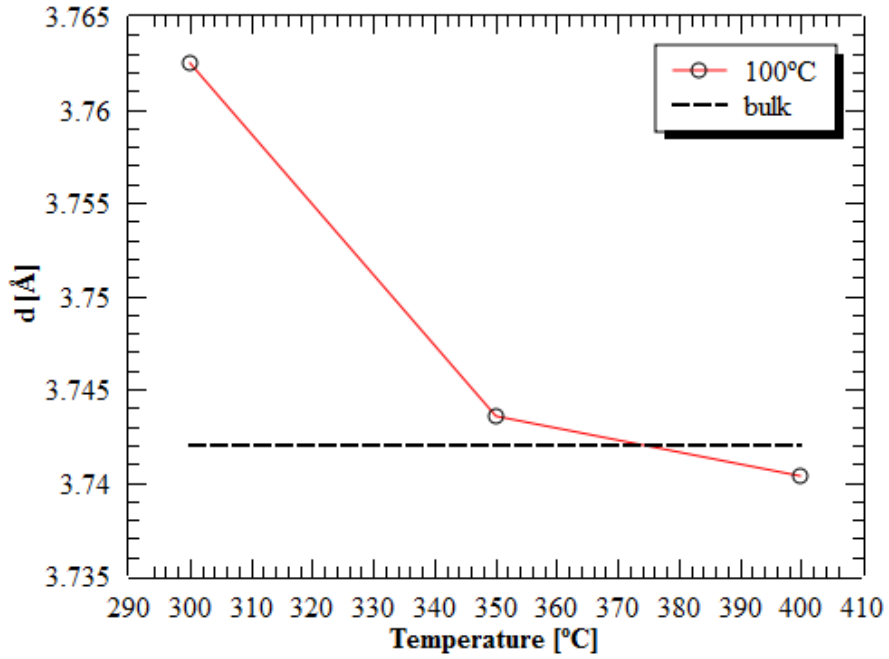


Figure 3-19 The d spacing of the CdTe solar cells at increasing substrate temperatures using 50 sccm Ar.

3.4. Discussion

The effect of the Ar gas flow, the temperature, and the working gas pressure on the stress formation in sputtered thin film CdS/CdTe solar cells has been investigated. The peak position was measured in the XRD spectra for various process conditions. Tauc plot analysis was performed using spectroscopic transmission measurements. Band gaps were also calculated. The crystalline structure of thin film CdTe solar cells was analysed from the TEM images of cross-sections. Different Ar gas flow rates were used during the CdTe layer deposition. The deposition rate decreased with increase in Ar gas flow. The highest deposition rate was 2.4 nm/s for CdTe devices deposited at 20 sccm Ar flow. The lowest deposition rate of 1.7 nm/s was measured at 100 sccm. The TEM analysis indicated that thin film CdTe solar cells, deposited at an Ar gas flow rate of 50 sccm, have a crystalline structure with columnar grains. These columnar grains extend through the film thickness with epitaxial columnar growth from the substrate. The TEM analysis of thin film devices deposited without substrate heating revealed that the solar cells deposited at an Ar gas flow rate of 20 sccm, have a crystalline structure with small grains. As Ar gas flow increases, more distinct columnar grains are formed in the films. The grains extend through the film thickness. The XRD measurements indicated that the position of the peak was closest to the bulk values for thin film CdTe devices deposited using 60 sccm Ar gas flow. The highest band gap value, 1.425 eV, was obtained for the CdTe device deposited using 20 sccm Ar. The band gap increased linearly with decreasing Ar gas flow. The deposition rate increased with decreasing substrate temperature during the

deposition of the CdTe solar cells at a constant Ar gas flow of 50 sccm. The highest deposition rate was 2.8 nm/s for thin film CdTe solar cells deposited without substrate heating. The deposition rate measured 1.6 nm/s for thin film CdTe devices deposited at 400 ºC. The STEM analysis of the as-deposited CdTe solar cells showed that the films have columnar structure with grains extending through the sample thickness. The grains had 50 nm - 70 nm diameters for the CdTe device deposited without substrate heating. The grain diameter increased to 250 nm when the CdTe was deposited at 200 °C substrate temperature. The TEM analysis indicated that the substrate temperature improves the film crystalline structure. The grain size increased to a diameter of ~500 nm for the devices deposited at 400 ºC. The EDX analysis (Figure 3-12) showed that there is 4 at% Ar in the CdTe layer. High densities of planar defects were observed in the HR-TEM images of the as-deposited material. Lower defect density was observed in the CdTe solar cell deposited at 200 ºC substrate temperature. The analysis showed that the stacking faults, which affect the solar cell performance, were removed after the $CdCl_2$ activation process. However, blister and void formation observed after the $CdCl_2$ activation process between 370 ºC and 408 ºC. Delamination also observed in the CdS/CdTe junction due to the voids.

The XRD measurements presented that the peak (111) position was closest to the stress—free bulk value for the devices deposited between 200 ºC and 300 ºC. The band gap of thin films approached stress-free bulk values of 1.45 eV for the thin film devices deposited at 300 ºC. Experiments were performed to explore the possibility

of removing the stress from the deposited thin films by annealing on a hot plate. A 10-min annealing at 350 ºC reduced the stress to the levels found in the bulk material. The experiments have revealed that the stress developed during film deposition can be controlled by the substrate temperature and the working gas pressure.

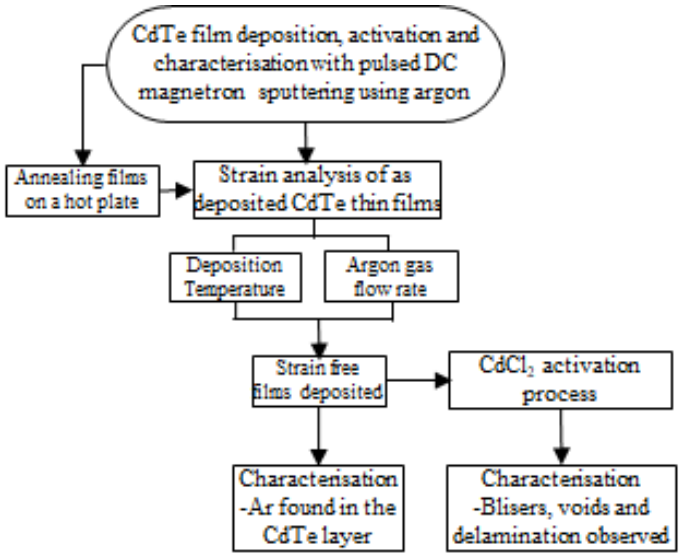


Figure 3-20 Chapter3 Schematic Diagram

CHAPTER IV

4. Pulsed DC Magnetron Sputtering with argon as the working gas

4.1 Introduction

Magnetron sputtering provides uniform coatings and high deposition rates for thin film CdS/CdTe solar cell deposition. It is suitable for large scale applications and contains an arc suppression technology. RF magnetron sputtering is a low temperature process and has been used by NREL and University of Toledo [81], [89], [145]–[147].

A longstanding difficulty of sputtered thin film CdTe solar cells is the formation of large scale blisters on the CdTe surface. Compaan and Bohn [1] deposited thin film CdTe solar cells using the RF sputtering technique as early as 1992. Blisters were

observed on the CdTe surface as shown in Figure 4-1. They reported that blistering occurred after the $CdCl_2$ activation process during the annealing process at 400 ºC [1]. The mechanisms that lead to blister formation have remained a mystery for over 25 years as no research was conducted on possible reasons of this issue. The reasons for blister formation will be revealed in this thesis.

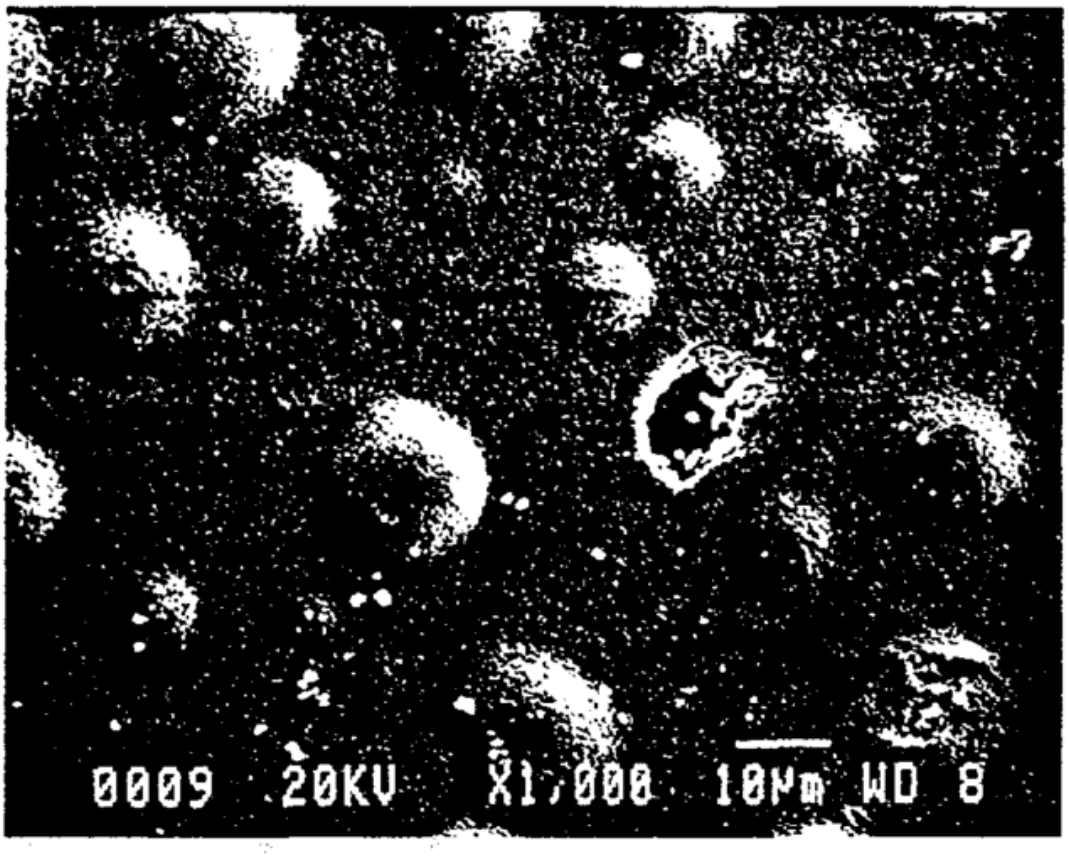


Figure 4-1 SEM images showing severe blistering after $CdCl_2$ activation process and annealed at 400 ºC taken from Compaan and Bohn in 1992 [1]

This chapter also focuses on the description of a new high rate deposition method to fabricate thin film CdS/CdTe solar cells by pulsed DC magnetron sputtering using

Ar as the working gas. The chapter concludes with a discussion on the effect of the $CdCl_2$ activation process on CdTe devices.

4.1.1. Literature on blister formation

Research on bubble and blister formation during the sputtering process, has been studied since the 1960s. However, the mechanism of bubble formation is still unknown. Material type, deposition method, target and substrate temperature during sputtering, and target preparation must be examined to obtain a better understanding of bubble/blister formation during deposition and after annealing processes. Navinsek [148] reviewed blister formation in metals and the formation of gas bubbles in near surface regions with energetic light ions implanted into a solid target. Due to their high internal gas pressure, bubbles can cause the surface of the metal to grow and deform. This deformation results in visible blister formation [148].

In 1986, Tyagi and Nandedkar [149] investigated the surface damage of ion bombarded metallic glasses using Ar at RT. Images of blistering and surface roughening were obtained using SEM. Blisters were dome shaped with diameters of between 1-3 μm. Blister formation and exfoliation were observed after annealing at 400 ºC. There were larger blisters with a size of 3 to 50 μm formed due to the migration and coalescence of smaller blisters. They also compared Ar and helium (He) [150], [151] ion irradiation of the same metallic glasses. It was observed that Ar bubbles are larger than He bubbles (Figure 4-2**).** Ar blistering disappeared at high implantation dose, whereas He blistering did not. [149]

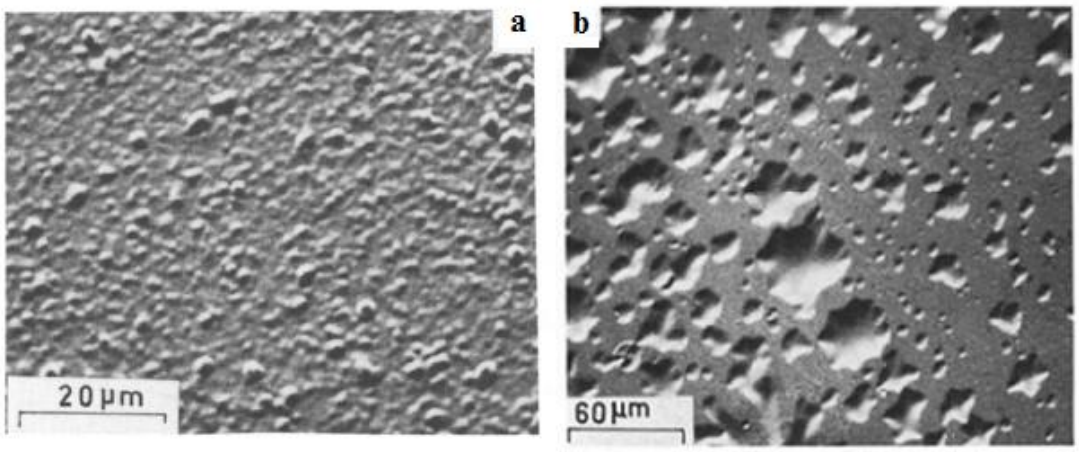


Figure 4-2 SEM image of a) $Ni_{60}Nb_{40}$ glass surface showing blistering with He ions [153] and b) $Fe_{40}Ni_{40}P_{14}B_6$ metallic glass surface showing blistering with Ar ions [152]

Keesom and Seidel [153] irradiated and then annealed a boron-doped Si crystal. He^4 was produced by the boron-neutron reaction.

$$B^{10}+n^1 \text{-->} He^4+Li^7 \qquad (4.1)$$

He was found to be liquid inside the crystal at low temperatures. A possible explanation for this is the high pressure the He is under inside the defects. After annealing at 930 °C for 24 hours He atoms had not remain localized, they had diffused to the GBs and collected in large groups. Moreover, 20% of the He diffused out of the crystal. The reason for this increased diffusion coefficient is the increased temperature. The presence of micro defects was observed with an optical microscope. [153]

Lee and Oblas [154] analysed Ar entrapment in a variety of sputtered metal films. They found that the amount of Ar in the film depends on the Ar pressure, the

distance between target and the substrate, and the sputtering voltage [155]. An increase in the reflected kinetic energy of Ar or an increase in the atomic spacing of the film lattice could explain increased Ar entrapment [154].

Romana et al. [156] observed blisters in alumina (Al_2O_3) films after Xe irradiation. The Al_2O_3 films were deposited with electron beam evaporation. The energy was 1.5 MeV. SEM images were obtained after Xe irradiation. The diameters of the bubbles were around 1-2 μm and 15% of the film surface was covered with blisters. It has been stated that the reason for blister formation is related to the energy of deposition. [156]

Bubble formation in sputtered thin film amorphous niobium-germanium (a-Nb_3Ge) devices was studied by Pruymboom et al [157]. It was found that increasing the Ar pressure and reducing the substrate temperature resulted in a lower concentration of Ar. The reason for the lower Ar concentration at higher Ar pressures might have been the thermalisation of energetic Ar atoms, or the effect of increased deposition rates. [157]

A recent study by Bras et al. [158] investigated blistering in copper zinc tin sulphide (CZTS) devices. CZTS films were deposited by pulsed DC magnetron sputtering at RT. Blister formation was observed after the annealing process. It has been indicated that Ar was trapped in the CZTS films during the deposition process. Annealing at high temperatures resulted in Ar migration, which coalesced to form blisters. After annealing, no blisters were observed in samples deposited at high sputtering

pressures. There were less blisters observed on the devices deposited at 150 ºC compared to RT. Ne, Ar and Kr were used as the process gas while the deposition conditions remained constant to minimise blister formation. CZTS devices deposited using Ne as the working gas resulted in large blisters in the film. Higher density of smaller blisters was observed in devices deposited using Ar as the working gas. Using Kr as the working gas resulted in fewer, much smaller blisters in the films. Due to less gas entrapment, devices that were deposited using Kr and Ar showed better results compared to devices deposited using Ne. (Figure 4-3) [158]

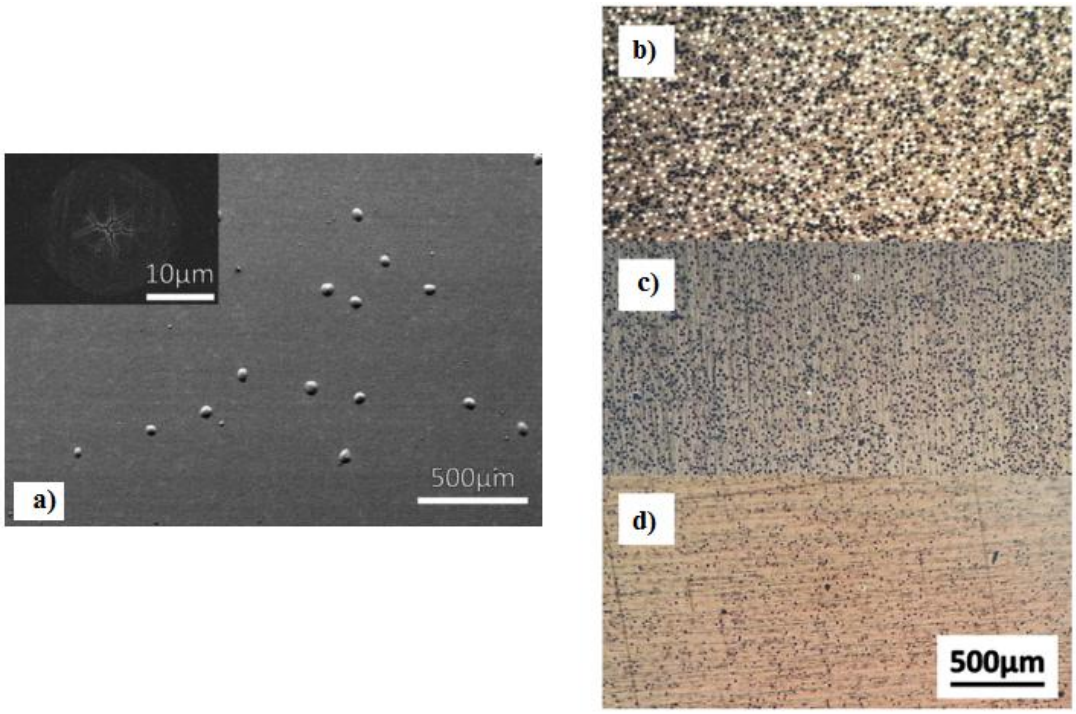


Figure 4-3 a) SEM image of the CZTS film (sputtered with Ar) after annealing. Blisters with diameters of 10-20 µm, and films sputtered with b) Ne, c) Ar, and d) Kr and annealed. Sample sputtered using Ne shows large blisters. Sample sputtered with Ar exhibits high density of smaller blisters. Sample deposited using Kr shows less and smaller blisters. [160]

Cao et al. [159] studied molybdenum (Mo) films deposited by DC magnetron sputtering. They found a strong relation between residual stress and deposition conditions. Bubble formation was observed at low working gas pressures and high sputtering powers [159].

4.1.2. Description of bubbles/blisters in CdTe solar cells

Little research has been conducted on the mechanism of bubble formation in semiconductors and in CdTe in particular. As mentioned earlier in the thesis, Compaan and Bohn [1] studied CdS/CdTe solar cells deposited by RF sputtering. Blisters occurred on the CdTe layer grown on CdS. Blistering occurred during the annealing process. Blister formation was near the centre of the film which was above the centre of the sputtering target [1].

Sanford [81] studied RF sputtered thin film CdTe solar cells in his doctoral thesis. He deposited the films with Ar at temperatures of 200 ºC, 300 ºC and 400 ºC. More bubbles were observed on the device deposited at 200 ºC. Blisters occurred during the annealing process. Blisters were not observed when the deposition was performed at a high deposition pressure (12 mTorr) [81]. Treharne [160] indicated that over treated RF sputtered thin film CdS/CdTe devices had degradation such as blistering.

Lienard et al. [161] studied the deposition of CdTe and ZnS layers by Ar or Xe ion beam sputtering. Compressed stress of Ar was 2700 MPa whereas it was only 800 MPa for Xe beams. Higher stress was measured in Ar ion beam sputtered devices

due to backscattered ion energy during deposition. On the CdTe target backscattered ion energy was 35% of the primary Ar beam energy, this was due to the strong mass differences between CdTe and Ar, whereas it was only 1% for Xe ions. Therefore, it was found that using Xe beams reduced compressive stress. [161]

4.1.3. Literature on the mechanisms of the bubble/blister formation

During the sputtering process of CZTS, a fraction of the Ar ions is backscattered toward the substrate and reach the film. If the energy of these particles is high, gas entrapment occurs. Increasing the sputtering pressure or substrate temperature reduces sputtering gas entrapments and blistering. During annealing at high temperatures trapped gas may diffuse along the GBs and accumulate at stacking faults and dislocations. [158]

Compressive stress generally occurs on ion beam sputtered films. The stress origin was described by the atomic peening model by Lienard et al [161]. It has been stated that compressive stress is more dependent on the momentum of the incident beam than the energy [161]. Fan and Zhou [162] also explained the stress formation in the sputtered films using the atomic peening model. This model describes the bombarding effect on the film by the energetic particle flux. Gas atoms scatter energetic particles travelling from target to the substrate. If the atomic mass of the target is large and the working gas pressure is low, compressive stress may be observed. [162]

Berndt et al. [163] studied the lattice defects and exfoliation in hydrogen (H) implanted thin film CdTe solar cells. Highly facetted bubbles formed in the treated devices. Strain analysis was performed using large-angle convergent-beam electron diffraction (LACBED) measurements. LACBED detected a highly strained lattice in the material containing bubbles. [163]

Romana et al. [156] demonstrated that blistering is an intrinsic mechanism. They suggest that residual gases trapped in structural defects are the reason for blister formation. Blistering can be described with the lateral compressive stress model. [156]

4.2. Experimental

4.2.1. Pulsed DC Magnetron Sputtering

Table 4-1 Synthesis conditions for CdTe deposition using pulsed DC magnetron sputtering

CdTe deposition conditions	
Deposition rate (nm/s)	1.6-2.8
CdTe thickness (µm)	1-5
Substrate temperature (°C)	RT-450
Magnetron working gas	Ar
Flow rate (sccm)	10-100
Pressure	0.5-8.1

4.2.2. The $CdCl_2$ Activation Process

4.2.2.1. Thermal Evaporator

Table 4-2 Parameters of the $CdCl_2$ activation process with a thermal evaporator

$CdCl_2$ deposition with a thermal evaporator	
deposition time (min)	5-10
Annealing on a hot plate	
annealing time (min)	15-20
annealing temperature (°C)	370-385

4.2.2.2. Wet Chemical Treatment

Table 4-3 Parameters of the $CdCl_2$ activation process with wet treatment

Wet treatment	
concentration (% wt.)	0.1-0.5
Annealing on a hot plate	
annealing time (min)	15-20
annealing temperature (°C)	370-385

4.2.2.3. Vapour deposition in a tube furnace

Table 4-4 Parameters of the $CdCl_2$ activation process in a tube furnace

Vapour deposition in a tube furnace	
Annealing time (min)	6-30
Annealing temperature (°C)	370-408

4.3. Results

4.3.1. $CdCl_2$ activation process

4.3.1.1. Thermal Evaporator

Several experiments have been conducted on with thermal evaporator but only a set of those experiments is shown in Table 4-5. Table 4-5 shows some of the *Voc* data and images of the $CdCl_2$ treated CdTe cells using evaporation. The thickness of the $CdCl_2$ layer deposited on CdTe layer was 50 nm. A value of ~30 mV (*Voc*) was measured for the as-deposited sample after the sputtering process. It was measured with a multimeter. *Voc* was improved to ~600 mV after the $CdCl_2$ activation process. The images indicate that the CdTe devices were delaminated after the $CdCl_2$ treatment. The colour change of the sample is the primary figure of merit to identify this issue.

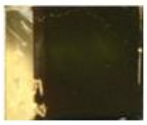
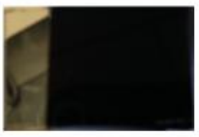
Table 4-5 Some voltage data and images of thin film CdTe solar cells after the $CdCl_2$ treatment using evaporation. CdTe films deposited at 250 °C and 400 °C using 60 sccm Ar and then $CdCl_2$ treated at 370 °C for 20 min and at 385 °C for 15 min. The Voc of the as-deposited sample is ~30 mV.

EVAPORATION					
Deposition Temperature (°C)	CdTe thickness (μm)	$CdCl_2$ treated CdTe film	Annealing Temperature (°C)	Annealing Time (min)	V_{OC} (mV)
RT	2		370	20	490
			385	15	420
250	1		385	15	600
	2		370	20	480
			385	15	560
	5		385	15	550
400	2		370	20	560
			385	15	610

4.3.1.2. Wet Chemical Treatment

Table 4-6 shows some of the voltage data and images of thin film CdTe solar cells after the solution based $CdCl_2$ wet treatment (0.5% wt. of $CdCl_2$ in methanol).

Table 4-6 Some voltage data and images of thin film CdTe solar cells after the wet atment. CdTe films deposited at 250 °C and 400 °C using 60 sccm Ar and then $CdCl_2$ treated at 370 °C for 20 min, at 385 °C for 15 min.

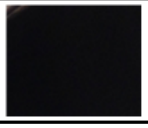
WET TREATMENT					
Deposition Temperature (°C)	CdTe thickness (µm)	$CdCl_2$ treated CdTe film	Annealing Temperature (°C)	Annealing Time (min)	V_{OC} (mV)
RT	2		385	15	380
250	1		385	15	490
	2		370	20	520
			385	15	550
	5		385	15	310
400	2		385	15	400

The *Voc* improved from ~30 mV to 550 mV. However, some of the CdTe solar cells were delaminated or under-treated after the $CdCl_2$ activation process. Moreover, this method did not treat the films uniformly. The colour change on the sample where the solution dropped is the primary figure of merit to identify this issue.

4.3.1.3. Vapour deposition in a tube furnace

Table 4-7 indicates some of the voltage data and images of thin film CdTe solar cells after annealing with $CdCl_2$ in a tube furnace. The voltage improved from ~30 mV to 725 mV.

Table 4-7 Some voltage data and images of thin film CdTe solar cells after the $CdCl_2$ treatment in a tube furnace. CdTe films deposited at 250 °C using 60 sccm Ar and then $CdCl_2$ treated at 370 °C for30 min, at 400 °C for 6 min, and 408°C for 8 min .

VAPOUR DEPOSITION IN A TUBE FURNACE					
Deposition Temperature (°C)	CdTe thickness (µm)	$CdCl_2$ treated CdTe film	Annealing Temperature (°C)	Annealing Time (min)	V_{OC} (mV)
RT	2		370	30	690
			400	6	550
250	1		370	30	725
			400	6	450
	2		370	30	617
			400	6	658
			408	8	680
400	2		370	30	620
			400	6	590

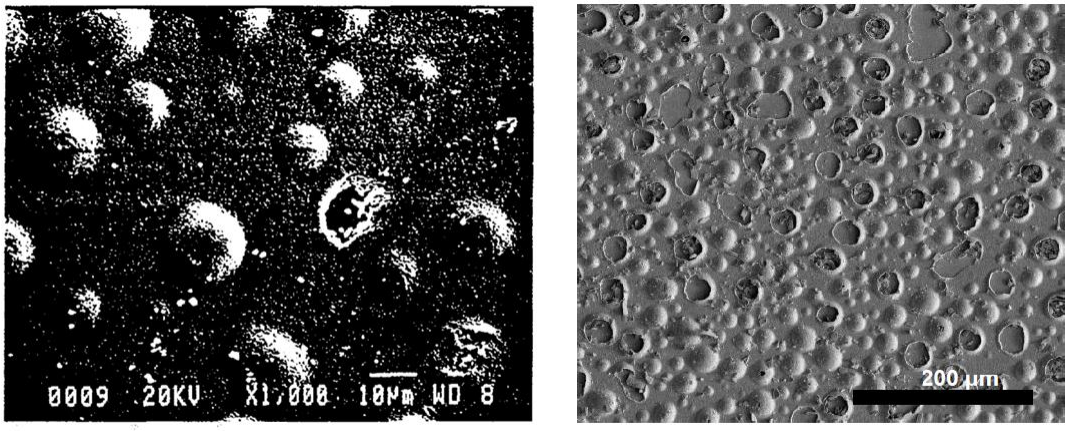
Higher voltage data was obtained with this method, when compared to the evaporation and wet treatment methods. The CdTe solar cells did not show any

delamination after the $CdCl_2$ activation process; however, there were voids observed shown on the STEM cross-section image in Figure 4-5a.

This method provides a fast and easy process; whereas, the $CdCl_2$ treatment with the evaporator is a two stage process including deposition of the $CdCl_2$ layer which takes a long time due to a long pump down time for the chamber and followed by the annealing process in a hot plate which is required to activate the CdTe solar cells. Wet treatment did not activate the films uniformly. Moreover, evaporation and wet treatment processes were more aggressive which resulted in colour change on the CdTe layer. This is due to the delamination in the Cds/CdTe junction. This was not observed for the samples treated with the tube furnace.

4.3.2. Microstructure of the $CdCl_2$ treated CdS/CdTe devices

Blister formation was observed on CdTe layer deposited using RF sputtering as shown in Figure 4-4a [1]. There are also several bubbles and blisters were observed on thin film CdTe devices deposited by pulsed DC magnetron sputtering as shown in Figure 4-4b. Bubbles, blisters or voids occur during the $CdCl_2$ activation process. Moreover, void formation at the CdS/CdTe junction causes delamination. These problems have been known for some time but the mechanisms leading to the formation of these defects have not been understood.



a) b)

Figure 4-4 SEM images showing blistering after $CdCl_2$ activation process of a) an RF sputtered [1] and b) a Pulsed DC magnetron sputtered CdTe devices. Sputtered device was deposited using 50 sccm Ar at RT. The size of the bubbles for the RF sputtered is ~10 µm whereas it is ~25 µm for the pulsed DC manetron sputtered CdTe layer.

It is known that the defect density reduces with the $CdCl_2$ activation process. In 1968, Woodman [164] published on stacking fault density in evaporated thin films of germanium (Ge). He found that preheating the substrate reduces the defect density. Moreover, the defect density reduces with the increase on deposition temperature. The reason may be due to increased self-diffusion of atoms followed by increased mismatched accommodation between the growing lattices. [164] Due to lower planar defect density in the CdTe device deposited at 200 ºC, twin type defects can be observed. The twin boundaries are electrically neutral [139], [165].

Subsequent thickening takes place through epitaxial growth on the grains and thin film CdTe solar cells tend to grow in columnar layers with (111) orientation at below ~350 ºC with PVD or CSS techniques [166], [167]. The columnar grain structure and high GB density provide fast diffusion of $CdCl_2$ to the CdS/CdTe junction. Stacking

faults were observed on both CdTe devices and their removal is required to increase the performance of the solar cells [92], [139], [165].

Figure 4-5a shows a STEM cross-section of the solar cell deposited at 200 ºC and treated with $CdCl_2$ in a tube furnace. The image shows that the stacking faults were removed after the $CdCl_2$ treatment. A major change of the crystalline structure was observed in the CdTe solar cell, the long columnar grains extending through the sample were not found in the device after $CdCl_2$ activation process. The grains grew into larger grains with a more irregular shape. More distinct grains were observed in the CdS film. Void formation can be seen within the CdTe layer and at the CdS/CdTe junction after the $CdCl_2$ activation process. These voids or pinholes may cause shunting issues. In Figure 4-5b the EDX analysis of the CdTe solar cell indicates that $CdCl_2$ decorated GBs. This was observed for a material deposited by CSS [165]. Delamination was also observed at the CdS/CdTe interface on the $CdCl_2$ treated devices.

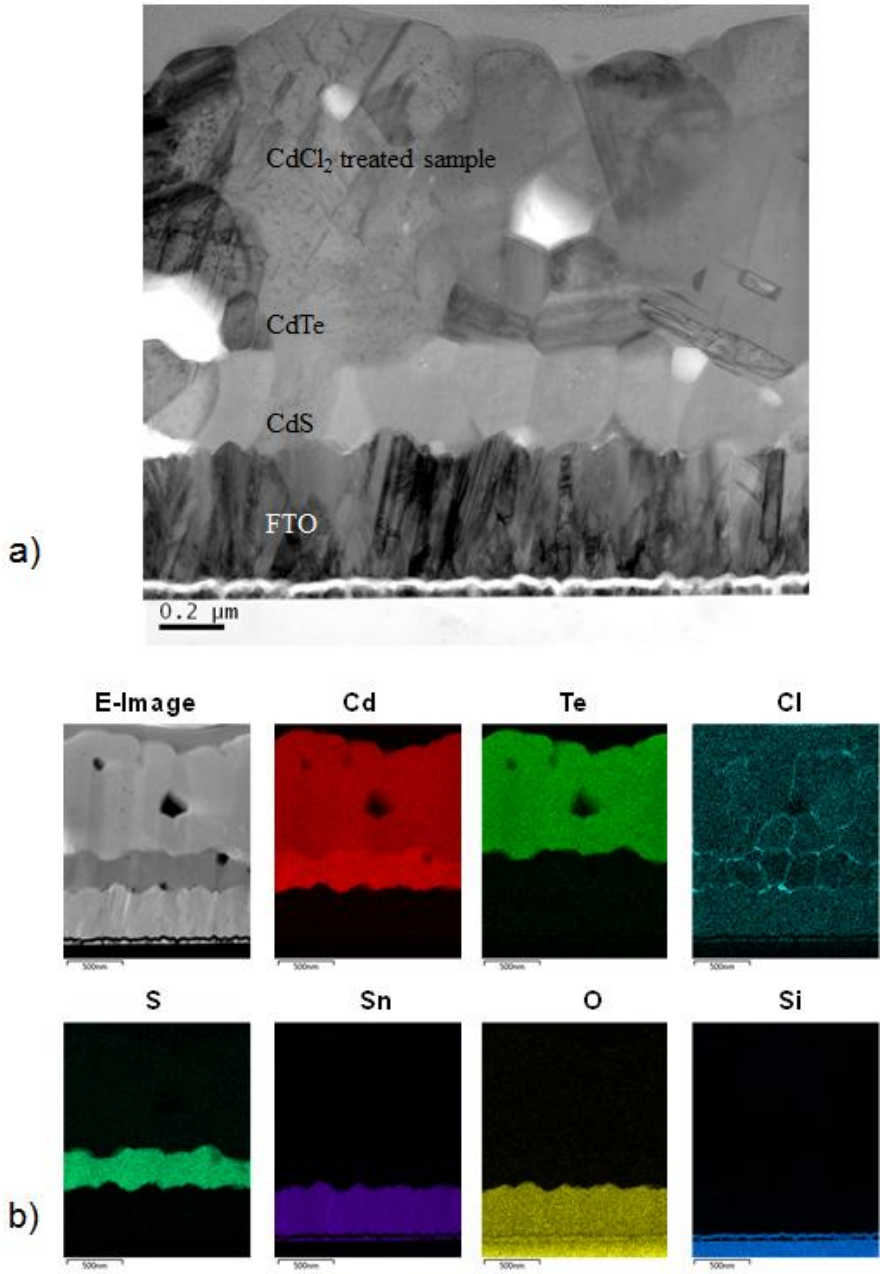


Figure 4-5 a) STEM cross-section image and b) EDX composition analysis of a $CdCl_2$ treated device. CdTe layer was deposited usin 50 sccm Ar at RT..

Figure 4-6 shows a cross section HR-TEM image of the $CdCl_2$ treated thin film CdTe solar cell. The analysis shows that the stacking faults observed in the as-

deposited CdTe solar cells (Figure 4-6) have been removed after $CdCl_2$ activation process. The twins were observed after the $CdCl_2$ treatment.

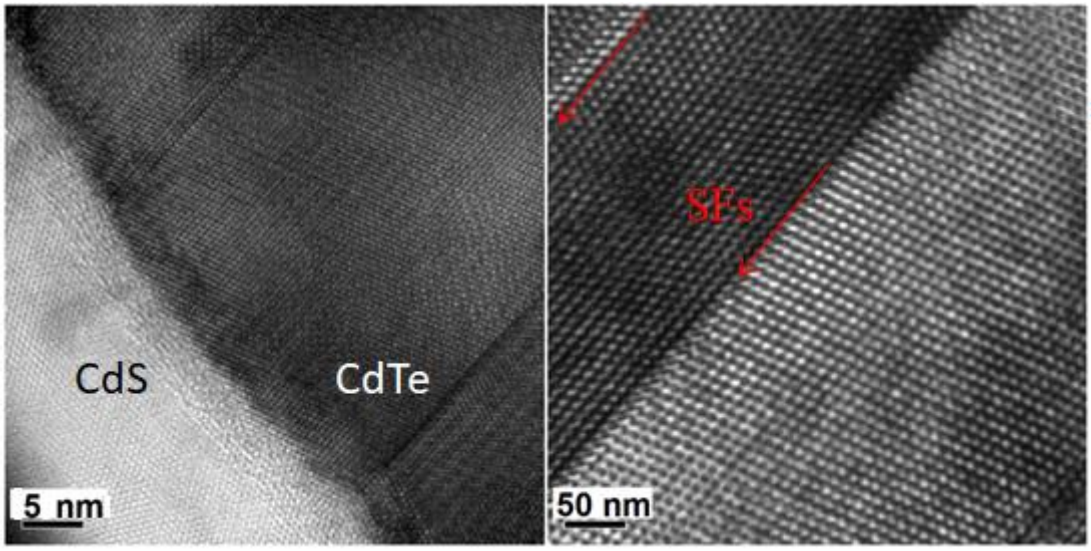


Figure 4-6 HR-TEM images of a $CdCl_2$ treated CdTe device deposited by pulsed DC magnetron sputtering. The sample was deposited at RT using 50 sccm Ar.

A TEM image of an as deposited CdTe solar cell is shown in Figure 4-7a. A TEM image is shown in Figure 4-7b, revealing the presence of voids. These are responsible for the low value of efficiency measured and shown in Figure 4-8. A J-V curve measured for the $CdCl_2$ treated CdTe device and ~5% efficiency was obtained. J-V characterisation is the primary electrical measurement for solar cells. The curve was generated by measuring the current as a function of the input voltage. The *Voc* of the as-deposited sample was ~30 mV and improved to 617 mV after the $CdCl_2$ treatment. The results show that the cell performance improved with the annealing process.

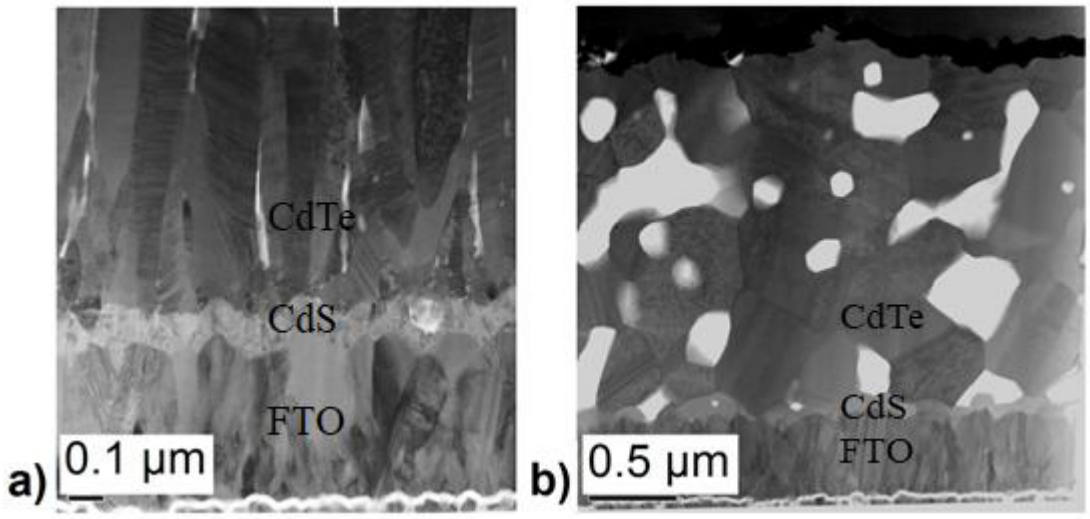


Figure 4-7 TEM images of the CdTe solar cell a) before and b) after the $CdCl_2$ activation process. CdTe layer was deposited using 50 sccm Ar and $CdCl_2$ treated at 385 ºC for 15 mins.

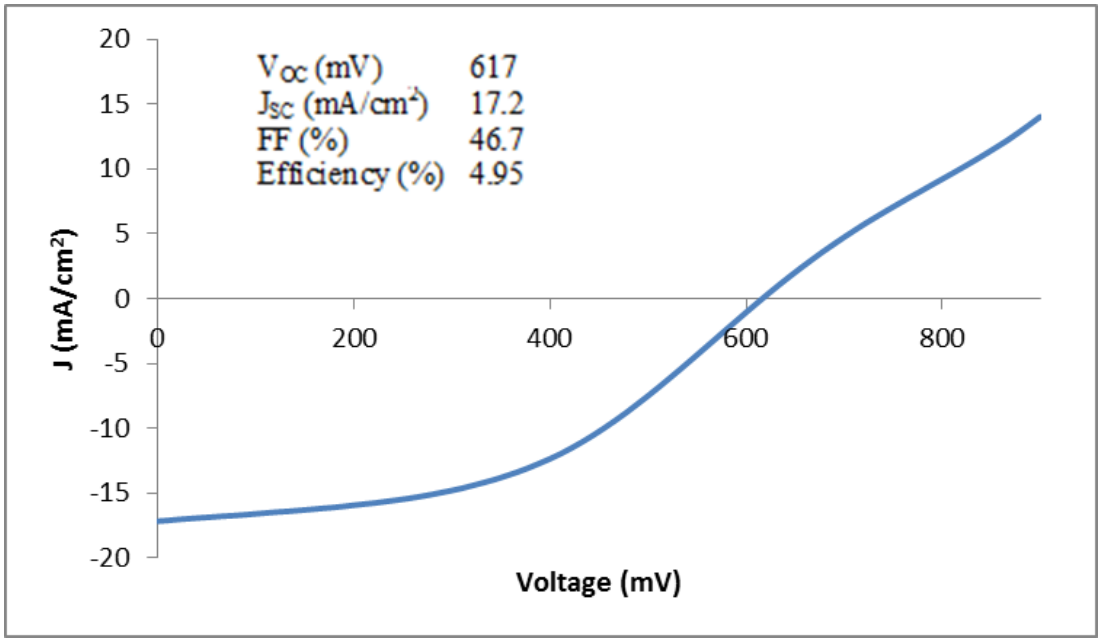


Figure 4-8 J-V characteristics of the $CdCl_2$ treated thin film CdTe solar cell. CdTe layer was deposited using 50 sccm Ar and $CdCl_2$ treated at 385 ºC for 15 mins. The efficiency is affected by void formation.

4.4. Conclusions

To optimise the $CdCl_2$ activation process, 3 different methods have been used (Figure 4-9). It was found that evaporation and wet treatment processes were aggressive for thin film CdTe solar cells deposited by pulsed DC magnetron sputtering. These treatments were aggressive mainly due to the use of $CdCl_2$ compound which causes blistering, void formation and delamination on thin film CdTe devices. Higher voltages were obtained by the $CdCl_2$ treatment in a vacuum evacuated tube furnace. This method also provided a fast and easy process. The EDX analysis showed that the Cl decorated GBs of CdS and CdTe layers. However, delamination was observed at the CdS/CdTe interface and catastrophic void formation was observed on the $CdCl_2$ treated devices. Further experiments need to be done to avoid void formation. One explanation may be stress formation, either during thin film CdTe deposition or during the $CdCl_2$ treatment. Therefore, strain analysis will be performed to eliminate the defect formation which occurred after the $CdCl_2$ treatment.

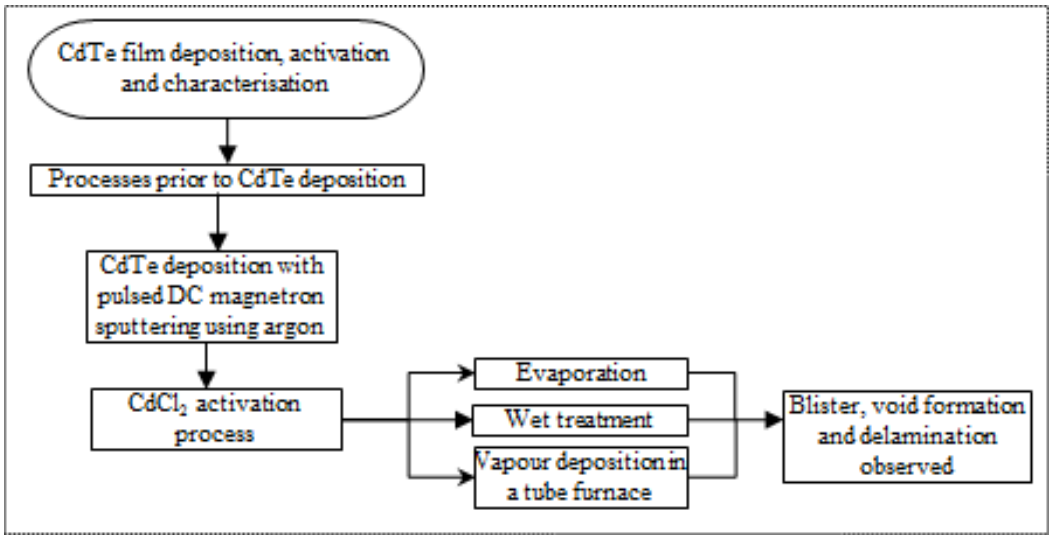


Figure 4-9 Chapter 4 Schematic Diagram

CHAPTER V

5. Annealing thin film CdS/CdTe solar cells using Rapid Thermal Processing

5.1. Introduction

In Chapter 3, it was reported that the $CdCl_2$ process causes catastrophic damage to magnetron sputtered thin film CdTe solar cells. Several studies and reviews have focused on the strain analysis of thin films to prevent the defect formation [129]–[134]. In Chapter 4, strain analyses were performed for thin film CdTe devices, deposited using pulsed DC magnetron sputtering, using Ar as the working gas. The deposition temperature and Ar gas flow rate during deposition were optimised to eliminate strain formation in the CdS/CdTe solar cells. However, even with

optimised conditions, delamination and void formation issues persist after the $CdCl_2$ activation process. The process involves the presence of $CdCl_2$ at around 400°C. To isolate the effect of $CdCl_2$ in the process, a compact RTP was used to perform an annealing only process of as-deposited thin film CdTe solar cells.

In the 1960s, Fairfield and Schwuttke [168] used pulsed laser beams as the foundation for developing RTP annealing as a research technique. Powell et al. [75] formed uniform titanium silicide ($TiSi_2$) films by RTP in only 10 seconds. In the following years, there have been several articles on the effects of the RTP system, its hardware design, and process [169]–[174]. RTP has the advantages of cycle time flexibility, process flexibility, temperature control, and processing speed [174]. Wilson et al. [171] found that RTP annealing resulted in improved sheet resistance and an increase in grain size of poly-Si films. Lee et al. [175] studied the reliability of the metal-oxide-semiconductor field effect transistors (MOFSETs) fabricated by RTP. They found that device characteristics were improved with the increase in temperature, however they degraded with increasing annealing time. The results were compatible with furnace annealing. [175]

Katz and Komem [176] studied the electrical properties and microstructure of contacts formed in the Ni/ Aluminium (Al)/ Si structure after RTP annealing at temperatures between 300 °C and 900 °C. The melting of Al at 580 °C resulted in lower sheet resistance. Katayama et al. [177] studied the effects of RTP on Silicon Dioxide/Gallium Arsenide (SiO_2/GaAs) interfaces with X-ray photoelectron spectroscopy. Rapid diffusion of Ga and a slight loss of arsenic (As) were observed.

A model of a RTP system was described by Gyurcsik et al. [178], [179] to achieve temperature uniformity. By using a short heating cycle, Copper Indium Selenium (CIS) thin films have been prepared by RTP with efficiencies higher than 10% [180]. Liu et al. [181] studied the design of RTP for large diameter applications of Si grating. Pascual et al. [182] performed a computer simulation of phase transformations in thin films, under different time and temperature conditions. It was observed that multi-step thermal processing is a promising technique to optimize the film structure [182].

Chakrabarti et al. [183] found that well crystallized thin film CdTe solar cells with large grains may be obtained by RTP annealing in an Ar atmosphere at ~500-550 ºC for 3 min. A zincblende structure was obtained after the annealing process and the devices were Te rich. Temperatures ≥576 ºC resulted in material loss during the annealing process. Recently, Ismail [184] described the effects of RTP on $CdCl_2$ treated vacuum evaporated CdTe devices. As-deposited CdTe solar cells showed a cubic zinc blend structure. A saturated $CdCl_2$ solution was used for the activation process, followed by annealing at 350 ºC for 15 min. It was then RTP annealed at 500 ºC for 30, 60, and 90 seconds respectively. Increase in grain size was observed after the RTP annealing. Increasing the annealing time resulted in a decrease in resistivity. RTP annealing reduced the stress on thin film CdTe devices. [184]

5.2. Experimental

Table 5-1 Synthesis conditions for CdTe deposition using pulsed DC magnetron sputtering and post-deposition annealing parameters with RTP for these CdTe devices

CdTe deposition conditions	
Deposition rate (nm/s)	2.4
CdTe thickness (µm)	1
Substrate temperature (°C)	250
Magnetron working gas	Ar
Flow rate (sccm)	20
Pressure (µbar)	1.9
Post-deposition annealing with RTP	
Annealing time	1-30 min, 4-12 hours
Annealing temperature (°C)	350-550

A Rapid Thermal Processor (RTP-1000D4), using a 10 kW halogen lamp with control over time and temperature [114], has been used in this study. The system was specifically designed for annealing semiconductor wafer or solar cells.

During the experiments with RTP, CSS-CdTe solar cells were supplied by Colorado State University (CSU). Sputtered devices were deposited at LU. Sublimated CSU devices had a CdTe absorber layer, ~2 µm thick. In contrast, sputtered LU samples had 1µm thick CdTe layers, deposited at around 250 °C. The RTP-1000D4 system was used for annealing thin film CdTe solar cells (Chapter 2). CdTe solar cells were placed on a sample holder and then both ends of the tube were sealed with flanges. The tube was evacuated to 10-120 mTorr and the temperature profile was set from the control panel. The control panel allows up to 30 process steps to be pre-set for fine control of the temperature, time, and ramping rate. Devices were annealed with

no Cl present in the system at temperatures between 350 °C and 550 °C and for 1 min to 30 min.

5.3. Results

5.3.1. Annealing at a lower temperature for longer periods

The voltage of the as-deposited sublimated thin film CdTe solar cell was measured ~460 mV for CSS samples. The voltage of the as-deposited sputtered CdTe device was measured ~30 mV for sputtered samples. Both samples were annealed with RTP at 350 °C for 4 to 12 hours to investigate the benefits of RTP processing. The results have been produced at conditions that are outside the ranges of the $CdCl_2$ process as no Cl was involved. Table 5-2 and Figure 5-1 present the results of the experiments. Increases in cell voltages were observed and the highest increase was obtained after 8 hours of annealing. The treatment caused a ≥65 mV increase for the CSS device, from ~460 mV to 525 mV. A 138 mV increase was measured for the sputtered sample, from ~30 mV to 168 mV. Longer than 8 hours annealing time resulted in a decrease in the cell voltages.

Table 5-2 The voltages of thin films after annealing at 350 °C

Temperature / Time	350 °C	
	CSS Voltage (mV)	Sputtered Voltage (mV)
4 hours	462	95
6 hours	491	130
8 hours	525	168
10 hours	455	155
12 hours	443	114

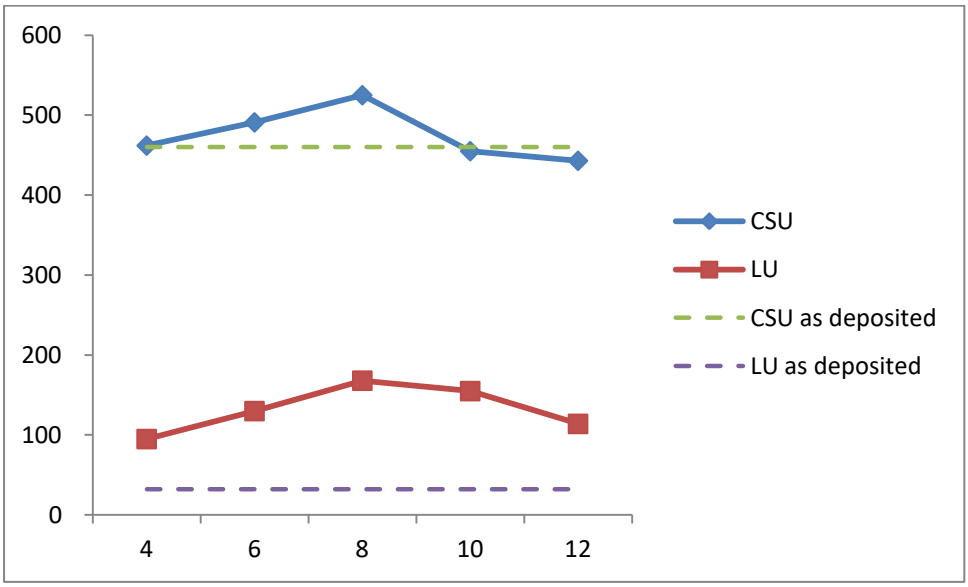


Figure 5-1 The voltages of CSU (CSS) and LU (sputtered) thin films after RTP annealing at 350°C

5.3.2. Annealing at high temperatures for short periods

Both CSS and sputtered samples were annealed with RTP at higher temperatures for short periods. The voltage data is shown in Table 5-3 and Figure 5-2. The results

have been produced at conditions that are outside the ranges of the $CdCl_2$ process as no Cl was involved. The voltage of the CSS sample increased by more than 60 mV, from ~460 mV to 526 mV, after 5 min annealing with RTP at 480 °C (Figure 5-2a). The cell voltage of the sputtered device was highest at 470 °C, after annealing for 5 min with a ≥190 mV voltage increase, from ~30 mV to 223 mV (Figure 5-2b). Annealing at higher temperatures resulted in a decrease of the cell voltage.

Table 5-3 The voltages of thin films after RTP annealing between 470 °C and 490 °C for 1 min to 5 min

Temperature	Time	CSS Voltage (mV)	Sputtered Voltage (mV)
470 °C	1 min	410	83
470 °C	3 min	430	115
470 °C	5 min	470	223
480 °C	1 min	380	97
480 °C	3 min	390	119
480 °C	5 min	526	182
490 °C	1 min	413	67
490 °C	3 min	441	151
490 °C	5 min	470	196

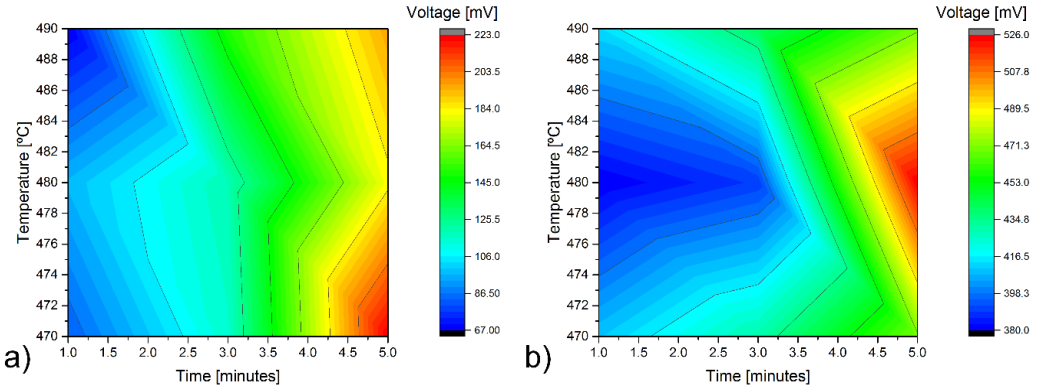


Figure 5-2 The voltages of a) CSS and b) Sputtered CdTe devices after RTP annealing between 470 °C and 490 °C for 1 min to 5 min (extrapolated graphs)

5.3.3. Annealing results and optimised conditions

Table 5-4 and Figure 5-3 summarise most of the experiments performed with RTP, between 380 °C to 480 °C for 1 min to 30 min. Annealing at high temperatures for over 10 min resulted in the evaporation of the entire CdTe absorber layer. The highest voltage of CSS device was increased from ~460 mV to 548 mV. The highest voltage of sputtered device was increased from ~30 mV to 384 mV. The highest voltage for CSS devices after RTP annealing was achieved for the solar cell annealed at 460 °C for 25 min. The highest voltage of 384 mV for sputtered devices was recorded for device annealed for 30 min at 460 °C. The increase in voltage of the annealed devices is promising, since Cl is not included during the annealing process.

In the first step, *Voc* measurements were performed with a digital multimeter and a light source. The *Voc* of thin films were not high enough to sputter back contact and measure the J-V curve and efficiency. Higher annealing temperatures were also

performed compared to $CdCl_2$ treatment because Cl is not used in the process and the films survived for longer annealing temperatures and times.

Table 5-4 The maximum voltages of CdTe thin films after RTP for both CSS and sputter-deposited samples

Temp / Time	380 °C		400 °C		440 °C		450 °C		460 °C		470 °C		480 °C	
	CSS	Spt	CSS	Spt	CSS	Spt	CSS	Spt	CSS	Spt	CSS	Spt	CSS	Spt
1 min	440	15	427	10	403	61	450	50	494	87	410	83	380	97
3 min	256	36	432	55	424	72	497	110	465	116	430	115	390	119
5 min	440	19	430	40	485	102	440	115	449	91	470	223	526	182
10 min	460	62	420	90	418	116	480	145	463	140	448	141	524	254
15 min	460	110	460	119	466	253	440	170	487	191	496	207		
20 min	516	66	464	97	520	338	500	333	535	362	530	375		
25 min	478	49	488	91	483	302	356	201	548	262				
30 min	460	100	479	120	508	360	490	230	0	384				

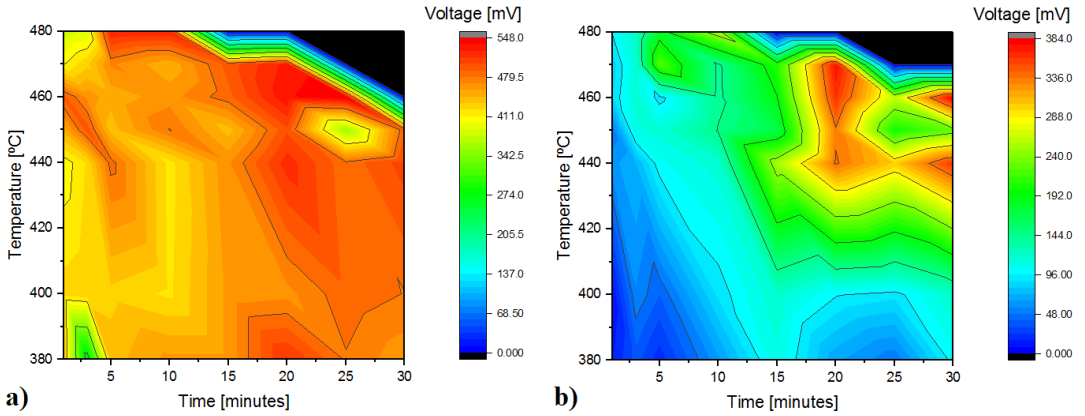


Figure 5-3 The photo-voltage contour maps of a) CSS and b) Sputtered thin films after RTP annealing as a function of annealing temperature and time (extrapolated graphs)

Sputtered samples had smaller grains due to the deposition at lower temperatures. More grains, which means more GBs, resulted in further relative increase on the cell voltage due to the passivation of more GBs.

5.3.4. RTP Annealing of sputtered thin film CdTe solar cells deposited by Loughborough University

Figure 5-4 shows a TEM cross-sectional image of a sputtered CdS/CdTe solar cell after annealing at 350 ºC for 12 hours. Small defects are observed at the GBs and the CdS/CdTe junction after the annealing process.

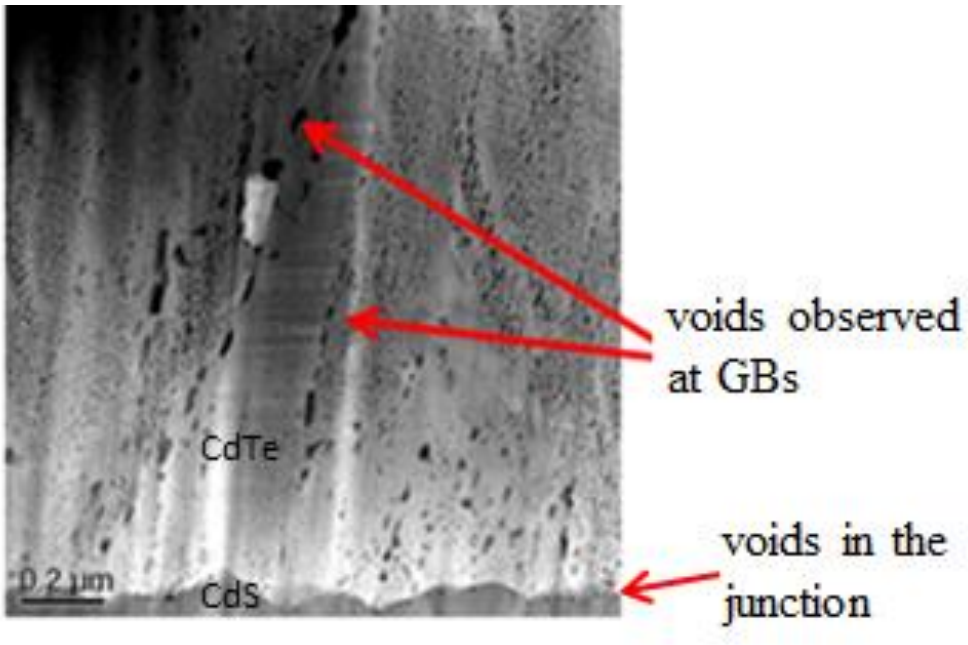


Figure 5-4 TEM images of cross-section of CdS/CdTe solar cells after annealing at 350 °C for 12 hours. Voids observed at GBs and in the CdS/ CdTe junction.

Figure 5-5 shows cross-section HR-TEM images of the RTP annealed sputtered CdTe devices. The HR-TEM shows that there are round defects with around 5 nm diameter through the CdTe layer. EDX analysis confirmed the presence of Ar atoms trapped in the absorber material in Figure 3-12. It is possible that these are Ar bubbles forming in the absorber material, shown in the HR-TEM. These defects are the Ar atoms diffuse in the lattice to form gas bubbles during the annealing process.

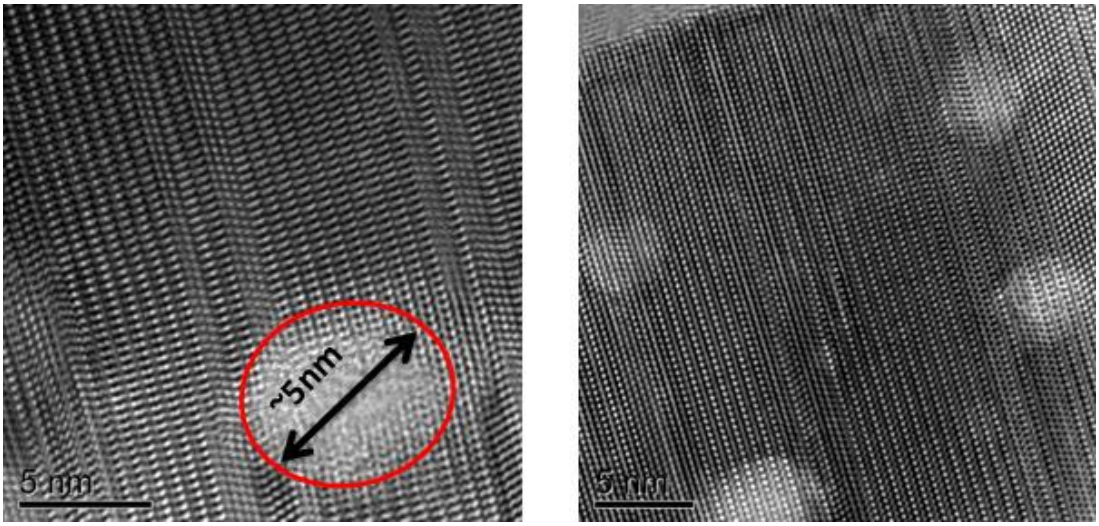


Figure 5-5 HR-TEM images of cross-section of thin film CdTe device annealed with RTP at 350 °C for 12 hours. The presence of several Ar gas bubbles approximately circular in shape and ~5 nm in diameter are shown.

During in-situ annealing in TEM, the movement of the small bubbles to GBs (where they coalesce and dramatically increase in size) has been observed, as shown in Figure 5-6. During the activation process, these bubbles grow and coalesce along the GBs and cause blistering, exfoliation and delamination.

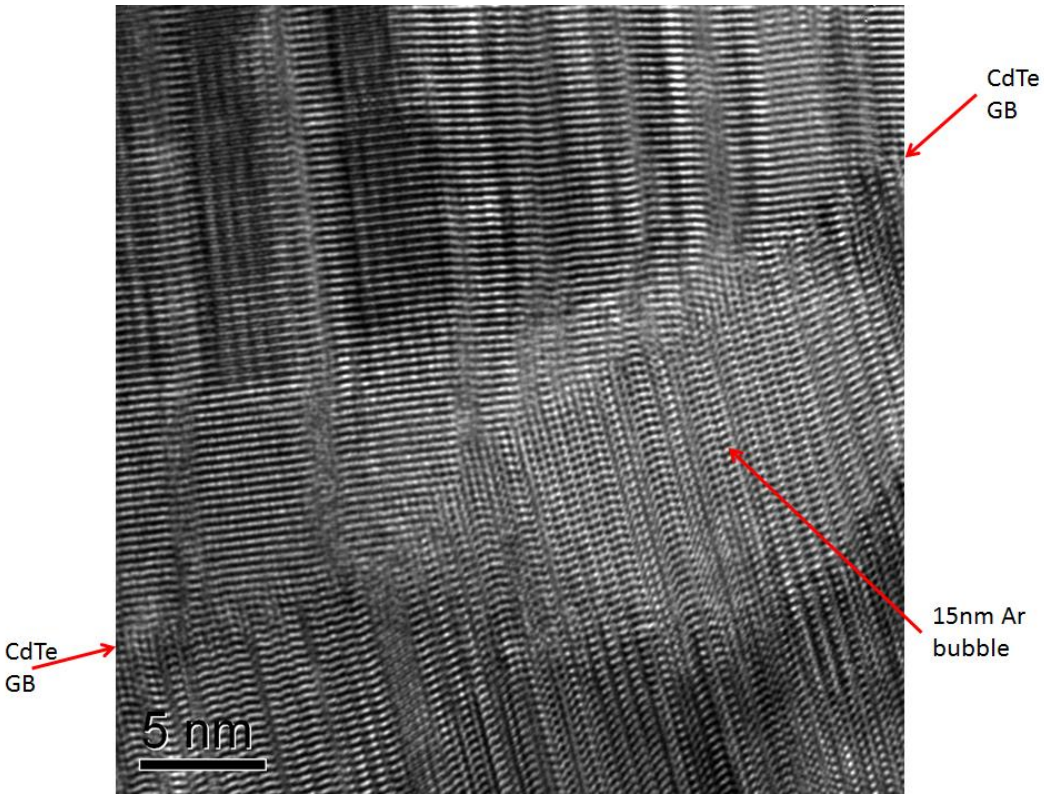


Figure 5-6 HR-TEM imageof cross-section of thin film CdTe device during in-situ annealing.

It is known that the $CdCl_2$ activation process has a major effect on the performance of the CdS/CdTe solar cells [185], such as removing defects, causing grain growth, and recrystallisation [81], [84], [85], [87], [186]. However, this process also causes void formation and surface blistering in the CdTe layer. Void formation at the CdS/CdTe interface damages the junction and potentially reduces the device efficiency. In this chapter, $CdCl_2$ was not used during the annealing process and the voltage still showed an increase. This was surprising that there were Ar bubbles observed in the CdTe layer after RTP annealing. It is the first time bubble formation has been observed at the atomic scale. It has not been mentioned or explained in

literature previously. We can deduce that not only the $CdCl_2$ treatment but also pre-annealing thin film CdTe devices has an impact on the cell performance. It is a temperature effect on the device.

5.4. Discussion and Conclusion

In Chapter 3, no voids were observed in the as-deposited sputtered CdTe devices. However, blisters were observed on the surface and catastrophic voids formed in the CdTe layer after the $CdCl_2$ activation process. Delamination occurred at the CdS/CdTe junction, due to blistering. About 4 at% Ar was trapped in the as-deposited CdTe layer, as discussed in Chapter 3.

To discover the cause of void or blister formation in thin film CdTe solar cells, it was necessary to isolate the effect of the annealing process from the effect of the $CdCl_2$ treatment. Therefore, the sputtered CdTe solar cells were annealed without $CdCl_2$. Annealing with RTP has improved the cell voltage of the CSS film from ~460 mV to 549 mV. The voltage of the sputtered sample has been increased from ~30 mV to 384 mV. Using RTP annealing without the presence of Cl resulted in the formation of small spherical features in HR-TEM images. These defects were observed in the GBs and at the CdS/CdTe junction and they were typically 5 nm in diameter but high in density with a tendency to accumulate in GBs and at the interfaces.

It has been discovered that these defects were caused by diffusion of the trapped Ar atoms in the CdTe lattice during the annealing process. In the $CdCl_2$ activation process, the Ar gas bubbles move and agglomerate particularly along GBs and at the

CdS/CdTe junction. In literature, it is known that light gasses trapped into solids can cause gas bubble formation in the substrate. Bubbles might grow into larger bubbles or form blisters [187]. Large voids are formed in the CdTe layer and are located at GBs and at the CdS/CdTe junction. Void formation at the CdS/CdTe interface leads to poor junction formation and to catastrophic delamination in thin film CdTe devices. It is the first direct observation of the formation of inert gas bubbles, after annealing at the atomic scale using HR-TEM.

This chapter reports the discovery that the formation of gas bubbles is responsible for these problems. Mitigating the mechanism that causes blistering and voids should result in an industrially viable sputtering process for the deposition of uniform and stable thin film CdTe devices. Other inert gases will be investigated in the next chapters as an attempt to improve cell performance.

CHAPTER VI

6. Deposition of thin film CdTe solar cells using krypton and neon

6.1. Introduction

The uniform deposition provides magnetron sputtering with important advantages as a deposition technique for some thin film CdTe solar cell applications. Moderately successful research has been conducted to develop a viable sputtering process in many laboratories. However, the conversion efficiency achieved has not matched that obtained using lower energy deposition techniques such as CSS or VTD. In particular, sputtered thin film CdTe solar cells are less tolerant than the high temperature processes to the $CdCl_2$ activation process. Delamination of the thin films at the CdS junction is often observed [188]–[192]. Catastrophic void formation

within the CdTe layer has also been reported [89], [191], [193], [194]. These issues have been discussed in earlier chapters.

This behaviour is often attributed to film stress even though this can be mitigated in the as-deposited films. Nanoscale defects, that are responsible for the poor response (such as bubbles or blisters) of sputtered CdTe devices to the $CdCl_2$ treatment, have been identified using state-of-the-art HR-TEM. Bubble and blister formation was observed on the annealed and $CdCl_2$ treated sputtered CdS/CdTe solar cells, using Ar as the working gas.

Ne and Kr gases were used for the magnetron working gas during thin CdTe layer deposition by pulsed DC magnetron sputtering, to eliminate the bubble or blister formation issue.

6.2. Experimental

6.2.1. Magnetron Sputtering

Table 6-1 Synthesis conditions for CdTe deposition using pulsed DC magnetron sputtering

CdTe deposition conditions			
Deposition rate (nm/s)	1.8	2.4	1.5
CdTe thickness (µm)	1		
Substrate temperature (°C)	200-250 (rot)		
Magnetron working gases	Ne	Ar	Kr
Flow rate (sccm)	20-50		
Pressure (µbar)	1.9	1.9	1.8

As covered in Chapters 2, 3 and 4, pulsed DC magnetron sputtering (PV Solar) was used to deposit CdS and CdTe layers on Pilkington TEC10 glass substrates. The substrates were cleaned in an ultrasonic bath and then subject to a plasma treatment. The CdS layers were deposited using Ar as the working gas. Then the deposition of CdTe layers were carried out using Ne, Ar, and Kr as the working gases, respectively. Ne, Ar and Kr compressed gas cylinders were connected to the sputtering system, respectively. In order to change the magnetron working gas during the sputtering process, two valves and a MFC were connected to the sputtering system. After the deposition of the CdS layer, the first valve was turned off to stop Ar gas flow. The Ar gas within the chamber was pumped out and monitored by the MFC to check that there was no gas left inside the chamber. Then, the second valve was turned on for the required working gas during CdTe deposition. The substrate temperature was 250 °C with rotation during the sputtering process. Thicknesses of 150 nm CdS and 1 µm CdTe layers were deposited respectively, without breaking the vacuum. The target voltage was ~800 V. The gas flow rate was 20 sccm. The deposition rates, shown in Table 6-2, were measured as 1.8 nm/s, 2 nm/s and 1.5 nm/s for the devices sputtered using Ne, Ar, and Kr respectively.

Table 6-2 Static deposition rates measured for thin film CdTe solar cells deposited using Ne, Ar, and Kr working gases

Magnetron working gas	dep.rate (nm/s)
Ne	1.8
Ar	2.4
Kr	1.5

6.2.2. $CdCl_2$ Process

Table 6-3 $CdCl_2$ activation process parameters for CdTe devices deposited using Ne, Ar and Kr as the magnetron working gases

$CdCl_2$ treatment Vapour deposition in a tube furnace	
Annealing time (min)	6
Annealing temperature (°C)	400

The devices deposited using Ne, Ar and Kr were annealed using a $CdCl_2$ vapour treatment. The devices were heated and kept at constant temperature (400 °C). Thin film CdS/CdTe solar cells were annealed for 6 min.

6.3. Results

6.3.1. As-deposited Material

Figure 6-1 shows TEM images of the CdS/CdTe PV device, deposited by pulsed DC magnetron sputtering using Ar. The Ar gas flow was 50 sccm and the substrate temperature was 200 °C during the deposition of the CdTe layer. The films showed columnar structure and covered the substrate uniformly without any voids or pinholes. Average grain diameter was around ~200 nm. The *Voc* of the as-deposited CdTe device was ~30 mV.

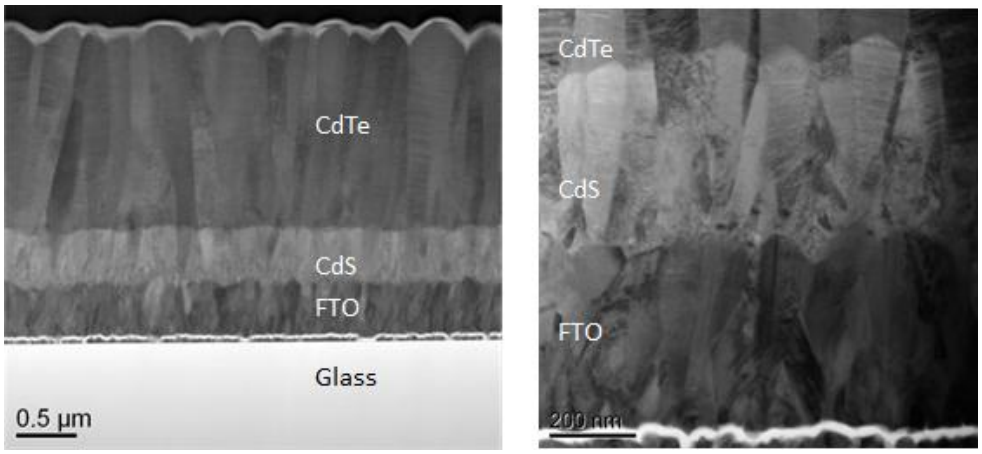


Figure 6-1 TEM images of cross-section of as-deposited thin film CdS/CdTe solar cells using 50 sccm Ar working gas at 200 ºC.

Result of EDX analysis of the as-deposited CdTe solar cell is shown in Figure 3-13. The spectrum on the top was obtained from the as-deposited CdTe layer. 48.1 at% Cd and 48.3 at% Te were observed. The second spectrum, obtained from the CdTe layer near the CdS junction, indicates that there was 48.1 at% Te and 49.9 at% Cd. Most importantly, the EDX measurement confirms the presence of about 4 at% Ar in the as-deposited film. Ar becomes trapped in the CdTe layer during the sputtering process and appears to be distributed uniformly. The potential difference between the substrate and the target causes the Ar ions to accelerate towards the film. Unbalanced magnetrons encourage Ar ion bombardment, resulting denser films [195].

6.3.2. $CdCl_2$ treatment

The *Voc* of the CdTe solar cell, treated with the $CdCl_2$ activation process at 400 ºC for 6 min, showed a sharp increase from ~30 mV to ~700 mV after the treatment. After the $CdCl_2$ treatment further analysis was performed with TEM. *Figure 6-2*

shows SEM images of a sputtered device following activation with $CdCl_2$. *Figure 6-2*a indicates blisters and perforated blisters formed on the surface. The blisters were between 10 µm to 200 µm in diameter. *Figure 6-2*b shows an SEM image of a cross-section of a blister (100 µm in diameter). Delamination occurred at the CdS/CdTe junction.

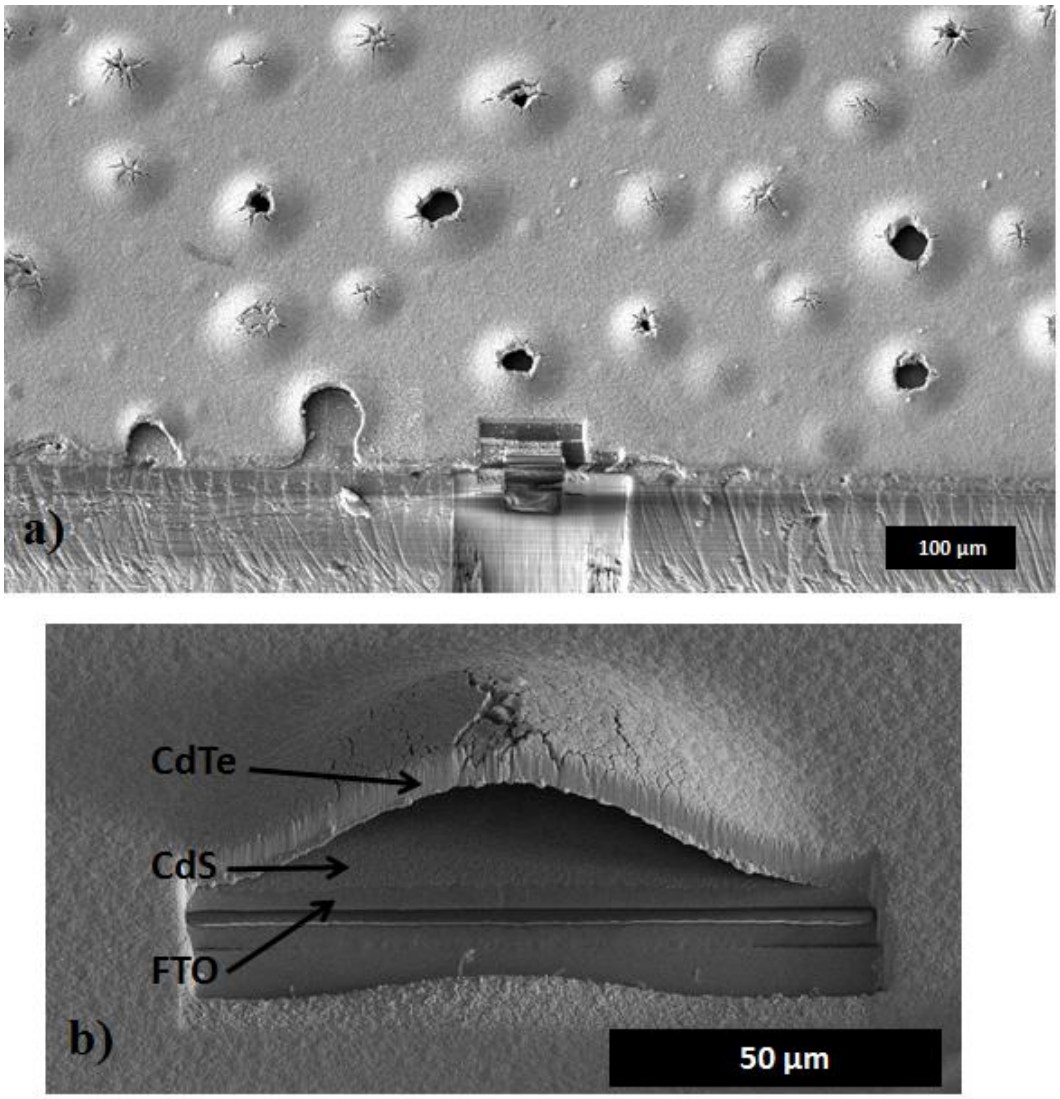


Figure 6-2 a) SEM image of a CdTe device deposited at 250 ºC using 20 sccm Ar magnetron working gas and then $CdCl_2$ treated at 400 ºC for 6 min. Blisters and perforated blisters appear on the surface, b) SEM image cross-section of a large blister prepared using a FIB.

Figure 6-3 shows a TEM image of the material cross-section of CdS/CdTe following the $CdCl_2$ activation process. CdTe grain diameters were between 300 nm and 500 nm. Catastrophic void formation occurred along the CdS/CdTe junction.

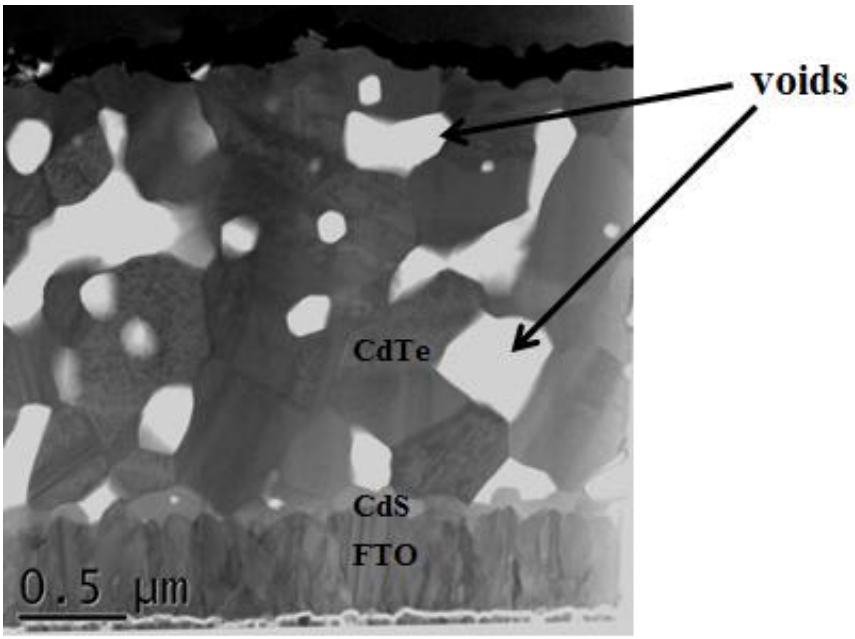


Figure 6-3 A TEM image of cross-section of CdS/CdTe following the $CdCl_2$ treatment. CdTe layer was deposited at 250 ºC using 20 sccm Ar working gas and $CdCl_2$ treated at 400 ºC for 6 min.

6.3.3. Krypton working gas

Ar is the standard working gas used in magnetron sputtering. However, the presence of Ar in deposited CdTe layers causes blistering, voids and delamination. Trapped inert gas in CdTe may be avoided by using an alternative inert gas as the magnetron working gas. The sputter yield of He is low and it is known to cause bubble formation in different materials [148], [196], [197]. Therefore, Ar was compared with Kr, which has a lower atomic mass than Cd and Te but is heavier than Ar.

A thin film CdS/CdTe solar cell was deposited using Kr. The substrate temperature was 250 ºC and the gas flow was maintained at 20 sccm during the deposition. TEM images of a cross-section of the as-deposited device, and after the $CdCl_2$ activation process at 400 ºC for 6 min, are shown in *Figure 6-4*. The as-deposited device had a columnar and dense structure and no voids were observed. However, Kr also caused gas bubble formation which coalesces during the $CdCl_2$ treatment. After the $CdCl_2$ activation process, extensive void formation was observed within the CdTe layer and at the CdS/CdTe junction. The Kr bubbles were smaller than those observed in the CdTe device deposited using Ar.

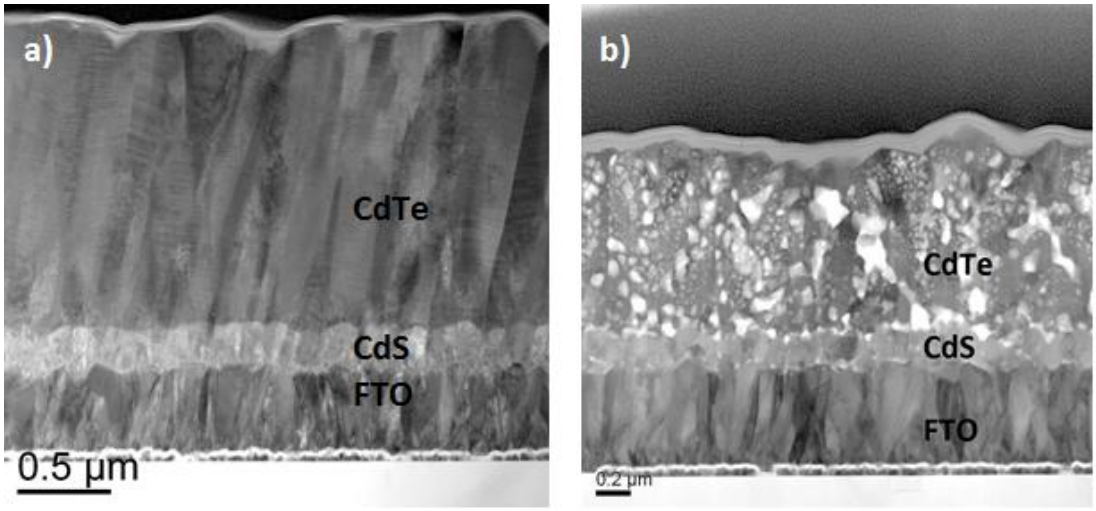


Figure 6-4 TEM cross section images of a) an as-deposited CdS/CdTe device using Kr as the magnetron working gas, b) following the CdCl2 activation treatment. The CdTe device was deposited at 250 ºC using 20 sccm Kr working gas and this was followed by the CdCl2 treatment at 400 ºC for 6 min.

Figure 6-5 shows the EDX analysis of an as-deposited thin film CdTe solar cell, sputtered using Kr. The grains were similar to the CdTe devices deposited using Ar

and the spectra indicates ~3 at% Kr was present in the CdTe layer. There was only 0.5 at% Kr in the CdS layer which does not show a negative effect on the CdS layer.

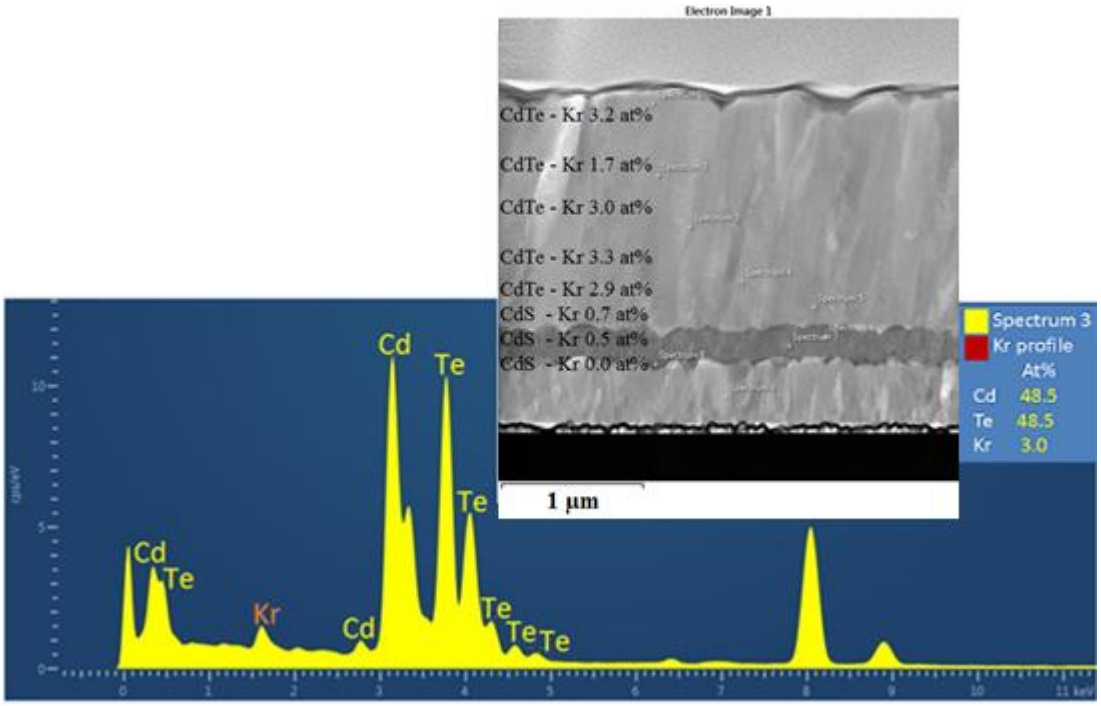


Figure 6-5 EDX analysis of a CdS/CdTe solar cell deposited at 250 ºC using 20 sccm Kr working gas

Figure 6-6 shows an EDX elemental map of the CdTe solar cell deposited using Kr, followed by the $CdCl_2$ activation process. The image shows that 1 at% Kr was observed after the $CdCl_2$ activation process. There was 2 at% Kr close to the CdTe surface. There was less amount of Kr observed in the CdTe layer after the $CdCl_2$ treatment. This can be explained with the annealing the samples which may release the trapped gas in the CdTe layer.

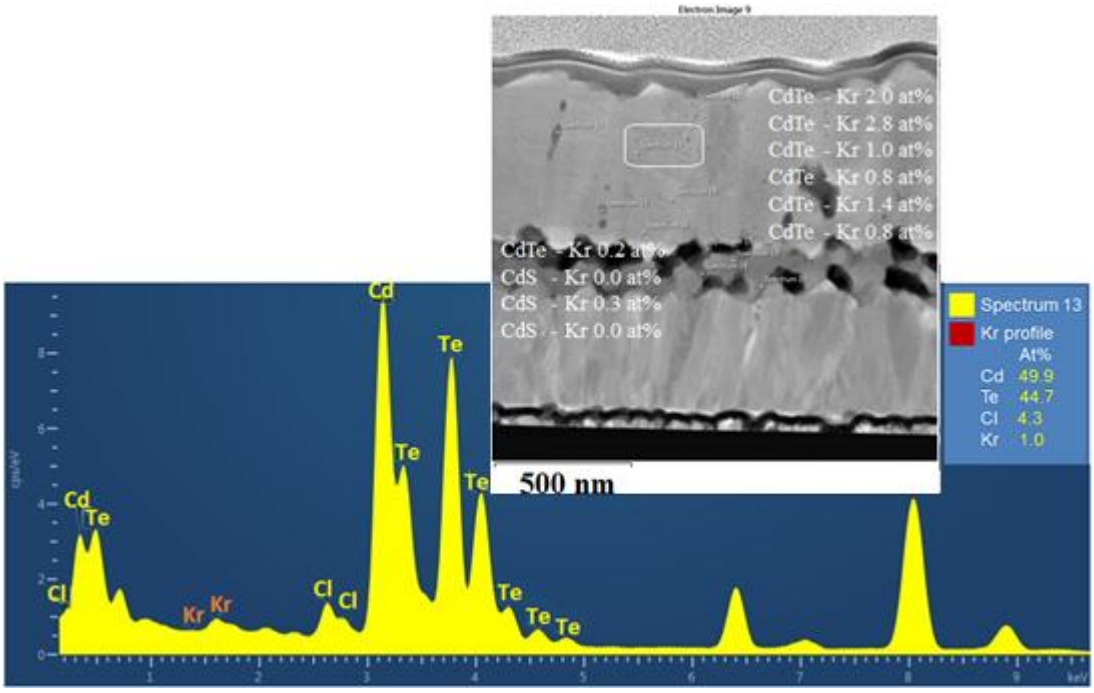


Figure 6-6 EDX analysis of a CdS/CdTe device deposited at 250 ºC using 20 sccm Kr working gas following the $CdCl_2$ treatment at 400 ºC for 6 min.

Figure 6-7 shows an EDX analysis of another $CdCl_2$ treated thin film CdTe solar cell deposited with Kr. The image indicates that there were high densities of Kr gas trapped in thin film CdTe solar cell and had formed small bubbles (shown in red in the image). Moreover, there were voids observed at the CdS/CdTe interface and bubbles were observed within the CdTe crystals. Although 4.3 at% of Cl was detected in the CdTe layer, CdTe grains did not recrystallize. There was ~5 at% of Kr observed after the $CdCl_2$ treatment.

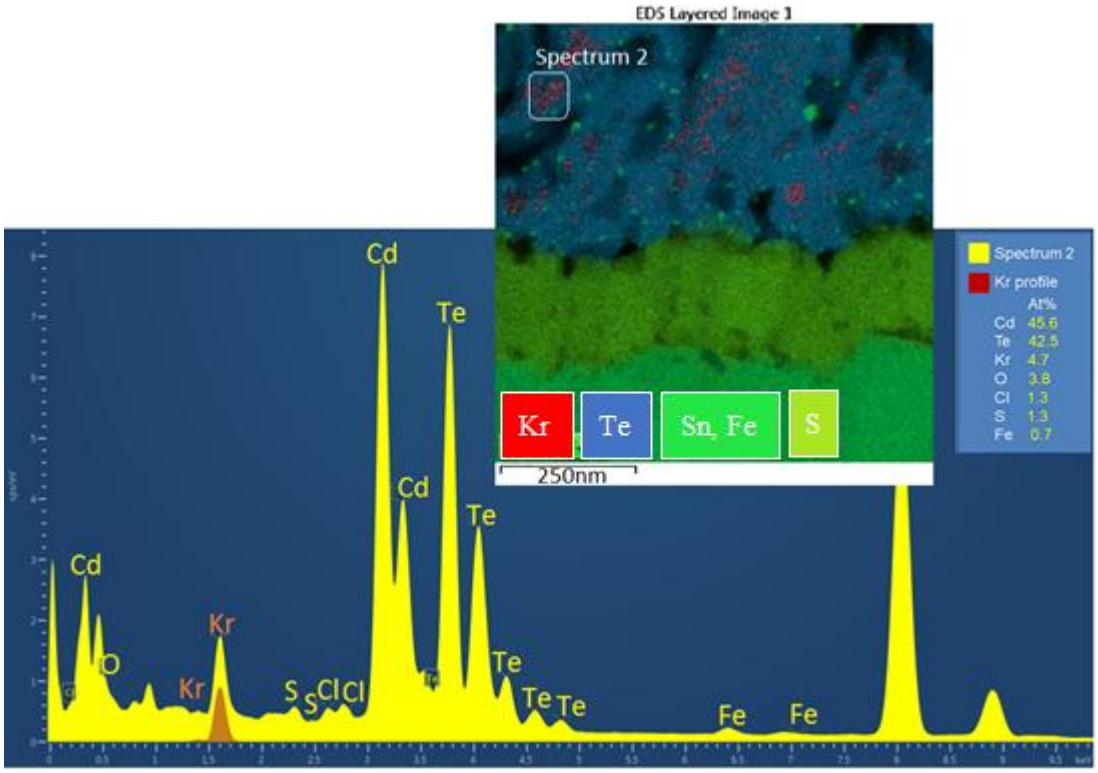


Figure 6-7 EDX analysis of a CdS/CdTe device deposited 250 ºC using 20 sccm Kr working gas following the $CdCl_2$ treatment at 400 ºC for 6 min.

6.3.4. Using of Ne as the working gas

A thin film CdS/CdTe solar cell was deposited using Ne as the magnetron working gas, which has lower atomic mass than Cd and Te and is lighter than Ar and Kr. The substrate temperature was maintained at 250 ºC and the gas flow at 20 sccm during the deposition. Figure 6-8 shows a TEM cross-section of the CdS/CdTe solar cell, deposited using Ne followed by the $CdCl_2$ activation process. After the $CdCl_2$ treatment, severe voids formation was observed. A high density of large voids was observed on the CdTe layer.

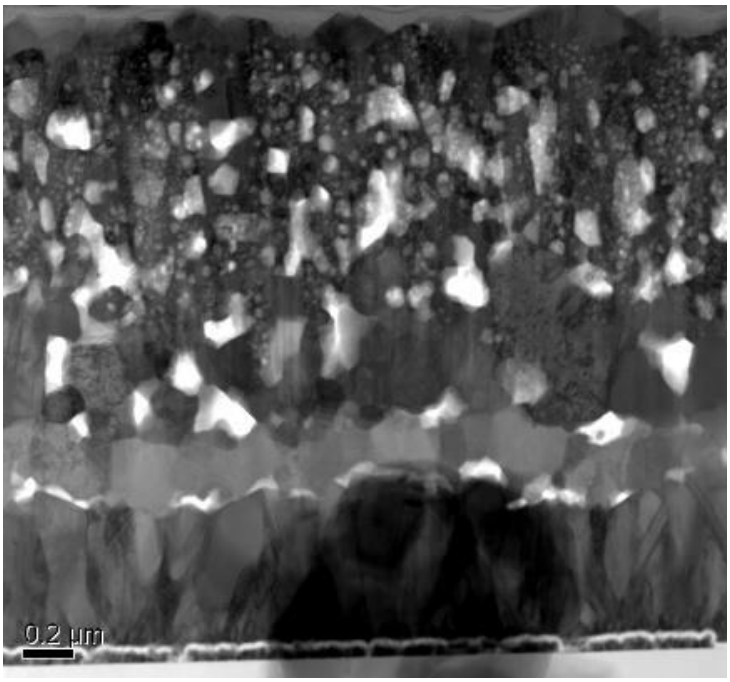


Figure 6-8 A TEM cross-section of thin film CdS/CdTe stack deposited at 250 ºC using 20 sccm Ne working gas followed by the $CdCl_2$ activation treatment at 400 ºC for 6 min.

In Figure 6-9, EDX analysis of the $CdCl_2$ treated CdTe solar cells shows that Ne was present in the CdTe layer, which caused bubble, void and blister formations.

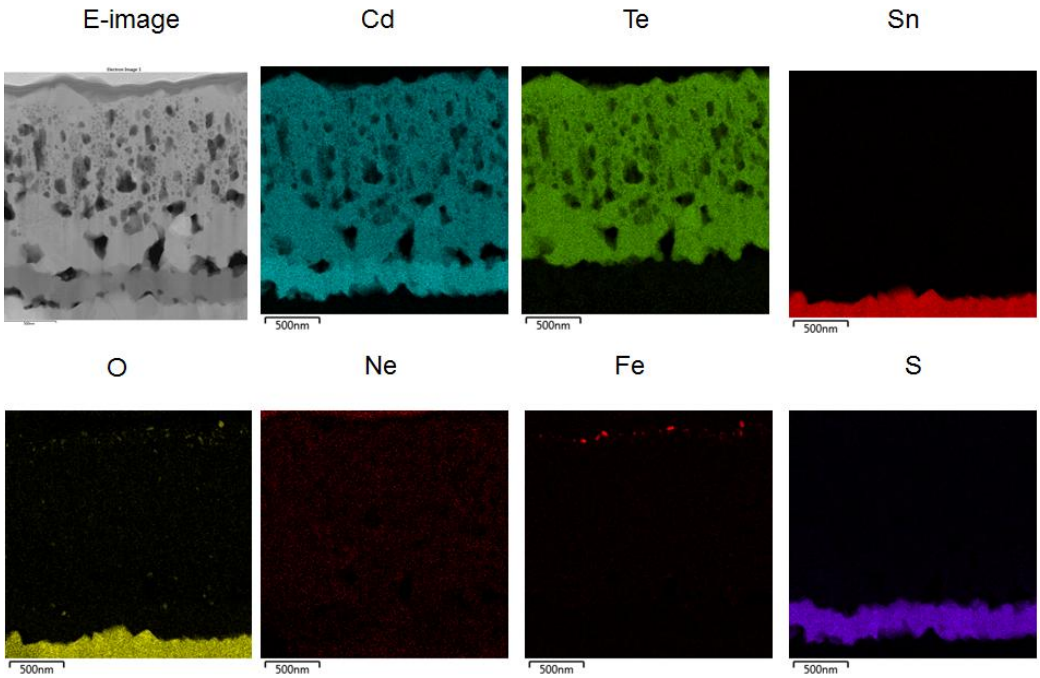


Figure 6-9 STEM EDX chemical distribution maps of a thin film CdS/CdTe solar cell deposited at 250 ºC using 20 sccm Ne working gas followed by $CdCl_2$ treatment at 400 ºC for 6 min.

6.4. Discussion and Conclusions

For investigating the damage of Ar, Ne, and Kr gases on the CdTe layer during the $CdCl_2$ activation process, as-deposited and $CdCl_2$ treated CdTe solar cells deposited by pulsed DC magnetron sputtering have been analysed with TEM. No voids were observed on the as-deposited sputtered CdTe devices with Ar; however, there was about 4 at% Ar found in the CdTe layer on EDX analysis. The results have shown a spatial distribution in the CdTe layer and Ar concentration was higher close to the film surface. During the $CdCl_2$ treatment voids appeared on the CdTe layer and delamination occurred at the CdS/CdTe junction. In Chapter 5, it was discovered that

Ar in the as-deposited cells coalesced into Ar bubbles after RTP annealing. Blisters and voids were formed after $CdCl_2$ activation process.

For an industrially viable sputtering process, mitigating the mechanism which causes blistering and void formation is essential if uniform and stable thin film CdS/CdTe solar cells are to be deposited. To eliminate the bubble or blister formation issue, thin CdTe layers were deposited by pulsed DC magnetron sputtering using, Ne and Kr as the magnetron working gas. The as-deposited CdTe device was in each case dense and columnar. The working gas was also trapped in the CdTe lattice when using Kr and Ne. This issue becomes more severe if inert gases of lower mass are used. The level of gas trapping can be controlled by lowering the energy of the Ar ions by the target voltage in the magnetron plasma; however, it is not an absolute solution. Similar problems have been reported on the blistering of different sputtered materials after the annealing process. Blistering on CZTS devices prepared by magnetron sputtering was studied recently, a correlation was found between the amount of blistering and the amount of trapped gas [158].

The next chapter will examine the effect of Xe as the working gas during CdTe layer deposition with pulsed DC magnetron sputtering.

CHAPTER VII

7. Pulsed DC Magnetron Sputtering of CdTe with xenon as the working gas

7.1. Introduction

Ar and Xe ion beam sputtering were compared during the deposition CdTe and ZnS layers. Due to the backscattered ion energy during deposition, Ar samples had higher stress. Therefore, there was less compressed stress on the substrate deposited with Xe beam. [161]

Ar is the standard working gas used in magnetron sputtering. In Chapter 6, Ne and Kr gases were used as the magnetron working gas. This is due to the bubble and blister formation in thin films CdS/CdTe solar cells deposited with Ar. However, the

solar cells deposited using Ne were worse than the CdTe devices deposited using Ar (Figure 6-8). Thin film CdTe solar cells deposited using Kr were better than the films deposited using Ar, however voids and blisters still formed in the device (*Figure 6-4*). Therefore, Xe was used to deposit CdTe layer. Xe has the highest atomic mass of all the inert gases, other than radon (Rn), shown in Figure 7-1.

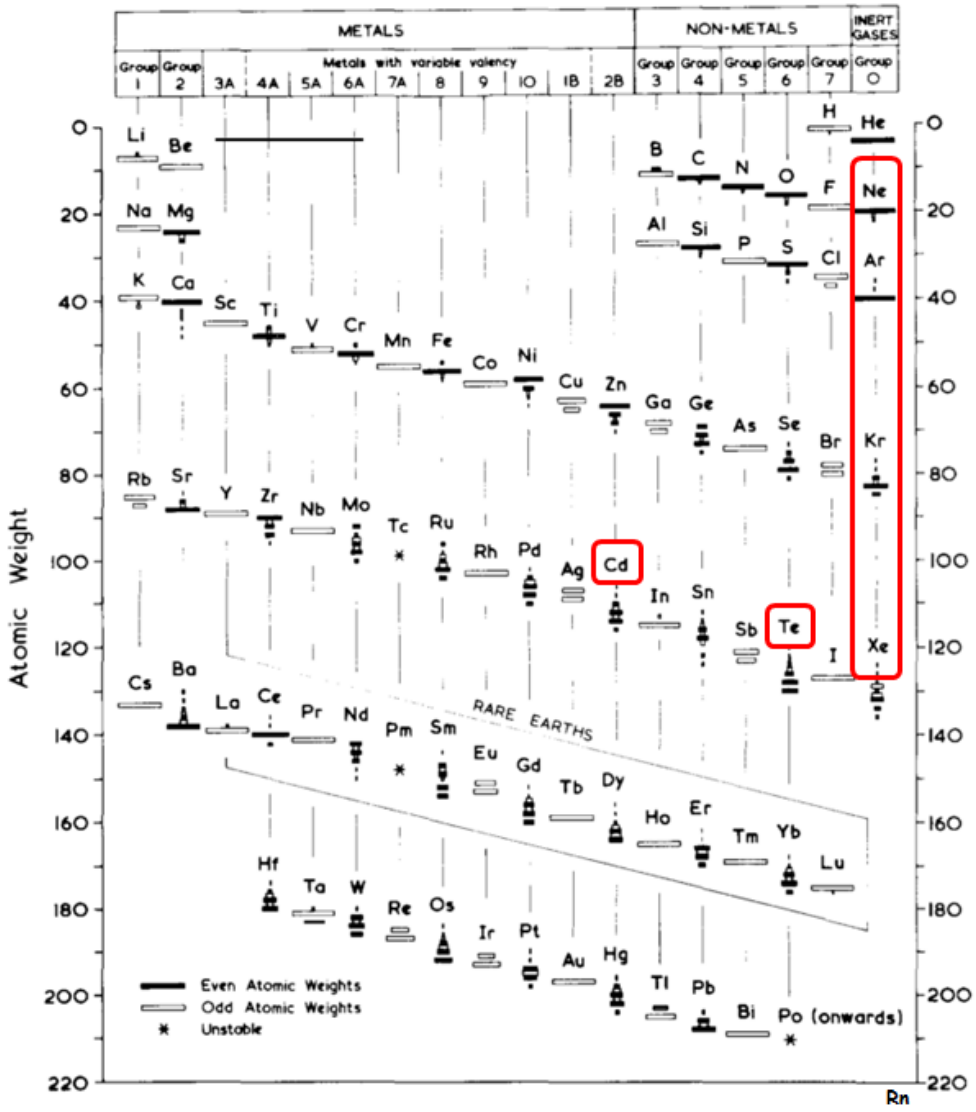


Figure 7-1 Periodic table of stable isotopes after Miledge [198]

7.2. Experimental

7.2.1. Magnetron Sputtering

Table 7-1 Synthesis conditions for CdTe deposition using pulsed DC magnetron sputtering

CdTe deposition conditions	
Deposition rate (nm/s)	2.8, 3.4, 3.1, 2
CdTe thickness (µm)	1
Substrate temperature (°C)	RT, 250, 400, 450 (static)
Magnetron working gas	Xe
Flow rate (sccm)	10, 20
Pressure (µbar)	1, 1.5

The deposition of a 1 µm thick CdTe layer was carried out using Xe as the working gas at 250 °C, without breaking the vacuum. During the sputtering process the target voltage was ~800 V and the gas flow rate was 20 sccm. For devices sputtered using Xe the deposition rate was 3.4 nm/s.

The static deposition rates for CdTe devices deposited using 10 and 20 sccm Xe flow rates were measured and shown in Figure 7-2. The results show that depositing at 20 sccm Xe flow rate results in a higher deposition rate compared to depositing at 10 sccm. In Figure 7-3 the measured static deposition rates of CdTe solar cells, deposited at different substrate temperatures are indicated. The highest deposition rate was at a temperature of 250 °C.

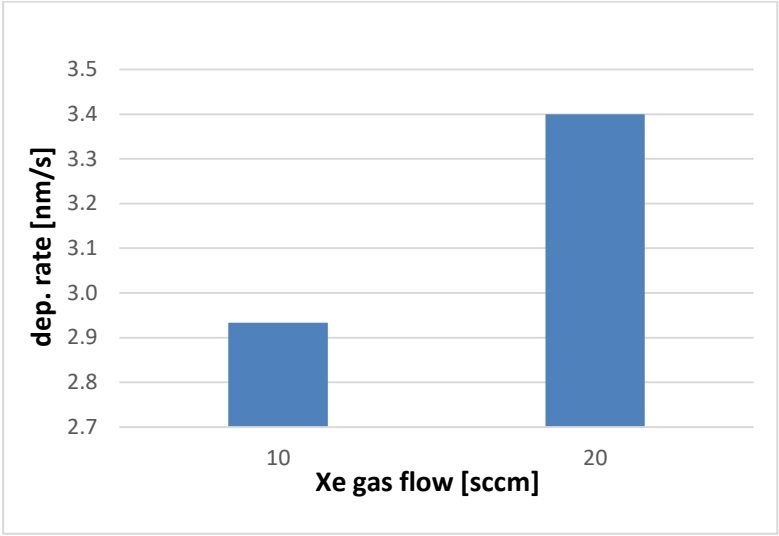


Figure 7-2 Static deposition rates measured for thin film CdTe solar cells deposited using 10 sccm and 20 sccm Xe magnetron working gas flows at 250 °C

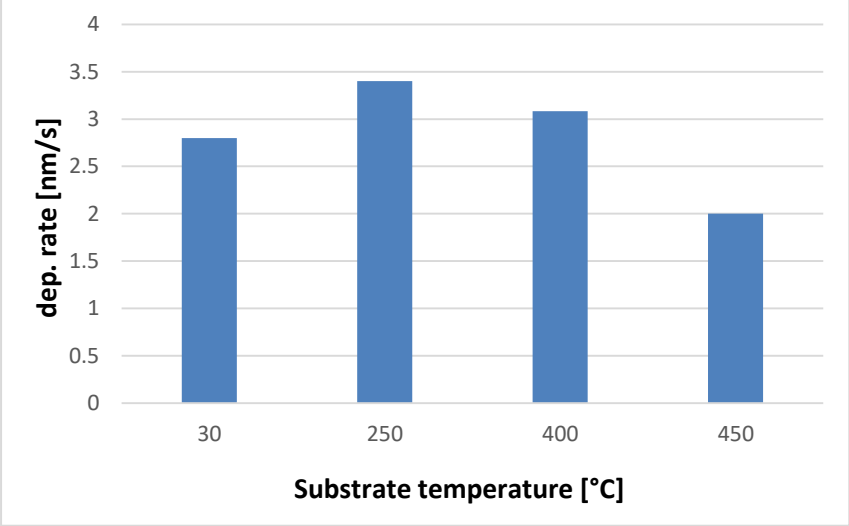


Figure 7-3 Static deposition rates measured for thin film CdTe solar cells deposited using 20 sccm Xe magnetron working gas at different substrate temperatures

7.2.2. $CdCl_2$ Activation Process

Table 7-2 $CdCl_2$ activation process parameters for CdTe devices deposited using Xe as the magnetron working gas

$CdCl_2$ treatment Vapour deposition in a tube furnace	
Annealing time (min)	6
Annealing temperature (°C)	400, 415

Thin film CdS/CdTe devices were annealed at 400 °C and 415 °C for 6 min using a $CdCl_2$ vapour treatment.

7.3. As-deposited CdTe using Xe as the working gas

Deposition conditions for sputtering CdS layers using Ar as the working gas was established by Lisco [104]. Xe was used as the magnetron working gas during CdTe deposition to avoid the bubble or blister formation. A switching valve connected to the system was used to switch the working gas between Ar and Xe. A MFC was used to monitor and control the flow rates of the magnetron working gas.

The substrate temperature was 250 ºC and the gas flow was maintained at 20 sccm during the CdTe layer deposition. A cross sectional TEM image of an as-deposited thin film CdS/CdTe solar cell is shown in Figure 7-4. The as deposited device had a columnar and dense structure and no voids were observed.

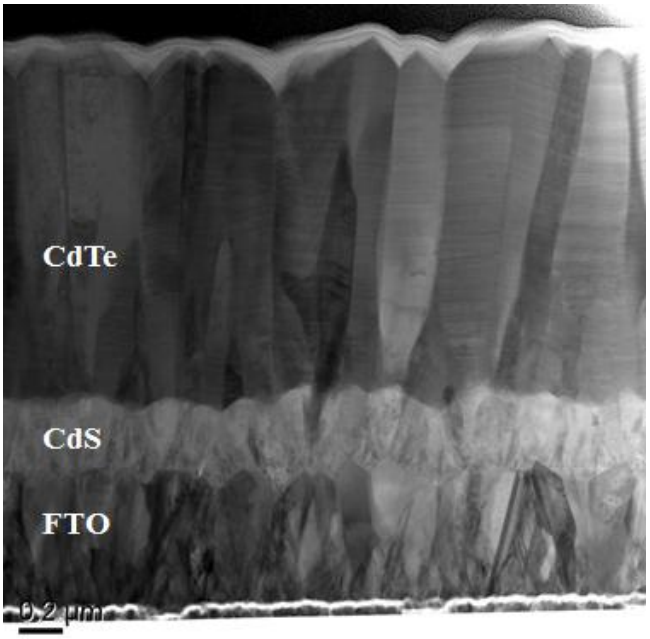


Figure 7-4 TEM cross section image of an as-deposited CdS/CdTe device using 20 sccm Xe working gas at 250 °C

Figure 7-5 shows the EDX spectra of an as-deposited CdTe solar cell sputtered using Xe. The spectra indicated that Xe was not detectable in the CdTe layer within the detection limits of the EDX technique.

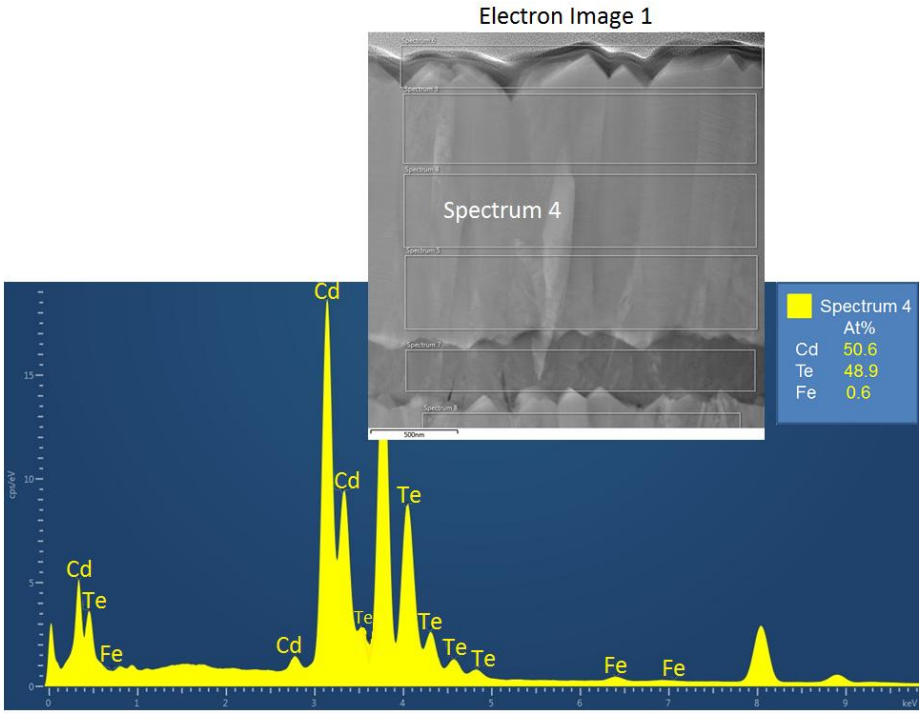


Figure 7-5 EDX analysis of as deposited thin film CdS/CdTe solar cell using 20 sccm Xe working gas at 250 °C

The as deposited device was activated with $CdCl_2$ at 415 ºC for 6 min. SEM images of treated CdS/CdTe device are shown in Figure 7-6. There were no blisters observed after the $CdCl_2$ activation process.

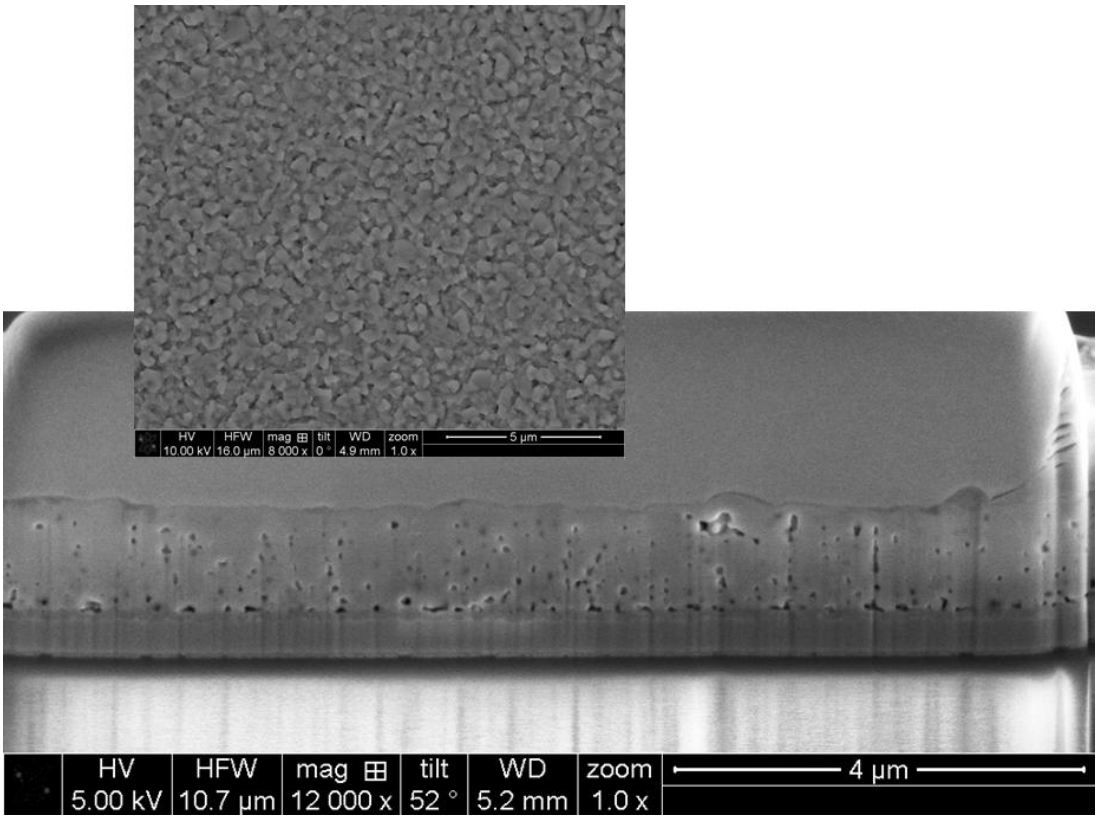


Figure 7-6 SEM images of thin film CdS/CdTe solar cell deposited by pulsed DC magnetron sputtering using 20 sccm Xe magnetron working gas at 250 °C and $CdCl_2$ treated at 415 ºC for 6 min.

In Figure 7-7, Bright Field STEM and High angle annular dark field STEM images of the cross-section of CdS/CdTe solar cells were obtained. No voids were visible in the CdTe layer after the $CdCl_2$ treatment, but Cl was observed at the GBs and at the CdS/CdTe interface.

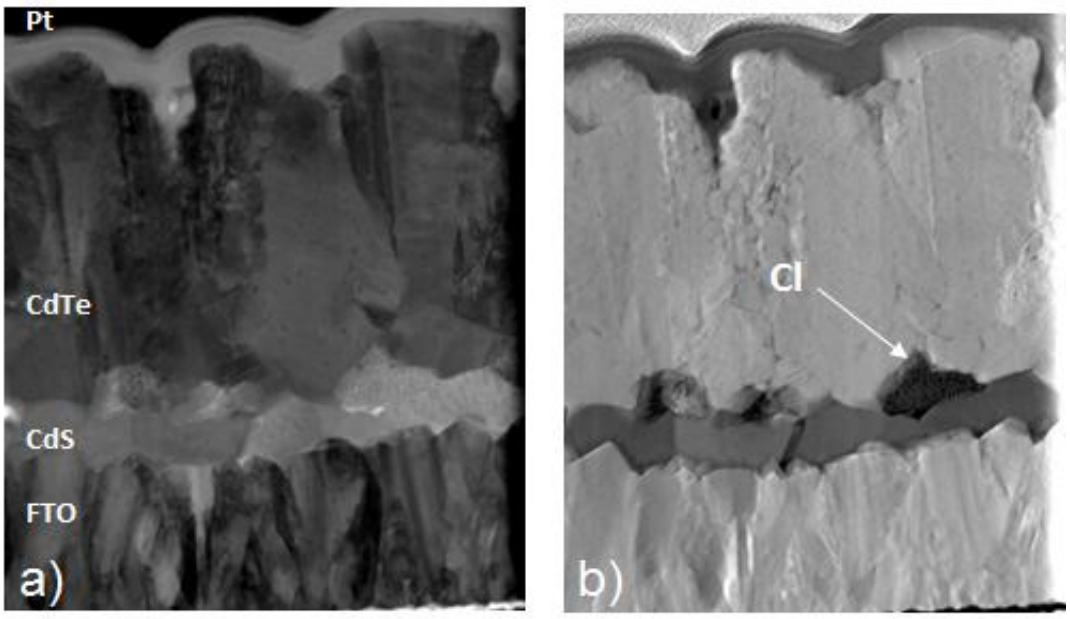


Figure 7-7 a) Bright Field STEM image and b) High angle annular dark field STEM image of cross-section of CdS/CdTe solar cells using Xe as the working gas for the CdTe layer and Ar for the CdS layer. CdTe layer was deposited using 20 sccm Xe magnetron working gas at 250 °C and $CdCl_2$ treated at 415 ºC for 6 min.

7.4. Conclusions

The aim of this chapter was to deposit a defect and void free CdTe layer. There were no defects observed in the as–deposited and $CdCl_2$ treated CdS layers deposited using Ar during the sputtering process. Uniform ~1 µm thick CdTe solar cells were deposited by pulsed DC magnetron sputtering using Xe as the magnetron working gas. TEM was used for investigating the effect of Xe gas on the CdTe layer before and after the $CdCl_2$ activation process. No voids were observed on the as deposited sputtered CdTe devices and no gas entrapment found in the CdTe layer using EDX

analysis. No voids were observed on the CdTe solar cell during the $CdCl_2$ treatment, however, Cl was detected at the CdS/CdTe junction.

It was found that Xe reduces gas entrapment in the as deposited material. This prevents blister formation and delamination issues following the $CdCl_2$ activation process. Blister formation has been a huge problem for sputtered CdTe devices. Using Xe as the working gas has the potential to overcome this problem. Nevertheless, there is still a lot of work required to optimize the deposition and annealing processes to improve the efficiency and quality of CdS/CdTe devices.

CHAPTER VIII

8. Conclusions and Future Studies

Renewable energy technologies are becoming more popular due to the high cost and insecurity of fossil fuel supplies. PV technology is one of the most important technologies available to produce clean energy. There are two technologies dominating the PV market; c-Si and thin film. Thin film technology is popular due to its reduced material usage and competitive cost. In this work, thin film CdTe solar cells were deposited by pulsed DC magnetron sputtering [193], a new technique which is industrially scalable and provides uniform coatings. This deposition technique has not been used to deposit thin film CdTe solar cell previously.

Figure 8-1 shows the thesis structure. Characterisation methods including SEM, TEM, HR-TEM, and EDX were used to analyse the microstructure of the sputtered CdTe devices, voltage measurements were used to ascertain the electrical performance of the devices.

A series of experiments used to optimise the $CdCl_2$ activation process is presented. Thin film CdTe solar cells require a $CdCl_2$ activation process to improve conversion efficiencies. The role of this activation process is to increase the grain size, remove stacking faults and pacify the GBs. Therefore, three different techniques for the $CdCl_2$ treatment were compared to improve the cell performance. Evaporation and wet chemical treatments were found to be quite aggressive for the CdTe devices deposited with pulsed DC magnetron sputtering with Ar as the working gas. Evaporation in a tube furnace resulted in higher voltage measurements, however, blister formation on the film surface and large void formation in the CdTe layer was observed after the $CdCl_2$ activation process.

It is believed that voids at the CdS/CdTe junction cause delamination. Using annealing and eliminating the presence of Cl, small defects were observed along the CdS/CdTe interface and at the GBs. The defects were spherical in shape and ~5 nm in diameter. Strain analysis of thin film CdS/CdTe solar cells was carried out to prevent the formation of defects such as delamination and void formation [72]. However, even though the strain was eliminated the defects still existed [199]. After simply annealing the CdTe devices at various temperatures, bubble formation was observed in the CdTe layer at the atomic scale [200]. Using HR-TEM, it has been discovered that trapped Ar, which was used as the working gas during deposition, diffuses through the lattice to form the bubbles during the annealing process with RTP. Moreover, EDX analysis showed a high concentration of Ar in the as deposited

devices. Subsequently the Ar bubbles coalesced and formed large surface blisters. Void formation was observed in the CdTe layer after the $CdCl_2$ treatment.

Ar atoms diffused and coalesced as the temperature increased. Ar diffused and formed small bubbles that developed into blisters or perforated blisters on the film surface. Exfoliation occurred at some of the surface blisters.

Ar was replaced with Kr and Ne in an attempt to eliminate the bubble and blister formation [200]. However, bubble formation was observed with both of these alternative gases. The use of a gas that has an atomic mass greater than that of CdTe, such as Xe as the working gas during magnetron sputtering, was found to reduce the inclusion of the working gas into the CdTe layer. No voids were visible in the Xe sputtered CdTe devices and no Xe gas entrapment was found in the CdTe layer. There are no voids observed on the $CdCl_2$ treated CdTe solar cell. Bright field STEM image and dark field STEM image showed that the CdTe layer deposited in the presence of Xe as the working gas had no gas bubbles or voids. It was discovered that Xe avoids gas entrapment in the as deposited material. This avoids blister formation and delamination following the $CdCl_2$ treatment. It was identified that a quality CdS/CdTe device can be formed by the selective use of a first gas, such as Ar, as the working gas during the deposition of the CdS layer as it is already optimised by Lisco [104] and a second gas, such as Xe, as the working gas during the deposition of the CdTe layer.

The mechanism that explains the blistering of sputtered CdS/CdTe solar cells has been discovered. However, there is still a lot of work required to optimize the

deposition and annealing processes. This optimisation could further improve the efficiency and quality of thin film CdS/CdTe solar cells deposited by pulsed DC magnetron sputtering. In order to do this, the following work is necessary.

- The deposition conditions of thin film CdTe, deposited by pulsed DC magnetron sputtering using Xe as the working gas needs to be optimised.
- The $CdCl_2$ activation process needs to be optimised for sputtered CdTe devices.

It is likely that these steps will lead to highly efficient thin film CdTe solar cells.

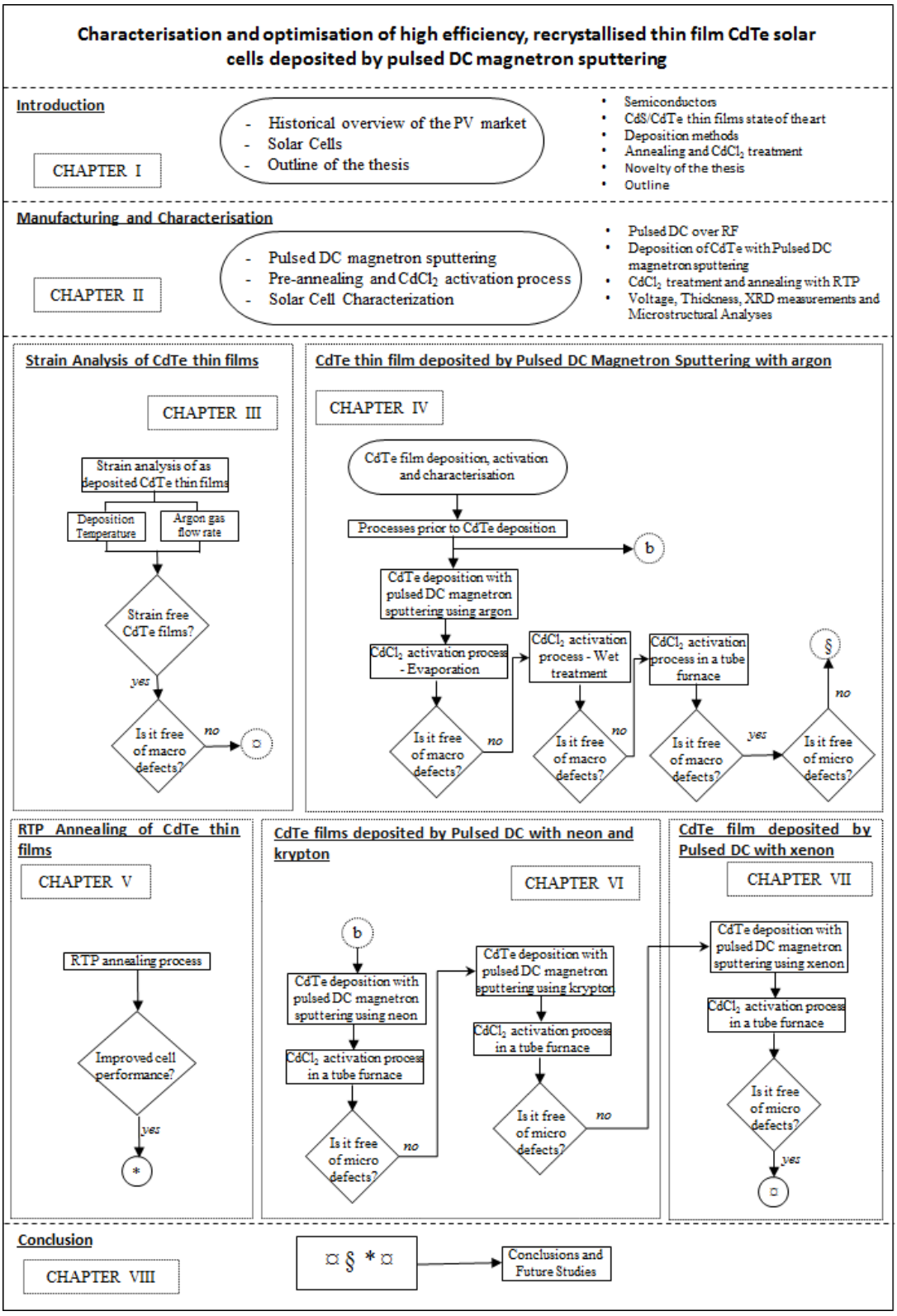


Figure 8-1 Thesis structure

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